The prospects for 10 nm III-V CMOS

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ABSTRACT

The increasing difficulties for further scaling down of Si CMOS is bringing to the fore the investigation of alternative channel materials. Among these, III-V compound semiconductors are very attractive due to their outstanding electron transport properties. This paper briefly reviews the prospects and the challenges for a III-V CMOS technology with gate lengths in the 10 nm range.

INTRODUCTION

CMOS scaling is at the heart of the microelectronics revolution. The ability of Si CMOS to continue to scale down transistor size while delivering enhanced performance is becoming increasingly difficult with every generation of technology. For Moore's law to reach beyond the limits of Si, a new channel material with a high carrier velocity is required. A promising family of materials for this is III-V compound semiconductors.

III-Vs are well known for their unique suitability for high frequency electronics. III-V-based ICs are currently in use in a variety of communications and defense applications: some are mission critical, such as space systems where exceedingly high reliability is essential; others are mass-market and very cost-sensitive applications such as power amplifiers for smart phones. The prospect of III-Vs entering the logic roadmap is tantalizing. The requirements are daunting, yet the payoff is huge. This work reviews some of the critical issues.

THE PROSPECTS FOR III-V CMOS

A way for us to assess the prospects for a future III-V CMOS technology with gate lengths in the 10 nm range consists on learning from today's devices. The High-Electron Mobility Transistor (HEMT), in itself a device with near THz capabilities, represents an excellent model system. At MIT, for the last few years, we have been investigating the logic characteristics of scaled-down InGaAs and InAs HEMTs. We have fabricated devices down to 30 nm in gate length that exhibit logic characteristics (in terms of current drive and short-channel effects) that rival those of state-of-the-art Si MOSFETs of equivalent gate lengths. This can be best seen in Fig. 1 which graphs the ON current for an OFF current of 100 nA/um at a V_{DD} of 0.5 V as a function of gate length. Shown in that graph are data for InGaAs and InAs channel HEMTs down to 30 nm in gate length [1-2]. Also in the figure are representative Si CMOS data from the most recent technology generations [3], as well as projections based on the International Technology Roadmap for Semiconductors. It is clear from this graph that today, InAs-channel HEMTs prototyped in a university environment significantly outperform state-of-the-art Si MOSFETs of similar gate length. The difference is more startling when we realize that the Si MOSFETs have a source resistance in the range of 80 ohm.um, while for the InAs HEMTs, R_s is about 230 ohm.um. Clearly, great improvements should be feasible if the extrinsic portion of the device is properly engineered. How far, in fact, could III-Vs go?

In order to answer this question, we have recently carried out an extraction of the electron injection velocity at the virtual source [4]. This is the velocity that matters to determine the current in a MOSFET in saturation. As shown in Fig. 2, values in excess of 3×10^7 cm/s are obtained for 30-40 nm gate length devices operating at V_{DS}=0.5 V. The injection velocity increases with the InAs mole fraction in the channel of the device. These values are twice as high as for strained Si at less than half the operating voltage.

A significant concern about the use of low-effective mass materials in the channel is their small density of states (DOS) and corresponding low quantum capacitance. This would blunt the scaling of the vertical dimensions of the FET and its overall scalability [5]. We have recently carried out a theoretical and experimental study of gate capacitance in advanced InGaAs and InAs HEMTs. We have found that the non-parabolicity of the conduction band coupled with channel quantization and biaxial compressive strain results in a significant increase in the DOS effective mass and the sheet charge density in the channel. We project that at the 10 nm gate length level and operating at V_{DD}=0.5 V, a sheet carrier density in the mid 10^{12} cm^{-2} range is eminently feasible [6].

The combination of these two recent results, injection velocity and scaled gate capacitance, suggests that a 10 nm gate length high-K dielectric III-V MOSFET with a thin InAs channel should be capable of reaching a drive current of about 1.5 mA/um, if a source resistance of 80 ohm.um can be attained, as it is possible today in Si. This is well in excess of the most optimistic scenario for Si CMOS.

THE CHALLENGES FOR III-V CMOS

Reaching the target outlined in the previous paragraph presents daunting challenges. Until recently, the development of a high-K dielectric gate technology with a

high-quality semiconductor interface was the greatest concern. Recent research suggests that this is an eminently attainable goal [7]. Transistor scalability is also a major worry. Will it be possible to scale to the required dimensions while preserving short-channel effects and attaining the demanding parasitic resistance objective? This is a topic that will call for extensive experimental and simulation research. Fortunately, calibrated simulators today reproduce quite well the characteristics of 30 nm gate length HEMTs and should be valuable in projecting to devices in the 10 nm range [8]. If planar device designs are unsuitable, 3D designs might offer a viable path. The recent demonstration of an InGaAs FinFET gives hope that this is a viable strategy [9]. A future III-V CMOS technology will have to "look and feel" as much as Si as possible. This calls for the epitaxial growth of thin high-quality III-V layers on top of large Si wafers. In fact, depending on what emerges as the best option for the p-channel device, a major challenge in itself, two dissimilar materials might need to be integrated side by side in very close proximity on top of a Si wafer.

Acknowledgements

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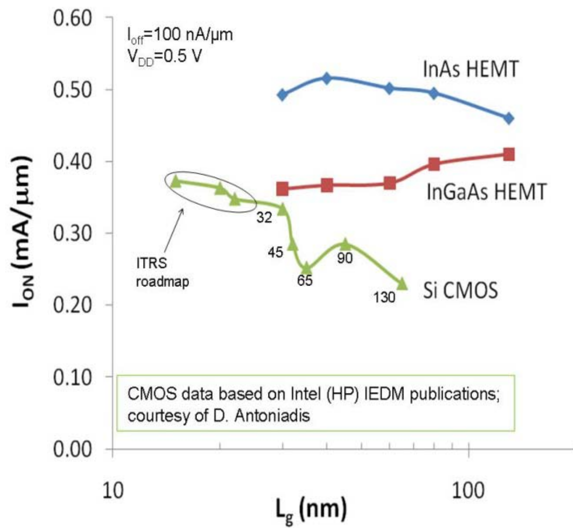

Fig. 1: I_{on} for I_{off}=100 nA/um at V_{DD}=0.5 V as a function of gate length for InGaAs and InAs HEMTs [1,2]. For reference, recent scaled Si CMOS technologies are also shown. These results are courtesy of D. Antoniadis [3] and are based on projections of Intel's HP CMOS technologies presented at IEDM. Also added are projections from the International Technology Roadmap for Semiconductors.

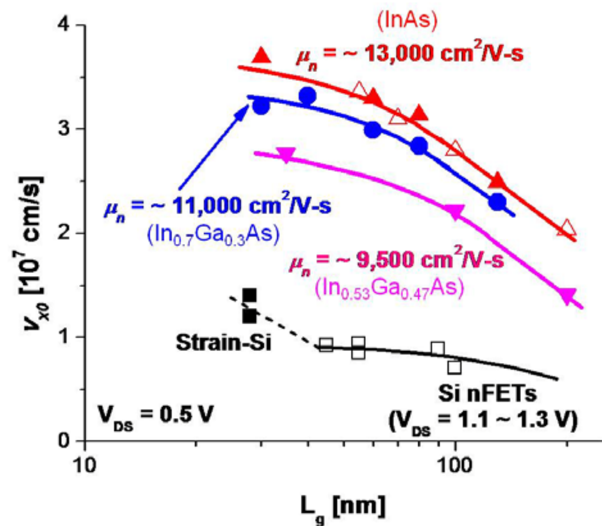

Fig. 2: Injection velocity at the virtual source in InGaAs and InAs HEMTs as a function of gate length at V_{DD}=0.5 V [4]. For reference, results from bulk and strained Si CMOS are included (V_{DD}=1.1-1.3 V) [4].