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# Design of a CMOS readout circuit on ultra-thin flexible silicon chip for printed strain gauges

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**Abstract.** Flexible electronics represents an emerging technology with features enabling several new applications such as wearable electronics and bendable displays. Precise and high-performance sensors readout chips are crucial for high quality flexible electronic products. In this work, the design of a CMOS readout circuit for an array of printed strain gauges is presented. The ultra-thin readout chip and the printed sensors are combined on a thin Benzocyclobutene/Polyimide (BCB/PI) substrate to form a Hybrid System-in-Foil (HySiF), which is used as an electronic skin for robotic applications. Each strain gauge utilizes a Wheatstone bridge circuit, where four Aerosol Jet® printed meander-shaped resistors form a full-bridge topology. The readout chip amplifies the output voltage difference (about 5 mV full-scale swing) of the strain gauge. One challenge during the sensor interface circuit design is to compensate for the relatively large dc offset (about 30 mV at 1 mA) in the bridge output voltage so that the amplified signal span matches the input range of an analog-to-digital converter (ADC). The circuit design uses the 0.5 µm mixed-signal GATEFOREST™ technology. In order to achieve the mechanical flexibility, the chip fabrication is based on either back thinned wafers or the ChipFilm™ technology, which enables the manufacturing of silicon chips with a thickness of about 20 µm. The implemented readout chip uses a supply of 5 V and includes a 5-bit digital-to-analog converter (DAC), a differential difference amplifier (DDA), and a 10-bit successive approximation register (SAR) ADC. The circuit is simulated across process, supply and temperature corners and the simulation results indicate excellent performance in terms of circuit stability and linearity.

## 1 Introduction

Flexible electronics is an emerging technology driven by its unique characteristics such as mechanical flexibility, thin form factor, the feasibility to be spread over large areas and many other novel capabilities (Sekitani et al., 2010; Harendt et al., 2014; Khan et al., 2015). In this context, high-end flexible electronic applications require high performance silicon chips for implementing different functions such as sensors interfacing, data acquisition and wireless data transmission systems. The minimum chip thickness and mechanical flexibility features are also desirable for several emerging applications such as bio-medical implants, electronic skin, Hybrid Systems-in-Foil and flexible displays (Burghartz et al., 2009). For example, the minimum chip thickness provides the capability to have an implantable bio-sensors platform (Nawito et al., 2015; Kim et al., 2013). In addition the mechanical flexibility of the ultra-thin silicon chip is utilized to implement a stress sensor chip, where on-chip MOS transistors oriented in different directions act as sensing elements, while implementing a relatively stress-insensitive readout circuit (Mahsereci et al., 2016; Kuhl et al., 2013).

In this work, the design of an ultra-thin readout silicon chip for an array of printed strain gauges is presented. The sensor readout chip is embedded in a thin BCB/PI foil substrate, while the strain gauges are printed on top of it (Hassan et al., 2013). The combination of the large-area and low-cost printed electronics with the fast and mature silicon chip technology forms a Hybrid System-in-Foil (HySiF), which represents the complementary advantages of both technologies and is used in this work as an electronic skin for robotic applications.

The main motivation behind this work is presented in Sect. 1. Section 2 explains the design, fabrication and characterization of the printed strain gauges. Additionally, Sect. 3 discusses the implementation of the readout interface chip and overviews its architecture and different building blocks. Finally, Sect. 4 concludes the main findings of this work.

## 2 Printed strain gauges

The principle of using the electrical resistance change to measure the strain distribution has been known for more than a century and is widely used nowadays in different fields such as bio-medical and aerospace applications (Wen et al., 2005; Stephen et al., 2004). This principle is utilized herein, where strain gauges are used to monitor the bending activity of the electronic skin.

### 2.1 Printing technology

Aerosol Jet® printing technique, also known as maskless mesoscale material deposition ($M^3D$), is utilized in this work to print the strain gauges on the BCB/PI substrate (Hedges et al., 2005; Paulsen and Renn, 2014). In this technology, the silver ink is atomized and converted into a dense aerosol, which is transported to the print head using an inert carrier gas. The print head focuses the aerosol resulting in a high-velocity jet, which is capable of creating a compact and high-resolution printing with a minimum feature size of 10 µm. Figure 1 shows four printed resistors in a Wheatstone bridge configuration to form one strain gauge on a BCB/PI substrate.

This printing technique has a main drawback, which is the variation between the horizontal and vertical printing directions. Minor impurities such as ink droplets or particles may accumulate near the nozzle tip of the print head during the printing causing a deviation of the ideally circular aerosol jet shape towards an elliptical geometry. This results in level variations in the silver ink density while printing in the vertical and horizontal directions. Consequently, a mismatch takes place between the resistance values of the vertically and horizontally printed meanders. This effect is illustrated by the scanning electron microscope (SEM) images of both the horizontal and vertical lines shown in Fig. 1. This mismatch between the strain gauge resistances results in an offset voltage between the output voltage of the strain gauge bridge circuit.

### 2.2 Sensor Design

As shown in Fig. 1, the Wheatstone bridge circuit is connected across two potentials, one is the supply voltage $V_S$ and the other is low potential $V_L$, where a constant biasing current is connected. It has two output terminals $V_1$ and $V_2$, which are equal when the bridge is balanced. The bridge is balanced when the ratio of the two resistors in one branch

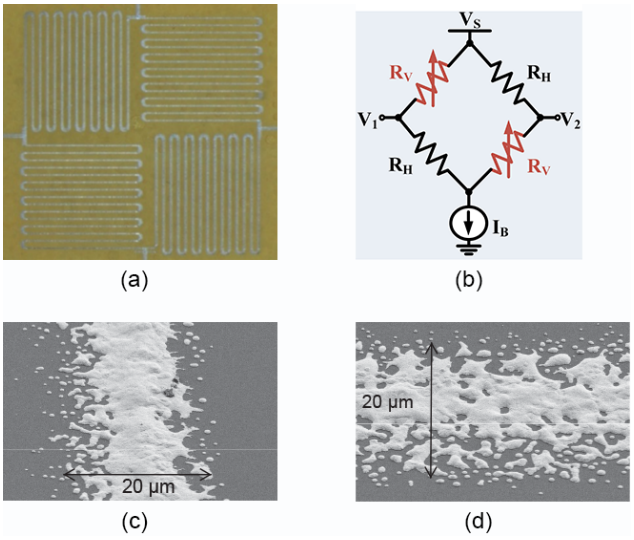


**Figure 1. (a)** Photograph of four meanders printed using silver ink on BCB/PI substrate. The Wheatstone bridge circuit is utilized in which two strain gauges are printed vertically ($R_V$), while the other two are printed horizontally ($R_H$). The line width is 20 µm and the total dimension of the bridge circuit is $5 \times 5\,mm^2$. **(b)** A schematic of the Wheatstone bridge circuit, which has four resistors arranged in a diamond shape. The circuit has two current nodes, where the supply voltage $V_S$ is connected to one node, while the biasing current $I_B$ is connected to the other node. The difference between the two output nodes $V_1$ and $V_2$ is related to the change in the resistance values as indicated using Eq. (2). SEM images of the silver-ink printed lines of the strain gauge, where **(c)** corresponds to the vertically printed meanders and **(d)** corresponds to the horizontally printed meanders. The images illustrate the variation of the silver-ink density between both printing directions, which results in level variations in the printed resistance values.

is equal to the ratio of the two resistors in the other branch. One or more resistors can be the sensing active element depending on the type of strain and the required accuracy of the measurements. In order to achieve high bridge sensitivity and linearity, full bridge topology is adapted in which two resistors, named $R_V$ in Fig. 1, are printed vertically to sense the vertical bending strain variations while the other two resistors $R_H$ are printed horizontally in the direction perpendicular to the bending strain. Equation (1) relates the resistance values of $R_V$ and $R_H$ to the voltage difference between the output terminals $V_{out}$, given constant biasing current $I_B$.

$$V_{out} = V_1 - V_2 = I_B \cdot \frac{R_{V,1}R_{V,2} - R_{H,1}R_{H,2}}{R_{V,1} + R_{V,2} + R_{H,1} + R_{H,2}}. \quad (1)$$

The linear transfer characteristics of the bridge with the change in the active resistors $\Delta R_V$ due to bending strain can be illustrated assuming $R_V + \Delta R_V = R_{V,1} = R_{V,2}$ and $R_H = R_{H,1} = R_{H,2}$ and using Eq. (1), this results in the fol-

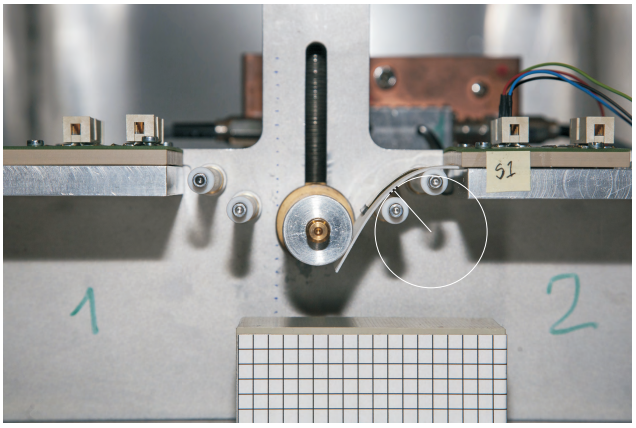


**Figure 2.** Photographs showing the measurement setup front view. The gripper finger is bent by the movable rod to the bending radius of about 38 mm.

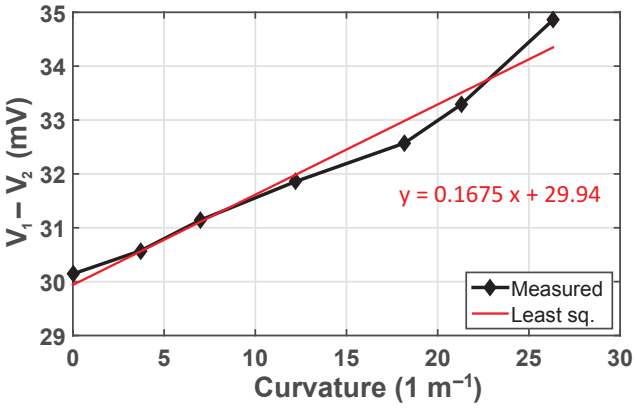


**Figure 3.** Strain gauge measurement results showing curvature of the gripper finger plotted against the output voltage of the strain gauge bridge circuit. Six measurements are taken during decreasing the bending radius of the gripper finger at bending radii of about 270, 142, 82, 55, 47 and 38 mm. The linearity of the bridge circuit is shown by fitting the measurements to a straight line using the least square method. The straight line equation is given and the coefficient of determination $R^2$ is 97 %. The non-linearity with respect to the full-scale span is about about 10 %.

lowing relation:

$$V_{\text{out}} = \frac{I_{\text{B}}}{2} \cdot \Delta R_{\text{V}} + V_{\text{offset}}, \tag{2}$$

where The offset voltage $V_{\text{offset}}$ corresponds to the mismatch between the two printing directions and is given by this relation:

$$V_{\text{offset}} = \frac{I_{\text{B}}}{2}(R_{\text{V}} - R_{\text{H}}). \tag{3}$$

The mechanical strain $\epsilon$, the bending curvature $1/r$ are linked using the following relation:

$$\epsilon = \frac{\Delta R_{\text{V}}/R_{\text{V}}}{\text{GF}} = \frac{y}{r}, \tag{4}$$

where $\Delta R_{\text{V}}/R_{\text{V}}$ is the relative change in the electrical resistance, GF is the gauge factor, $y$ is the distance from the neutral surface of the bending object. From Eqs. (2) and (4), the end-to-end relation, which links the output voltage of the strain gauge to bending curvature is as follows:

$$V_{\text{out}} = \frac{I_{\text{B}}}{2} \cdot \text{GF} \cdot R_{\text{V}} \cdot \frac{y}{r} + V_{\text{offset}}. \tag{5}$$

### 2.3 Characterization

The robotic finger experiences a non-uniform strain distribution during its bending. However, we can assume that the bending curvature is the same within the relatively small area of each strain gauge ($5 \times 5\,\text{mm}^2$), thus the bending curvature of the gripper finger can be related to the output voltage of the strain gauge bridge circuit. Accordingly, an experimental study of the behavior of the printed strain gauge under tensile bending strain is presented in this section. Figure 2 shows the image of the gripper material while bending. A column with movable rod is used to bend the strain gauge sample, which is mounted on the gripper finger material. Additionally, the side view images are captured using a high resolution digital camera. Consequently, the bending radius at the strain gauge position is extracted from the images by defining three points on the gripper finger curved surface and taking a grid of 5 mm × 5 mm squares as a reference.

The output voltage of the strain gauge bridge circuit ideally varies linearly with the bending curvature as given by Eq. (5). Figure 3 shows the strain gauge output voltage plotted with the curvature of the gripper finger. The full-scale output voltage change is about 5 mV during increasing the bending curvature at 1 mA biasing current. At the maximum bending curvature, the sensitivity of the strain gauge is evaluated by dividing the full scale output voltage change by the total voltage drop on the strain gauge, which is measured and equals about 440 mV. Consequently, the sensitivity for the measured strain gauge is about $10\,\text{mV V}^{-1}$. At the flat state, the output voltage of the strain gauge is at the offset voltage, which traces back to the levels variations of the individual bridge resistors. The offset voltage $V_{\text{offset}}$ is about 30 mV at a biasing current of 1 mA, which is compensated later by the readout chip. Table 1 shows a summary of the printed sensor main characteristics.

## 3 Sensor readout

An application specific integrated circuit (ASIC) is implemented for the purpose of interfacing with the printed strain gauge. Figure 4 shows a schematic illustration of the mixed-signal ASIC architecture. It consists of an analog interface circuit and a digital controller. The analog interface generates

**Table 1.** Printed strain gauges characterization results.

| | |
|---|---|
| Printing tech. | Aerosol Jet® |
| Dimension | $5 \times 5\,\text{mm}^2$ |
| Line width | $20\,\mu\text{m}$ |
| Thickness | 1–3 µm |
| Gauge resistance $R_g$ | $\approx 800\,\Omega$ |
| $\Delta R_g/R_g$ | $\pm 1.25\,\%$ |
| Sensitivity | $10\,\text{mV}\,\text{V}^{-1}$ |
| Gauge factor | 2 |
| Strain $\epsilon$ | $\pm 0.625\,\%$ |
| Bridge output voltage | $4.6\,\text{V} \pm 5\,\text{mV}$ |
| Offset voltage | $\approx 30\,\text{mV}$ at $I_B = 1\,\text{mA}$ |

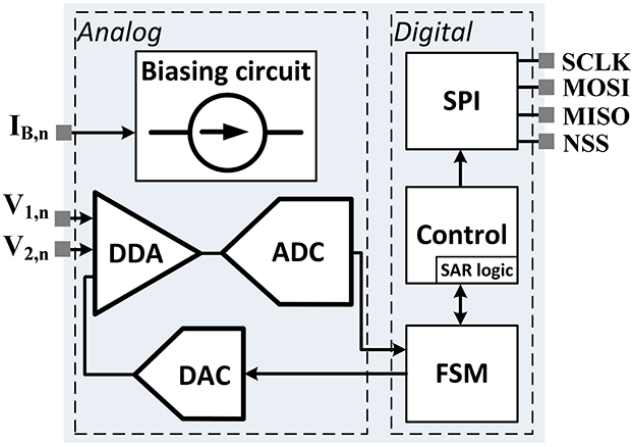


**Figure 4.** A schematic illustrating the top level system architecture of the ASIC including the analog and digital blocks. The analog part contains a biasing circuit for the printed sensors as well as for the analog interface circuit, which includes the differential difference amplifier (DDA), 5-bit digital-to-analog converter (DAC) and 10-bit analog-to-digital converter (ADC) based on successive approximation register topology (SAR). The digital part controls the operation and timing of the analog circuit using a finite state machine (FSM) as well as communicating to external receiver using serial peripheral interface (SPI) interface.

the sensor and readout circuit biasing currents and voltages in addition to performing the required signal conditioning and digitization of the strain gauge signals. The digital controller manages the analog circuit timing and the digital communication of the sensor data to an external receiver. The ASIC design is based on the 0.5 µm mixed-signal GATEFOREST™ technology, which is a sea-of-gates transistor array (IMS, 2011).

The sensor readout should meet certain design goals, which are influenced by the nature of the printed sensor and the required performance of the whole electronic skin system. In fact, the ASIC should perform one measurement of the printed sensor array every 1 ms in order to be able to monitor the electronic skin bending activity in quasi real-time. This requirement is achieved by duty cycling the analog interface circuit for the three different sensors. Since the printed sensor has a relatively low gauge resistance (about 800 Ω), low voltage drop across the sensor is inevitable. Consequently, the sensor readout is designed to cope with the relatively high dc level of the sensor output voltages (4.6 V), which is close to the supply voltage. Additionally, the input referred noise level of the sensor interface circuit should be well below the useful signal from the printed sensor (about 5 mV), which is to be amplified by the differential difference amplifier (DDA) and then digitized by the analog-to-digital converter (ADC). The dc offset voltage, which is larger than the useful sensor signal, is inherently contained in the sensor signal and is compensated by the sensor interface circuit before the useful sensor signal amplification. Finally, the influence of the chip bending on the active transistors is minimized by placing the chip at the bottom part of the electronic skin, which is affected by the least amount of bending strain.

### 3.1 Digital controller

The digital controller contains a finite state machine (FSM), which has four states; one idle state and three measure states where each measurement state is for one strain gauge at a time. During idle state, all analog operations are switched-off in order to reduce power consumption, while during the measure states the analog interface circuit is switched on and each strain gauge is measured one after another. The duration of the three measurements should take 1 ms and the resulting 30-bit measurement data is available to be fetched by the digital controller, which saves this data locally and/or communicates it to an external receiver using the Serial Peripheral Interface Bus (SPI). The digital operation uses a main clock with frequency of 864 kHz. Note that the influence of bending on the digital transistors and thus the digital circuit performance in terms of setup and hold times is minimized by increasing the base uncertainty during circuit synthesis (Mahsereci et al., 2016).

### 3.2 Analog interface circuit

Figure 5 shows the schematic of the implemented analog interface circuit. It includes a 5-bit digital-to-analog converter (DAC), voltage buffer, DDA, 10-bit successive approximation register (SAR-ADC) in addition to the strain gauge bridge circuit. The voltage buffer shields the low impedance node at the resistor $R_1$ from the high impedance node of the constant DAC output $V_{\text{ref1}}$. The 10-bit SAR-ADC is used to digitize the output voltage of the DDA and the SAR logic is included in the digital control circuit.

#### 3.2.1 Digital-to-analog converter

The DAC is based on the resistor string architecture, which is the most basic and simple DAC architecture. It provides good accuracy when no output current is required. This is the case

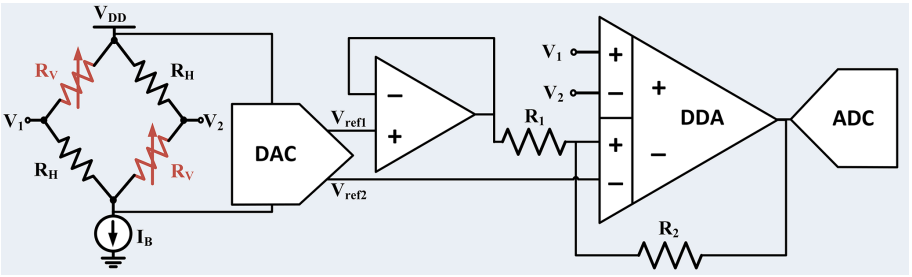


**Figure 5.** A schematic of the implemented analog interface circuit. It consists of the strain gauge bridge circuit, a 5-bit resistor string digital-to-analog converter (DAC), a voltage buffer, a DDA and a 10-bit successive approximation (SAR-ADC). The DAC has an output voltage defined as $V_{\mathrm{ref2}}$ and a constant reference voltage $V_{\mathrm{ref1}}$, which is used by the DDA. The DAC is used to cancel the offset voltage in the differential input signal $(V_2 - V_1)$. The voltage buffer provides low impedance node for the resistor $R_1$, which determines the close-loop gain of the DDA together with the resistor $R_2$.

in our design since both the DAC output voltage and the constant reference voltage ($V_{\mathrm{ref2}}$ and $V_{\mathrm{ref1}}$) are connected to high impedance nodes of the voltage buffer and the DDA inputs respectively. The DAC output voltage ($V_{\mathrm{ref2}}$) can be varied digitally for each strain gauge. The DAC mid-range voltage ($V_{\mathrm{ref1}}$) is used as a constant reference voltage required by the DDA and cannot be changed digitally.

The DAC comprises of 31 identical resistors ($R_{\mathrm{unit}} = 3.115\,\mathrm{k}\Omega$) and 32 identical switches. The analog switches use PMOS transistors since the DAC operates closer to the supply voltage. Two relatively large resistors are added on the top and bottom of the string respectively in order to scale down the range of voltages required by the DAC to resolve, thus using less number of bits to achieve the $1\,\mathrm{LSB} = 10\,\mathrm{mV}$ increments. The DAC is connected in parallel to the strain gauge bridge circuit, where one node is connected to $V_{\mathrm{DD}}$ (normally 5 V) and during readout the second is connected to the lower voltage of the strain gauge (ideally 4.2 V when $R_{\mathrm{g}} = 800\,\Omega$ and $I_{\mathrm{B}} = 1\,\mathrm{mA}$) where the biasing current is connected.

Since the DAC is connected across the strain gauge bridge circuit, it has the same voltage drop. The high resistance value of the DAC will have a negligible loading effect when connected in parallel to the printed sensor during readout. The constant voltage $V_{\mathrm{ref1}}$, which is used as a voltage reference by the DDA, is defined as the mid-range voltage drop on the strain gauge (also mid-range of the DAC) and is calculated as follows:

$$V_{\mathrm{ref1}} = V_{\mathrm{DD}} - \frac{I_{\mathrm{B}} \cdot R_{\mathrm{g}}}{2}, \tag{6}$$

where $\mathrm{V_{DD}}$ is the supply voltage, $I_{\mathrm{B}}$ is the sensor biasing current and $R_{\mathrm{g}}$ is the gauge resistance value.

With no differential input signal and ideally no offset voltage, the dc output of the DDA should be at the mid-point of the rail-to-rail supply voltage ($V_{\mathrm{DD}}/2$). By utilizing Eq. (9) and given the closed-loop gain of the DDA ($A_{\mathrm{c}} = 50$), the DAC analog output voltage $V_{\mathrm{ref2}}$ can be designed as follows:

$$V_{\mathrm{ref2}} = \frac{V_{\mathrm{out}}}{A_{\mathrm{c}}} + \left(\frac{A_{\mathrm{c}} - 1}{A_{\mathrm{c}}}\right) V_{\mathrm{ref1}}. \tag{7}$$

The resistor string architecture guarantees monotonic DAC output. However, the differential non-linearity (DNL) as well as integral non-linearity (INL) occur in this DAC due to the process variations in the CMOS fabrication technology. These process variations causes the poly unit resistors to have a tolerance ($\Delta R/R$) of about 2 %. In order for this DAC to function properly, its DNL and INL should be lower than half LSB. The worst-case DNL can be determined using the following relation (Baker, 2010):

$$\mathrm{DNL} = \mathrm{LSB} \cdot \frac{\Delta R}{R} = 0.02\,\mathrm{LSB},$$

while the worst-case INL is calculated as follows:

$$\mathrm{INL} = \mathrm{LSB} \cdot 2^{N-1} \cdot \frac{\Delta R}{R} = 0.0224 = 0.32\,\mathrm{LSB},$$

where $N$ is the number of bits of the DAC.

### 3.2.2 Differential difference amplifier

The DDA is an important analog building block and has been utilized in many signal conditioning circuits (Säckinger and Guggenbühl, 1987; Kuhl et al., 2013). The open-loop output voltage of the DDA is given by the following relation:

$$V_{\mathrm{out}} = A_{\mathrm{o}}[(V_{\mathrm{pp}} - V_{\mathrm{pn}}) - (V_{\mathrm{np}} - V_{\mathrm{nn}})], \tag{8}$$

where $A_{\mathrm{o}}$ is the open-loop gain, $(V_{\mathrm{pp}} - V_{\mathrm{pn}})$ and $(V_{\mathrm{np}} - V_{\mathrm{nn}})$ are two differential inputs with high input impedance and $V_{\mathrm{out}}$ is a single-ended output with low output impedance. The DDA is placed in a negative feedback configuration by the two resistors $R_1$ and $R_2$ as shown in Fig. 5. The closed-loop output voltage of the DDA, which is derived from Eq. (8), is given by the following relation:

$$V_{\mathrm{out}} = A_{\mathrm{c}}(V_2 - V_1 + V_{\mathrm{ref2}} - \left(\frac{A_{\mathrm{c}} - 1}{A_{\mathrm{c}}}\right) V_{\mathrm{ref1}}), \tag{9}$$

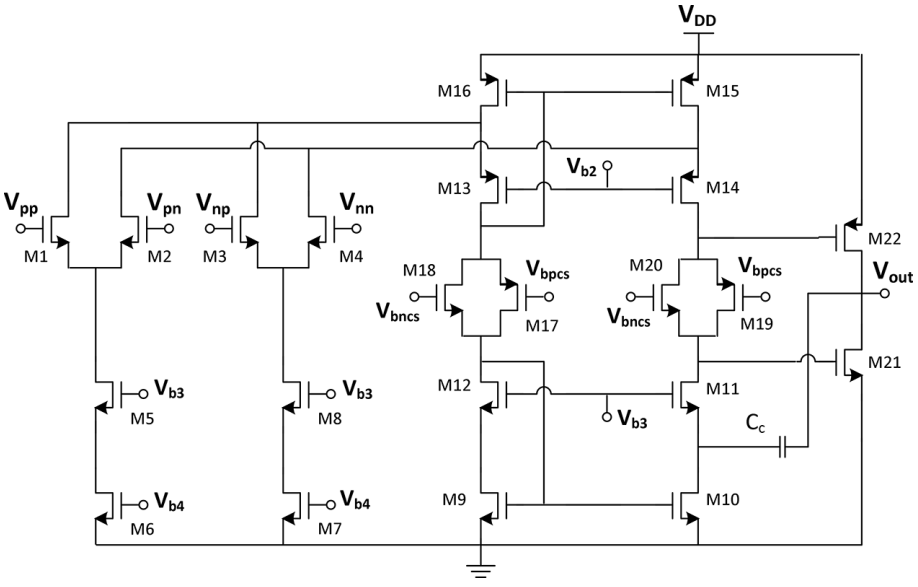


**Figure 6.** A schematic for the differential difference amplifier circuit. Only the standard transistors from the GATEFOREST™ technology library are used in this design.

where $V_1$ and $V_2$ are the strain gauge output voltages, $V_{ref1}$ is a constant reference voltage, $V_{ref2}$ is the DAC output voltage and $A_c$ is the closed-loop gain of the DDA, which is given by the following relation:

$$A_c = 1 + \frac{R_2}{R_1}. \tag{10}$$

Since the dc level of the strain gauge output voltages are close to the supply voltage, the DDA is designed using the folded-cascode topology with NMOS input differential pairs. The DDA output is driving the feedback resistor $R_2$, which has a lower value compared to the high output impedance of the folded-cascode stage. Consequently, a class AB output stage is used. Figure 6 shows the schematic of the folded-cascode implementation of the DDA including the class AB output stage and excluding the biasing circuit. The standard transistors from the GATEFOREST™ technology library are used in this design. Two differential pairs consist of the NMOS transistors M1 to M4. The NMOS transistors M5 to M8 configure the biasing current for the differential pairs. They are biased using constant voltages $V_{b3}$ and $V_{b4}$ generated from the biasing network. Two wide-swing current mirrors comprise the NMOS transistors M9 to M12 and the PMOS transistors M13 to M16. The NMOS current mirror is dc biased using the constant voltage $V_{b3}$, while the PMOS current mirror is biased using a constant voltage $V_{b2}$. Two floating current sources are implemented using transistors M17 to M20. They are biased using two constant voltages $V_{ncs}$ and $V_{pcs}$. The class AB output stage comprises NMOS transistor (M21) and PMOS transistor (M22). The capacitor $C_c$ is a compensation capacitor. The biasing network is not shown and can be found in Baker (2010).

### 3.2.3 Simulation results

Figure 7 shows the dc response of the DDA, where it shows a dc gain of 50 and linear response in the input differential signal range of about ±50 mV. The ac response of the DDA is simulated and shows an open-loop gain of more than 100 dB and a gain-bandwidth product of about 47 MHz. The gain and phase margins are extracted from the ac simulations and found to be 7 dB and 63° respectively, which ensures the stability of the DDA in the negative feedback configuration.

The sensor interface circuit shown in Fig. 5 is simulated, and Table 2 includes a summary of its operation properties. Most of the simulations are done using the nominal values of the devices' models in the GATEFOREST™ technology as well as a supply voltage of 5 V and room temperature of 27 °C. However, these values are changed during the Monte Carlo and process corners simulations, which are used to verify the interface circuit proper operation across fabrication process, supply voltage and temperature variations. It is important to mention that the presented analog interface circuit simulations are performed for a strain gauge bridge resistance $R_g$ of 800 Ω and a biasing current $I_B$ of 1 mA. In order to mimic the real printed sensor, an intentional mismatch is introduced in the four bridge resistors, which results in about 30 mV offset voltage. The two strain sensitive resistors are varied by ±10 Ω. This results in a relative change in the gauge resistance value $\Delta R_g/R_g$ in the range of ±1.25 % and thus a differential output voltage swing of ±5 mV.

The sensor interface circuit consumes a current of 1.9 mA, where 1 mA is used to bias the strain gauge. Figure 8 shows the transient response of the sensor interface circuit, where the differential input and output voltages are plotted in the

**Table 2.** Summary of the sensor interface circuit properties.

| | |
|---|---|
| Technology | 0.5 µm |
| Chip dimensions | $4.6 \times 4.6\,\text{mm}^2 \times 20\,\mu\text{m}$ |
| Supply voltage | 3.8 to 5.2 V |
| Diff. input voltage | ±0.1 to ±50 mV |
| Strain $\epsilon$ | ±0.02 to ±5 % |
| DC input level | 0.5 to 4.8 V |
| Offset cancellation | 150, 10 mV step |
| Integrated input-referred noise (1 Hz–100 kHz) | ≈ 27 µVrms |
| ADC resolution | 10 bit |
| Digital clock frequency | 864 kHz |

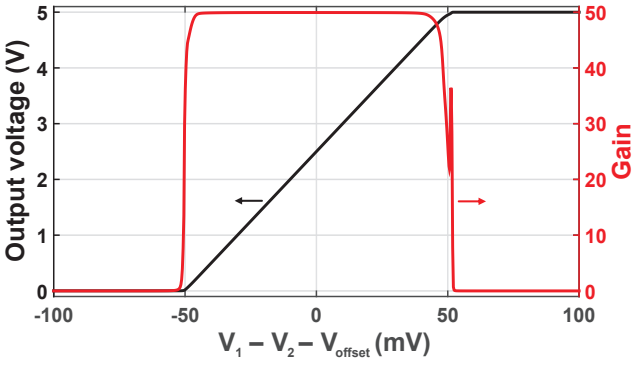


**Figure 7.** The dc response simulation results, where the differential input voltage ($V_1 - V_2$) is varied and the output voltage as well as the close-loop gain of the DDA are plotted. The simulations show a linear response and a constant close-loop gain in the input range of about ±50 mV.

same figure. At $\Delta R_g/R_g = 0$ and 30 mV input signal, the circuit output voltage equals to 2.5 V, which indicates a successful cancellation of the dc offset voltage. In addition, the sensor signal (about ±5 mV) is amplified by 50 using the closed-loop gain of the DDA.

Additionally, the noise performance of the analog interface circuit is simulated and shows an integrated input-referred noise in the frequency band from 1 Hz to 100 kHz is about 27 µVrms and output noise of 1.36 mVrms, which is lower than half of the ADC LSB. Furthermore, the supply voltage is varied from 5.2 V down to 3.5 V and the output voltage is plotted as shown in Fig. 9. The simulations show that as the supply voltage decreases, the output voltage decreases as well since all the circuit components use the same supply voltage. However, the circuit closed-loop gain and linearity are maintained down to a supply voltage of about 3.8 V.

### 3.2.4 Layout

The layout of the sensor interface circuit is based on the 0.5 µm mixed-signal gate array technology, which is a sea-of-gates transistor array (IMS, 2011). The sensor readout ASIC contains a digital core and in total 74 available ana-

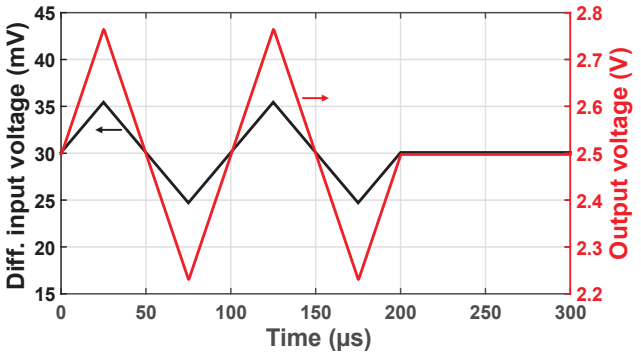


**Figure 8.** The transient simulation results of the analog interface circuit, where the differential input voltage ($V_1 - V_2$) and the output of the DDA are plotted with time. When the input voltage equals to the offset voltage (30 mV), the output of the DDA is at half the supply voltage. The sensor signal changes in the range of ±5 mV and is amplified by the DDA with a factor of 50.

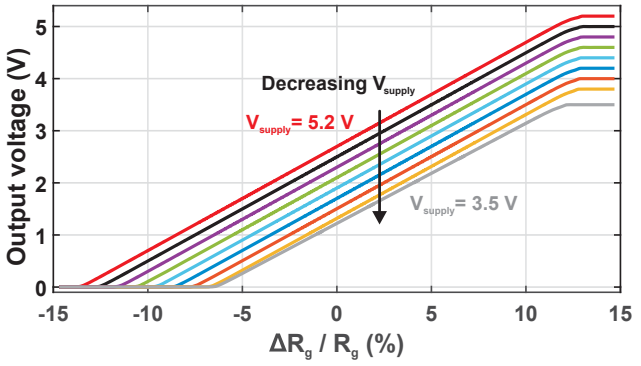


**Figure 9.** The relative change of the gauge active resistor ($\Delta R_g/R_g$) is varied and the dc output voltage of the DDA is plotted at different supply levels starting from 5.2 V down to 3.5 V. The linearity of the sensor interface circuit is maintained down to a supply voltage of 3.8 V.

log sites, where each analog site occupies an area of about 48 µm × 300 µm. The analog interface circuit consumes 16 analog sites, where the 5-bit DAC, the buffer and the DDA occupy 5, 5 and 6 analog sites respectively. The rest of the available sites are used for the SAR-ADC and other analog blocks. The common centroid layout technique is adapted to improve the matching between the DDA as well as the buffer op-amp input pairs. Placement of critical structures, such as DAC resistors, current mirrors and input pairs, close to each other is used in order to mitigate the stress-induced effects, which happens during the bending of the ultra-thin chip.

## 4 Conclusions

A flexible Hybrid System-in-Foil (HySiF) is designed to be used as an electronic skin for robotic applications. The system comprises of an array of printed strain gauges and ultra-

thin flexible silicon chips, which demonstrates the complementary benefits of combining the low-cost printed electronics and the high performance silicon technologies in one system. The strain gauges are printed using high resolution Aerosol Jet® printing technique. The full swing sensor output voltage is about 5 mV, with a dc offset voltage about 30 mV at 1 mA biasing current. A sensor readout ASIC is implemented using IMS CHIPS 0.5 µm CMOS mixed-signal gate array (GATEFOREST™) technology. The analog interface circuit amplifies the sensor output voltage by a factor of 50 as well as canceling the offset voltage. The sensor interface circuit comprises of a DDA, voltage buffer, 5-bit DAC and 10-bit SAR ADC. The simulation results shows the proper operation of the circuit in terms of stability and linearity. Furthermore, it is able to detect the bending strain $\epsilon$ in the range from $\pm 0.02$ to $\pm 5\,\%$. Further improvements are possible, which include additional optimization of the DDA circuit to target low power operation. In addition, the implementation of a closed-loop algorithm and automatically search for a proper DAC value, which could be used by the DDA for offset cancellation.

*Data availability.* The measurement and simulation data are available through a public repository (https://doi.org/10.17632/wz9kwf7grv.2, see Elsobky, 2017).

*Competing interests.* The authors declare that they have no conflict of interest.

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