Performance Analysis on the Intel Knights Landing Architecture

Michael Wagner, Judit Gimenez

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High performance computing (HPC) systems provide enormous computational resources. But the increasing performance introduces more and more complexity, as well. Current leading edge HPC systems consist of millions of heterogeneous processing elements . They require consideration of parallel execution, network, system topology, and hardware accelerators as well as a variety of different parallel programming models such as message passing (MPI), threading and tasking (OpenMP), one-sided communication (PGAS), and architecture specific models to incorporate hardware accelerators such as GPUs. As a result, appropriate support tools have become inevitable in the development process.

Performance analysis tools assist developers not only in identifying performance issues within their applications but also in understanding their complex parallel behavior. Thereby, the development of such tools is facing their own challenges. On the one hand, there are challenges specific to the tools such as techniques to gather appropriate information from the running application while introducing minimal bias, the post-processing of the collected data to correctly correlate data from a plenitude of different data source, and finally methods to present the data or derived results in an appropriate manner to allow an accessible and meaningful analysis. On the other hand, the tools encounter challenges of similar nature as the application the support, for instance, scaling in all aspects (number of cores, file systems, parallel analysis operations) to current HPC system sizes, utilize and capture a variety of parallel programming models and concepts, and operate on and support new arising architectures.

One of the emerging architectures in HPC systems is Intel's Knights Landing (KNL) many core chip, which will also be part of BSC's next HPC installation MareNostrum 4. KNL is the code name of the second generation of Intel XEON Phi, a many integrated core architecture (MIC) with up to 72 cores with four-time hyper-threading. It includes up to 384 GB of DDR4 RAM and 8-16 GB of stacked MCDRAM, a version of high bandwidth memory. In addition, each core will have two 512-bit vector units and will support AVX-512 SIMD instructions.

To support HPC software developers at BSC and beyond in utilizing the capabilities of this new architecture, the BSC performance analysis tools (*https://tools.bsc.es*) are ready to record and analyze parallel applications on the new Knights Landing architecture. This presentation will demonstrate the functionality and capabilities of the tools on the KNL architecture. Based on a case study of an FFT kernel from an electronic-structure calculations and materials modeling simulation framework, the presentation will highlight the application recording as well as analysis process starting from identifying the most severe performance issues using a parallel performance model, analyzing and understanding the uncovered performance issues with increasing levels of detail, and finishing with the advanced techniques to cluster and track different application phases with increasing scale. In addition, specific suggestions for potential code optimizations and a quick review of a proof-of-concept implementation of these suggestions conclude the presentation.

Within POP, the European Performance Optimisation and Productivity Centre of Excellence in Computing Applications (*https://pop-coe.eu/*) the tools and expertise are used to help customers to improve performance in various aspects of HPC: Code developers are assisted with an assessment of detailed actual behavior and suggestions of most productive directions to code re-factoring. Application users are supported with an assessment of achieved performance in specific production conditions, possible improvements modifying environment setup and evidence to interact with code providers. Finally, infrastructure operators benefit from an assessment of achieved performance in production conditions, possible improvements from modifying environment setup, information for scheduling and process allocation, as well as training of support staff.

Michael Wagner received the M.Ed. degree in mathematics and computer science and the Ph.D. degree in computer science from the Technische Universität Dresden, Dresden, Germany, in 2008 and 2015, respectively. He was a research scientist in performance analysis at the Center for Information Services and HPC (ZIH), Dresden, Germany and is currently a HPC application analyst at the Barcelona Supercomputing Center (BSC), Barcelona, Spain. His research interests are in high performance computing with emphasis on performance analysis.