DOI 10.1016/j.sna.2017.06.022

Differential Temperature Sensor with high sensitivity, wide dynamic range and digital offset calibration.

Eva Vidal [a], Sergio Ruiz [a], Jérémy Duquenoy [b], J.L. González[c] and Josep Altet [a].

[a] Electronic Engineering Department, Universitat Politècnica de Catalunya, Barcelona, Spain.

[b] ENSEIRB-MATMECA, Bordeaux Institute of Technology, Talence, France.

[c] DACLE/LAIR CEA-Leti, MINATEC Campus, Grenoble, France.

Abstract

The goal of this paper is twofold: first to add together all different causes that can alter the offset of a differential temperature sensor and, second, to present a new differential temperature sensor architecture that can digitally compensate for this behavior and therefore extends the sensor dynamic range. Measurements performed on a 65nm CMOS differential temperature sensor are presented to illustrate the discussion. As evolution of the state of the art, an automatic calibration procedure and the new sensor topology is presented. With this new topology, not only the thermal offset can be digitally calibrated, but the application field of differential temperature sensors is widened, being now suitable for use in measurements where both wide input range and high differential sensitivity are required.

Keywords:

Differential Temperature Sensors, Integrated Circuits, CMOS temperature sensors, thermal testing, offset temperature correction.

Introduction

Temperature sensors are embedded in the same silicon die than other complex/high performance circuits with the goal of either increase its reliability (e.g. thermal management of microprocessors [1,2]) or as built-in testers, (e.g. to perform a structural test [3] or a functional test [4,5] of RF and mmW analog circuits). In this last scenario, the temperature sensor is placed near the analog circuital block to be tested (e.g., low noise amplifier – LNA-, power amplifier – PA-), so called in general Circuit Under Test –CUT- in order to extract some or their figures of merit (e.g. efficiency [5], central frequency [4], bandwidth [4]). CUT and temperature sensor are thermally coupled through the silicon substrate. As explained in [4] and [5], the temperature sensor tracks the temperature variations generated by the CUT power dissipation, which, in turn, depends on the electrical signals (voltage and current) present within the CUT, which, in turn, may depend on its particular performances (e.g. if the CUT is an amplifier: its gain) or structure (i.e. presence of structural defects, such as bridges – undesired short circuits between nodes- or opens). Due to this relation, the temperature increase generated on the silicon surface by a running CUT is a signature of its status and performance.

Several topologies of temperature sensors used as built-in testers are reported in the literature: PN junctions [5], MOS transistors in diode configuration [6] or differential temperature sensors [3,4]. Among them, the ones with highest sensitivity are the differential temperature sensors.

Differential temperature sensors have similar topology to electrical differential amplifiers [7], but in the temperature sensors, the differential pair is not imbalanced by a difference of the input devices electrical voltage, but due to a difference in the working temperature of each transistor. The coupled devices that form the differential pair are the sensor's temperature transducers. Differential temperature sensors may offer high sensitivity (2,4V/ºC is reported in [7], where ºC stands for the working temperature difference between the two temperature transducers), but with a limited input range. The high sensitivity combined with the limited input range, makes this sensor topology readily affected by any circumstance that may lead the sensor's output voltage to saturation when it is supposed to work within the linear range. In fact process variations that produce mismatches in the differential pair and currents mirrors are not the only responsible of the circuit going out of its linear range, but also external temperature

variations independent of the CUT. All these effects, similarly to differential voltage amplifiers, can be modeled as an input temperature offset (ITO) into an ideal differential temperature sensor.

So far, the differential temperature sensors published in the literature have been used as proof of concept to validate new procedures to extract figures of merit from temperature measurements (e.g. the extraction of the 3dB bandwidth of a high frequency amplifier [4]) in research experiments. As all the experimentation has been carried out in a controlled laboratory environment the ITO has been manually compensated for (example is the procedure reported in [3]). Moving forward, we envision the scenario where several temperature sensors are placed within complex integrated circuits such as transceivers. In this context, temperature sensors would be placed in close proximity with high frequency analog circuits that act as CUT, with the objective of performing a built-in and in-field test/characterization of them. The final goal of this set up could be part of a self-healing strategy to avoid the consequences of Process Voltage and Temperature –PVT- variations or aging on the overall circuit performance [8]. In this envisioned scenario, temperature sensor's thermal offset should to be automatically compensated for.

The goal of this paper is to discuss the different causes of ITO in a differential temperature sensor and present a novel design strategy to automatically compensate for this offset. This new strategy will drive us to a new sensor topology, which would not only allow a digital offset calibration, but to improve sensor's performances by allowing to perform high sensitivity measurements combined with high input range temperature measurements.

The paper is structured as follows: section 2 reviews the basic topology of differential temperature sensors and discusses the ITO effects/sources and outlines how this offset has been dealt with within the state of the art. Experimental ITO measurements performed on a 65nm CMOS differential temperature sensor are presented. A procedure proposed to automatically compensate ITO is introduced. An experimental proof of concept is presented using the BiCMOS differential temperature sensor designed in [7] and a simple microprocessor. After discussing the weak points that this experimental set-up has when it has to be built-in with CUTs, we present the new sensor architecture in section 3. Schematic and simulated results when designed with a 0,35 microns CMOS technology are presented and the advantages of this architecture with respect to the state of the art are discussed. Finally, section 4 concludes the paper.

2. Structure of a differential temperature sensor. Causes and Effects of Input Temperature Offset.

The goal of this section is to introduce the causes of ITO and its effects when a CUT is going to be tested/characterized through temperature measurements.

2.1 Definitions.

Fig. 1 shows the symbol of a generic differential temperature sensor. The inputs represent two devices that act as temperature transducers, whose working temperature are T_2 and T_1. The sensor core contains all the other devices needed to generate the sensor output voltage. The function of this sensor is to provide an output voltage proportional to the difference of temperature $(T_2\text{-}T_1)_{Sensed}$:

$$V_{out} = S_d \cdot (T_2 - T_1)_{Sensed} \quad (1)$$

where S_d is the sensor's differential thermal sensitivity (Units: V/ºC).

Figure 2 shows the typical input-output characteristic of the sensor. It has clearly two zones: linear range (when $(T_2\text{-}T_1)_{Sensed}$ is comprised between Δ_{MIN} and Δ_{MAX}), where eq. (1) holds, and saturation. In the ideal test situation, the difference temperature sensed is only caused by changes of the power dissipated by the CUT.

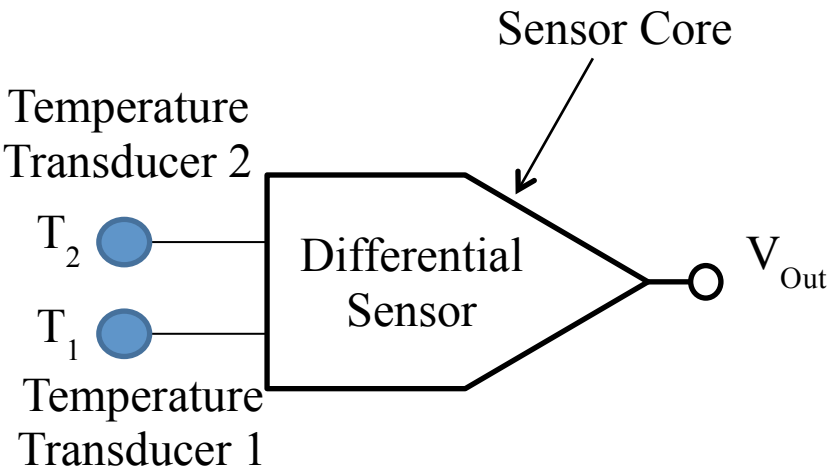

Figure 1. Generic Symbol of a Differential Temperature Sensor. The two circles represent the two devices used as temperature transducers; the other devices that form the sensor are within the sensor core.

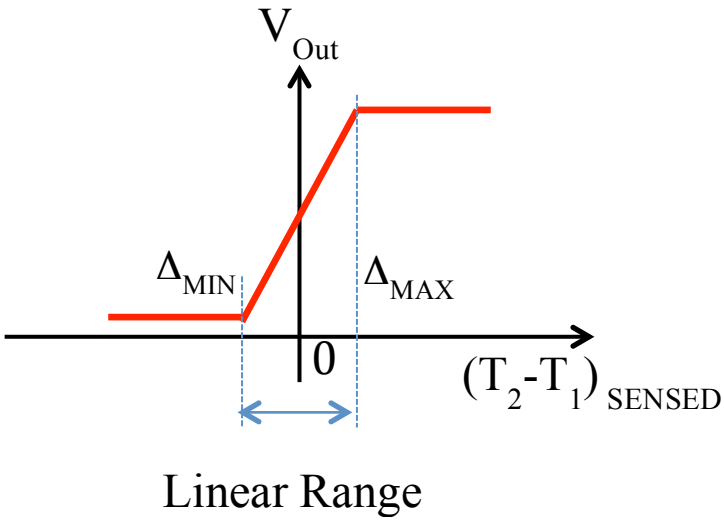

Figure 2. Differential temperature sensor input-output characteristic. The sensor is working in the linear range when (T_2-T_1) is comprised between Δ_{MIN} and Δ_{MAX}.

There are two sources of ITO:

i) External to the sensor: The temperature difference sensed by the sensor can be written as the addition of the temperature difference generated by the CUT, which superimposes to a previous existing temperature difference (so called offset), for instance created by another circuit different than the CUT.

$$(T_2 - T_1)_{Sensed} = (T_2 - T_1)_{CUT} + (T_2 - T_1)_{Offset} \quad (2)$$

As shown in Fig. 3, if $(T_2\text{-}T_1)_{Offset}$ is high enough, small changes of temperature increase generated by the power dissipated by the CUT does not move the temperature sensor from the saturation region, being the sensor's output voltage insensitive to $(T_2\text{-}T_1)_{CUT}$.

ii) Internal to the sensor: these are caused by device mismatches and process variations. When this is the case, the transfer function is transformed into the one depicted in Figure 4. In this figure, we assume that the only temperature increase is generated by the CUT, i.e., $(T_2\text{-}T_1)_{SENSED} = (T_2\text{-}T_1)_{CUT}$. Likewise to the previous case, if the sensor transfer function shift is high enough, small changes of the temperature increase generated by the CUT, may not move the temperature sensor from saturation. This is the situation depicted in Figure 4.

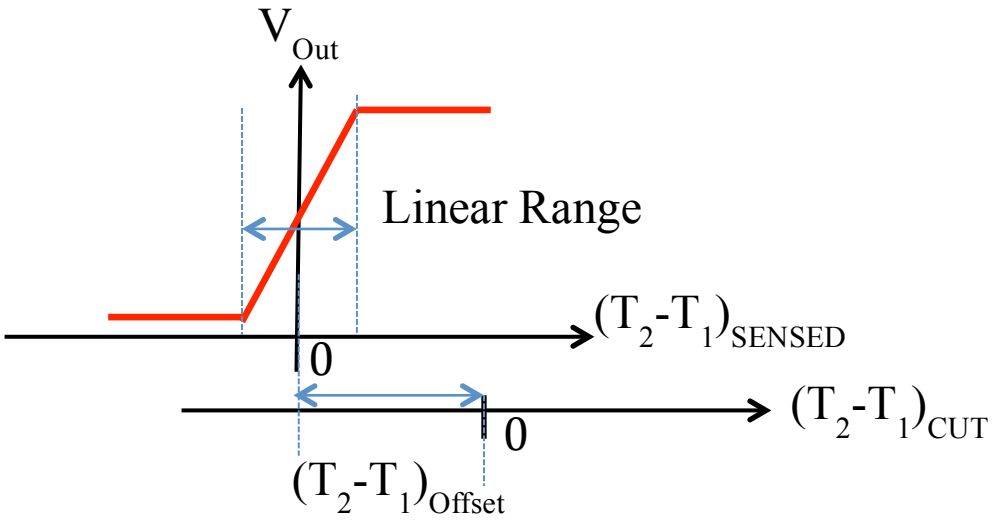

Figure 3: Effect of sensing the superimposition of two different temperature gradients.

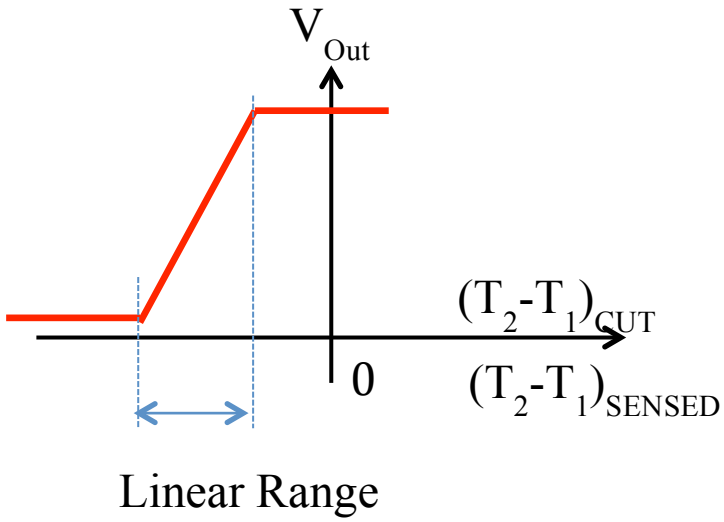

Figure 4. Effect of device mismatch and process variations on the temperature sensor input-output characteristic.

2.2 ITO Characterization in a 65nm CMOS differential temperature sensor. Strategies for ITO cancellation. State of the Art.

In order to further explain how different causes of ITO affect the behavior of the sensor we have chosen as example the sensor used in [4] shown in figure 5. This temperature sensor has been designed to measure the central frequency and 3dB bandwidth of a narrow band 60 GHz Power Amplifier (PA) devoted to high-definition video and high data-rate communications. In this sensor, the bipolar transistors Q_2 and Q_1 act as temperature transducers. The function of the devices that form the sensor core (following the notation of Fig. 1) is: the current provided by MN_1 is split into the

differential pair. The three current mirrors (MP_1-MP_2, MP_3-MP_4 and MN_2-MN_3) and the high impedance of the node formed by the drains of MP_4-MN_3, convert the current imbalance at the input pair provoked by temperature differences at Q_1- Q_2 into changes in the voltage of this node. The output buffer is added to get a differential sensitivity and a sensor bandwidth independent of the loading conditions. Transistors biased with the signals V_{CMp} and V_{CMn} are used as voltage controlled current sources for offset compensation.

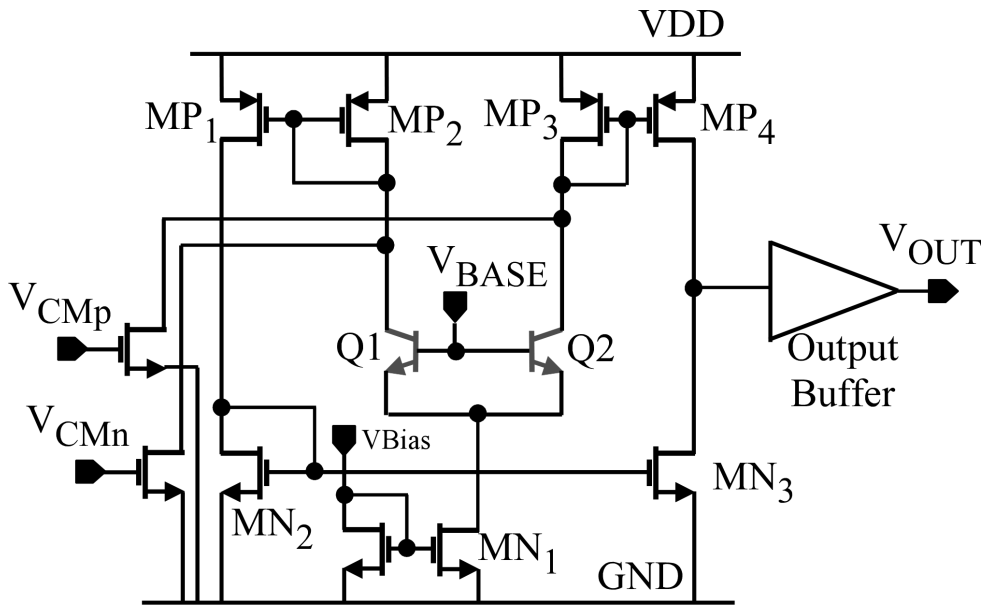

Figure 5. Schematic of the differential temperature sensor implemented in [4]. The two temperature transducers are the bipolar transistors Q1 and Q2, which form the input differential pair.

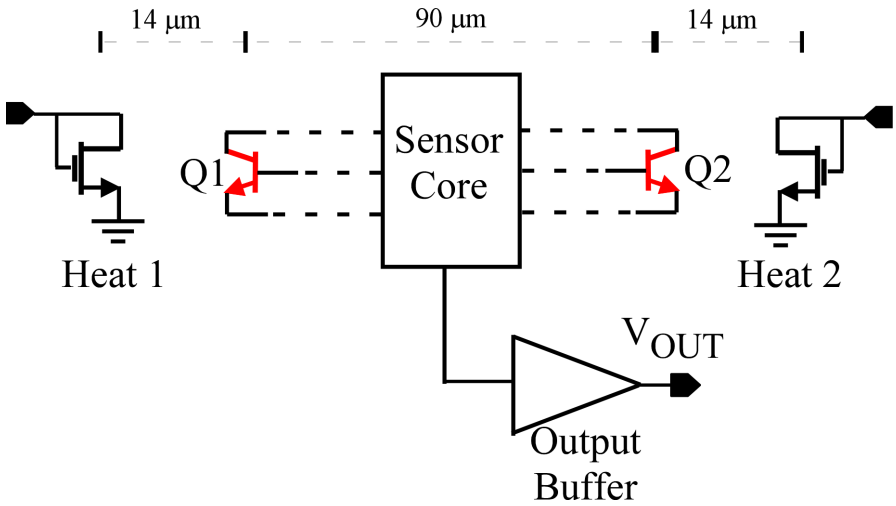

Figure 6 Simplified schematic that shows the differential temperature sensor, temperature transducers and the two MOS transistors in diode configuration used as heat sources to imbalance the temperature of Q1 and Q2.

This sensor was implemented in a 65 nm CMOS process. As the goal is to measure a temperature difference between the transistors Q_1 and Q_2, thermal mismatching between the two temperature transducers has to be enhanced. To this end, a considerable distance between both transducers in the layout is implemented. In the circuit in [4] the distance between both transistors is 90 μm.

To characterize the sensor's differential sensitivity, similar procedure as the one reported in [7] has been followed: To increase the temperature of one transducer in respect to the other in a controlled way, an additional MOS transistor connected in diode configuration has been placed as heat source next to each temperature transducer. The schematic is shown in Fig. 6. These MOS transistors are named *Heat 1* and *Heat 2*, depending on the name of the closest temperature transducer. The function of these transistors is to emulate the behavior of a CUT acting as heat sources. As described in the figure, the distance between each temperature transducer and its closest heat source is 14 μm. This short distance enhances the thermal coupling between the heat source and the temperature transducer [7]. With this set up we know that if the MOS transistor *Heat 2* dissipates power, the differential temperature (T_2-T_1) increases. On the other hand, if the MOS transistor *Heat 1* dissipates power, the differential temperature (T_2-T_1) decreases, going into negative values.

Fig. 7 shows the evolution of the sensor output voltage as a function of the power dissipated either by *Heat 1* or by *Heat 2*. The sensor has been biased with different values of V_{CMp} and V_{CMn}.

Let's focus in the case when both voltage controlled current sources are off *(i.e.* V_{CMp} = V_{CMn}= 0V; solid black line). From the experimental characterization, we observe that when the sensor is biased and no thermal unbalance is generated, the sensor's output voltage is 790 mV. However, it was designed to have a $V_{OUT}=V_{DD}/2$ (@V_{DD}=1,2 V, V_{Bias}= 0,7 V and V_{BASE}=0,85 V). As indicated in the introduction, this shift from the expected behavior can be modeled as an ideal differential temperature sensor, whose output voltage is the ideal $V_{DD}/2$= 600 mV, plus an ITO which imbalances the ideal sensor. Clearly, the source of this ITO is internal:

- Process variations.
- Mismatches in the DC output resistance of transistors MP_4-MN_3.
- Current mirror mismatches.
- Transducer mismatches, which are enhanced due to the particular layout configuration: the larger the distance between both transducers, the higher the

transducer mismatch.

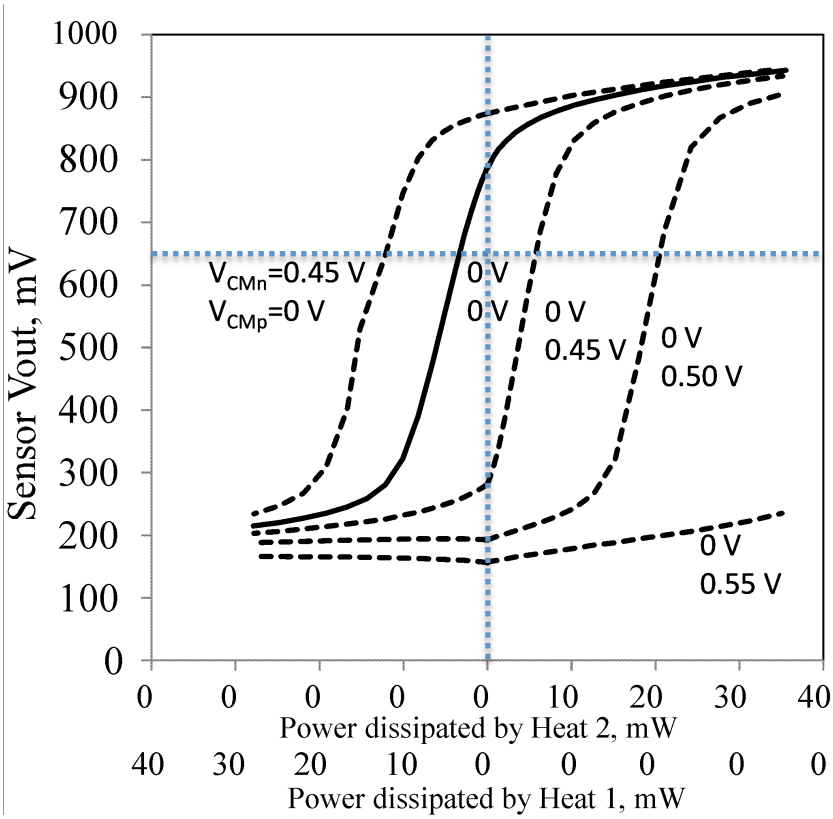

Figure 7. Sensor's input output characteristic for different values of the voltage applied to the voltage controlled current sources.

Those sources of offset are in fact commons to any type of differential pair topology (the sensor is, as a matter of a fact, a variation of a differential operational transconductance amplifier, OTA [7]).

As a consequence of this internal ITO, the sensor input output characteristic is not centered for a 0 input power (i.e. a 0 temperature difference between the transducers). In fact, the sensor output voltage is almost in saturation when the power dissipated by Heat1 is zero and Heat2 is increasing. Therefore, the circuit tracks, by sensing the temperature increase, the power dissipated by *Heat 2* with lower sensitivity than expected.

Analyzing further the measurements in Fig. 7, we can derive that the coupling between *Heat 1* and the sensor has a linear input range of about 8 mW, with a maximum sensitivity of -55 V/W (from simulation, the differential thermal sensitivity is 0.6 V/ºC). For *Heat 1* power dissipation levels higher than 8 mW, the sensor's sensitivity decreases and the sensor output voltage saturates.

Let's consider now external sources of ITO. Two possible sources of external ITO exist. First, the power dissipated by other circuits than the CUT that generate a thermal imbalance that superimposes to the one generated by the CUT. Second, the power dissipated by the CUT itself. To clarify this point, the works [4,9] have analysed the DC power dissipated by a Power Amplifier used as CUT, and it turns out that it can be written as the addition of two components:

$$P_{CUT\_DC} = P_{bias} + P_{RF} \quad (3)$$

where $P_{BIASias}$ stands for the power dissipated due to the DC bias and P_{RF} stands for the DC power dissipated by the Power Amplifier due to the processing of high frequency AC electrical signals. Interestingly, P_{RF} usually has negative sign, meaning that when the power amplifier is only biased, the maximum DC self-heating (and therefore the maximum thermal coupling) occurs. When AC signals are applied to the PA's input, this self-heating decreases, as part of the energy previously dissipated by the PA is now delivered to the load (nice infra-red thermographic images showing this fact are available in [9]).

Both power dissipation components contain interesting information. For instance, monitoring P_{bias} trough temperature measurements has been used in [3] to perform structural test of low noise amplifiers, whereas monitoring the evolution of P_{RF} has been used in [4] to measure the central frequency and 3 dB bandwidth of the PA in figure 6. In [9] both components are measured in order to obtain the efficiency of a PA designed to work in the ISM band. Another usual characteristic is that $/P_{bias}/ >> /P_{RF}/$. That implies that if the target is to measure P_{RF}, the sensor sensitivity should be high (which implies a low dynamic range). It this scenario, when P_{RF} is the final measurement goal, then P_{BIAS} generates a $(T_2\text{-}T_1)_{OFFSET}$ that, as in the case of Figure 4, might saturate the temperature sensor, and no measure of P_{RF} could be performed. Clearly, the temperature difference generated by P_{BIAS} can be modelled as well as an input temperature offset, ITO.

In all the works referred above, the IC measured were research proof of concepts, where the CUT and the differential temperature sensor where the only circuits placed in the IC. In real applications, other devices/circuits can dissipate power and, therefore, prior biasing the targeted CUT, the two temperature transducers can already experience a temperature difference which may saturate the sensor.

In Fig. 5, the function of the controlled current sources driven by the signals V_{CMp} and

V_{VMn} is to remove current from either one or another differential pair branch, to the final end or either balancing or unbalancing currents flowing through the temperature transducers and current mirrors. As measured in Fig. 7, they shift the sensor's input-output characteristic either to the left or to the right.

To better illustrate the effects of these current sources, let's analyze two of the plots with deeper detail:

Analysis 1: when V_{CMp} = 500 mV and V_{CMn}= 0 V, the sensor linear range goes approximately from 15 mW to 23 mW, when dissipated by Heat 2. This setting could compensate the ITO if the CUT were *Heat 2* and its P_{BIAS} were about 22 mW and P_{RF} went from 1mW to -7 mW. With this bias, the temperature differences generated by P_{RF} would completely fall within the sensor's linear range and measurements could be done with maximum sensitivity.

Analysis 2: when V_{CMp} = 0 V and V_{CMn}= 450 mV the linear range is from 11 mW to 19 mW dissipated by *Heat 1*. This setting could compensate for the external ITO generated, considering that the CUT is *Heat 1* with P_{BIAS} = 18 mW. Then, the linear range of P_{RF} goes from 1 to -7 mW. In other words, this setting compensates for an ITO equivalent to the dissipation of 18 mW by *Heat 1*.

As a final remark from the two previous examples, due to negative nature of P_{RF}, if the dynamic range wants to be maximized, the sensor should be biased at one of the edges between saturation and linear behavior. The particular edge depends on the location of the CUT in respect to the temperature transducers.

The suitable values of V_{CMp} and V_{CMn} can be automatically adjusted with a calibration procedure prior to P_{RF} measurements using a low cost microprocessor, following the algorithm depicted in Fig. 8: During the initialization phase both V_{CMp} and V_{CMn} are set to ensure that both current sources are cut-off. The sensor's output voltage is read by the microprocessor analog to digital converter. Comparison is digitally performed. As low cost microprocessors does not usually have digital to analog converters, the analog voltages that drive the voltage controlled current sources can be generated by low pass filtering a pulse width modulated digital signal.

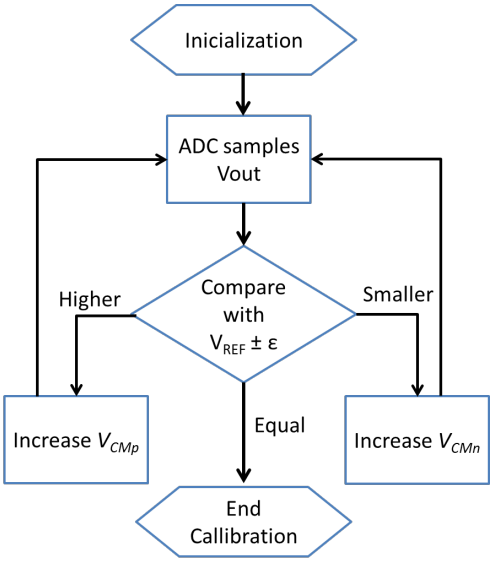

Figure 8: Algorithm implemented by the digital circuitry during calibration mode.

We have implemented this algorithm using the Atmega 32u4 microprocessor, which has a 10 bits analog to digital converter. Analog signals have been generated with a 490 Hz pulse width modulation digital signal, whose duty cycle can be adjusted with 8 bits precision. We have implemented a second order passive low pass filter, with a cut-off frequency of 32 Hz. As a result, the controlling voltages are set with a 0,02 V/bit sensitivity. Using the temperature sensor reported in [7], we have selected V_{REF} to be $V_{DD}/2$ (The sensor in [7] is biased with V_{DD} = 5V), with a tolerance $\boldsymbol{\varepsilon}$ of 0,1 V. We have used the heat sources to emulate the DC power dissipated by a CUT. First, we have emulated three different values of P_{BIAS}: 5 mW, 10 mW and 15 mW. Once the thermal steady state is reached (i.e., a $(T_2\text{-}T_1)_{Offset}$ is generated), the calibrating algorithm is activated. When finished, we have emulated different values of $P_{RF.}$ Fig. 9 shows the sensor output voltage as a function of the total power dissipated by the heat source (P_{DC}+P_{RF}). Thanks to the calibration process, when P_{bias} = 5 mW, the graph intersects the point (5 mW, 2,5 V), when Pbias = 10 mW, it intersects the point (10 mW, 2,5 V), whereas when Pbias = 15 mW, it intersects the point (15 mW, 2,5 V). As a result of the calibration process, the sensor is biased to track P_{RF} with the highest sensitivity regardless the ITO generated by the P_{BIAS}.

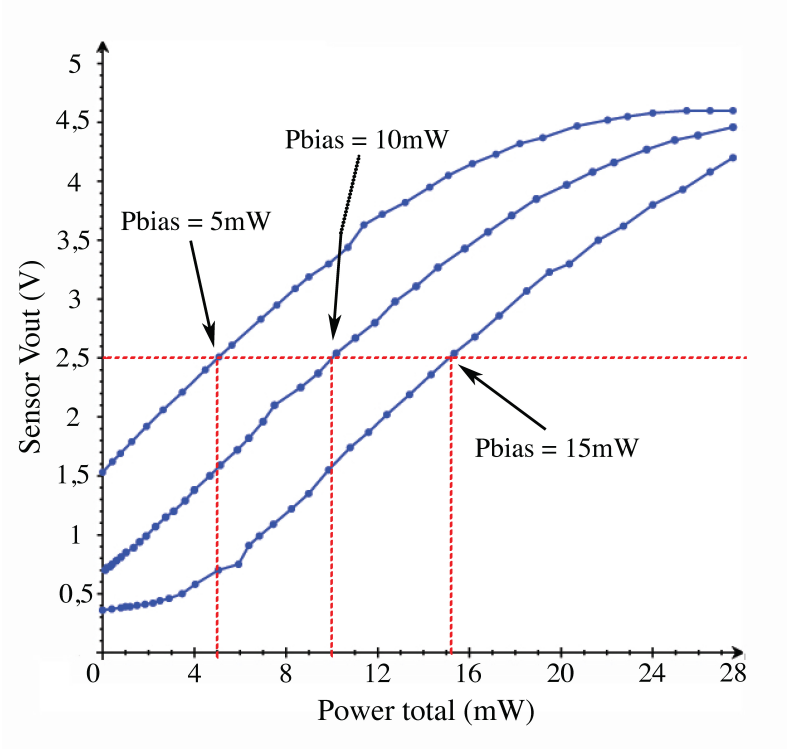

Figure 9: Temperature sensor transfer function after three different calibrating process have been done to compensate for the external ITO generated by the MOS transistor.

3. Differential temperature sensor topology with digital offset compensation, high input range and high sensitivity.

The automatic offset compensation procedure as demonstrated in the previous section is not feasible if it has to be built-in within the CUT. The filter that provides the analog voltages requires values of capacitance too big to be integrated. The use of the filter can be avoided with the sensor architecture proposed in Fig. 10.

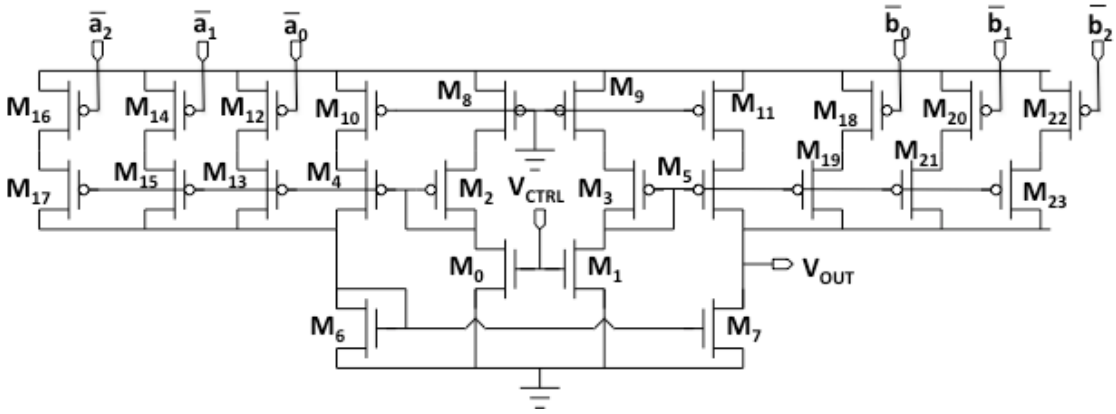

Figure 10: Differential temperature sensor with digital offset callibration. .

In Fig. 10, the temperature transducers are the MOS transistors M_0 and M_1: MOS transistors may offer some advantages over Bipolar transistors when implementing temperature sensors for test pourposes [10,11]. V_{CTRL} sets for both temperature transducers the same gate to source bias. Depending on this bias, the sensitivity of the drain current to temperature, $\frac{\partial I_D}{\partial T}$, can be positive, zero or negative [12]. Similarly to the topologies already presented, the current mirrors (M_2-M_4, M_3-M_5 and M_6-M_7) conduct the current difference within the differential pair to the high resistance output node, where the current to voltage conversion is performed. As the drain current sensitivity to temperature is higher in absolute value when the temperature transducer is working in weak inversion, and then the differential pair is biased in this operation mode, accurate sizing of transistors within the current mirrors has to be done to ensure that these transistors work in saturation even for low V_{CTRL} values. The final sensitivity of the sensor can be adjusted with the aspect ratio of the current mirrors and the sensor's output resistance, which depends as well on the drain to source current in M_5 and M_7.

The main novelty is the two current sources that compensates for ITO. Each current source is formed by the parallel of three MOS transistors, which are M_{17}, M_{15} and M_{13} for the first source and M_{19}, M_{21} and M_{23} for the second one. The function of these transistors is to behave as a parallel of weighted current sources. To this end, the relative width of the transistors that form each source is: $W_{M17} = 2 \cdot W_{M15} = 4 \cdot W_{M13}$; $W_{M23} = 2 \cdot W_{M21} = 4 \cdot W_{M19}$ with $W_{M13} = W_{M19}$. The current value provided by each current source is digitable controlable with the digital vectors $a_2a_1a_0$ and $b_2b_1b_0$ encoded in binary natural, which drive transistors M_{12}-M_{14}-M_{16} and M_{18}-M_{20}-M_{22} behaving as switches. If we focus on the source formed by M_{17}, M_{15} and M_{13}, let us define N as the number that can be encoded in binary with the bits $a_2a_1a_0$. The drain current of transistor M_6 can be written as the sum of three terms: the bias current, the current variation due to the thermal coupling between the CUT and transistor M_0 and the current injected by the current source formed by transistors M_{17}, M_{15} and M_{13}:

$$I_{D6} = K_{2\_4} \cdot I_{D0Q} + K_{2\_4} \cdot \Delta T_{M0} \cdot \left.\frac{\partial I_{D0}}{\partial T}\right|_{I_{D0}=I_{D0Q}} + N \cdot K_{2\_13} \cdot I_{D0Q} \qquad (4)$$

where K_{2_4} and K_{2_13} are the width ratio of transistors that form the current mirrors M_2-M_4 and M_2-M_{13}. I_{D0} is the expression of the M_0 drain current, which depends on the bias voltage V_{CTRL}, I_{D0Q} is the M_0 bias drain current value and ΔT_{M0} is the temperature

increase of M_0 in respect to the bias temperature. This expression assumes that $N \cdot K_{2\_13} < K_{2\_4}$.

Depending on the digital code applied to the current source, the sensor input-output characteristic is either shifted towards right or towards left, correcting an ITO equal to:

$$\Delta T_{M0} = -\frac{N \cdot K_{2\_13} \cdot I_{D0Q}}{K_{2\_4} \cdot \frac{\partial I_{D0}}{\partial T}_{I_{D0}=I_{D0Q}}} \tag{5}$$

Simulation results are in Fig. 11. when the sensor is implemented in a 0,35 microns CMOS technology. In this plot, horizontal axis is temperature difference, whereas the transfer function plotted depends on the digital code applied to the current sources.

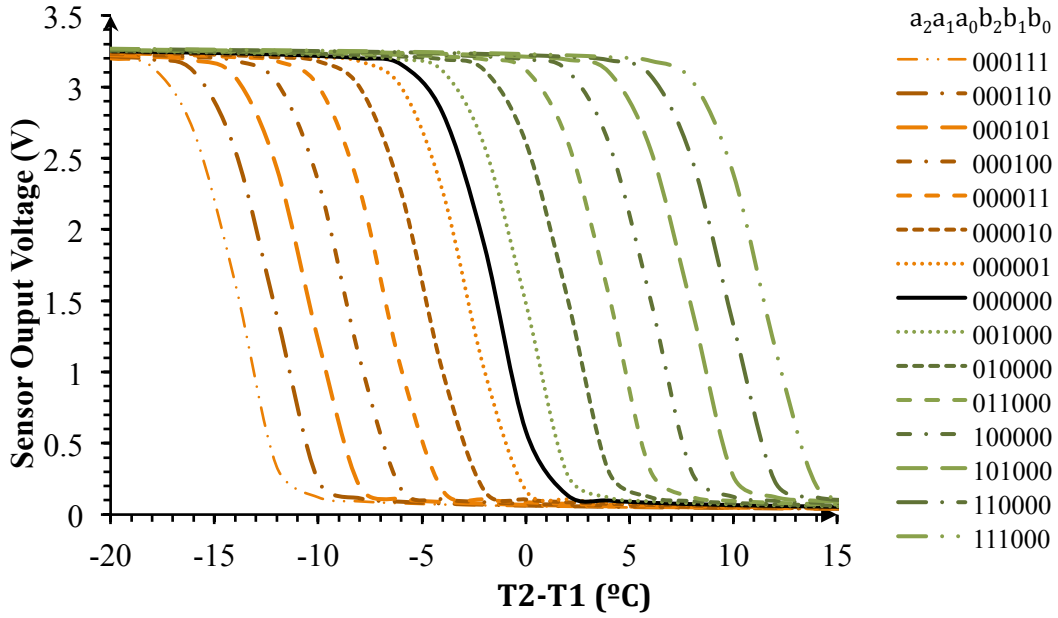

Figure 11: Sensor transfer function as a function of the digital code used in the callibration current sources.

With this sensor architecture, the hardware needed to perform the callibration could be composed of two comparators, which inform if the sensor output voltage is higher of smaller than the reference voltage (V_{REF} in Fig. 8). The comparator's output voltages can drive a simple state machine, which would activate when needed the enable of the two binary counters that generate the A and B codes for the sensor.

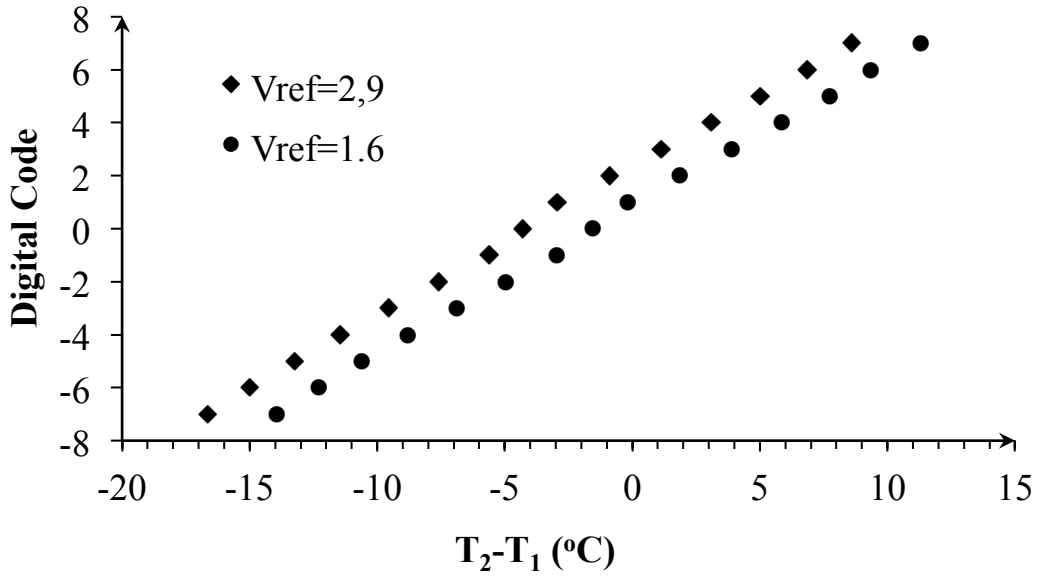

Figure 12: Digital code that should be applied to the current sources in order to compensate for the ITO indicated in the horizontal axis and to set the sensor's output voltage to the V_{ref} value.

Fig. 12 shows the digital code that should be applied to the current sources to compensate for different values of ITO and to set the sensor's output voltage to V_{ref}. In the vertical axis of Fig. 12, positive values represent the binary code that should be applied $a_2a_1a_0$, whereas negative values represent the absolute value should be applied to $b_2b_1b_0$. The horizontal axis shows the ITO that this particular arquitecture can compensate for. Wider range can be achieved by increasing the range of the current sources. Results in Fig. 12 are plotted for two different V_{ref} values: $V_{dd}/2$ (=1,6 V) and 2,9 V. This latter value would be the edge between the saturation region and the linear region acording the results in Fig. 11.

This figure indicates another possible application of this circuitry: digital output differential temperature sensor. This idea is suggested by eq. (5). The temperature difference sensed by the sensor can be written as:

$$\Delta T = S_{TD} \cdot (N_1 - N_0) \qquad (6)$$

Where S_{TD} is the inverse of the slope of functions in Fig. 12, which relates the digital code with the tempeature increase, N_0 is the digital code that has been obtained before CUT activation to compensate for ITO (i.e. the code needed to set the sensor output voltage to V_{REF}), and N_1 is the digital code needed to retrieve the sensor's output voltage to V_{REF} once the CUT has been activated and the temperature gradient to measure has been generated. If we compare the plots in Figs. 11 and 12, we see that the

transfer functions in Fig. 11 have a dynamic range of about 4,5 ºC, whereas the ones in Fig. 12 have a dynamic range of about 30ºC. As usually, $P_{bias} >> P_{FR,}$ the digital output can be used to measure the temperature gradient generated by $P_{bias,}$ whereas the analog output can be used to track the evolution of P_{FR} . This sensor topology is suitable for the applications reported in [3] or [9], where both P_{bias} and P_{FR} should be measured in order to perform the CUT test/characterization. Higer resolution can be achieved with more bits and with lower MOS aspect ratio (in this example all transistors that form the current source have L=3 microns, being the smallest W equal to the L, and just 3 bits have been considered per current source, in order to clearly present the effect of the digital code in the sensor's transfer function).

4. Conclusions.

In this paper we have reviewed the differentes causes of offset that can alter a differentail temperature sensor and we have presented a new sensor architecture that allows offset correction in those differential temperature sensors and widens the sensor input range, allowing to measure both the temperature increases generated by the circuit under test during DC bias and due to its high frequency activity. Detailed characterization of the offset sources has been done with a differential temperature sensor implemented in a 65 nm CMOS technology.

Acknowledgements

This work has been partially supported by the Spanish MINECO and ERDF (TEC2013-45638-C3-2-R).

REFERENCES

[1] X. Tang, W. Tung Ng, K. P. Pun, A Resistor-Based Sub-1-V CMOS Smart Temperature Sensor for VLSI Thermal Management, *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on,* On page(s): 1651 - 1660 Volume: 23, Issue: 9, Sept. 2015

[2] T. Oshita, J. Shor, D. E. Duarte, A. Kornfeld, D. Zilberman, Compact BJT-Based Thermal Sensor for Processor Applications in a 14 nm tri-Gate CMOS Process, *Solid-State Circuits, IEEE Journal of,* On page(s): 799 - 807 Volume: 50, Issue: 3, March 2015

[3] L. Abdallah, H. Stratigopoulos, S. Mir, J. Altet, Defect-oriented non-intrusive RF test using on-chip temperature sensors, Proc. 2013 31th IEEE VLSI Test Symposium, 29 April 2013, Berkeley, CA.

[4] X. Aragonés, D. Mateo, J.L. Gonzalez, E. Vidal, D. Gomez, B. Martineau, J. Altet, DC Temperature

measurements to Characterize the Central Frequency and 3dB Bandwidth in MMW Power Amplifiers, IEEE Microwave and Wireles Components Letters, Nov. 2015, pp. 745-747.

[5] S.M. Bowers, K. Sengupta, K. Dasgupta, B.D. Parker, A. Hajimiri, Integrated Self-Healing for mm-Wave Power Amplifiers, IEEE Transactions on Microwave Theory and Techniques, March 2013, pp. 1301-1315.

[6] F. Reverter, D. Gomez, J. Altet, On-Chip MOSFET Temperature Sensor for Electrical Characterization of RF Circuits, IEEE Sensors Journal, Sep. 2013, pp. 3343-3344.

[7] J. Altet, A. Rubio, E. Schaub, S. Dilhaire, W. Claeys, Thermal coupling in integrated circuits: application to thermal testing, IEEE Journal of Solid State Circuits, Vol. 36, no. 1, Jan. 2001, pp. 81-91.

[8] M. Onabajo, J. Silva-Martinez,Analog Circuit Design for Process Variation Resilient Systems-on-a-Chip", Springer, New York 2012.

[9] J. Altet, D. Gómez, X. Perpinyà, D. Mateo, J.L. González, M. Vellvehi, X. Jordà, Efficiency determination of RF linear power amplifiers by steady-state temperature monitoring using built-in sensors, Sensors and Actuators A: Physical, Vol. 192, 1 April 2013, pp. 49.57.

[10] F. Reverter, X. Perpiñà, E. Barajas, J. Leon, M. Vellvehi, X. Jordà, J. Altet, MOSFET dynamic termal sensor for IC testing applications, Sensors and Actuators A: Physical, Vol., 242, 1 May 2016, pp. 195-202.

[11] F. Reverter, J. Altet, On-Chip Thermal Testing Using MOSFETs in Weak Inversion, IEEE Transactions on Instrumentation and Measurement, Vol. 64, no. 2, pp. 524-532, Feb. 2015.

[12] I. M. Filanovsky, A. Allam, "Mutual compensation of mobility and thereshold voltage temperature effects with applications in CMOS circuits", IEEE trans. Circuits Syst. I Fundam. Theory Appl., Vol. 48, no. 7, pp. 876-884, Jul. 2001.