UNIVERSITAT POLITÈCNICA DE CATALUNYA
BARCELONATECH

Departament d'Enginyeria Electrònica

Control and Modulation of Modular Multilevel Converters

Thesis submitted in partial fulfilment of the requirement for the PhD Degree issued by the Universitat Politècnica de Catalunya, in its Electronic Engineering Program.

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October 2016

Originality Statement

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Signed:

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Dedicated to Antònia, Josep and Oriol.

Acknowledgements

First of all, I would like to express my appreciation to my supervisors, Dr. Josep Pou and Dr. Jordi Zaragoza, for their guidance and support in the development of this PhD thesis. Dr. Pou convinced me to pursue this PhD and, despite the distance, he has continued to motivate me and suggest solutions for every challenge. Dr. Zaragoza has stood by my side every day, doing the hard work of supporting me and giving advice in the easy and difficult moments. I have great admiration for both of them, and I thank them for having believed in me from the start.

I would like to thank Dr. Salvador Ceballos, who has inspired some of the ideas developed in this thesis and who has always shared his knowledge with me.

I would like to thank all my colleagues from the Universitat Politècnica de Catalunya in the Electronic Engineering Department in Terrassa, for their advice and encouraging words when things became difficult. Particularly, I would like to thank Biel for his help and advice, not only in electronics but also in LaTeX, English language and technical writing. I also want to thank Josep, Juan and Manel for our interesting and useful talks. And a very special thanks to my friend Néstor, who is always motivating me with new ideas and has given me good advice for work and for life.

I would like to thank Dr. Alan Watson for giving me the opportunity to stay at the Power Electronics, Machines and Control group at the University of Nottingham. My stay in Nottingham was a very pleasant experience, where I made very good friends and learnt a lot. I would especially like to thank Jordi, who helped me before and after arriving there, and who also became a good friend. I also want to thank Marco, Jonathan and Miquel for giving me the opportunity to participate in the Moto-E experience; and Ewan, Marija and Sharmila for their help in the PEMC.

Finally, I would like to thank all my friends and family who always listen patiently to my long stories. And very specially, I would like to thank my parents Josep and Antònia and my brother Oriol, to whom I dedicate this thesis, because they have always helped and supported me, during both the good and the bad moments.

This work has been supported by the Ministerio de Economía y Competitividad of Spain under the scholarship *Ayudas para contratos predoctorales para la formación de doctores 2013* (BES-2013-063590).

Abstract

The integration of renewable energy sources in the electrical grid is reducing our dependence on fossil fuels. However, to ensure feasibility and reliability of distributed energy generation, more efficient and higher power converters are required. The modular multilevel converter (MMC) is a modern topology of multilevel converter that is very attractive for medium- and high-voltage/power applications, including high-voltage direct current transmission systems and high-power motor drives.

The main features of the MMC are modularity, scalability to different power and voltage levels, redundancy and high quality output voltages and currents. However, the operation of the MMC is complex, and there are some issues that still have to be further investigated. One of these issues is the voltage ripples of the submodule (SM) capacitors. The voltage ripples define the minimum value of the capacitances needed for the converter, and therefore its overall size and cost. The use of a proper circulating current controller can reduce the voltage ripples. In this thesis, three techniques for calculating the circulating current reference are presented: two techniques based on optimization functions for minimizing the capacitor voltage ripples; and a fast-processing technique that provides results close to optimal.

The capacitor voltage ripples can also be reduced by adding a zero-sequence signal to the modulation signals. In this thesis, the application of discontinuous modulation to the MMC is proposed for the first time. This technique is based on the injection of a discontinuous zero-sequence signal and highly reduces the switching power losses and capacitor voltage ripples.

Real applications of the MMC are composed of a high number of SMs. This implies a challenge in the control system, including the data acquisition system. A new technique for measuring the capacitor voltages with only a few sensors has been presented in this thesis. From the output voltage provided by a group of SMs, the individual voltage of each one of them can be acquired. Since acquisition cannot be performed at each sampling time, the capacitor voltages are calculated between samples using an estimation algorithm.

Reliability is a feature required in industrial applications. The structure of the MMC facilitates the existence of redundant SMs, but faults need to be detected and localized

for deactivating the faulty component. This thesis presents a robust and fast strategy for detecting, localizing and correcting faults in SMs and voltage sensors. The technique is based on three additional sensors per arm, which measure the output voltage of a group of SMs and compare it with the expected voltage.

Capacitance differences between the SMs can appear due to component tolerance or ageing of the capacitors. Capacitance mismatches cause uneven distribution of the power losses, thus increasing the thermal stress of some semiconductors, and therefore, their probability of failure. A power loss balancing technique has been proposed, equalising the losses in all the SMs and therefore avoiding the concentration of power losses in some SMs. Application of the MMC to motor drive applications has also been studied in this thesis. The operation of the MMC at low motor speeds/frequencies is still a challenge, since the capacitor voltage ripples are inversely proportional to the current frequency. In this thesis, it has been demonstrated that discontinuous modulation can help to reduce capacitor voltage ripples in motor drive applications, achieving very low speed operation. The technique is compared with other state-of-the-art methods, and it achieves similar capacitor voltage ripples and a significant reduction in power losses.

All the control and modulation techniques proposed in this thesis have been studied by simulation in the MATLAB/Simulink environment and corroborated experimentally on low-power laboratory prototypes.

Resum

La integració de fonts d'energia renovables a la xarxa elèctrica està reduint la nostra dependència dels recursos fòssils. Però per tal d'assegurar la viabilitat i fiabilitat de la generació d'energia distribuïda, fan falta convertidors estàtics més eficients i de més potència. El convertidor multinivell modular (MMC) és una topologia de convertidor multinivell recent, molt prometedora per aplicacions de mitja i alta potència, com són els sistemes de transmissió d'energia en corrent continua o els accionaments de motors d'alta potència.

Els principals avantatges del MMC són modularitat, escalabilitat en tensió i potència, redundància i gran qualitat de la tensió i corrent de sortida. El funcionament del MMC, però, és complex i encara hi ha alguns problemes que s'han d'investigar amb més profunditat. Un dels problemes és l'arrissat de tensió del condensador de sub-mòdul (SM). L'arrissat de tensió defineix el valor mínim d'aquests condensadors i per tant, el seu cost. L'ús d'un corrent circulant adequat pot reduir l'arrissat de tensió. En aquesta tesi es presenten tres tècniques per calcular la consigna del corrent circulant: dues tècniques basades en funcions d'optimització que minimitzen l'arrissat de tensió i una tècnica d'aplicació més simple, la qual proporciona resultats pròxims als òptims però que es pot calcular més ràpidament.

L'arrissat de tensió també es pot reduir afegint un component homopolar en els senyals de modulació. En aquesta tesi es proposa per primera vegada l'ús de la modulació discontinua per al MMC. Aquesta tècnica, basada en la injecció d'un component homopolar, permet una gran reducció de l'arrissat de tensió i de les pèrdues de commutació.

Les aplicacions reals del convertidor MMC es componen per un gran nombre de SMs. Això implica un repte en el disseny del sistema de control, particularment en l'etapa d'adquisició de dades. Aquesta tesi presenta un nou sistema de mesura per a les tensions dels condensadors de SM, en el qual es necessiten pocs sensors. A partir de la tensió de sortida d'un grup de SMs, el sistema pot adquirir la tensió de cada un d'ells. Com que l'adquisició no es pot fer a cada període de mostreig, entre adquisicions la tensió es calcula mitjançant un algoritme d'estimació.

Un dels requisits de les aplicacions industrials és la fiabilitat. L'estructura del MMC permet l'ús de SMs redundants, però les fallades s'han de detectar i localitzar per tal de desactivar el component erroni. En aquesta tesi es presenta un sistema ràpid i robust de detecció, localització i correcció de fallades en SMs i sensors de tensió. El sistema es basa en l'ús de tres sensors addicionals per semi-branca, els quals mesuren la tensió de sortida d'un grup de SMs i la comparen amb la tensió esperada.

A causa de la tolerància o l'envelliment dels condensadors, poden aparèixer diferències en la capacitat dels SMs. Aquestes diferències causen una mala distribució de les pèrdues dels semiconductors, incrementant l'estrès tèrmic d'alguns dels components i la probabilitat de fallada. Per això, es proposa un algoritme d'equilibrat de pèrdues, el qual iguala les pèrdues dels SMs i n'evita la concentració en algun SM.

En aquesta tesi també s'ha estudiat l'aplicació del MMC en accionaments de motors. El funcionament del MMC a baixa velocitat/freqüència del motor és un repte encara no resolt, ja que l'arrissat de tensió dels condensadors és inversament proporcional a la freqüència del corrent. Aquesta tesi demostra que la modulació discontinua es pot utilitzar per reduir l'arrissat de tensió en aquesta situació, aconseguint un bon funcionament a molt baixa velocitat. En comparació amb altres tècniques actuals de baixa velocitat, la modulació discontinua aconsegueix un arrissat de tensió similar i una reducció de les pèrdues.

Totes les tècniques proposades en aquesta tesi s'han estudiat mitjançant simulació en l'entorn MATLAB/Simulink i s'han corroborat experimentalment en prototips de laboratori.

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List of Acronyms

Acronym	*Definition*
AAC	Alternative arm converter
ac	Alternating current
AERI	Australian Energy Research Institute
APOD-PWM	Alternative phase-opposition disposition pulse-width modulation
CB-SVPWM	Carrier-based space-vector pulse-width modulation
CL-DPWM	Closed-loop discontinuous pulse-width modulation
CMsin	Low-speed technique based on a sinusoidal zero-sequence
CMsqr	Low-speed technique based on a square zero-sequence
dc	Direct current
DEE	Departament d'Enginyeria Electrònica
DSP	Digital signal processor
EMI	Electro-magnetic interference
FACTS	Flexible alternating current transmission system
FC	Flying capacitors
FPGA	Field programmable gate array
HVDC	High-voltage direct current
IGBT	Isolated-gate bipolar transistor
IMB-CNM	Institute of Microelectronics of Barcelona - Centro Nacional de Microelectrónica
LS-PWM	Level-shifted pulse-width modulation
MEC	Modulated energy control
MMC	Modular multilevel converter
MOSFET	Metal-oxide-semiconductor field-effect transistor
MTTF	Mean time to failure

NLM	Nearest level modulation
NPC	Neutral point clamped
OC	Open-circuit
OL-DPWM	Open-loop discontinuous pulse-width modulation
PEMC	Power Electronics, Motors and Control (group)
PCB	Printed-circuit board
PD-PWM	Phase-disposition pulse-width modulation
PI	Proportional integral
PLL	Phase-locked loop
PMSM	Permanent magnet synchronous machine
POD-PWM	Phase-opposition disposition pulse-width modulation
PR	Proportional resonant
PS-PWM	Phase-shifted pulse-width modulation
PWM	Pulse-width modulation
rms	Root mean square
RL	Resistive-inductive
SC	Short-circuit
SHE	Selective harmonic elimination
SM	Submodule
SPWM	Sinusoidal pulse-width modulation
STATCOM	Static compensator
STB	Switching transition balancing (algorithm)
SVM	Space-vector modulation
THD	Total harmonic distortion
TIEG-P	Terrassa Industrial Electronics Group - Power
TLB	Total loss balancing (algorithm)
UNSW	University of New South Wales
UPC	Universitat Politècnica de Catalunya
VDPWM	Virtual discontinuous pulse-width modulation
VOC	Voltage oriented control
VSC	Voltage-source converter

List of Symbols

Symbol	Definition
A_{cr}	Amplitude of the carrier signal v_{cr}
C	Submodule capacitor
C_{dc}	dc-link capacitor
C_{est}	Estimated capacitance
C_{jz}	Arm equivalent capacitor, j being the phase identifier $j \in \{a, b, c\}$ and the arm identifier $z \in \{u, l\}$
C_{real}	Real capacitance
C'_{jz}	Equivalent submodule capacitor in the arm z of phase j of the equivalent energy model
$C_{jz_{eq}}$	Equivalent arm capacitor in the arm z of phase j of the equivalent energy model
$Cnt_{z(n)}$	Counter of cycles without updating the estimator, z being the arm identifier and (n) the number of submodule
$d_{jz(n)}$	Duty cycle of submodule (n) in arm z and phase j
$e_{exp\ z(k)}$	Expected set error in the arm z, k being the number of set
$e_{t\ z(k)}$	Theoretical set error in the arm z and set k
E_{on}	IGBT turn-on energy loss
E_{off}	IGBT turn-off energy loss
E_{rec}	Diode reverse recovery energy
f	ac-side current fundamental frequency
f_{cr}	Carrier frequency
f_{samp}	Sampling frequency
f_{sin}	Frequency of the zero-sequence voltage used in CMsin
f_{sqr}	Frequency of the zero-sequence voltage used in CMsqr

f_{sw}	Switching frequency
F_{opt}	Optimization function
h	Harmonic order identifier
i_{jcomm}	Common mode current at phase j
i_d	d-component of the stator current in a synchronous reference frame
i_d^*	i_d reference
i_D	Diode current
i_{dc}	dc component in the circulating current
i_{jdiff}	Differential or circulating current at phase j
i_j	ac-side current of phase j
i_{jz}	Current of arm z of phase j
i_q	q-component of the stator current in a synchronous reference frame
i_q^*	i_q reference
i_T	IGBT current
i_{Wjz}^*	Circulating current reference for controlling the energy in the arm z of phase j
I_{ac}	Amplitude of the ac-side current
I_{jdiff0}	Initial differential current at phase j
I_N	Rated current of the motor
j	Phase identifier, where $j \in \{a, b, c\}$
(k)	Number of the measuring set, where $k \in \{1, ..., nS\}$
k_{jz}	Ratio between the average measured submodule capacitor voltage and the theoretical submodule capacitor voltage of arm z of phase j
K_{device}	Gain of the TLB algorithm for a particular kind of device i.e., upper IGBT, upper diode, lower IGBT or lower diode
$K_{enforced}$	Gain of the enforced activation method
K_h	Amplitude of the hth harmonic component in the circulating current
K_{lim}	Gain of the CL-DPWM proportional limit
K_{RSF}	Gain of the feedback loop in the voltage balancing algorithm with reduced switching frequency
K_{sw}	Gain of the STB algorithm
l_j	Number of activated submodules in the lower arm of phase j
L	Arm inductor

L_{ac}	Grid inductor
L_{out}	Load inductor
L_d	Equivalent stator inductance in the d-component of a synchronous reference frame
L_q	Equivalent stator inductance in the q-component of a synchronous reference frame
m	Modulation index
M	Number of additional submodules per arm
n	Number of output levels of the converter
(n)	Number of the submodule, where $n = \{1, ..., N\}$
nS	Number of measuring sets per arm
nM	Number of submodules per measuring set
nT	Number switching transitions in a fundamental period
N	Number of basic submodules per arm
O_{lim}	Offset of the CL-DPWM proportional limit
p	Number of pole pairs of the motor
p_z	Instantaneous power in the arm z
P_{cond}	Conduction power losses
P_N	Nominal power of the motor
P_{out}	Output power
P_{sw}	Switching power losses
P_{tot}	Total power losses
R_{CE}	IGBT equivalent series resistor
R_D	Diode equivalent series resistor
R_{out}	Load resistor
R_s	Stator resistance
$R(t)$	Reliability function
$s_{jz(n)}$	Control function defining the state of the submodule (n) of arm z of phase j
$s_N(v_{Cz})$	Standard deviation of the submodule capacitor voltages of arm z
t	Time
T	Fundamental period
T_e	Rated torque of the motor
u_j	Number of activated submodules in the upper arm of phase j

U_{sin}	Amplitude of the zero-sequence voltage used in CMsin
U_{sqr}	Amplitude of the zero-sequence voltage used in CMsqr
v_{ac}	ac-voltage generated by the arms
v_{Az}	Supervisory arm sensor voltage of the arm z
$v_{Cjz(n)}$	Submodule capacitor voltage, j being the phase identifier, z the arm identifier and (n) the number of submodule
v_{jcomm}	Common mode voltage at phase j
v_{cr}	Modulation carrier signal
$v^*_{Cz(n)}$	Capacitor voltage of submodule (n) of arm z modified by the enforced measuring algorithm
v_{Czavg}	Average value of all the submodule capacitor voltages in the arm z
v_d	d-component of the stator voltage in a synchronous reference frame
v_{jdiff}	Differential voltage at phase j
v_j	ac-side voltage of phase j
v_{jd}	Discontinuous modulation signal of phase j
v_{jm}	Modulation signal of phase j
v_{jz}	Voltage provided by the arm z of phase j
v_{jzd}	Discontinuous modulation signal for the arm z
v_{jzff}	Arm z of phase j modulation signal after feed-forward compensation
v_{jzm}	Arm z of phase j modulation signal
v_q	q-component of the stator voltage in a synchronous reference frame
v_{SMjz}	Output voltage of the submodule (n) of arm z of phase j
$v_{Sz(k)}$	Measuring set voltage, z being the arm identifier and (k) the number of set
$v_{Sz(k)\ exp}$	Expected voltage of the set (k) of arm z
$v_{Sz(k)\ t}$	Theoretical voltage of the set (k) of arm z
v_{zs}	Zero-sequence voltage
V_{CE}	IGBT collector-emitter saturation voltage
$V_{Cjz(n)0}$	Initial voltage of the capacitor (n) of arm z and phase j
$V_{Cz(n)S}$	Submodule capacitor voltage acquired through a measuring set, z being the arm identifier and (n) the number of submodule
V_{dc}	dc-link voltage
V_F	Diode forward voltage

V_g	Amplitude of the grid voltage
W_{Cjz}	Energy stored in the arm z of phase j
W^*_{Cjz}	Arm energy reference for the arm z of the phase j
x	Voltage level designed by the modulator
$\overline{y}$	Locally averaged value of the variable y
y_{norm}	Normalized value of the variable y
y_{rms}	rms value of the variable y
z	Arm identifier, where z indicates the upper arm (u) or the lower arm (l)
Z_{out}	Output impedance
δ	Variation of the capacitor voltages in the enforced measuring algorithm
δW_{Cjz}	Interval energy variation in the arm z
$\Delta v_{Cjz(n)}$	Submodule capacitor voltage ripple amplitude, j being the phase identifier, z the arm identifier and (n) the number of submodule
Δv_{est}	Estimated voltage variation in a submodule capacitor
Δv_{jm}	Differential control signal of phase j
Δv_{real}	Voltage variation in a submodule capacitor
Δv_{zs}	Zero-sequence compensation for the OL-DPWM
ΔW_{Cj}	Energy difference between upper and lower arms of phase j
ΔW^*_{Cj}	Energy difference reference for phase j
$\Delta\varphi$	Phase displacement between carriers in PS-PWM
λ_A	Failure rate of a supervisory arm sensor
λ_I	Failure rate of an individual submodule sensor
λ_m	Magnetic flux of the motor permanent magnets
λ_S	Failure rate of a supervisory set sensor
λ_{SM}	Failure rate of a submodule
ΣW_{Cj}	Total energy stored in the phase-leg j
ΣW^*_{Cj}	Phase-leg j total energy reference
φ	Output current phase angle
φ_h	Phase angle of an harmonic component in the circulating current, h being the harmonic order
ω	Fundamental angular frequency
ω_e	Electrical frequency of a motor
ω_N	Nominal speed of a motor

ω_o	Mechanical speed of a motor
ω_{sin}	Frequency, in rad/s, of the zero-sequence voltage used in CMsin
$\nabla F(x, y)$	Gradient of a multivariable function

Chapter 1

Introduction

This chapter presents the context and motivation for this research work. It includes a review of the previous research about modelling, modulation strategies, control techniques and fault-tolerant strategies for the MMC. This chapter also states the main objectives of this thesis and includes a list of the publications derived from it. To conclude, the thesis outline and the main contributions are presented.

1.1 Research Environment

The present thesis was developed in the Departament d'Enginyeria Electrònica (DEE) at the Universitat Politecnica de Catalunya (UPC), in the Terrassa Industrial Electronics Group – Power (TIEG-P). The main interests of the research group are:

- Electromagnetic compatibility: Electromagnetic interference (EMI) modelling, diagnostic and mitigation techniques for industrial environments, in vehicles, ships and aircraft.
- Renewable energy: Modelling and design of power converters for wind and photovoltaic (PV) systems.
- Power quality in electric systems: Measuring and correcting power supply disturbances in the generation and distribution systems.
- Control techniques for electric drives: Advanced techniques for matrix converters and multilevel converters.

This thesis has been funded mainly by the scholarship *Ayudas para contratos predoctorales para la formación de doctores 2013* (BES-2013-063590), which was granted by Spain's Ministerio de Economía y Competitividad.

Part of this thesis was developed during a research stay in the Power Electronics, Motors and Control (PEMC) group at the University of Nottingham, UK. The research stay was funded by the scholarship *Ayudas a la movilidad predoctoral para la realización de estancias breves en centros de I+D durante el año 2016* (EEBB-I-16-10672), which was also granted by Spain's Ministerio de Economía y Competitividad.

The research developed in this thesis was carried out in collaboration with researchers from the Energy Unit at Tecnalia Research and Innovation, Basque Country, Spain; the Australian Energy Research Institute at the University of New South Wales, Sydney, Australia; and the PEMC group at the University of Nottingham, UK.

This work is part of the activities developed under the projects RURALGRID, Consolider-Ingenio (CSD2009-00046) and CONNECT-DC (ENE2012-36871-C02-01).

The RURALGRID project, *Feasibility study in order to introduce renewable energies by means of microgrids in the Pyrenees Area*, was developed in the framework of the Comunidad de Trabajo de los Pirineos (CTP), which involved research organizations from Aragón (Universidad San Jorge and INYCOM), the Basque Country (Universidad del País Vasco/Euskal Herriko Unibertsitatea, Tecnalia Research and Innovation, and Jema Energy), Catalunya (UPC), Aquitaine (École Supérieure des Technologies Industrielles Avancées, IMS Bordeaux, and LOREKI), and Midi-Pyrénées (École Nationale d'Ingénieurs de Tarbes). In the case of Catalunya, the project was supported by the Secretaria d'Universitats i Recerca of the Departament d'Economia i Coneixement of the Generalitat de Catalunya. The RURALGRID project was devoted to studying the feasibility of implementing micro-grids in the Pyrenees area. New converter technologies were also analysed to improve the energy efficiency of micro-grids and distributed generation systems.

The project CSD2009-00046 of the Consolider-Ingenio Program, *Advanced wide band gap semiconductor devices for rational use of energy*, was funded by the Ministerio de Economía y Competitividad of Spain and was a collaboration between multiple research institutions, one of which was the UPC. It was led by the Institute of Microelectronics of Barcelona (Centro Nacional de Microelectrónica (IMB-CNM)). The CSD2009-00046 project was devoted to studying the use of wide band-gap semiconductor materials, such as silicon carbide (SiC) and Gallium Nitride (GaN), in a new generation of power semiconductor devices. The objectives of this project were to develop new semiconductor devices, characterize the new devices and implement power converters for demonstrating the advantages of the wide band-gap technology. The test converters have been selected to test characteristics such as operation at high temperature, extremely fast response or handling of high voltage.

The CONNECT-DC project, *Topologies and control of power electronic converters for offshore high voltage dc energy transmission*, funded by Spain's Ministerio de Economía y Competitividad, is a collaboration between two research organizations: the UPC and Tecnalia Research and Innovation. The CONNECT-DC project is devoted to analysing a medium-voltage dc transmission architecture for offshore applications. The main feature of this architecture is that the ac to dc current transformation is not located in an offshore platform but is instead distributed to each of the wind turbines. In this way it is possible to eliminate –or at least significantly reduce– the size of the offshore platform, thus reducing the costs of the transmission system. Other targets of this project are: development of control algorithms for wind turbine generators in order to optimize energy conversion efficiency; characterization of wind resources; and the development of control strategies for medium-voltage dc/ac onshore grid-connected power converters, including the modular multilevel converter (MMC).

1.2 Research Motivation

For a long time now, energy production has been dependent on fossil fuels. However, the paradigm has changed over recent decades as a result of the emergence of cleaner and cheaper energy resources. The development and improvement of renewable energy sources has lead to a distributed generation system, where multiple sources are connected to the electrical grid. Power converters allow integrating these energy sources from diverse origins into the electrical grid. The rise of renewable energy sources has led to requirements for higher power and more efficient converters.

Multilevel converters are indeed attractive power conversion topologies for medium- and high-voltage/power applications [1, 2]. The use of multiple semiconductor devices allows distribution of the voltage stress in each device, which increases the maximum ratings of the converter while using cheaper and more efficient semiconductors. Moreover, the multilevel output increases the quality of the ac-voltage, reducing the size and cost of the output filters. Some application fields of multilevel converters are: large electrical machine drives, such as offshore wind turbines; high-voltage direct current (HVDC) transmission systems; and flexible alternating current transmission systems (FACTS). The MMC [3], is a modern topology of multilevel converter that in just a few years has become the principal technology option for HVDC systems [4].

The main feature of the MMC is its modularity, which provides multiple benefits: scalability to different power and voltage levels; reliability with the use of redundant cells; compatibility with commercial semiconductors and easy manufacturing of the system [5,

6]. However, its internal performance is complex, and there are different issues that still must be improved and investigated further.

A very important aspect of the MMC is the so-called circulating current [7]. This inner current does not appear at the output, but is highly related to the system's stability, the efficiency of the converter and to the capacitor voltage ripples. The elimination of all the harmonic components in the circulating current increases the efficiency of the converter, but some studies indicate that the use of specific references can reduce the capacitor voltage ripples [8]. The MMC is composed of a high number of costly and bulky capacitors, and a reduction in the capacitor voltage ripples allows a reduction in the capacitances and in the cost of the converter. The use of circulating current references for reducing the capacitor voltage ripples is a worthy focus of research.

Multiple strategies can be used for controlling power converter switches. Due to the high number of MMC switches, the same output voltage can be obtained with multiple combinations. This degree of freedom in the modulation is usually used for balancing the capacitor voltages [9], but further targets can be considered. Moreover, adding a zero-sequence signal to the modulation or reference signals can also be studied with the objective of improving some of the previously mentioned aspects: effectiveness, capacitor voltage ripples and circulating current.

Industrial application aspects of the MMC are also an important point of study. Techniques for reducing the requirements of the MMC control system (such as simplifying the data acquisition system) and fault-tolerant techniques for allowing uninterrupted performance are topics that can be further studied.

This thesis attempts to contribute to all these topics.

1.3 Review of Previous Research

Although hough a similar topology was presented in 1981 [10], the current MMC topology was introduced in 2003 [3]. The MMC consists of two arms per phase-leg, where each arm comprises N series-connected submodules (SMs) and a series arm inductor L. Each SM consists of a capacitor C with a switching structure, which connects or disconnects the capacitor in-series within the arm. The main features of the MMC [5] are: its modularity and scalability to different power and voltage levels; its redundancy; and the high quality of the output voltages and currents. Those features make it one of the most attractive converters for high-power applications [2] like HVDC [4] and FACTS [11]. In recent years, the MMC has become a very important research topic

and multiple alternative topologies, modulation strategies and control techniques have appeared [6, 12].

The modelling of the MMC is a complex task, since it includes a high number of non-linear elements. In order to study the dynamic performance of the MMC, simplified models of the converter are required. For this reason, modelling of the MMC has been a common research topic [13, 14]. Multiple assumptions and calculations in this thesis are based on the averaged model presented in [15].

Like in most converter topologies [1], the modulation of the MMC [16] is a widely studied field. The MMC was originally presented with a space vector modulation (SVM) [3], which can be calculated on a plane or in a three-dimensional space [17, 18]. However, this technique becomes too complicated when the number of levels increases, and the most common modulation techniques are based on multicarrier pulse-width modulation (PWM) [19, 20]. The common multicarrier techniques use as many carriers as SMs (N), but some strategies based on interleaving [21] use $2N$ carriers for obtaining more output voltage levels. The multiple PWM carriers can be distributed along the modulation range (level-shifted) [9] or phase-shifted in a sampling period [22, 23]. The nearest level modulation (NLM) [24, 25] has also been considered for the MMC, but only in converters with a high number of levels. Selective harmonic elimination (SHE) is another technique considered in multiple articles [26–28], but the hard-processing requirements of this technique make it feasible only for converters with a low number of levels. Some papers have proposed new modulation techniques specifically designed for the MMC, such as a modified PWM [29] and another technique that switches at fundamental frequency [30].

Modulation techniques usually define the output voltage level, but not which SMs to activate. This degree of freedom can be used to balance the capacitor voltages in the arms. This task is performed by the voltage balancing algorithm. The most common voltage balancing algorithm is based on sampling the capacitor voltages, sorting them, and selecting those that balance the voltages [3, 9, 31]. Some papers present improved versions of the algorithm for reducing the switching frequency [24, 32]. Voltage balancing algorithms for modulation techniques that directly link the SMs to a particular carrier have also been developed [23, 33]. Those techniques modify the modulation signal or the carrier of each SM in order to balance the voltages.

Another widely studied topic is the dynamic analysis and control of the circulating current [34, 35]. This current flows through the arms of the converter without appearing at the output, and it is naturally composed of a dc component and low order harmonics [7, 36], mainly the second one. In order to ensure system stability and improve converter performance, the circulating current must be controlled. It can be controlled

through the voltage applied to the arm inductors, usually by adding a differential reference in the upper and lower arm modulation signals [7]. Since the voltage is applied over inductances, a proportional controller is commonly used [37]. More complex controllers can be used, such as: resonant controllers [38, 39], repetitive controllers [40, 41] or controllers operating with d-q variables [32, 42].

The circulating current reference can be defined according to multiple objectives. Some studies propose eliminating all the harmonic components, which reduces the arm rms current and therefore the power losses [32,38]. A fundamental frequency component can also be added to balance the energy stored in the upper and lower arms [7, 39]. Other studies propose injecting second and/or fourth harmonic components to reduce the capacitor voltage ripples [8, 43]. Reducing the capacitor voltage ripples is important for reducing the size of the capacitors [44] and, therefore, the overall cost of the converter.

The circulating current can also be combined with a zero-sequence voltage. Some studies propose using a fixed frequency zero-sequence and circulating current in order to translate the power oscillations to a higher frequency [45]. This technique is very useful for reducing capacitor voltage ripples at low frequencies, which is especially interesting in motor drive applications [46,47]. Zero-sequence signals have been used for motor drive applications and for extending the linear operating range, such as third harmonic injection or those based on SVM [48]. However, apart from those, the topic of zero-sequence signal has not been studied further in relation to the MMC. In this thesis, discontinuous zero-sequences, which have been widely studied in other converter topologies [49–52], are applied to the MMC for the first time.

In real applications of the MMC, such as in HVDC applications, the voltage specifications require the use of hundreds of SMs [4]. With the common voltage balancing algorithms, the voltage of each SM has to be measured in order to sort and select the SMs to be activated. Acquisition and conditioning of such a large number of signals is a challenge, and some techniques have appeared in recent years. Some studies try to solve this challenge with open-loop voltage balancing algorithms [19, 30, 53], but those methods can become unstable. Other studies develop simpler voltage balancing algorithms for a high number of SMs, but many voltage sensors are still required [33, 54, 55]. A possible solution for reducing the number of voltage sensors is to use observers and estimators [56, 57]. However, the reliability of the measuring system is reduced. A first approach to reducing the hardware complexity is presented in [58], where the acquisition system is highly simplified, but not the number of sensors.

A very important requirement of real applications is the reliability of the system, and a lot of research has recently been conducted on fault-tolerant solutions. Failures in the dc-link [59–61] and on the ac-side [62] have been highly studied. However, the most

common failures in power converters are due to faults in switching devices [63]. The MMC can easily provide redundancy of the SMs with the use of additional SMs [64–66], but the fault has to be detected and localized before disabling the faulty SM. Some techniques have emerged for detecting faults in the SM switching devices, and these are based on the use of additional sensors [67–69] or on the use of estimators and observers [70–72]. Another focus for improving converter reliability is to study the failure mechanisms of the switching devices [73, 74]. The failures are usually related to power losses, which, if not controlled, can be unevenly shared among the SMs in the arms [31].

1.4 Thesis Objectives

This thesis focuses on the study and development of new control and modulation techniques that improve some practical issues with the MMC. The developed techniques aim to fulfill three general purposes: (1) reducing the capacitor voltage ripples, (2) simplifying the MMC hardware and (3) improving its reliability. Furthermore, this thesis is devoted to studying and developing techniques for the application of the MMC to motor drives.

For these purposes, the following objectives are defined in this thesis:

- To define a circulating current reference that reduces the capacitor voltage ripples while also developing a method for calculating the optimal reference that minimizes the voltage ripples.
- To study the suitability of using discontinuous modulation in the MMC; evaluate its performance; and improve the technique with the goal of reducing power losses and capacitor voltage ripples.
- To develop a technique for measuring capacitor voltages while reducing the number of voltage sensors required by the MMC.
- To define a mechanism for detecting and localizing faults in both the SMs and the voltage sensors of the MMC while also developing a method for substituting the faulty sensors.
- To study the distribution of power losses in the switching devices when considering different capacitance values, and to also develop an algorithm for balancing these same power losses.

- To study the application of the MMC to motor drives and application of capacitor voltage ripple reduction techniques in order to allow MMC operation at low speeds/frequencies.

1.5 List of Publications

The following papers are as a result of the research developed in this thesis and have been published in different journals and conference proceedings.

1.5.1 Journal Papers

The following journal papers have been published or are already accepted for publication:

[1] J. Pou, S. Ceballos, G. Konstantinou, V. G. Agelidis, R. Picas, and J. Zaragoza, "Circulating current injection methods based on instantaneous information for the modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 777-788, Feb. 2015.

[2] R. Darus, J. Pou, G. Konstantinou, S. Ceballos, R. Picas, and V. G. Agelidis, "A modified voltage balancing algorithm for the modular multilevel converter: Evaluation for staircase and phase-disposition PWM," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4119-4127, Aug. 2015.

[3] R. Picas, S. Ceballos, J. Pou, J. Zaragoza, G. Konstantinou, and V. G. Agelidis, "Closed loop discontinuous modulation technique for capacitor voltage ripples and switching losses reduction in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4714-4725, Sep. 2015.

[4] R. Picas, J. Zaragoza, J. Pou, S. Ceballos, and J. Balcells, "New measuring technique for reducing the number of voltage sensors in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 177-187, Jan. 2016.

[5] G. Konstantinou, J. Pou, S. Ceballos, R. Picas, J. Zaragoza, and V. G. Agelidis, "Control of circulating currents in modular multilevel converters through redundant voltage levels," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7761 - 7769, Nov. 2016.

[6] R. Picas, J. Zaragoza, J. Pou, and S. Ceballos, "Reliable modular multilevel converter fault detection with redundant voltage sensor," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 39-51, Jan. 2017.

1.5.2 Conference Papers

The following papers have been presented in international conferences:

[7] R. Picas, J. Pou, S. Ceballos, V. G. Agelidis, and M. Saeedifard, "Minimization of the capacitor voltage fluctuations of a modular multilevel converter by circulating current control," in *Proc. IECON 2012 - 38th Annual Conference of the IEEE Industrial Electronics Society*, Montréal, Canada, 2012, pp. 4985–4991.

[8] R. Picas, J. Pou, S. Ceballos, J. Zaragoza, G. Konstantinou, and V. G. Agelidis, "Optimal injection of harmonics in circulating currents of modular multilevel converters for capacitor voltage ripple minimization," in *Proc. ECCE Asia Downunder (ECCE Asia), 2013 IEEE*, Melbourne, Australia, 2013, pp. 318–324.

[9] R. Picas, S. Ceballos, J. Pou, J. Zaragoza, G. Konstantinou, and V. G. Agelidis, "Improving capacitor voltage ripples and power losses of modular multilevel converters through discontinuous modulation," in *Proc. IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*, Vienna, Austria, 2013, pp. 6233–6238.

[10] R. Picas, S. Ceballos, J. Pou, J. Zaragoza, G. Konstantinou, V. G. Agelidis, and J. Balcells, "Discontinuous modulation of modular multilevel converters without the need for extra submodules," in *Proc. IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society*, Yokohama, Japan, 2015, pp. 2538–2543.

[11] G. Konstantinou, J. Pou, S. Ceballos, R. Picas, J. Zaragoza, and V. G. Agelidis, "Utilising redundant voltage levels for circulating current control in modular multilevel converters," in *Proc. IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society*, Yokohama, Japan, 2015, pp. 2213–2218.

[12] R. Picas, J. Pou, J. Zaragoza, A. Watson, G. Konstantinou, S. Ceballos, and J. Clare, "Submodule power losses balancing algorithms for the modular multilevel converter," in *Proc. IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, Florence, Italy, 2016.

1.5.3 Patents

[13] R. Picas, J. Zaragoza, and J. Pou, "Sistema y método de medida de las tensiones de las disposiciones capacitivas de los sub-módulos de un convertidor de potencia multinivel con almacenamiento distribuido de energía (MMC) y convertidor MMC," Patent ES P201430893, 11 June 2014.

TABLE 1.1: Relationship between chapters and publications.

Chapter	**Publication**
Chapter 2 The Modular Multilevel Converter	[2],[5],[7],[11]
Chapter 3 Circulating Current References for Capacitor Voltage Ripple Reduction	[1],[7],[8]
Chapter 4 Discontinuous Modulation	[3],[9],[10]
Chapter 5 Voltage Measurement System	[4],[13],[14]
Chapter 6 Fault Tolerant Topology	[6]
Chapter 7 Balancing Algorithms for Submodule Power Losses	[12]
Chapter 8 Application of the MMC in Low-Speed Motor Drives with Discontinuous Modulation	[15]

[14] R. Picas, J. Zaragoza, and J. Pou, "System and method for measuring the voltages of the capacitive arrangements of the sub-modules of a multilevel power converter with distributed energy storage (MMC) and an MMC converter," Patent WO/2015/189453, 10 June 2015.

1.5.4 Papers under Revision

The following paper has been submitted to a journal and it is currently under consideration for publication:

[15] R. Picas, J. Zaragoza, J. Pou, S. Ceballos, G. Konstantinou, and V.G. Agelidis, "Study and comparison of discontinuous modulation for modular multilevel converters in motor drive applications," submitted to *IEEE Trans. Ind. Electron.*

The selected journal and conference papers are associated with the chapters of the thesis that are shown in Table 1.1.

1.6 Thesis Outline and Main Contributions

This thesis is composed of nine chapters. The following summary indicates the main contents of each one.

- Chapter 2 presents the MMC with details of its operating principles, a mathematical model and an explanation of the main control strategies. Within these strategies, a scalable algorithm for the level-shifted PWM (LS-PWM) is implemented; a new implementation of the voltage balancing algorithm is detailed; and a novel method for controlling the circulating current is presented. It also reviews the main applications of the MMC and presents the MMC prototypes used in this thesis.

- Chapter 3 presents three methods for calculating the circulating current reference. All these methods have the objective of reducing the capacitor voltage ripples. The first one defines an approximated continuous function of the capacitor voltage ripples and obtains an optimal function for the second harmonic of the circulating current. The second method applies an iterative optimization method by evaluating all the combinations of the second and fourth harmonics and selecting the optimal ones. The third technique calculates the theoretical optimal reference from a simplified model of the converter and obtains a nearly optimal reference that can be calculated on-line.

- Chapter 4 presents the discontinuous modulation for application in the MMC. This technique reduces the switching power losses and the capacitor voltage ripples, especially for low modulation indices. Three approaches to discontinuous modulation are presented. The first approach consists of an open-loop technique that uses a pre-defined modulation signal. The second approach uses a closed-loop algorithm for defining the zero-sequence signal, thus further reducing power losses and capacitor voltage ripples. Finally, the third approach is adapted to medium-power applications by reducing the number of required SMs.

- Chapter 5 presents a new voltage measuring system, where only two sensors per arm are required. The sensors measure the voltage provided by a set of SMs and acquire the capacitor voltages when only a single SM in the set is activated. Between actual measurements, the system performs an estimation of the capacitor voltages.

- Chapter 6 presents a fault detection and localization system for the MMC. The topology is based on three additional sensors per arm, which compare the expected voltage with the measured one. The system is able to detect open-circuit and short-circuit faults in the switching devices and faults in the voltage sensors. The use of additional sensors allows substituting the faulty sensors with the measuring algorithm presented in Chapter 5.

- Chapter 7 studies the distribution of power losses in an MMC when the SM capacitances are not equal. The inequalities in the capacitances can be caused by

the manufacturing tolerance or by a degradation of the capacitors. A system for balancing the losses between the SMs is also presented.

- Chapter 8 deals with the application of the MMC to a variable-speed motor drive. This application presents problems at low speeds/frequencies, where the capacitor voltage ripples can become excessive. Discontinuous modulation is applied in order to reduce the capacitor voltage ripples, presenting a good performance of the motor at 1% of the nominal speed. The technique is compared with other state-of-the-art low-speed operation techniques, and discontinuous modulation is found to be the one that presents the lowest power losses with similar capacitor voltage ripples.

- Finally, Chapter 9 summarizes the main contributions of the thesis and includes some discussion of possible future research.

Chapter 2

The Modular Multilevel Converter

This chapter introduces the MMC, detailing its structure and principles of operation. It continues developing the mathematical model of the converter and detailing the simplified models used in this thesis. The most common modulation algorithms and control techniques are also presented, focusing on capacitor voltage balancing and circulating current control algorithms. The most common applications of this topology are also presented. Finally, the low-power MMC prototypes used and developed during this thesis are presented.

2.1 Introduction

A voltage source converter (VSC) is an electrical system used to convert power from a dc voltage source to single or multiphase ac voltages, usually generating sinusoidal currents suitable for the grid or for driving ac motors. VSCs are commonly implemented for single-phase or three-phase systems, and their power flow can be bidirectional. That is, they can provide energy from the dc-side to the ac-side, working as inverters, or from the ac-side to the dc-side, working as rectifiers. VSCs are implemented with fully-controllable power switches, like isolated-gate bipolar transistors (IGBTs) or metal-oxide-semiconductor field-effect transistors (MOSFETs). These power devices provide the characteristic that define the VSC, the ability to work as a voltage sources.

Multilevel converters [1, 2] are VSC topologies that provide more than two voltage levels at the ac-side. The main advantages of multilevel converters are the high quality of the output voltages and reduced voltage stress in the power devices. The high

quality of the output voltages enables the use of smaller reactive components for output filters, while reduced voltage applied to the power switches allows the converters to handle higher voltages. For this reason, multilevel converters have attracted significant interests for medium- and high-voltage/power applications in the last decades. The most common multilevel converter topologies are the neutral-point clamped (NPC) converter [75], the flying capacitor (FC) converter [76], the cascaded H-bridge converter [77] and the MMC [3].

In the recent years, the MMC has become one of the most attractive topologies for high-voltage and high-power applications. The main characteristics of this converter [5,6] are:

- Modularity and scalability to different power and voltage levels.
- Redundancy and reliability.
- Compatibility with commercial semiconductors.
- High efficiency.
- High quality of the output voltages.
- Absence of additional capacitors on the dc-link.

In this thesis, the most common MMC topology is studied, converting from dc to ac, or inversely. This topology can be used alone, supplied by a dc source, with two MMCs in back-to-back or transmission line configuration [9], which consists in connecting two dc-ac converters by the dc-side, or in multiterminal configuration [78], where more than two MMCs are connected to a common dc-link. However, in the recent years, other configurations of the MMC have appeared, like the direct ac-ac converter [79, 80], the MMC-based dc-dc converter [81, 82] or some hybrid MMC topologies [83, 84].

2.1.1 MMC Topology and Principles of Operation

The MMC (also called M2C or MMLC) was first presented in 2003 [3], and it has been intensively investigated in the last few years. In fact, the basic circuit using voltage sources instead of capacitors, was already proposed in 1981 [10]. A diagram of a three-phase MMC is depicted on Fig. 2.1. The topology consists of two arms per phase-leg where each arm comprises N series-connected, identical, submodules (SMs) and a series arm inductor L.

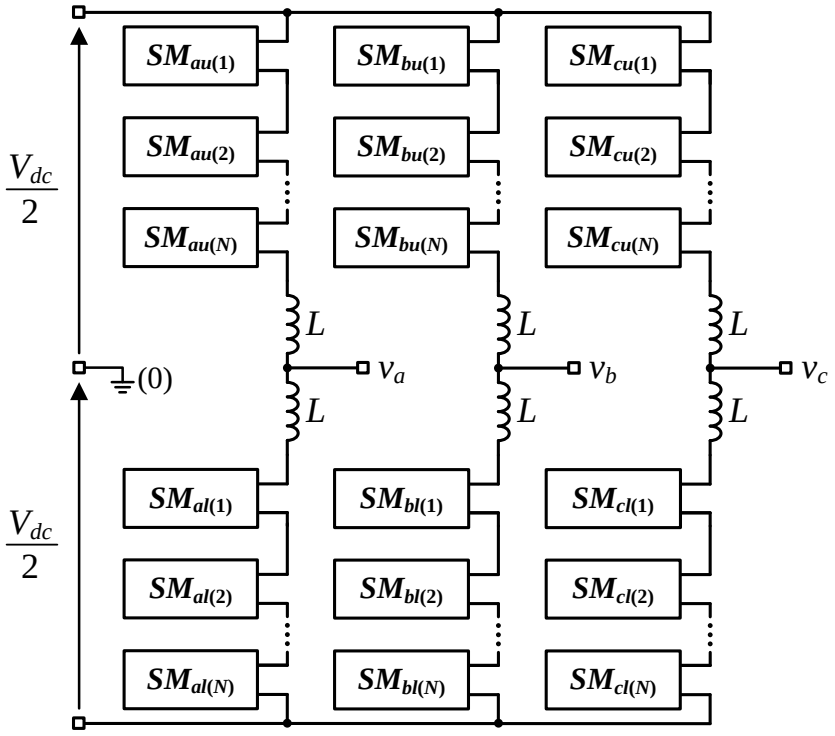


FIGURE 2.1: Circuit diagram of a three-phase MMC.

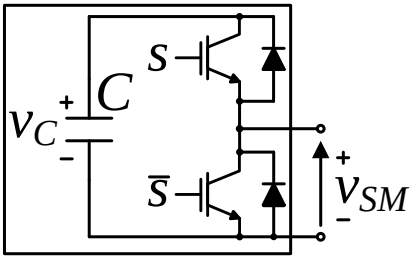


FIGURE 2.2: Circuit diagram of a half-bridge SM.

Each SM consists of a capacitor bank C with a switching structure, which connects or disconnects the capacitor in-series within the arm. Multiple SM configurations can be used, but the most common one, which is studied in this thesis, is the half-bridge structure, depicted in Fig. 2.2. If the SM is activated (s=1), the output voltage of the SM v_{SM} is equal to the capacitor voltage v_C. Otherwise, if the SM is deactivated (s=0), the output of the SM is zero. The SMs can also be implemented using full bridges (H-bridges), which can supply three voltage levels ($+v_C$, 0 or $-v_C$), and other multilevel structures [85].

The SMs of the MMC act as multiple voltage sources connected in series, providing voltage when they are activated and acting as short-circuits when they are deactivated. With the activation and deactivation of the SMs, the arms of the MMC provide multilevel waveforms. When synthesizing a voltage waveform v_j at the output, where $j \in \{a, b, c\}$

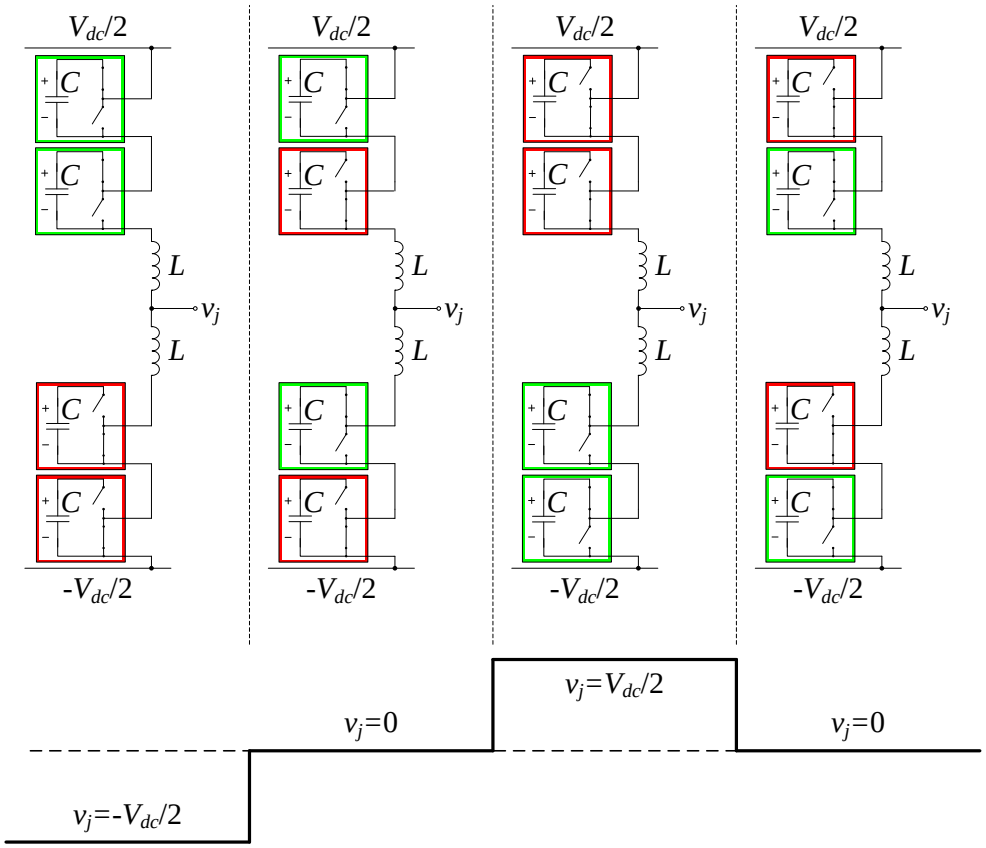


FIGURE 2.3: Synthesis of a multilevel waveform in an MMC with two SMs per arm (N=2). Activated and deactivated SMs are highlighted in green and red colour, respectively.

is the phase identifier, the voltage provided by the SMs in the upper arm is subtracted to the voltage of the positive terminal of the dc-link, i.e. the output voltage is maximum when all the SMs in the upper arm are deactivated and minimum when all the SMs are activated. On the contrary, the voltage provided by the SMs of the lower arm is added to the voltage of the negative terminal of the dc-link.

Since the voltage provided from the upper arm has to match the voltage provided from the lower arm, its control has to be complementary, i.e. the lower arm has as many SMs activated as the upper arm has deactivated. This implies that there are always N SMs activated on a phase-leg, and therefore, the average value of the capacitor voltages is V_{dc}/N. An example of multilevel waveform synthesis is depicted in Fig. 2.3.

The arm inductors L allow small mismatches in the voltage provided by the upper and lower arms. The voltage mismatches can be caused by the variation in the SM capacitor voltages, or can be forced by the control. This voltage difference creates a differential current, also called circulating current, that flows within the arms without appearing at the output. The effects of the circulating current have been extensively studied in the literature and represent an important part of this thesis.

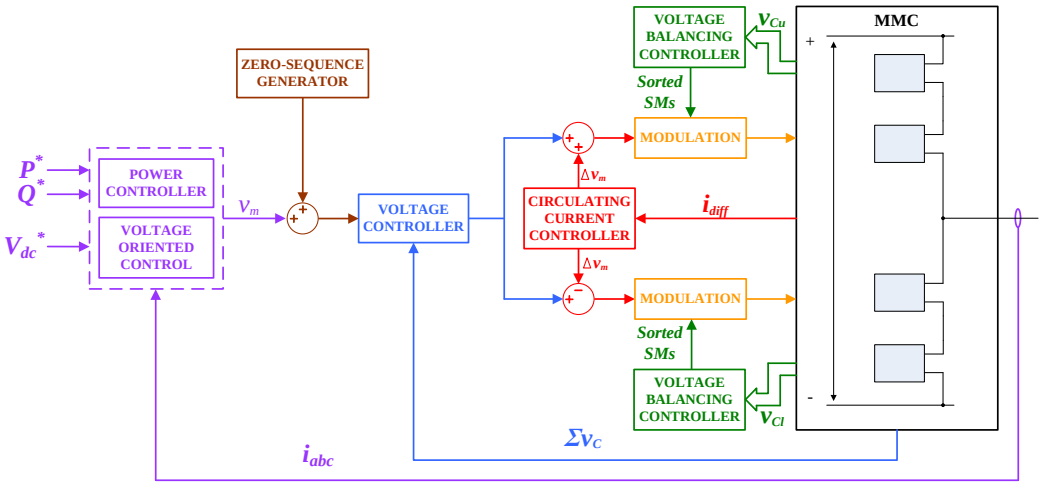


FIGURE 2.4: Block diagram of multiple control loops implemented in an MMC.

2.1.2 Control Strategy of the MMC

The MMC is a complex system with multiple variables to control. For this reason, the control system of an MMC is usually composed by multiple chained loops or control algorithms. A block diagram of the multiple control loops implemented in an MMC converter is depicted in Fig. 2.4.

The most inner control loop is the modulator, which activates the SMs and synthesizes the ac waveform [1,16]. Each arm of the converter is considered as an independent voltage source, therefore, a modulator is used for each arm. In the synthesis of an ac waveform with an MMC, most of the voltage levels can be obtained with multiple combinations of activated SMs. This degree of freedom in the control is normally used to balance the SM capacitor voltages, that is, getting the capacitor voltages of the different SMs in the same arm as close as possible. This task is achieved by the voltage balancing controller [3,9], which performance is linked to the modulator. In most cases, the modulator selects the voltage level to apply to the output and the voltage balancing control selects the particular SMs to be activated.

Although it is not essential, most converters use a circulating current controller [7, 32], which can substantially improve the performance of the converter. This controller regulates the circulating current by applying a voltage difference in the arms inductors. The reference for the circulating current can be defined in multiple ways: an off-line calculated waveform, as a function of the instantaneous value of the current or with the use of an energy balancing loop.

An output voltage loop can also be included for the control of the MMC [86]. Since the capacitor voltages are not constant, capacitor voltage variations can cause distortion at the output voltage. The output voltage loop, modifies the modulation signal considering the capacitor voltage ripples. This control is sometimes implemented in a feed-forward topology without measuring the output voltage.

Finally, an output current control loop is used [9]. This loop control defines the basic modulation reference in order to control the output current. The reference of the current is usually calculated as a function of the active and reactive power supplied, or obtained from an even outer loop, which controls the dc-link voltage or the speed and torque of a motor in motor drive applications.

Apart from the control loops, the modulation signal can be modified by the addition of a zero-sequence component [48]. In equilibrated three-phase systems, the zero-sequence component can modify the performance of the controller without affecting to the line-to-line voltages, and therefore, without affecting the output currents.

2.2 Mathematical Models of the MMC

Considering the semiconductors of the MMC as ideal switches, a switched model of the MMC can be obtained. As explained in the previous section, the series-connected SMs can be understood as multilevel voltage sources. An equivalent model of a phase-leg of the MMC is depicted on Fig. 2.5. In this model and the posterior equations, the subindex $j \in \{a, b, c\}$ is the phase identifier and the subindex u and l are used to identify the upper and lower arms, respectively.

The value of the upper and lower arm voltage sources, v_{SMju} and v_{SMjl}, respectively, can be calculated as the sum of the voltages of all the activated SMs:

$$v_{SMju} = \sum_{n=1}^{N} s_{ju(n)} \cdot v_{Cju(n)} \text{ and} \tag{2.1}$$

$$v_{SMjl} = \sum_{n=1}^{N} s_{jl(n)} \cdot v_{Cjl(n)} \ , \tag{2.2}$$

where $n \in \{1, ..., N\}$ identifies the number of SM, $s_{ju(n)}$ and $s_{jl(n)}$ are the switching operators, and $v_{Cju(n)}$ and $v_{Cjl(n)}$ the capacitor voltages of each SM.

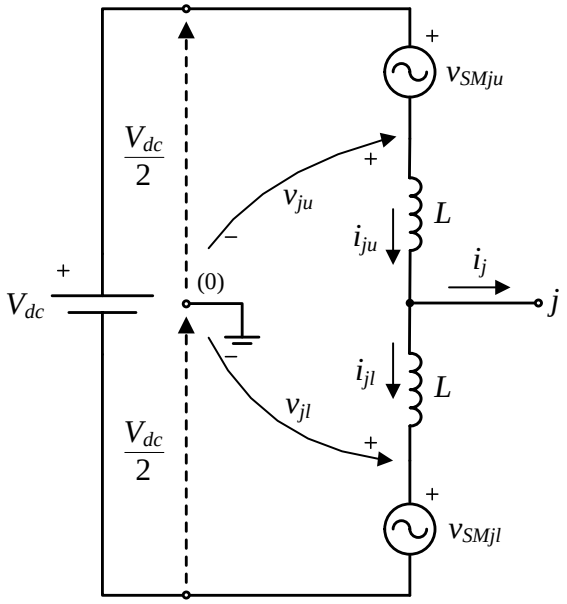


FIGURE 2.5: Equivalent circuit of an MMC phase-leg considering the arms as voltage sources.

Considering the fictitious dc-bus mid-point as the reference or "0", the voltages provided by the upper and lower arms, v_{ju} and v_{jl}, respectively, are defined as:

$$v_{ju} = \frac{V_{dc}}{2} - v_{SMju} \text{ and} \tag{2.3}$$

$$v_{ju} = -\frac{V_{dc}}{2} + v_{SMjl} \ . \tag{2.4}$$

As explained in [87], the voltage applied to the extremes of the inductors can be divided into the common and differential voltages:

$$v_{jcomm} = \frac{v_{ju} + v_{jl}}{2} \text{ and} \tag{2.5}$$

$$v_{jdiff} = \frac{v_{ju} - v_{jl}}{2} \ . \tag{2.6}$$

Applying the principle of superposition, common and differential mode circuits can be obtained. Fig. 2.6(a) and (b), show the equivalent common and differential circuits when considering an output impedance Z_{out}, respectively.

Considering an output current i_j and the same value in the inductors L, the common current can be defined as a half of the output current:

$$i_{jcomm} = \frac{i_j}{2} \ , \tag{2.7}$$

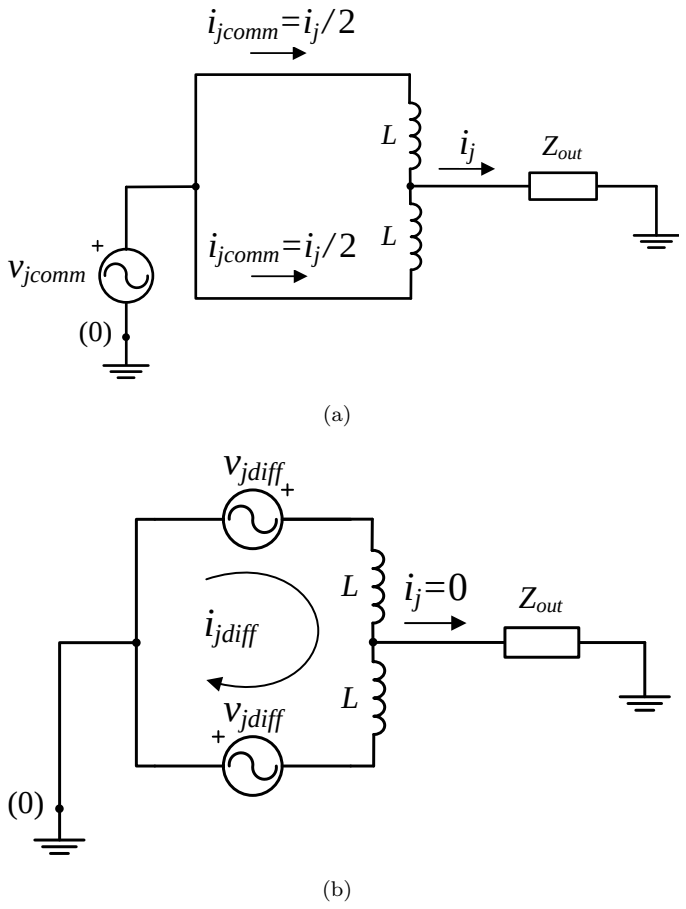


FIGURE 2.6: Equivalent circuit of an MMC phase-leg : (a) common and (b) differential circuits.

while the differential current can be defined as:

$$i_{jdiff} = \frac{1}{L}\int_0^t v_{jdiff}dt + I_{jdiff0}\ , \tag{2.8}$$

where I_{jdiff0} is the initial value of the differential voltage. The differential current is also called circulating current, since it flows through the legs of the converter without appearing at the output. (2.8) demonstrates that the circulating current can be controlled trough the differential voltage.

From (2.7) and (2.8), the arm currents can be defined as:

$$i_{ju} = \frac{i_j}{2} + i_{jdiff} \text{ and} \tag{2.9}$$

$$i_{jl} = -\frac{i_j}{2} + i_{jdiff}\ . \tag{2.10}$$

From Fig. 2.6(b) it can be deduced that the differential circuit does not affect the output voltage. Therefore, it can be defined as:

$$v_j = v_{jcomm} - \frac{L}{2}\frac{d}{dt}i_j \ . \tag{2.11}$$

Finally, once the arm current is defined, the voltage of each SM capacitor can be calculated. Considering ideal switches and capacitors, the capacitor voltage of a particular SM only varies when the SM is activated and hence the arm current flows through it:

$$v_{Cju(n)} = \frac{1}{C}\int_0^t s_{ju(n)} \cdot i_{ju} dt + V_{Cju(n)0} \text{ and} \tag{2.12}$$

$$v_{Cjl(n)} = \frac{1}{C}\int_0^t s_{jl(n)} \cdot i_{jl} dt + V_{Cjl(n)0} \ , \tag{2.13}$$

where $V_{Cju(n)0}$ and $V_{Cjl(n)0}$ are the initial capacitor voltages.

2.2.1 Simplified Model with Equivalent Capacitors

In order to study the dynamic performance of the MMC, simplified models of the converter are required. This has been an important focus of research and several papers have been published about MMC modelling [13, 14]. Some of the studies developed in this thesis are based on the equivalent dynamic model introduced in [15] and extended in [87]. This simplified model is based on considering the series-connected SMs as an equivalent capacitor, which capacitance depends on the number of connected SMs. A circuit diagram of the equivalent model is depicted on Fig. 2.7.

The equivalent capacitances C_{ju} and C_{jl} are defined as the nominal capacitance of the SMs C divided by the number of activated SMs in the upper (u_j) or lower arm (l_j):

$$C_{ju} = \frac{C}{u_j} \text{ and} \tag{2.14}$$

$$C_{jl} = \frac{C}{l_j} \ . \tag{2.15}$$

Assuming that no differential voltage is imposed for the control of the circulating current and infinite switching frequency, the number of activated SMs in the upper and lower arms are defined as a linear function of the modulation signal v_{jm}, which is the normalized ac reference signal that ranges in the interval $[-1, 1]$:

$$u_j = N\frac{1 - v_{jm}}{2} \text{ and} \tag{2.16}$$

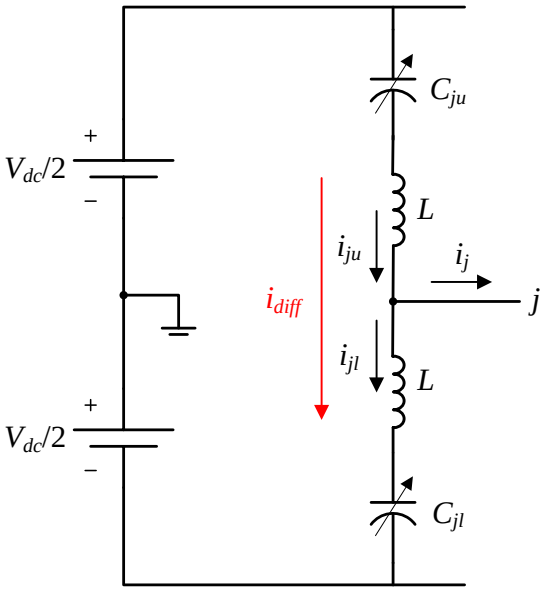


FIGURE 2.7: Equivalent model of an MMC phase-leg.

$$l_j = N\frac{1+v_{jm}}{2} \ . \tag{2.17}$$

Considering no arm inductors ($L=0$), the output phase current i_j is shared between the upper and lower arms based on the capacitance value:

$$i_{ju} = i_j\frac{C_{ju}}{C_{ju}+C_{jl}} = i_j\frac{l_j}{u_j+l_j} \text{ and} \tag{2.18}$$

$$i_{jl} = -i_j\frac{C_{jl}}{C_{ju}+C_{jl}} = -i_j\frac{u_j}{u_j+l_j} \ . \tag{2.19}$$

Substituting (2.16) and (2.17) into (2.18) and (2.19), the arm currents become

$$i_{ju} = i_j\frac{1+v_{jm}}{2} \text{ and} \tag{2.20}$$

$$i_{jl} = -i_j\frac{1-v_{jm}}{2} \ . \tag{2.21}$$

According to (2.9) and (2.10), the differential current can be defined as:

$$i_{jdiff} = \frac{i_{ju}+i_{jl}}{2} \ , \tag{2.22}$$

which in the equivalent model becomes:

$$i_{jdiff} = \frac{i_j v_{jm}}{2} \ . \tag{2.23}$$

2.2.2 Averaged model of the converter

An averaged model of the MMC was also developed in [15]. That model has been used in some chapters of the thesis for predicting the SMs capacitor voltage ripples.

From the switched equations of the capacitor voltages (2.12) and (2.13), the locally averaged model over the switching period can be obtained:

$$\overline{v_{Cju(n)}} = \frac{1}{C}\int_0^t d_{ju(n)} \cdot \overline{i_{ju}} dt + V_{Cju(n)0} \text{ and} \tag{2.24}$$

$$\overline{v_{Cjl(n)}} = \frac{1}{C}\int_0^t d_{jl(n)} \cdot \overline{i_{jl}} dt + V_{Cjl(n)0} \ , \tag{2.25}$$

where $\overline{v_{Cju(n)}}$, $\overline{v_{Cjl(n)}}$, $\overline{i_{ju}}$ and $\overline{i_{jl}}$ are the locally averaged voltages and currents, and $d_{ju(n)}$ and $d_{jl(n)}$ are the duty cycles of the individual SMs.

Operating with high switching frequency and using a proper voltage balancing technique, the same duty cycle for all the SMs in an arm can be assumed ($d_{ju} \approx d_{ju(n)}$ and $d_{jl} \approx d_{jl(n)}$). Similarly to how the number of activated SMs in the arms are defined in (2.16) and (2.17), the duty cycles are defined as the modulation signal v_{jm} displaced and scaled to the range $[0, 1]$. The duty cycles of the upper and lower arms are obtained as follows:

$$d_{ju(n)} = \frac{1 - v_{jm}}{2} \text{ and} \tag{2.26}$$

$$d_{jl(n)} \frac{1 + v_{jm}}{2} \ . \tag{2.27}$$

Substituting (2.26) and (2.27) into (2.24) and (2.25), the locally-averaged SM capacitor voltages become:

$$\overline{v_{Cju(n)}} = \frac{1}{C}\int_0^t \overline{i_{ju}} \frac{1 - v_{jm}}{2} dt + V_{Cju(n)0} \text{ and} \tag{2.28}$$

$$\overline{v_{Cjl(n)}} = \frac{1}{C}\int_0^t \overline{i_{jl}} \frac{1 + v_{jm}}{2} dt + V_{Cjl(n)0} \ . \tag{2.29}$$

2.3 Modulation Strategies

Several modulation strategies for multilevel converters have been proposed in the last decades. In [1], an overview and classification of the most common techniques is presented, and in [16] a review of the application of these techniques in an MMC is done. A classification of the most common modulation techniques for multilevel converters is shown in Fig. 2.8.

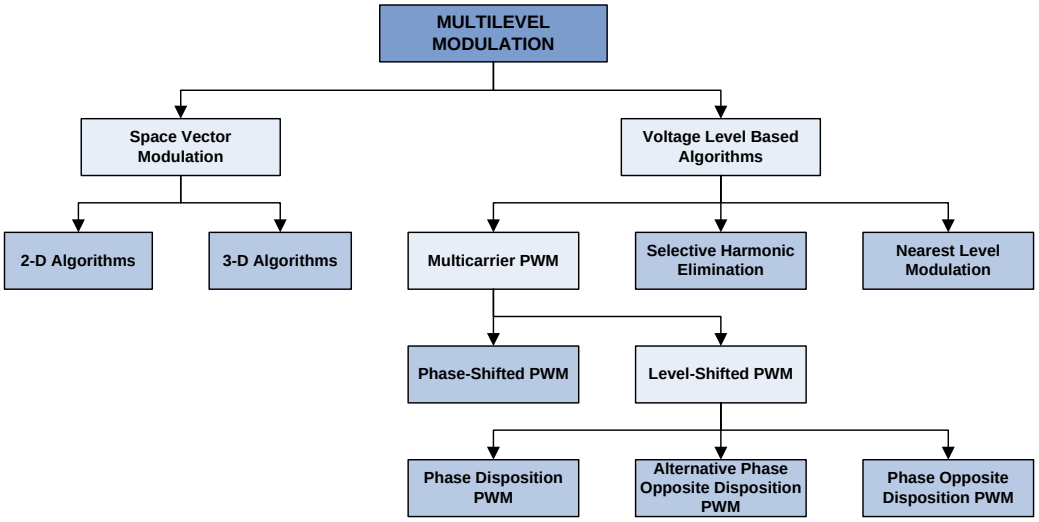


FIGURE 2.8: Modulation techniques for multilevel converters.

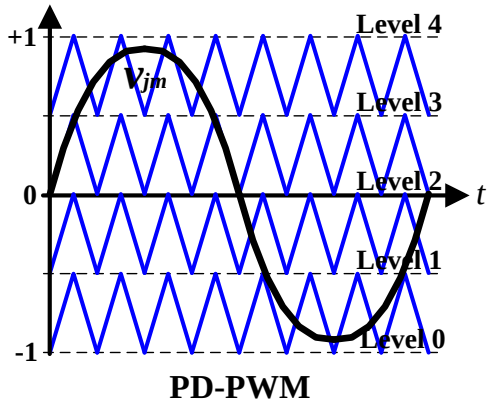
2.3.1 Level-Shifted PWM

Multicarrier PWM techniques are the most extended ones for controlling multilevel converters with high number of levels. They are based on comparing several high-frequency carriers, normally with triangular shape, with the modulation or reference signal. Usually $n-1$ carriers are compared with the reference signal, n being the number of output levels of the converter.

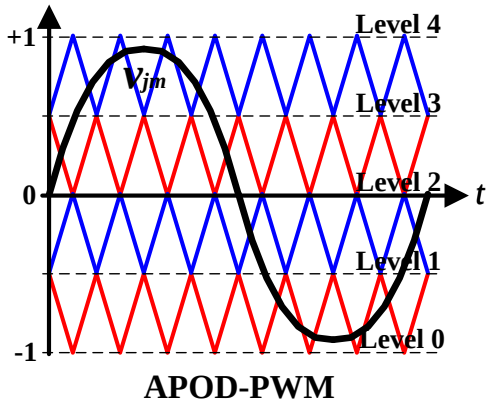
The LS-PWM techniques consist in distributing N carriers vertically along the modulation amplitude range $[-1, 1]$. Each carrier defines a transition between two consecutive output levels or can be directly associated to a specific SM. The modulating signal is compared with the N carriers, activating as many SMs as carriers are under the modulation signal.

Linking each carrier to a specific SM disables the ability of the MMC from providing the same voltage level with multiple SM combinations, and therefore impossibles the voltage balancing task. For this reason, the LS-PWM is usually used for defining the number of activated SMs and the particular SM to be activated is defined by the voltage balancing algorithm [9].

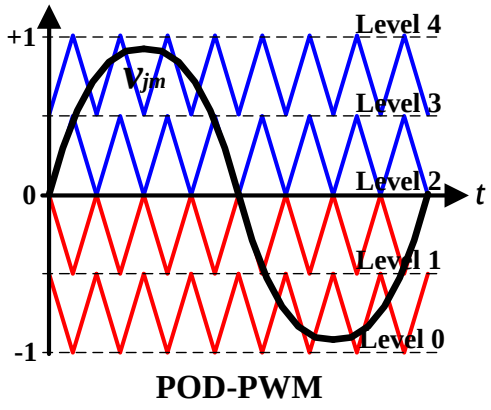
There are several LS-PWM techniques depending on the phase disposition of the carriers [19]. In phase-disposition PWM (PD-PWM), all the carriers have the same phase displacement. Alternative phase-opposition disposition (APOD-PWM) is based on shifting each carrier 180° from its adjacent carrier. In some converters, this technique can be used for reducing the third order harmonic component from the output voltage [20]. Finally, the phase-opposition disposition (POD-PWM) uses carriers in



(a)



(b)



(c)

FIGURE 2.9: Representation of carrier dispositions of LS-PWM for a five-level converter: (a) PD-PWM, (b) APOD-PWM and (c) POD-PWM.

the negative range of the modulation signal that are 180° shifted from the carriers in the positive range of the modulation signal. Fig. 2.9 represents examples of the three LS-PWM carrier dispositions.

All the studies developed in this thesis are based on the PD-PWM technique to define

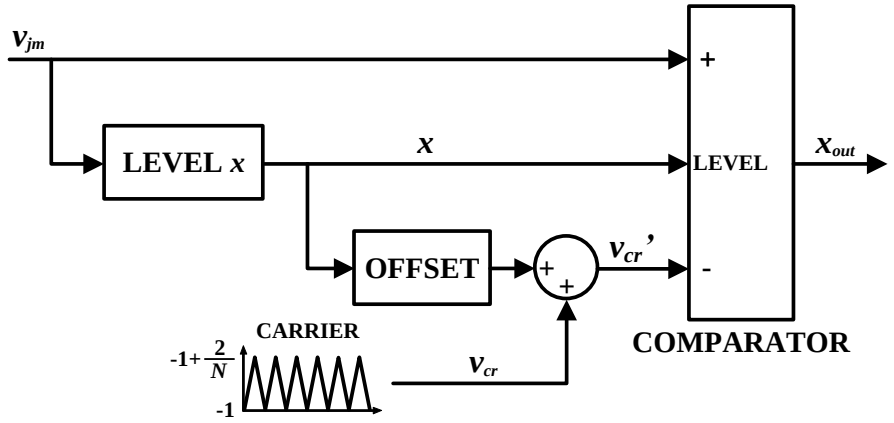


FIGURE 2.10: Block diagram of the scalable PD-PWM algorithm.

the number of activated SMs, but not the particular SM. Since the implementation of N triangular carriers requires a high number of processing resources, an scalable modulation strategy has been developed during this thesis [88]. The scalable strategy is based on using only one carrier and displacing it vertically when required. A block diagram of this scalable PD-PWM is shown at Fig. 2.10.

A triangular carrier signal v_{cr} with a constant amplitude A_{cr} is calculated in the processor. The carrier is implemented in the range $[-1, -1 + A_{cr}]$, and the amplitude is defined as:

$$A_{cr} = \frac{2}{N} \,. \tag{2.30}$$

To emulate the N different carriers, an offset is added to the carrier v_{cr}. Since each carrier ranges between two output levels, the lower level x has to be calculated. The lower level is defined as the integer part of the number of activated SMs in (2.17):

$$x = \left\lfloor N \frac{1 - v_{jm}}{2} \right\rfloor \,. \tag{2.31}$$

Then, the offset and the resulting level shifted carrier can be defined as:

$$v'_{cr} = v_{cr} + x\frac{2}{N} \,. \tag{2.32}$$

As if multiple carriers were used, the displaced carrier is compared with the modulation signal and the upper or lower level is selected to be applied at the output:

$$x_{out} = \begin{cases} x & \text{if } v_{jm} < v'_{cr} \\ x+1 & \text{if } v_{jm} \geq v'_{cr} \end{cases} \text{ and} \tag{2.33}$$

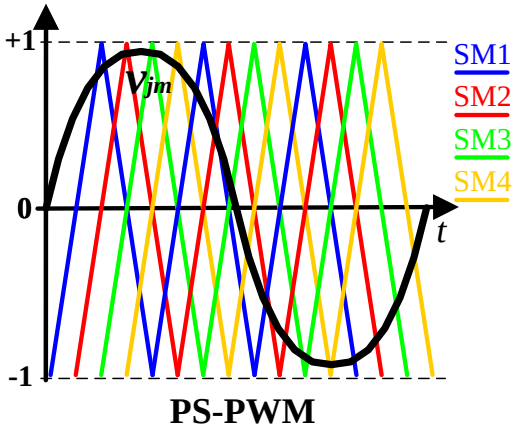


FIGURE 2.11: Block diagram of the scalable PD-PWM algorithm.

2.3.2 Phase-Shifted PWM

Phase-shifted PWM (PS-PWM) is another highly extended multicarrier modulation technique, because it eliminates all low order harmonic components of the output voltage [22] and is easy to implement. An example of PS-PWM for a five-level converter is depicted in Fig. 2.11.

In this technique, the peak-to-peak amplitudes of the carriers range the interval $[-1, 1]$, but they are phase shifted along the carrier period. The phase displacement between carriers is:

$$\Delta\varphi = \frac{2\pi}{N} \ . \tag{2.34}$$

Similar to LS-PWM each carrier can be linked to a particular SM [23] or the number of carriers under the modulation signal are used to define the output level. In PS-PWM, the equivalent switching frequency is multiplied by the number of carriers (N), as in one carrier period the modulating signal crosses N carriers. That is, the effective output switching frequency f_{sw} is N times the carrier frequency f_{cr}:

$$f_{sw} = N \cdot f_{cr} \ . \tag{2.35}$$

2.3.3 Arms Interleaving

The technique known as interleaving between the arms is a common modification of multicarrier PWM techniques for increasing the number of output levels in an MMC [89]. When the upper and lower arms are activated synchronously, $N + 1$ voltage levels can be provided to the output. However, if the switching transitions of the upper and lower arms are not synchronized, new intermediate voltage levels appear at the output. That

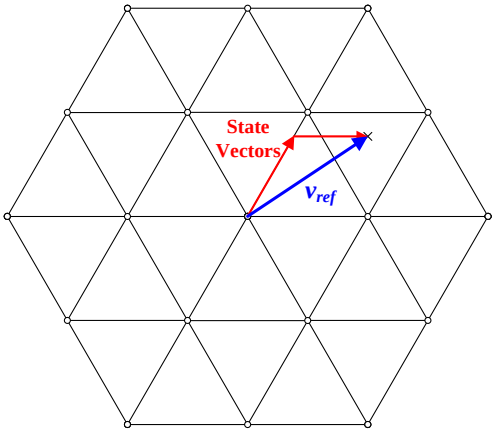


FIGURE 2.12: Space vector diagram of a three-level converter.

is, if the upper arm is providing the level x and the lower arm is providing the level $x+1$, the resulting common voltage is the level $x+\frac{1}{2}$.

A simple way to produce interleaving when using LS-PWM consists in shifting the carriers of the lower arm 180° respect to the carriers used for the upper arm [90]. With this method, the number of output levels per phase is increased to $2N+1$ and the equivalent output switching frequency is doubled.

2.3.4 Space Vector Modulation

SVM is based on the representation in the alpha-beta plane of the voltage reference and the voltages provided by the converter. Each of the switching combinations of the converter leads to an output voltage level for each phase of the converter, which can also be represented as a voltage vector or state vector. The output voltage reference, represented as a rotating vector, can be implemented by the lineal combination of multiple state vectors at each sampling period. The multiplier of each state vector in the lineal combination is the amount of time that the state has to be active in order to synthesize the voltage reference. An example of space vector diagram for a three-level converter is depicted in Fig. 2.12.

SVM is usually calculated in a plane [3], but it can also be represented in a three-dimensional space (3D-SVM) [17], where apart from the alpha and beta axes, the gamma axis is added in order to control the zero-sequence.

SVM provides very good control of the converter, but it is not practical for controlling converters with high number of levels, as the number of space vectors grows proportionally to the cubic of the number of voltage levels [18].

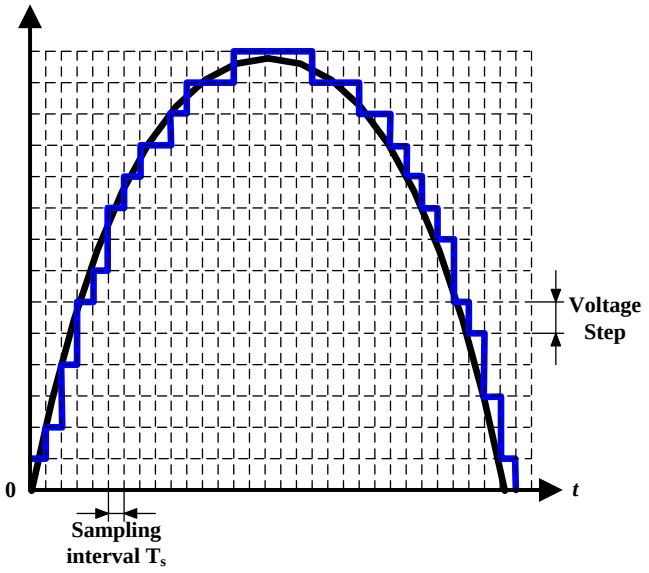


FIGURE 2.13: Example of the waveform provided by the NLM technique.

2.3.5 Nearest Level Modulation

NLM method consists on generating the voltage level closest to the voltage reference for a full switching period. This technique is based on approximation and not on modulation of the reference. For this reason, this technique is used in converters with high number of voltage levels, like in HVDC applications [24], where a good approximation to the reference voltage can be done. The main advantages of this technique are simplicity of application, strong reduction of the switching frequency and, consequently, reduction of the switching power losses. However, the reduction of switching frequency is also its main drawback, as due to its low and variable switching frequency, high harmonic distortion appears, especially in converters with a low number of levels. A study of the effects of NLM sampling frequency in the capacitor voltage ripples of the MMC was performed in [25]. An example of the voltage provided with NLM is depicted in Fig. 2.13.

2.3.6 Selective Harmonic Elimination

SHE is considered, like NLM, a low switching frequency modulation technique. It offers high control of some harmonics of the output voltage while minimizing number of switching transitions. It is based on the Fourier decomposition of the output voltage waveform, where the switching angles are calculated in order to cancel some specific harmonics, generally low frequency harmonics [26–28]. The technique calculates the switching angles for one quarter of a period and they are applied symmetrically for the

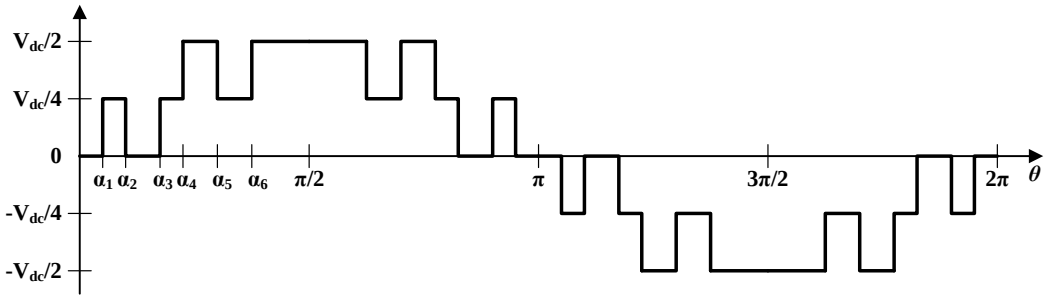


FIGURE 2.14: Example of the output voltage provided by a five-level converter controlled with SHE.

rest of the period. An example of output voltage calculated with SHE is depicted in Fig. 2.14.

One of the main drawbacks of SHE algorithms is that they are limited to operate in open-loop control, since the switching angles are calculated off-line, stored in tables and interpolated according to the operating conditions. In addition, SHE algorithms become complex to implement when the number of levels is high [1].

Multiple versions of SHE algorithms have been published. In [30], a modulation technique for the MMC that switch at fundamental output frequency is developed. The algorithm defines the angles where pulses of π width have to be centred in order to eliminate low order harmonics and balance the capacitor voltages. Only one angle per period is defined, repeating the same sequence every N periods (as many periods as the number of SMs), the amount of periods required for balancing the capacitor voltages.

2.4 Voltage Balancing Algorithm

A very important factor in the performance of the MMC is the capacitor voltage balancing within its arms. If the capacitor voltages are not properly balanced, the voltage steps are not regular and the output voltage has some additional distortion. The voltage balancing controller is the most internal control loop and is usually integrated with the modulation algorithm.

As explained before, most modulation strategies define the number of SMs to activate, but not the particular ones to be activated. This degree of freedom can be used to balance the SM capacitor voltages within each arm. The most common voltage balancing algorithm [3, 9, 31], measures all the capacitor voltages at each period and sorts them. If the arm current is positive, the SMs with the lowest capacitor voltages are activated, so that the SM capacitors will be charged, increasing their voltages. On the

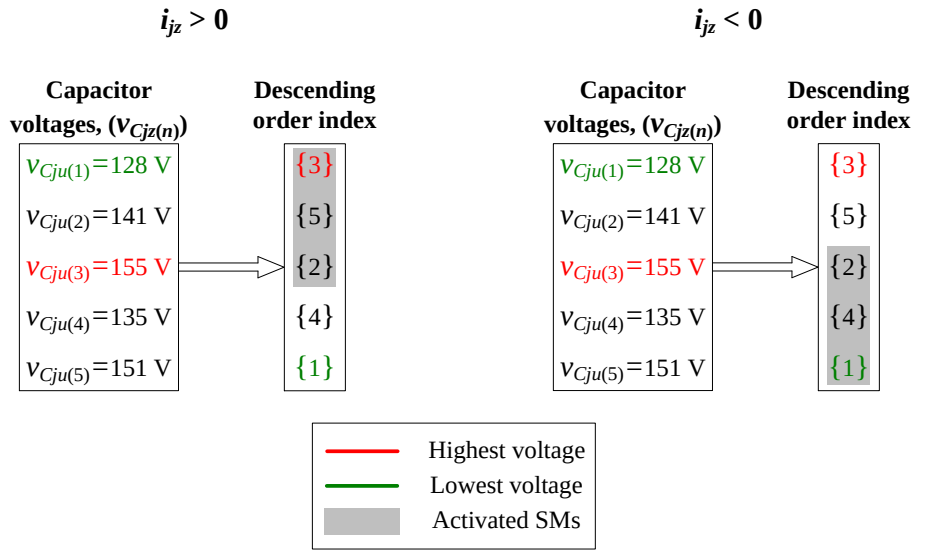


FIGURE 2.15: Example of voltage balancing in an MMC with five SMs per arm ($N = 5$).

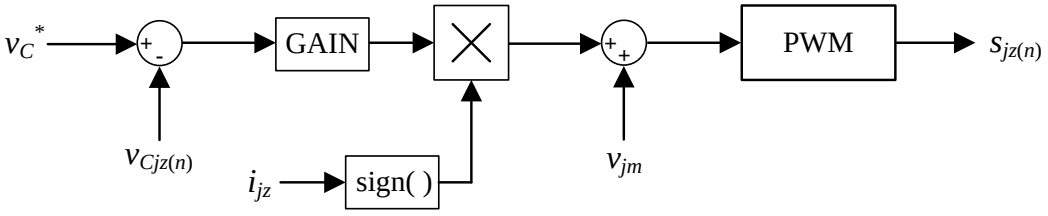


FIGURE 2.16: Block diagram of the voltage balancing algorithm without sorting.

contrary, if the arm current is negative, the SMs with the highest capacitor voltages are activated, discharging the capacitors and decreasing their voltages. A performance example of the sorting-based voltage balancing algorithm is depicted in Fig. 2.15. This voltage balancing algorithm is simple and effective, but it implies the measurement and sorting of all the SM capacitor voltages at each sampling period. For this reason, it is difficult to implement and process in real-time in converters with high number of SMs.

Some voltage balancing techniques have also been developed for modulation techniques that directly link the carrier crossing events with particular SM switchings. In [23] a PS-PWM method is implemented, using a carrier and a modulation signal for each SM. The modulation signal, derived from the output voltage reference, is modified by a voltage balancing closed-loop controller. This loop adds an offset to the modulation signal proportional to the capacitor voltage error. This technique avoids the need of sorting the SM capacitor voltages but it requires an individual control loop for each SM. A block diagram of the voltage balancing algorithm used for the PS-PWM technique is shown in Fig. 2.16.

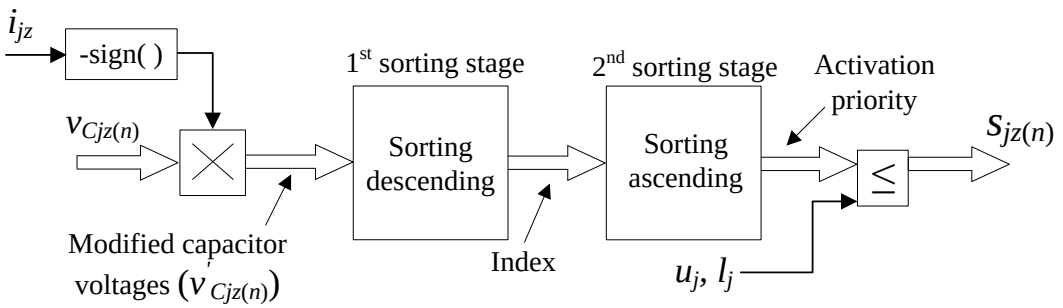


FIGURE 2.17: Block diagram of the voltage balancing algorithm based on two cascaded sorting structures.

2.4.1 Voltage Balancing Algorithms with Reduced Switching Frequency

Some modifications of the voltage balancing algorithm based on sorting the SMs have appeared in order to reduce the switching frequency of the converter. The algorithm presented in [32] significantly reduces the switching frequency by changing the state of only one SM per arm in each period. If the number of activated SMs increases, only the deactivated SMs are sorted out and the most suitable one is activated (the one with the lowest/highest voltage for positive/negative arm current). In contrast, if the number of activated SMs decreases, only the activated SMs are sorted out and the least suitable one is deactivated.

A detailed implementation of the sorting-based voltage balancing algorithm and the reduced switching frequency voltage balancing algorithm were presented in [91]. The sorting algorithm uses two cascaded index sorting structures and a simple comparator for the selection of the SMs and generation of the arm switching states. A block diagram of the sorting algorithm is depicted in Fig. 2.17. Firstly, the capacitor voltages are multiplied with the opposite sign of the arm current. If the current is positive, i.e., charging the capacitors, the capacitor voltages are multiplied by -1. On the contrary, if the current is negative, i.e. discharging the capacitors, the capacitor voltages are multiplied by one. Once the sign is adjusted, the voltages are sorted in descending order, providing the index of the sorted cells at the output. The result is sorted again, this time in ascending order and the index is also taken as output. The final result provides the activation priority of the SMs, 1 being the maximum priority and N the minimum one. The priority is compared with the number of activated SMs (u and l), activating all the SMs with a priority smaller or equal to the number of SMs to be activated.

An operation example of the double sorting algorithm when the current is positive is shown in Fig. 2.18. The SM capacitors with the lowest voltages are given the maximum priority (lowest number) and are the ones that are activated.

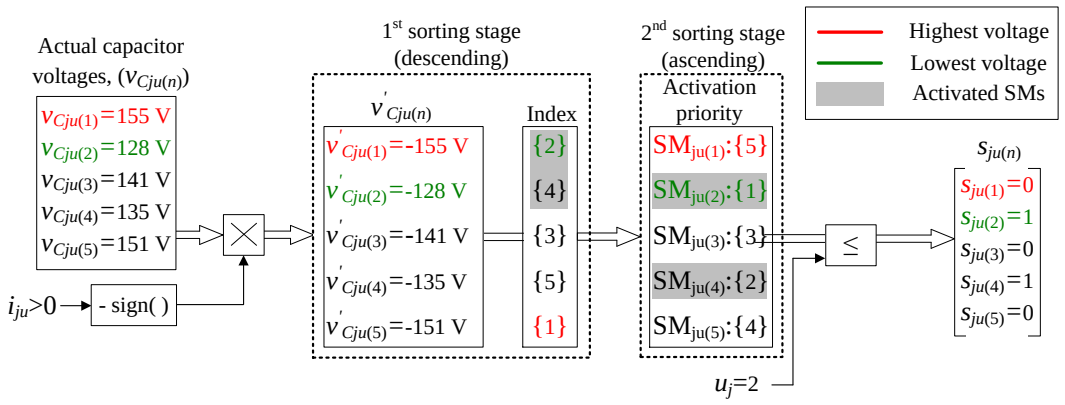


FIGURE 2.18: Example of the voltage balancing algorithm based on two cascaded sorting structures.

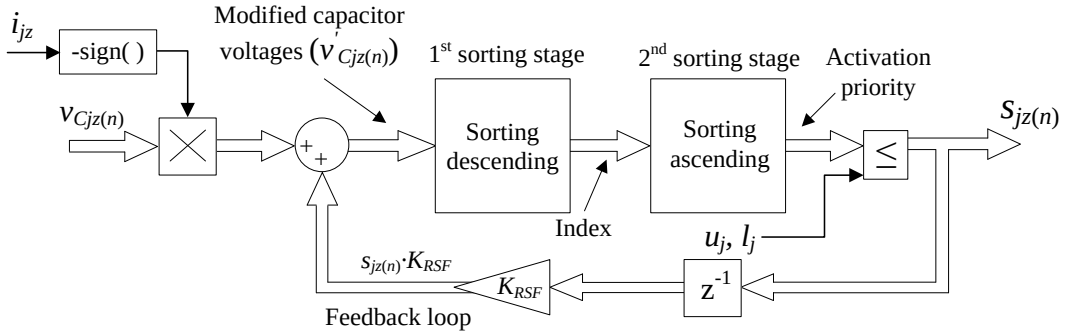


FIGURE 2.19: Block diagram of the reduced frequency voltage balancing algorithm.

Apart from the double sorting algorithm, a reduced-switching frequency algorithm is presented in [91]. The reduction on the switching frequency is provided by adding a feedback loop to the sorting algorithm. An offset is added to the voltages of the SMs that are activated, preventing them from deactivation until the total number of activated SMs is reduced. The offset has a value K_{RSF} high enough to maintain the SM activation independent of the capacitor voltage ripples. A block diagram of the reduced-switching frequency algorithm is depicted in Fig. 2.19.

The feedback loop ensures a higher priority to the SMs activated in the previous sampling time. However, the sorting processes are maintained, activating the most discharged (charged) SMs when the number of activated SMs increases and the current is positive (negative) and deactivating the most charged (discharged) SMs when the number of activated SMs decreases. A performance example of this voltage balancing algorithm can be seen in Fig. 2.20. Fig. 2.20(a) shows the application of the algorithm when the current is positive and two SMs are activated. Fig. 2.20(b) shows that a change in the current sign without changing the number of activated SMs, does not have any effect on the output state.

The reduced switching frequency voltage balancing algorithms are very useful when

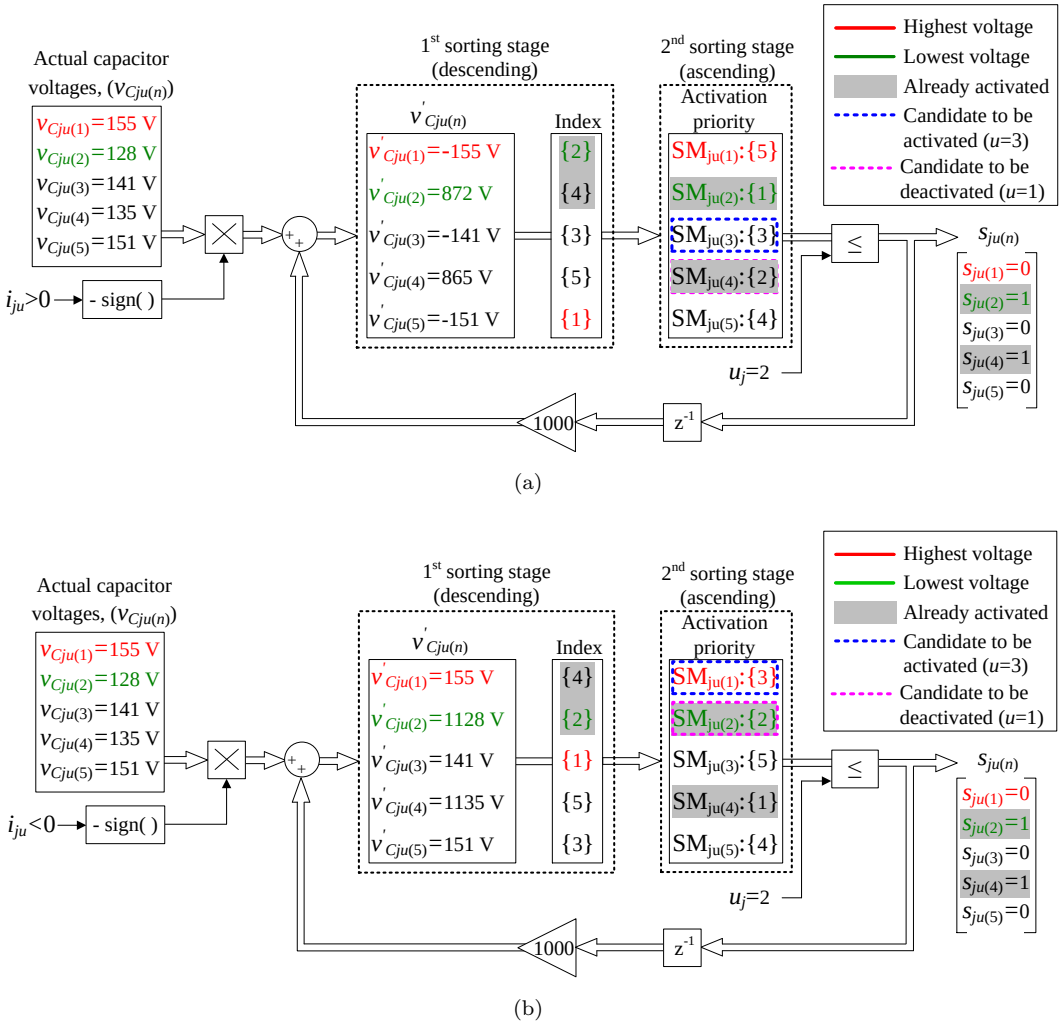


FIGURE 2.20: Example of the reduced switching frequency algorithm when two SMs per arm are activated for a positive arm current (a) and negative arm current (b).

combined with PWM techniques, as they reduce the switching frequency and switching losses of the converter without increasing the capacitor voltage ripples significantly [91]. However, the reduced switching frequency voltage balancing algorithm causes high capacitor voltage ripples when combined with NLM [91]. In this case, specific voltage balancing techniques adapted to the modulation technique should be used. A similar voltage balancing technique was presented in [24] for the use with NLM. In that technique, the switching frequency is reduced by both modifying the priority of the already switched-on SMs and the priority of the SMs that exceed the voltage limits.

2.5 Circulating Current

As defined in (2.9) and (2.10), the arm currents are composed of a common mode current i_{jcomm} and a differential or circulating current i_{jdiff}. The common mode current

provides the output current, while the circulating current flows within the arms of the converter without appearing at the output.

In order to identify the magnitude of the circulating current that appears naturally, its amplitude in an ideal situation is calculated. In an MMC with an infinite number of SMs, switching at infinite equivalent frequency and neglecting the effects of the inductors L, the model from Subsection 2.2.2 can be assumed. The circulating current is calculated for sinusoidal modulation signal v_{jm} and phase current i_j:

$$v_{jm} = m \cos \omega t \text{ and} \tag{2.36}$$

$$i_j = I_{ac} \cos\left(\omega t + \varphi\right) , \tag{2.37}$$

where m is the modulation index, ω is the modulation angular frequency, I_{ac} is the amplitude of the output current and φ is the output current phase angle. Substituting (2.36) and (2.37) into (2.23), the value of the circulating current is obtained:

$$i_{jdiff} = \frac{mI_{ac}}{4} \cos(2\omega t + \varphi) + \frac{mI_{ac}}{4} \cos(\varphi) . \tag{2.38}$$

This equation demonstrates that the circulating current is composed by two main components: a second harmonic component and a dc component. The second harmonic component does not have any essential use in the MMC performance and can be eliminated or controlled to a particular reference in order to reduce capacitor voltage ripples [7]. Moreover, in practical implementations, higher order harmonics appear in the circulating current [36], which can also be eliminated or controlled. On the contrary, the dc component is associated with the active power exchange between the dc-side and ac-side of the MMC [15] and cannot be eliminated.

Considering the existence of higher order harmonics, the differential current can be re-defined as:

$$i_{jdiff} = i_{dc} + \sum K_h I_{ac} \cos\left(h\omega t + \varphi_h\right) , \tag{2.39}$$

where h identifies the harmonic order, K_h is the amplitude of the harmonic relative to the amplitude of the output fundamental current, φ_h is the phase displacement of each harmonic and i_{dc} is the dc component of the differential current:

$$i_{dc} = \frac{mI_{ac}}{4} \cos(\varphi) . \tag{2.40}$$

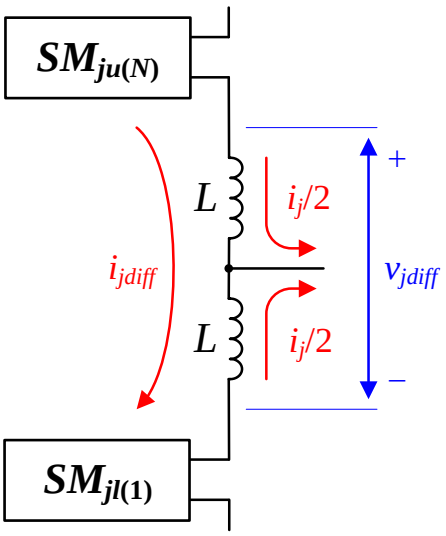


FIGURE 2.21: Representation of the differential voltage and current.

2.5.1 Control of the Circulating Current

The first studies about the control of the circulating current [34, 35] determined its relation with the inductance L and proposed to adjust the amplitude of the circulating current through the value of L. This passive method does not allow complete elimination of the circulating current neither its control to a predefined reference. For this reason, the circulating control is usually actively controlled through the differential voltage v_{jdiff}. As defined in (2.8), the circulating current has an integral relation with the differential voltage, that is, the voltage applied to the extremes of the inductances. A representation of the differential voltage and currents can be seen in Fig. 2.21.

The most common structure for controlling the circulating current [7] is to apply an offset to modulation signal of the upper and lower arms. The offset, added to the upper arm and subtracted to the lower arm, modifies the voltage generated by the arms, and creates a differential voltage. A block diagram of the circulating current control is depicted in Fig. 2.22. Defining the control offset as differential control signal Δv_{jm}, the new modulation signals for the upper (v_{jum}) and lower (v_{jlm}) arms can be defined as:

$$v_{jum} = v_{jm} + \Delta v_{jm} \text{ and} \tag{2.41}$$

$$v_{jlm} = v_{jm} - \Delta v_{jm} \, . \tag{2.42}$$

According to (2.8), the relation between the differential current and differential voltage is integrative. For this reason, the circulating current can be regulated with a simple proportional controller [37]. However, these equations are based on a simplified model,

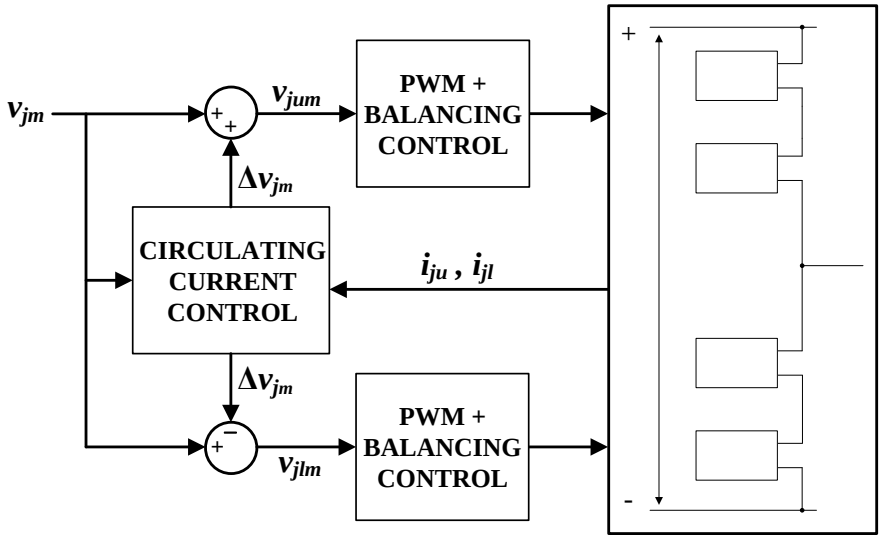


FIGURE 2.22: Block diagram of the circulating current control.

where the equivalent resistor in the arms is considered negligible. For this reason a proportional-integral (PI) controller can also be used [23].

A more complex technique widely used is a resonant or proportional-resonant (PR) controller [38, 39]. The resonant controller provides a high gain for a particular frequency, while rejecting all the other signals. Since this controller amplifies the feedback of a particular frequency, the static error of a fixed-frequency ac component can be eliminated. This technique is widely used to eliminate the second harmonic component of the circulating current. Using multiple PRs in parallel, multiple harmonic components can also be tracked (ω, 2ω, 4ω, etc). It has to be noted that in three-phase systems the component at 3ω is not tracked although it may appear in the current reference. This is because it would produce a current component that would not be cancelled with the other phase-legs and hence it would appear in the dc-link [8].

Other circulating current control techniques have also been studied in the literature. In [32, 42], the circulating currents in a three-phase system are translated to the double line-frequency rotational frame (d-q axis system) in order to eliminate the second harmonic of the circulating current. Recently, the use of repetitive controllers for eliminating the circulating current has been proposed [40, 41].

An alternative implementation of a circulating current controller was presented in [92, 93]. Instead of controlling the circulating current with the addition of a differential control signal to the modulation signal, this technique uses the available redundancies in the MMC controlled with $2N + 1$ modulation. The $2N + 1$ modulation is the control strategy where $2N + 1$ levels are implemented at the output of the converter, instead of the basic $N + 1$. This technique can be implemented by phase shifting by 180 degrees

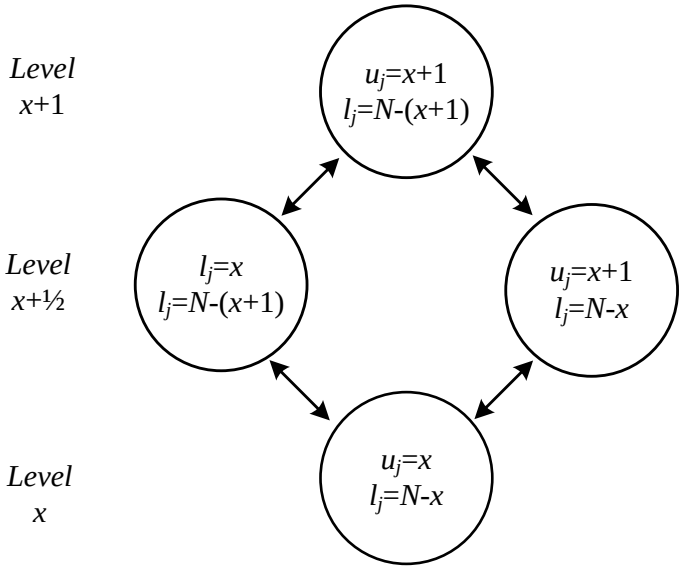


FIGURE 2.23: Transitions between adjacent levels and number of activated SMs in $2N + 1$ modulation.

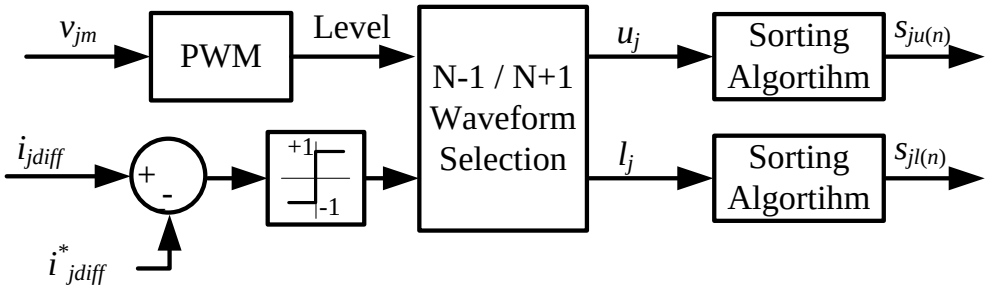


FIGURE 2.24: Block diagram of the circulating current control based on level redundancies.

the carriers of the arms (Sub-Section 2.3.3) or by directly modulating the converter with $2N$ carriers [21]. As introduced in Sub-Section 2.3.3, the additional levels of the $2N + 1$ modulation are intermediate levels that appear when the number of SMs in the phase-leg is $N + 1$ or $N - 1$. The same intermediate level can be implemented by adding an SM in the upper arm or subtracting it in the lower arm. An example of the additional level redundancies can be seen in Fig. 2.23. Although both options provide the same intermediate level, each option causes a differential voltage v_{jdiff} with different sign. The circulating current control presented in [93] uses this redundancy to control the circulating current. The measured circulating current is compared to its reference and an on/off control selects if the differential voltage must be positive or negative. A block diagram of this circulating current control can be seen in Fig. 2.24.

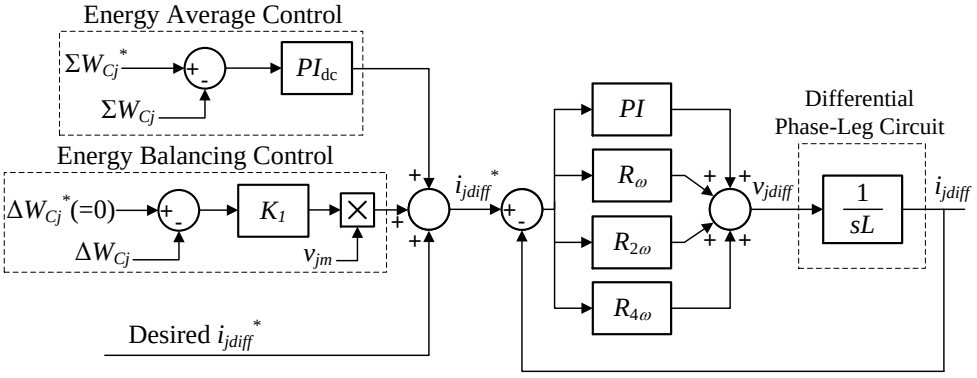


FIGURE 2.25: Block diagram of a circulating current controller.

2.5.2 Reference of the Circulating Current

The reference of the circulating current can be defined according to multiple objectives. Since the harmonic components of the circulating current increase the rms value of the arm current and the power losses of the converter, multiple studies propose to eliminate them, maintaining a circulating current composed by only the dc component. However, other studies propose to injection of particular harmonic components in order to improve the converter dynamics.

The dc component is the only one required for the operation of the converter. This component is used to maintain the energy in the phase-leg and its value can be estimated from the power transferred to the ac-side. However, to obtain an accurate dc reference, the energy stored in the capacitors have to be measured and the estimated reference corrected. This correction, usually calculated through a PI regulator, compensates for the converter power losses.

In most control systems, a first harmonic component is also added to the differential current. This component is used to transfer energy from the upper to the lower arms, balancing their energy levels when required [7, 39]. In order to correctly transfer energy between the arms, the current component has to be in phase with the arm voltages. A block diagram of a circulating current controller with an energy control system can be seen in Fig. 2.25. The system, based on PR controllers, includes a dc component regulator (i), a first harmonic energy balancing system (ii) and an externally defined circulating current reference, which can contain multiple harmonic components (iii).

Many other harmonic components can be used to improve the system dynamics, but the most common ones are the second and fourth harmonics. In fact, only even order harmonics not multiple of three can be used [8], otherwise they would flow through the dc-bus, which is not desired. The aim of injecting these harmonic components is to

reduce the capacitor voltage ripples, and consequently, to potentially reduce the capacitance needed given a maximum ripple. In [43], a dc component plus a second harmonic circulating current reference is determined from the instantaneous output power, cancelling the second harmonic power fluctuation in the arm. In [42], a second harmonic is calculated in closed-loop operation from the value of the capacitor voltages. In [8], both the second and fourth harmonic components are used for voltage ripple minimization, achieving a significant reduction in the voltage ripples and capacitor values. This topic has been studied in this thesis and is further explained in Chapter 3.

Finally, high-frequency components can be added to the circulating current combined with a common-mode signal in the modulation for transferring the power oscillations, and consequently the capacitor voltage ripples, to a higher frequency [45]. This technique can be used in low-speed motor drive applications, where the low frequency current causes excessive capacitor voltage ripples [94].

2.6 Voltage Control or Feed-forward Compensation

The performance of the modulation strategies depend on the variation of the SM capacitor voltages. If the SM capacitor voltage ripples are significant, the voltage synthesized at the output can present low-frequency distortion. In order to compensate for such distortion, a feed-forward voltage control loop can be included.

The most common voltage control loop [86] is based on measuring the capacitor voltages and correcting the modulation signal according to their value. If a common reference is used for all the SMs, like in PD-PWM, the average value of all the SMs is considered for adjusting the modulation signal of the upper and lower arms. However, if an individual reference is used for each SM [23], the correction is applied individually.

The voltage feed-forward compensation eliminates the low frequency output voltage distortion, but it can present stability problems. According to [7], the capacitor voltage ripples create a circulating current that balances the energy in the converter arms. The feed-forward compensation eliminates the effect of the capacitor voltage ripples in the output voltage and in the circulating current, deactivating the self-balancing mechanism. For this reason, the feed-forward compensation has to be complemented with total energy and energy balancing controllers. A block diagram of a feed-forward compensation is depicted on Fig. 2.26.

In converters with a high number of SMs, the measure of all the capacitor voltage can be a challenge. For this reason, some studies propose a feed-forward compensation based

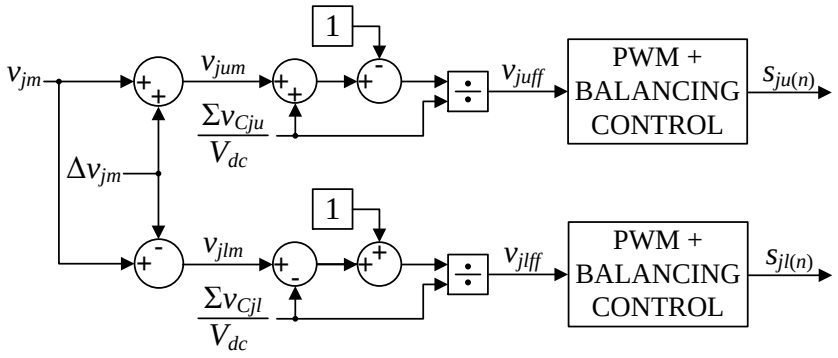


FIGURE 2.26: Block diagram of a voltage control based on feed-forward compensation.

on arm energy estimators [95, 96]. This technique calculates the voltage compensation from measuring the output current and dc-link voltage.

2.7 Output Current Control

Most applications include an external current control loop to define the MMC output voltage references. The track and control of an ac reference can be a difficult task for most linear controllers. For this reason, the current control is usually based on *d-q* variables. If the ac voltage frequency is constant and known (or can be measured with a phase-locked loop (PLL)), this technique allows to convert the ac waveforms to continuous variables.

Once the current is controlled in *d-q* coordinates, the current references can be defined as constant or calculated from an outer loop. The magnitude controlled by the outer loop depends on the application of the converter. In a grid-connected back-to-back application [9], one MMC is configured as a power controller, regulating the active and reactive powers supplied to the grid, while the other MMC regulates the reactive power and the dc-link voltage, usually with a voltage oriented control (VOC) structure. A block diagram of a grid-connected current controller is depicted in Fig. 2.26, where both power controlled and VOC strategies are detailed.

If the MMC is used in a motor drive application, the controlled variables are the flux and torque of the machine, usually with flux oriented control (FOC) [97] or direct torque control (DTC) strategies. The torque reference is usually defined by a speed control loop.

In the recent years, multiple studies have developed current control strategies for unbalanced grids [98, 99] and systems tolerant to single-line-to-ground faults [62]. Those techniques are based on decoupling the measured currents and voltages into the positive,

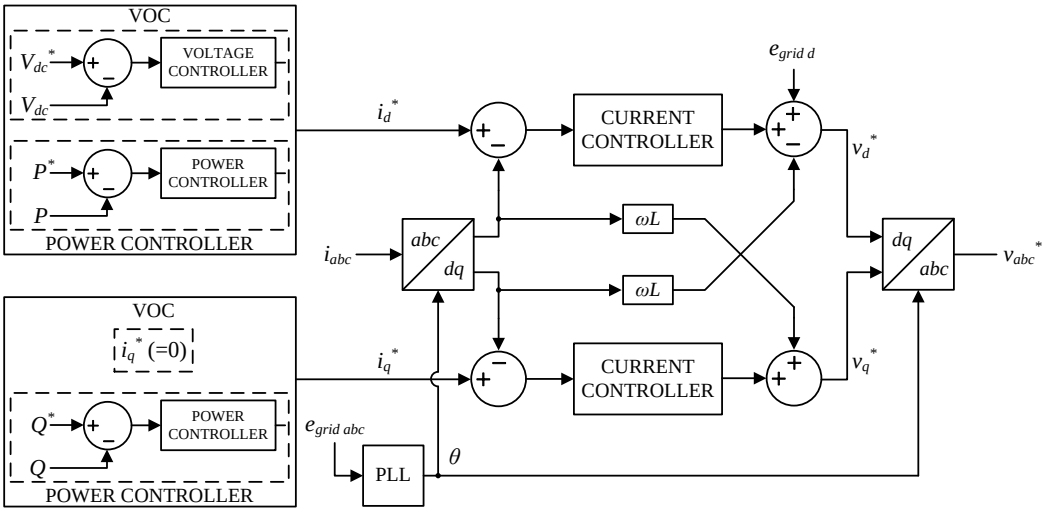


FIGURE 2.27: Block diagram of a grid-connected current control loop.

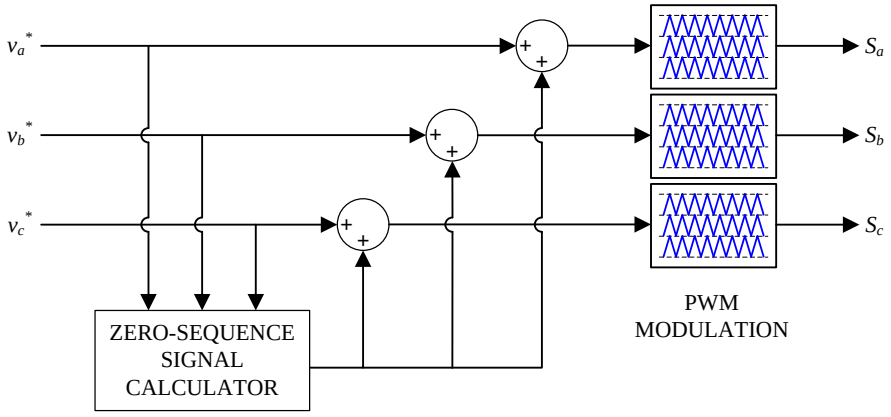


FIGURE 2.28: Block diagram of the zero-sequence injection.

negative and zero-sequence components and afterwards individually controlling each component.

2.8 Zero-sequence Component

The injection of a zero-sequence signal is a widely extended practice for converters operating over Delta-connected loads and Wye-connected loads with open neutral. The absence of the neutral current path allows the addition of a zero-sequence voltage, i.e. a voltage common to the three phases, that modifies the modulation signals without affecting the line-to-line output voltages [100]. Fig. 2.28 shows a block diagram of the zero-sequence injection.

A widely used technique is the addition of a third harmonic component in the modulation signal. The third harmonic reduces the peak voltage of the modulation signal

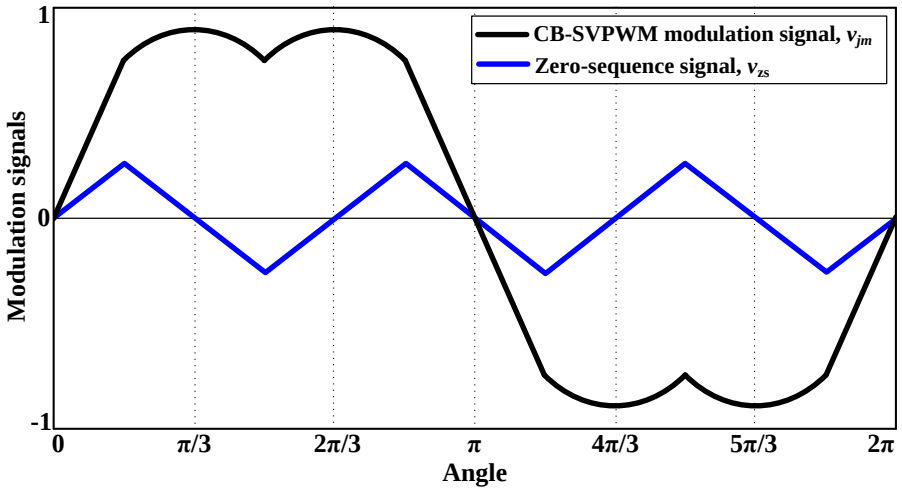


FIGURE 2.29: Example of CB-SVPWM, showing the zero-sequence and the resulting modulation signal.

without modifying the output voltage. This technique allows to increase the linear modulation range of the converter. Another widely used technique is to add the same zero-sequence signal created by a space-vector modulation (SVM) strategy [48,49]. The modulation based on this zero-sequence signal will be hereinafter called carrier-based space-vector pulse-width modulation (CB-SVPWM). An example of CB-SVPWM is shown at Fig. 2.29. This technique allows an increase of about 15% of the linear range of the modulation signal and the zero-sequence signal is defined as:

$$v_{zs} = -\frac{\max\{v_a, v_b, v_c\} + \min\{v_a, v_b, v_c\}}{2} , \tag{2.43}$$

2.9 Applications of the MMC

The particular features of the MMC make it suitable for high/medium voltage/power applications. Although the most common application is HVDC transmission [89], the MMC is also used in motor drives [101], grid interties [43] and static compensators (STATCOM) [11].

In the recent years, the MMC topology has become the most potential candidate for HVDC applications. Not only lots of academic papers have been published applying the MMC topology to HVDC [9,18,35,89,102], but also the principal manufacturers in this field have presented new products based on the MMC or variations of the same topology. Siemens Energy Sector commercialises the basic MMC topology [4,103,104] under the commercial brand of HVDC PLUS. The first HVDC PLUS installation was the Trans Bay Cable Project, a 88 km-long transmission line of ±200kV and 400 MW commissioned

in 2007 in California. Another important installation in process is the INELFE project, a 65 km-long transmission line of ±320kV and 2000MW between Spain and France. ABB Power Systems commercialises a multilevel converter based on the MMC topology under the name of cascaded two-level (CTL) HVDC LIGHT [105–107]. Alstom Grid also commercialises a multilevel converter under the name of HVDC MaxSine [108, 109]. Although this converter is based on the alternative arm converter (AAC) topology [84], its structure and operation concept is very similar to the MMC.

A second widely investigated application of the MMC is its use to motor drives. This topology might be a very interesting solution for driving high-power wind turbines, but some operational problems have still to be solved [110]. The main problem for the application of the MMC to motor drives is that the capacitor voltage ripples are inversely proportional to the output frequency. Therefore, in low speed operation of the motor, the capacitor voltage ripples can be excessively high. This topic is further investigated on Chapter 8, where some of the existing techniques for reducing the capacitor voltage ripples at low-speed operation are compared with a technique developed during this thesis.

Other applications where MMCs could be used are interties between different voltage and frequency grids. The application of an MMC for the interconnection of the European 15kV/16.7Hz rail supply with the 50Hz grid is considered in [43]. The use of MMCs as STATCOMs [11, 111, 112] is another widely studied application field.

2.10 MMC Prototypes

The experimental results presented in this thesis have been obtained with three different experimental prototypes. Most results have been obtained with a three-phase MMC prototype that has been developed during this thesis in the TIEG-P facilities in Terrassa. The prototype has been developed from scratch, designing the schematics and printed-circuit board (PCB) of the SMs, sensors and control boards to implement and assembling all of them. However, the designed prototype was not ready when the first investigations were tested and an alternative prototype had to be used. The results obtained for the first papers derived from this thesis were obtained from a phase-leg prototype in the University of New South Wales (UNSW), Sydney, Australia. Also, part of this thesis has been developed during a research stay at the University of Nottingham, UK, where the results were obtained using an AAC prototype that performed as an MMC.

TABLE 2.1: Specifications of the TIEG-P prototype

Parameter	**Value**
Number of SMs per Arm, N	4 or 8
SM Capacitors, C	1500 μF
Arm Inductors, L	3 mH
Rated Power, P_{out}	10 kVA

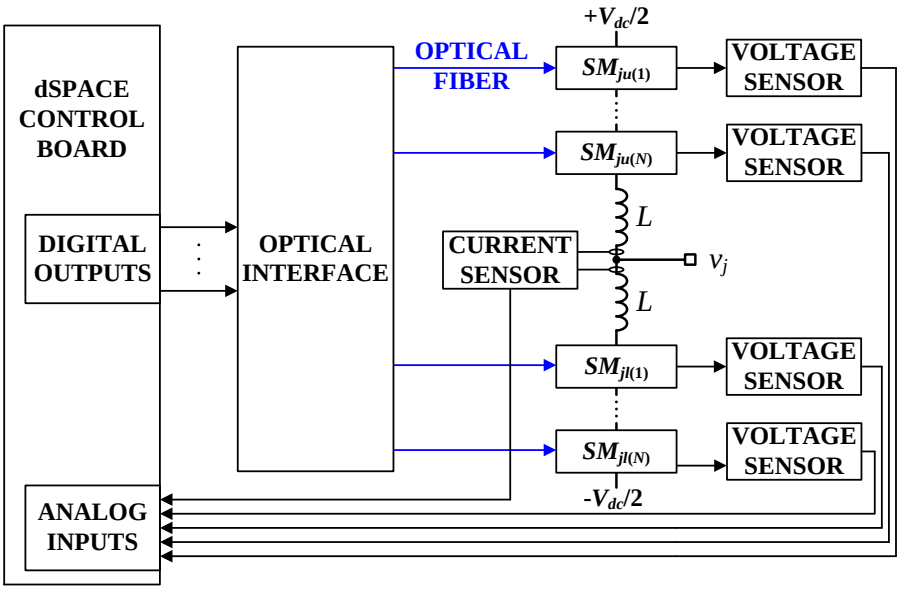


FIGURE 2.30: Block diagram of control and measure boards for one phase-leg of the TIEG-P prototype.

2.10.1 TIEG-P prototype

A prototype of MMC has been designed and implemented during the development of this thesis. The TIEG-P prototype has been implemented with a modular and configurable structure, using different configurations. For studies where a high number of SMs were required, the prototype was used as a single-phase converter with eight SMs per arm ($N = 8$). For studies where a three-phase system was required, the converter was converted into a three-phase MMC with four SMs per arm ($N = 4$), achieving a rated power of 10 kVA. Main characteristics of TIEG-P prototype are given in Table 2.1

The design consists on four different boards: the SMs, the voltage sensors, the current sensors and the optical interface. The control of the prototype is performed through a dSPACE device, a single board DS1103 for the single-phase configuration and a modular dSPACE DS1006 with two high-speed analog-to-digital boards and a field programmable gate array (FPGA) board for the three-phase configuration. A block diagram of the control and measure boards for one phase-leg of the prototype is depicted on Fig. 2.30.

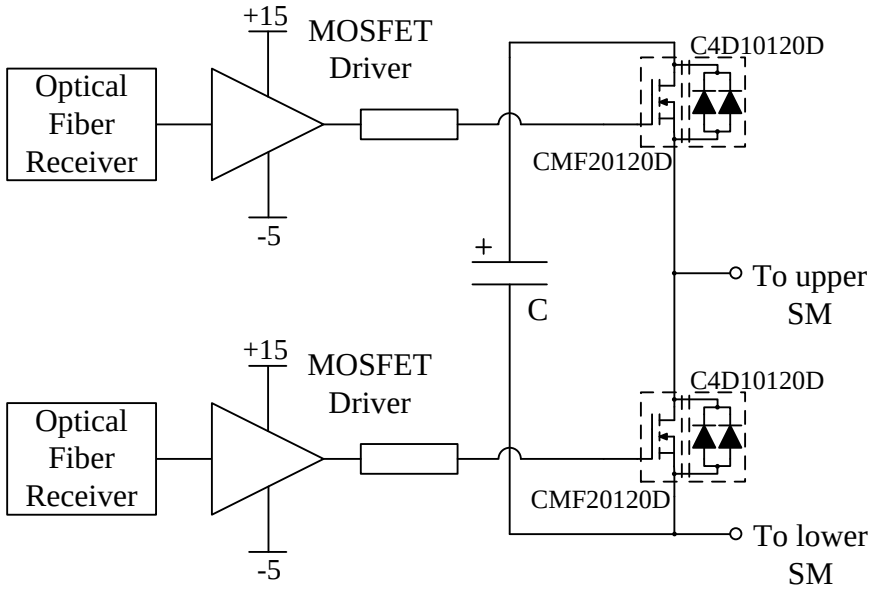


FIGURE 2.31: Simplified circuit diagram of the TIEG-P SM prototype.

Each SM is implemented in an individual board, including the power switches, the gate drivers, the optical interface and the SM capacitor. The power switches are based on silicon-carbide (SiC) technology, with MOSFET devices CREE CMF20120D and Schottky diodes CREE C4D10120D. The power switches have been rated at 1200 V and 42 A, but the SM capacitor has been rated at 250 V, reducing the maximum voltage of the SM. The capacitance of the SM is 1500 μF. Fig. 2.31 shows a simplified circuit diagram of the SM.

The voltage and current sensors measure the variables and provide isolated and adapted output signals for the dSPACE input levels ($\pm$15 V). Each voltage sensor is implemented in an individual board, scaling the voltage through a resistive voltage divider and providing isolation with a linear optocoupler. The current sensors are implemented in a different board, using two sensors in the same board. The measurement and isolation is performed through a LEM Hall effect sensor.

The last designed board is an optical interface, which converts the digital signals provided by the dSPACE to optical signals for the activation of the SMs. This board also implements some logic operation, like emergency stop, demultiplexing the upper and lower switch signals (the dSPACE provides the state of the SM but not the state of the switches) and the dead-time between the upper and lower switches of the SM.

Pictures of the single-phase and three-phase configurations can be seen in Figs. 2.32 and 2.33, respectively.

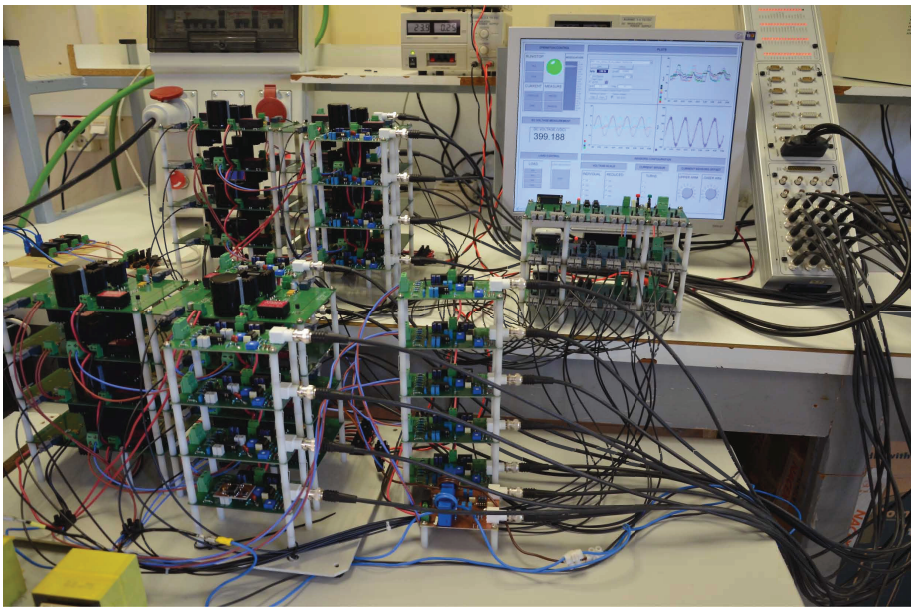


FIGURE 2.32: TIEG-P experimental prototype configured as a single-phase MMC.

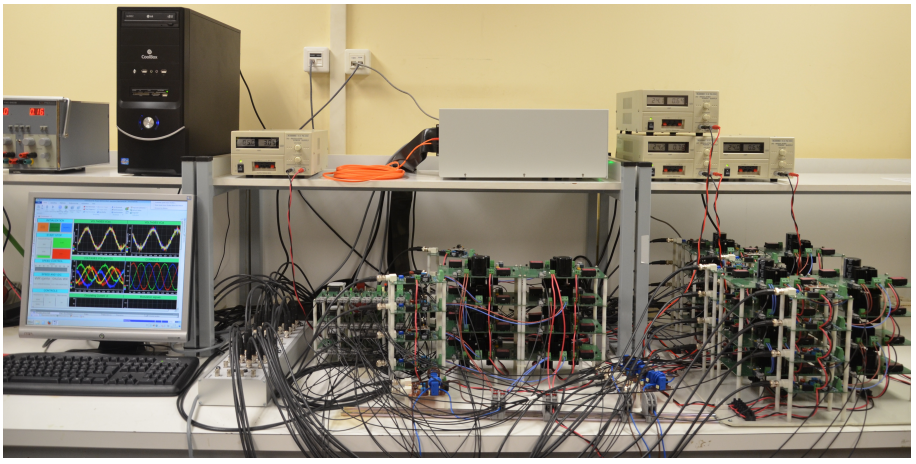


FIGURE 2.33: TIEG-P Experimental prototype configured as a three-phase MMC.

2.10.2 UNSW Prototype

The UNSW prototype is a single-phase MMC from the Australian Energy Research Institute (AERI). This 5-kVA converter is composed of five SMs per arm ($N = 5$) and operates with passive loads connected between the phase output and the midpoint of the dc-link, created using two series-connected capacitors (C_{dc}). The control is implemented using a dSPACE dS1103 board, and the main characteristics are given in Table 2.2. A picture of the converter can be seen in Fig. 2.34.

TABLE 2.2: Specifications of the UNSW prototype

Parameter	**Value**
Number of SMs per Arm, N	5
SM Capacitors, C	3600 μF
Arm Inductors, L	3.6 mH
DC-Link Capacitors, C_{dc}	3300 μF
Rated Power, P_{out}	5 kVA

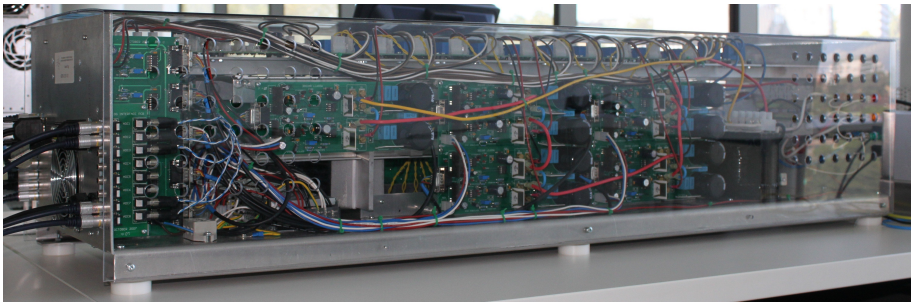


FIGURE 2.34: Experimental prototype from the UNSW.

2.10.3 University of Nottingham AAC Prototype

In order to acquire some experience in an international centre, part of this thesis was developed during a research stay in the PEMC group of The University of Nottingham, UK. At the time of the stay, the host research group did not have a three-phase MMC available and all the experiments were performed in an AAC prototype, which control was adapted to perform as an MMC. An AAC consists in an MMC with full-bridge SMs and a power switch (IGBT) in-series with the arms. However, if the full-bridges are controlled as half-bridges and the series power switches are always on, its performance is the same than an MMC but with some additional losses.

The AAC prototype is a 10-kVA three-phase system with four SMs per arm ($N = 4$). The SMs include multiple capacitors, allowing the use of multiple configurations, from a minimum capacitance of 75 μF to a maximum of 303 μF. The passive values are smaller than usual MMC prototypes, but they were calculated for AAC operation. The control of the AAC prototype is performed through four FPGA boards, i.e. one per each phase-leg and a master board, and a digital signal processor (DSP) controller. Main characteristics of the AAC prototype are summarized in Table 2.3, and a picture can be observed on Fig. 2.35.

TABLE 2.3: Specifications of the University of Nottingham prototype

Parameter	**Value**
Number of SMs per Arm, N	4
SM Capacitors, C	75 μF to 303 μF
Arm Inductors, L	2 mH
Rated Power, P_{out}	10 kVA

FIGURE 2.35: Experimental AAC prototype from The University of Nottingham.

Chapter 3

Circulating Current References for Capacitor Voltage Ripple Reduction

This chapter presents three techniques for calculating the reference of the circulating current. These techniques are focused on reducing the capacitor voltage ripples. The first technique defines a continuous function of the capacitor voltage ripples and minimizes it, calculating an optimal second harmonic current for reducing the capacitor voltage ripples. The second technique implements an off-line iterative optimization technique, which evaluates all the possible combinations of amplitude and phase of the second and fourth harmonics, and selects the optimal one for minimizing the capacitor voltage ripples. Finally, the third technique calculates two theoretical optimum references, based on simplified models of the converter. The third technique provides results close to the optimal ones with a reference calculated easily from the instantaneous values of current and modulation signal.

3.1 Introduction

The differential or circulating current is a current component that flows within the arms of the converter without appearing at the output. The circulating current is usually controlled in order to improve the dynamic performance of the converter. However, the reference of this current can be settled according to different objectives, such as reducing the current in the converter arm by eliminating all the harmonic components [7, 23, 32], or redistributing the energy between the arms by injecting controlled harmonic components [7, 8].

Most studies follow the objective of eliminating the circulating current, reducing the rms value of the arms currents and, therefore, the power losses of the MMC. However, the techniques studied in this thesis look for the reduction of the capacitor voltage ripples. Reducing the capacitor voltage ripples is an important target because it enables the use of smaller capacitors [44]. This eventually helps to reduce the cost of the MMC due to the large number of capacitors integrated in the topology.

3.2 Quadratic Function Optimization Technique

The first technique studied was presented in [88] and calculates the optimum second harmonic component of the circulating current for minimizing the capacitor voltage ripples. Considering the mathematical models of the MMC developed in Chapter 2, a quadratic cost function of the capacitor voltage is obtained and optimized by equalling its gradient (partial derivatives in a multivariable system) to zero. The function is optimized for the second harmonic component, providing the amplitude and phase that minimizes the capacitor voltage ripples.

The variable that we want to optimize is the amplitude of the capacitor voltage, which can be defined as the difference between the maximum and minimum value of $v_{Cju(n)}$.

$$\Delta v_{Cju(n)} = \max\{v_{Cju(n)}\} - \min\{v_{Cju(n)}\} \ . \tag{3.1}$$

Since $\Delta v_{Cju(n)}$ is not a continuous equation, it is not derivable, and therefore difficult to optimize. For this reason, the capacitor voltage ripple is optimized through an indirect optimization function. Considering the locally averaged capacitor voltage obtained in Subsection 2.2.2:

$$\overline{v_{Cju(n)}} = \frac{1}{C}\int_0^t \overline{i_{ju}}\frac{1-v_{jm}}{2}dt + V_{Cju(n)0} \ , \tag{2.28 revisited}$$

the new cost function F_{opt} is defined as the integral of the quadratic function of the current in the capacitor:

$$F_{opt} = \int_0^t \left(i_{ju}\frac{1-v_{jm}}{2}\right)^2 dt \ . \tag{3.2}$$

The optimization function F_{opt} does not directly represents the amplitude of the capacitor voltage ripple, but by reducing the quadratic function, the ripple $\Delta v_{Cju(n)}$ is reduced as well. The constant C and the initial voltage $V_{Cjun(n)0}$ from (2.28) have been ignored in the cost function because they do not affect in the optimization process. The

optimization process is only performed for the upper arm because in a simplified model the upper and lower arm voltages have the same performance but half period displaced.

The cost function is evaluated considering the basic arm current equation, given in (2.9), where the differential current is composed by a dc component plus the optimal harmonic components:

$$i_{jdiff} = i_{dc} + \sum K_h I_{ac} \cos\left(h\omega t + \varphi_h\right) \ , \qquad \text{(2.39 revisited)}$$

where i_{dc} is the dc component related with the converter energy transfer defined in (2.40).

This function can be evaluated for different order harmonic currents, but in this study only the optimal second order harmonic is calculated, since it is the most significant component that contributes to the capacitor voltage ripples. Considering the differential current (2.39), a sinusoidal modulation signal (2.36) and sinusoidal output current (2.37), (3.2) can be developed as:

$$\begin{aligned} F_{opt}\left(K_2, \varphi_2\right) = \int_0^t \Bigg[\Bigg(& \frac{I_{ac}}{2} \cos\left(\omega t + \varphi\right) + \frac{I_{ac}\, m}{4} \cos\left(\varphi\right) \\ & + K_2 I_{ac} \cos\left(2\omega t + \varphi_2\right) \Bigg) \frac{1 - m\cos\left(\omega t\right)}{2} \Bigg]^2 dt \ . \end{aligned} \qquad (3.3)$$

The optimal values of phase angle and amplitude of the second harmonic are obtained by equalling the gradient of the cost function to zero and solving the equation:

$$\nabla F_{opt}\left(K_2, \varphi_2\right) = 0 \ . \qquad (3.4)$$

3.2.1 Simulation Results

The effectiveness of the quadratic function optimization technique on reducing the capacitor voltage ripples has been demonstrated by simulation results. The capacitor voltages obtained when using the optimal current as a reference for the circulating current controller have been measured and compared to the capacitor voltages when using only a dc component, as proposed in [7, 32], and to when no circulating current controller is used. The results have been obtained in a switched model of the MMC with the characteristics detailed in Table 3.1.

Fig. 3.1 depicts a comparison of the capacitor voltage ripples under three scenarios: (i) with no circulating current control; (ii) with a circulating current control using only a dc component as a reference; and (iii) with a circulating current control using a dc

TABLE 3.1: Specifications of the Simulation Test Converter Used for the Quadratic Function Optimization Technique

Parameter	**Value**
Number of SMs per Arm, N	4
SM Capacitors, C	1360 μF
Arm Inductors, L	6 mH
DC-Link Voltage, V_{dc}	6 kV
AC-Side rms Current, $I_{ac\,rms}$	10 A
Modulation Index, m	1
Output Current Phase Angle, φ	0°
Carrier Frequency, f_{cr}	4 kHz
Output Frequency, f	50 Hz

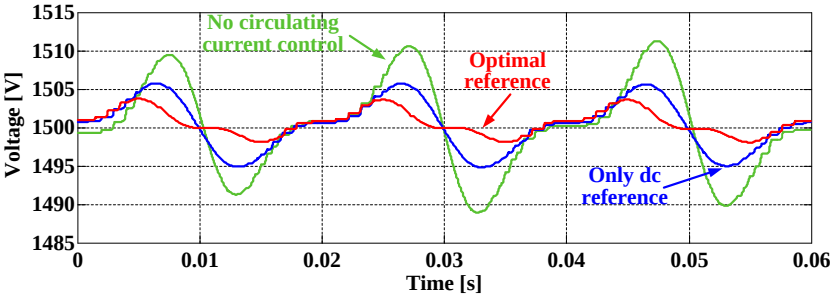


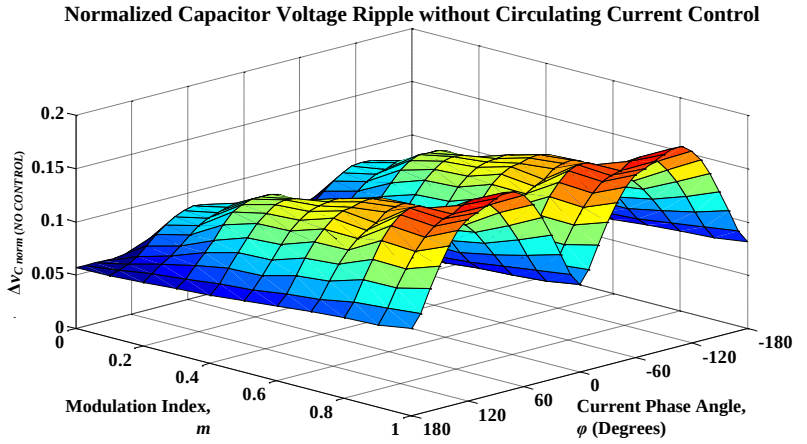
FIGURE 3.1: Capacitor voltage ripples when using the optimal second harmonic component obtained with the quadratic function as a reference, when using only a dc component as a reference and when the circulating current is not controlled.

component plus the optimal second harmonic component obtained with the quadratic function optimization technique. It can be seen that the capacitor voltage ripples obtained with the optimal current are significantly smaller than when only a dc component is injected and than when the circulating current is not controlled.

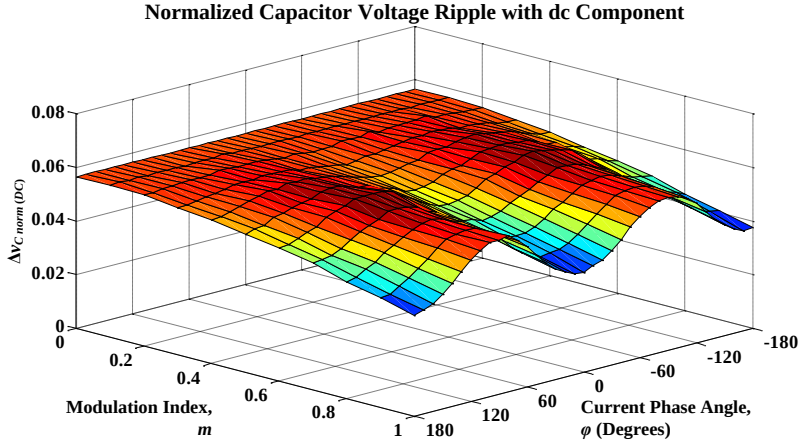
In order to visualise the difference in the capacitor voltage ripple amplitudes for different operating conditions, a sweep in the modulation index m and in the ac-side current phase angle φ has been performed. Simulation results can be seen in Fig. 3.2, where the capacitor voltage ripple amplitudes obtained with the three compared strategies are depicted for multiple operating points. The capacitor voltage ripples have been normalized with respect to the following equation:

$$\Delta v_{Cnorm} = \frac{\Delta v_C f C}{I_{ac\,rms}} \,, \tag{3.5}$$

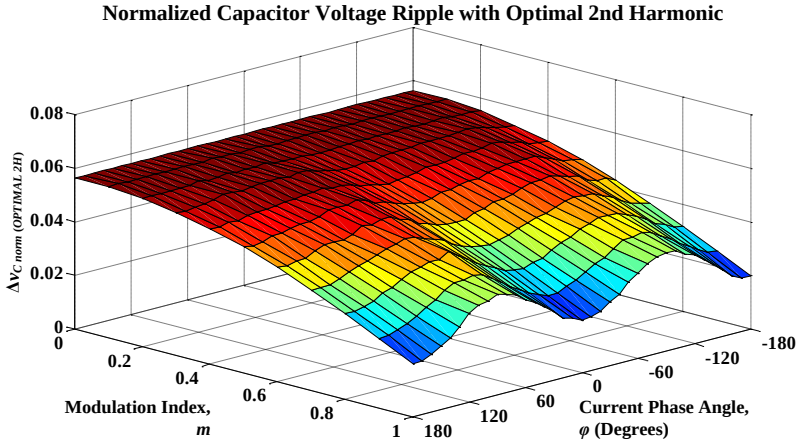
Fig. 3.3 depicts the ratio between the capacitor voltage ripples when using the optimal second harmonic current and when using only a dc-component. The figure shows



(a)



(b)



(c)

FIGURE 3.2: Normalized amplitude of the capacitor voltage ripples: (a) with no circulating current control, (b) with a circulating current control using only a dc component as a reference, and (c) with a circulating current control using a dc component plus the optimal second harmonic component obtained with the quadratic function optimization technique.

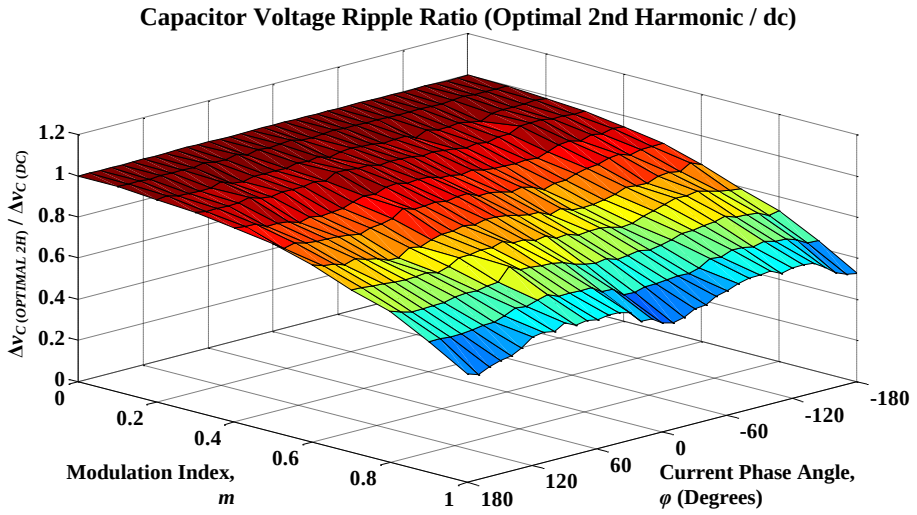


FIGURE 3.3: Ratio between the capacitor voltage ripples obtained with the optimal second harmonic and the capacitor voltage ripples obtained with a dc component.

that the ratio is always under the unit, demonstrating that the optimal current reduces the capacitor voltage ripples under all the operating conditions. Moreover, it can be observed that the capacitor voltage ripple reduction is higher at high modulation indices, which is the operation region of high-power grid-connected converters.

3.3 Iterative Optimization Technique

Most of the optimization techniques, like the one presented in Section 3.2, are based on approximation techniques, and cannot claim that actual minimum capacitor voltage ripple amplitudes are achieved. In this section, a different optimization technique is presented [113], which as a difference from other techniques, is based on an iterative optimization algorithm. In this method, all the possible combinations of circulating currents (amplitude and phase for different harmonic currents) within a bounded range are evaluated using the averaged capacitor voltage equation, given in (2.28), and the one which produces the lowest capacitor voltage ripple amplitude is selected as the optimal one.

The iterative optimization method has been applied for multiple operating conditions of the MMC, regarding modulation index and relative phase of the output current. As a result, a set of tables have been obtained, one for each of the optimized variables, indicating the optimal amplitude and phase of the circulating current harmonics for each operating point. The study has been performed considering two circulating current patterns: using a dc component plus a second harmonic; and using a dc component plus a set of second and fourth harmonics. It must be noted that in order to obtain

the minimum capacitor voltage ripples, the second harmonic component may present different values for each pattern.

In order to simulate a practical application, a three-phase system where the modulation signal includes the CB-SVPWM zero-sequence signal has been considered. This modulation technique has been detailed in Subsection 2.8 and increases the linear modulation range about a 15%.

The capacitor voltage amplitudes are obtained by calculating the instantaneous values of the capacitor voltage (2.28) during one period, and then calculating the voltage ripple (3.1). Due to the non-linear zero-sequence, the development of (2.28) results in a piece-wise function. The voltage ripple is calculated inside multiple chained loops, each one ranging the bounded values of the optimized variables, and the different operating points tested. The results are the optimal amplitudes (K_2 and K_4) and phases (φ_2 and φ_4) that provide the minimum capacitor voltage ripple for each operating point (m and φ). In order to reduce the processing time, the phase angle values of the fourth harmonic (φ_4) have been defined as an array instead of a loop. A block diagram of the algorithm applied for calculating the optimal results for the set of second and fourth harmonic components is shown at Fig. 3.4.

In contrast to the quadratic approximation, this optimization method is an off-line technique that requires long processing times to obtain the results (a few days using a standard personal computer). Nevertheless, the results can be saved in look-up tables and used in a real-time application. The minimization algorithm has been implemented in MATLAB.

3.3.1 Simulation Results

In the first place, the expected capacitor voltage ripples have been evaluated by simulation studies. Simulations have been performed over an averaged model of the converter, which consists in applying the averaged capacitor voltage equation (2.28) for a fundamental period when the differential current (2.39) is composed of the energy-related dc component (2.40) plus the optimal harmonics. Results are presented with normalized variables, providing the capacitor voltage ripple amplitudes in the form of (3.5). Fig. 3.5 shows the normalized capacitor voltage ripples when using the set of optimal second and fourth harmonics for all the operating conditions considered, i.e. modulation index and phase angle of the output current. It can be seen that, for high modulation indices, the normalized capacitor voltage ripples reach very low values, around 0.01 p.u. These values contrast with the ones obtained with the quadratic function optimization technique, previously shown at Fig. 3.2(c), where a minimum ripple of 0.02 p.u. is achieved.

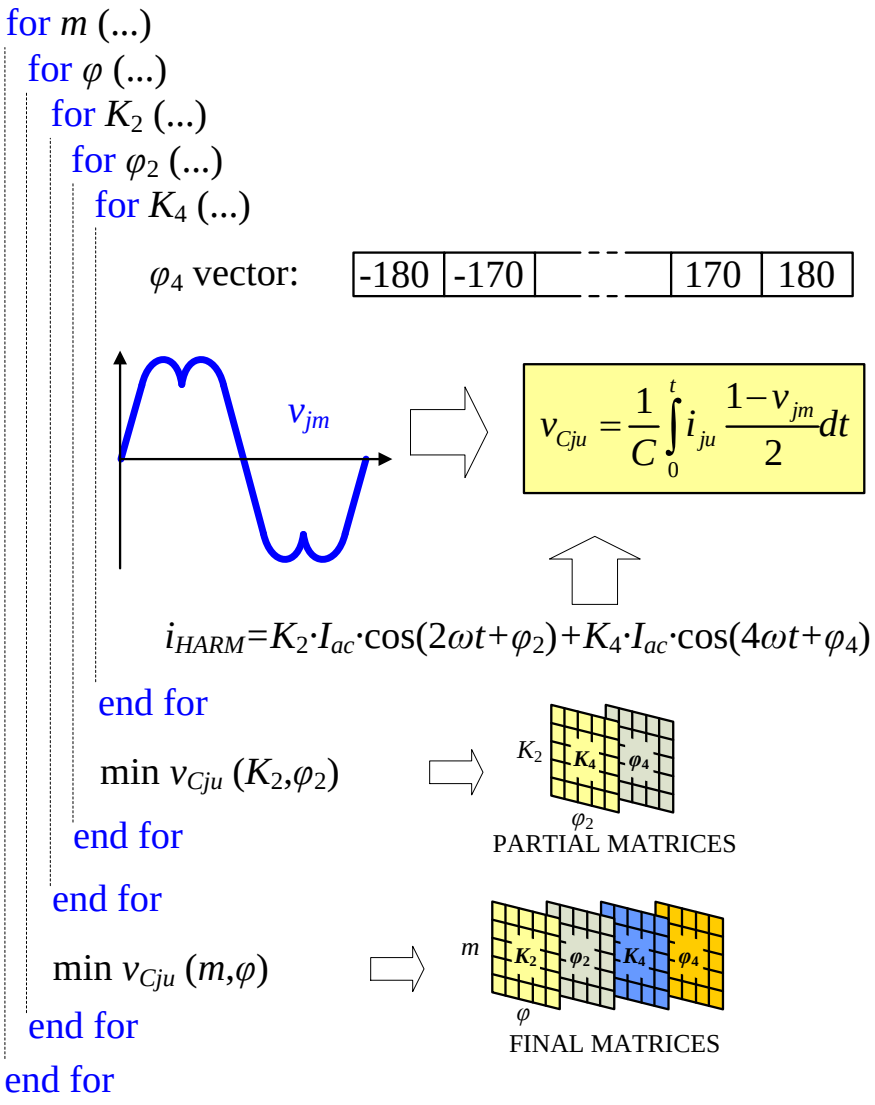


FIGURE 3.4: Block diagram of the iterative optimization algorithm for the set of second and fourth harmonic components.

The reduction of the capacitor voltage ripples is not only caused by the use of the iterative optimization technique, but also for the use of a set of second and fourth harmonic components. This fact can be seen at Fig. 3.6, where the ratio between the capacitor voltage ripple amplitudes obtained with the optimal set of second and fourth harmonics and the obtained with the optimal second harmonic obtained by iterative optimization is depicted. It can be seen that the addition of a fourth harmonic increases the reduction of the capacitor voltage ripples for high modulation indices and highly reactive currents.

As studied in [8, 32], the main drawback of the injection of harmonic components is an increase of the rms value of the arm current, and therefore, an increase of the conduction losses of the converter. For this reason, the rms value of the arm current

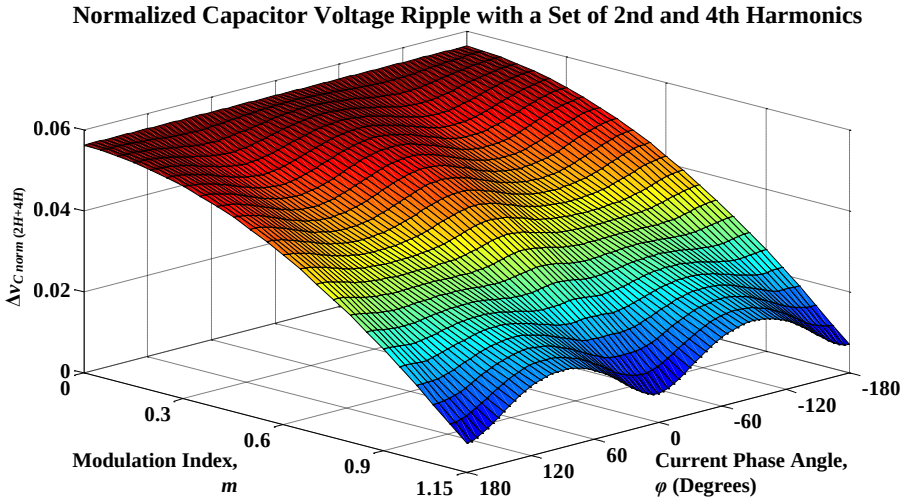


FIGURE 3.5: Normalized capacitor voltage ripple amplitudes when using the set of optimal 2nd and 4th harmonics obtained by iterative optimization.

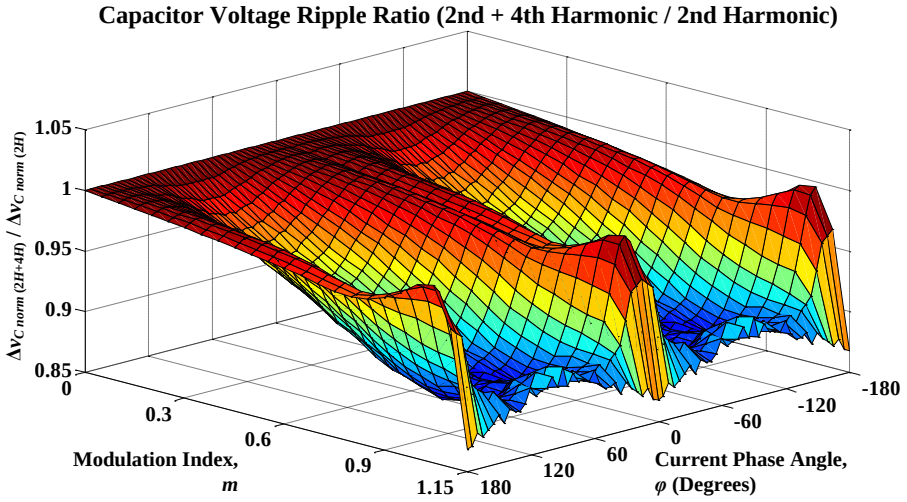


FIGURE 3.6: Capacitor voltage ripples ratio between the optimal set of second and fourth harmonics and the optimal second harmonic obtained by iterative optimization.

when using the optimal harmonic currents has also been evaluated. Fig. 3.7 shows the normalized rms arm current value when the set of optimal second and fourth harmonics is considered. It can be observed that the current increases with the modulation index, reaching its maximum value at $m = 0.7$. The current has been normalized according to:

$$i_{jz\,norm} = \frac{i_{jz\,rms}}{i_{j\,rms}} \,, \tag{3.6}$$

being $z \in \{u, l\}$ the upper or lower arm identifier.

The use of a set of second and fourth harmonics reduce the capacitor voltage ripples, but it also increases the rms current value. This can be seen in Fig. 3.8, where the ratio between the rms arm current of the optimal set of second and fourth harmonics and the

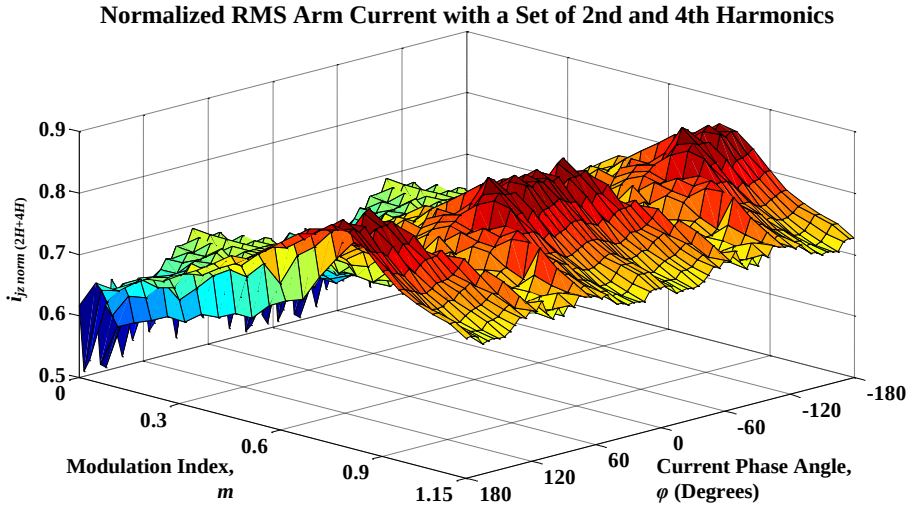


FIGURE 3.7: Normalized rms arm current when using the set of optimal 2nd and 4th harmonics obtained by iterative optimization.

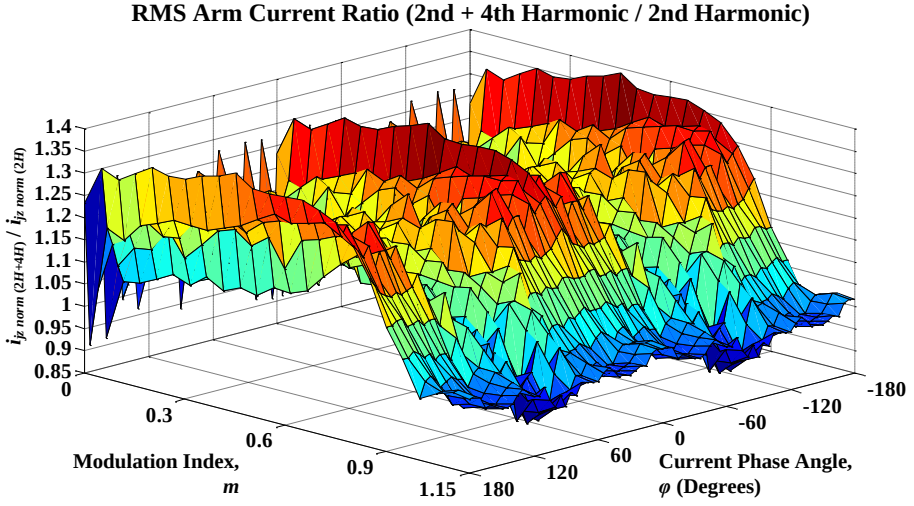


FIGURE 3.8: Ratio between the rms arm current when using the set of optimal 2nd and 4th harmonics and the rms arm current when using the optimal 2nd harmonic obtained by iterative optimization.

rms arm current of the optimal second harmonic, is represented. The set of second and fourth harmonics significantly increases the rms value for almost all operating conditions, except for high modulation indices, where it presents almost the same value or even achieves a small reductions of the rms current.

The results demonstrate that the use of an optimal set of second and fourth harmonics in the circulating current is recommended for reducing the capacitor voltage ripples. Its benefits are more important for high modulation indices, when it does not significantly increase the rms arm current, and therefore, the power losses.

TABLE 3.2: Specifications of the Simulation Test Converter Used for the Iterative Optimization Technique

Parameter	**Value**
Number of SMs per Arm, N	5
SM Capacitors, C	3600 μF
Arm Inductors, L	3.6 mH
DC-Link Voltage, V_{dc}	300 V
AC-side rms Current, $I_{ac\,rms}$	3.75 A
Modulation Index, m	0.9
Carrier Frequency, f_{cr}	4 kHz
Output Frequency, f	50 Hz

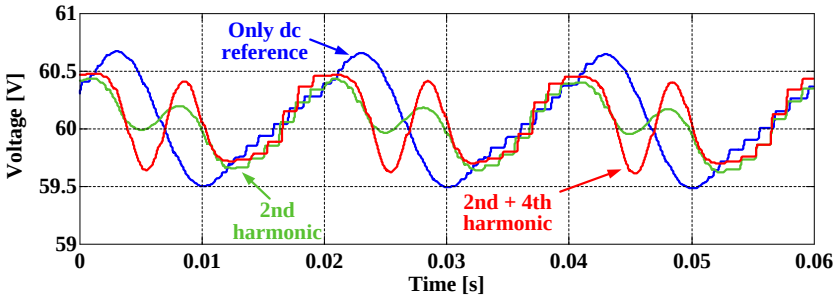


FIGURE 3.9: Simulation results. Upper arm capacitor voltages with only a dc component in the circulating current, an optimal second harmonic and a set of second and fourth harmonics with an output current phase angle of -2.6°.

After evaluating the ideal performance of the harmonics in an averaged model, simulation analysis with a switched model of the MMC have been obtained. A three-phase converter with the specifications detailed at Table 3.2 has been simulated in the MATLAB/Simulink environment.

The capacitor voltages have been obtained for three case scenarios: (i) with only a dc circulating current, (ii) with an optimal second harmonic, and (iii) with a set of optimal second and fourth harmonics. Upper arm capacitor voltages are presented for three output current phase angles: -2.6° in Fig. 3.9, -45° in Fig. 3.10 and -90° in Fig. 3.11. It can be observed that the amplitudes of the capacitor voltage ripples are reduced when the circulating current contains ac components. The reduction is slightly more significant when not only a second harmonic but also a fourth one is included in the circulating current. The switched model results agree with the expected from the average model (Fig. 3.8).

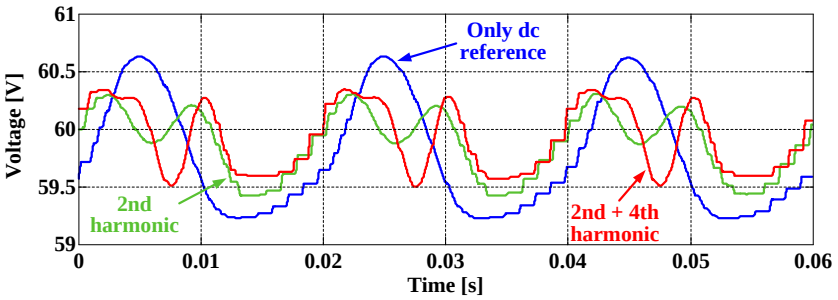


FIGURE 3.10: Simulation results. Upper arm capacitor voltages with only a dc component in the circulating current, an optimal second harmonic and a set of second and fourth harmonics with an output current phase angle of -45°.

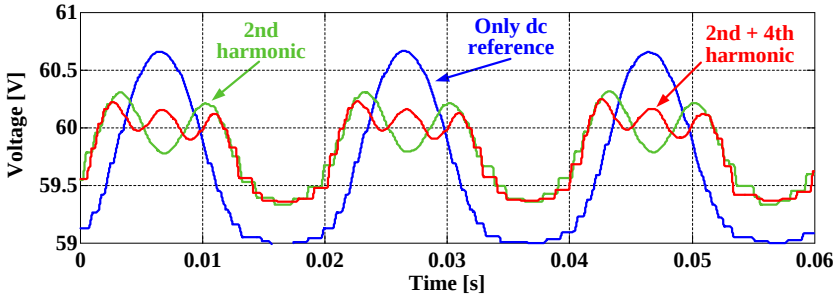


FIGURE 3.11: Simulation results. Upper arm capacitor voltages with only a dc component in the circulating current, an optimal second harmonic and a set of second and fourth harmonics with an output current phase angle of -90°.

3.3.2 Experimental Results

The performance of the optimal currents calculated with the iterative optimization technique has been validated with experimental results. The results have been obtained from the single-phase prototype from the UNSW (Subsection 2.10.2) with a resistive-inductive (RL) load. The value of the parameters used for this experimental results are given in Table 3.2. Considering the phase effect of the arm inductors L, the dc-bus capacitors C_{dc}, and the RL load, the calculated rms output current is $I_{acrms} = 3.75\,\text{A}$ with a phase angle of $\varphi = \text{-}2.6°$.

Since the prototype is a single-phase configuration, no zero-sequence will be injected into the voltage reference signal. Therefore, the same optimization results used for the simulation analysis cannot be applied to this configuration. In order to obtain experimental results from this single-phase configuration, the optimization algorithm has been adapted and new optimal values have been calculated.

Fig. 3.12 shows the experimentally measured differential and ouptut currents when the circulating current reference changes from a dc component to a dc component plus the optimal second harmonic, and finally changes to a dc current plus a set of optimal

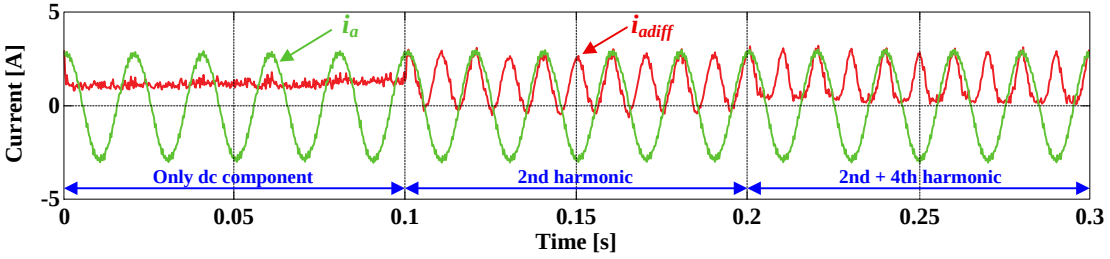


FIGURE 3.12: Experimental results. Circulating and ac-side currents when changing the circulating current reference from a dc component, to a dc plus an optimal 2nd harmonic component and to a dc plus a set of optimal 2nd and 4th harmonics.

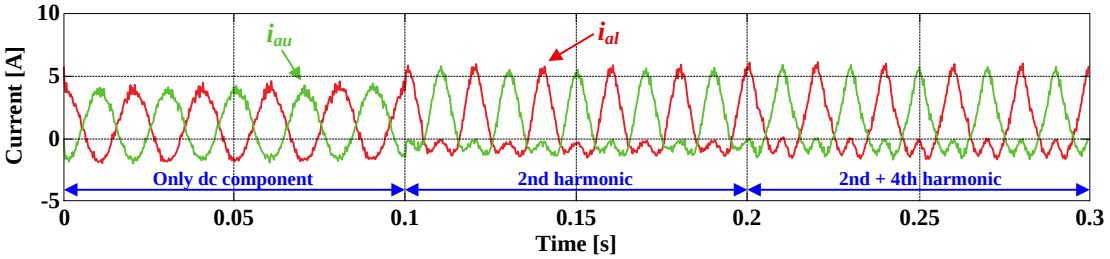


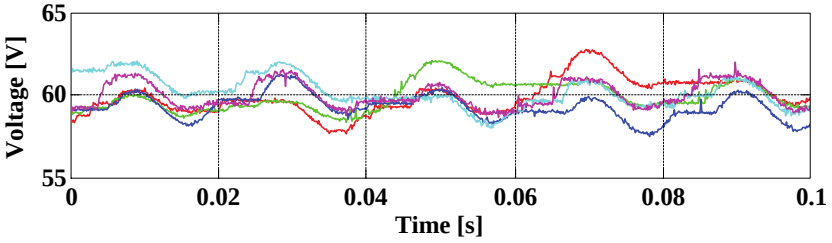
FIGURE 3.13: Experimental results. Arm currents when changing the circulating current reference from a dc component, to a dc plus an optimal 2nd harmonic component and to a dc plus a set of optimal 2nd and 4th harmonics.

second and fourth harmonic components. Fig. 3.13 shows the upper and lower arm currents in the same situations.

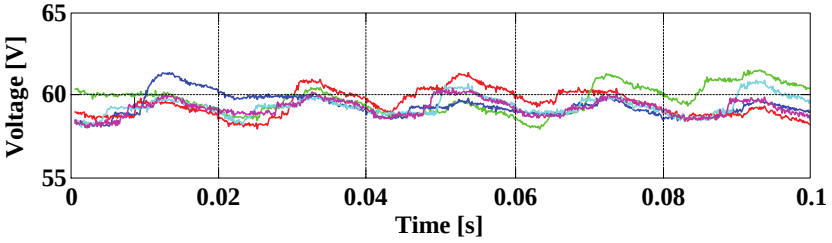
The SM capacitor voltages for the three scenarios are shown in Fig. 3.14. It can be observed that the capacitor voltage ripples are highly reduced when injecting the second harmonic component (Fig. 3.14(b)) in compariosn to when only a dc component is used as a circulating current (Fig. 3.14(a)). On the other hand, only a little difference can be appreciated in the amplitudes of the capacitor voltage ripples when comparing the case of injecting only a second harmonic (Fig. 3.14(b)), and a second plus a fourth harmonic (Fig. 3.14(c)).

3.4 Instantaneous Reference Calculation Method

The third method for calculating the circulating current reference was presented in [87] and is based on the instantaneous information of the converter. Two references are derived from a comprehensive analysis of the MMC based on the evaluation of the oscillating energy/power in the arms. The power oscillations are analysed and compared when using three circulating current references. The first reference consists on injecting only the dc component. The second one was already presented in [39], and it is the same



(a)



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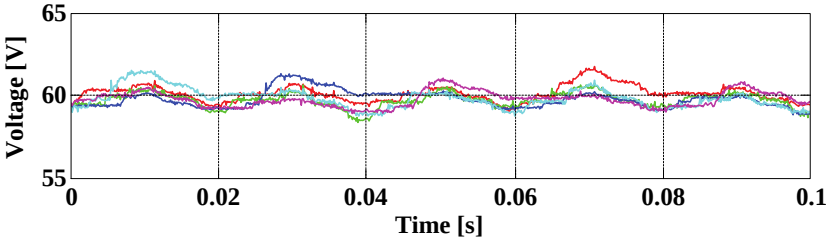


(c)

FIGURE 3.14: Experimental results. SM capacitor voltages when the circulating current reference is a dc component (a), when it is a dc component plus an optimal 2nd harmonic (b) and when it is a dc component plus a set of optimal 2nd and 4th harmonics.

one that was introduced in [43], although it was derived from a different approach. The third circulating current reference is a new approach.

The SM capacitor voltages are closely connected to the energy in the arms. Therefore, it is interesting to analyse the energy variation in the arms, which is related to the power in the arms, in order to develop a proper control for the MMC. Considering the voltage in the arms as an ac voltage v_{ac} plus a continuous offset $V_{dc}/2$, as depicted in Fig. 3.15, and neglecting the effect of the inductors, the power in the arms can be defined as:

$$p_u = \left(\frac{V_{dc}}{2} - v_{ac}\right) i_{ju} \text{ and} \tag{3.7}$$

$$p_l = -\left(\frac{V_{dc}}{2} + v_{ac}\right) i_{jl} \text{ and} \tag{3.8}$$

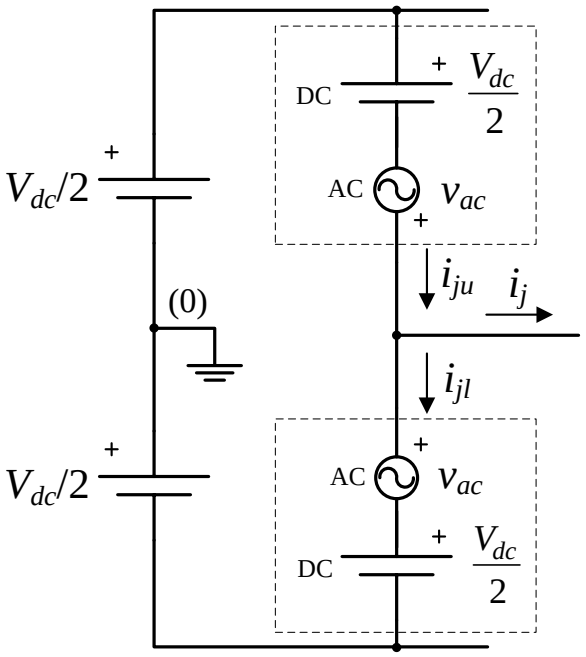


FIGURE 3.15: Circuit diagram of an MMC phase-leg with equivalent voltages.

Applying the arm currents (2.9) and (2.10), and assuming a sinusoidal output current and arm voltage:

$$i_j = I_{ac}\cos(\omega t + \varphi) \text{ and} \qquad \text{(2.37 revisited)}$$

$$v_{ac} = m\frac{V_{dc}}{2}\cos(\omega t)\ , \qquad (3.9)$$

the power in the arms becomes

$$\begin{aligned} p_u =& -\frac{mV_{dc}I_{ac}}{8}\cos(\varphi) + \frac{V_{dc}I_{ac}}{4}\cos(\omega t + \varphi) - \frac{mV_{dc}I_{ac}}{8}\cos(2\omega t + \varphi) \\ &+\frac{V_{dc}}{2}i_{jdiff} - \frac{mV_{dc}}{2}\cos(\omega t)i_{jdiff} \text{ and} \end{aligned} \qquad (3.10)$$

$$\begin{aligned} p_l =& -\frac{mV_{dc}I_{ac}}{8}\cos(\varphi) - \frac{V_{dc}I_{ac}}{4}\cos(\omega t + \varphi) - \frac{mV_{dc}I_{ac}}{8}\cos(2\omega t + \varphi) \\ &+\frac{V_{dc}}{2}i_{jdiff} + \frac{mV_{dc}}{2}\cos(\omega t)i_{jdiff}\ . \end{aligned} \qquad (3.11)$$

In steady state, no dc power component should appear in the arms; otherwise, the accumulated energy in the capacitors would increase or decrease continuously. Therefore, the differential current i_{jdiff} has to contain a dc component able to compensate for the first term in (3.10) and (3.11). The other terms show that there will be power oscillations in the arms and, consequently, voltage ripples in the capacitors.

3.4.1 DC Circulating Current

In order to reduce the power losses in the semiconductors of the MMC, some studies try to minimize the rms values of the arm currents. This can be achieved by imposing a circulating current that contains a dc component only. The dc component related with the active power transfer between dc and ac-side is:

$$i_{dc} = \frac{mI_{ac}}{4}\cos(\varphi)\ . \qquad \text{(2.40 revisited)}$$

By substituting (2.40) into (3.10) and (3.11) it is demonstrated that the dc component presented in Section 2.5.2 compensates the dc term in the power equations:

$$\begin{aligned} p_u =& \frac{V_{dc}I_{ac}}{4}\cos(\omega t+\varphi) - \frac{m^2V_{dc}I_{ac}}{8}\cos(\varphi)\cos(\omega t) \\ & -\frac{mV_{dc}I_{ac}}{8}\cos(2\omega t+\varphi) \text{ and} \end{aligned} \qquad (3.12)$$

$$\begin{aligned} p_l =& -\frac{V_{dc}I_{ac}}{4}\cos(\omega t+\varphi) + \frac{m^2V_{dc}I_{ac}}{8}\cos(\varphi)\cos(\omega t) \\ & -\frac{mV_{dc}I_{ac}}{8}\cos(2\omega t+\varphi)\ . \end{aligned} \qquad (3.13)$$

3.4.2 Determination of the Circulating Current from the Equivalent Capacitors Model

In order to cause low ripples to the capacitor voltages, the arm that inserts fewer capacitors connected in series (i.e., higher equivalent capacitance) should carry more output current. This ideal situation corresponds to the model developed in Subsection 2.2.2, hereinafter called equivalent capacitors model, which would happen naturally if the inductors L were assumed to be zero [15]. A circuit diagram of the equivalent model can be seen in Fig. 2.7. In this model, the arms are considered as equivalent capacitors C_{ju} and C_{jl}, whose value varies with the number of activated SMs (2.14) and (2.15). In this situation, the circulating current can be defined as:

$$i_{jdiff} = \frac{i_j v_{jm}}{2}\ . \qquad \text{(2.23 revisited)}$$

Considering a sinusoidal reference signal and output current, as in (3.9) and (2.37), respectively, the circulating current would be composed by only the dc component and a second harmonic component:

$$i_{jdiff} = \frac{mI_{ac}}{4}\cos(2\omega t+\varphi) + \frac{mI_{ac}}{4}\cos(\varphi)\ . \qquad \text{(2.38 revisited)}$$

Substituting (2.38) into (3.10) and (3.11), we obtain the arms power of the equivalent capacitors model:

$$\begin{aligned} p_u =& \frac{V_{dc} I_{ac}}{4} \sqrt{1 + \frac{m^2}{2}\left[\frac{m^2}{8} - 1 + (m^2 - 2)\cos^2\varphi\right]} \cdot \cos\left(\omega t + \varphi'\right) \\ & - \frac{m^2 V_{dc} I_{ac}}{16} \cos\left(3\omega t + \varphi\right) \text{ and} \end{aligned} \tag{3.14}$$

$$p_l = -p_u, \tag{3.15}$$

where

$$\varphi' = \arctan\left(\frac{\left(4 - m^2\right)\sin\varphi}{\left(4 - 3m^2\right)\cos\varphi}\right) . \tag{3.16}$$

It can be observed that when a second harmonic is used, the sum of p_u and p_l is zero; this means that there is no power and energy oscillations within the whole phase leg. The second-order power oscillations that appear in (3.12) and (3.13) are cancelled in (3.14) and (3.15). A third harmonic appears instead; however, it has smaller amplitude. Additionally, the first-order power oscillation term (ω) has lower amplitude than that in the previous case. These factors lead to a reduction in the capacitor voltage ripple amplitudes.

In order to achieve similar performance in real MMCs, the circulating current from (2.23) can be used as reference. This reference reduces the capacitor voltage ripples and can be obtained directly from the instantaneous values of the output current and the modulation signal. As a difference from previous methods, there is no need to determine the amplitude and phase of the output current. This represents a practical advantage when implemented in a real MMC as both instantaneous values are readily available to the controller.

3.4.3 Determination of the Circulating Current from the Equivalent Energy Model

A second method for determining the circulating current reference from instantaneous values has been developed. Assuming an infinite switching frequency, a new dynamic model of the converter can be obtained. In the situation of a really high switching frequency, all the SMs in a specific arm will be operated with the same duty cycle. This is equivalent to assume that all the SMs in the arm will be activated for some time to represent the activated ones (u_j and l_j), even when looking into a short time span. Therefore, all the capacitors will be charged/discharged the same because, on average, they will be exposed to the same amount of current. In other words, all N SM capacitors

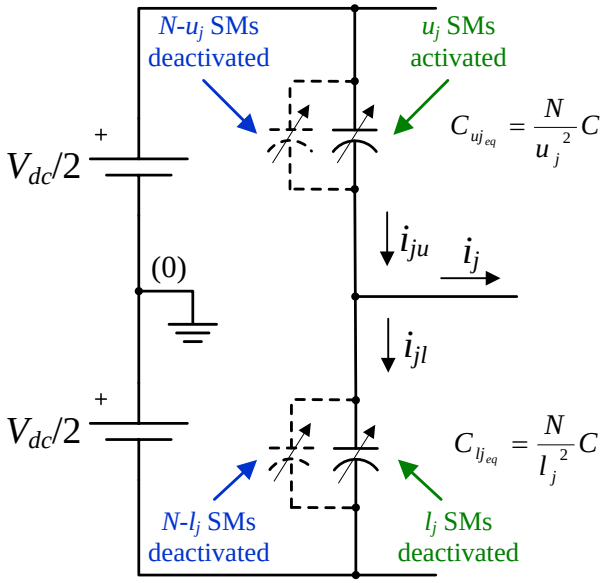


FIGURE 3.16: Equivalent model of an MMC phase-leg based on the equivalent energy model.

of each arm will evenly share the position of the activated ones within a time interval and will be charged with the same energy. The sharing of the position and charge implies that the equivalent (or averaged) capacitance of the activated SMs is bigger than C. An equivalent model of the MMC with the equivalent capacitances is depicted in Fig 3.16.

The value of the equivalent capacitor can be found from an energy point of view. Considering that all the capacitors have the same voltage, the energy variation δW_{ju} of all the SM capacitors in the upper arm within a time interval $[t_0, t_1]$ is:

$$\delta W_{Cju} = W_{Cju\,t1} - W_{Cju\,t0} = N\frac{1}{2}C\left(v^2_{Cju\,t1} - v^2_{Cju\,t0}\right) \ , \tag{3.17}$$

where $v_{Cju\,t0}$ and $v_{Cju\,t1}$ are the capacitor voltages at the time instants t_0 and t_1, respectively.

This energy variation has to be the same for the activated SMs assuming that they have an equivalent capacitance C'_{ju} instead of C as follows:

$$\delta W_{Cju} = W_{Cju\,t1} - W_{Cju\,t0} = u_j\frac{1}{2}C'_{ju}\left(v^2_{Cju\,t1} - v^2_{Cju\,t0}\right) \ . \tag{3.18}$$

From (3.17) and (3.18), the value of the equivalent SM capacitors for the upper and lower arms can be deduced as:

$$C'_{ju} = \frac{N}{u_j}C \text{ and} \tag{3.19}$$

$$C'_{jl} = \frac{N}{l_j}C \ . \tag{3.20}$$

Hence, taking into account that there are u_j and l_j activated SMs in the upper and lower arms, respectively, the values of the equivalent arm capacitors are

$$C_{ju_{eq}} = \frac{C'_{ju}}{u_j} = \frac{N}{u_j^2}C \text{ and} \tag{3.21}$$

$$C_{jl_{eq}} = \frac{C'_{jl}}{l_j} = \frac{N}{l_j^2}C \ . \tag{3.22}$$

According to Subsection 2.2.2, the correct sharing of the phase current between the upper and lower arms is given by (2.18) and (2.19). Considering the equivalent capacitors developed in this new model, the current sharing becomes:

$$i_{ju} = i_j \frac{C_{ju_{eq}}}{C_{ju_{eq}} + C_{jl_{eq}}} = i_j \frac{l_j^2}{u_j^2 + l_j^2} \text{ and} \tag{3.23}$$

$$i_{jl} = -i_j \frac{C_{jl_{eq}}}{C_{ju_{eq}} + C_{jl_{eq}}} = -i_j \frac{u_j^2}{u_j^2 + l_j^2} \ . \tag{3.24}$$

Substituting the definition of u_j and l_j from (2.16) and (2.17), respectively, into (3.23) and (3.24), the arm currents result in:

$$i_{ju} = \frac{i_j}{2} \frac{(1 + v_{jm})^2}{(1 + v_{jm}^2)} \text{ and} \tag{3.25}$$

$$i_{jl} = -\frac{i_j}{2} \frac{(1 - v_{jm})^2}{(1 + v_{jm}^2)} \ . \tag{3.26}$$

These equations provide the instantaneous references for the arm currents. Considering the definition of differential current (2.22), the resulting circulating current reference is:

$$i_{jdiff} = \frac{i_j v_{jm}}{1 + v_{jm}^2} \ . \tag{3.27}$$

Equation (3.27) provides the differential current reference obtained from the instantaneous value of the output current and the modulation signal when considering the equivalent energy model. If the modulation signal and the output current are sinusoidal, as it was assumed in (3.9) and (2.37), this current does not cancel the dc component in the power equations (3.10) and (3.11). This means that this method does not provide the proper dc value to the differential current. Nevertheless, this can be compensated by the use of an arm energy controller. On the other hand, the ac component provided by (3.27) leads to a reduction of the capacitor voltage ripples, as it will be shown in the simulation and experimental results.

3.4.4 Simulation Results

The capacitor voltage ripples and arm currents obtained with the studied references have been evaluated by simulation results. Hereinafter, the circulating current obtained from the equivalent capacitors model (2.23) is called Method 1, and the circulating current obtained from the equivalent energy model (3.27) is called Method 2. The simulation studies have been performed over the averaged model of the converter, applying the capacitor voltage equation from (2.28). Simulation results are presented with normalized variables, providing the capacitor voltage ripple results in the form of (3.5).

In order to extend the linear operation range of the MMC, a zero-sequence third-order harmonic has been introduced into the modulation signals:

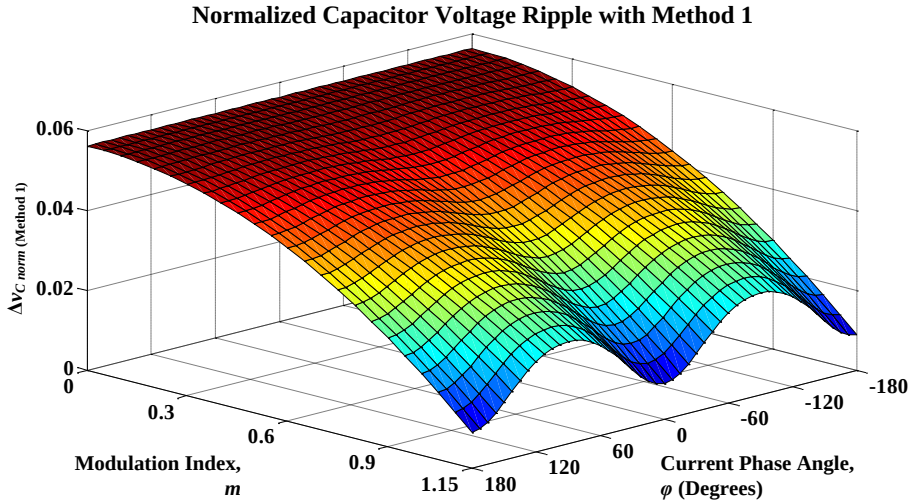
$$v_{jm} = m\cos(\omega t) - \frac{m}{6}\cos(3\omega t)\ . \tag{3.28}$$

With the use of this zero-sequence component, Method 1 still cancels the dc term in the power equations, but new harmonic components appear in the power of the arms. However, the high-frequency components are small in amplitude, and the main power oscillation is situated at the fundamental frequency (ωt). With the same modulation reference, Method 2 also introduces high frequency components, but the most significant are the low frequency ones.

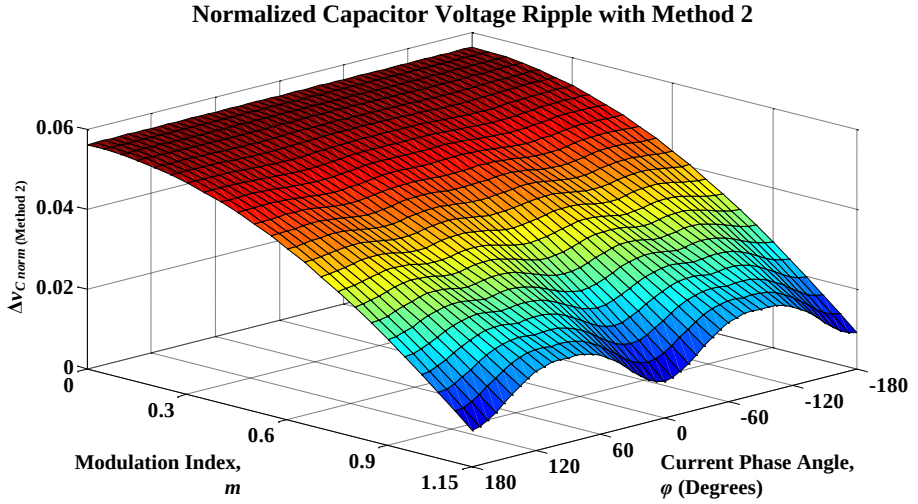
Fig. 3.17 show the normalized capacitor voltage ripples for Method 1 (a) and Method 2 (b). As it can be observed, Method 2 produces lower capacitor voltage ripples than Method 1, with the exception of some small operating areas at very large modulation indices. Fig. 3.18 show the rms value of the arm currents with both techniques. It can be seen that the rms current values produced by Method 2 (Fig. 3.18(a)) are slightly higher than those produced by Method 1 (Fig. 3.18(b)). Therefore, Method 2 slightly increases the power losses of the MMC.

In order to evaluate the circulating current references, results are benchmarked against those obtained by iterative optimization (Subsection 3.3). Results in Subsection 3.3 considered the use of a CB-SVPWM modulation, which is quite different to the use of a third harmonic. For this reason, the iterative optimization process was launched again considering the use of a third harmonic zero-sequence signal. From the two optimization cases studied in Subsection 3.3, the set of a second and fourth harmonics has been used as a benchmark.

Fig. 3.19 shows the ratio of the capacitor voltage ripples when comparing Methods 1 and 2 against the results obtained with the iterative optimization method. In both cases, the capacitor voltage ripple ratios are relatively close to the unity, which means



(a)

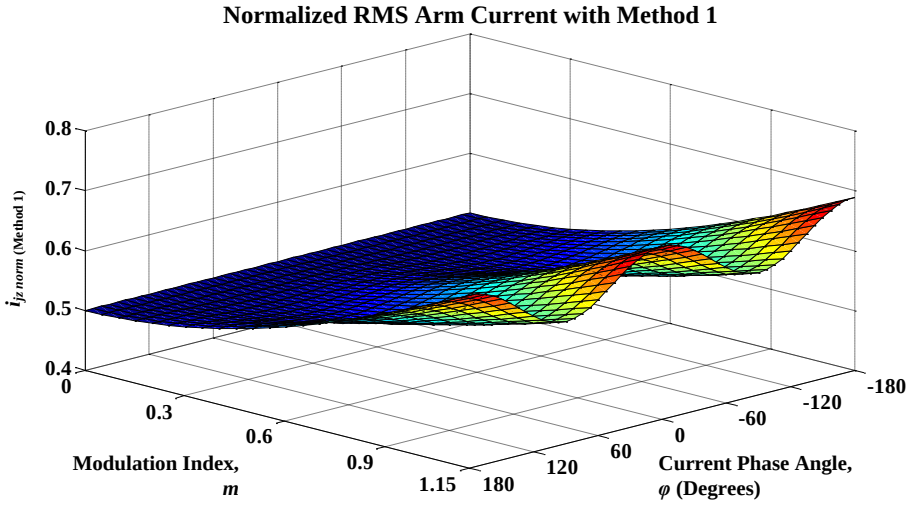


(b)

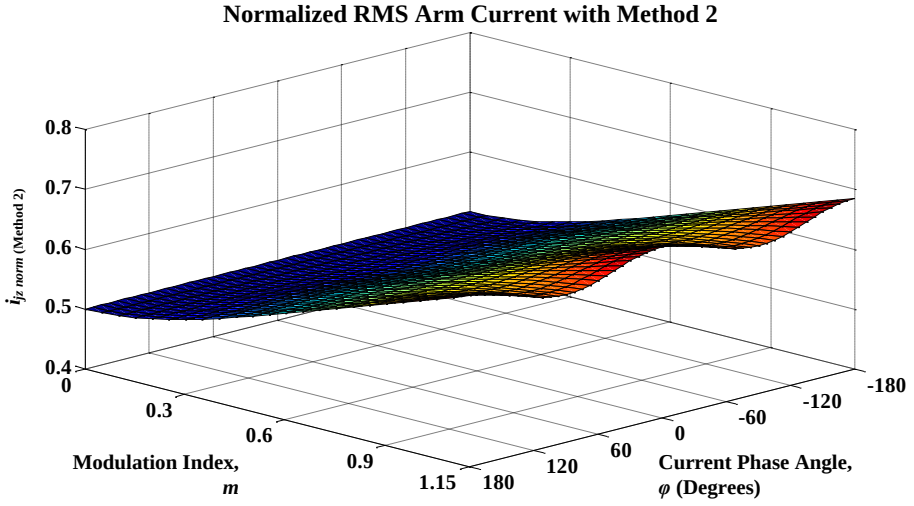
FIGURE 3.17: Normalized capacitor voltage ripples obtained with Method 1 (a) and Method 2(b).

that Methods 1 and 2 produce capacitor voltage ripples close to the optimal ones, but still higher. Fig. 3.20 shows the ratio of the rms arm current values when comparing also Methods 1 and 2 against the iterative optimization. In this case, Methods 1 and 2 produce lower values than the optimal case for all the operating conditions.

It can be concluded that Methods 1 and 2 produce capacitor voltage ripples close to the minimum ones but with lower rms arm currents. Therefore, they provide a compromise solution between reducing the capacitor voltage ripples and the power losses in the converter. It should be noted that the implementation of Methods 1 and 2, based on instantaneous values, does not require offline calculations and is significantly simpler.



(a)



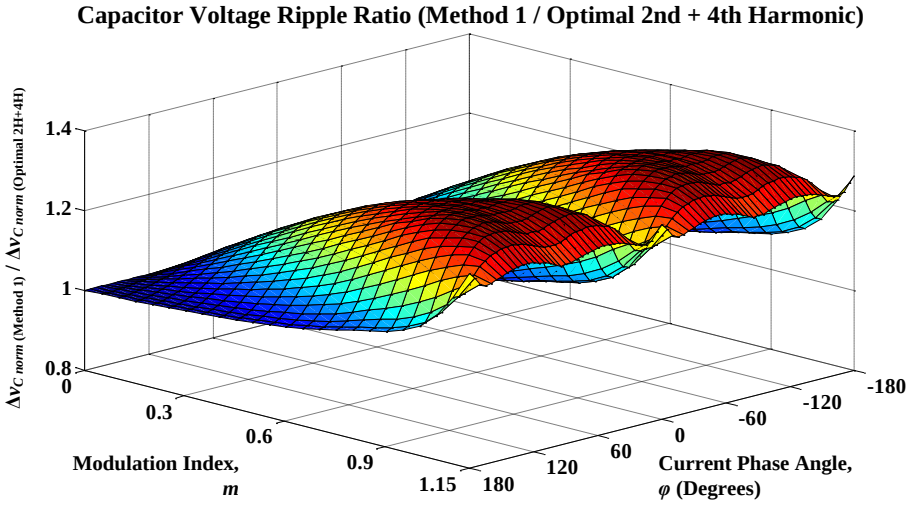
(b)

FIGURE 3.18: Normalized rms arm current obtained with Method 1 (a) and Method 2(b).

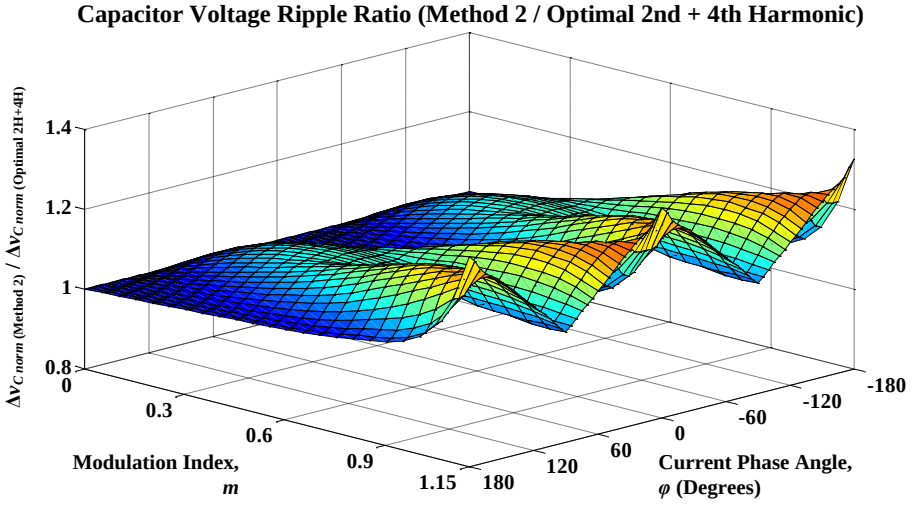
3.4.5 Experimental Results

The experimental evaluation of the proposed circulating current references has been performed in the single-phase 5-kVA prototype from the UNSW, which is composed by five SMs per arm ($N = 5$). A single-phase series-connected RL load is connected between the phase terminal and the dc-link midpoint. Since a single-phase prototype is used, the zero-sequence component from (3.28) is not used. The system parameters are given in Table 3.3.

Fig. 3.21 shows the differential current (i_{adiff}) and the output current (i_a) for the two cases under study. In Fig. 3.21(a) the circulating current obtained with Method 1 shows an important second harmonic component. In Fig. 3.21(b), where the circulating



(a)

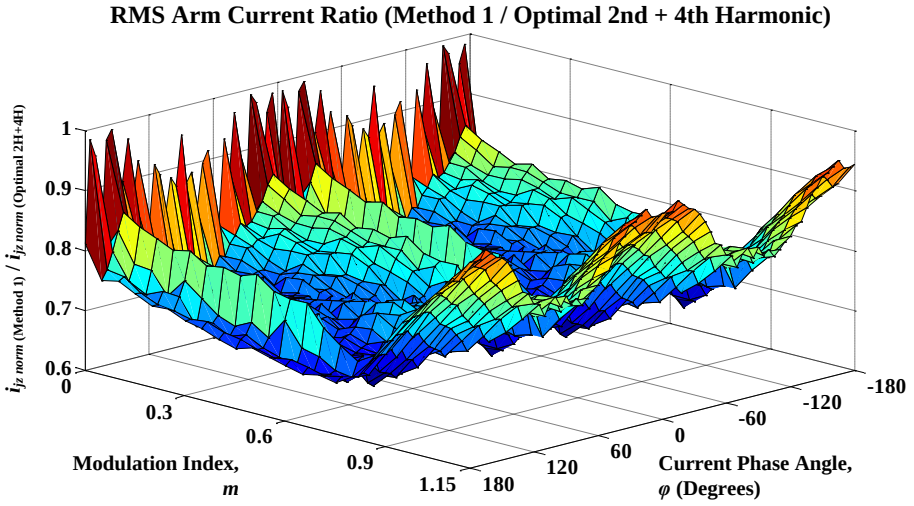


(b)

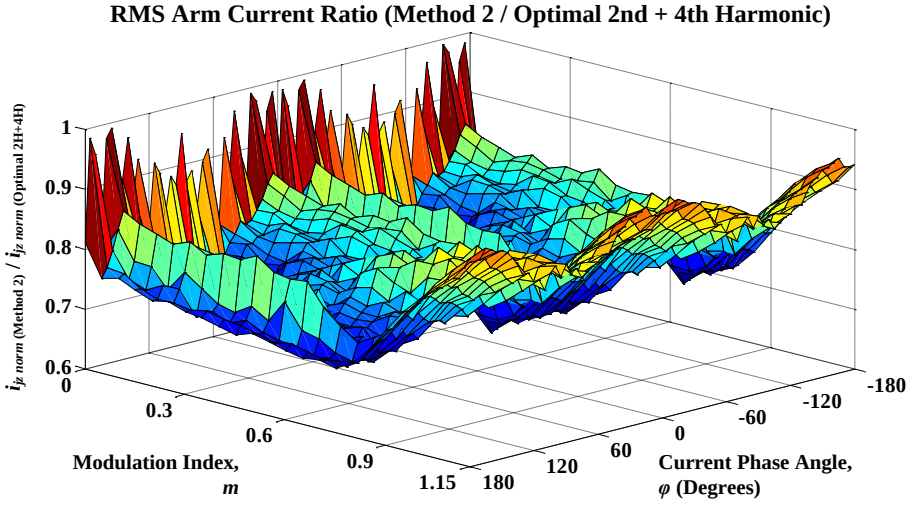
FIGURE 3.19: Ratio of the capacitor voltage ripples when benchmarked against the iterative optimization method: Method 1 (a) and Method 2 (b).

current with Method 2 is represented, additional harmonic components in the circulating current are present.

Fig. 3.22 shows the SM capacitor voltages of the upper and lower arms. These were obtained operating with only a dc component in the circulating current and with the circulating currents shown in Fig. 3.21. Comparing Fig. 3.22(a) (only a dc component) with Fig. 3.22(b) (Method 1), the capacitor voltage ripples are reduced significantly when a second harmonic is added to the differential current. Additionally, Fig. 3.22(c) shows that a further reduction in the capacitor voltage ripple amplitudes can be achieved by using Method 2. Table 3.4 summarizes the values of the ripple amplitudes for the three cases.



(a)



(b)

FIGURE 3.20: Ratio of the rms arm current when benchmarked against the iterative optimization method: Method 1 (a) and Method 2 (b).

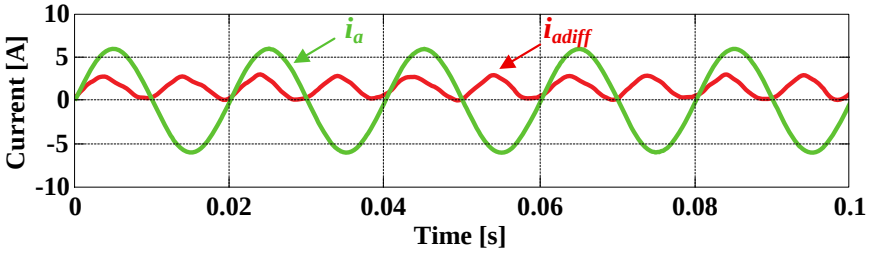
3.5 Conclusion

In this chapter, the reduction of the capacitor voltage ripples trough the circulating current is studied. The injection of selective harmonic components in the circulating current allows to reduce the capacitor voltage ripples. This salient feature is of significance for reducing the SM capacitors, which leads to the smaller footprint and reduced cost of an MMC-based system. However, those techniques increase the arm rms currents, increasing the losses of the converters. Three techniques for calculating the most effective circulating current reference have been developed.

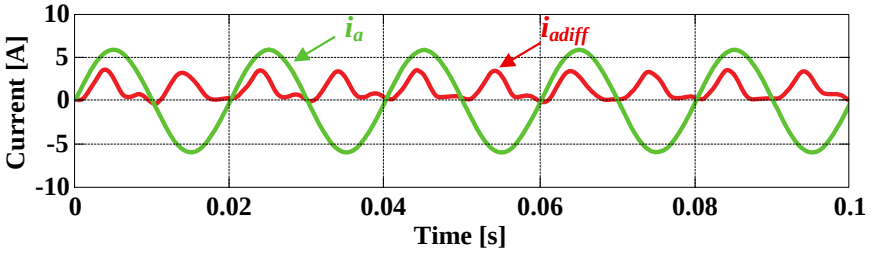
The first technique is based on the injection of a second harmonic current, which is

TABLE 3.3: Specifications of the Simulation Test Converter used for the Instantaneous Reference Techniques

Parameter	**Value**
Number of SMs per Arm, N	5
SM Capacitors, C	3600 μF
Arm Inductors, L	3.6 mH
DC-Link Voltage, V_{dc}	300 V
Modulation Index, m	0.9
Carrier Frequency, f_{cr}	4 kHz
Output Frequency, f	50 Hz
Load Resistor, R_{out}	36 Ω
Load Inductor, L_{out}	5 mH



(a)



(b)

FIGURE 3.21: Experimental results: Output and circulating current when applying Method 1 (a) and Method 2 (b).

TABLE 3.4: Capacitor Voltage Ripple Amplitudes with the Instantaneous Reference Techniques

Circulating Current	**Ripple Amplitude** $\Delta v_C/2$	**Normalized Amplitude** $\Delta v_{Cnorm}/2$
Only dc	1.30 V	0.062
Method 1	1.05 V	0.050
Method 2	0.95 V	0.046

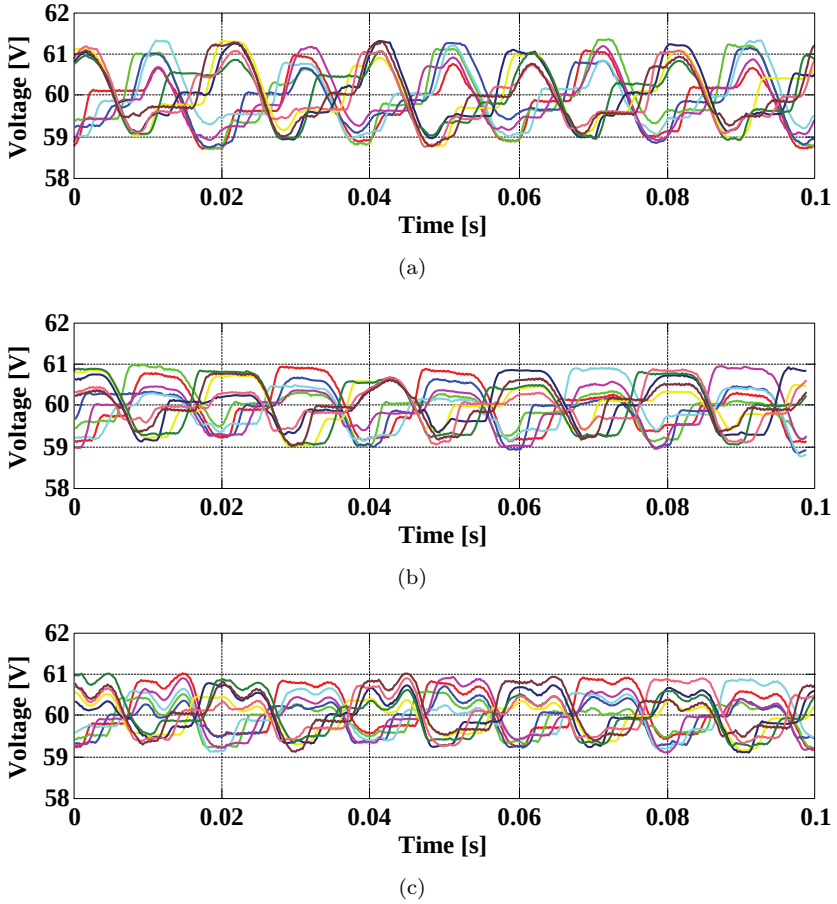


FIGURE 3.22: Experimental results: Upper and lower arm capacitor voltages when using a dc component in the circulating current (a), when using the references provided by Method 1(b) and Mehtod 2 (c).

calculated through a continuous optimization function. The optimization function used is the integral of the quadratic value of the capacitor voltages, since its reduction implies a reduction of the capacitor voltage ripples. Simulation results demonstrate that this technique reduces the amplitude of the capacitor voltage ripples for all the operation points.

The second technique calculates the harmonic components to inject with an iterative optimization method, an algorithm that evaluates all the possibilities and selects the best one. This technique requires hard-processing and has to be calculated off-line, but calculates the absolute optimal circulating current reference. The algorithm has been applied for a second and fourth harmonic components, determining its amplitude and phase at different operation points. Simulation and experimental results demonstrate that the optimal current references significantly reduces the capacitor voltage ripple amplitudes, mainly when injecting a set of second plus fourth harmonic components.

Finally, the third technique calculates the circulating current reference from equivalent models of the converter. With the objective of reducing the power fluctuations in the arms, the ideal circulating currents are calculated. Using two different equivalent models, two circulating current references are calculated from the instantaneous values of current and modulation signal. Both references are compared with optimal current calculated by iterative optimization, the second method. The capacitor voltage ripples obtained with the references calculated from instantaneous values are close to the obtained with the optimal current, but still higher. However, the instantaneous references reduce the rms value of the arm currents. A good performance of the instantaneous references and a good arrangement with the theory is demonstrated with simulation and experimental results.

Chapter 4

Discontinuous Modulation

In this chapter, a new discontinuous modulation technique is presented for the operation of the MMC. The modulation technique is based on adding a zero-sequence to the modulation signals so that the MMC arms are clamped to the upper or lower terminals of the dc-link. This technique provides a reduction in the switching power losses, since there is always a phase-leg that is not switching for some intervals. A significant reduction in the capacitor voltage ripples is also achieved, especially when operating with low modulation indices. Three versions of the discontinuous modulation are presented in this chapter. A first modulation based on a pre-defined discontinuous pattern, or open-loop technique. A second modulation based on a closed-loop, controlling the clamping intervals according to the value of the output current. And a third modulation, where virtual clampings are used for eliminating the requirement of additional SMs per arm.

4.1 Introduction

The potential of the MMC in the area of medium-voltage motor drives has already been demonstrated [110, 114]. However, there is still a challenge that has to be addressed. Using standard modulation strategies, the capacitor voltage ripples are inversely proportional to the output frequency, producing excessive capacitor voltage ripples when operating with low output frequencies, i.e., at low motor speeds.

Different solutions have been proposed, such as using a new MMC topology [115] or combining the use of a common-mode voltage and circulating current component of relatively high frequency [46, 47, 94, 116, 117]. The last method is based on compensating for the fundamental frequency arm power fluctuations, translating the dominant terms in the capacitor voltage ripples to a fixed frequency.

In this chapter, the use of a discontinuous modulation technique for the MMC is explained, which aims to reduce the switching power losses and the capacitor voltage ripples, especially at low modulation indices, operating area of low-speed motor drives. A preliminary study on the discontinuous modulation applied to the MMC was presented in [118]. The technique is based on clamping one arm of the converter to a non-switching position. This clamping effect is achieved by the addition of a zero-sequence component. The discontinuous modulation was also combined with a circulating current control, using references determined from the instantaneous magnitudes of the modulation signal and output current of each phase-leg (Sub-section 3.4). Although some interesting results were shown in [118], the reductions achieved in the capacitor voltage ripples and switching power losses were not optimized. This is because the clamping intervals of the reference signals were fixed and could not be changed. Furthermore, the implementation of zero-sequence injection based on two steps, i.e., adding a theoretical zero sequence and then correcting it because of the injection of the circulating current control signals, was not optimal and could be improved.

In [119], an improved and more efficient implementation of the discontinuous modulation technique was presented. The new implementation selects the phase-leg that needs to be clamped by using a closed-loop controller, which receives feedback from the output current. Moreover, the injected zero-sequence is defined in a single step, considering the circulating current control signals that are superimposed to the voltage reference signals. The new implementation can achieve a significant reduction in the capacitor voltage ripples for all operating conditions compared to [118]. Furthermore, the switching power losses are also reduced for most of the operating points, mainly when operating with large modulation indices, which is very interesting for grid-connected applications.

Both implementations of the discontinuous modulation require the use of additional SMs in each arm to provide control of the circulating current during the clamping intervals. This fact might not be relevant in high power applications, where a large number of SMs is required and additional SMs are usually provided anyway for reliability purposes. However, in medium-power applications of the MMC, such as motor drives, including additional SMs in the arms is usually avoided because of the significant impact on the overall cost of the converter. A benefit of this is that the MMC has less conduction power losses. Moreover, in medium-power MMCs, the use of wide band-gap semiconductor devices is being considered, particularly high-voltage silicon carbide (SiC) devices, which present a higher influence of conduction losses than switching losses [120]. For these reasons, a third approach to the discontinuous modulation, which didn't require the use of additional SMs was presented in [121]. In this implementation, instead of by-passing the arm of the clamped phase-leg with less SMs activated, the arm with the highest or

lowest modulation signal is clamped, without taking into account if it is the upper or lower arm. Since there is no requirement for increasing the number of SMs in the MMC with this approach, the conduction losses of the converter are reduced compared to the case of implementing the original discontinuous modulation [119].

4.2 Discontinuous Modulation for the MMC

Discontinuous modulation consists in the injection of a discontinuous zero-sequence signal into the references of a multiphase converter, generally a three-phase converter [122]. The zero-sequence is such that one of the phase-legs is clamped to the upper or lower terminals of the dc-link for certain intervals (Fig. 4.1). Like in the CB-SVPWM technique, the linear operation mode of the converter is increased thanks to the injection of this zero-sequence. Furthermore, since there is always one phase-leg that is not switching for some intervals, the average switching frequency of the power devices is reduced and thus the switching power losses of the converter. Multiple discontinuous modulation techniques have been studied and developed for two-level converters [49, 50] and multilevel converters [51, 52].

Discontinuous modulation can also be applied to the MMC. In this case, all the SMs of one arm of a particular phase-leg are deactivated (bypassed) for some intervals. Therefore, the phase-leg is clamped to the upper or lower dc-bus terminals. During those intervals, since one arm of the converter is not switching, the switching power losses are reduced. An example of discontinuous modulation is depicted on Fig. 4.1. The discontinuous modulation signal v_{jd} is the result from adding the zero-sequence v_{zs} to the reference signal v_{jm}:

$$v_{jd} = v_{jm} + v_{zs} \ . \tag{4.1}$$

When discontinuous modulation is applied to the MMC, only one of the arms of a particular phase-leg is clamped, whereas the other one in the same phase-leg still keeps switching for the control of the circulating current. Nevertheless, a significant reduction of the switching power losses is still achieved.

Discontinuous modulation can also provide another benefit to the MMC: a reduction in the capacitor voltage ripple amplitudes. This reduction is explained by assuming the simplified model of the MMC detailed at Subsection 2.2.2, where the arms are assumed as variable equivalent capacitors (Fig. 2.7). According to (2.18) and (2.19), the larger the equivalent capacitance is in a specific arm, the more output current goes through that arm. Therefore, the arm that has less SMs activated (larger capacitance) carries

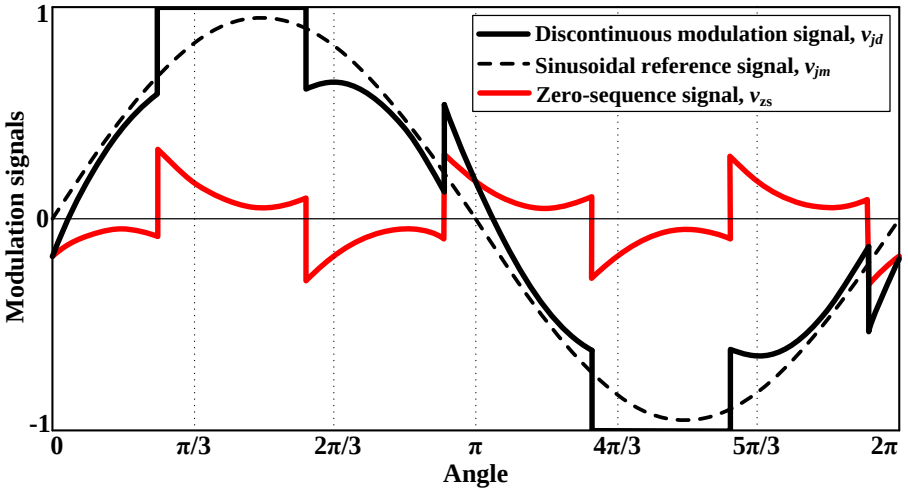


FIGURE 4.1: Example of discontinuous modulation, sinusoidal reference and zero-sequence signals.

more output current, and vice versa:

$$i_{ju} = i_j \frac{C_{ju}}{C_{ju} + C_{jl}} = i_j \frac{l_j}{u_j + l_j} \text{ and} \qquad \text{(2.18 revisited)}$$

$$i_{jl} = -i_j \frac{C_{jl}}{C_{ju} + C_{jl}} = -i_j \frac{u_j}{u_j + l_j} \, . \qquad \text{(2.19 revisited)}$$

Under this assumption, when a phase-leg of the MMC is clamped to a dc-link terminal, i.e. $u_j = 0$ or $l_j = 0$, the clamped arm presents an infinite equivalent capacitance, and no current circulates through the unclamped arm. Consequently, during the clamping process, no current will circulate through any SM capacitor of the whole phase-leg. This is a desired situation from the point of view of minimizing capacitor voltage ripples. Fig. 4.2 depicts a circuit diagram of an MMC phase-leg when clamping it to the upper and lower dc-bus terminals. In this representation, the SMs that are bypassed are shown in red colour and those that are activated are in green colour. During the clamping, the output current circulates through the arm that has all the SMs bypassed, which is indicated in blue colour in Fig. 4.2.

When operating with very low modulation indices and no zero-sequence is injected, a similar number of SMs are activated in the upper and the lower arms. In such operating conditions, the output current is equally shared between both arms of a phase-leg, flowing through N SMs and producing large deviations to the SM capacitor voltages. Under the same conditions, if discontinuous modulation is implemented, the zero-sequence will lead the reference signals of all the phases far from zero. This will reduce the capacitor voltage ripples significantly. Hence, the maximum reduction in the capacitor voltage ripples due to discontinuous modulation is expected to happen at low modulation indices.

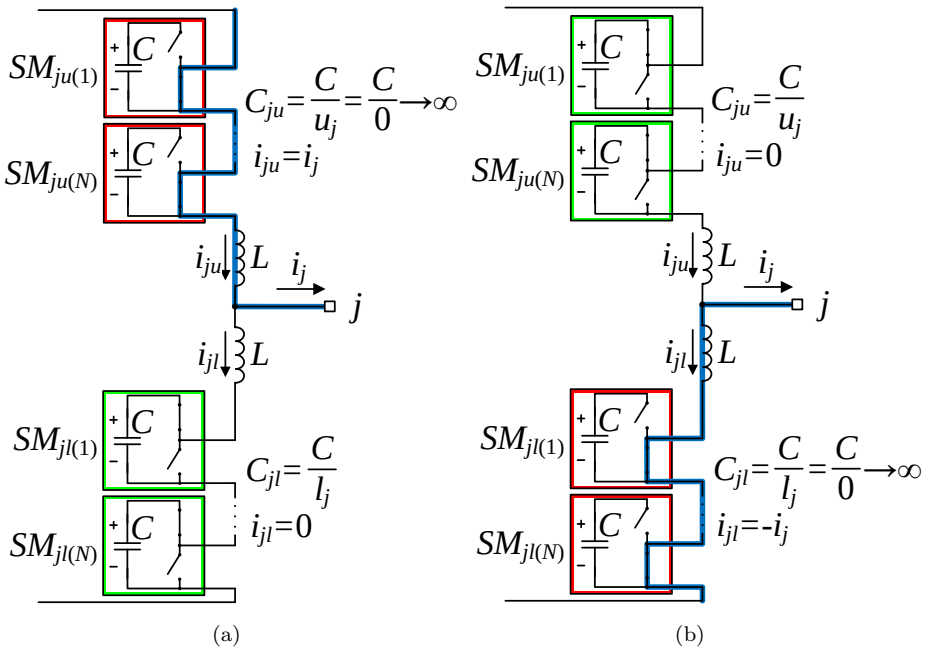


FIGURE 4.2: Circuit diagram of an MMC phase-leg when clamping to the (a) upper and (b) lower dc-bus terminals.

This reasoning has been done assuming negligible arm inductor values. However, when those inductors are considered in the arms (i.e., $L \neq 0$), the arm currents will change with respect to the desired case. Nevertheless, a performance close to the simplified model can be obtained by controlling the circulating current with the reference obtained from the equivalent capacitors model (2.23). Since in the implementation of the discontinuous modulation signal v_{jd} substitutes the original modulation signal v_{jm}, (2.23) can be re-written as:

$$i_{jdiff} = \frac{i_j v_{jd}}{2} \,. \tag{4.2}$$

4.3 Open-loop Discontinuous Modulation

The open-loop discontinuous pulse-width modulation, hereinafter abbreviated as OL-DPWM, was the first implementation of the discontinuous modulation for the MMC [118]. This technique is based on an open-loop control, using a pre-defined zero-sequence signal. The pre-defined signal is based on dividing the fundamental period is into six equal intervals, of $\pi/3$ radians each one, and clamping each phase-leg to the upper terminal of the dc-link during one interval, and to the lower terminal during another interval. The clamping intervals are centred with the maximum and minimum values of the sinusoidal reference, that is at the phase angle 0 and π of a cosinusoidal signal. An example of the pre-defined discontinuous modulation is shown at Fig. 4.3.

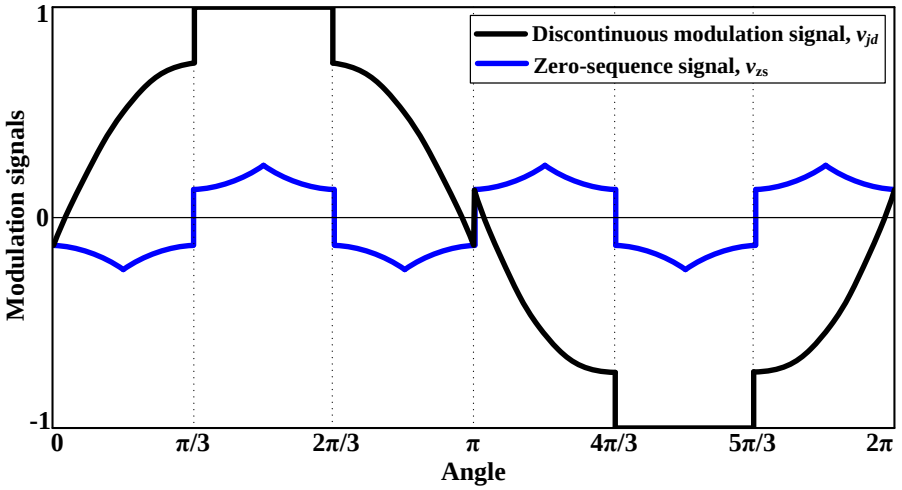


FIGURE 4.3: Example of the pre-defined discontinuous modulation, showing the zero-sequence and the resulting modulation signal.

4.3.1 Asymmetrical Circulating Current Control

The circulating current control implemented for OL-DPWM is based on the same operation principle detailed on Section 2.5.2, which is to add a positive differential control signal at the upper arm (2.41) and a negative differential control signal at the lower arm (2.42). However, the differential control signal Δv_m cannot be added to the the clamped phase-leg, since a variation in the modulation signal would unclamp the arm, switch some modules of the arm and the switching losses save would be avoided.

In order to keep the circulating current under control and maintain the arm clamping, an asymmetric control is proposed. This technique consists of leaving the clamped arm without differential control signal and applying it doubled to the opposite arm. When clamping to the upper arm with asymmetric control, the discontinuous modulation signals for the upper (v_{jud}) and lower (v_{jld}) arms become:

$$v_{jud} = v_{jd} \text{ and} \tag{4.3}$$

$$v_{jld} = v_{jd} - 2\Delta v_{jm} \ ; \tag{4.4}$$

and when clamping to the lower arm:

$$v_{jud} = v_{jd} + 2\Delta v_{jm} \text{ and} \tag{4.5}$$

$$v_{jld} = v_{jd} \ . \tag{4.6}$$

The asymmetric control is only applied to the clamped arms. This control method enables the implementation of the discontinuous modulation but causes distortion in

the phase-to-phase voltage. The distortion value can be expressed as an offset in the common voltage v_{jcomm} of the clamped phase-leg. The offset is equal in amplitude to the differential control voltage, being negative or positive when clamping the upper or lower arms, respectively:

$$v_{jcomm} = \frac{V_{dc}}{2}(v_{jd} \pm \Delta v_{jm}) \ . \tag{4.7}$$

In order to compensate the phase-to-phase distortion, an offset is added to the non-clamped phase-legs modulation signal. The value of the offset Δv_{zs} is the differential control signal of the clamped phase-leg. Its sign depends on the clamping direction:

$$\Delta v_{zs} = \pm \Delta v_{m\,clamped-phase} \ . \tag{4.8}$$

Summarizing, the final modulation signals for the non-clamped phase legs $v_{jud\,corrected}$ and $v_{jld\,corrected}$ are defined as:

$$v_{jud\,corrected} = v_{jd} + \Delta v_{jm} + \Delta v_{zs} \text{ and} \tag{4.9}$$

$$v_{jld\,corrected} = v_{jd} - \Delta v_{jm} + \Delta v_{zs} \ . \tag{4.10}$$

An example of the voltage provided by the arms and the differential voltage during a clamping with asymmetric control is shown in Fig. 4.4. It can be seen that while the voltage provided by the clamped arm is zero, the opposite arm controls the circulating current.

4.3.2 Additional SMs per Arm

If the differential control signal Δv_{jm} is positive, the upper arm reference signal is larger than the lower arm reference signal of the same phase-leg. Therefore, when clamping one arm to the upper or lower terminals of the dc-link, the reference of the opposite arm remains within the modulation limits [1,-1]. However, if the differential control signal is negative ($\Delta v_{jm} < 0$), the resulting modulating signal of the opposite arm will be higher than 1 or lower than -1, producing overmodulation and losing control of the circulating current.

In order to increase the modulation range, additional SMs are used in the arms. The additional SMs allow the arms to provide higher voltages, which correspond to modulation signals higher than 1 for the lower arms and lower than -1 for the upper arms. The addition of M SMs to the N basic ones increases the cost of the MMC, but provides further benefits to the converter.

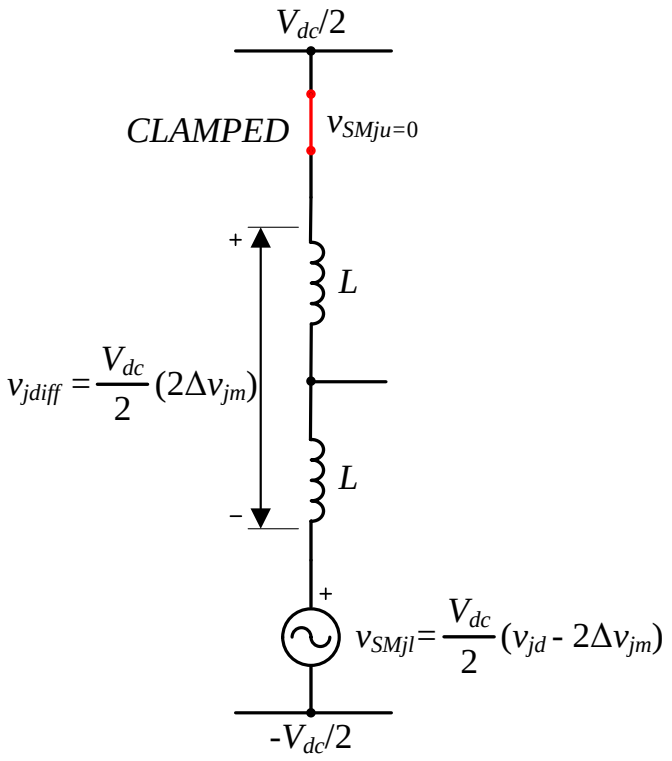


FIGURE 4.4: Arms and differential voltages during a clamping with asymmetric control.

The main benefit of using additional SMs is fault tolerance capability, since we are using redundant components. In this thesis the technique of active redundant SMs is used [64,123], which gives the same consideration to all the SMs, but in normal operation the maximum number of SMs activated in each arm is N out of the $N+M$ available. This technique provides the extra benefit of reducing the capacitor voltage ripples because the energy fluctuations in the phase-legs is distributed within more SMs.

4.3.3 Simulation Results

The performance of an MMC operating with the open-loop discontinuous modulation (OL-DPWM) has been evaluated with MATLAB/Simulink simulation studies. The simulation studies have been performed with a switched model of the MMC, analysing and comparing the capacitor voltage ripples and power losses obtained with OL-DPWM and CB-SVPWM. Both modulation techniques are implemented with a voltage balancing algorithm without reduced switching frequency [9]. The simulated plant consists on a 5-MW MMC with ten basic SMs per arm (N=10) plus one additional SM (M=1). The specifications of this test converter are given in Table 4.1.

TABLE 4.1: Specifications of the Simulation Test Converter Used for OL-DPWM

Parameter	**Value**
Number of Basic SMs per Arm, N	10
Number of Additional SMs per Arm, M	1
SM Capacitors, C	5600 μF
Arm Inductors, L	1.8 mH
DC-Link Voltage, V_{dc}	10 kV
AC-side rms Current, $I_{ac\,rms}$	500 A
Carrier Frequency, f_{cr}	5 kHz
Output Frequency, f	50 Hz

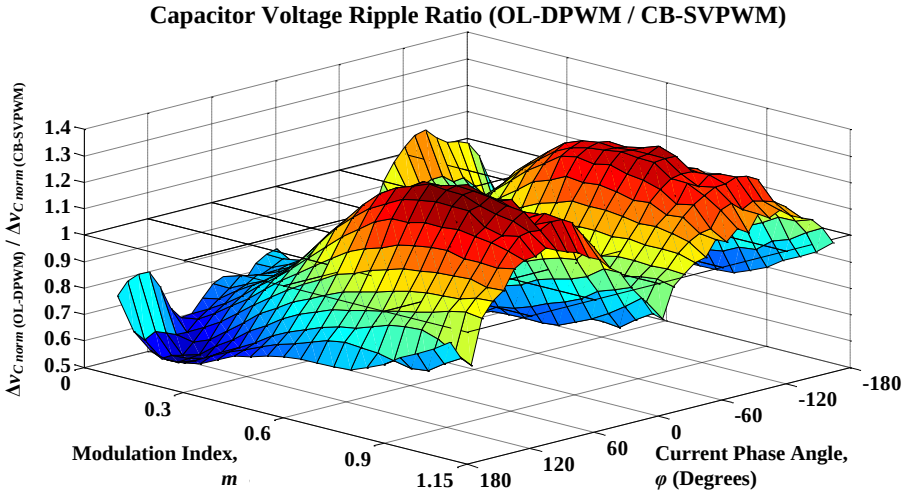


FIGURE 4.5: Ratio of the capacitor voltage ripple amplitudes (OL-DPWM over CB-SVPWM).

Simulation results have been obtained for different operating points, where m refers to the modulation index before the injection of a zero-sequence (defined from 0 to 1.15 p.u.), and φ corresponds to the output current phase angle in degrees [-180°, 180°].

Fig. 4.5 depicts the ratio of capacitor voltage ripple amplitudes between OL-DPWM and CB-SVPWM. As expected, the ripples ratio is lower than the unity for low modulation indices, which means that discontinuous modulation reduces the capacitor voltage ripples. Such a reduction is very significant (about 30-50%) for modulation indices below 0.2. This facilitates the use of the MMC for motor drive applications, where the MMC has to operate with low modulation indices for low frequencies/speeds. For higher modulation indices and active currents, the capacitor voltage ripples are still lower with OL-DPWM, but for highly reactive currents, the capacitor voltage ripples reach values of 30% higher than with CB-SVPWM.

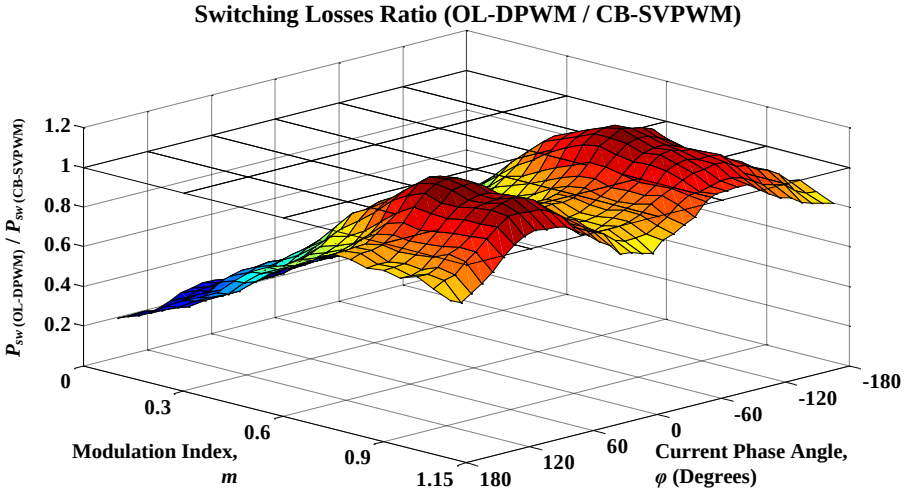


FIGURE 4.6: Switching power losses: ratio between OL-DPWM and CB-SVPWM.

In order to evaluate the power losses of the converter, the losses of a particular IGBT have been modelled. The IGBT considered is the module DIM1200NSM17-E000, which allows a maximum forward current of 1200 A and a maximum direct voltage of 1700 V. The simulation model calculates the switching and conduction losses separately, using the dynamic and static characteristics of the IGBT obtained from the datasheet. The equations used for power losses calculation are detailed in Section 7.2.

Fig. 4.6 shows the switching power losses (P_{sw}) ratio between using OL-DPWM and CB-SVPWM. It can be seen that the switching losses ratio decreases with the modulation index, reaching a minimum ratio of 20% at $m = 0.05$. For this reason, it can be stated that OL-DPWM reduces the switching losses for almost all the operating points, with the exception of high modulation indices (above 0.7) and highly reactive currents.

Fig. 4.7 shows the conduction power losses (P_{cond}) ratio. In this case, unlike in the switching power losses, OL-DPWM increases the losses for almost all the operating points. Nevertheless, since in this example the conduction losses are significantly less than the switching losses (switching losses range from 20 kW to 80 kW and conduction losses range from 15 kW to 25 kW), the total power losses (P_{tot}) ratio between both modulation techniques (Fig. 4.8) remains very similar to the switching losses ratio, i.e. losses with OL-DPWM are generally smaller than with CB-SVPWM.

4.4 Closed-loop Discontinuous Modulation

In order to reduce the capacitor voltage ripples and the power losses of the MMC further, the clamping intervals of the discontinuous modulation can be variable and defined

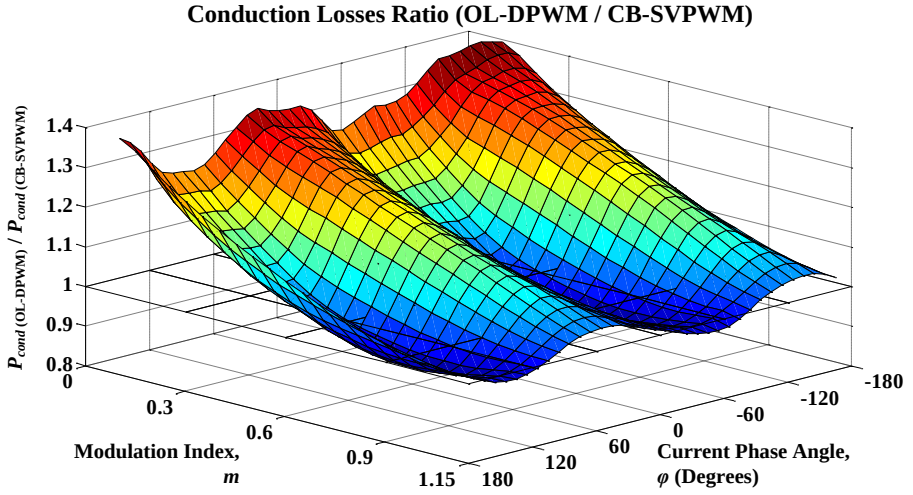


FIGURE 4.7: Conduction power losses: ratio between OL-DPWM and CB-SVPWM.

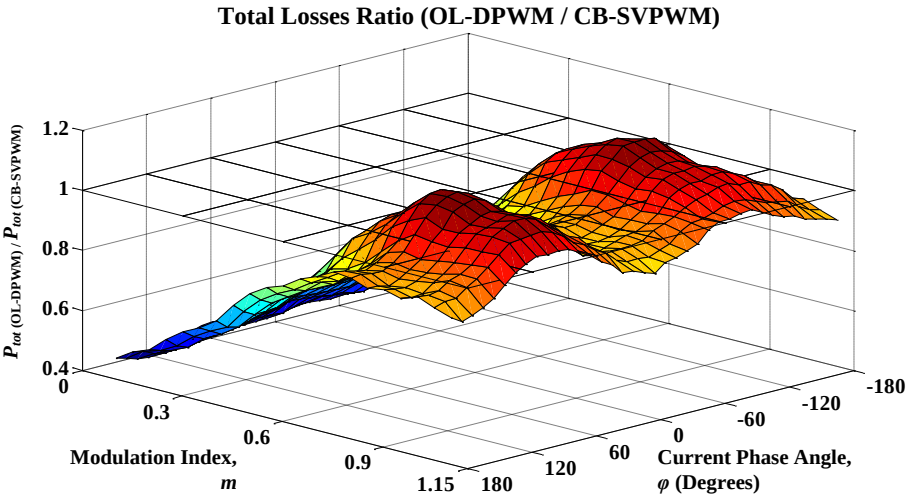


FIGURE 4.8: Total power losses: ratio between OL-DPWM and CB-SVPWM.

trough a closed loop. In the clamped arm, no current circulates through the SM capacitors and hence no capacitor voltage ripple is produced. Therefore, it is desirable to clamp the phase-leg that carries more output current (in absolute value) whenever it is possible.

At any time, only one out of two possible phase-legs of a multiphase system is clamped. The two phase-legs that can be clamped are the one with the highest reference signal v_{jm}, which can be clamped to the upper dc-link terminal ($v_{jd}=1$), and the phase-leg with the lowest modulation signal, which can be clamped to the lower terminal ($v_{jd}=-1$). If the phase-leg with the maximum current (absolute value) is one of the phase-legs suitable to be clamped, it is clamped. In contrast, if the phase-leg with the maximum current is the one that cannot be clamped because it corresponds to neither the maximum nor the minimum reference signals, the phase-leg with the second highest current is the one that is clamped. An example of the application of this clamping

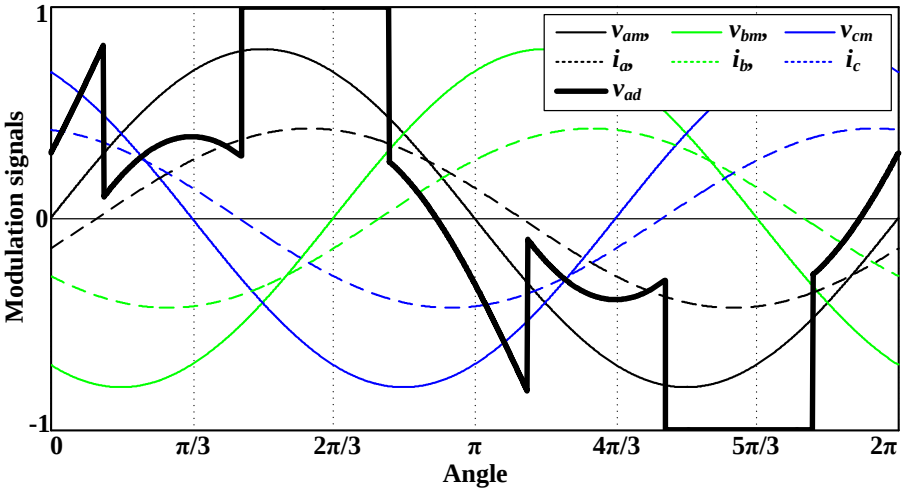


FIGURE 4.9: Example of CL-DPWM where the clamping intervals are defined by the maximum value of the output current.

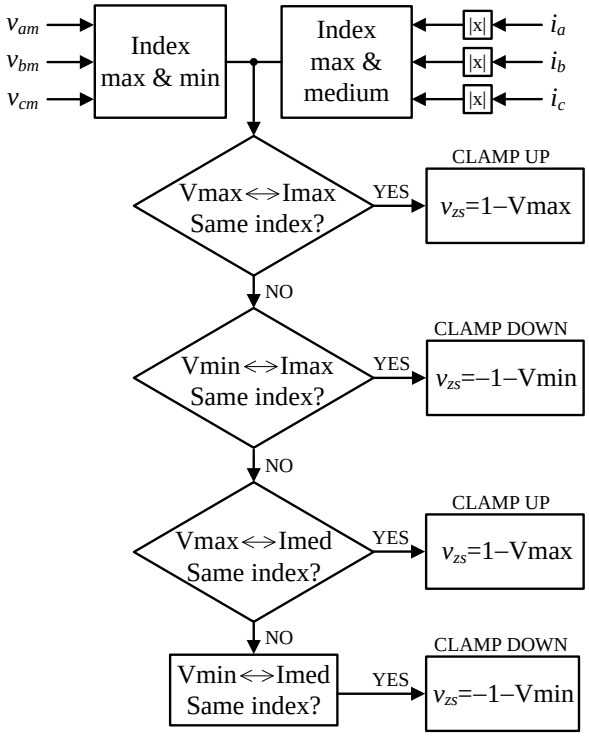


FIGURE 4.10: Block diagram of the discontinuous zero-sequence algorithm.

criterion is presented in Fig. 4.9. This figure shows the original reference signals (v_{am}, v_{bm} and v_{cm}), the p.u. output currents (i_a, i_b and i_c) and the final reference signal for phase a (v_{ad}). It can be observed that the clamping intervals of v_{ad} coincide with the peaks of the current i_a. A block diagram of the algorithm that determines the zero-sequence signal according to the explained criteria is depicted in Fig. 4.10.

Unlike OL-DPWM, the proposed technique, called closed-loop discontinuous pulse-width modulation (CL-DPWM), adapts the clamping interval to the output current

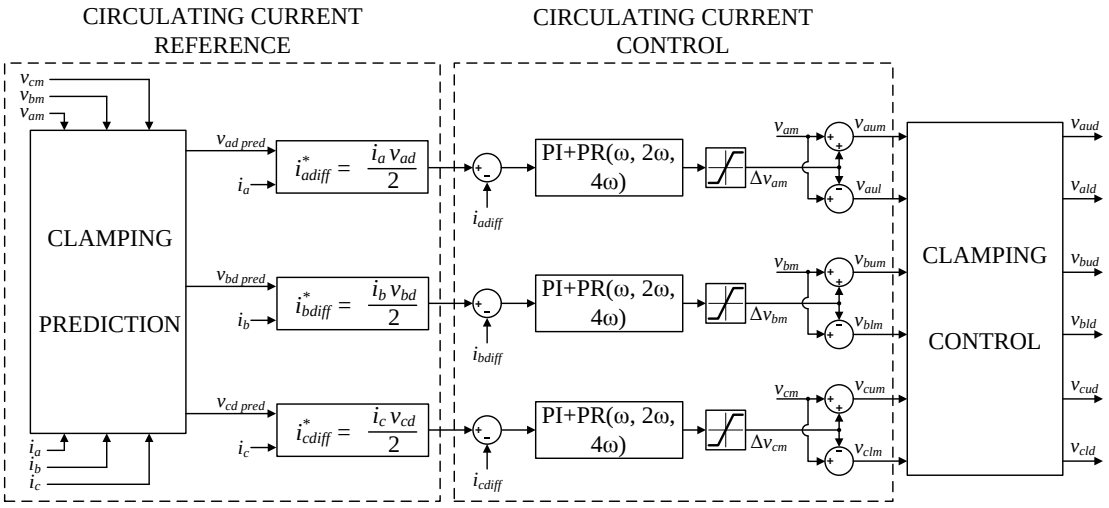


FIGURE 4.11: Block diagram of the control system: circulating current reference calculation, circulating current controller and clamping controller.

phase angle. This fact reduces the capacitor voltage ripples significantly, since the largest or second largest output current in absolute value flows through an arm with no activated SMs. It also reduces the switching power losses of the MMC.

4.4.1 Control Structure

CL-DPWM control strategy is based on two main control loops, which are mutually coupled. The first one is the circulating current control, which calculates the differential control signal Δv_{jm} and the arm modulation references v_{jum} and v_{jlm}. The second loop calculates the zero-sequence, using the output currents and the six arm modulation references as an input. The two loops can be considered coupled because the reference of the circulating current is calculated from the zero-sequence signal. The control structure can be divided into three stages: (i) calculation of the circulating current reference, (ii) circulating current controller and (iii) clamping controller. A block diagram of the control system is depicted in Fig. 4.11.

In the first stage, the circulating current reference (4.2) is calculated. It should be calculated from the discontinuous modulation signal (v_{jd}), which includes the discontinuous zero-sequence. However, the discontinuous zero-sequence is determined and applied in a subsequent control. To solve this algebraic loop, a prediction of the zero-sequence is performed. This prediction consists on applying the CL-DPWM over the original modulation signals, without including the differential control signals for the control of the circulating currents. Since these last control signals are relatively small, no significant deviations will be produced due to the use of the predicted zero-sequence, and hence, the circulating current reference would be very close to the desired one.

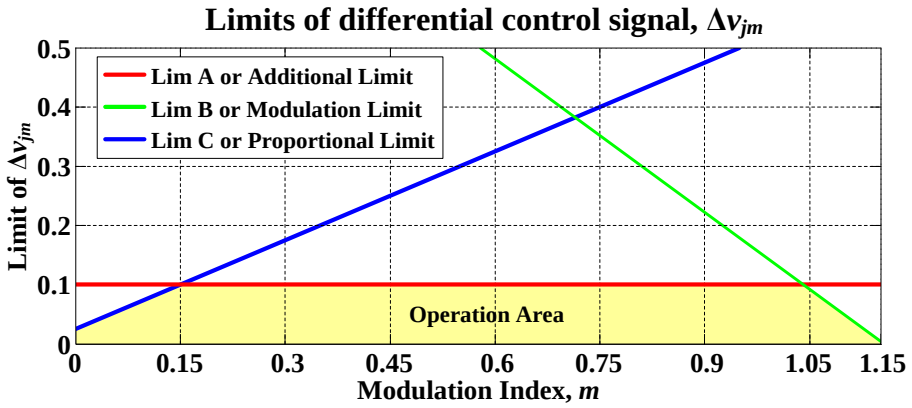


FIGURE 4.12: Example of the limits of the differential control signal.

In the second stage, the circulating current is controlled. Since the current reference contains a dc term as well as some harmonics, a set of PR controllers can be included in addition to a PI controller [39]. Each one of the resonant controllers is tuned at the main frequency components of the circulating current reference, i.e., ω, 2ω and 4ω.

The differential control signal Δv_{jm}, obtained from the circulating current controller, is added and subtracted to the reference modulation signal (v_{jm}) of the phase-leg, obtaining the independent voltage reference for each of the arms of a phase-leg (v_{jum} and v_{jlm}). As in OL-DPWM, a negative differential control signal causes overmodulation in the opposite arm to the clamped one. For this reason, the use of M additional SMs is required.

Finally, the clamping control is applied to the arm reference signals and the zero-sequence calculated. The six reference signals of the MMC (one per arm) are considered for the clamping. The maximum reference signal of the upper arms defines the arm that can be potentially clamped to the upper dc-terminal, while the minimum reference signal of the lower arms defines the arm that can be potentially clamped to the lower dc-terminal.

4.4.2 Limits of the Differential Control Signal

Excessive values of the differential control signals can deteriorate the MMC performance due to overmodulation or undesired clamping conditions. This is why the differential voltage signals are limited. Fig. 4.12 shows an example of the limits of the differential control signal. The three criteria used to define the limits are explained next.

The first limiting criterion is used to avoid overmodulation in the clamped phase-leg (*lim A* or additional limit). The use of M additional SMs allows overpassing the nominal modulation limits in the clamped phase-leg, but only for a limited range. This range

corresponds to M additional carriers located beyond the interval [-1,1]:

$$v_{jm\,lim\,A} = 1 + M\,A_{cr}\ , \tag{4.11}$$

where A_{cr} is the amplitude of the carriers (2.30). The difference between the upper and the lower arm modulation signals is twice the differential control signal, since it is added to the upper arm and subtracted to the lower arm. Therefore, the limit of the differential control signal when one of the arms is clamped (v_{jm}=1) is:

$$\Delta v_{jm\,lim\,A} = \frac{M\,A_{cr}}{2} = \frac{M}{N}\ . \tag{4.12}$$

The second limiting criterion, *lim B* or modulation limit, prevents overmodulation in the non-clamped phase-legs. This overmodulation can appear when the modified modulation signal (v_{jum} or v_{jlm}) for the clamped arm is higher than 1 or lower than -1. In this situation, the discontinuous zero-sequence is negative when clamping up (positive when clamping down) approaching the opposite sign phases to the modulation limit. It can be demonstrated that for a purely sinusoidal three-phase system with no injection of the differential control signal, no overmodulation appears for modulation indices below $2/\sqrt{3}$ (≈ 1.1547). However, when adding the differential control signal, the modulation index limit depends on this control signal.

The premise for avoiding this overmodulation is ensuring that the lowest margin of the non-clamped phase-legs is bigger or equal to the discontinuous zero-sequence (difference between the clamped arm and 1 or -1). Considering the case of clamping in the upper arm, the premise can be expressed as:

$$v_{jzm\,min} + 1 \geq v_{jzm\,max} - 1\ , \tag{4.13}$$

where $z \in \{u, l\}$ is the upper or lower arm identifier.

For example, assuming three sinusoidal reference signals, and considering that v_{aum} is the maximum signal and v_{clm} is the minimum signal, (4.13) can be rewritten as:

$$m \sin\left(\omega t + \frac{2\pi}{3}\right) - \Delta v_{a\,lim\,B} + 1 \geq m \sin\left(\omega t\right) + \Delta v_{a\,lim\,B} - 1\ . \tag{4.14}$$

In this example, the worst situation is produced at $\omega t = 2\pi/3$, where

$$\Delta v_{a\,lim\,B} \leq 1 - m\frac{\sqrt{3}}{2}\ . \tag{4.15}$$

The same result is obtained when the inequation (4.15) is solved for the other phase combinations.

The third limiting criterion, *lim C* or proportional limit, aims for avoiding an excessive modification of the modulation signals at low modulation indices. It is considered that the applied clamping interval is similar to the predicted one, but this is only accomplished if the differential control signal is significantly smaller than the modulation signal. Without this limit, the clamping intervals applied at low modulation indices may be very different from the predicted ones, modifying the circulating current and thus increasing power losses and capacitor voltage ripples.

The limit is proportional to the modulation index with a gain of K_{lim}, except for the addition an offset component O_{lim}, which allows the control of the circulating current at modulation indices close to zero:

$$\Delta v_{j\ lim\ C} = O_{lim} + K_{lim}\ m\ . \tag{4.16}$$

The values of the parameters O_{lim} and K_{lim} should be adapted to the particularities of each converter. In the simulations of the next section, these parameters have been adjusted as $O_{lim}=0.025$ and $K_{lim}=0.5$. Therefore, (4.16) becomes:

$$\Delta v_{j\ lim\ C} = 0.025 + 0.5\ m\ . \tag{4.17}$$

The differential control signal limit is implemented by calculating all the limitation criteria at each modulation index value and using the most restrictive. An example of these three limits is shown in Fig. 4.12, where the shaded zone represents the operation area defined by the most restrictive limit.

4.4.3 Simulation Results

The proposed modulation and control techniques have been simulated under MATLAB/Simulink environment. The simulation studies have been developed using two different models: an averaged model to evaluate the capacitor voltage ripples and a switched model to estimate the power losses. In both models, the results obtained with CL-DPWM, are compared to the results obtained with CB-SVPWM. Results are presented for different operating points, where m is the modulation index before the injection of a zero-sequence (defined from 0 to 1.15 p.u.), and φ corresponds to the output current phase angle in degrees [-180°, 180°].

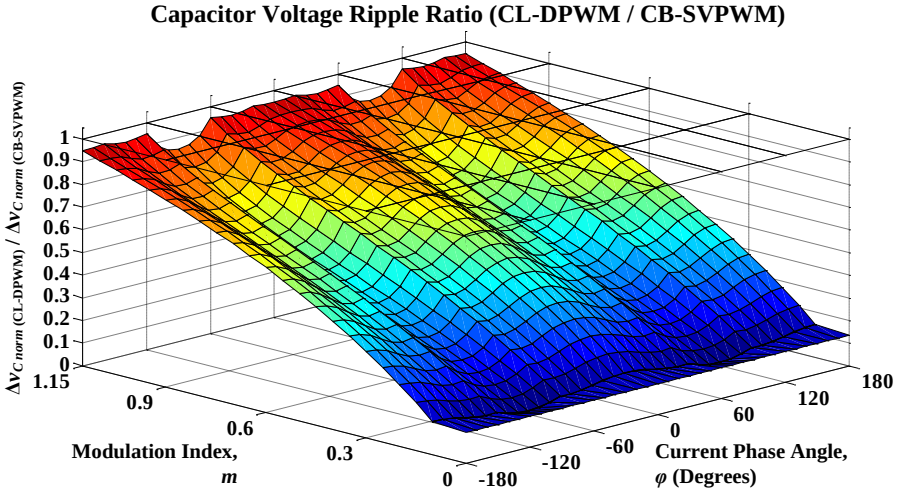


FIGURE 4.13: Ratio of the capacitor voltage ripple amplitudes (CL-DPWM over CB-SVPWM).

The capacitor voltage ripples have been studied with an averaged model of the MMC, that is, applying the capacitor voltage equations given in (2.28) and (2.29), and considering that the arm currents are a half of the output current plus the circulating current reference (4.2). Although a circulating current controller has to be implemented to impose the circulating current, the differential control signal is assumed to be very small so that it does not affect the predicted discontinuous modulation. Therefore, the results obtained are independent of the parameters of the controller and some parameters of the MMC, such as the arm inductor and the dc-link voltage.

Fig. 4.13 depicts the ratio of capacitor voltage ripple amplitudes between CL-DPWM and CB-SVPWM. It can be observed that this ratio is lower than the unity for all operation conditions, which means that CL-DPWM produces smaller capacitor voltage ripple amplitudes than CB-SVPWM. The reduction increases when the modulation index decreases, ranging from about 5% reduction with large modulation indices to about 90% reduction for low modulation indices. The capacitor voltage ripples are also smaller than in OL-DPWM, which does not reduce the capacitor voltage ripples for all operating points.

Fig. 4.13 also shows an interesting effect that appears in phase angles from -120° to -60° and from 60° to 120°, where a higher reduction of the capacitor voltage ripples is produced. The reason for this is that, under these operating conditions, each arm is clamped twice per period instead of once, i.e., a specific arm is clamped for a period of time when the absolute value of the phase current is the maximum, and it is clamped again when the output current has the second highest value (absolute values). The fact of clamping twice produces a better distribution of the charging and discharging capacitor currents, reducing the peak-to-peak variation of the capacitor voltages.

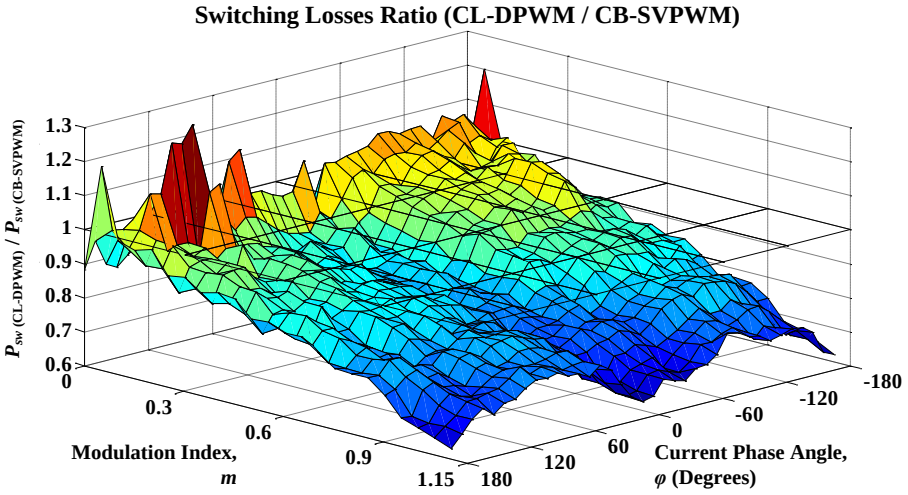


FIGURE 4.14: Switching power losses: ratio between CL-DPWM and CB-SVPWM.

These results suggest the suitability of this technique for motor drive applications. When a motor drive operates with low speed, the frequency and modulation index are low as well. Significant reductions of the capacitor voltage ripples are achieved for low modulation indices with CL-DPWM.

CL-DPWM has also been implemented in the same switched simulation model of the MMC used for the OL-DPWM. However, in this case a reduced switching frequency voltage balancing algorithm [91] has been implemented. The model has been used to calculate the power losses of a 5-MW converter with ten basic SMs per arm ($N = 10$) plus an additional one ($M = 1$). The losses are evaluated considering the use of the IGBT module DIM1200NSM17-E000, whose maximum ratings are a forward current of 1200 A and a direct voltage of 1700 V. Further characteristics of the MMC model are detailed in Table 4.1.

Fig. 4.14 shows the switching losses ratio obtained when comparing the CL-DPWM with CB-SVPWM. Unlike the capacitor voltage ripples, the ratio of the switching losses reduces when increasing the the modulation index, reaching a minimum ratio of 65% at large modulation indices. However, CL-DPWM causes higher switching losses than CB-SVPWM at very low modulation indices. This is because the savings achieved with the clamping of CL-DPWM do no compensate for the increase of losses produced by the large transitions needed for clamping the arms under such conditions. This drawback is acceptable when considering the significant reduction in the capacitor voltage ripples achieved under low modulation indices. Fig. 4.14 also shows the effect of the double clamping for phase angles from -120° to -60° and from 60° to 120°, where the additional clamping transitions produce further switching losses to the MMC.

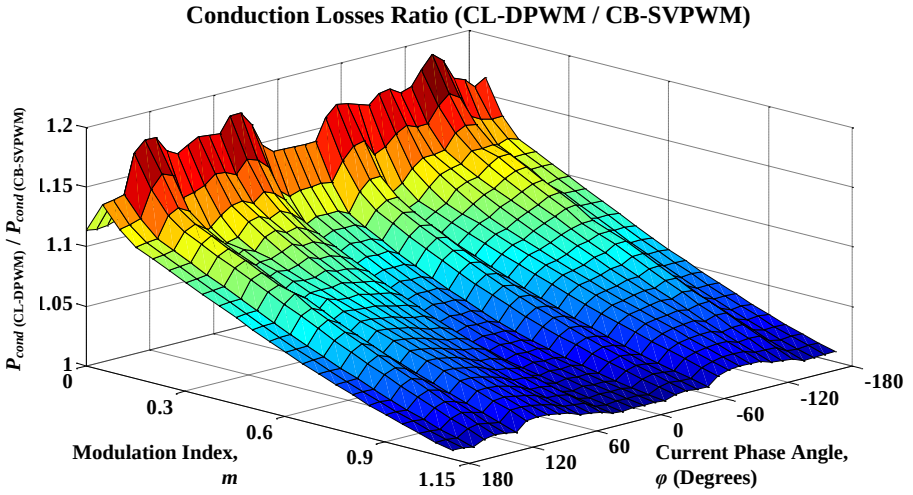


FIGURE 4.15: Conduction power losses: ratio between CL-DPWM and CB-SVPWM.

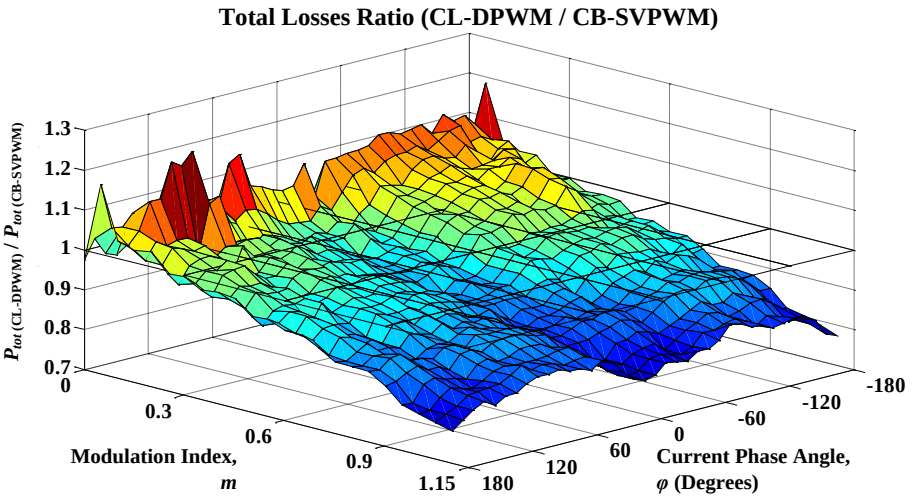


FIGURE 4.16: Total power losses: ratio between CL-DPWM and CB-SVPWM.

The conduction losses ratio is depicted in Fig. 4.15. In this case, CL-DPWM causes higher conduction losses in all the operating points because the rms value of the arm currents is bigger than with CB-SVPWM, mainly for highly reactive currents. Nevertheless, the conduction losses change within a low variation range (from 6.2 kW to 7.2 kW) when compared to the switching losses variation range (from 5.9 kW to 11.7 kW). Therefore, the total power losses ratio, presented in Fig. 4.16, is similar to the switching power losses ratio with an offset. Fig. 4.16 also shows that CL-DPWM reduces the total power losses for modulation indices larger than $m = 0.3$.

The reduction of power losses for high modulation indices makes this technique also suitable for grid-connected MMCs. However, in some transient situations where low modulation indices are needed, such as grid voltage sags, a switching-mode system between different modulation schemes can be used for avoiding the increase of power losses at low modulation indices.

TABLE 4.2: Specifications of the Laboratory Prototype for CL-DPWM

Parameter	**Value**
Number of Basic SMs per Arm, N	4
Number of Additional SMs per Arm, M	1
SM Capacitors, C	3.6 mF
Arm Inductors, L	3.6 mH
DC-Link Voltage, V_{dc}	160 V
Carrier Frequency MMC, $f_{cr\,MMC}$	2 kHz
Carrier Frequency Two-Level Leg, $f_{cr\,2L}$	10 kHz
Output Frequency, f	50 Hz
Load 1 (Resistive-Inductive)	$R_{out} = 22\,\Omega$, $L_{out} = 5$ mH
Load 2 (Inductive)	$R_{out} = 0\,\Omega$, $L_{out} = 50$ mH

4.4.4 Experimental Results

CL-DPWM has been implemented and tested in the single-phase prototype from the UNSW (Subsection 2.10.2), which is composed of five SMs per arm ($N = 4$, $M = 1$). The main data of the prototype are given in Table 4.2. This MMC prototype is based on a single phase-leg with an RL load. In order to be able to inject a zero-sequence into the reference signal of the phase-leg without distorting the output current, the load is connected between the output of the MMC phase-leg and a voltage generator that emulates the neutral-point voltage of an equivalent three-phase Wye-connected load. The generator of the neutral-point voltage consists of a two-level half-bridge inverter that shares the same dc bus with the MMC phase-leg. A block diagram of the experimental setup is depicted in Fig. 4.17.

Figs. 4.18 and 4.19 present experimental results operating with a modulation index $m = 0.95$. In Fig. 4.18, the MMC operates with CB-SVPWM, while in Fig. 4.19 CL-DPWM is applied to the converter. Fig. 4.19(a) shows the reference signal of CL-DPWM. One can observe that the intervals where the reference signal is clamped are lagging the peak of the reference signal. This is because the inductive component of the load makes the output current lag with respect to the voltage applied. Thus, the intervals where the reference signal is clamped coincide with the peaks of the output current. Comparing Fig. 4.18(c) with Fig. 4.19(d), one can observe that CL-DPWM can achieve a reduction in the capacitor voltage ripples of about 10%, which matches more or less what is expected according to Fig. 4.13.

In Figs. 4.20 and 4.21 the MMC operates with a modulation index $m = 0.45$. The converter operates with CB-SVPWM in Fig. 4.20 while CL-DPWM is applied in

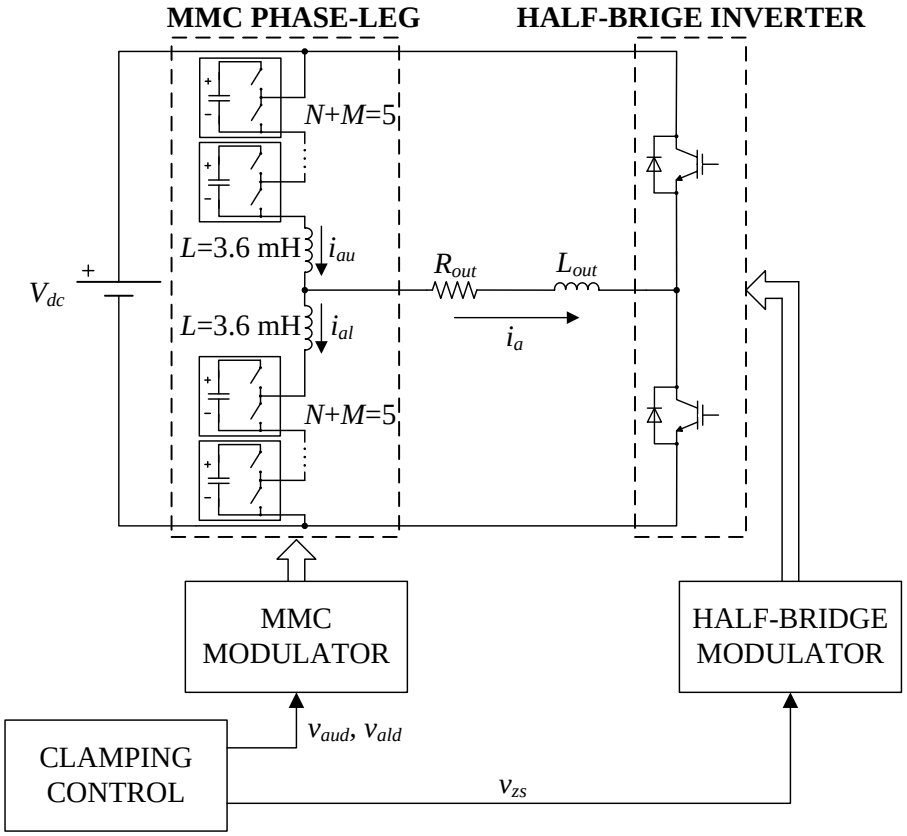


FIGURE 4.17: Block diagram of the laboratory setup.

Fig. 4.21. Comparing Fig. 4.20(c) with Fig. 4.21(d), it can be observed that CL-DPWM is able to reduce the capacitor voltage ripples by about 35%. In this case, a larger reduction was expected according to Fig. 4.13 (about 48%). One of the reasons for this difference is that the differential control signal was not considered in the averaged model used for obtaining Fig. 4.13. In any case, a significant reduction in the capacitor voltage ripples is achieved in all the cases tested when CL-DPWM is applied.

In Fig. 4.19(c) and Fig. 4.21(c), which correspond to the output currents obtained with CL-DPWM, some additional distortion can be observed. To evaluate this, the total harmonic distortion (THD) has been calculated for the output currents, using the first 40 harmonic components measured with a Teledyne LeCroy HD 4096 oscilloscope. The THD values are given in the figures of the output currents (Fig. 4.18(b), Fig. 4.19(c), Fig. 4.20(b) and Fig. 4.21(c)), and are also summarized in Table 4.3. From these values, one can conclude that such additional distortion produced with CL-DPWM is relatively small.

As it can be observed in Figs. 4.19(b) and 4.21(b), during the intervals in which a particular arm is clamped, the current of the other arm of that phase-leg is close to zero. As a consequence, the capacitor voltages of the unclamped arm will be practically

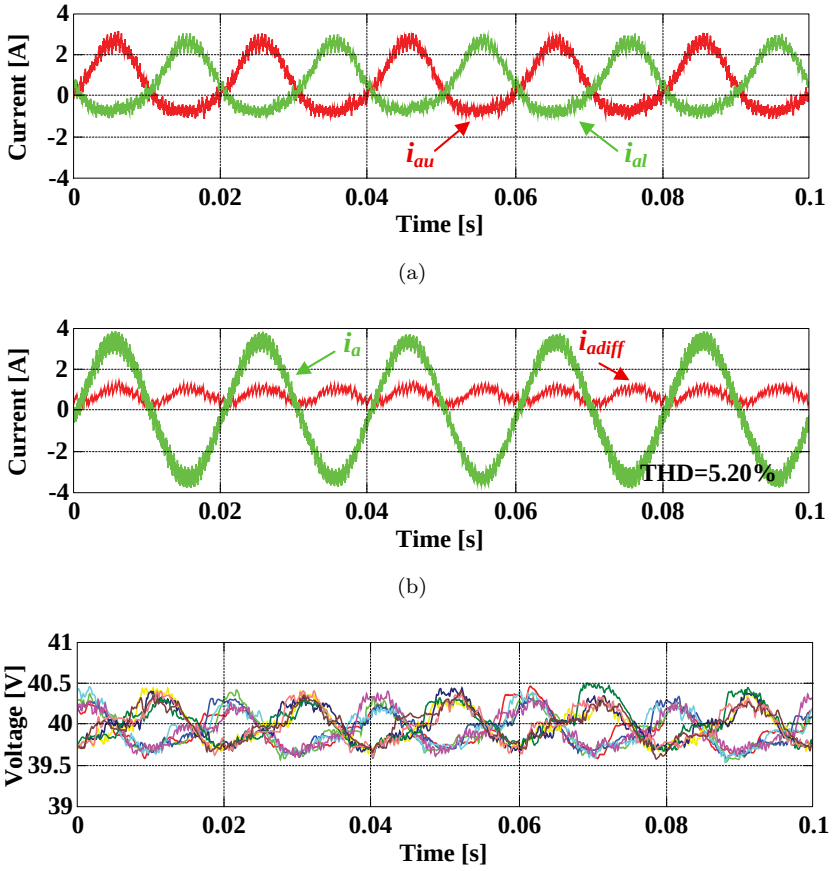


FIGURE 4.18: Experimental results of CB-SVPWM operating with a resistive-inductive load (Load 1) and $m = 0.95$: (a) arm currents, (b) output current and differential current, and (c) capacitor voltages.

TABLE 4.3: Output Current THD (%) with CL-DPWM and CB-SVPWM

	$m = 0.95$	$m = 0.45$
CB-SVPWM	5.20	11.91
CL-DPWM	5.41	12.85

constant. Since the capacitor voltages of the clamped arm are also constant (no current circulates through them because the SMs are bypassed) all the capacitor voltages of the phase-leg tend to be constant during the clamping intervals, as it can be appreciated in Figs. 4.19(d) and 4.21(d).

In order to produce double clamping with the CL-DPWM strategy, Fig. 4.22 shows experimental results operating with a purely inductive load (Load 2: $R_{out} = 0\,\Omega$, $L_{out} = 50\,\text{mH}$). As discussed previously, the double clamping reduces the capacitor voltage ripples further.

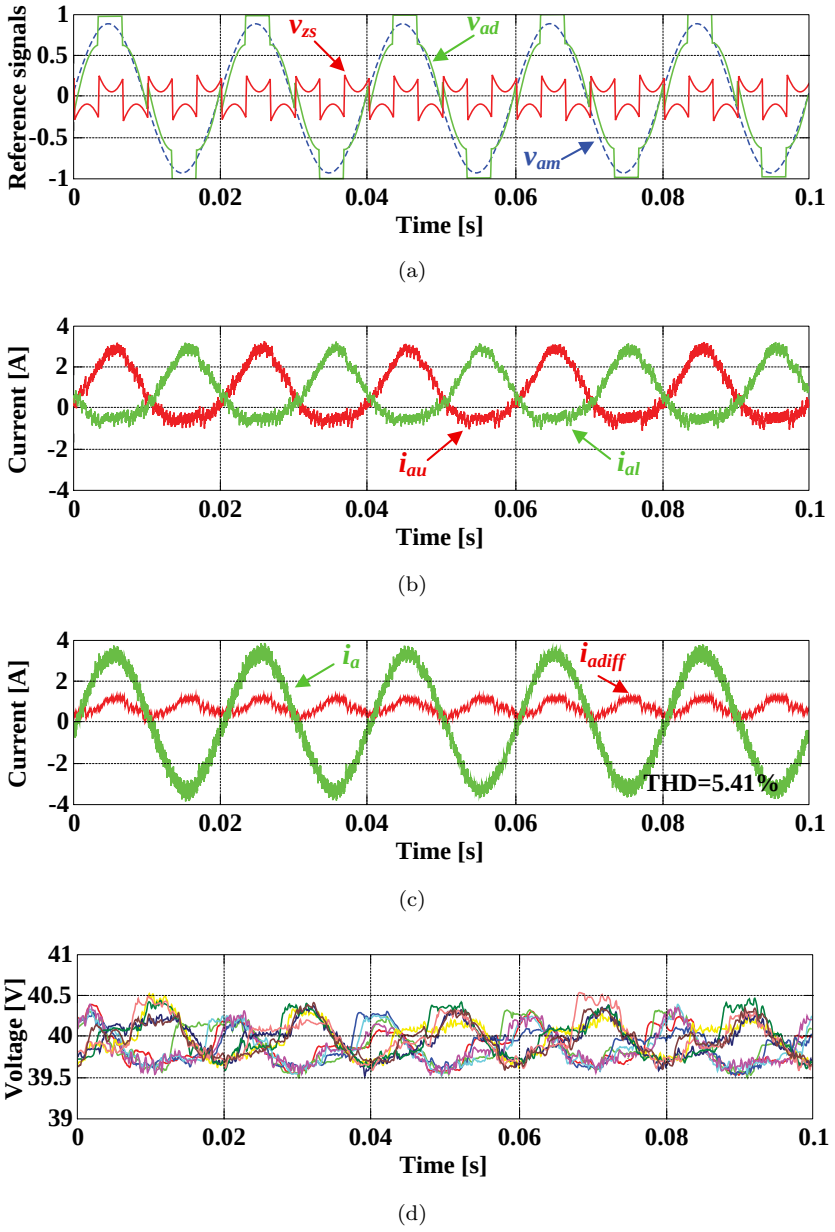


FIGURE 4.19: Experimental results of CL-DPWM operating with a resistive-inductive load (Load 1) and $m = 0.95$: (a) reference signal, (b) arm currents, (c) output and circulating currents, and (d) capacitor voltages.

4.5 Medium-Voltage Application of Discontinuous Modulation

A third approach to discontinuous modulation has been presented in [121]. The technique called virtual discontinuous pulse-width modulation (VDPWM) implements a clamping algorithm that eliminates the requirement of additional SMs in the arms. This technique can be very useful for medium-power applications, where the use of additional SMs in the arms has a significant impact on the cost of the converter. Moreover, the

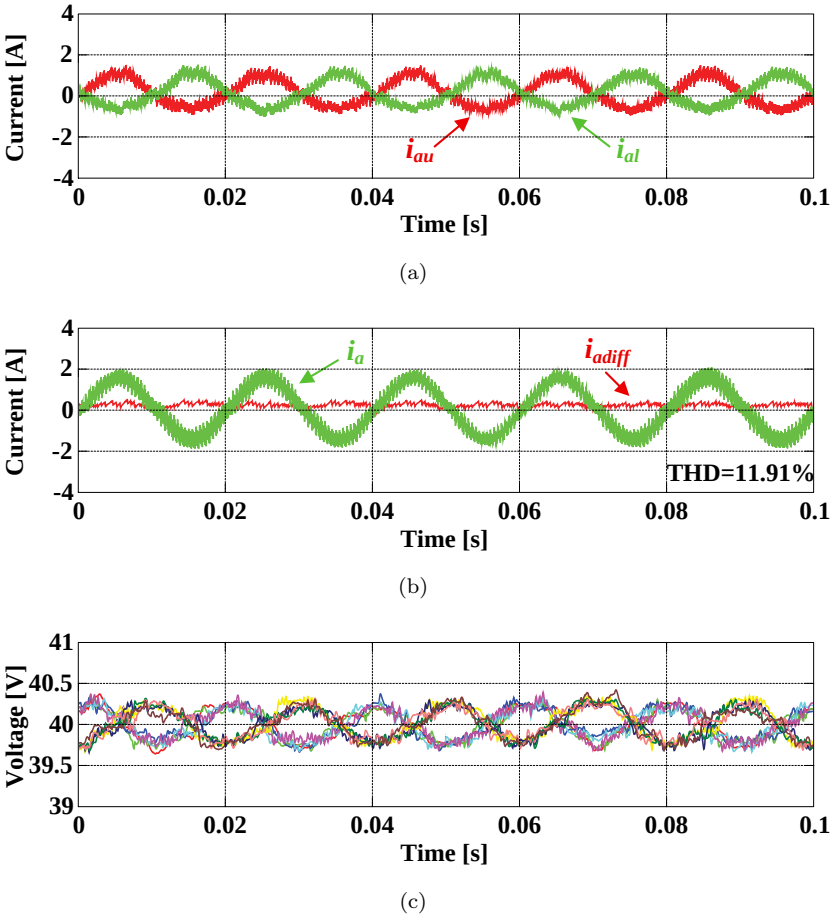


FIGURE 4.20: Experimental results of CB-SVPWM operating with a resistive-inductive load (Load 1) and $m = 0.45$: (a) arm currents, (b) output current and differential current, and (c) capacitor voltages.

conduction losses are reduced, since the arm current flows through a lower number of switching devices. This reduction is specially significant if wide band-gap semiconductor devices are used, like silicon carbide (SiC) ones, where the conduction losses represent an important part of the total power losses.

4.5.1 Virtual Clamping Concept

In both OL-DPWM and CL-DPWM, the use of additional SMs provides the capability of controlling the circulating current of a clamped phase-leg. However, if the clamping methodology is modified when the differential control signal is negative, the requirement for additional SMs is avoided.

CL-DPWM always clamps the upper arm to the upper rail of the dc-link and the lower arm to the lower rail of the dc-link. In contrast, VDPWM considers that an arm is clamped not only when all the SMs are deactivated (bypassed), but also when all of them

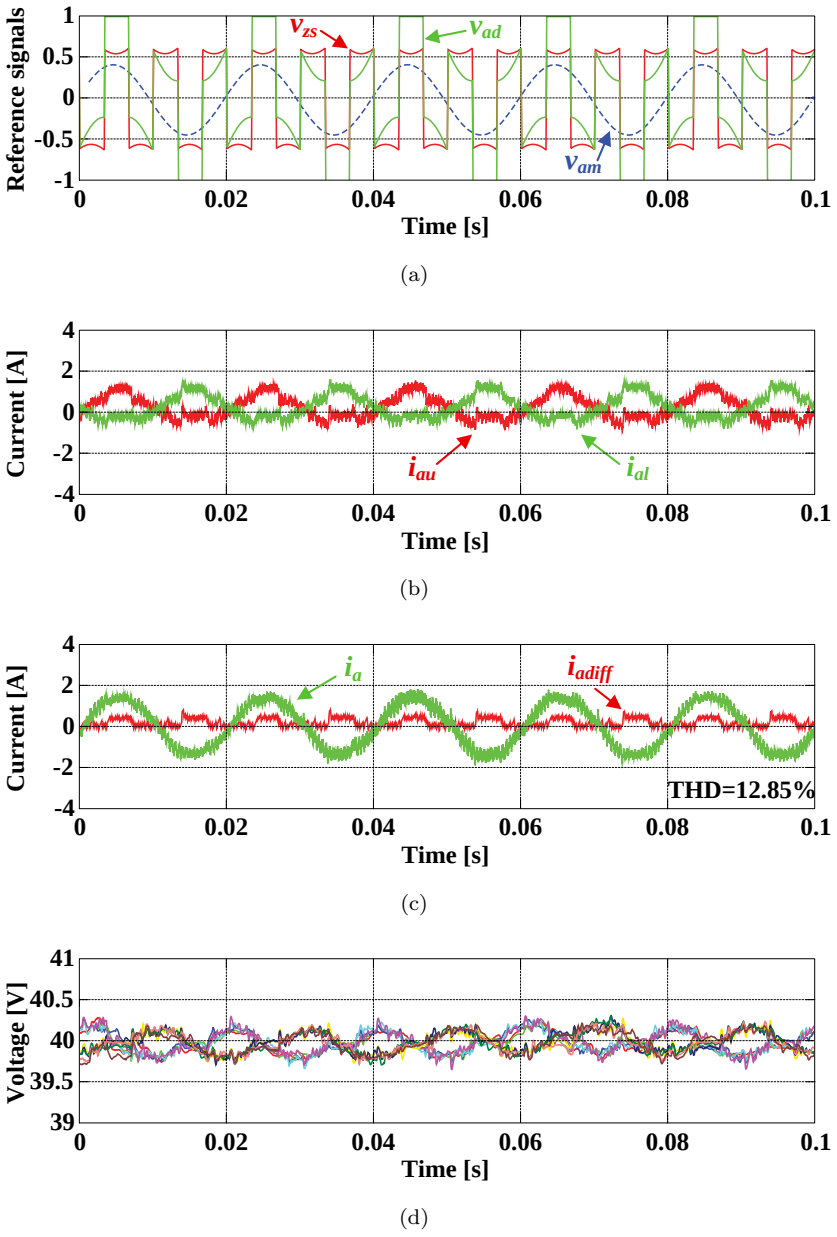


FIGURE 4.21: Experimental results of CL-DPWM operating with a resistive-inductive load (Load 1) and $m = 0.45$: (a) reference signal, (b) arm currents, (c) output and circulating currents, and (d) capacitor voltages.

are activated. Therefore, when a phase-leg is clamped, the arm that has an individual reference signal clamped to 1 (or -1) is the arm with the maximum (minimum) reference signal, without taking into account if it is the upper or lower arm. When the differential control signal is positive, the performance is the same than in CL-DPWM. However, when the differential control signal is negative, the arm fixed to 1 or -1 is the one with all the SMs activated.

As an example, if the lower reference signal of an arm that should be clamped up is higher than the upper reference signal, the lower arm is fixed to 1. This situation is

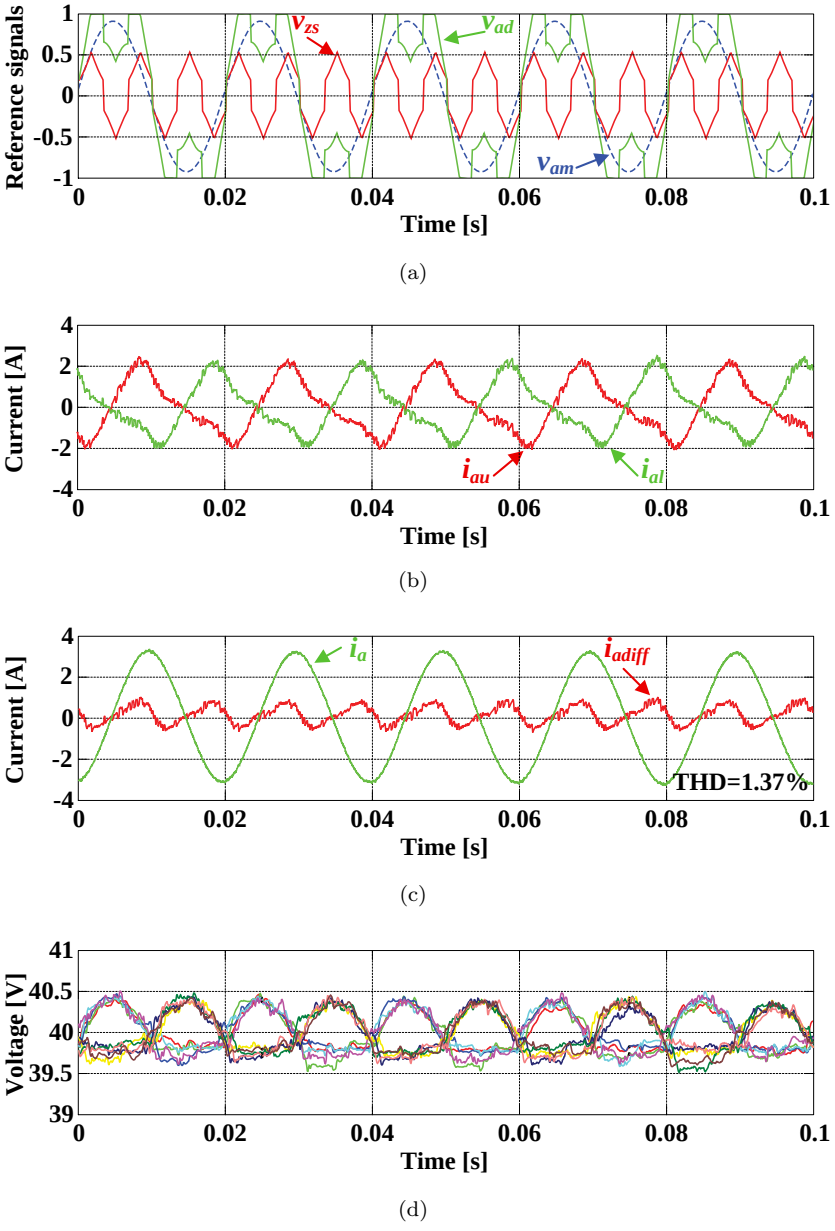


FIGURE 4.22: Experimental results using CL-DPWM with a purely inductive load (Load 2) and $m = 0.95$: (a) modulation and zero-sequence signals, (b) arm currents, (c) output current and circulating current, and (d) capacitor voltages.

called virtual clamping, since the arm that should have no SMs activated is the one that remains switching to control the circulating current. This approach to discontinuous modulation eliminates the requirement of working out of the modulation limits [1,-1], and therefore, the need for additional SMs.

Fig. 4.23 depicts an example of actual and virtual clampings on the upper rail of the dc-link. Note in this figure that, in the case of applying CL-DPWM (Fig. 4.23(a)), the arms include M additional SMs to the N basic ones. During the clamping interval in this example, all the SMs of the upper arm are bypassed (deactivated) while some SMs

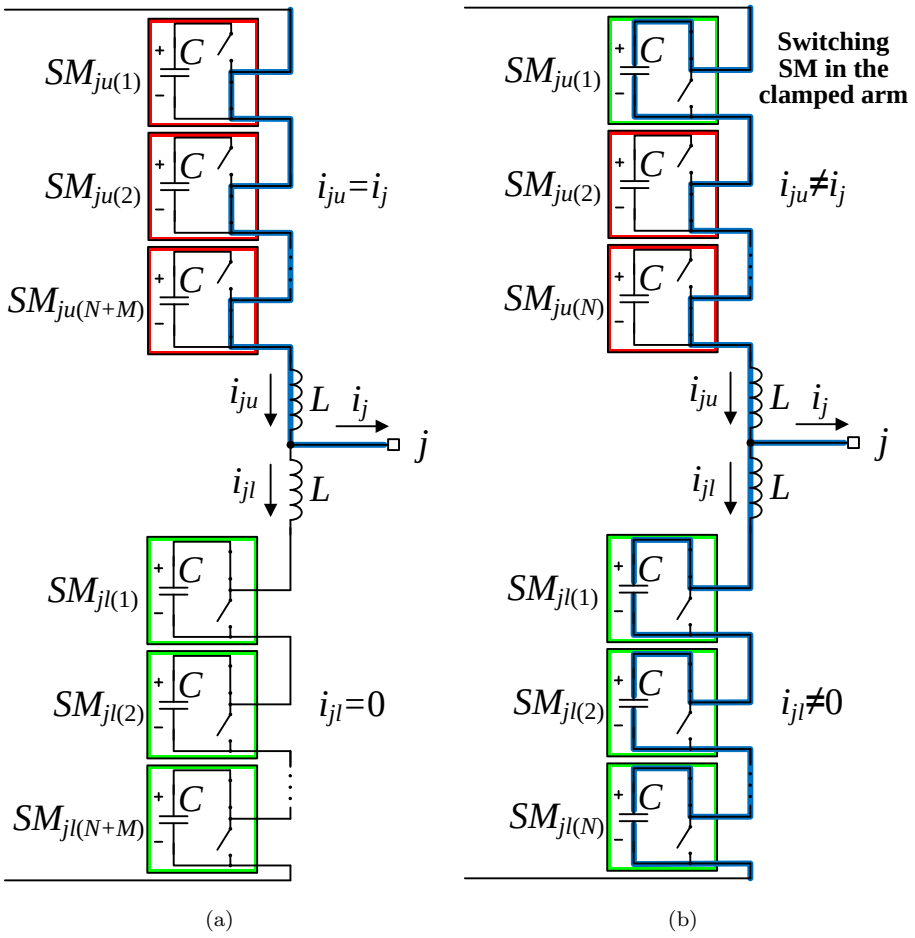


FIGURE 4.23: Circuit diagram of an MMC phase-leg when performing (a) actual clamping with CL-DPWM and (b) virtual clamping with VDPWM.

of the lower arm switch to regulate the circulating current. On the other hand, with VDPWM (Fig. 4.23(b)), no extra SMs are included. In this case, some SMs from the upper or the lower arms can switch to control the circulating current.

This implementation avoids the use of additional SMs, but increases the capacitor voltage ripples with respect to CL-DPWM. It also increases the switching power losses, as during the virtual clampings, the arm that switches is the one that carries more current within the phase-leg. In converters with low-speed switching devices, the new approach may imply an increase in the total power losses. However, when using fast-speed switching devices, the savings in conduction losses can be higher than the increase in switching losses. For this reason, the VDPWM is expected to be useful for medium-power MMCs with a low number of SMs and implemented with fast-speed semiconductors, reducing the overall cost of the converter and the total power losses while slightly increasing the capacitor voltage ripples.

TABLE 4.4: Specifications of the Simulation Test Converter Used for VDPWM

Parameter	**Value**
Number of Basic SMs per Arm, N	3
Number of Additional SMs per Arm (only for CL-DPWM), M	1
SM Capacitors, C	1500 μF
Arm Inductors, L	3 mH
DC-Link Voltage, V_{dc}	700 V
AC-side rms Current, $I_{ac\,rms}$	4 A
Carrier Frequency, f_{cr}	5 kHz
Output Frequency, f	50 Hz

4.5.2 Simulation Results

VDPWM has been tested with simulations studies under MATLAB/Simulink environment. Simulation studies have been performed in a switched model of a three-phase SiC-based MMC. The model implemented has a nominal power of 3.5 kW and integrates three basic SMs per arm ($N = 3$). A three-phase current source has been considered as a load, and a reduced switching frequency voltage balancing algorithm has been implemented [91]. Specifications of this test converter are given in Table 4.4.

Simulation studies evaluate the total power losses and the capacitor voltage ripple amplitudes obtained with VDPWM. Results are compared to the ones obtained with CL-DPWM and with CB-SVPWM. The model used for the simulation of CL-DPWM includes one additional SM ($M = 1$). Results are presented for different operating points, where m is the modulation index before the injection of a zero-sequence (0.1 to 1.15), and φ corresponds to the current phase angle in degrees [-180°, 180°].

The power losses are calculated considering the SiC commercial components Cree CMF20120D MOSFET and Cree C4D10120D diode. The main maximum ratings of the transistor are a forward current of 42 A and a direct voltage of 1200 V. The data of the MOSFET and diode for the calculation of the losses are obtained from the manufacturer datasheet.

A reduction in the conduction losses and an increase in the switching losses is expected when comparing VDPWM against CL-DPWM. However, switching power losses in the SiC-based test converter are very small to be significant. For this reason, only the total power losses are presented, considering that the main differences are caused by the conduction losses. Fig. 4.24 depicts the total power losses ratio between VDPWM and CL-DPWM for different operating points. It can be seen that the power losses with

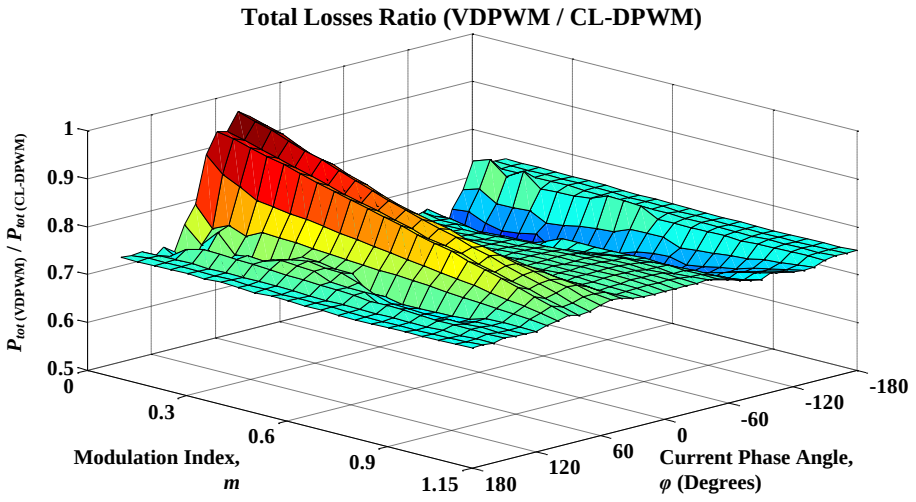


FIGURE 4.24: Simulation results: total power losses ratio between VDPWM and CL-DPWM.

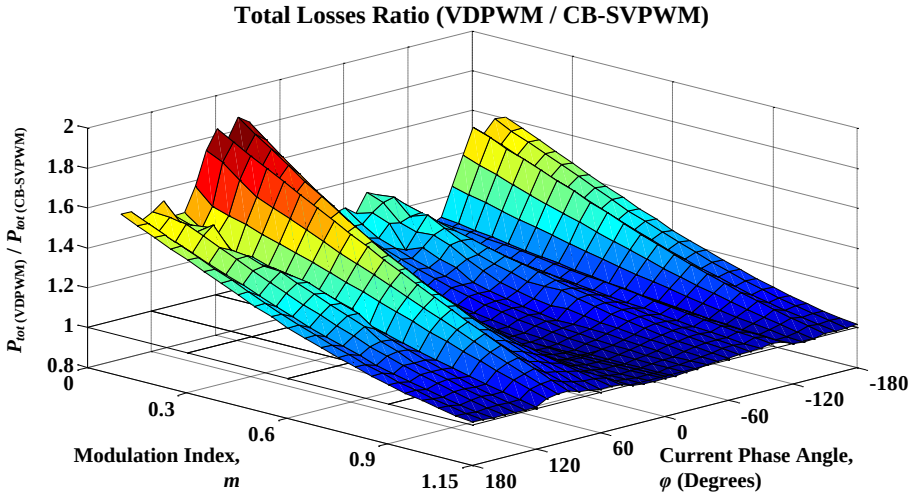


FIGURE 4.25: Simulation results: total power losses ratio between VDPWM and CB-SVPWM.

VDPWM are lower than with CL-DPWM for all the operating points. On average, the losses produced with VDPWM are 25% lower than those produced with CL-DPWM.

When using any kind of discontinuous modulation, the rms value of the circulating current increases when compared to CB-SVPWM. This fact can be observed in Fig. 4.25, where the losses of VDPWM and CB-SVPWM are compared. The losses ratio is always higher than one, having a mean value of 1.223.

One of the main benefits of discontinuous modulation techniques respect to the traditional ones, such as CB-SVPWM, is a reduction in the capacitor voltage ripples. In the case of VDPWM, such a reduction is slightly lower than with CL-DPWM. Moreover, the use of additional SMs in CL-DPWM provides a further reduction in the capacitor voltage ripples. Fig. 4.26 shows the ratio of the capacitor voltage ripple amplitudes

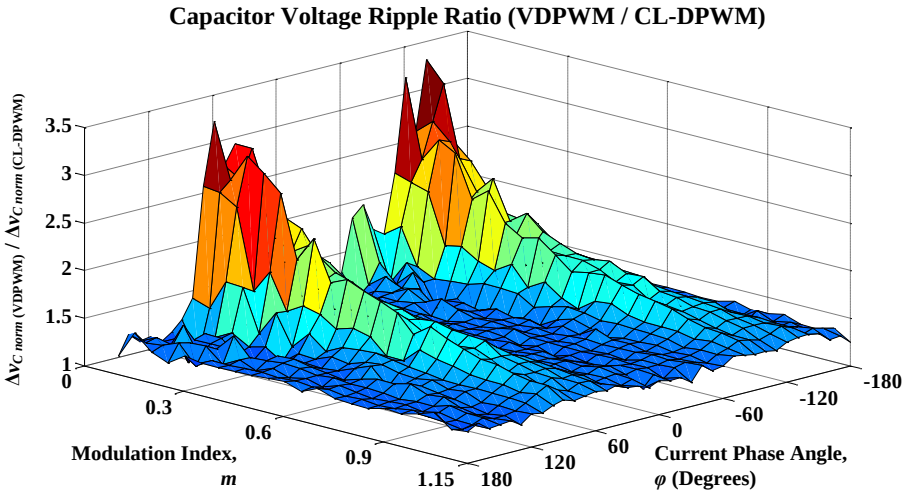


FIGURE 4.26: Simulation results: Capacitor voltage ripple ratio between VDPWM and CL-DPWM.

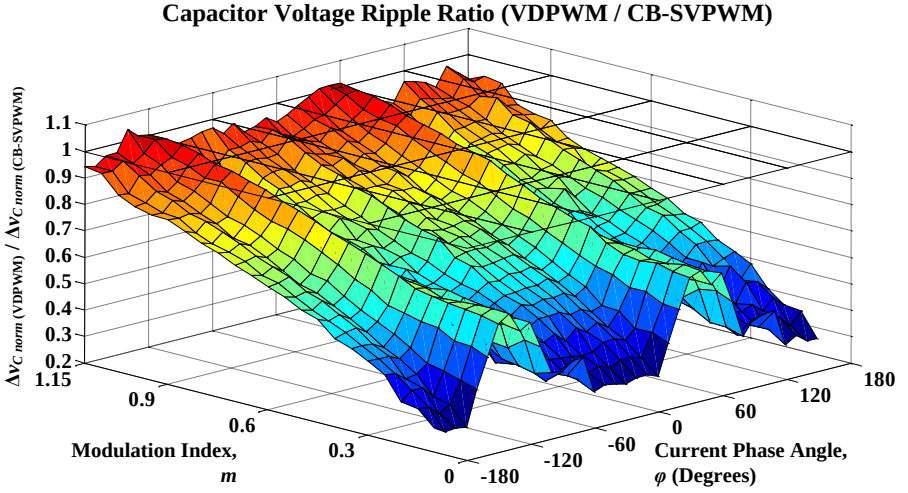


FIGURE 4.27: Simulation results: Capacitor voltage ripple ratio between VDPWM over CB-SVPWM.

between VDPWM and CL-DPWM. It can be seen that ripples are higher with the VDPWM, especially at low modulation indices and highly reactive currents. On average, the capacitor voltage ripples with modulation indices from 0.3 to 1.15 are 46% higher with VDPWM than with CL-DPWM. Nevertheless, VDPWM maintains a reduction in the capacitor voltage ripples for all the operating conditions with respect to CB-SVPWM, as it can be observed in Fig. 4.27. The reduction in the capacitor voltage ripples reaches a minimum ratio of 0.26 for a modulation index $m = 0.1$.

4.5.3 Experimental Results

VDPWM has also been implemented and tested in the TIEG-P prototype, configured as a three-phase MMC. The prototype has been implemented using the SiC devices

TABLE 4.5: Additional Specifications of the Laboratory Prototype for the VDPWM

Parameter	**Value**
DC-Link Voltage, V_{dc}	200 V
Load Resistor, R_{out}	25 Ω
Load Inductor, L_{out}	6 mH

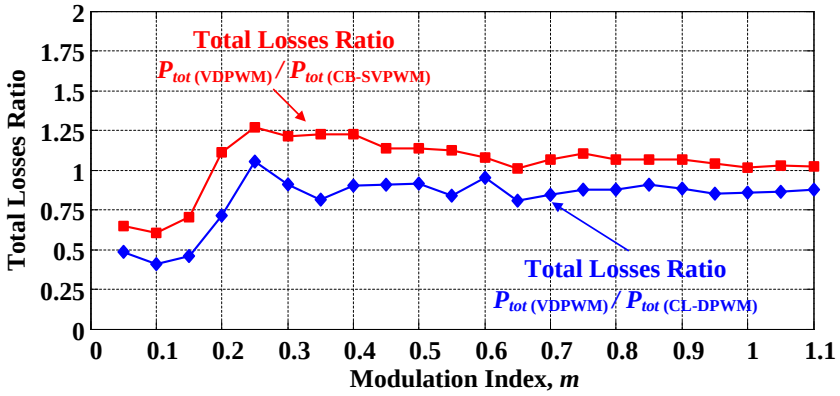


FIGURE 4.28: Experimental results. Total power losses ratio between the VDPWM and CL-DPWM and between VDPWM and CB-SVPWM.

considered in simulation and the tests have been done over an RL load. Most of the parameters are the same with the simulation tests, given in Table 4.4, except those that are given in Table 4.5.

The comparison of VDPWM against CL-DPWM and CB-SVPWM has also been done with the experimental results. Total power losses and capacitor voltage ripples have been measured for different operating conditions of m, which ranges between 0.05 to 1.10. The phase of the output current respect to the output voltage (φ) is defined by the RL load and is about -4°.

Fig. 4.28 depicts the total losses ratio measured experimentally. It can be seen that the power losses with VDPWM are lower than with CL-DPWM for almost all the operating conditions. In contrast, the losses produced by VDPWM are higher than the ones produced with CB-SVPWM.

Comparisons of the capacitor voltage ripples with the different techniques are depicted in Fig. 4.29. As expected, the ratio between VDPWM and CB-SVPWM is lower than one, as VDPWM reduces the capacitor voltage ripples. However, VDPWM is not as successful as CL-DPWM in reducing the capacitor voltage ripples, this is why the ratio between VDPWM and CL-DPWM is higher than one in most operation conditions. An example of the differences in the capacitor voltage ripples depending on the

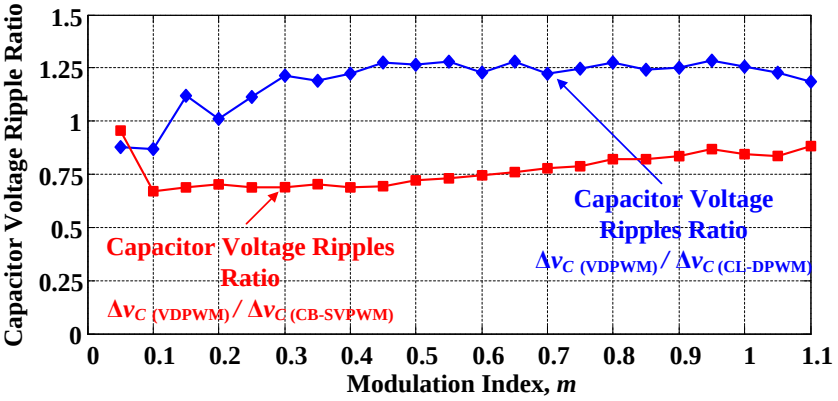


FIGURE 4.29: Experimental results. Capacitor voltage ripples ratio between the VD-PWM and CL-DPWM and between VDPWM and CB-SVPWM.

modulation technique can be observed in Fig. 4.30, where the measured voltages are depicted.

4.6 Conclusion

In this chapter, discontinuous modulation has been considered for the operation of the MMC. This technique is based on clamping the phase leg to the upper or lower terminals of the dc-link. In the clamped arm no switching transitions are produced, reducing the switching power losses. Moreover, the major part of the phase current flows through the clamped arm, where no SMs are activated, highly reducing the capacitor voltage ripples, especially for low modulation indices. The effectiveness of the technique has been demonstrated with simulation and experimental results. This technique not only helps to reduce the switching power losses of the MMC in grid-connected applications, but it also enables the use of the MMC in motor drive applications by reducing the capacitor voltage ripples when the motor operates with low modulation indices, i.e., low frequencies/speeds.

Three approaches of discontinuous modulation are presented. A first open-loop approach (OL-DPWM) is based on a modulation signal with constant clamping intervals. Those intervals coincide with the maximum values of the modulation signal. A second approach (CL-DPWM) uses a closed-loop algorithm for defining the zero-sequence signal. If possible, the arm with the highest current in absolute value is clamped, maximizing the switching power losses and capacitor voltage ripple reduction. Finally, a third approach for medium-power applications (VDPWM) is presented, which does not require the use of additional SMs. The third approach does not reduce the capacitor voltage ripples and switching losses as much as CL-DPWM, but reduces the number of SMs in the arms, and therefore, the converter costs and the conduction losses. If a

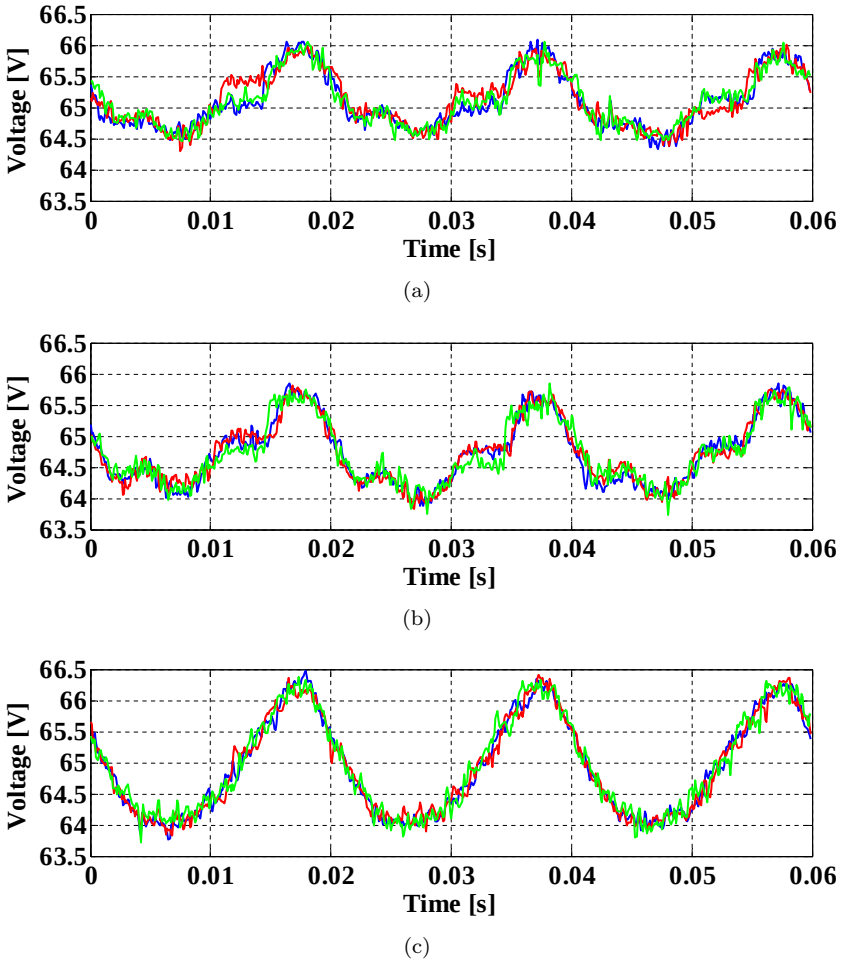


FIGURE 4.30: Experimental results of the capacitor voltages with $m = 0.8$ when using different modulation techniques: (a) CL-DPWM, (b) VDPWM and (c) CB-SVPWM.

fast-switching technology of power devices like SiC is used, the reduction in conduction losses implies a total reduction of the overall power losses of the converter.

Chapter 5

Voltage Measurement System

A new technique for measuring the capacitor voltages in an MMC is explained in this chapter. This technique allows to measure the capacitor voltages of all the SMs with only two voltage sensors per arm. Each sensor measures the output voltage of a set of SMs connected in series and acquires a new measurement when there is only one SM activated within the set. The acquired value corresponds to the capacitor voltage of the activated SM minus the voltage drops produced in the switches. A simple mathematical model is used to estimate all the SM capacitor voltages, and it is then updated whenever there is a new measurement available. This measuring technique highly reduces the number of voltage sensors, hence reducing the complexity and costs of the signal conditioning and data acquisition stages.

5.1 Introduction

The capacitor voltages of the SMs of an MMC are usually obtained by direct measurement of all the SM capacitors. In real applications of the MMC, the number of SMs per arm can reach into the hundreds [4]. Therefore, a large number of voltage sensors is required in order to provide signal measurements that need to be acquired and adapted. Aside from compromising its reliability, this complicates the implementation and control of the MMC.

Several studies have been performed to solve this challenge. Multiple open-loop techniques, based on modulation patterns or carrier rotation, have been developed [19, 30, 53], but their stability may be compromised because of the open-loop operation. Recently, techniques based on advanced estimators have also appeared. In [56], the capacitor voltage values are calculated from other variables including the arm currents

and the dc-link voltage, and in [57], the capacitor voltages are estimated by the arm currents and corrected by measuring the arm voltages. Closed-loop voltage balancing algorithms that reduce the processing time in MMCs with a large number of SMs have also been proposed [33,54,55], however they do not reduce the number of voltage sensors required. A technique to reduce the hardware complexity of the voltage sensing stage maintaining closed-loop operation was presented in [58]. In that publication, the SM capacitor voltage signals are multiplexed, measuring only a part of the signals each sampling period. The SM capacitor voltages are estimated in between the measurements. Although the technique presented in [58] does not reduce the number of sensors, it highly reduces the complexity of the acquisition stage.

A new technique to determine the SM capacitor voltages by using a reduced number of voltage sensors was presented in [124]. In this technique, the minimum number of voltage sensors required per arm is two. Each voltage sensor is connected at the output of a set of SMs in series, acquiring the voltage measurement only when one SM of the set is activated. The acquired value corresponds to the capacitor voltage of the activated SM minus the voltage drops in the semiconductors, which can be easily estimated. Similarly to [58], since the measurements of all the capacitor voltages are not always available, they are estimated by a mathematical model between actual measures. In this mathematical model the capacitor voltage values are updated whenever there is an actual measurement available. In order to ensure a periodic update of each of the estimated capacitor voltages, an algorithm that enforces measurement of each capacitor voltage is also introduced to improve the proposed sensing technique. This technique was registered as a Spanish [125] and international patent [126].

5.2 Topology and Principles of Operation

The measuring technique presented in [124] is based on dividing each arm of the converter into sets of SMs and using a voltage sensor for each set. The sensors are connected at the output of the series-connected SMs, measuring the sum of the voltages supplied by the SMs of the specific set. The measured voltage is $v_{Sz(k)}$, where z identifies the upper or lower arm ($z \in \{u, l\}$) and k the number of the measuring set. Voltage $v_{Sz(k)}$ is a multilevel waveform that will be acquired when only one SM of the measuring set is activated, obtaining a voltage almost equal to the capacitor voltage of the activated SM. The difference between the real and the measured capacitor voltage corresponds to the voltage drop in the on-state switches, which can be considered negligible or be estimated easily.

In order to avoid switching noise, the voltage measurements are synchronized with the pulse-width modulator. The capacitor voltage is sampled at the midpoint between switchings, i.e. when the triangular carrier is maximum and minimum. Moreover, the measurements acquired very close to a switching transition are rejected.

Fig. 5.1 shows a diagram of an MMC phase-leg where each arm is divided into two sets. The figure shows the distribution of the sets and the connection points of the sensors in the phase-leg. Since the voltage measurement technique is performed individually per each phase-leg, this chapter is explained for a single-phase converter, excluding the phase identifier j from the mathematical analysis and block diagrams.

A measurement example of an MMC with six SMs per arm (N=6) is depicted in Fig. 5.2. Since there is only one SM activated in each set at this particular instant, each sensor in the example measures the voltage of a single SM capacitor; i.e., $v_{Su(1)}$ and $v_{Su(2)}$ are practically equal to $v_{Cu(1)}$ and $v_{Cu(5)}$, respectively.

5.2.1 Voltage Estimation

Due to its principle of operation, the measuring technique on its own does not provide the instantaneous capacitor voltages at all times. However, the capacitor voltage balancing algorithms requires continuous updating. For this reason, the measuring technique is complemented with an algorithm that calculates the estimated capacitor voltage value since the last measurement. The estimation has to be performed for all the SMs, so a simple and fast-processing algorithm should be used. By knowing the state of the SMs $s_{z(n)}$ and the arm current i_z, the capacitor voltages $v_{Cz(n)}$ are calculated by applying the switched model of the converter (Section 2.2). Capacitor voltage given in (2.12) can be re-written as:

$$v_{Cz(n)} = \frac{1}{C}\int_{t_0}^{t} s_{z(n)} i_z dt + V_{Cz(n)S} \ , \tag{5.1}$$

where t_0 is the last measuring time of the capacitor voltage, and $V_{Cz(n)S}$ is the measured capacitor voltage at t_0 with the set sensor. When a new measurement of the capacitor voltage is available, the integral term in (5.1) is reset and $V_{Cz(n)S}$ becomes the measured voltage. Hence, the error accumulated in the capacitor voltage estimator is periodically eliminated by incorporating the actual voltage measurement.

The use of estimation algorithms that are executed continuously in the central processing unit (CPU), allows responding rapidly to dynamic changes of the converter operation. Any standard CPU can process the estimation algorithm very quickly, allowing the MMC controllers to operate with no practical speed limitations due to the implementation of the proposed measuring technique. The periodic measurements of

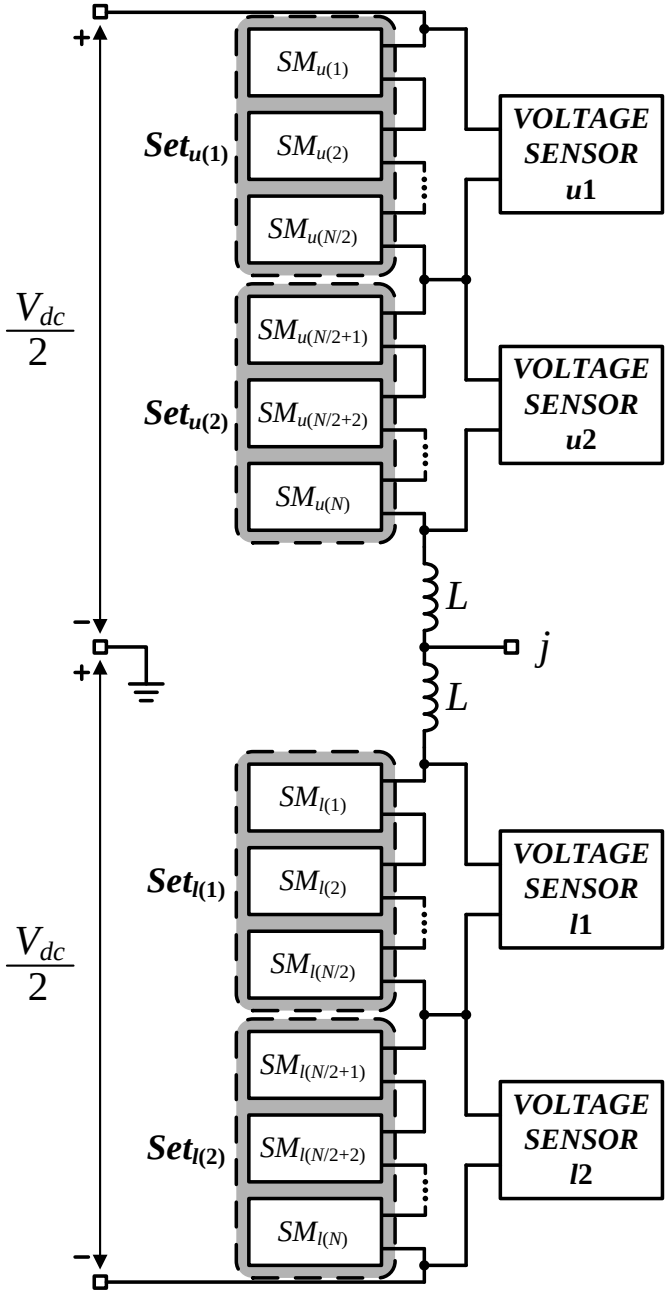


FIGURE 5.1: Distribution example of measuring sensors on a phase-leg. Each arm is divided into two sets of SMs.

the capacitor voltages are used only to update the values of the estimators in order to avoid accumulative errors in the estimated voltages.

In fact, in MMCs with a high number of levels, the new measuring technique can even reduce the response time because the estimation algorithm can be executed faster than the acquisition of many SM capacitor voltages.

The new measuring technique has only been tested with a simple and fast-processing

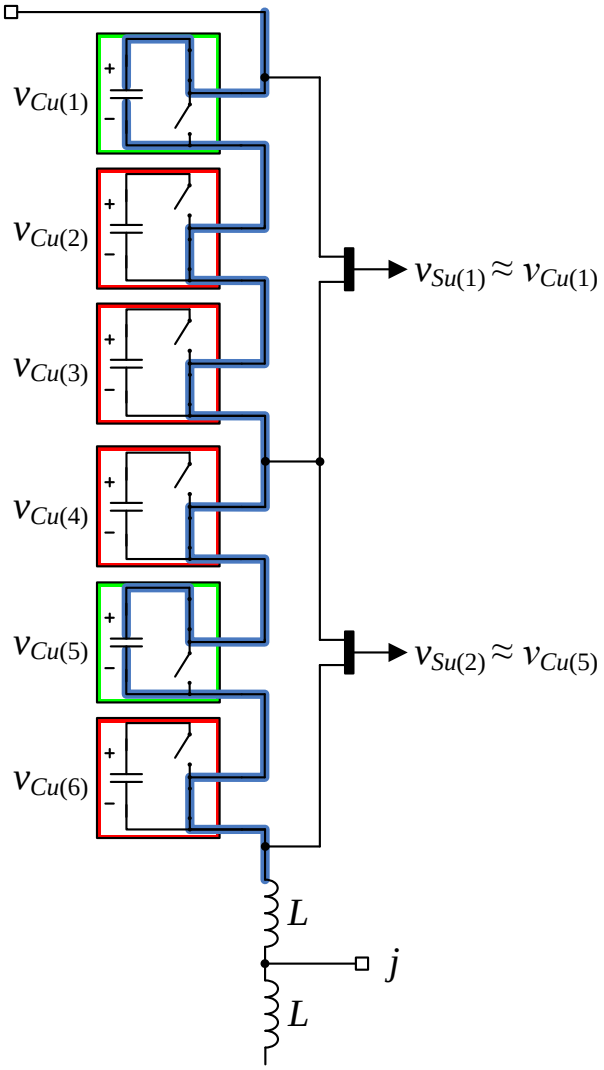


FIGURE 5.2: Measurement example in an arm with six SMs (N=6).

algorithm for the estimation of the capacitor voltages. However, more accurate estimation models, like those presented in [56] and [58], could also be used.

The block diagram depicted in Fig. 5.3 shows the different processes that integrate the new voltage measuring technique. First, the set voltages ($v_{Sz(k)}$) are acquired and their correspondence with a single capacitor voltage measurement is checked. An individual counter ($Cnt_{z(n)}$) is used for each SM and it is increased every time a measurement is performed. If the measure corresponds to a single SM capacitor voltage, the measure is updated in the estimator and the individual counter is reset. The estimated voltages are sent to the enforced measuring algorithm, which, if necessary, modifies their values in order to facilitate the single measurement of a particular capacitor. The performance of this algorithm is detailed in Section 5.3.

As shown in Fig. 5.3, the measuring technique provides the capacitor voltages to

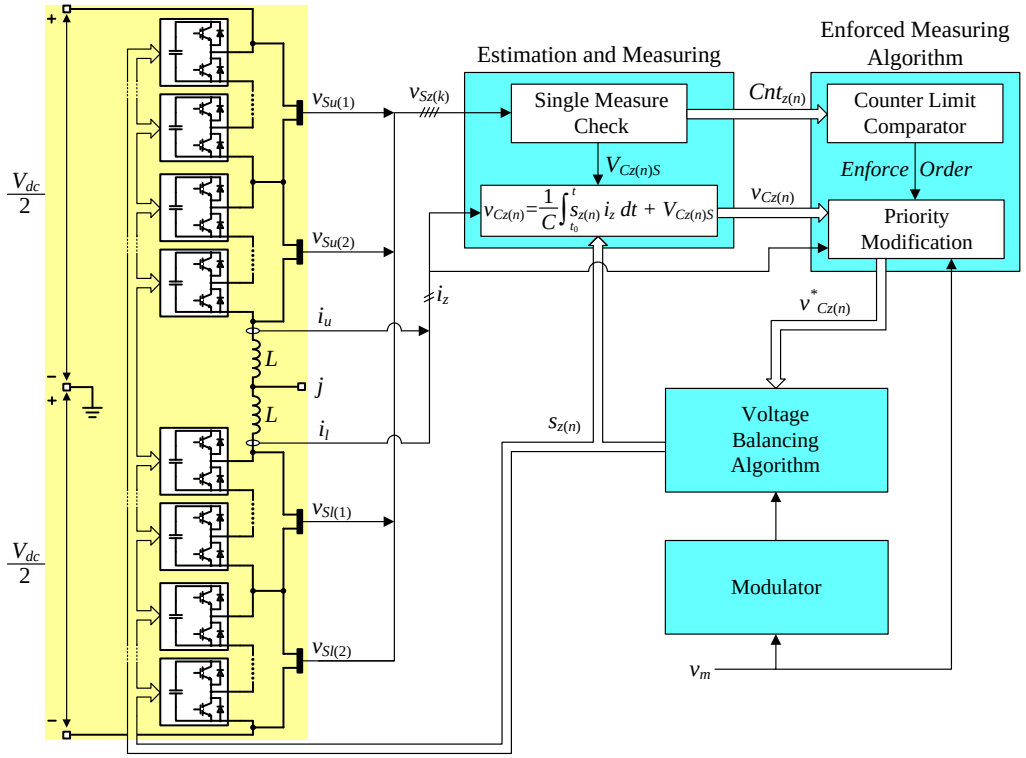


FIGURE 5.3: Block diagram of the measuring technique.

the voltage balancing algorithm as an input, without affecting its internal performance. Therefore, this technique is not only independent of the modulation technique implemented, but also of the algorithm used to balance the capacitor voltages. In the case of using a voltage balancing algorithm without reduced switching frequency, estimation inaccuracies may modify the switching frequency because several SMs can be activated and deactivated at any switching transition to balance the capacitor voltages. However, if a voltage balancing algorithm with reduced switching frequency is used (Subsection 2.4.1), only one SM is activated or deactivated per switching transition, achieving constant switching frequency regardless the accuracy in the capacitor voltage measurement.

5.2.2 Minimum Number of Sensors

The measuring technique could be applied by dividing each arm into only one measuring set of SMs; i.e., using one voltage sensor per arm. However, its application range would be limited, since voltage measurements would be performed when only one SM per arm is activated. In MMCs with a high number of SMs, this situation would never happen when operating with low modulation indices. For this reason, the measuring technique is used with a minimum of two sensors per arm, each one of them will measure the voltage supplied by half of SMs in the arm. The use of two measuring sets per arm allows measurements to be performed when $N/2+1$ SMs or less are activated, a situation that

appears for all the modulation indices. To perform the measurement, only one SM in a measuring can be activated, being the rest of activated SMs in the other set. Although the minimum number of sensors in the arm is two, this number can be increased in order to improve the measuring frequency and therefore reduce the maximum error accumulated in the capacitor voltage estimators.

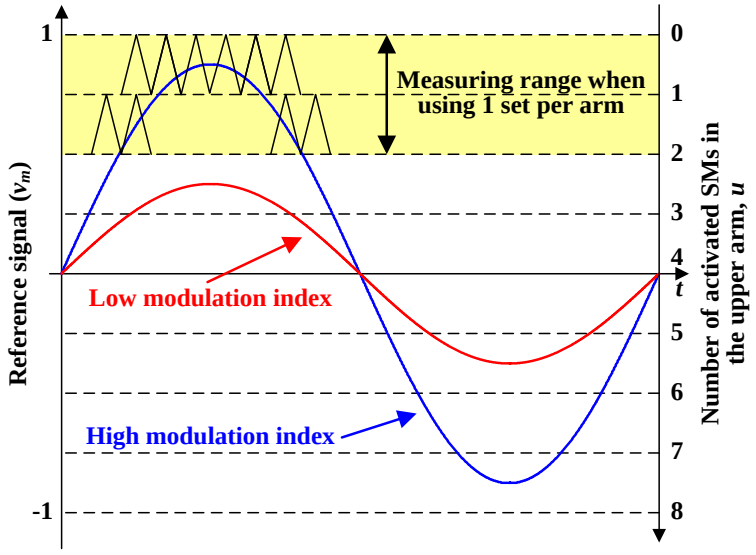
An example of the operation range of the proposed technique depending on the number of sets per arm is depicted in Fig. 5.4. In this example, the number of SMs per arm is eight (N=8) and the reference signal can range in the interval [-1, 1]. The yellow areas are those in which a single SM of a set can be activated in the upper arm. Fig. 5.4(a) shows the case of using a single sensor per arm. In this case, a single SM of the upper arm will be activated only when the reference signal is located within the two upper zones. Since the reference signal will only reach those zones when operating with high modulation indices ($m > 0.5$ in this example), measurements can not be performed for the full operation range of the converter. One the other hand, Fig. 5.4(b) shows the case of using two voltage sensors per arm. Now, the yellow areas where a single SM in each set may be activated involve both low and large modulation indices. Consequently, capacitor voltage measurements can be performed for the full range of operation of the converter.

5.2.3 Implementation Considerations

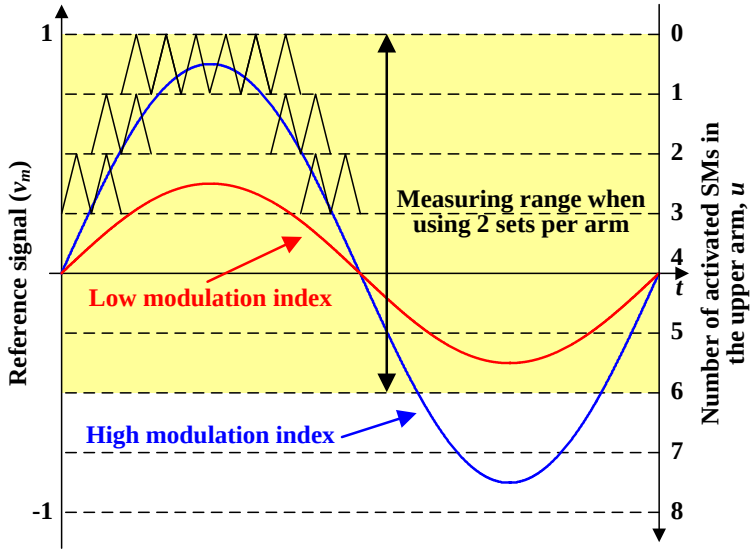
In high-voltage applications, where the number of SMs per arm is very high, different aspects have to be considered to select the proper number of voltage sensors. The main criterion that should be optimized is the actual measuring frequency of the capacitor voltages. The sampling frequency of the voltage sensor has to be always twice the switching frequency. However, actual measures are performed when only one SM in the measuring set is active, and only one SM is measured at a time. For this reason, the higher is the number of SMs in a measuring set, the lower is the actual measuring frequency. This measuring frequency depends on several factors, such as the number of SMs per measuring set, the switching frequency, the modulation index, the voltage balancing algorithm, etc., it is therefore difficult to adjust and thus it is adjusted empirically.

For example, in an MMC with 200 SMs per arm, 20 voltage sensors per arm can be used, which corresponds to one sensor for each 10 SMs. This means a significant reduction in the cost and complexity of the measuring system.

There is a second criterion that must be taken into account when defining the number of voltage sensors: the maximum voltage range of the sensor. The voltage sensors used in the proposed measuring technique have to withstand voltage values much larger than



(a)



(b)

FIGURE 5.4: Measuring range example for the upper arm with N=8 when using: (a) one and (b) two measuring sets per arm.

their usual measuring value, i.e., the voltage of a single capacitor. As the maximum voltage range is proportional to the number of SMs in a measuring set, this parameter has to be considered when defining the number of voltage sensors.

The requirement of withstanding a maximum voltage range much higher than the usual measuring value leads to an important reduction on the accuracy of the measurements. In order to solve this problem, a signal conditioning stage based on a voltage limiter is proposed. A circuit diagram of the proposed solution is depicted in Fig. 5.5, where the measured voltage is reduced using a precision voltage divider made with resistors. The voltage seen by the voltage transducer is limited using a series of Zener diodes.

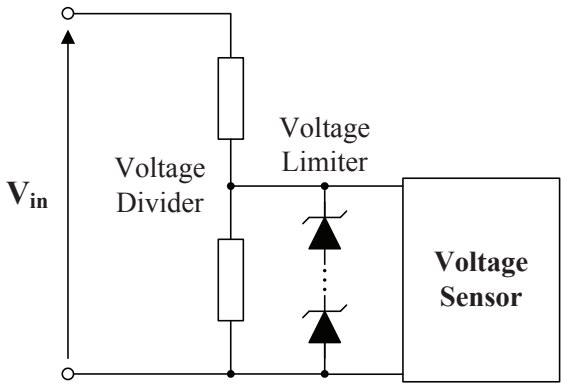


FIGURE 5.5: Circuit diagram of the voltage sensor conditioning stage.

This circuit reduces the maximum voltage applied to the sensor without compromising the measurement accuracy.

5.3 Enforced Measuring Algorithm

The measuring technique uses the favourable situations that happen in the operation of the MMC to perform the individual capacitor voltage measurement. However, it does not ensure measurement of all the SM capacitor voltages in a delimited time interval. For this reason, the measuring technique can be complemented by an enforced measuring algorithm. If a particular SM capacitor voltage is not measured for a certain time, the enforced measuring algorithm will facilitate the activation of that SM alone in the measuring set.

Unlike the measuring and estimation technique, the enforced measuring algorithm depends on the internal operation of the voltage balancing algorithm. In this thesis, only voltage balancing algorithms based on sorting the SM capacitor voltages have been considered. An algorithm with reduced switching frequency (Subection 2.4.1) has been considered in this chapter, but the same enforced algorithm would work properly with other sorting techniques.

In order to implement the enforced algorithm, the time since the last actual measurement of each SM ($Cnt_{z(n)}$) is considered. If a particular time surpasses a pre-defined limit, the enforced measuring algorithm will be activated. In order not to interfere much with the operation of the converter, this algorithm will increase the probability of the SM to be activated alone in the measuring set by increasing its priority and decreasing the priority of the other SMs in the same measuring set.

The priority modification is achieved by increasing or decreasing the estimated capacitor voltage values $v_{Cz(n)}$ in a percentage δ. The modified capacitor voltages $v^*_{Cz(n)}$

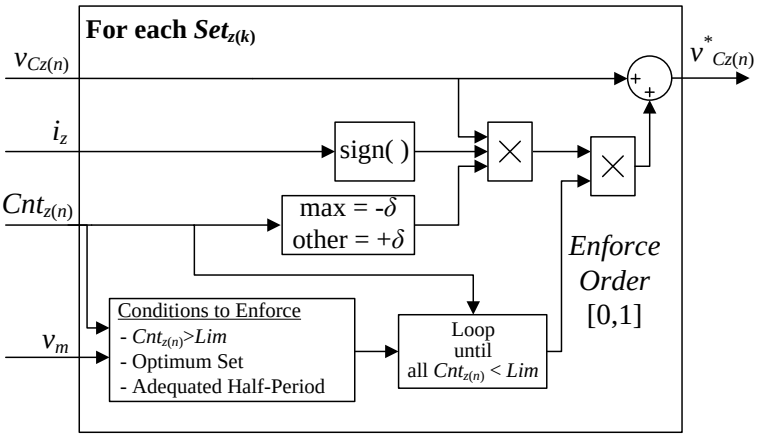


FIGURE 5.6: Block diagram of the enforced measuring algorithm.

are the ones used in the voltage balancing algorithm. When the arm current is positive (it charges the SM capacitors), the priority of the target SM is increased by reducing the modified voltage $v^*_{Cz(n)}$. On the contrary, it is increased by the same amount if the arm current goes in the discharging direction. The priority of the other SMs in the same measuring set is reduced by proceeding in the opposite way, i.e., increasing the estimated voltage when the current is positive and decreasing the voltage when the current is negative.

The percentage δ is designed to increase the priority of the SMs enough to change its state during the next sampling period. For this reason, the modified capacitor voltage of the target SM should be higher (or lower) than all the other SMs. But in order not to disturb excessively the voltage balancing operation, the voltage modification should be the minimum possible. A good reference for the value of δ is to be twice the capacitor voltage ripple amplitude operating under rated conditions, i.e., if the voltage ripple amplitude is 5% of the reference value, δ should be set to about 10%.

A block diagram showing the proposed enforcing algorithm is depicted in Fig. 5.6. In this figure, the algorithm of the priority modification process is detailed. The requirements for activating the enforced measuring algorithm are also summarized.

The main requirement for activating the enforced measurement algorithm is an excessive amount of time since the last actual measurement of a SM. However, as this algorithm modifies the operation of the converter, more considerations have to be taken into account to minimize its negative effects. Single measurements in a particular arm can only happen during one half-period of the modulation signal or when the modulation reference is near zero, i.e., when the number of SMs activated in the arm is less than or equal to $N/2 + 1$. For this reason, the enforced measuring algorithm will only be activated in the adequate half-period, i.e., when the modulation signal is positive for the upper arm and negative for the lower arm.

A second restriction that has to be considered in the application of the enforced measuring algorithm is that more than one SM can surpass the actual measuring time limit at the same time. As only one SM can be enforced at a time, an order between them has to be imposed. Although a logical order could be directly defined from the time that has happened since the SM last single measurement, this may interfere significantly with the voltage balancing process.

When enforcing a measurement, some time is required for changing the activated SMs between two different measuring sets. That is, if a particular SM capacitor in a measuring set needs to be measured and other SMs in the same set are activated, they have to be deactivated and the same amount of SMs needs to be activated in other measuring sets. When using a voltage balancing algorithm with reduced switching transitions, a limited number of SMs will change each switching period and therefore several switching periods are needed until a forced voltage measurement can be performed. Let us assume that three capacitor voltages need to be measured: the first SM is in the measuring set $Set_{u(1)}$, the second one is in the measuring set $Set_{u(2)}$, and the third one is again in $Set_{u(1)}$. In this case, the enforcing process will require some time transferring the SMs from the $Set_{u(1)}$ to the $Set_{u(2)}$; then form the $Set_{u(2)}$ to the $Set_{u(1)}$, and finally from $Set_{u(1)}$ to the $Set_{u(2)}$ again.

In order to reduce the time required for the enforced measuring process, it will start by focusing on the SMs that have surpassed the time limit in the same set before changing to another set. That is, all the voltage measurements required in $Set_{u(1)}$ will be performed before proceeding with $Set_{u(2)}$.

The enforced measuring algorithm modifies the values sent to the voltage balancing algorithm in order to facilitate the activation of the desired SMs, but it does not force additional switching in the SMs. Moreover, when a voltage balancing algorithm with reduced switching frequency is used, the switching frequency of the SMs is exactly the same. The unique negative effect produced by the enforced measuring algorithm is a slight increase in the capacitor voltage imbalances, as the voltage values seen by the balancing algorithm are different than the estimated/real ones.

5.4 Simulation Results

The performance of the measuring technique has been tested with simulation studies developed in the MATLAB/Simulink environment. Simulation have been carried over a switched model of a three-phase MMC with twenty SMs per arm (N=20) and connected to the grid through the inductors L_{ac}. The measuring system has been implemented

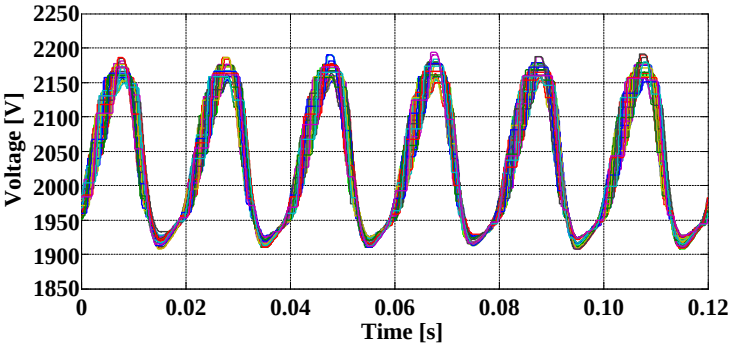
TABLE 5.1: Specifications of the Simulation Test Converter for the Measuring Technique

Parameter	**Value**
Number of SMs per Arm, N	20
SM Capacitors, C	1500 μF
Arm Inductors, L	3 mH
Grid Inductor, L_{ac}	12 mH
DC-Link Voltage, V_{dc}	40 kV
Grid Voltage, V_g	9.9 kV
AC-side rms Current, $I_{ac\,rms}$	200 A
Output Current Phase Angle, φ	45°
Carrier Frequency, f_{cr}	5 kHz
Sampling Frequency, f_{samp}	100 kHz
Output Frequency, f	50 Hz

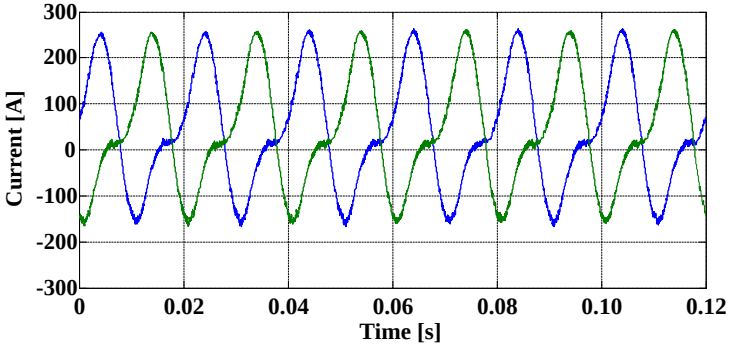
with only two voltage sensors per arm, and some non-ideal acquisition effects have been modelled, such as random noise to both the voltage and current sensors and a discrete sampling time. The specifications of this test converter are given in Table 5.1. In this simulation model, the circulating current is controlled according to the instantaneous reference calculation method from Subsection 3.4.2, using a sinusoidal reference as a modulation signal.

Fig. 5.7 presents the simulation results of the capacitor voltages of the upper arm SMs and the arm currents operating with a modulation index m=0.7. Two measuring techniques are compared: in Figs. 5.7(a) and (b) individual voltage sensors per SM are used while in Figs. 5.7(c) and (d) the proposed measuring technique is applied. Due to small differences between the estimated and the measured capacitor voltages, the capacitor voltages in Fig. 5.7(c) show more dispersion than those in Fig. 5.7(a). Nevertheless, such imbalances are small and within acceptable limits. Arm currents do not present any differences, demonstrating that the circulating current controller is not affected by the measuring technique. It should be remarked that in this example, 40 voltage sensors per phase-leg would be required with the individual sensors measuring technique while the new measuring technique requires only four sensors.

In order to demonstrate the effectiveness of the technique in correcting the accumulated errors, a simulation study using different SM capacitances has been performed. In this simulation, the capacitances have been modified randomly, following a normal distribution with a mean value of 1500 μF and a variance of 10%. Fig. 5.8 presents the simulation results with the randomly modified capacitances. Fig. 5.8(a) shows the



(a)



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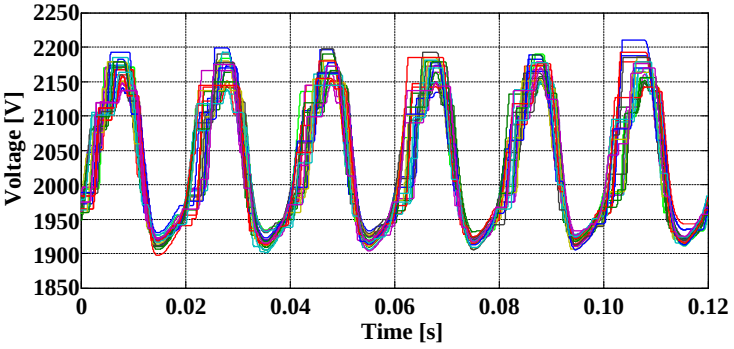

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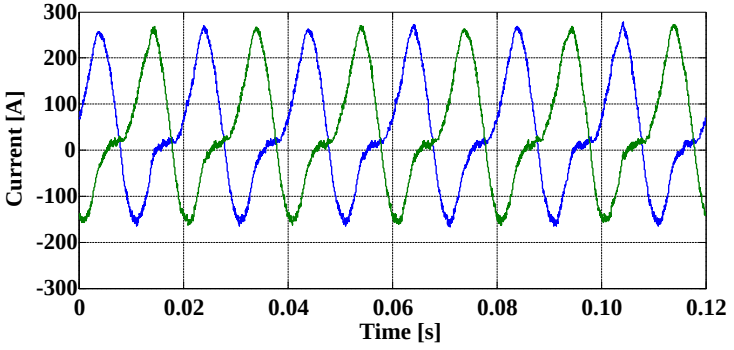
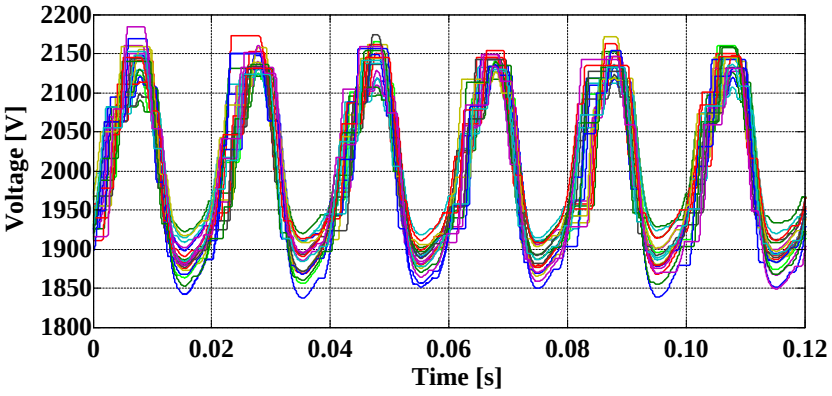
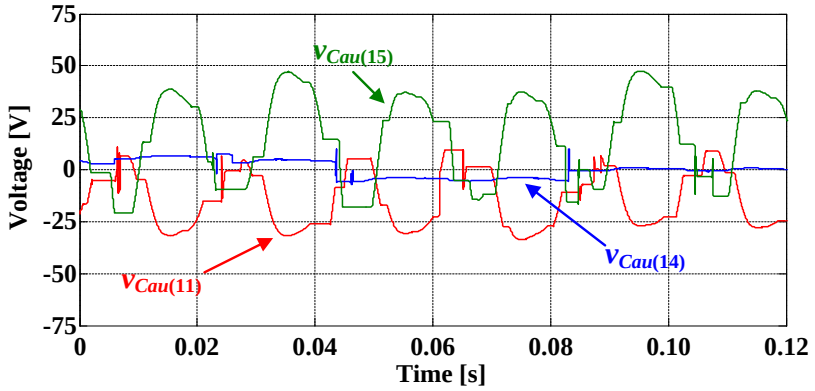


(d)

FIGURE 5.7: Simulation results with N=20 and m=0.7. Upper arm capacitor voltages (a) and arm currents (b) with individual measuring technique and upper arm capacitor voltages (c) and arm currents (d) with the new measuring technique.



(a)



(b)

FIGURE 5.8: Simulation results with the new measuring technique when considering different capacitances: (a) Upper arm capacitor voltages and (b) errors of the estimated capacitor voltages $v_{Cau(11)}$, $v_{Cau(14)}$, and $v_{Cau(15)}$, which capacitances are 1745 μF, 1500 μF, and 1227 μF, respectively.

capacitor voltages of the upper arm SMs when applying the new measuring technique. Fig. 5.8(b) shows the estimation errors (estimated value minus real value) of the capacitor voltages $v_{Cau(11)}$, $v_{Cau(14)}$, and $v_{Cau(15)}$, which capacitances are 1745 μF, 1500 μF and 1227 μF, respectively. As it can be seen the errors are periodically corrected, although the capacitor voltages are less balanced and have increased voltage ripples. The error correction is caused both by the intrinsic system dynamic and the updated information provided by actual measurements.

The periodic updating with actual values provides robustness to the estimation algorithm. However, if one or more capacitors have a capacitance significantly smaller than the nominal one, the new measuring system may produce instability to the converter. This can be demonstrated considering a simplified analysis where the capacitor voltage ripples are neglected. In that supposition, if a capacitor voltage was different than the reference value, the voltage balancing algorithm would activate or deactivate the corresponding SM until the estimated voltage equals the other capacitor voltages in the arm. However, if the real capacitance of the SM (C_{real}) was smaller than the expected one

(C_{est}), i.e. the nominal capacitance, the change in the capacitor voltage (Δv_{real}) would be larger than the estimated one (Δv_{est}):

$$\Delta v_{real} = \Delta v_{est} \frac{C_{est}}{C_{real}} \, . \tag{5.2}$$

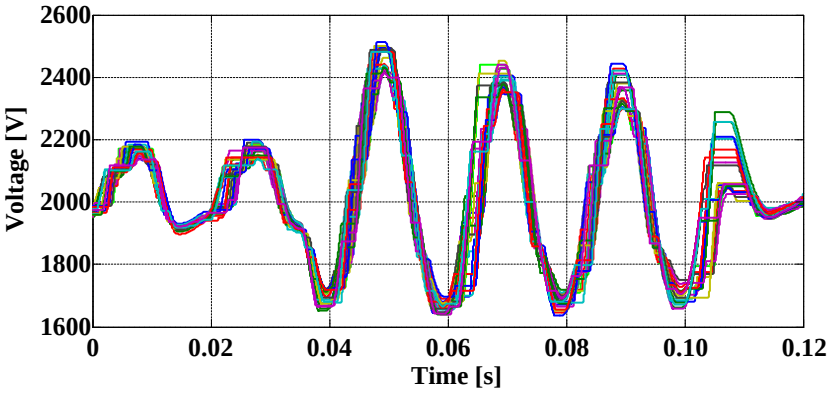
If the actual capacitance was smaller than half the estimated capacitance ($C_{real} < C_{est}/2$), the variation of the capacitor voltage after compensation would be more than twice the estimated variation, and consequently the error of the voltage would be larger than the original one but in the opposite direction. The measuring system would realize of this in the next actual measure and consequently the balancing controller will try to compensate for it. Then, the absolute value of the error would increase continuously making the system unstable. On the contrary, in the case that the SM capacitance was larger than half of the estimated one ($C_{real} > C_{est}/2$) the absolute value of the error after compensating would decrease and hence the system would be stable. It should be remarked that, in practice, having a capacitance smaller than 50% of its nominal value is not expected. Furthermore, the instability problem can be avoided by using an estimation algorithm that also estimates the capacitance value [58].

Finally, a single line-to-ground fault has been simulated to evaluate the proposed measuring technique performance during current transients. Fig. 5.9(a) show the upper arm capacitor voltages and Fig. 5.9(b) the output currents during a fault in phase a, which has been applied from $t = 0.035$ s to $t = 0.105$ s. Despite the current transients, the estimation method works properly, and the capacitor voltages are well balanced at all times.

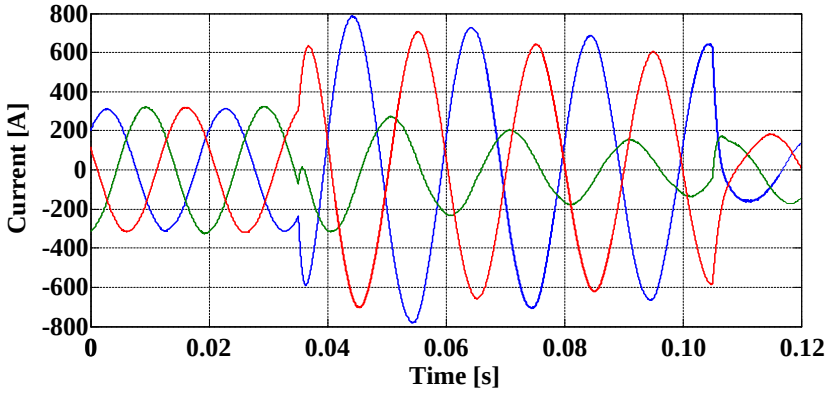
5.5 Experimental Results

The new measuring technique has been implemented and tested in the TIEG-P prototype, configured as a single-phase MMC with eight SMs per arm ($N = 8$) with an RL load. Control and modulation of the converter is performed as explained in Section 5.4, and all the results have been obtained with a modulation index of m=0.9. The main data of the prototype are given in Table 5.2.

Fig. 5.10 presents the upper arm capacitor voltages measured experimentally when using the two compared techniques: wit the individual measuring technique (Fig. 5.10(a)) and with the new measuring technique (Fig. 5.10(b)). In order fairly compare the techniques, the waveform depicted in Fig. 5.10(b) show the capacitor voltages individually measured when the system is controlled with the new measuring technique. As it can be seen, the voltages in Fig 5.10(a) present a slightly higher dispersion than those in



(a)



(b)

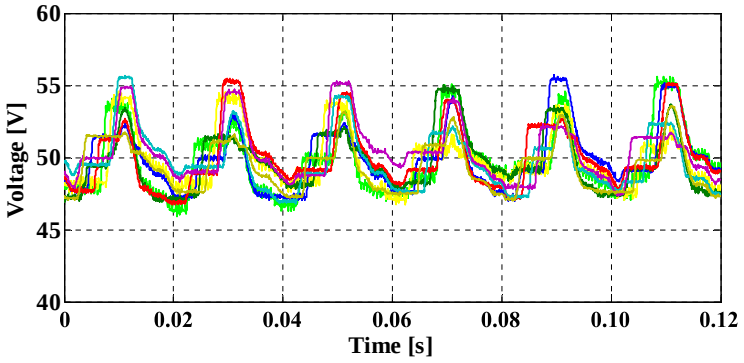
FIGURE 5.9: Simulation results using the proposed measuring technique with a single line-to-ground fault: (a) Upper arm capacitor voltages and (b) output currents.

TABLE 5.2: Specifications of the Prototype Converter used for the Measuring Technique

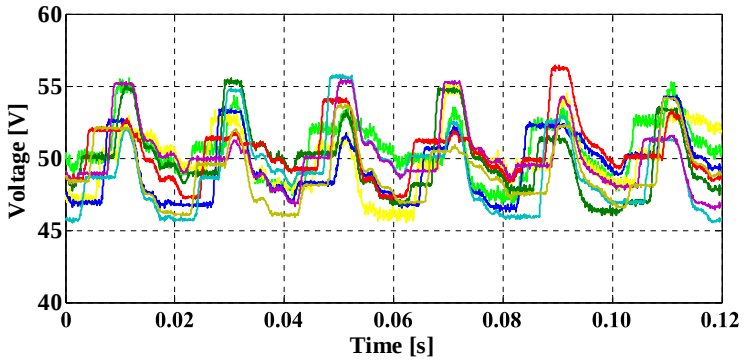
Parameter	**Value**
Number of SMs per Arm, N	8
SM Capacitors, C	1500 μF
Arm Inductors, L	3 mH
DC-Link Voltage, V_{dc}	400 V
Load Resistor, R_{out}	7 Ω
Load Inductor, L_{out}	6 mH
Carrier Frequency, f_{cr}	1.724 kHz
Sampling Frequency, f_{samp}	34.482 kHz
Output Frequency, f	50 Hz

Fig 5.10(a). However, the amplitude of the capacitor voltage ripples is not increased significantly.

With the objective of demonstrating that the new voltage measuring technique does



(a)



(b)

FIGURE 5.10: Experimental results. Upper arm capacitor voltages with individual measuring technique (a) and with the new measuring technique (b).

not present negative effects in the performance of the converter, the output voltage and currents are also presented. The output voltages obtained with the individual measuring technique and the new measuring techniques are presented in Fig. 5.11, while the output currents are presented in Fig. 5.12. No significant differences can be appreciated in the waveforms between using individual sensors and the new measuring technique. Therefore, it can be stated that the performance of the MMC with the new measuring technique is very similar to using the individual sensors per SM.

The effectiveness of the new measuring technique has been evaluated by measuring the dispersion of the capacitor voltages. The parameter to quantify such dispersion is the standard deviation of the capacitor voltages $s_N(v_{Cz})$, which is calculated for each instant of time, as follows:

$$s_N(v_{Cz}) = \sqrt{\frac{1}{N}\sum_{n=1}^{N}\left(v_{Cz(n)} - \overline{v_{Cz}}\right)^2}\,, \tag{5.3}$$

where $\overline{v_{Cz}}$ is the average value of all the capacitor voltages in the arm at that instant of time.

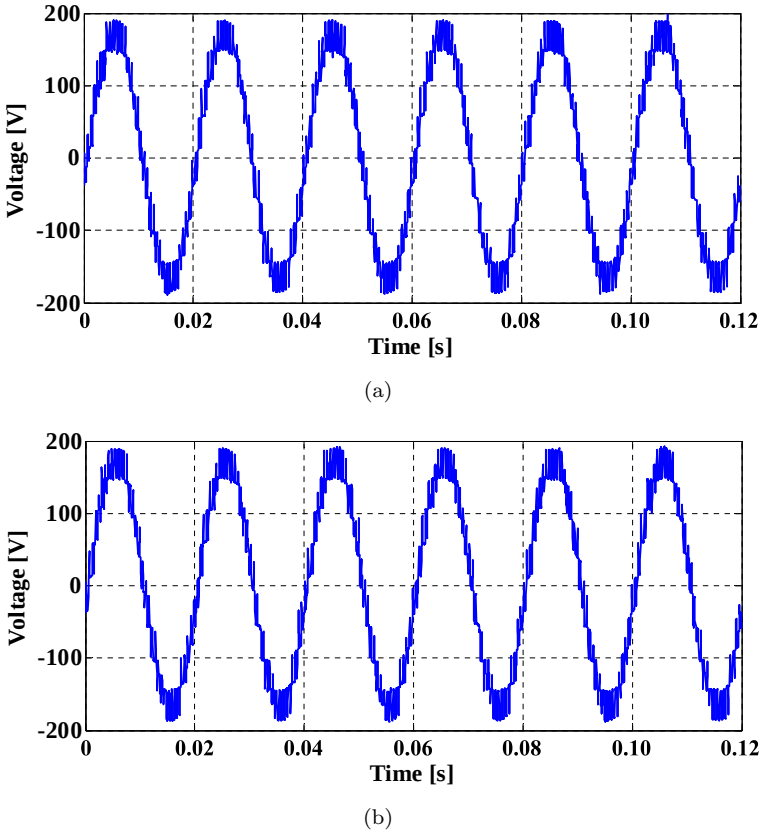
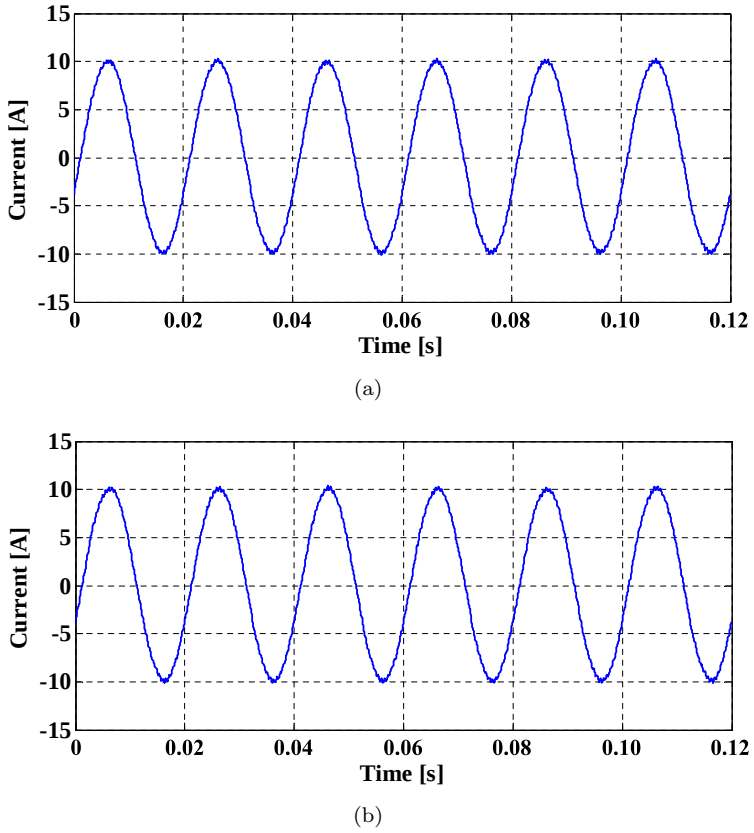


FIGURE 5.11: Experimental results. Output voltage with individual measuring technique (a) and with the new measuring technique (b).

In order to obtain an averaged value of the dispersion, the instantaneous value of the standard deviation has been averaged by a moving window of one-period width. The averaged standard deviation of the capacitor voltages obtained with the individual measuring technique and with the new measuring technique are depicted in Fig. 5.13. It can be seen that deviation curve is slightly higher with the new measuring technique, but it is still close to the individual measuring technique. The average value of the standard deviation for the whole time interval represented is 1.04 V for the individual sensors and 1.43 V for the new measuring technique.

Finally, the dynamic response of the new measuring technique is tested by applying load changes to the converter when controlled with the new measuring technique. Fig. 5.14 shows the experimental results when the resistive component of the RL load is reduced, changing from 68 Ω to 17 Ω and when it is increased, changing from 17 Ω to 68 Ω again.

Fig. 5.14(a) depicts the upper arm capacitor voltages. As it can be observed, the capacitor voltages are quickly balanced when the load resistance value is decreased. On the contrary, some more time is required to achieve voltage balance when increasing the load resistance value. This delay is due to a change in the dynamic of the voltage



(a)

(b)

FIGURE 5.12: Experimental results. Output current with individual measuring technique (a) and with the new measuring technique (b).

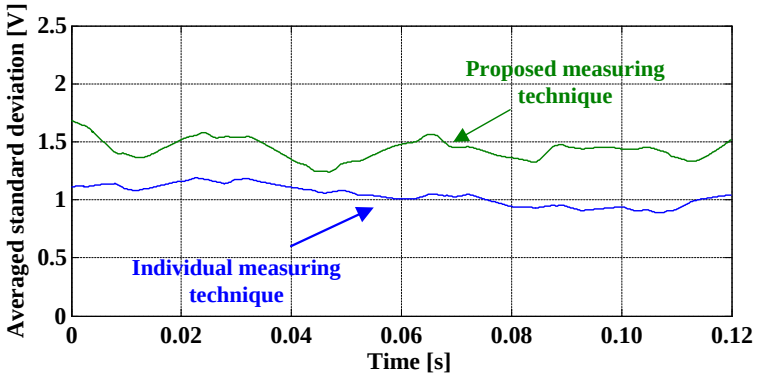


FIGURE 5.13: Averaged standard deviation of the upper arm capacitor voltages obtained from experimental results.

balancing algorithm and it has nothing to do with the proposed measuring technique. When increasing the load resistance value, the output current and the arm currents decrease, and therefore the capability of balancing the capacitor voltages is reduced accordingly. The arm currents and the output current during this process are shown in Figs. 5.14(b) and (c) respectively.

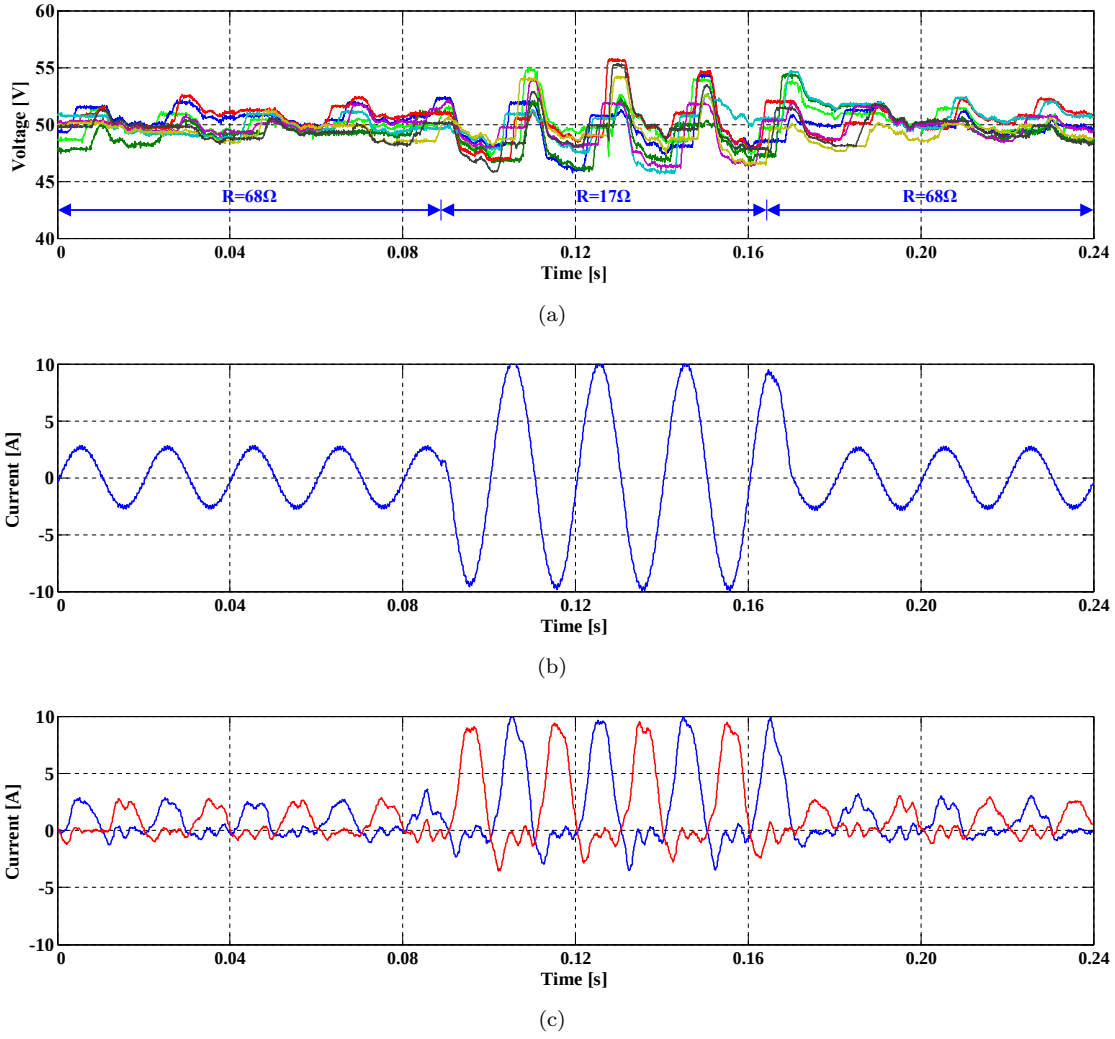


FIGURE 5.14: Experimental results using the new measuring technique with load changes: (a) Upper arm capacitor voltages, (b) upper and lower arm currents, and (c) output current.

5.6 Conclusion

In this chapter, a new capacitor voltage measuring technique for the MMC has been developed. Each sensor is able to measure the capacitor voltages of multiple SMs. The arms of the MMC are divided into sets of SMs connected in series, and each sensor measures the output voltage of one of these sets. Two sensors per arm is the minimum number required; therefore, the total number of sensors is drastically reduced, and thus also the complexity and cost of the data acquisition system. The measuring technique involves capacitor voltage estimators that are updated whenever there is an actual measurement. This is performed when only one SM in the measuring set is activated. Despite the simplicity of the estimator, the fact that the voltage values are periodically updated limits the maximum accumulated error. The technique is complemented with an enforced measuring algorithm to ensure periodical refreshment of all the capacitor

voltages. Experimental and Simulation results demonstrate that the capacitor voltage ripples increase slightly, but without compromising proper operation of the converter. This technique is especially interesting for MMCs with a large number of SMs, due to the significantly lower number of voltage sensors required.

Chapter 6

Fault Tolerant Topology

This chapter presents a fault tolerant configuration for the MMC. The procedure is able to detect faults in voltage sensors and semiconductor switching devices, and it can reconfigure the system so that it can keep on operating. Both switch and sensor faults can be detected by comparing the output voltage of a set of SMs, which is measured by a so-called supervisory sensor, with two calculated reference voltages. Faults in the supervisory sensors are also considered. Sensor faults are overcome by using the measuring technique detailed in Chapter 5. Additional SMs are included in the arms so that the MMC can bypass a faulty SM and continue operating without affecting the output voltage of the phase-leg.

6.1 Introduction

Reliability is one of the most important challenges in MMCs, since they include many switching devices, which are the weakest components in power converters [63]. For this reason, the development of fault-tolerant converter topologies and strategies are relevant research topics nowadays. Multiple studies analyze their reliability and provide solutions to faults on the dc side [59–61] and ac side [62] of the converter. Control techniques under SM faults have also been investigated based on including additional SMs in the arms of the converter. Redundancy is a characteristic inherit to the modular structure of the MMC, and the number of SMs can be easily increased in order to substitute faulty SMs [64–66].

In the case of a component failure, the fault must be detected and localized. In some faults, like an open-circuit fault in a switching device, the capacitor voltage of the faulty SM may increase, which could cause further damage to the MMC. Given the large

number of identical SMs and the symmetrical structure of the converter, localization of a faulty SM is challenging. Some fault detection techniques are based on using additional sensors for each switching device [67], SM [68], or using driver modules with integrated fault detection functions [69]. However, these techniques imply a high increase in the converter cost and complexity.

Recently, new fault detection techniques have appeared based on observers and estimators. In [70], a sliding mode observer-based fault detection method was proposed. The same observer was improved in [71], increasing the robustness and reducing the fault detection time. The method is based on comparing the measured circulating current values with the values calculated by a sliding mode observer. This detection and localization method is robust and does not require the use of additional sensors, however it performs relatively slowly (the minimum localization time is 50 ms), and only detects open-circuit (OC) faults in the switching devices. In [72], a detection and localization method based on a Kalman filter is presented. The proposed technique compares the measured voltage and current values with the estimated ones using a Kalman filter. The technique is capable of detecting multiple faults at the same time, but it is still slow, with an average time of over 100 ms. Furthermore, it only detects OC faults.

In this chapter, the fault detection and localization technique presented in [127] is detailed. The technique is based on dividing the arms in a minimum of two sets of SMs, and adding voltage sensors to measure the output voltage of each set of series-connected SMs. The technique only requires three additional sensors per arm and is capable of detecting and correcting OC faults, short-circuit (SC) faults, and also voltage sensor faults, which is a kind of fault that has not been studied much in the existing literature.

The detection and localization process follows three main steps: detection, localization and correction. In steady-state, the fault detection method supervises the system. Supervision consists on comparing the voltage of the additional sensors with a calculated reference. When the measured and reference voltages do not coincide, a fault is detected and its kind identified. Then, the fault localization method is initiated. This step is composed by multiple algorithms, since each kind of fault requires a different localization process. In summary, localization is based on checking if the fault is detected each time a SM is deactivated. When the fault disappears, the fault is localized on the last activated or deactivated SM. Finally, when the fault is localized, the faulty sensor is substituted by the alternative measuring system (Chapter 5) or the faulty SM is bypassed. The overall technique does not require intensive processing and provides a fast response, detecting and localizing faults generally in less than 5 ms.

6.2 Redundant Sensors and Additional SMs Topology

The topology of the fault detection technique includes additional sensors and SMs in order to detect and solve two kinds of faults: a fault in a voltage sensor and a fault in an SM switching device. Faulty sensors provide a constant output value that is normally zero, and faults in the SMs can be classified as SC and OC faults in both the upper and lower power switches of the half-bridge SMs. All the faults are considered permanent. Faults in the diodes are not differentiated from faults in the controlled devices (IGBT or MOSFET). The performance of the SM with a SC fault in a diode is the same as with a SC fault in a controlled device. On the other hand, OC faults in the diodes must be detected indirectly. Since the MMC arms are highly inductive circuits, an OC fault in a diode will block the current path, which may cause a short-circuit break to another device.

Each arm is divided into nS sets of SMs, each one composed of nM series-connected SMs. Fault detection is achieved by using additional voltage sensors (Fig. 6.1) that measure the output voltage of the sets of SMs, $v_{Sz(k)}$, where z identifies the upper or lower arm ($z \in \{u, l\}$) and k the number of the set. The voltage provided by each supervisory set sensor is compared with a reference value for fault detection. It is also used to substitute faulty individual SM voltage sensors by applying the measuring algorithm presented in [124] and detailed in Chapter 5. A circuit diagram of the proposed fault-tolerant topology is depicted in Fig. 6.1. For the sake of simplification, this chapter is explained for a single-phase converter, excluding the phase identifier j from the mathematical analysis and block diagrams.

Faults in the supervisory set sensors are also considered. In order to check their performance and substitute them when faults appear, a third sensor is used: the so-called supervisory arm sensor. This sensor measures the voltage provided by all the series-connected SMs of the arm (v_{Az}) and should be equal to the sum of all the supervisory set sensors, i.e.:

$$v_{Az} = \sum_{k=1}^{nS} v_{Sz(k)} \ . \tag{6.1}$$

If a supervisory set sensor fails, it can simply be disabled and its value will be measured indirectly. By subtracting the voltage of all the correct supervisory set sensors from the supervisory arm sensor, the value of the faulty sensor is obtained. The supervisory arm sensor is the only sensor that cannot be substituted. If a fault appears in this sensor, the system loses the fault localization capability, since when a new fault is detected, it is impossible to check if it has occurred in a SM or individual sensor or in a supervisory set sensor.

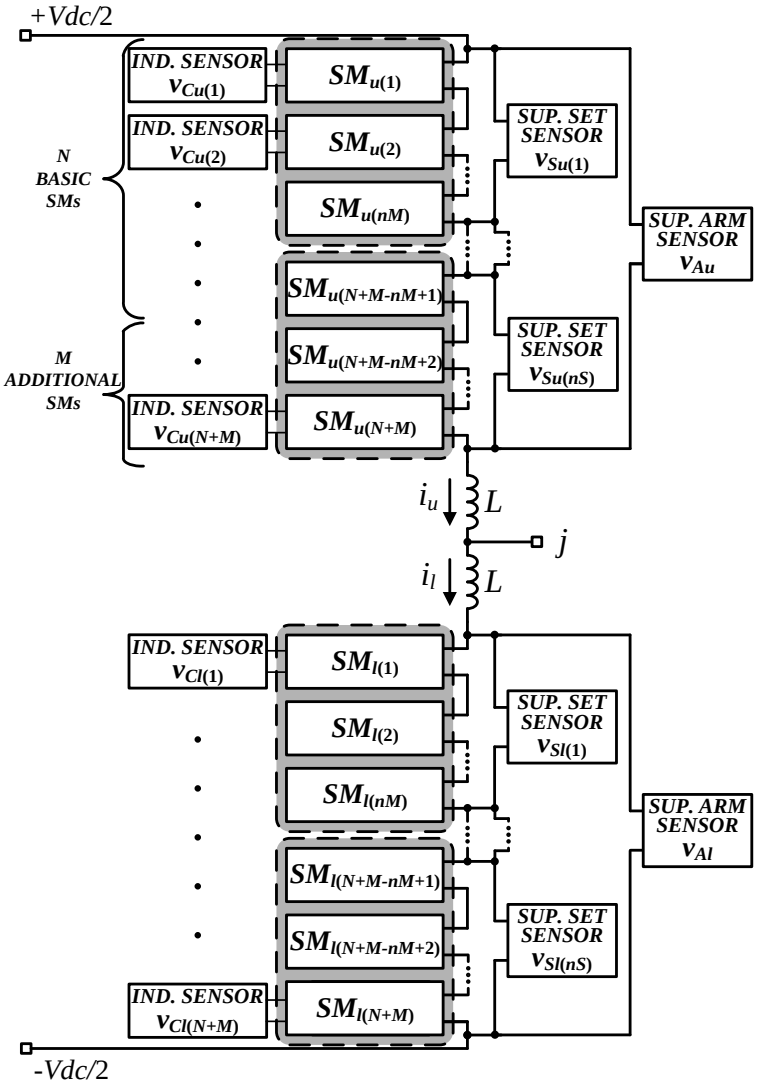


FIGURE 6.1: Distribution of the supervisory sensors and the redundant SMs.

The minimum number of sets per arm (nS), and therefore the number of additional supervisory set sensors, is two. The minimum number of sets is defined by the voltage measurement technique used to substitute faulty sensors (Chapter 5), and by the supervisory arm sensor checking, which is based on comparing its value with the two different supervisory set sensors. However, the number of sets and sensors can be increased if required. A low number of sensors per arm reduces the cost of the converter and improves its reliability, since the number of devices that can fail is lower. On the other hand, a higher number of sensors per arm requires lower accuracy of the sensors and allows higher noise margins, since the voltage of one SM has to be higher than the error margin of the set sensor. Moreover, the cost and voltage limitations of each sensor should be taken into account when defining the number of sets. Reducing the number of sets reduces the number of sensors and the cost of the measuring system, but it also increases the maximum voltage applied to each of the sensors.

In order to be able to reconfigure the MMC under switch faults, SM redundancy is provided. This redundancy is achieved by adding a number M of additional SMs to the N basic ones in the arms. In this implementation, the redundant SMs are also active, which, in addition to provide redundancy, it helps to reduce the capacitor voltage ripples during normal operation mode [64]. When a fault in a switching device is detected, it is corrected by simply disabling and short-circuiting the SM. Disablement is performed by considering the faulty SM the one with less priority in the voltage balancing algorithm, preventing it to be activated anymore. Moreover, the SM is short-circuited by an external device, i.e., a high-speed by-pass switch or thyristor [4].

6.3 Fault Detection Method

The proposed fault detection method is based on comparing the voltage measured by the supervisory set sensors, $v_{Sz(k)}$, with a calculated reference. Two different reference voltages are calculated, one for detecting sensor and OC faults, and another for detecting SC faults. The first reference signal, which is named *expected voltage* ($v_{Sz(k)\,exp}$), is calculated as the sum of the voltages of the activated SMs:

$$v_{Sz(k)\,exp} = \sum_{n=nM(k-1)+1}^{nMk} s_{z(n)} v_{Cz(n)} \ , \tag{6.2}$$

where n is the SM identifier, with $n \in \{1, ..., N+M\}$, $s_{z(n)}$ is the state of the SM, and $v_{Cz(n)}$ is the SM capacitor voltage.

The second reference signal, $v_{Sz(k)\,t}$, is named *theoretical voltage*. It consists of the product of the number of activated SMs and the average value of the voltages of all the SMs in the arm:

$$v_{Sz(k)\,t} = \sum_{n=nM(k-1)+1}^{nMk} s_{z(n)} v_{Czavg} \ , \tag{6.3}$$

where

$$v_{Czavg} = \sum_{n=1}^{N+M} \frac{v_{Cz(n)}}{N+M} \ . \tag{6.4}$$

If the measured voltage $v_{Sz(k)}$ and the calculated reference signals, $v_{Sz(k)\,exp}$ and $v_{Sz(k)\,t}$, are different, a fault is detected. Variables $e_{exp\,z(k)}$ and $e_{t\,z(k)}$ represent the difference between the measured voltage and the expected and theoretical voltages, respectively:

$$e_{exp\,z(k)} = v_{Sz(k)} - v_{Sz(k)\,exp} \ \text{ and} \tag{6.5}$$

$$e_{t\,z(k)} = v_{Sz(k)} - v_{Sz(k)\,t} \ . \tag{6.6}$$

Due to nonidealities, the error values are always different from zero. For this reason, a fault is considered only when the error values are higher than a threshold value. Threshold values cannot be defined theoretically, since they depend on multiple factors like voltage sensors noise, sensors accuracy and voltage drops in the switching devices and connections. For this reason, the threshold values should be adjusted empirically. For the results obtained in this chapter, the threshold of the *expected error* has been adjusted to a value of 20% of the capacitor nominal voltage (V_{dc}/N). The *theoretical error* is also affected by the capacitor voltage imbalance, as it is calculated from the average capacitor voltage value of the SMs in the arm. Therefore, the threshold value of the theoretical error should be higher than the threshold of the expected value. In this chapter, a value of 50% of the capacitor nominal voltage has been adopted.

Faults are only detected in one specific switching state of the SM (on or off, depending on the kind of fault). Consequently, a significant delay may exist between the moment the fault appears and its detection. In order to reduce this delay, a second mechanism is used for detecting faults. The mechanism, known as alarm indicator, consists in comparing the values of the individual sensors with pre-fixed limit values at each sampling period. If an individual sensor provides a value too high or too low, the alarm indicator for that SM is activated. In order to distinguish between faults and capacitor voltage ripples that appear during normal operation of the converter, the upper limit is defined near the maximum value allowed to the capacitor voltages and the lower limit is defined close to zero.

6.3.1 Supervisory Sensor Fault Detection

Differences between the measured and the calculated voltages correspond to faults in SMs or sensors only if the supervisory set sensor measurement is correct. For this reason, the correct performance of the supervisory set sensor is checked at each sampling period.

The correct performance of the supervisory sensors is verified by comparing the sum of the supervisory set sensor voltages $v_{Sz(k)}$ with the voltage of the supervisory arm sensor v_{Az}. If the difference is within a tolerance margin (small errors are expected due to noise and sensor accuracy), then the supervisory set sensor voltages and calculated voltages are compared. Otherwise, the process for localizing the faulty supervisory sensor is initiated.

6.3.2 Voltage Sensor Fault Detection

The results obtained in this chapter are based on a voltage sensor with a resistive input impedance is used, and faults are emulated as an open-circuit at the linking cable between the SM and the voltage sensor. Therefore, when a fault appears, the measured voltage decreases rapidly to zero. Most times, the sensor faults are detected through the alarm mechanism, but comparisons of measured and calculated voltages are still required. If a different sensor topology were used, the fault process might be different, but the detection method would not require many modifications.

When an SM with a faulty sensor is activated, a significant difference appears between the expected and the measured voltage. The measured voltage is the sum of the voltages of the activated SMs, including the one with the faulty SM, which has a voltage value close to the other SM voltage values. In contrast, the expected voltage considers the voltage measured by the faulty individual sensor, which is lower than the others.

The difference between the measured and the expected value does not appear in the theoretical error. The measured voltage is very similar to the theoretical voltage, as the second one considers the average voltage of all the SMs for the SM with the faulty sensor, which is close to the real value. The variation of the average voltage value due to the faulty sensor is not significant enough to detect an error, since the average is performed by considering all the SMs in the arm.

If the sensor voltage drops too fast or the SM is deactivated when the fault appears, the fault is detected through the minimum voltage alarm. However, a comparison between the measured and calculated voltages is also required in order to differentiate between sensor and SM faults.

6.3.3 SM Fault Detection

SM faults considered in this paper are faults in controlled switching devices, which can be both OC and SC faults. Considering that only one fault appears at the same time, there are four kinds of faults, each one with its own dynamics: OC in the upper switch, OC in the lower switch, SC in the upper switch, and SC in the lower switch. OC and SC faults can be detected and differentiated through the error of expected and theoretical voltages. Fig. 6.2 depicts the circuit diagram of each fault equivalent circuit and current flow path, depending on the SM state and the current direction.

OC faults are detected when the current should pass through the open-circuited semiconductor but, due to the fault is forced to pass through the opposite switch diode.

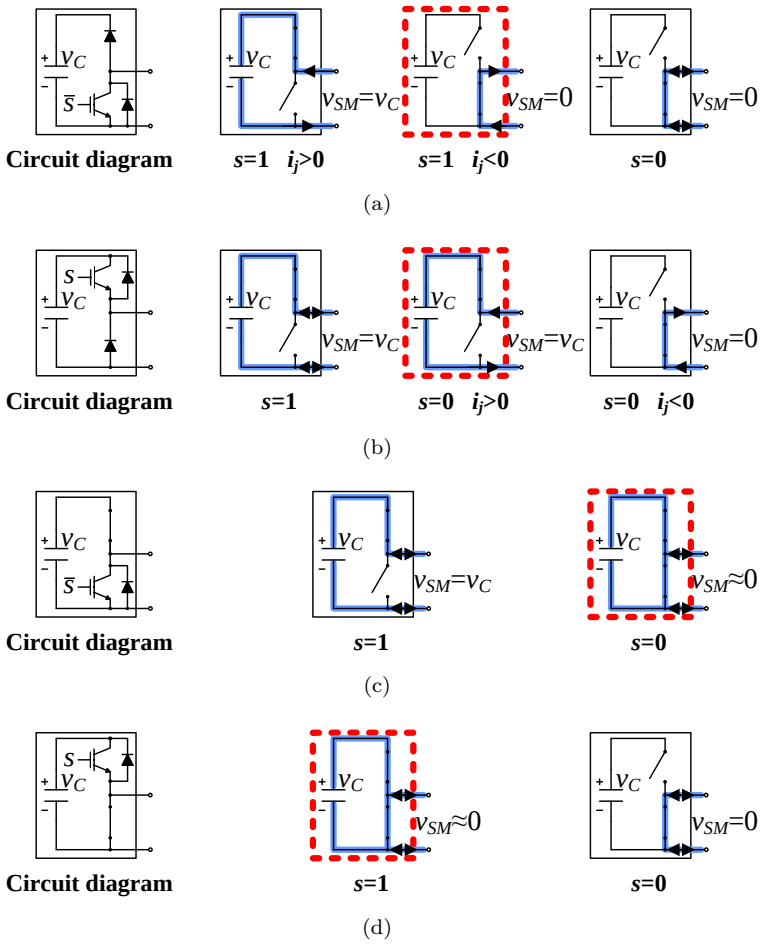


FIGURE 6.2: Circuit diagram and current path for each kind of SM fault: (a) upper switch OC, (b) lower switch OC, (c) upper switch SC and (d) lower switch SC.

For example, in an upper switch OC fault, if the current is negative when the SM should be activated, the current cannot circulate through the transistor and is forced to flow through the lower diode. This provides zero volts at the output of the SM instead of the capacitor voltage. In this situation, a negative error appears in both the expected voltage value and the theoretical voltage value, as the measured voltage is lower than the calculated voltages. The flow path of the current can be observed in Fig. 6.2(a).

When an OC fault occurs in a lower switch, the opposite happens: when the SM should be deactivated and the current is positive, the OC forces the current to flow through the diode of the upper switch (Fig. 6.2(b)). In this case, the SM provides the voltage of the capacitor instead of zero volts, causing a positive error in both the expected and theoretical errors.

There is not much difference between the upper and lower switches in SC fault detection, therefore they are not differentiated. When an SC fault appears and the opposite switch is activated, the capacitor is short-circuited and rapidly discharged.

TABLE 6.1: Summary of the Fault Detection Method

Fault	$v_{Sz(k)} > v_{Sz(k)\ exp}$	$v_{Sz(k)} < v_{Sz(k)\ exp}$	$v_{Sz(k)} \neq v_{Sz(k)\ t}$
Individual sensor fault	Yes	No	No
Upper switch OC SM fault	No	Yes	Yes
Lower switch OC SM fault	Yes	No	Yes
SC SM fault	No	No	Yes

Considering a similar resistance in the short-circuited switch and the on-state switch, the voltage provided at the output is half the capacitor voltage, whose value is very low. SC faults are detected by the theoretical error, as the value provided by the SM (almost zero) is much lower than the calculated one (the average value of all the SMs). However, no error is detected in the expected value, as the measured voltage value is very low, and so it is in the calculated value (although an error exists, it is not significant enough to be considered a fault). When an SC appears in the upper switch, the capacitor is discharged during the off-state of the SM, but the fault is detected when activating it. Conversely, if an SC fault is produced in the lower switch, the fault is detected in the on-state of the SM, while the capacitor is being discharged.

A summary of the SM and sensor faults and their detection methods is shown in Table 6.1.

6.3.4 Alarm Indicator and Enforced Activation Method

If the voltage seen by the individual sensor reaches the nominal bounds (i.e., too high or too low), an alarm indicator is activated. This indicator facilitates detection and localization of the fault, as the SM where the alarm has been activated is where the fault was produced. When an alarm indicator is triggered in an activated SM (or the origin of the alarm is a lower switch OC fault), the voltage measured by the supervisory set sensor will be different from the expected and theoretical voltages and the kind of fault will be detected immediately. However, if an alarm indicator of a deactivated SM is triggered, the expected and theoretical voltages are not modified, and hence the kind of fault cannot be detected and corrected. In order to identify the fault as soon as possible, the SM is forced to be activated through the enforced activation method.

The enforced activation method is an adapted version of the enforced activation algorithm explained in Subsection 5.3, an algorithm that modifies the activation priority of the SMs without affecting the output voltage of the converter. The SMs whose priority wants to be modified are indicated in the *enforcing vector*. This vector is scaled with the

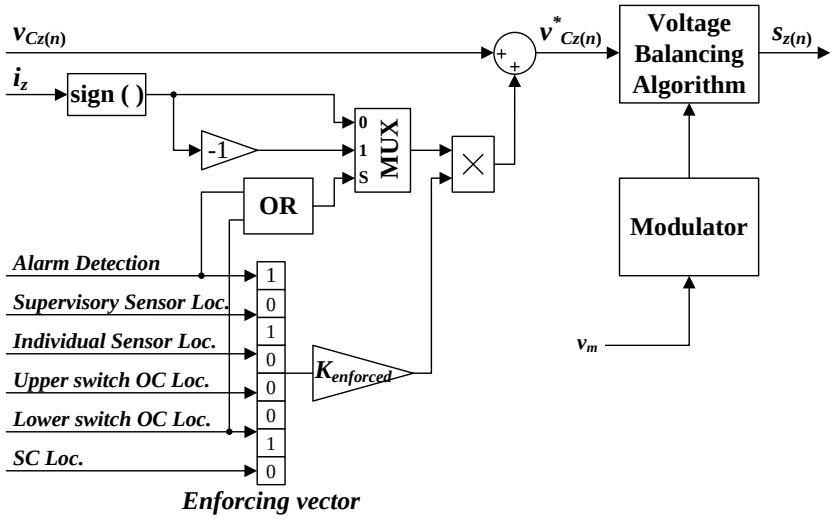


FIGURE 6.3: Block diagram of the enforced activation method.

gain $K_{enforced}$ and added as an offset to the measured capacitor voltage values. When the indicated SMs have to be deactivated, the sign of the offset is the same than the sign of the arm current. However, algorithms like fault detection by alarm indicator and lower switch OC fault localization, require activating the specified SMs. In this situation, the offset is added with the opposite sign than that of the arm current. A block diagram of this enforced activation method is depicted in Fig. 6.3.

6.4 Fault Localization Method

After detecting a fault, the faulty SM or sensor has to be determined. Each kind of fault has its own localization method, therefore different algorithms have to be executed, depending on the fault origin. A state machine has been implemented to manage all the processes related to fault detection and localization. The detection and localization system has nine different states:

- State 0 - Initialization.
- State 1 - Supervision: Check of the supervisory sensors as well as expected and theoretical errors.
- State 2 - Alarm Detection: Identification of the fault type when an alarm indicator is activated.
- State 3 - Supervisory Sensor Fault Localization.
- State 4 - Individual Sensor Fault Localization.

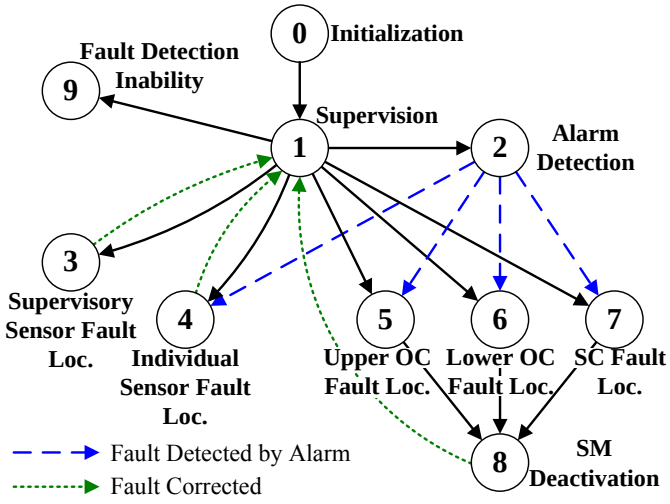


FIGURE 6.4: Diagram of the state machine.

- State 5 - Upper Switch OC Fault Localization.
- State 6 - Lower Switch OC Fault Localization.
- State 7 - SC Fault Localization.
- State 8 - SM Deactivation: Used to ensure deactivation of a faulty SM before returning to the supervision system.
- State 9 - Fault Detection Inability: After a supervisory arm sensor fault, the performance of supervisory sensors cannot be checked, and therefore it is impossible to identify the kind of fault detected by the supervision state (not coming from an alarm indicator).

The state machine diagram is detailed in Fig. 6.4. The detection system starts with the Initialization State or State 0, which is used only before achieving the steady-state performance of the system. Once the system has started, it stays in the Supervision State, looking for faults in the sensors or in the SMs.

When a fault is detected, the state machine goes to the corresponding localization method. If the fault is detected by an alarm indicator, the detection system changes from Supervision State to Alarm Detection State before starting a localization method. Both Supervisory Sensor Fault Localization and Individual Sensor Fault Localization States localize and correct the fault and return to the Supervision State.

In contrast, the SM Fault Localization States change to the SM Deactivation State after localizing a fault. This state waits for the next capacitor voltage balancing algorithm

sampling period before returning to the Supervision State, since the slower sampling period of this algorithm cannot ensure the immediate deactivation of the faulty SM after its localization.

Fault Detection Inability State or State 9 is activated only when a fault has been previously detected in the supervisory arm sensor and a fault is now detected in the Supervision State. The new fault cannot be identified because the correct performance of the supervisory set sensors cannot be checked; consequently, it cannot be corrected. This state finishes the fault detection and localization processes until the faulty sensor is fixed and the system has restarted.

6.4.1 Supervisory Sensor Fault Localization

When a fault in a supervisory sensor is detected, the system changes to State 3, and looks for the faulty supervisory sensor. The localization method consists of comparing all the supervisory set sensors with the supervisory arm sensor when their values should be the same. That is, when all the activated SMs are in the compared set and all the SMs of the other sets are deactivated.

Under proper operation of the voltage sensors, the supervisory arm sensor and the supervisory set sensor should provide the same voltage value. However, since an error has been detected, one or more of the comparisons will be different and the faulty sensor will be detected. If only one of the comparisons is different, the compared supervisory set sensor is the faulty one. On the contrary, if all the comparisons are different, the faulty sensor is the supervisory arm sensor.

Activation or deactivation of all the SMs in a Set is performed through the enforced activation method. In order to deactivate all the SMs in a set, the number of on-state SMs in the arm has to be equal or lower than the number of SMs in a set. Since this situation is only available during half a period, the enforced activation method will not be activated until the number of activated SMs is the required, that is, until the modulation signal is positive for the upper arm or negative for the lower arm. This limitation reduces the time where the enforcement is activated, and therefore, the capacitor voltage imbalances.

6.4.2 Sensor and SM Fault Localization

The localization methods for sensor faults and SM faults are very similar. In fact, they use the same pattern, but the analysed variables and the applied solutions are different for each localization method.

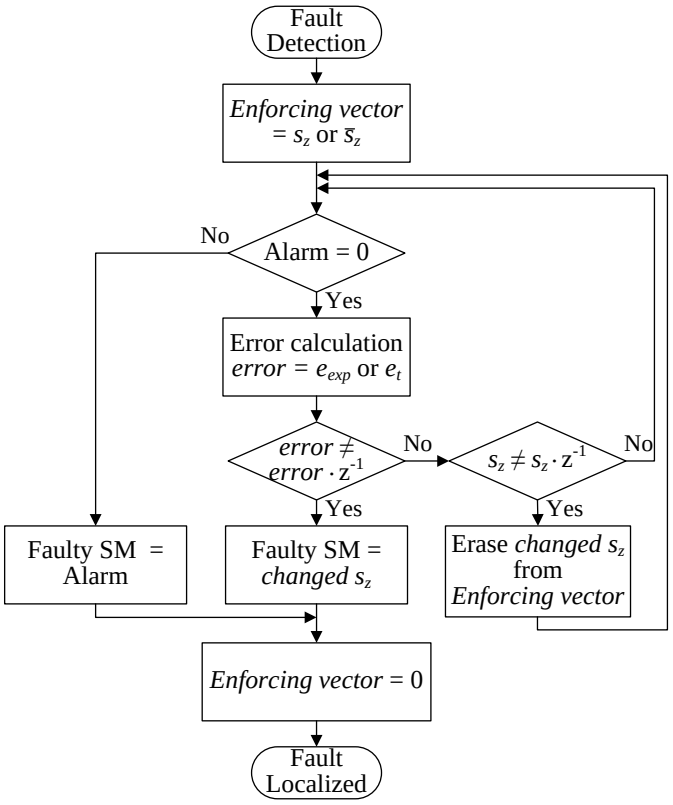


FIGURE 6.5: Flowchart of the localization method.

The localization method is based on looking for a change in the value of the error when the SM where the fault is located changes its state. As an error has been detected just before activating the localization method, the faulty SM is in the state that causes the error to be larger than the threshold value when the localization process starts. When the error disappears, the last changing SM corresponds to the one with the fault. If the fault has been detected from an alarm or an alarm appears during the localization process, the origin of the alarm is automatically assigned as the faulty SM. A flowchart of the localization method algorithm is depicted in Fig. 6.5.

In order to accelerate the process, the enforcing activation method is used. Taking into account the dynamic of each fault, the SMs in the set that are in the faulty state (activated or deactivated) are forced to change. Each time one of the targeted SMs changes its state without changing the error significance, that SM is eliminated from the vector of SMs to be forced.

The differences between the localization methods are mainly the checked error and the forced change of state. In the sensor fault localization method, the expected error $e_{exp\,z(k)}$ is the variable that is tracked for a change, and the activated SMs are forced to be deactivated.

The same changes are searched for in the upper switch OC localization method; but due to the fault dynamics, the error change is checked only when the current is negative. Also, the SMs are eliminated from the enforcing list only when they change with negative current. The dynamic characteristics of OC faults are explained in Subsection 6.4.3.

Lower switch OC faults are also localized from a change in the expected error, which is detected when a faulty SM is deactivated. Therefore, the SMs are forced to be activated. Error change detection is only validated when the current is positive.

Finally, SC faults are localized through a change in the theoretical error $e_{t\,z(k)}$ in both current directions. Due to the rapid discharge of the SMs, SC faults are often localized by an alarm indicator.

6.4.3 OC Fault Dynamics

Open-circuit faults can be detected for only one direction of the arm current. The upper switch OC faults appear only when the current is negative, and lower switch OC faults appear with positive current. This fact reduces the opportunities to localize the fault, as a change in the error variable means that the faulty SM has been deactivated only if the change is produced with the correct current direction.

Moreover, OC faults modify the internal dynamics of the arm currents. In upper switch OC faults (which are detected when the arm current is negative), the fault reduces the voltage generated by the arm. The change in the applied voltage increases the voltage in the arm inductors and the arm current. If the power flows from the dc side to the ac side of the MMC, the arm current is mostly positive. Consequently, the increase in the arm current can change the direction of the arm current from negative to positive. This change in the arm current to positive causes the effects of the fault to disappear, provoking an oscillating dynamic around zero during the negative part of the arm current.

The oscillating dynamics make localizing OC faults very difficult, as the expected error continuously appears and disappears. With the purpose of reducing the oscillating dynamics and detecting the upper switch OC fault, the circulating current reference is modified, forcing a negative arm current. This modification consists on adding a gain in the circulating current reference when it is negative, and hence increasing the negative differential control signal.

Lower switch OC faults have an opposite effect, reducing the arm current when it is positive. If the power flows from the dc side to the ac side of the converter, the positive part of the arm current is large enough to avoid an oscillating dynamic. However, if the

power flows from the ac side to the dc side, an oscillating dynamic may also appear. Therefore, under this kind of fault, the current reference is modified in the opposite direction, forcing a positive arm current. It should be highlighted that the circulating current reference modification is only applied during OC fault localization algorithms.

6.5 Reliability Analysis

Reliability improvement achieved with the fault-tolerant topology studied in this chapter can be demonstrated numerically. Assuming different failure rate values for the switching devices and the voltage sensors, the total failure rate of one arm of the MMC has been calculated. Failure rate for the whole SM (λ_{SM}) has been assumed to be 100 failures per year and 10^5 hours of operation. Failure rate for the individual sensors (λ_I), supervisory set sensors (λ_S) and supervisory arm sensors (λ_A) are assumed to be 10, 15 and 20 failures per year and 10^5 hours, respectively. The supervisory sensors have a higher failure rate due to the higher nominal voltage requirements.

The total failure rate of a system [63,128,129], is calculated through the combination of individual reliability functions $R(t)$. Once the total reliability function is obtained, the mean time to failure (MTTF) is calculated, and also the failure rate obtained as the inverse of MTTF. The main equations are as follows:

$$R(t) = \mathrm{e}^{-\lambda t} \,, \tag{6.7}$$

$$MTTF = \int_0^\infty R(t)\,\mathrm{d}t \text{ and} \tag{6.8}$$

$$\lambda = \frac{1}{MTTF} \,. \tag{6.9}$$

In this paper, three MMC configurations are considered and compared:

- A basic MMC without any fault detection system ($R(t)_{Basic}$). Since this topology is not able to detect and localize faulty devices, the faulty SMs cannot be disabled. Therefore, the whole converter fails after any simple fault of the SMs or of the individual sensors. The reliability of this configuration is calculated as the product all the devices reliability function, what is equivalent to add the failure rates:

$$R(t)_{Basic} = R(t)_{SM}^{N+M} \cdot R(t)_{I}^{N+M} = \mathrm{e}^{-(N+M)(\lambda_{SM}+\lambda_I)t} \,. \tag{6.10}$$

- An MMC with a fault-tolerant system based on estimators [70–72] ($R(t)_{Est}$). This configuration is able to detect, localize and bypass M faulty SMs, but not individual sensor faults. Therefore, a failure of the system is produced after $M+1$ SM faults or after a sensor fault. Equations for calculating the reliability of a system with some redundancy are obtained from [63, 128]. The reliability function of all the SMs is multiplied by the reliability function of the sensors, because one simple fault of them causes failure of the entire converter.

$$R(t)_{Est} = \left(\sum_{r=N}^{N+M} \frac{(N+M)!}{r!(N+M-r)!} \left(\mathrm{e}^{-\lambda_{SM} t} \right)^{r} \cdot \left(1 - \mathrm{e}^{-\lambda_{SM} t} \right)^{(N+M-r)} \right) \cdot \mathrm{e}^{-(N+M)\lambda_I t} \,. \tag{6.11}$$

- An MMC with the fault-tolerant topology studied in this chapter, based on additional sensors ($R(t)_{Add}$). The proposed system can tolerate M faulty SMs, and failure of all the individual sensors. However, it loses its fault-tolerant capability after the fault of the supervisory arm sensor or the fault of two supervisory set sensors. For the sake of simplification, these conditions are considered as a failure of the entire system. Therefore, the total reliability function is calculated as the product of the reliability of all the SMs, the reliability of the supervisory set sensors (which can tolerate one fault) and the reliability of the supervisory arm sensor:

$$R(t)_{Add} = \left(\sum_{r=N}^{N+M} \frac{(N+M)!}{r!(N+M-r)!} \left(\mathrm{e}^{-\lambda_{SM} t} \right)^{r} \cdot \left(1 - \mathrm{e}^{-\lambda_{SM} t} \right)^{(N+M-r)} \right) \cdot \mathrm{e}^{-(N+M)\lambda_A t} \cdot \left(nS\mathrm{e}^{-(nS-1)\lambda_S t} - (nS-1)\mathrm{e}^{-nS\lambda_S t} \right) \,. \tag{6.12}$$

The failure rates have been calculated for three different MMC configurations: (i) $N = 7$ and $M = 1$, (ii) $N = 7$ and $M = 3$, and (iii) $N = 20$ and $M = 5$. In the proposed topology, two supervisory set sensors per arm are used ($nS = 2$). The results shown in Table 6.2 demonstrate that the proposed technique highly reduces the failure rate of the converter. Reliability is mainly provided by the tolerance to SM faults, since the estimator-based fault-tolerant MMC also presents a low failure rate. However, tolerance to sensor faults also increases the reliability. The reliability improvement of the proposed technique is more significant as the number of SMs increases, since the reliability of the proposed system is independent of the number of individual sensors.

TABLE 6.2: Reliability Comparison of Different Fault-Tolerant MMC Configurations. Converter Failures per Year and 100,000 Units

	$N = 7, M = 1$	$N = 7, M = 3$	$N = 20, M = 5$
Basic MMC without Fault Detection Capability	880.0	1100	2750
Estimator-based Fault-tolerant MMC	434.4	275.0	531.6
Additional Sensors Fault-tolerant MMC	389.0	222.1	384.9

TABLE 6.3: Specifications of the Laboratory Prototype for the Fault-tolerant System

Parameter	**Value**
Number of Basic SMs per Arm, N	7
Number of Additional SMs per Arm, M	1
Number of Supervisory Set Sensors per Arm, nS	2
SM Capacitors, C	1500 μF
Arm Inductors, L	3 mH
DC-link Voltage, V_{dc}	400 V
Carrier Frequency, f_{cr}	1.25 kHz
Output Frequency, f	50 Hz
Load Resistor, R_{out}	17 Ω
Load Inductor, L_{out}	6 mH

6.6 Experimental Results

The fault-tolerant topology and detection method have been tested experimentally. The results have been obtained in the TIEG-P prototype configured as a single-phase MMC operating over an RL load. The arms of this prototype are composed of seven basic SMs ($N = 7$) and an additional one ($M = 1$). Each arm has been divided into two supervisory sets ($nS = 2$), of which each one supervises four SMs ($nM = 4$). All tests have been performed with a modulation index $m = 0.7$. Characteristics of the experimental set are in Table 6.3.

The effectiveness of the fault detection and localization technique is demonstrated by testing the system response for almost all the considered sensor and SM faults.

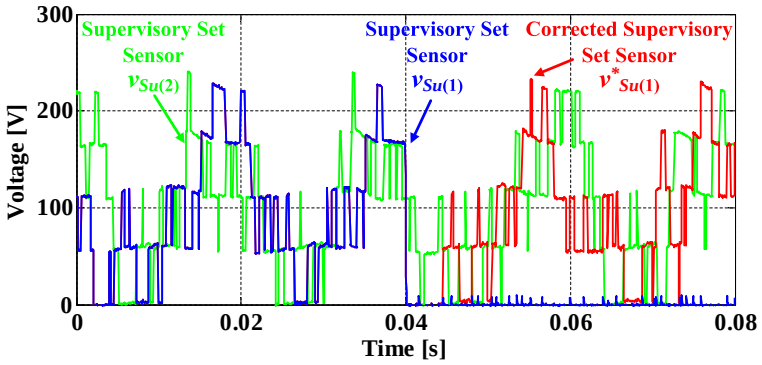


FIGURE 6.6: Experimental results when a fault appears in the upper arm supervisory set sensor $v_{Su(1)}$: voltage of the first supervisory set sensor $v_{Su(1)}$, substituted voltage of the first supervisory set sensor and voltage of the second supervisory set sensor $v_{Su(2)}$.

6.6.1 Supervisory Set Sensor Fault

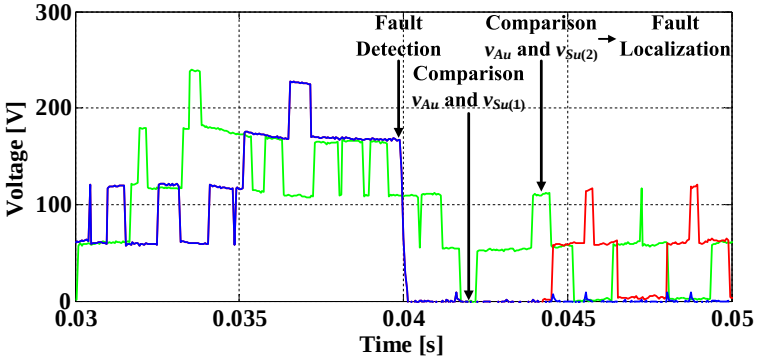
The first fault is tested in an upper arm supervisory set sensor, $v_{Su(1)}$. The fault is produced by opening a relay that is in series with the sensor. Fig. 6.6 shows the voltages of the upper arm supervisory set sensors when a fault appears. The voltage $v_{Su(1)}$ drops to zero at time $t = 0.04s$, but when the fault is localized shortly afterwards, the measured value is substituted by the calculated value $v^*_{Su(1)}$.

Fig. 6.7 depicts the localization process in detail. Fig. 6.7(a) depicts the supervisory set sensor voltages and the supervisory arm sensor voltage. The fault is detected just immediately after it appears, as the sum of the supervisory sensor voltages does not equal the supervisory arm sensor voltage. Then, the supervisory sensor fault localization process (State 3) is initiated. The instants when each of the supervisory set sensors and the supervisory arm sensor are compared can be seen in Fig. 6.7(a). The system state is depicted in Fig. 6.7(b).

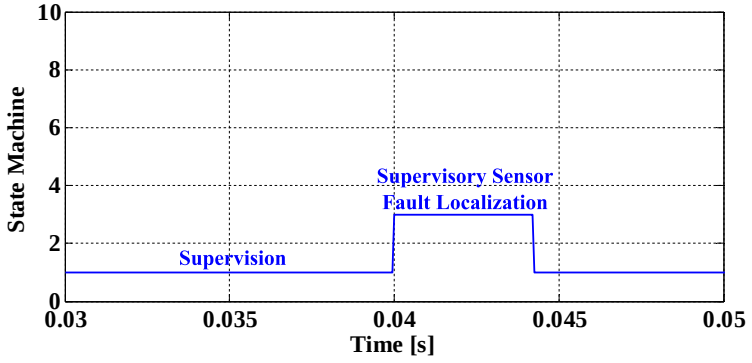
6.6.2 Individual Sensor Fault

Figs. 6.8 and 6.9 show the experimental results from forcing a fault in an individual sensor. Fig. 6.8(a) depicts the measured capacitor voltages when a fault appears on sensor $v_{Cu(2)}$ at time $t = 0.01s$. The fault is rapidly detected and the estimation algorithm substitutes the individual sensor. In Fig. 6.8(b), it can be seen how the estimated voltage is close to the other capacitor voltages. With the aim of having a reference value, the voltage $v_{Cu(3)}$ is depicted in the same figure.

Fig. 6.9(a) shows the expected and theoretical errors in detail, $e_{exp\,u(1)}$ and $e_{t\,u(1)}$. As can be observed, the expected error has a high positive value when the SM is activated, as the measured value is higher than the calculated one. Conversely, the theoretical



(a)



(b)

FIGURE 6.7: Experimental results of a fault in the upper arm supervisory set sensor $v_{Su(1)}$, in detail: (a) fault detection method and (b) state of the system.

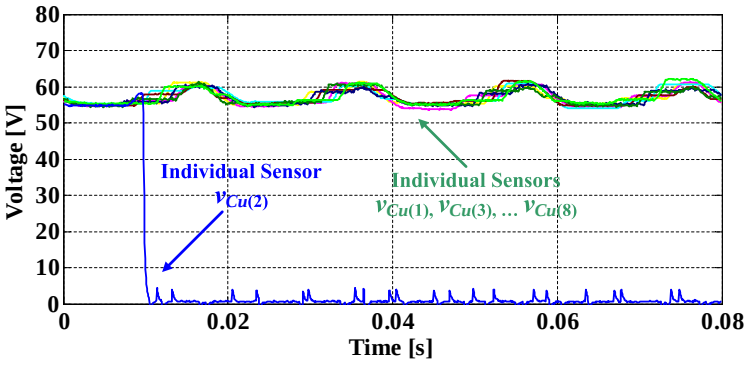
error remains at a low value. Fig. 6.9(b) shows the system state, which activates State 2 in order to identify the origin of the alarm indicator, followed by State 4 being activated to locate and substitute the faulty sensor.

6.6.3 Open-Circuit Fault

OC SM faults have been tested only for the upper switch. The implemented prototype does not include switching devices to bypass the faulty SMs. Therefore, the SMs can be deactivated, but not externally short-circuited. This fact prevents testing lower switch OC faults, since they cannot be corrected.

Similar to the sensor faults, the OC fault is tested by opening a relay connected in series with the MOSFET device. Results are shown in Figs. 6.10, 6.11, and 6.12.

Fig. 6.10(a) shows the SM capacitor voltages when a fault appears in the $SM_{u(1)}$. The fault is detected at time $t = 0.04s$, when the faulty SM is activated with negative current. Fig. 6.10(b) shows the output voltage of the converter, which becomes slightly distorted between the fault appearance and its correction. Due to the existence of additional SMs,



(a)

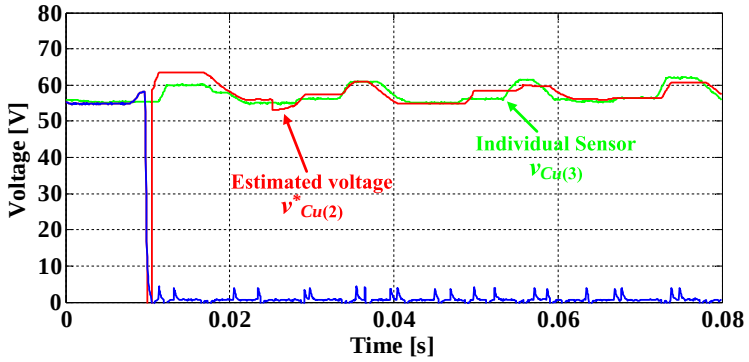


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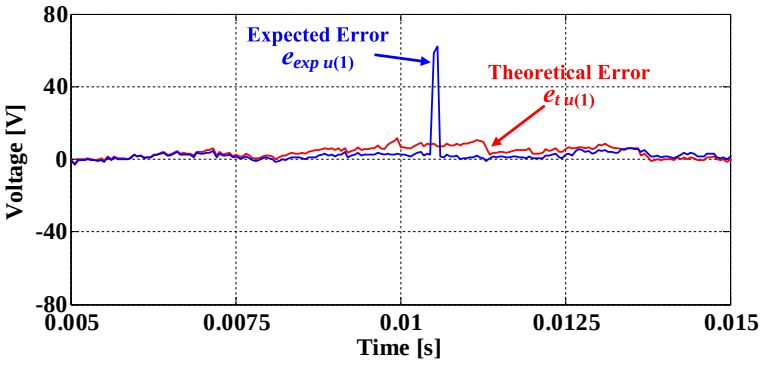
FIGURE 6.8: Experimental results of a fault in the individual sensor $v_{Cu(2)}$: (a) measured upper arm capacitor voltages and (b) comparison of the faulty sensor voltage $v_{Cu(2)}$, estimated voltage, and $v_{Cu(3)}$.

the output voltage is not modified when disabling the faulty SM. The dynamics of the upper arm current can be seen in Fig. 6.10(c), where the current becomes zero when the fault appears. Due to the modification in the circulating current reference, the current is forced to be negative and the fault is located about 2 ms after its appearance. A detail of the circulating current modification is depicted in Fig. 6.10, where the upper arm current, its normal reference, and the modified reference are depicted.

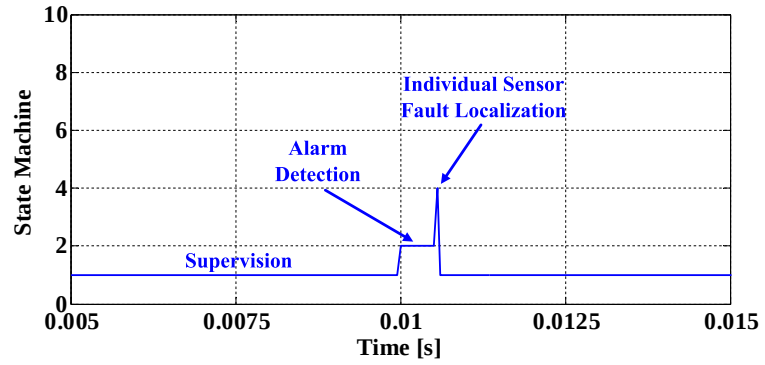
The details of the fault localization process are depicted in Fig. 6.12. The expected and theoretical errors (both of which have the same values) are depicted in Fig. 6.12(a), and the state of the system is depicted in Fig. 6.12(b). The system changes from State 1 (fault detection) to State 5 (upper switch OC fault localization) at time $t = 0.04s$ and then changes to State 8 (SM deactivation) at time $t = 0.0418s$.

6.6.4 Short-Circuit Fault

Short-circuit faults have been tested in both the upper and lower switches. In order to limit the peak current during the tests, short-circuits have been emulated by activating



(a)



(b)

FIGURE 6.9: Experimental results of a fault in an individual sensor in detail: (a) expected and theoretical errors, and (b) state of the system.

a low value resistance in parallel to the switch. In this paper, a $5\,\Omega$ resistor has been used.

Fig. 6.13(a) shows the SM capacitor voltages during an upper switch SC fault. It can be seen that the capacitor of the faulty SM discharges before the fault detection, as the SM is deactivated. When the SM is activated, the fault is detected and immediately located. Then, as the SM is deactivated, its capacitor continues discharging. Fig. 6.13(b) shows the output and arm currents in which a distortion appears when the fault is detected. The distortion appears only in the circulating current, without affecting the output current.

A detail of the fault detection and localization processes are depicted in Fig. 6.14. The theoretical and expected errors are shown in Fig. 6.14(a). It can be seen that the expected error remains near zero while the theoretical error changes. The theoretical error increases before fault detection due to the variation of the average voltage v_{Cuavg}, but it does not overpass the threshold value. However, when the SM is activated, the theoretical error becomes negative and overpasses the threshold value, whereby the fault is detected. The state of the system is depicted in Fig. 6.14(b), which shows that the

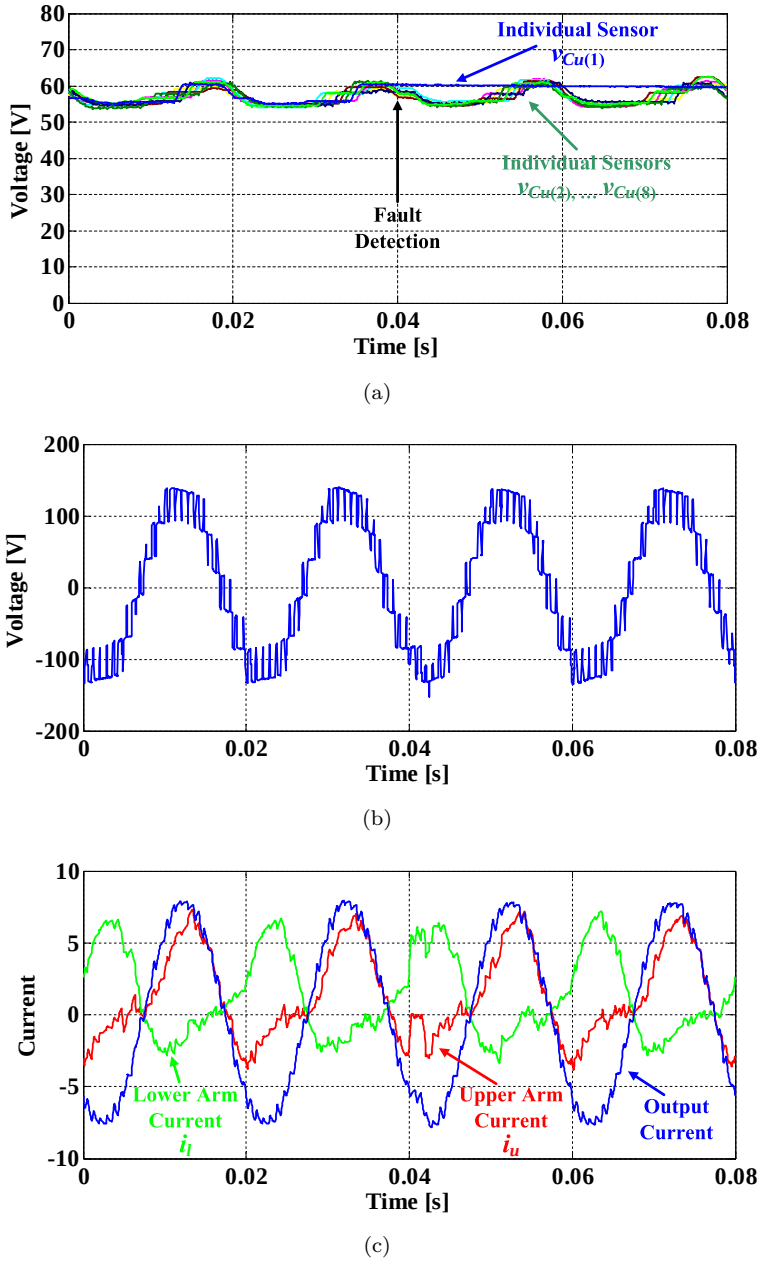


FIGURE 6.10: Experimental results of an upper switch OC fault at $SM_{u(1)}$: (a) upper arm capacitor voltages, (b) output voltage, and (c) upper arm current, lower arm current and output current.

error is localized (State 7) immediately after its detection, and it then changes to the SM Deactivation State (State 8).

SC faults have also been tested in the lower switch of a SM. Fig. 6.15 depicts the SM capacitor voltage when an SC fault appears on the lower switch of the $SM_{u(1)}$. This figure shows how the voltage of the faulty SM drops until the fault is detected. Once the fault is corrected, the voltage of the SM capacitor remains at the same value.

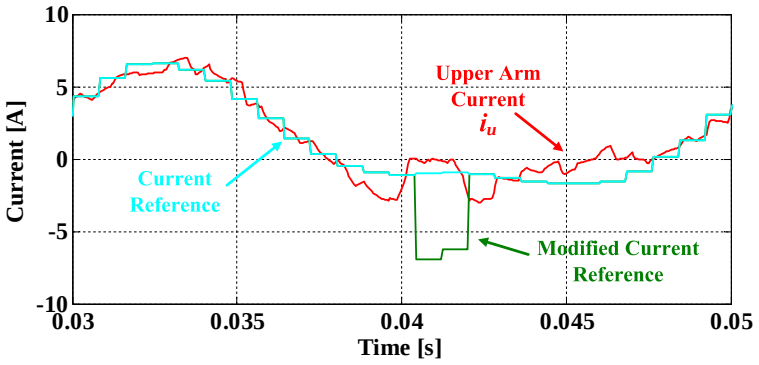
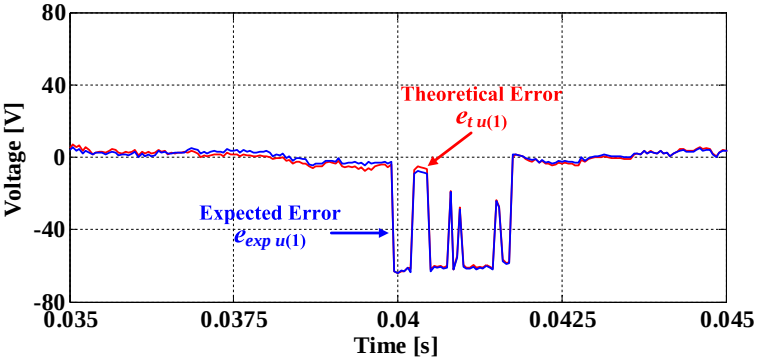
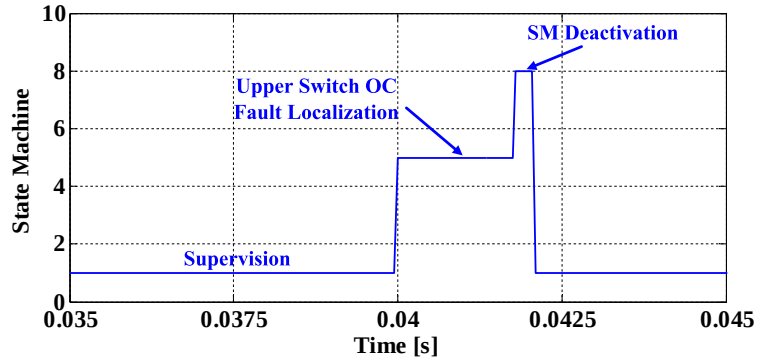


FIGURE 6.11: Detail of the circulating current modification during an upper switch OC fault: upper arm current, upper arm normal current reference, and upper arm modified current reference.



(a)



(b)

FIGURE 6.12: Experimental results of an upper switch OC fault in detail: (a) expected and theoretical errors, and (b) state of the system.

6.7 Conclusion

In this chapter, a strategy for detecting, localizing and correcting SM and sensor faults in MMCs has been explained. The use of a few external sensors provides fault detection capability and voltage sensor redundancy. Moreover, the use of additional SMs allows the faulty ones to be substituted easily. The detection technique is based on measuring the voltage provided by a set of SMs and comparing it with a calculated reference value.

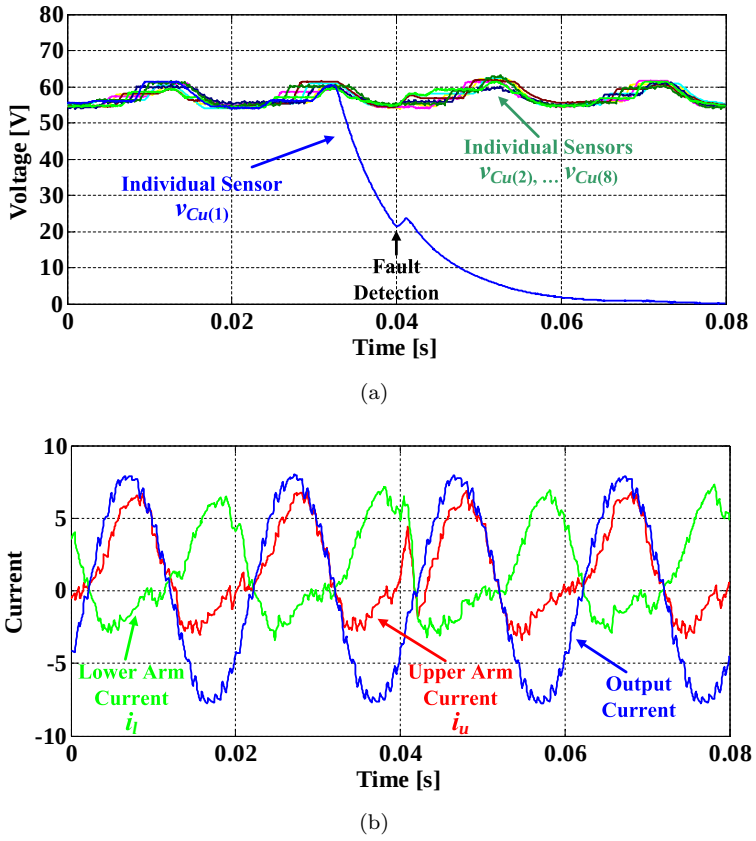
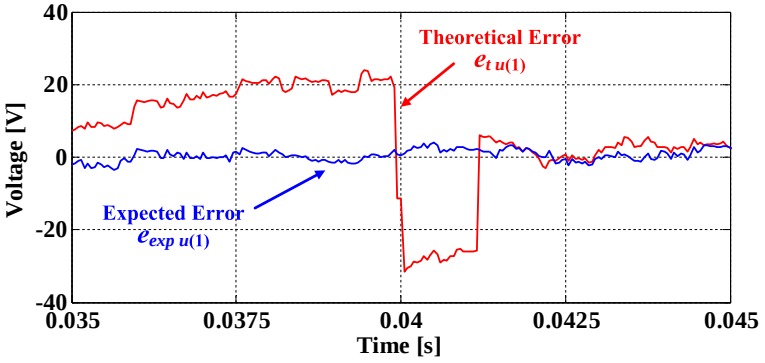
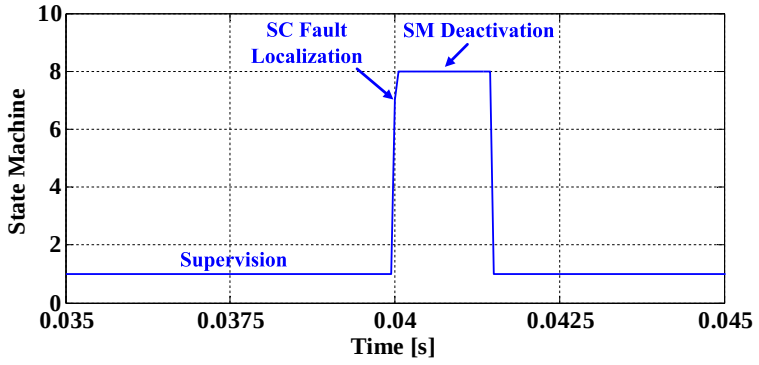


FIGURE 6.13: Experimental results of an SC fault in the upper switch: (a) SM capacitor voltages and (b) arm and output currents.

The localization method is based on forcing the deactivation of the suspicious SMs until the fault disappears. This method provides robust and fast responses to both SM and sensor faults with minor additional costs. The experimental results demonstrate the effectiveness of the proposed technique in detecting and correcting all considered faults in less than 5 milliseconds, which is much faster than other methods that can be found in the literature.



(a)



(b)

FIGURE 6.14: Experimental results of an SC fault in the upper switch in detail: (a) expected and theoretical errors, and (b) state of the system.

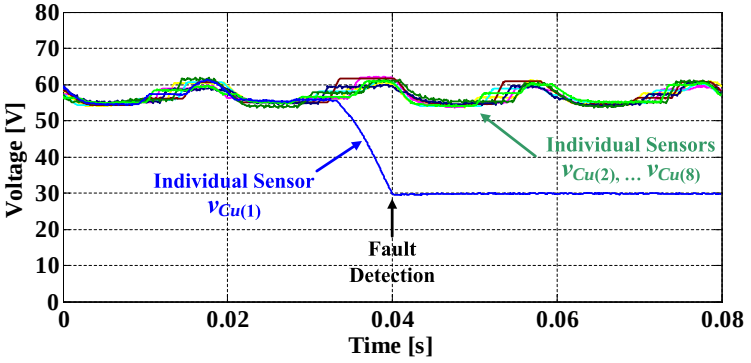


FIGURE 6.15: Experimental results of an SC fault in the lower switch: SM capacitor voltages.

Chapter 7

Balancing Algorithms for Submodule Power Losses

Tolerance and component ageing can cause significant differences in the capacitance values of the SMs. These capacitance mismatches may produce uneven switching transitions in the SMs, hence imbalances in the power losses that can lead to reliability problems. In this chapter, the imbalances that can appear in high-power MMCs are studied, and an algorithm that helps achieve evenly distributed losses in the converter SMs is presented. The proposed algorithm is based on a modification of the common voltage balancing algorithms, which use a weighted function of the capacitor voltage and the power losses as input. Even distribution of power losses is achieved at the cost of slightly increasing the capacitor voltage ripples.

7.1 Introduction

Reliability is one of the most important challenges in MMCs, since they include many switching devices and these are the weakest components in power converters [63, 130]. One of the main reasons for high-power semiconductor failure is ageing produced by mechanical and thermal stresses [73, 74], which are themselves caused by semiconductor power losses. For low and medium voltage applications, where a low number of SMs is used, the switching and conduction power losses are evenly distributed among the SMs [31]. However, the high number of SMs per phase-leg in HVDC applications may result in significant imbalance distribution of power losses and temperature in the semiconductors [131]. Consequently, uneven degradation of the semiconductors is produced, thus reducing converter reliability.

Capacitance values are different among SM capacitors, due to both fabrication tolerance and ageing of the capacitors [132, 133]. This may produce uneven distribution of switching transitions and power losses in the SMs. The effect is more significant in high-power MMCs, which already have unbalanced power loss distribution. In this chapter, the study of the loss distribution developed in [134] is detailed and extended. In addition to studying the loss distribution in converters with mismatched capacitances, a power loss balancing strategy is also presented. The proposed strategy is based on modifying the input of a voltage balancing algorithm based on sorting the SM capacitor voltages (Section 2.4). An offset is then added to the input of the voltage balancing algorithm, thus modifying the activation priority of the SMs in accordance with the objective of loss balancing. Two algorithms for calculating the loss balancing offset are detailed. The first algorithm is based on balancing the number of switching transitions for each SM, and the second one is based on balancing the estimation of both switching and conduction losses.

7.2 Power Loss Distribution with Unbalanced SM Capacitances

The main factors for capacitance mismatches in SM capacitors are fabrication tolerance (which can reach 20% in electrolytic capacitors) and ageing degradation. Small differences between the SM capacitors do not significantly affect the quality of the output voltages and currents, nor the capacitor voltage ripples, since those variables are usually regulated through closed-loop techniques. However, the control action for balancing the capacitor voltages can lead to uneven distribution of power losses among the SMs, which reduces converter reliability.

Here, the effects of nonidentical capacitances in the SMs are evaluated through simulation analysis. A simulation model of a 70-MW grid-connected MMC was implemented in MATLAB/Simulink with the PLECS toolbox. The modulation signal is provided by an output current control in the *d-q* coordinates (Section 2.7), which is synchronized with the grid frequency through a PLL. The current reference is set in order to provide or consume a fixed amount of power. The system includes a circulating current controller with the reference defined in equation (2.23) and a reduced switching frequency voltage balancing algorithm. The main characteristics of the MMC simulation model are shown in Table 7.1.

The power losses of each SM are calculated by modelling the conduction and switching losses of the semiconductors. Specifically, we model the commercial component

TABLE 7.1: Specifications of the Grid-Connected Simulation Model for the Power Loss Balance

Parameter	**Value**
Number of SMs per Arm, N	10
SM Capacitors, C	1500 μF
Arm Inductors, L	9 mH
DC-Link Voltage, V_{dc}	100 kV
Nominal Output Power, P_{out}	70 MW
Carrier Frequency, f_{cr}	2 kHz
Grid Frequency, f	50 Hz

TABLE 7.2: Linearised Static and Dynamic Semiconductor Specifications at 125°C

Parameter	**Value**
Diode Forward Voltage, V_F	1.15 V
Diode Equivalent Series Resistor, R_D	0.7 mΩ
IGBT Collector-Emitter Saturation Voltage, V_{CE}	1.3 V
IGBT Equivalent Series Resistor, R_{CE}	1.1 mΩ
Diode Reverse Recovery Energy at 800 A, E_{rec}	218 mJ
IGBT Turn-on Energy Loss at 800 A, E_{on}	242 mJ
IGBT Turn-off Energy Loss at 800 A, E_{off}	320 mJ

IGBT Fuji Electric 1MBI1200U4C-170, whose maximum ratings are a forward current of 1200 A and a direct voltage of 1700 V. Conduction losses are calculated through the static model of the IGBT and diode, while switching losses are calculated by linearising the dynamic curves from the datasheet. Considering an operation temperature of 125°C, the characteristics shown in Table 7.2 have been obtained. In order to fulfill the voltage ratings of the SM, the use of seven semiconductors connected in series are considered. For the sake of simplicity, the losses are calculated by considering the same voltage drop in each of the semiconductors.

The conduction losses for the IGBTs ($P_{cond\,T}$) and diodes ($P_{cond\,D}$) are calculated from the linearised static model of the component using the datasheet characteristics. The simplified model of the switches in the on-state can be represented by a voltage source (V_{CE} and V_F for the IGBT and the diode, respectively) and an equivalent series resistor (R_{CE} and R_D for the IGBT and the diode, respectively). The average conduction power losses are calculated over a fundamental period (T):

$$P_{cond\,T} = \frac{1}{T}\int_0^T (V_{CE} + R_{CE}\, i_T)\, i_T\, dt \text{ and} \tag{7.1}$$

$$P_{cond\,D} = \frac{1}{T}\int_0^T (V_F + R_D\, i_D)\, i_D\, dt\ , \tag{7.2}$$

where i_T and i_D represent the currents through the IGBT and diode, respectively.

The switching losses for the IGBT ($P_{sw\,T}$) are calculated as individual energy losses during the turn-on and turn-off transients. For the diode ($P_{sw\,D}$), only the turn-off transients are considered, since the turn-on losses can be assumed negligible. The energy loss functions were obtained by approximating the datasheet curves to second order polynomials using the current as a variable. The functions are also scaled to the off-state collector-emitter voltage, which is always the SM capacitor voltage $v_{Cjz(n)}$. The average power losses are calculated as the sum of all the individual energy losses over a fundamental period:

$$P_{sw\,T} = \frac{1}{T}\sum_{q=1}^{nT}\left[E_{on_q}(i_T, v_{Cjz(n)}) + E_{off_q}(i_T, v_{Cjz(n)})\right] \text{ and} \tag{7.3}$$

$$P_{sw\,D} = \frac{1}{T}\sum_{q=1}^{nT}\left[E_{rec_q}(i_D, v_{Cjz(n)})\right]\ , \tag{7.4}$$

where nT is the number of transitions in one fundamental period.

7.2.1 Performance with Unbalanced Capacitances

The following study shows the distribution of power losses when the capacitances in the SMs are different. In the simulations, the SM capacitors have been modified by using only 50% of the nominal capacitance in the first SM of phase a ($C_{au(1)}$) and, for the remaining SMs, using values that increase gradually from 85% of the nominal capacitance in the second SM ($C_{au(2)}$) to 115% of the nominal capacitance in the last SM of the upper arm ($C_{au(10)}$). The converter is controlled to provide 70 MW of active power, which corresponds to 777 A rms of output current.

Fig. 7.1 shows the upper arm capacitor voltages of phase a. Despite the capacitance mismatch, the capacitor voltages are relatively balanced, with their values being maintained within acceptable limits. The capacitor voltage of $SM_{au(1)}$, which has the smallest capacitance, presents a faster dynamic response than the other capacitors, with a peak-to-peak voltage ripple that is 35% greater than the average value. In contrast, the SM with the highest capacitance (i.e., $SM_{au(10)}$) presents the lowest ripple, with a peak-to-peak value that is 20% lower than the average.

The semiconductor power losses are significantly unbalanced. Fig. 7.2 shows the averaged values of the total, including switching and conduction losses. The power

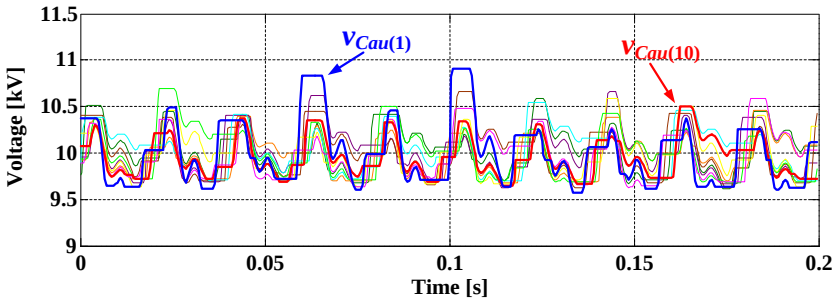


FIGURE 7.1: Upper arm capacitor voltages when using mismatched capacitances in the SMs.

losses have been averaged over a fundamental period using a moving average window for the entire period represented. Fig. 7.2(a) shows the total power losses (P_{tot}) in each SM. Due to the reduced switching frequency of each SM, the power losses show oscillating dynamics, with a frequency lower than the fundamental of the output current. It can be observed that the total power losses of $SM_{au(1)}$ are lower than the average. In contrast, the power losses of $SM_{au(9)}$, where the capacitance is increased by 10%, are the highest. The total power losses averaged over a long period (4 s) are 6.12 kW and 6.47 kW for $SM_{au(1)}$ and $SM_{au(9)}$, respectively, which means an imbalance of 5.7% in the power losses.

As can be seen in Fig. 7.2(b), the conduction losses, which are well balanced, are not the main reason for power loss imbalance. The switching power losses, which are significantly unbalanced, are represented in Fig. 7.2(c). An imbalance of 47% can be observed between $SM_{au(1)}$ and $SM_{au(9)}$, with total average power losses of 875 W and 1.28 kW, respectively.

7.3 Balancing Algorithms for Power Losses

The proposed strategy for achieving balanced power losses among the SMs of an arm is based on the degree of freedom that the MMC offers when selecting the particular SMs to be activated. This degree of freedom is generally used for balancing the capacitor voltage by selecting the most charged or discharged SMs in order to balance its voltage values. This task is performed by the voltage balancing algorithms, introduced in Section 2.4. The power loss balancing strategy is based on a modification of the reduced switching frequency voltage balancing algorithm presented in [91]. Instead of balancing only the voltage values, the modified algorithm balances a weighted function of voltage and power losses.

The proposed energy balancing strategy modifies the input of the sorting algorithm by adding an offset. The offset is calculated to change the priority of activation of the

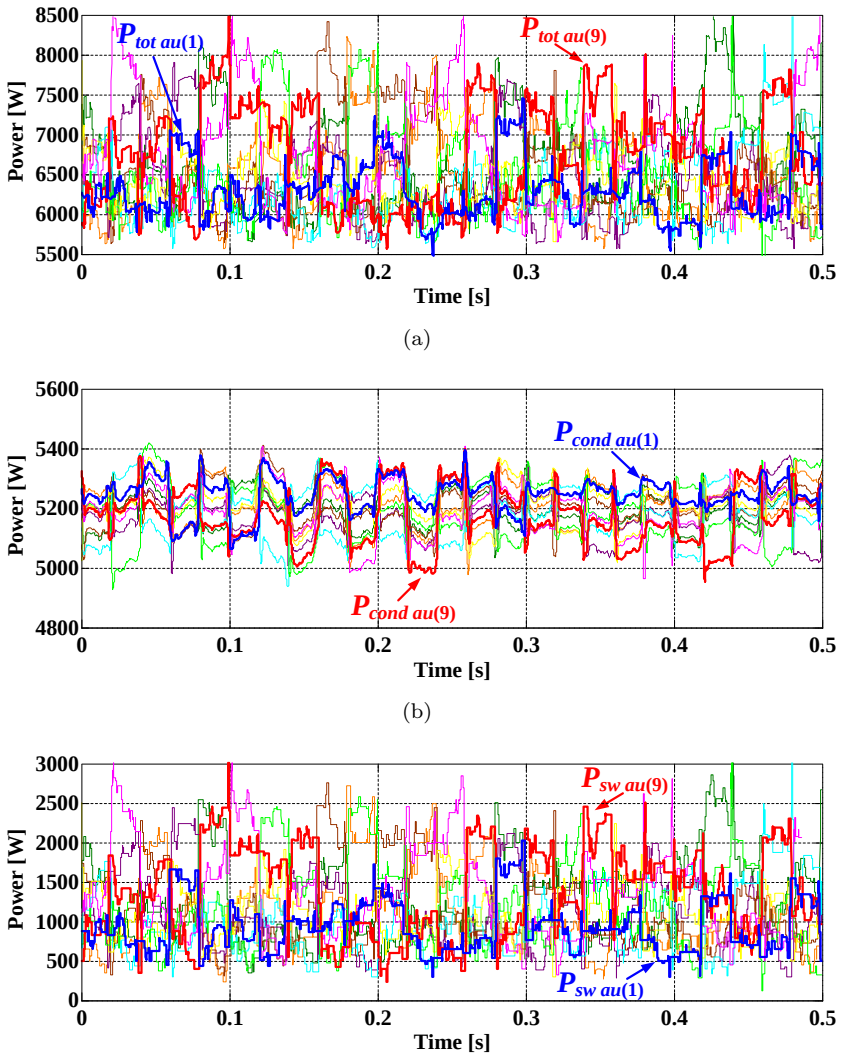


FIGURE 7.2: Power losses of the upper arm SMs when using mismatched capacitances in the SMs: (a) total power losses, (b) conduction power losses and (c) switching power losses.

SMs to balance the SM power losses. Fig. 7.3 shows the block diagram of this strategy integrated with the voltage balancing algorithm. Two different algorithms are proposed for calculating the offset added to the input of the sorting algorithm.

7.3.1 Switching Transition Balancing Algorithm

As shown in Section 7.2, capacitance variation can create significant imbalances in the switching power losses among the SMs. For this reason, a first approach is to balance the switching power losses by distributing the number of transitions evenly among the SMs. The hereinafter called switching transition balancing (STB) algorithm aims to achieve this objective.

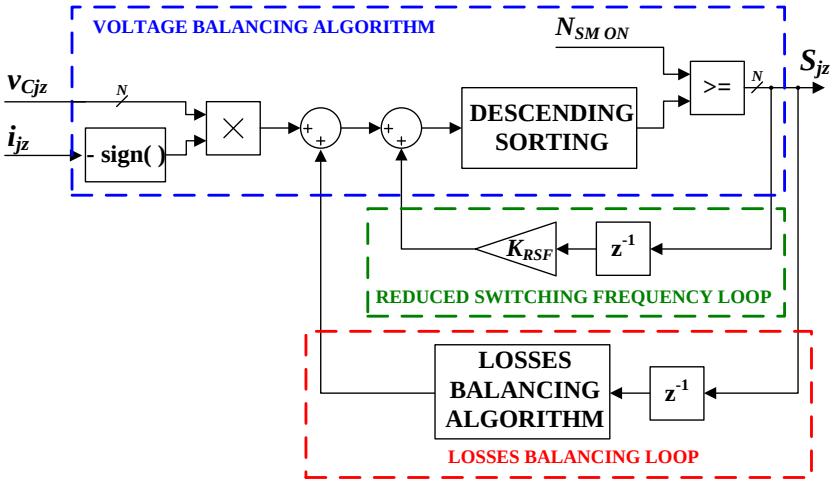


FIGURE 7.3: Block diagram of the loss balancing strategy.

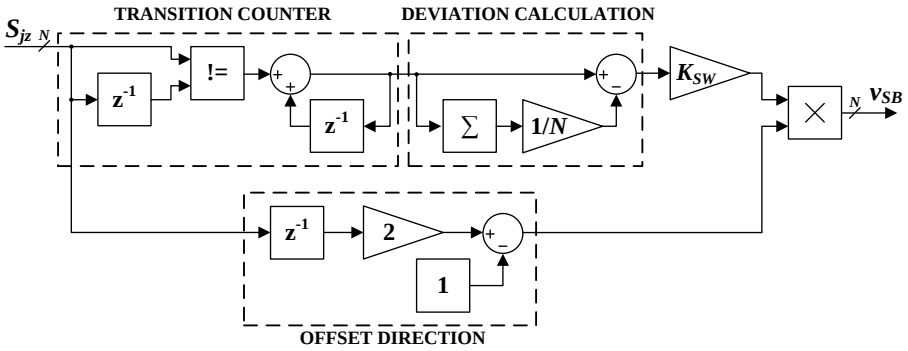


FIGURE 7.4: Block diagram of the Switching Transition Balancing Algorithm.

The STB algorithm starts by counting the number of transitions of each SM. Then, the average number of transitions is calculated by adding all the SM transitions and dividing by the number of SMs. Finally, the deviation of each SM from the average value is calculated. If the deviation is positive (the number of transitions of the SM is higher than the average), the algorithm tries to avoid the change of state of the SM. In contrast, if the deviation is negative, the algorithm tries to change the state of the SM.

In order to reduce the probability of changing the state, the activation priority is increased when the SM is activated and reduced when the SM is deactivated. That is, a positive offset is added when the SM is activated and a negative one when it is deactivated. The value of the offset consists of the deviation multiplied by a feedback gain (K_{sw}); therefore, when the deviation is negative, the offset is applied in the opposite direction. A block diagram of the STB algorithm is depicted in Fig. 7.4.

The feedback gain has to be adjusted to the specifications of each converter. For the results obtained in this chapter, it has been approximated to 20% of the capacitor voltage ripples when the switching deviation is the number of transitions performed by

a SM over a fundamental period:

$$K_{sw} = \frac{0.2\Delta v_C N}{f_{cr} T} \ . \tag{7.5}$$

7.3.2 Total Loss Balancing Algorithm

The second algorithm proposed in this chapter is called the total loss balancing (TLB) algorithm. This algorithm directly balances the power losses of each semiconductor. For this purpose, the conduction power losses of the upper and lower IGBTs and diodes are estimated and their deviation calculated. Since the states of the upper and lower switches are complementary, the switching losses are estimated and balanced for the whole SM, not for each semiconductor.

The conduction power losses depend on the sign of the current; i.e., when the current is positive, the upper diode or lower IGBT will carry the arm current, while the upper IGBT or lower diode will carry the arm current when it is negative. For this reason, the output offset is calculated differently when the current is positive or negative and it is using only the deviations that can be controlled at each moment. To reduce the power losses in the upper semiconductors, the activation priority should decrease, thus facilitating SM deactivation. In contrast, the priority should increase in order to reduce the power losses of the lower semiconductors. Since the sorting algorithm is calculated in descending order, a positive offset means an increase in the activation priority, and a negative offset a decrease in such a priority.

The switching power losses are estimated according to the dynamic characteristics of the semiconductors and the measured values of voltages and currents in the SMs. Then its deviation value is calculated, and the losses are balanced in a similar way to the number of switching transitions in the STB algorithm. That is, the priority of changing the state is increased when the deviation is negative and decreased when it is positive.

The total offset of the TLB algorithm is calculated as the sum of all the correcting actions. Fig. 7.5 shows a block diagram of the TLB algorithm. Each one of the correction offsets is multiplied by a feedback gain, which can be calculated similarly to the STxB algorithm. In this case, the offset has been adjusted to 50% of the capacitor voltage ripple when the deviation is equal to the average power in the semiconductor:

$$K_{device} = \frac{0.5\Delta v_C}{P_{device}} \ , \tag{7.6}$$

where the subindex *device* identifies the semiconductor in which the conduction power losses are balanced (upper IGBT, upper diode, lower IGBT or lower diode) or identifies the switching power losses of all the SM.

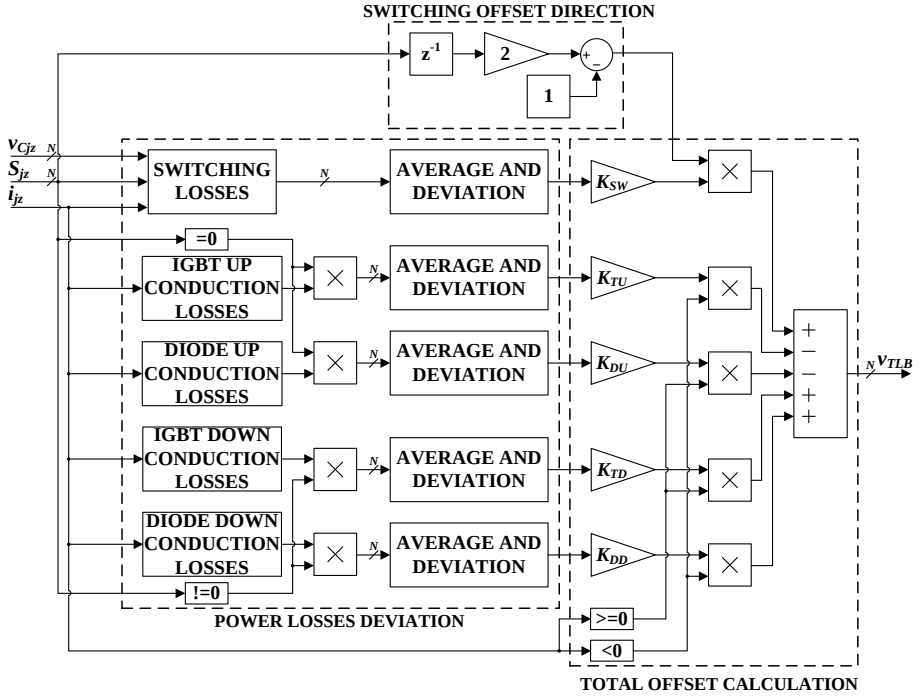


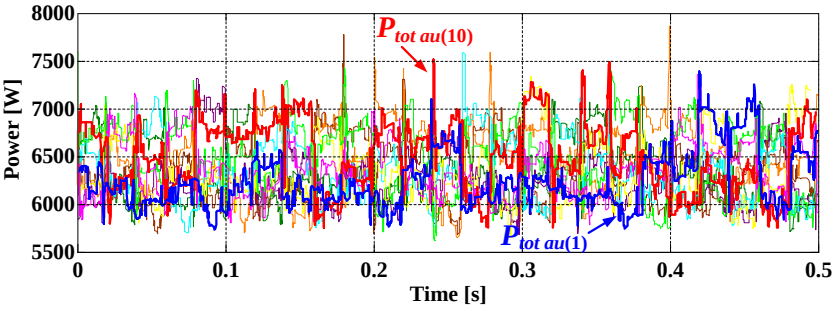
FIGURE 7.5: Block diagram of the STB algorithm.

7.4 Simulation Results

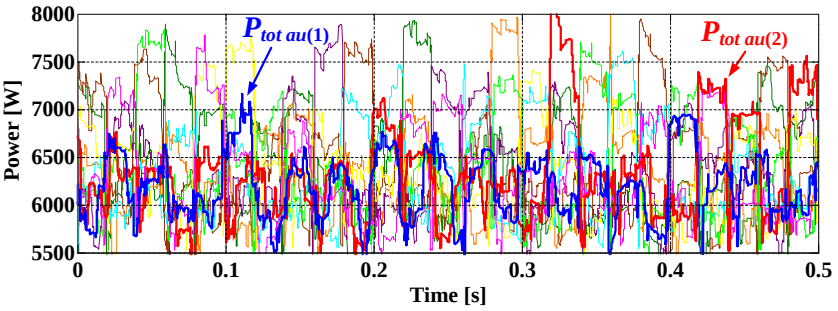
The performance of the power loss balancing strategy has been tested by simulation studies. The two proposed algorithms, STB and TLB, have been simulated and compared in the 70-MW grid-connected model detailed in Section 7.2.

Fig. 7.6 shows the total averaged power losses of the SMs in the upper arm of phase a. Fig. 7.6(a) represents the power losses when applying the STB algorithm. Since the main imbalance without control appears in the switching power losses, balancing the number of switching transitions improves the overall balance of total power losses in the SMs. The figure depicts averaged power losses with fewer oscillations than when no balancing strategy is applied (Fig. 7.2(c)). The total average power losses for a long period (4 s) are, respectively, 6.18 kW and 6.42 kW for the SMs with the highest capacitance ($SM_{au(1)}$) and the lowest capacitance ($SM_{au(10)}$). This means that the maximum power loss imbalance among SMs has been reduced to 3.9%.

Fig. 7.6(b) represents the power losses when applying the TLB algorithm. Although the figure depicts averaged power losses with low frequency oscillations, the total averaged value over the long term demonstrates that this algorithm efficiently balances the power losses. The SM with the lowest losses is the one with lowest capacitance, $SM_{au(1)}$, which presents an average of 6.32 kW; while the SM with the highest losses is $SM_{au(2)}$, the second SM with less capacitance (a reduction of 15%) and an averaged



(a)



(b)

FIGURE 7.6: Power losses of the upper arm SMs when using the balancing strategy: (a) STB algorithm and (b) TLB algorithm.

TABLE 7.3: Power Loss Imbalances with Different Strategies

Strategies	**Maximum Power Loss Imbalance**
No power loss balancing strategy	5.7%
STB algorithm	3.8%
TLB algorithm	1.4%

value of 6.41 kW. Therefore, the maximum imbalance is only 1.4%. A summary of the power loss imbalance with the different algorithms is shown in Table 7.3.

Since the objective of the power loss balancing strategy is to reduce the ageing of the SMs with the highest power losses, it is interesting to see that both power loss balancing algorithms reduce the maximum value of power losses. While the SM with maximum power losses in the converter without a control strategy presents a power loss of 6.47 kW, the maximum value obtained with the STB algorithm is 6.42 kW, and with the TLB algorithm is 6.41 kW. Therefore, it can be stated that the proposed algorithms reduce the accelerated ageing of some semiconductors.

Since the proposed algorithms are based on modifying the input signals of the capacitor voltage balancing algorithm, the capacitor voltage ripples should also be evaluated. Fig. 7.7 shows the SM capacitor voltages of the upper arm. Fig. 7.7(a) shows the SM capacitor voltages when using the STB algorithm. As observed, the SM capacitor voltages

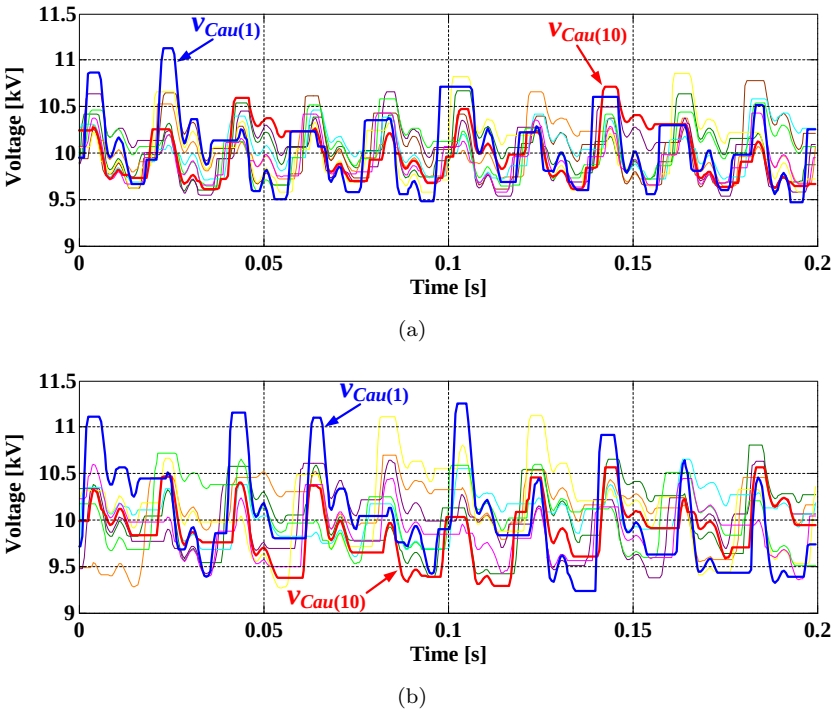


FIGURE 7.7: Upper arm capacitor voltages: (a) STB algorithm and (b) TLB algorithm.

have the same average value, but the voltage ripples are higher when compared with the case of not using any power loss balancing control (Fig. 7.1). While the original voltage ripples have a peak-to-peak value of 1.2 kV, the voltages obtained with the STB algorithm present a peak-to-peak value of 1.6 kV.

As shown in Fig. 7.7(b), the capacitor voltage ripples are similar when using the TLB algorithm. Since the offset applied with this algorithm is larger, the capacitor voltage ripples are slightly increased. The maximum peak-to-peak voltage ripple in the smallest capacitor is now 2 kV.

The increase in the capacitor voltage ripples can cause some negative effects, such as worsening the quality of the output voltages and reducing the lifetime of the capacitors. Nevertheless, the maximum peak-to-peak value of the capacitor voltage ripples is maintained within a reasonable value, i.e., 20% of the nominal voltage.

7.5 Low-Power Experimental Results

Loss imbalances with capacitance mismatches and loss balancing algorithms have been tested experimentally. The results were obtained from the University of Nottingham prototype, an AAC used as a three-phase grid-connected MMC with four SMs per arm ($N = 4$). All the tests were conducted by reducing the capacitance of the $SM_{au(1)}$ to 50%

TABLE 7.4: Specifications of the Laboratory Prototype for Power Balancing Algorithms

Parameter	**Value**
Number of Basic SMs per Arm, N	4
Basic SM Capacitors, C	303 μF
Arm Inductors, L	2 mH
DC-link Voltage, V_{dc}	500 V
Grid rms Voltage, $V_{g\,rms}$	110 V
Output Power, P_{out}	1 kW
Carrier Frequency, f_{cr}	3.6 kHz
Grid Frequency, f	50 Hz

of the nominal capacitance. The loss balancing algorithms were implemented only in the upper arm of phase a. The tests were performed with an output current control whose reference was regulated to provide 1 kW of active power to the grid. Characteristics of the experimental setup are detailed in Table 7.4.

Measuring the individual power losses of each SM is a difficult task. One possible method for measuring SM losses is to individually measure the voltage and current of each device. However, this method requires that a high number of voltage and current probes be connected to the terminals of the switching devices, which sometimes are not accessible. Another method is to measure the input power of the SMs for a few periods. Since the capacitors store reactive power, the average SM power in a period corresponds to the losses of the SM. However, this value includes the power losses of the switching devices and the capacitors.

In a low-power prototype, the power losses of the SMs are even more difficult to accurately measure. Conduction losses can be measured from the current and voltage drop in the semiconductors. The voltage sensors require a relatively high voltage range and a really high resolution, since the voltage drop in the semiconductors has a value of around 0.7 V for a measuring range of 150 V. Switching losses are even more difficult to measure, since activation and deactivation transitions are really fast and this requires high bandwidth sensors with really low delay.

Since those requirements were not fulfilled when the test was performed, a power loss estimation method was used. Considering static and dynamic models of the semiconductors that are similar to those explained in Section 7.2, the losses of the semiconductors were calculated in the DSP while using the measured arm currents and capacitor voltages as inputs. The switching devices used in the University of Nottingham prototype

TABLE 7.5: Linearised Static and Dynamic Semiconductor Specifications of the Experimental Test

Parameter	**Value**
Diode Forward Voltage, V_F	0.74 V
Diode Equivalent Series Resistor, R_D	16 mΩ
IGBT Collector-Emitter Saturation Voltage, V_{CE}	0.65 V
IGBT Equivalent Series Resistor, R_{CE}	23 mΩ
Diode Reverse Recovery Energy at 800 A, E_{rec}	0.42 mJ
IGBT Turn-on Energy Loss at 800 A, E_{on}	0.46 mJ
IGBT Turn-off Energy Loss at 800 A, E_{off}	1.20 mJ

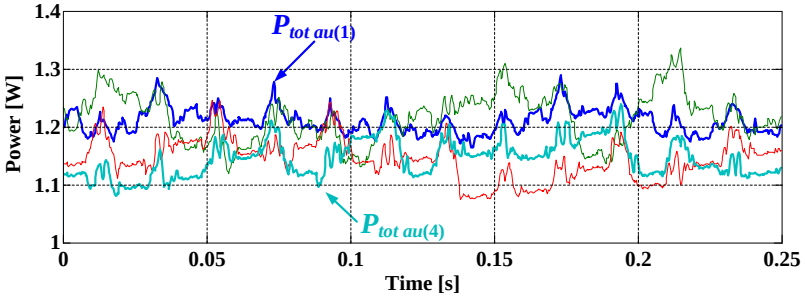
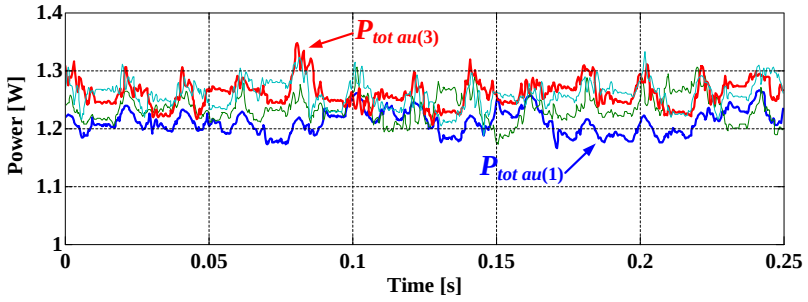


FIGURE 7.8: Experimental results. Power losses of the upper arm SMs with no loss balancing algorithm.

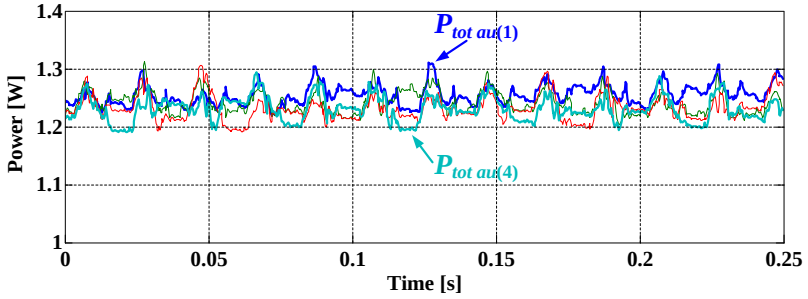
were the IGBT modules Infineon F4-50R06W1E3, whose maximum ratings are a forward current of 50 A and a direct voltage of 600 V. The linearised static and dynamic specifications are detailed in Table 7.5.

Fig. 7.8 shows the averaged values of the total losses of the phase a upper arm SMs when no loss balancing algorithm is applied. The power losses have been averaged over a fundamental period using a moving average window for all the represented period. It can be seen that the losses are unbalanced, wherein the SM with less capacitance ($SM_{au(1)}$) is the one with the highest losses, and $SM_{au(4)}$ is the one with the lowest losses. The value of the losses averaged over the entire depicted period (0.25 s) is 1.176 W for $SM_{au(1)}$ and 1.1 W for $SM_{au(4)}$, which means an imbalance of 6.9%.

Fig. 7.9 shows the averaged loss when the proposed losses balancing algorithms are applied. Fig. 7.9(a) shows the averaged losses when applying the STB algorithm. It can be observed that the losses are more balanced than in Fig. 7.8. In this case, $SM_{au(1)}$ presents the lowest power, with a total average of 1.209 W, while $SM_{au(3)}$ presents the highest total average power (1.266 W). With the STB algorithm, the imbalance is 4.7%. Fig. 7.9(b) shows the averaged losses with the TLB algorithm, which, as expected from the simulations, is the one that best reduces the power imbalances. The total average



(a)



(b)

FIGURE 7.9: Experimental results. Power losses of the upper arm SMs with the loss balancing algorithms: (a) STB and (b) TLB.

TABLE 7.6: Experimental Power Loss Imbalances with Different Strategies

Strategies	**Maximum Power Loss Imbalance**
No power loss balancing strategy	6.9%
STB algorithm	4.7%
TLB algorithm	1.6%

losses are 1.253 W for $SM_{au(1)}$ and 1.233 W for $SM_{au(4)}$, reducing the imbalance to a value of 1.6%. A summary of the loss imbalances is shown in Table 7.6.

Fig. 7.10 shows the upper arm capacitor voltages of phase a when no losses control is used and when the two loss balancing algorithms are applied. It can be observed that $SM_{au(1)}$ presents the highest ripples, since its capacitance is reduced by 50%. As expected from the simulations, the capacitor voltage ripples are higher when using the loss balancing algorithms than when no loss balancing control is used.

7.6 Conclusion

In this chapter, the effects of differences in capacitance values among SMs of a high-powered, grid-connected MMC have been studied. The capacitance differences can cause uneven distribution of the semiconductor power losses, leading to accelerated ageing of

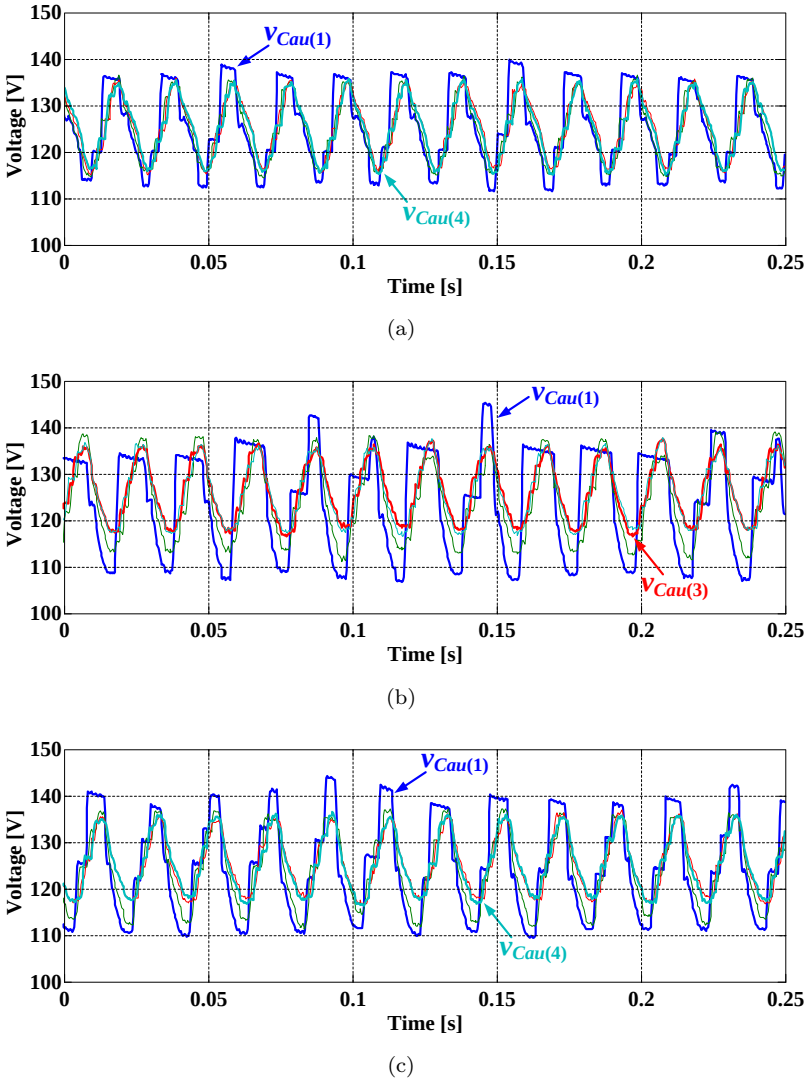


FIGURE 7.10: Experimental results. Capacitor voltages of the upper arm SMs with different control techniques: (a) no loss balancing algorithm, (b) STB algorithm, and (c) TLB algorithm.

some semiconductors and, hence, reducing converter reliability. To address this problem, a power loss balancing strategy is proposed, which is based on modifying the input signals of the capacitor voltage balancing algorithm. Two solutions are proposed: an algorithm based on balancing the number of switching transitions and another algorithm based on balancing the estimated power losses in the semiconductors. The effectiveness of the proposed algorithms has been studied through simulation and experimental results. It has been demonstrated that the two algorithms reduce power loss imbalances, although they increase the capacitor voltage ripples. The proposed strategy can also be used to force imbalances in the distribution of semiconductor power losses. This can be useful in MMC where the physical location and cooling conditions of the SMs produce uneven distribution of heat dissipation, which can be compensated by forcing imbalances in the SM power losses.

Chapter 8

Application of the MMC in Low-Speed Motor Drives with Discontinuous Modulation

The use of the MMC for motor drive applications is limited by the high capacitor voltage ripples that appear at low modulation indices. Discontinuous modulation has been demonstrated to be an effective method for reducing the capacitor voltage ripples. For this reason, it could be used in motor drive applications. In this chapter, this technique is adapted and applied for driving a permanent magnet synchronous machine (PMSM). A new energy controller is also presented, which is suitable for operation with nonsinusoidal reference signals.

8.1 Introduction

In the field of high-power motor drives (megawatt range), the quality of the voltages generated by the power converter is a decisive factor. Voltage harmonics cause additional power losses to the motor, which in turn reduce its efficiency and complicate thermal management. This is why the MMC is a promising topology in this field. Suitability of the MMC in the area of medium-voltage motor drives has also been reported [110, 114]. However, the main challenge that limits the widespread use of the MMC in motor drive applications is the large capacitor voltage ripples produced under low-speed operation. The capacitor voltage ripple amplitudes are inversely proportional to the output frequency of the converter, i.e. the motor speed.

Multiple solutions have been proposed to reduce the capacitor voltage ripples in motor-drive applications. Some publications propose using new MMC topologies [115] or MMCs based on full-bridge SMs [135, 136]. However, reducing capacitor voltage ripples with the standard MMC topology based on half-bridge SMs remains a challenge.

The control of the circulating current to reduce the capacitor voltage ripples has been extensively studied, as detailed in Chapter 3. However, when operating with low frequencies, those techniques cannot sufficiently reduce the capacitor voltage ripples. Operation of the MMC at very low frequencies was firstly achieved in [94], where a sinusoidal zero-sequence component of a higher frequency was added to the modulation signals in combination with circulating currents of the same frequency. This technique is able to translate the power fluctuations to a higher frequency, achieving a significant reduction in the capacitor voltage ripples. It is only practical when operating with low output frequencies, otherwise the frequency of the injected zero-sequence component would be excessively high. For this reason, [137] and [46] present hybrid mechanisms that switch from low to high speed operation modes. In the case of high speed operation, the average SM capacitor voltages can be reduced to accommodate higher voltage ripples [138].

With the objective of reducing the circulating current and conduction power losses, [47, 139] present a technique based on the injection of a square-wave zero-sequence signal and a square-wave circulating current. This technique achieves a reduction of up to 50% of the circulating current peak value. Similar techniques are presented in [116] and [140], which combine the square-wave zero-sequence with a sinusoidal circulating current.

Discontinuous modulation (Chapter 4) is another technique that can be used for reducing the capacitor voltage ripples. Its effectiveness has been demonstrated in grid-frequency applications [119], but it has never been tested in variable-speed motor drives. In this chapter, the closed-loop discontinuous modulation technique (CL-DPWM) is applied to a motor drive based on a permanent-magnet synchronous machine (PMSM). The modulation technique has been implemented together with a typical field-oriented control (FOC), a strategy based on a coordinate transformation in a synchronous rotating *d-q* reference frame. This control strategy presents a high dynamic and static performance through internal current control loops [141].

Since the modulation signal is not sinusoidal when in discontinuous modulation, the common energy balancing controllers based on the injection of a fundamental component [7, 87] do not present an optimal performance with this modulation technique. For this reason, a new energy controller is also proposed. The new energy controller, named modulated energy controller (MEC), is based on instantaneous values of the reference signals and is effective for any kind of modulation signals.

The high capacitor voltage ripples that appear at low modulation indices also cause distortion at the output voltages and currents. For this reason a voltage control technique based on a feed-forward compensation of the voltage ripples is developed and tested. This feed-forward compensation is based on the technique developed in [86, 142].

Experimental results operating at ultra-low frequency are obtained from driving a PMSM at a speed of 30 r/min (1% of the nominal value) with a load torque of 70%. In order to highlight the benefits of this technique, the results have been compared with those achieved using the techniques based on sinusoidal [94] and square-wave [139] zero-sequence signal injection. The discontinuous modulation produces capacitor voltage ripples similar to those obtained with the injection of a higher frequency signal in the zero-sequence and circulating currents, but it can achieve a significant reduction in the rms value of the circulating currents and, hence, in the power losses.

8.2 Mathematical Development of Discontinuous Modulation

The suitability of discontinuous modulation for reducing the capacitor voltage ripples for low modulation indices and low frequencies has been demonstrated mathematically. Considering the use of CL-DPWM over a sinusoidal reference signal (2.36) with a sinusoidal output current (2.37) that is in phase with the reference ($\varphi = 0$), the clamping periods would coincide with the maximum and minimum values of the reference signal. That is, the clamping periods are centred at the phase angles 0 and π of a cosinusoidal signal. With these considerations, the zero-sequence signal is defined as:

$$v_{zs} = \begin{cases} 1 - m\,\cos(\omega t) & \text{if } -\dfrac{\pi}{6} < \omega t < \dfrac{\pi}{6} \\ -1 - m\,\cos\left(\omega t + \dfrac{2\pi}{3}\right) & \text{if } \dfrac{\pi}{6} < \omega t < \dfrac{3\pi}{6} \\ 1 - m\,\cos\left(\omega t - \dfrac{2\pi}{3}\right) & \text{if } \dfrac{3\pi}{6} < \omega t < \dfrac{5\pi}{6} \\ -1 - m\,\cos(\omega t) & \text{if } \dfrac{5\pi}{6} < \omega t < \dfrac{7\pi}{6} \\ 1 - m\,\cos\left(\omega t + \dfrac{2\pi}{3}\right) & \text{if } \dfrac{7\pi}{6} < \omega t < \dfrac{9\pi}{6} \\ -1 - m\,\cos\left(\omega t - \dfrac{2\pi}{3}\right) & \text{if } \dfrac{9\pi}{6} < \omega t < \dfrac{11\pi}{6} \end{cases} \tag{8.1}$$

According to (4.1), the discontinuous modulation signal v_{jd} consists of the addition of the reference signal v_{jm} and the zero-sequence signal v_{zs}. Considering an ideal circulating current (4.2), the capacitor voltage can be calculated by applying the equations of the

averaged model of the converter (2.18). It has to be noted that the original modulation signal v_{jm} in (2.18) has to be substituted with the discontinuous modulation signal v_{jm}:

$$\overline{v_{Cju(n)}} = \frac{1}{C}\int_0^t \overline{i_{ju}}\frac{1-v_{jd}}{2}dt + V_{Cju(n)0}\ . \tag{8.2}$$

Under such conditions, the piecewise defined function of the voltage variation with CL-DPWM for the upper arm becomes:

$$v_{Cju(n)} = \begin{cases} V_{Cju(n)0} & \text{if } -\frac{\pi}{6} < \omega t < \frac{\pi}{6} \\ \frac{3I_{ac}m}{8\omega C}\left\{\omega t - \frac{1}{\sqrt{3}}\cos\left(2\omega t + \frac{\pi}{3}\right)\right. & \\ \quad + m\left[\frac{\sqrt{7}}{2}\sin\left(\omega t + \pi - \frac{1}{3}\right)\right. & \text{if } \frac{\pi}{6} < \omega t < \frac{3\pi}{6} \\ \quad \left.\left. + \frac{1}{6}\sin\left(3\omega t + \frac{2\pi}{3}\right)\right]\right\} + V_{Cju(n)0} & \\ \frac{3I_{ac}m}{8\omega C}\left\{-\omega t - \frac{1}{\sqrt{3}}\cos\left(2\omega t - \frac{\pi}{3}\right)\right. & \\ \quad + m\left[\frac{\sqrt{7}}{2}\sin\left(\omega t + \pi + \frac{1}{3}\right)\right. & \text{if } \frac{3\pi}{6} < \omega t < \frac{5\pi}{6} \\ \quad \left.\left. + \frac{1}{6}\sin\left(3\omega t - \frac{2\pi}{3}\right)\right]\right\} + V_{Cju(n)0} & \\ V_{Cju(n)0} & \text{if } \frac{5\pi}{6} < \omega t < \frac{7\pi}{6} \\ \frac{3I_{ac}m}{8\omega C}\left\{-\omega t + \frac{1}{\sqrt{3}}\cos\left(2\omega t + \frac{\pi}{3}\right)\right. & \\ \quad + m\left[\frac{\sqrt{7}}{2}\sin\left(\omega t + \pi - \frac{1}{3}\right)\right. & \text{if } \frac{7\pi}{6} < \omega t < \frac{9\pi}{6} \\ \quad \left.\left. + \frac{1}{6}\sin\left(3\omega t + \frac{2\pi}{3}\right)\right]\right\} + V_{Cju(n)0} & \\ \frac{3I_{ac}m}{8\omega C}\left\{\omega t + \frac{1}{\sqrt{3}}\cos\left(2\omega t - \frac{\pi}{3}\right)\right. & \\ \quad + m\left[\frac{\sqrt{7}}{2}\sin\left(\omega t + \pi + \frac{1}{3}\right)\right. & \text{if } \frac{9\pi}{6} < \omega t < \frac{11\pi}{6} \\ \quad \left.\left. + \frac{1}{6}\sin\left(3\omega t - \frac{2\pi}{3}\right)\right]\right\} + V_{Cju(n)0} & \end{cases} \tag{8.3}$$

where $V_{Cju(n)0}$ is the voltage of the capacitor at the end of the previous clamping period.

Equation (8.3) demonstrates that the capacitor voltage ripples with CL-DPWM are proportional to the modulation signal. Therefore, this modulation technique reduces the capacitor voltage ripples when working with low modulation indices. Moreover, the output voltage in motor drive applications is usually proportional to the output frequency; therefore, the modulation index is too. Consequently, the term $\frac{3I_{ac}m}{8\omega C}$ can be considered constant. This means that the capacitor voltage ripple amplitude would no longer be inversely proportional to the output frequency, thus allowing for operation of the converter at low speeds.

If the multiplier $\frac{3I_{ac}m}{8\omega C}$ is considered constant, the voltage variation in the capacitors is bounded and the maximum and minimum values can be found. Two main terms can be identified in (8.3), the first one being independent of the modulation index, and the second one proportional to the modulation index. As a consequence, the minimum capacitor voltage ripple appears with a modulation index equal to 1, and the maximum ripple is produced when the modulation index tends to 0:

$$\Delta v_{C\,CL-DPWM\,min}(m=1) = \frac{I_{ac}}{4\omega_N C} \cdot 0.6416 \text{ and} \tag{8.4}$$

$$\Delta v_{C\,CL-DPWM\,max}(m \to 0) = \frac{I_{ac}}{4\omega_N C} \cdot \pi \ , \tag{8.5}$$

where ω_N is the nominal speed of the motor, achieved with $m = 1$.

In contrast, a sinusoidal modulation will produce a voltage variation inversely proportional to the fundamental frequency, tending to infinity when the modulation frequency tends to zero. In order to illustrate this fact, the voltage variation with a purely sinusoidal modulation index and the capacitor voltage ripples at modulation index 1 and 0.1 have been obtained:

$$v_{C\,SPWM} = \frac{I_{ac}}{4\omega C}\left[\sin(\omega t) - \frac{m^2}{4}\left(\sin(\omega t) + \frac{1}{3}\sin(3\omega t)\right)\right] \ , \tag{8.6}$$

$$\Delta v_{C\,SPWM\,min}(m=1) = \frac{I_{ac}}{4\omega_N C} \cdot \frac{2}{3} \text{ and} \tag{8.7}$$

$$\Delta v_{C\,SPWM}(m=0.1) = \frac{I_{ac}}{4\omega_N C} \cdot 9.935 \ . \tag{8.8}$$

The theoretical capacitor voltage ripples at modulation index 1 are very similar, albeit slightly smaller with CL-DPWM. However, since the voltage ripples with sinusoidal modulation are inversely proportional to the output frequency, the voltage ripples are more than three times larger when the modulation index is 0.1 (10% of nominal speed) than with CL-DPWM.

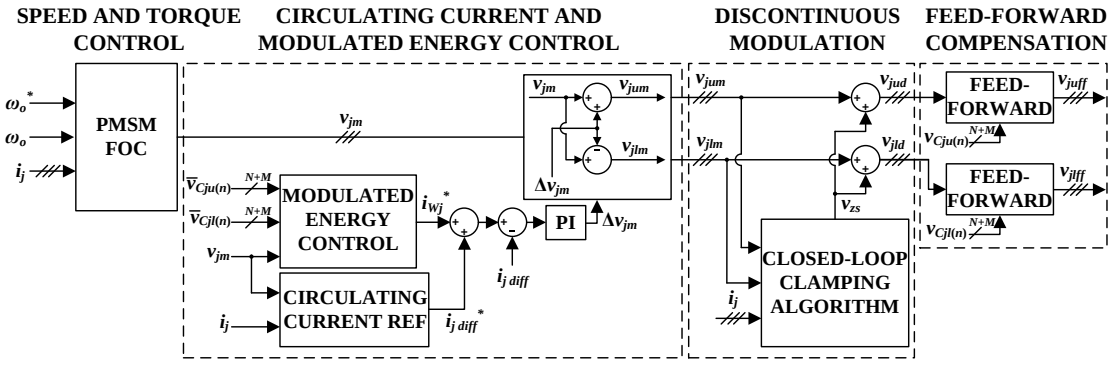


FIGURE 8.1: Block diagram of the control system.

8.3 Control System

The use of discontinuous modulation for an MMC motor drive application requires the use of a complete control system. The proposed control scheme can be divided into four stages. The first one is the FOC, that implements the PMSM speed and torque control loops. The second stage is composed of the circulating current controller and the MEC, which produces a signal to be added to the circulating current reference. The third stage is composed of the discontinuous modulation block, which calculates and adds the zero-sequence component. Finally, the feed-forward compensation block modifies the modulation signals according to the capacitor voltages. A block diagram of the control system is depicted in Fig. 8.1. The balancing of the capacitor voltages is performed with a reduced switching frequency voltage balancing algorithm.

The first control block involves the speed and torque loops of the PMSM. Those loops are implemented using the FOC strategy [97], whose block diagram is shown in Fig. 8.2. The FOC strategy is based on the *d-q* coordinates model of the PMSM:

$$v_d = R_s i_d + L_d \frac{d}{dt} i_d - \omega_e L_q i_q \quad \text{and} \tag{8.9}$$

$$v_q = R_s i_q + L_q \frac{d}{dt} i_q + \omega_e L_d i_d + \omega_e \lambda_m \ , \tag{8.10}$$

where v_d and v_q are the stator voltage components, i_d and i_q are the stator current components, R_s is the stator resistance, L_d and L_q are the equivalent *d-q* inductances, λ_m is the magnetic flux of the permanent magnets, and ω_e is the electrical frequency. The electrical frequency is calculated as a product of the mechanical speed ω_o and the number of pole pairs of the machine (p).

The i_d component is related to the motor magnetization. In order to avoid demagnetization of the permanent magnets, the i_d reference is set to zero ($i_d^* = 0$). In contrast, i_q is directly proportional to the output torque. Therefore, the q-axis current reference

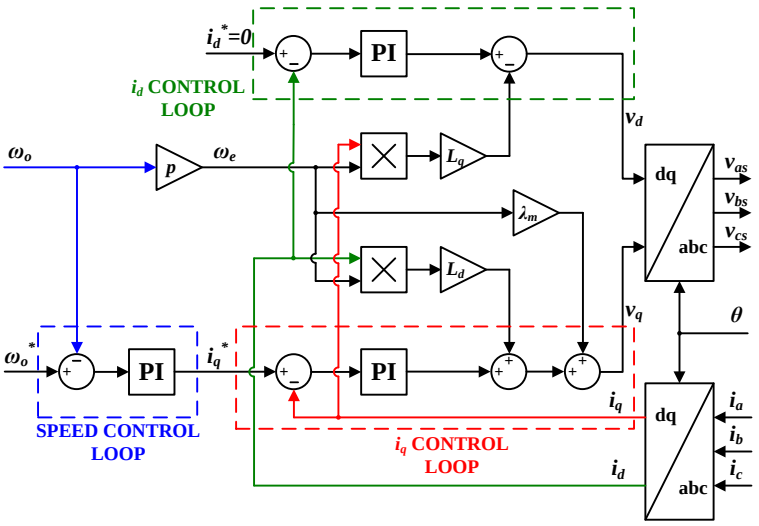


FIGURE 8.2: PMSM FOC diagram.

i_q^* is calculated by the outer loop, which regulates the motor speed. In order to decouple the d and q control loops, crossed terms ($\omega_e L_d i_d$ and $-\omega_e L_q i_q$) are incorporated in the control scheme in order to provide the final voltage references (v_d and v_q).

The second control block consists of the circulating current controller and voltage reference calculation. The main component of the circulating current reference (4.2) is the one that ensures capacitor voltage ripple reduction in discontinuous modulation (Section4.2). However, an additional component for achieving energy balance between the upper and lower arms needs to be added to the circulating current reference. This component is calculated by the MEC, which is explained in Section 8.4.

The third block calculates and adds the discontinuous zero-sequence signal to the reference signals for the upper and lower arms. According to the CL-DPWM algorithm, the six reference signals (i.e., two for each phase-leg) and the three output current measurements are used to select which arms should be clamped. The arms that are candidates for clamping are those with the highest upper arm reference signal or the lowest lower arm reference signal. In order to reduce switching power losses, the final arm to be clamped is the one that belongs to a phase-leg with the highest absolute value of the output current.

8.3.1 Feed-Forward Voltage Compensation

The capacitor voltage ripples modify the voltage provided by the MMC arms. If the capacitor voltage ripples are small, the modification does not significantly affect the output voltages and currents. However, if the capacitor voltage ripples are large (such as when the motor operates at low speed/frequency), the output voltages can differ

significantly in respect to those that are expected. In order to avoid voltage distortion, the fourth block of the control scheme implements a feed-forward compensation.

Considering that the capacitor voltages in an arm have very similar values, a ratio between the theoretical capacitor voltage and the real one can be defined as:

$$k_{jz} = \frac{\sum_{n=1}^{N+M} v_{Cjz(n)}}{N+M} \frac{N}{V_{dc}} \,. \tag{8.11}$$

Considering this capacitor voltage ratio, the voltages provided by the upper and lower arms before applying any compensation are:

$$v_{ju} = \frac{V_{dc}}{2} - \left(\frac{-v_{jud} + 1}{2} \right) k_{ju} V_{dc} \text{ and} \tag{8.12}$$

$$v_{jl} = -\frac{V_{dc}}{2} + \left(\frac{v_{jld} + 1}{2} \right) k_{jl} V_{dc} \,. \tag{8.13}$$

It can be seen that the real voltage is highly affected by the capacitor voltage ratio. However, if the ratio is known, the modulation signal can be modified in order to compensate the capacitor voltage ripples:

$$v_{juff} = \frac{v_{jud} + k_{ju} - 1}{k_{ju}} \text{ and} \tag{8.14}$$

$$v_{jlff} = \frac{v_{jld} - k_{jl} + 1}{k_{jl}} \,. \tag{8.15}$$

The feed-forward compensation improves the output voltage quality, mainly when applying large zero-sequence signals. However, as explained in Section 2.6, it disables the energy self-balancing mechanism of the MMC. This is due to the fact that the circulating current is no longer dependent on the capacitor voltages. For this reason, a system with feed-forward compensation requires a fast energy control algorithm.

8.4 Modulated Energy Controller

The implementation of an energy balancing controller based on injecting a fundamental component into the circulating current was presented in [7]. This technique is based on the energy transfer that occurs when multiplying a sinusoidal inner arm voltage by a sinusoidal differential current with the same phase. However, a sinusoidal voltage is not the optimal reference when the main component of the inner arm voltage is not the fundamental voltage. When applying discontinuous modulation, the arm voltage

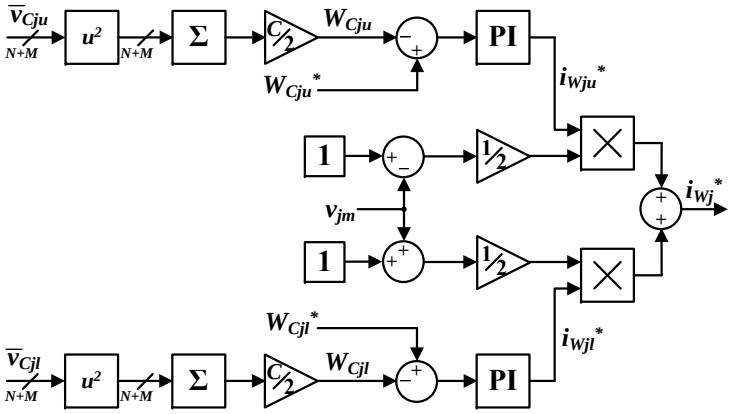


FIGURE 8.3: Block diagram of the proposed MEC.

includes multiple harmonic components, which can be dominant at low modulation indices. In order to improve energy balancing, a new energy control technique, named MEC, is proposed. This technique injects a circulating current proportional to the modulation signal and can be adapted to any kind of control strategy.

In the MEC technique, two control loops are implemented, one for each arm. Each control loop regulates the energy stored in the upper (W_{Cju}) or lower (W_{Cjl}) arms individually, thus defining two different current references (i^*_{Wju} and i^*_{Wjl}). Those references are then weighted with the arm voltage, since the energy control has more effect on the higher voltage arm and less effect on the lower voltage arm. Both weighted references are added, which then define the energy control current reference:

$$i^*_{Wj} = i^*_{Wju}\frac{1 - v_{jm}}{2} + i^*_{Wjl}\frac{1 + v_{jm}}{2} \ . \tag{8.16}$$

This equation applies the current references proportionally to the number of SMs activated in each arm, thus improving the energy control. As an example, when the modulation signal is 1 and hence no SMs are activated in the upper arm, the energy control current reference for the upper arm is multiplied by zero, since this reference would have no effect on the capacitor voltages. In contrast, the energy control current reference for the lower arm is multiplied by one, since all the SMs in that arm are activated and it has the maximum effect.

The MEC not only regulates the energy balance between the upper and lower arms, but also the average energy value in each arm. The average control is performed because the current references are not calculated from the energy difference between the arms, but instead from the error between the energy reference and the measured arm energy. A block diagram of the proposed MEC is depicted in Fig. 8.3.

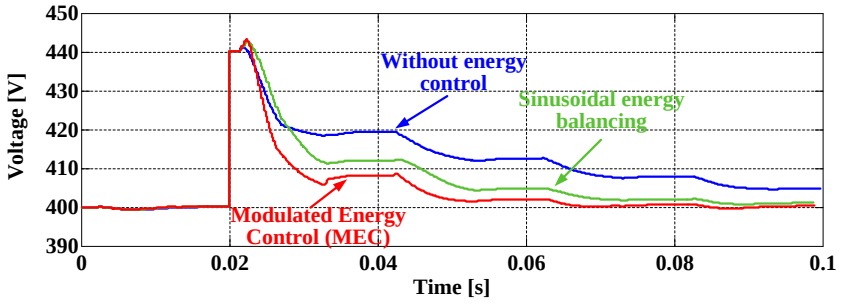


FIGURE 8.4: Simulation results. Upper arm capacitor voltage when a voltage imbalance is applied. Comparison of the MEC with the traditional sinusoidal energy balancing technique and also without any energy controller.

Simulation results using a switched model of the MMC with 4 SMs per arm ($N = 3$ and $M = 1$) have been obtained to demonstrate the effectiveness of the MEC. In order to reduce the duration of the transient and nonideal effects that would appear in a motor drive, the results have been obtained with high voltage values ($V_{dc} = 1200$ V) and operating with an RL load (10 Ω and 3 mH).

Fig. 8.4 shows the capacitor voltages of the upper arm when applying different control strategies: without energy balancing control, with sinusoidal energy balancing control, and with the proposed MEC. In the three cases, an initial voltage imbalance of 10% is applied at $t = 0.2$ s. CL-DPWM is applied over a sinusoidal reference signal with low modulation index ($m = 0.1$) which is the operation point of the motor drive at low speed. In order to accelerate the simulation, the a 50 Hz reference has been used. Fig. 8.4 demonstrates that the proposed technique balances the SM voltages faster than the other techniques.

8.5 Benchmarking Techniques

The CL-DPWM performance for the MMC motor drive application has been compared with three modulation techniques: the basic CB-SVPWM and two state-of-the-art techniques for low-speed operation. The low-frequency techniques used for benchmarking are based on two types of injections: the first injects a sinusoidal zero-sequence component and a sinusoidal circulating current [94], hereinafter called CMsin; and the second injects a square-wave zero-sequence component and a square-wave circulating current [47], hereinafter called CMsqr.

The low-frequency operation techniques are based on the injection of a constant frequency zero-sequence component that is complemented with a circulating current. The circulating current includes two terms: a double fundamental frequency term, which is based on (2.23) and is used for compensating the common-mode power fluctuations in

TABLE 8.1: Specifications of the Benchmarking Techniques

Parameter	**Value**
Amplitude of the CMsin and CMsqr zero-sequence, U_{sin} and U_{sqr}	40 V
Frequency of the CMsin and CMsqr zero-sequence, f_{sin} and f_{sqr}	50 Hz

the arms; and a second term that pulses at the zero-sequence frequency, which compensates the differential-mode power fluctuations.

In order to perform fair comparisons, the techniques are implemented in the same way: the zero-sequence component is added to the voltage references provided by the FOC algorithm, and the differential control signal is applied afterwards. For each technique, circulating current is complemented with the reference provided by the MEC technique. The circulating current reference for the CB-SVPWM is calculated from the instantaneous values of current and modulation signal (2.23).

The CMsin modulation contains a sinusoidal zero-sequence component with amplitude U_{sin} and angular frequency ω_{sin}. The amplitude has to be large enough to reduce the capacitor voltage ripples and minimize the circulating currents, which are inversely proportional to the zero-sequence voltage amplitude. However, the amplitude of the zero sequence is limited by the modulation range. The values of U_{sin} and f_{sin} ($f_{sin} = \omega_{sin}/2\pi$) used in the experimental results are shown in Table 8.1. The zero-sequence voltage and circulating current reference used in CMsin are:

$$v_{sin} = U_{sin}\sin(\omega_{sin}t) \text{ and} \tag{8.17}$$

$$i^*_{j\,diff\,sin} = \frac{i_j v_{jm}}{2} - \frac{V_{dc}}{2\,U_{sin}}\left(v_{jm}^2 - 1\right) i_j \sin(\omega_{sin}t)\ . \tag{8.18}$$

The CMsqr is based on a square-wave zero-sequence signal and has the advantage of requiring lower circulating currents for the same zero-sequence amplitude. As shown in Table 8.1, the amplitude U_{sqr} and frequency f_{sqr} have been chosen the same as in CMsin. The zero-sequence voltage and circulating current in CMsqr are:

$$v_{sqr} = \begin{cases} -U_{sqr} & \text{if } 0 < t < \dfrac{1}{2f_{sqr}} \\ U_{sqr} & \text{if } \dfrac{1}{2f_{sqr}} < t < \dfrac{1}{f_{sqr}} \end{cases} \text{ and} \tag{8.19}$$

$$i^*_{j\,diff\,sqr} = \begin{cases} \dfrac{i_j v_{jm}}{2} + \dfrac{V_{dc}}{4\,U_{sqr}}\left(v_{jm}^2 - 1\right) i_j & \text{if } 0 < t < \dfrac{1}{2f_{sqr}} \\ \dfrac{i_j v_{jm}}{2} - \dfrac{V_{dc}}{4\,U_{sqr}}\left(v_{jm}^2 - 1\right) i_j & \text{if } \dfrac{1}{2f_{sqr}} < t < \dfrac{1}{f_{sqr}} \end{cases}\ . \tag{8.20}$$

TABLE 8.2: Specifications of the Laboratory Prototype Used for the Motor Drive

Parameter	**Value**
Number of Basic SMs per Arm, N	3
Number of Additional SMs per Arm, M	1
SM Capacitors, C	$1500\,\mu$F
Arm Inductors, L	3 mH
DC-Link Voltage, V_{dc}	120 V
Carrier Frequency, f_{cr}	5 kHz

TABLE 8.3: Specifications of the PMSM

Parameter	**Value**
Nominal Power, P_N	200 W
Rated Current, I_N	2 A
Rated Torque, T_e	0.64 Nm
Nominal Speed, ω_N	3000 r/min
Pole Pairs, p	4
Stator Inductors, L_d and L_q	8.45 mH
Stator Resistance, R_s	2.5 Ω
Magnet Flux, λ_m	0.045 Wb

8.6 Experimental Results

Experimental results were obtained from the TIEG-P prototype, which was configured as a three-phase MMC. The SiC-based converter is composed of three basic SMs ($N = 3$) per arm, plus an additional one ($M = 1$). The motor driven in this application is a 200-W PMSM Yaskawa Servomotor 02CE2. The main data of the converter and the PMSM are shown in Tables 8.3 and 8.3, respectively. Different experiments were conducted at speeds of 1500 r/min, 120 r/min, 90 r/min and 30 r/min, which represent 50%, 4%, 3% and 1% of the rated speeds, respectively. All those experiments were performed with a constant torque load of 70% of the rated torque. Except for those in Subsection 8.6.2, the experiments were conducted without activating the feed-forward compensation.

8.6.1 Minimum Speed with CB-SVPWM

The first experiment was conducted in order to determine the minimum speed that a normal modulation technique (CB-SVPWM) is able to reach. Fig. 8.5 presents the experimental results obtained for all modulation techniques at a speed of 120 r/min

and load torque of 70% of rated torque (equivalent rms current of 1.4 A). Fig. 8.5(a) shows the upper arm capacitor voltages operating with CB-SVPWM. The peak-to-peak voltage is 10 V, which is 25% of the average voltage (V_{Cavg}=40 V). This is the minimum speed that can be achieved with this modulation technique, since lower speeds produce excessive capacitor voltage ripples that cause instability. Figs. 8.5(b) and (c) show the capacitor voltages when using CMsin and CMsqr, respectively. In these cases, the capacitor voltage ripples are lower, with peak-to-peak values of 6 V with CMsin and of 5 V with CMsqr. Finally, Fig. 8.5(d) depicts the capacitor voltages produced with CL-DPWM. The peak-to-peak voltage obtained with CL-DPWM is slightly smaller than that produced by CMsqr.

8.6.2 Feed-forward Compensation

Low-frequency techniques are beneficial for reducing capacitor voltage ripples but they also present some issues, such as distortion at the output voltages and currents. In order to avoid this distortion, the feed-forward voltage compensation can be applied. The current distortion and its compensation can be observed in Fig. 8.6. The first time interval in Fig. 8.6 shows the PMSM currents while using the low-frequency techniques with no feed-forward compensation. Some distortion appears with all the low-frequency techniques, but it is more significant with CMsin and CMsqr, both of which present a superimposed high-frequency ripple. Nevertheless, when the feed-forward compensation is activated in the second time interval of Fig. 8.6, the current distortion is practically eliminated. This is because the feed-forward compensation generates output voltages that are very close to the theoretical ones.

Feed-forward voltage compensation improves the quality of the output voltages and currents, but presents two main disadvantages. First of all, the feed-forward compensation disables the energy self-balancing that the converter performs naturally. In order to ensure system stability, a fast energy balancing controller is needed. However, the existing energy balancing techniques, and so the MEC, regulate the average energy in a fundamental period. This fact limits the dynamic response of the controller to the fundamental frequency, which at low-speed operation is very low. For this reason, the stability of the system is limited when using the feed-forward compensation technique, with 90 r/min being the minimum stable speed that can be achieved by the feed-forward compensation.

A second disadvantage of the feed-forward compensation is that it changes the interaction between circulating currents and zero-sequence signals. This reduces the power fluctuation compensation of the low-speed modulation techniques, thus increasing the

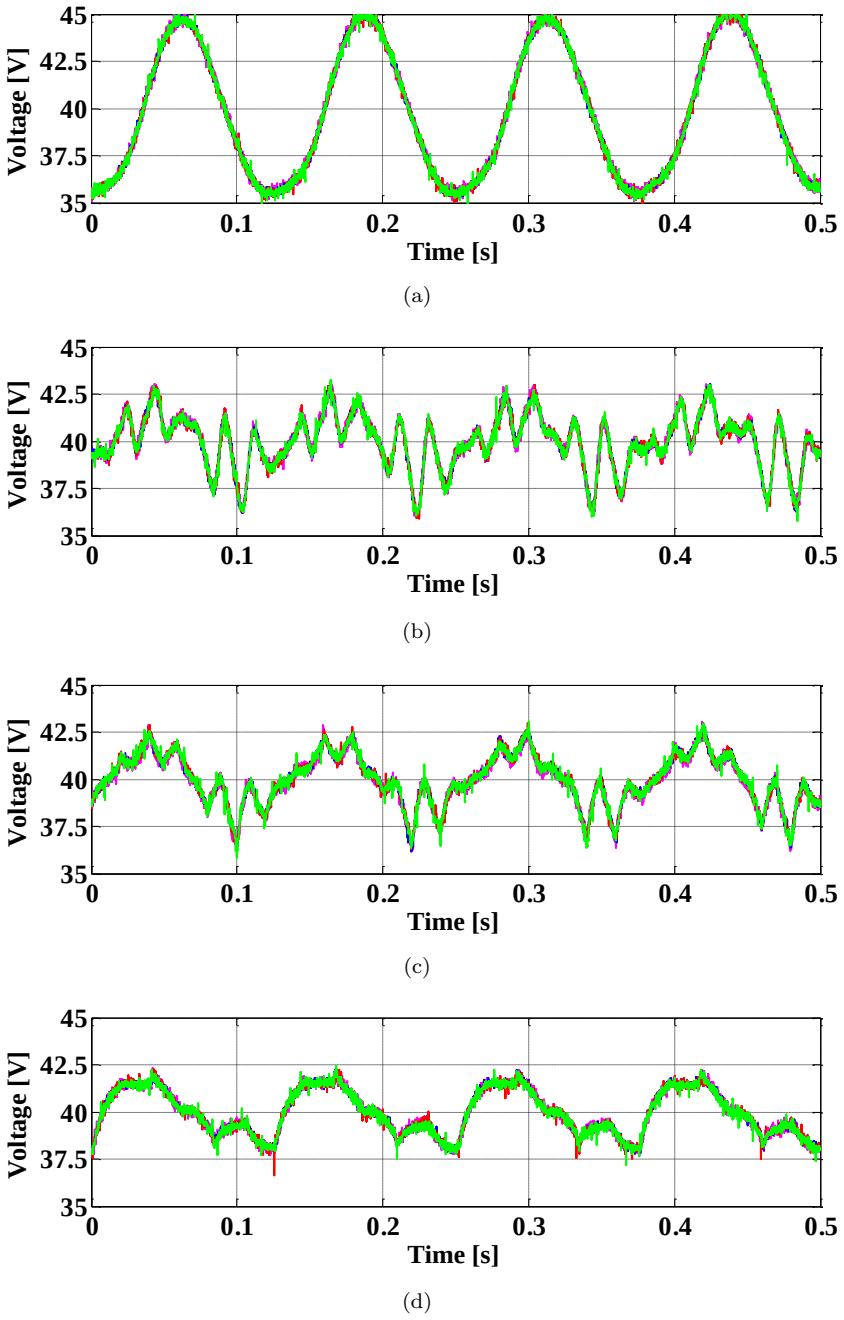
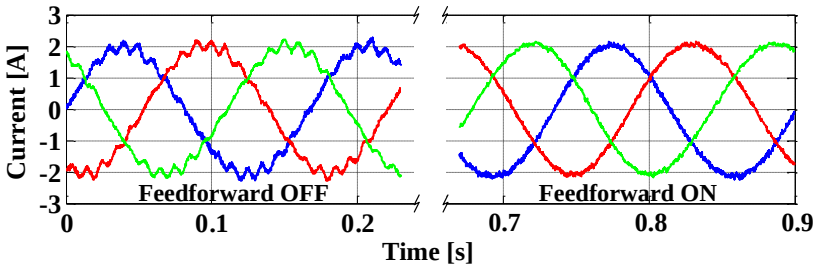
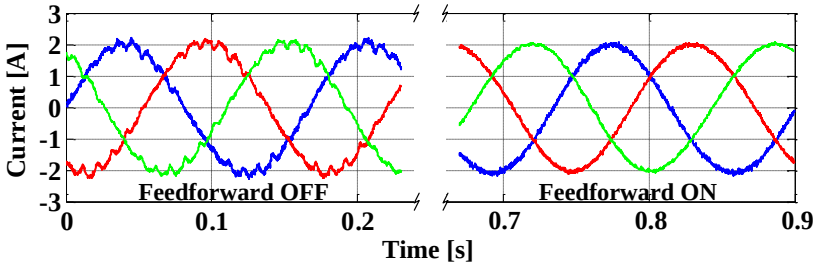


FIGURE 8.5: Experimental results at the minimum speed achieved by CB-SVPWM (120 r/min). Upper arm capacitor voltages with: (a) CB-SVPWM, (b) CMsin, (c) CMsqr and (d) CL-DPWM.

capacitor voltage ripples. Fig. 8.7 shows the capacitor voltages with and without feed-forward compensation at a speed of 90 r/min. As can be seen, the capacitor voltage ripples increase when the feed-forward compensation is activated. The peak-to-peak voltage ripples increase up to 7.5 V and 9 V with CMsin and CMsqr, respectively. However, the peak-to-peak voltage ripple increases up to 20 V in the case of CL-DPWM.



(a)



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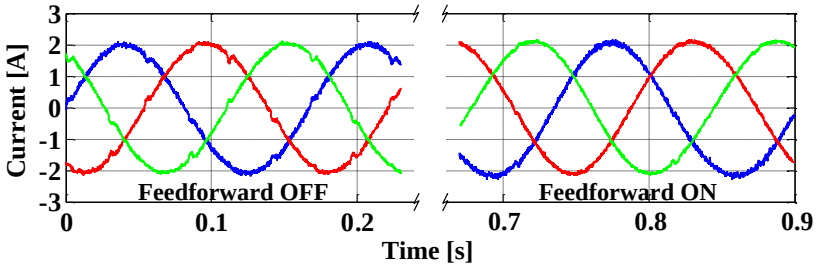


(c)

FIGURE 8.6: Experimental results obtained with and without the feed-forward compensation at 90 r/min. Stator currents obtained with different control techniques: (a) CMsin, (b) CMsqr and (c) CL-DPWM.

8.6.3 Very Low-Speed Operation

In order to highlight the advantages of CL-DPWM, the capacitor voltage ripples and circulating currents at a very low speed are compared with those obtained with CMsin and CMsqr. The capacitor voltages at 30 r/min (1% of the rated speed) are shown in Fig. 8.8. All techniques maintain acceptable values of voltage ripples, with a maximum peak-to-peak value of 10 V with CMsin, as shown in Fig. 8.8(a). CMsqr and CL-DPWM, depicted in Figs. 8.8(b) and (c), present lower voltage ripples, with a peak-to-peak value of 7.5 V each.

The amplitude of the capacitor voltage ripples of CL-DPWM and CMsqr are very similar, but not the values of the circulating currents. As can be seen in Fig. 8.9, where the reference and measured circulating currents are shown in red and blue colours, respectively, CMsin produces the highest circulating currents, with a peak value of 3 A

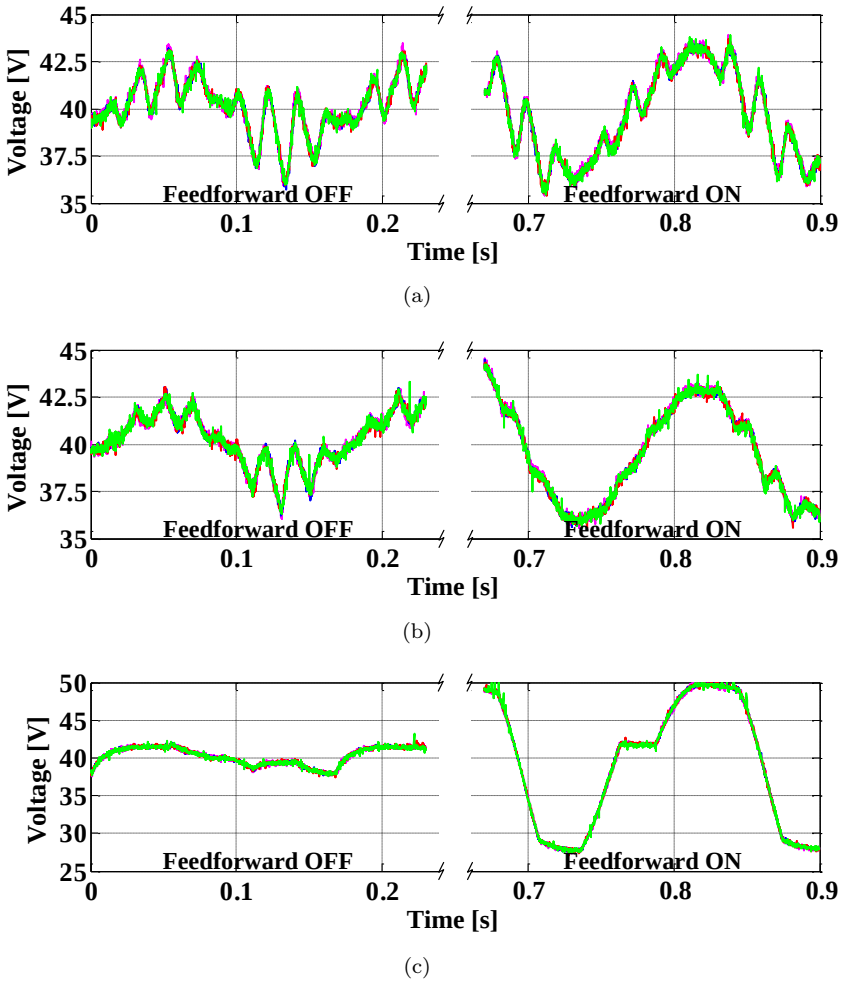
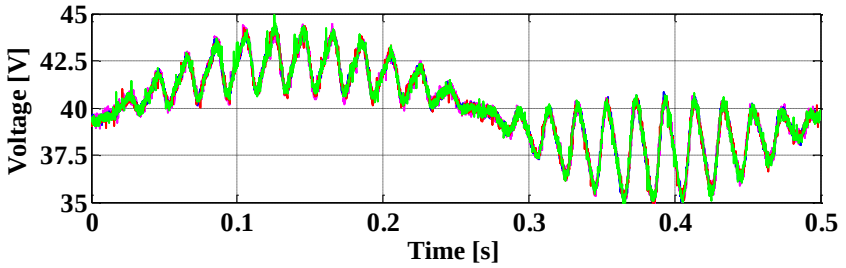


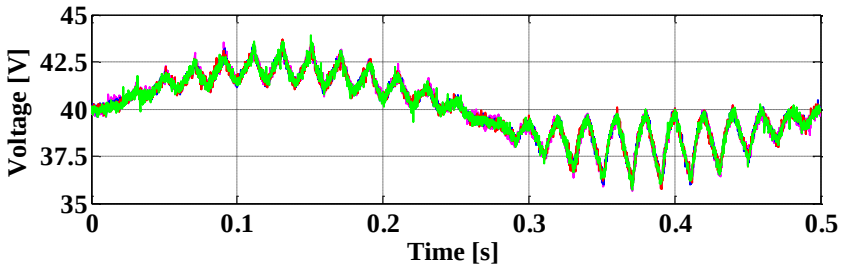
FIGURE 8.7: Experimental results obtained with and without the feed-forward compensation at 90 r/min. Upper arm capacitor voltages obtained with different control techniques: (a) CMsin, (b) CMsqr and (c) CL-DPWM.

and rms value of 1.47 A. As expected from [47], CMsqr requires a smaller circulating current, with a measured peak value of 2.3 A, but a reference of 1.7 A and a rms value of 1.17 A. Finally, CL-DPWM produces the lowest circulating currents. Although the peak value of its current reference is 0.85 A, it has a measured peak value of 2.4 A. These peaks are caused by the capacitor voltage ripples. Since the capacitor voltages are not at the reference value, the voltage applied to the arm inductors changes suddenly during the clamping transitions, causing a pulse in the circulating current. Nevertheless, these current peaks are very short and they do not much affect the rms value of the circulating current, which is only 0.85 A, 30% less than that with CMsqr. As a result, it can be deducted that CL-DPWM also reduces the conduction losses of the converter when compared to CMsqr and CMsin.

In order to demonstrate the power loss reduction of the CL-DPWM technique, the efficiency of the different techniques has been measured. Fig. 8.10 shows the efficiency



(a)



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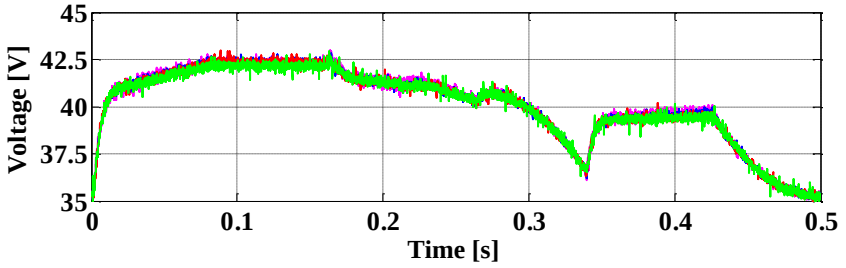
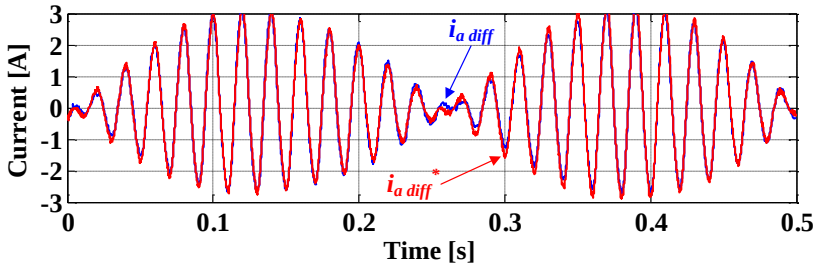


(c)

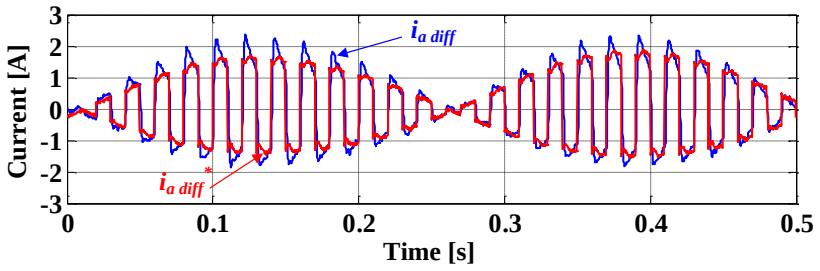
FIGURE 8.8: Experimental results obtained at the speed of 30 r/min. Capacitor voltage with: (a) CMsin, (b) CMsqr and (c) CL-DPWM.

of the converter when using the four techniques studied in the speed range of 30 r/min to 150 r/min (CB-SVPWM was tested only from 120 r/min to 150 r/min). In all the cases, the same load torque has been applied. The efficiency values were measured with a YOKOGAWA WT1600 Digital Power Meter.

Fig. 8.10 demonstrates that CL-DPWM is the most efficient low-speed modulation technique, with efficiency values ranging from 76% to 85%. In contrast, CMsin is the least efficient one, with efficiency values ranging from 58% at 30 r/min to 69% at 150 r/min. The reduction in power losses with CL-DPWM is mostly due to the reduction in the circulating current values, and therefore in the conduction losses. The switching power losses do not play an important role in this analysis, since the MMC prototype is comprised of SiC devices, which have very small switching losses. For this reason, CB-SVPWM is the most efficient at the operating points where it can be applied (i.e., medium and high speeds), since it requires small circulating currents.



(a)



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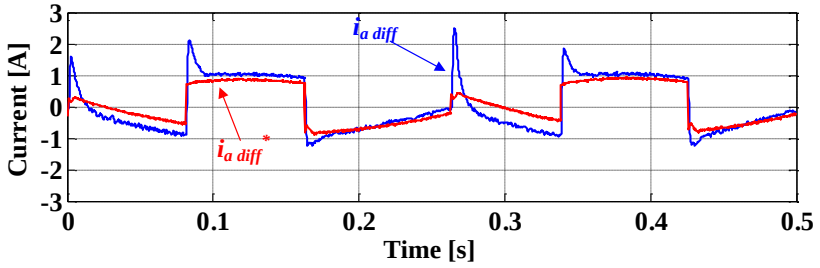


(c)

FIGURE 8.9: Experimental results obtained at very low speed (30 r/min). Reference and measured circulating current in phase-leg a obtained with: (a) CMsin, (b) CMsqr and (c) CL-DPWM.

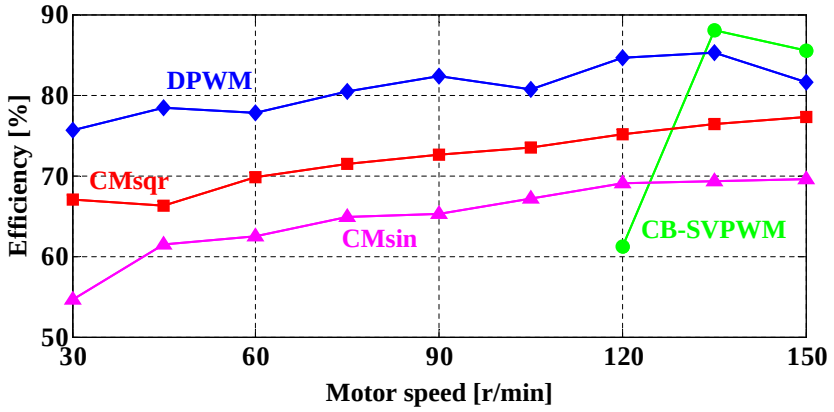
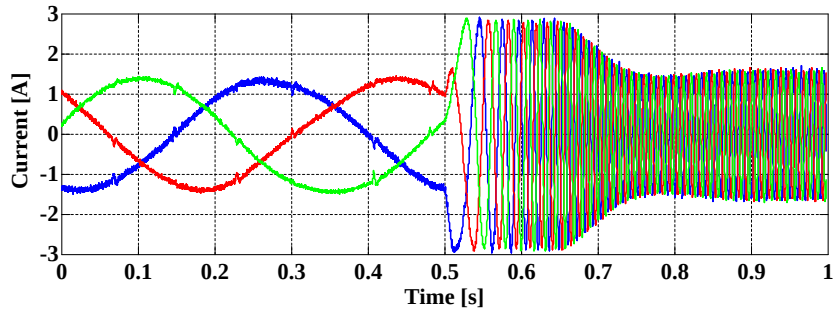
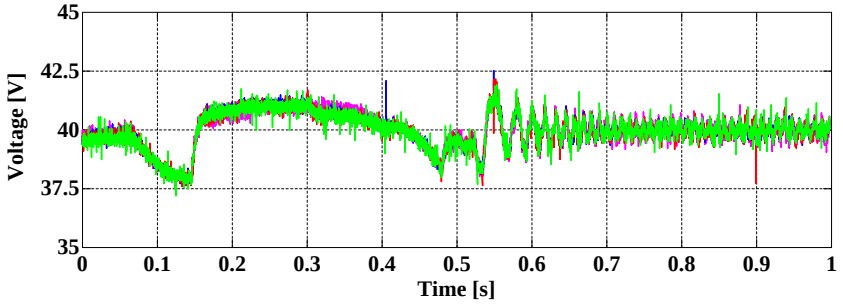


FIGURE 8.10: Efficiency of the converter in the speed range of 30 r/min to 150 r/min.



(a)



(b)

FIGURE 8.11: Experimental results when applying a step change in the speed reference from 30 r/min to 1500 r/min (1% to 50% of the nominal speed) at t=0.5 s: output currents (a) and capacitor voltages (b), obtained with CL-DPWM.

8.6.4 Speed Range and Dynamic Performance

The speed range of CMsin and CMsqr is limited, since they are based on the injection of a constant frequency zero-sequence component. When the fundamental frequency is close to the zero-sequence frequency, the system becomes unstable, and additional algorithms have to be added to switch from the low-speed modulation technique to a medium- or high-speed modulation technique [116, 143]

In contrast, CL-DPWM does not operate at a fixed frequency, since its zero-sequence signal is calculated from the output currents and the voltage reference signals. This allows the CL-DPWM to perform very well at both low and high speeds.

Fig. 8.11 shows the dynamic performance of the converter when a reference step from 30 r/min to 1500 r/min (1% to 50% of the nominal speed) is applied to the speed controller. The modulation technique does not affect the dynamics of this speed change, which only depends on the motor dynamics and the tuning of the FOC controllers.

Fig. 8.11 (a) depicts the output currents of the converter. As can be seen, there is a fast increase in the current frequency, and therefore in the motor speed. The CL-DPWM modulation technique does not disturb the dynamics of the system.

Fig. 8.11 (b) shows the SM capacitor voltages during the speed reference step. It can be observed that the capacitor voltage ripples are maintained consistently low, with their maximum value occurring at low speed and reducing with the increase in speed. The voltage peaks that appear at t=0.4 s and t=0.9 s are caused by the measuring noise.

8.7 Conclusion

In this chapter, the effectiveness of discontinuous modulation for applying MMCs in motor drive applications has been studied. Discontinuous modulation was adapted for use in a PMSM drive, which includes the design of a new energy control system for modulation techniques with high zero-sequence injection. The effectiveness of these techniques has been demonstrated with simulation and experimental results. Operation of the PMSM at low speeds was tested and benchmarked against other low-speed techniques based on the injection of sinusoidal and square-wave zero sequences. The results demonstrate the capability of discontinuous modulation for reducing capacitor voltage ripples, thus allowing the PMSM to operate at very low speeds with capacitor voltage ripple amplitudes that are similar to those obtained with other state-of-the-art techniques. Moreover, when compared to other low-speed techniques, discontinuous modulation reduces the power losses and hence increases converter efficiency.

Chapter 9

Conclusions and Future Research

This chapter summarizes the main conclusions of this thesis and introduces some future research topics that can be derived from it.

9.1 Conclusion

Improvement of the MMC topology and its control are some of the main research topics in the field of power electronics. For this reason, making any notable contribution to the current state-of-the-art is a difficult challenge. In this thesis, some of the main problems with the MMC have been studied and new solutions have been proposed with the objective of advancing knowledge of the converter and improving its performance.

One of the problems with the MMC is the size and cost of the SM capacitors. SM capacitance is essentially defined by the capacitor voltage ripples, which can be reduced with the injection of selective harmonic components into the circulating current. This topic is studied in Chapter 3, which presents three techniques for calculating the circulating current reference. The first technique presents an optimization method for calculating a reference based on a second harmonic current. However, this technique is based on a function approximation of the capacitor voltage ripples, because the original function is not continuous. A second technique proposes an iterative optimization method, which finds the optimal values of the second and fourth harmonics in order to reduce the capacitor voltage ripples. The current determined by this technique can be considered the optimal one, since the technique evaluates the capacitor voltage ripples for all possible combinations of amplitudes and phases of the harmonics before selecting the best ones. The problem with this technique is that it has to be calculated off-line, since it requires a lot of processing resources. It also increases the rms value of the current, and therefore, the conduction losses. The most interesting aspect of this technique

is that it can be used for benchmarking. A third technique is proposed, in which two equivalent models of the MMC find two current references that can be calculated from the instantaneous values of the current and modulation signals. This third technique produces capacitor voltage ripple amplitudes close to the optimal circulating current, but with the advantage of being calculated on-line. Furthermore, it does not increase the rms current value as much as the optimal method.

A different approach for reducing the capacitor voltage ripples is presented in Chapter 4. In this chapter, discontinuous modulation, a technique based on the injection of a zero-sequence signal into the modulation references, is applied to the MMC. The discontinuous modulation clamps a phase-leg to the upper or lower terminals of the dc-link for a short period of time, which avoids switching transitions in the clamped arm and therefore reduces the switching power losses of the converter. Moreover, this technique also highly reduces the capacitor voltage ripples because the major part of the phase current flows through the clamped arm, where no SMs are activated. The capacitor voltage ripples are reduced mainly for low modulation indices and thus enable the use of the MMC in motor drive applications, where the capacitor voltage ripples become excessive when operating with low modulation indices, i.e., low speeds/frequencies.

Three approaches for discontinuous modulation are presented: an open-loop implementation (OL-DPWM) based on constant clamping intervals; a closed-loop approach (CL-DPWM) that selects the clamping periods according to the maximum output current, thus improving efficiency and capacitor voltage ripples; and a third approach (VD-PWM) that is suitable for medium-power applications, i.e., MMCs with a low number of SMs. The last approach is especially recommended for converters that are based on silicon-carbide technology, where switching power losses are far lower than conduction power losses.

In Chapter 5, one of the main problems with the practical implementation of the MMC is studied: the measurement of the capacitor voltages in converters with a high number of SMs. A new voltage measuring technique is presented, where each sensor is able to measure the voltages of multiple SMs. The sensors measure the output voltage provided by a set of SMs, thus acquiring the voltage when only one SM in the set is activated. The acquired voltage corresponds to the capacitor voltage of the activated SM minus the voltage drop in the semiconductors, which can be easily estimated or neglected. Between actual measures, the capacitor voltage ripples are estimated, which allows maintaining good voltage balance within the arm. Since the estimator is updated with actual measures of the voltages, the estimation error is not accumulated. This technique requires a minimum of two sensors per arm; but, for converters with a high number of SMs, more sensors can be used. Even so, the technique highly reduces

the number of required sensors in the MMC, thus also reducing the cost of the data acquisition system.

A second industrial-focused technique that has been developed is a fault-tolerant strategy for the MMC. In Chapter 6, a technique is developed for detecting, localizing and correcting faults in the SM semiconductors and in the capacitor voltage sensors. The technique is based on the addition of a minimum of three sensors per arm: two arranged like the voltage measuring technique developed in Chapter 5, and one measuring the voltage provided by the whole arm. If the voltage measured by the sensors is different from the expected voltage, a fault is detected. Once the fault is identified (fault in a sensor, open-circuit in a semiconductor or short-circuit in a semiconductor) and localized, it is corrected. If the fault appears in a sensor, it is substituted with the voltage measuring technique introduced in Chapter 5. If the fault is in an SM, it is simply deactivated because some redundant SMs are assumed to be included in the arms. This method requires only minor additional costs and provides a robust and fast response to MMC faults (they can be detected and corrected in less than 5 milliseconds).

Another approach for improving system reliability is to reduce the possibilities of failure. Semiconductor ageing is caused mainly by thermal stress due to power losses. For this reason, it is important to minimize power losses and to distribute them evenly among the switching devices of the converter. In Chapter 7, the distribution of the power losses in an MMC with capacitance differences is studied. Due to manufacturing tolerances or ageing of the capacitors, capacitance differences are common in real converters and cause unbalanced power losses in the switching devices. In order to address this situation, a loss balancing strategy is presented, which is based on modifying the input signals of the capacitor voltage balancing algorithm. Two algorithms are proposed: one for balancing the number of switching transitions, and another for balancing the individual losses of each semiconductor. Simulation and experimental results demonstrate a reduction in power loss imbalances at the cost of a small increase in capacitor voltage ripples. The proposed strategy can also be used to force imbalances in the distribution of semiconductor power losses. This can be useful in MMCs where the physical location and cooling conditions of the SMs produce uneven distribution of heat dissipation.

Finally, the use of the MMC in motor drive applications has been studied. The main problem with this application is the excessive capacitor voltage ripples that appear at low frequencies/speeds, which occurs because, with sinusoidal modulation, the capacitor voltage ripples are inversely proportional to the frequency. In Chapter 8, the use of discontinuous modulation in a low-speed motor drive application is studied and tested in a PMSM. Mathematical development demonstrates that if the ratio between modulation index and frequency is constant, capacitor voltage ripples with discontinuous

modulation are not inversely proportional to the frequency. This allows operating the MMC-based motor drive at very low speeds (1% of the nominal speed). The technique is benchmarked against other state-of-the-art low-speed operation techniques, which are based on the injection of sinusoidal and square-wave zero-sequences. Experimental results demonstrate that discontinuous modulation reduces the capacitor voltage ripples as much as the benchmarking techniques, while also increasing the efficiency of the converter.

9.2 Future Research

New research areas can be foreseen from the work developed in this thesis. Some of these ideas are suggested next.

- **Development of a faster optimization algorithm for the circulating current reference**

  In this thesis, an iterative optimization algorithm has been developed for calculating the circulating current reference that minimizes the capacitor voltages. The iterative optimization algorithm finds the amplitude and phase of the second and fourth harmonics of the circulating current, but it requires a lot of processing resources and has to be calculated off-line. In a common personal computer, this process can take several days. The use of more advanced optimization techniques for this process could be investigated. Even if it were an off-line processing technique, a faster method could be useful for studying the effect of higher harmonic components, or for optimizing the circulating current in non-sinusoidal modulation techniques.

- **Effects of the circulating current components in MMCs with back-to-back topologies**

  Injecting harmonic components into the circulating current is considered to have no effect on the dc-link, because the harmonics in a three-phase system are cancelled (except the harmonics multiple of three, which are never injected). However, the injection of a first harmonic for balancing the energy between the upper and lower arms will not be cancelled, since it is calculated individually for each phase-leg. This current component could cause problems in back-to-back configurations, where two different MMCs share the same dc-link. A phase-leg energy controller with harmonic cancellation has been developed [144], but the topic can be further investigated.

- **Effects of inductance mismatches between the arms**

  The effects of capacitance voltage differences between the SMs has been studied, with power loss imbalances being observed in the SMs. Capacitance differences are generally caused by manufacturing tolerances. In the same way, inductance values are affected by tolerances. The equivalent common mode circuit of the MMC suggests that inductance mismatch can cause output voltage distortion. One research area that has never been studied is the particular effects of inductance tolerances in the MMC and methods for detecting and correcting these effects.

- **Implementation of the loss balancing algorithm in a high-power MMC and switching power loss measuring techniques**

  SM capacitance mismatches create power loss imbalances that can be corrected with a balancing strategy. However, this technique has been tested experimentally only in a low-power MMC prototype. The immediate follow-up to this topic is testing this technique in medium- or high-power converters. Another research direction that can be derived from this topic is finding a method for measuring or accurately estimating the switching power losses in the SMs of the MMC.

- **Improvement of the feed-forward voltage compensation for discontinuous modulation**

  In the motor drive application of the MMC, a voltage controlling technique based on a feed-forward compensation is applied. This technique improves the output voltage and current, but highly increases the capacitor voltage ripples when using discontinuous modulation. Moreover, it becomes unstable at very low speeds. Further research could be done on the voltage controller, both by improving its application and by developing an energy controller with a faster dynamic.

- **FPGA implementation of voltage balancing algorithms for a high number of SMs**

  Capacitor voltage balancing algorithms have been widely studied. Most techniques are studied by simulation or implemented in low-power prototypes. However, their implementation in MMCs with a high number of SMs can become a problem. The implementation of a voltage sorting algorithm in an FPGA requires a lot of processing resources. One study based on an MMC with 44 SMs per arm proposes a distributed voltage balancing algorithm [55], which requires fewer hardware processing resources. This topic could be further investigated. A first approach would be to consider that all the SMs in the same state (on or off) have the same increase or decrease in voltage, since the current flowing through them is the same. Consequently, they maintain the same relative activation priority. This premise can be used for simplifying the sorting algorithm.

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