Joint Symbol and Chip Synchronization for a Burst-Mode-Communication Superregenerative MSK Receiver

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Abstract—In this paper we describe a superregenerative (SR) MSK receiver able to operate in a burst-mode framework where synchronization is required for each packet. The receiver is based on an SR oscillator which provides samples of the incoming instantaneous phase trajectories. We develop a simple yet effective technique to achieve joint chip and symbol synchronization within the time limits of a suitable preamble. We develop some general results and focus on the case of the IEEE 802.15.4 MSK physical layer. We provide details on a VHDL implementation on an FPGA where the most complex digital processing block is an accumulator. Simulation and experimental results are provided to validate the described technique.

Index Terms—Low-power communication receivers, MSK demodulation, RF receivers, superregenerative receiver, synchronization.

I. INTRODUCTION

SUPERREGENERATIVE (SR) Receivers (SRR) are among the most energy-efficient detectors for wireless data reception. They were introduced almost a century ago [1] but were later relegated to low demanding applications due to the superiority of superheterodyne receivers in terms of selectivity. The last years have seen a significant increase in SR-related research trying to take advantage of the intrinsic properties of SRR [2] [3], namely their low-complexity structure that allows low-power [4] and/or low-cost implementations. These advantages are at the expense of a sub-optimum performance mainly due an equivalent noise bandwith greater than the theoretical minimum for conventional modulations [5]. Several of today's wireless communication needs may be served by SRR thanks to recent demonstrations of the SR principle to PSK [6] [7] and FSK/MSK modulations [8]. As it is well-known, the synchronization problem (which appears at many levels) is a main issue in receiver design, accounting for a significant fraction of receiver cost in terms of area or consumption [9]. In the SR context, very low-complexity synchronization approaches are to be targeted to avoid spoiling the whole point of SR reception.

Digital communications can be classified as burst-mode or continuous transmissions, each placing different requirements on the synchronization scheme. In burst-mode, also called packet communications, each data packet has a training sequence (sometimes called preamble) to achieve carrier, chip and symbol synchronization. In some cases, once acquired, synchronization can be maintained until the end of the packet thanks to the stability of the crystal oscillators.

The synchronization problem in SR receivers for ASK modulations has received some attention, e.g., in [4] or [10]. Recently [11], an asynchronous preamble based on pseudo-noise sequences with amplitude-modulated pulses with a suitable pulse shaping function, combined with a fractional symbol period delay, is proposed. There, the SR oscillator (SRO) signal is fed to an envelope detector and chip and symbol synchronization is achieved thanks to a suitable processing scheme.

MSK modulation [12] belongs to the class of continuous phase modulations (CPM), and is equivalent to an offset quadrature phase shift keying (OQPSK) modulation with half-sine pulse shaping [13]. MSK exhibits low bandwidth, constant envelope for efficient power amplification, and achieves QPSK bit error rate (BER) for so called precoded-type MSK. These properties make MSK the choice for power-efficient wireless networks such as IEEE 802.15.4 [14].

The SRR has recently been shown to be able to detect MSK signals: in the approach in [8], a SR front end is able to deliver samples of the instantaneous received signal phase using 1-bit ADC. In conventional MSK receivers, after preamplification and IQ downconversion, the I and Q signals are digitized and synchronization and data detection is achieved by digital signal processing techniques. This is a flexible approach at the expense of a non-negligible amount of hardware resources and power consumption.

There is a wealth of literature describing different synchronization approaches. Basic material is presented in [9], [13] while more recent results may be easily found, for instance, in [15] and references therein. Some of them require sampling the phase trajectories with a sampling frequency higher than the MSK symbol rate f_x, with $\times 8$ factors being common [16]. For instance, [17] describes a method that is well-suited for digital implementation with a sampling rate that is only twice the symbol rate. This is also the case of, e.g., [18]. On the other hand, timing recovery techniques such as [19] or [20], while operating at the symbol rate, do not achieve the higher

level synchronization (chip and symbol) required, for instance, for IEEE 802.15.4.

Following [9], the possible approaches to synchronization can be divided into two categories: ad-hoc and derived structure. In the ad-hoc structure case, an a-priori proposed hardware is thought to be able to address the problem. In the derived structure case, the structure is obtained as the solution to an optimization problem, with no a priori guesses.

In the case of the SR receiver, a sampling frequency higher than f_x would imply a wider receiver bandwidth, meaning lower signal to noise ratio (SNR) [5]. Hence, here we develop a technique that performs joint symbol and chip synchronization after the observation of a known synchronization preamble while operating at f_x. It belongs to the data-aided, ad-hoc structure family of methods. After acquisition, we rely on the stability of the local clock to keep synchronization until the end of the packet. In consonance with the low-cost, low-power and low-complexity objectives of SR reception, the whole synchronization procedure is translated into a simple digital implementation where the most complex digital building block is an accumulator. We present general ideas which may be used for a variety of standards but, due to its specific interest, we concentrate on an implementation targeting the physical level of MSK IEEE 802.15.4 packet reception.

II. FRAMEWORK

In what follows we call *chip* the basic transmission unit lasting T_x seconds, as this is the case with several standards using Direct-Sequence Spread-Spectrum at the physical layer, such as IEEE 802.15.4. However, the whole discussion is also extensible to the cases where the basic transmission unit is a bit. Also, for convenience, chip values will be assumed to be ± 1. First, we recall some results on SR receivers for narrowband FSK [8] receiver. The response of an SRO operating in the linear mode to a signal given by

$$x(t) = \sum_{n=-\infty}^{\infty} p_c(t - nT_x) \cos(\omega_n t + \phi_n) \qquad (1)$$

may be written as [5], [8]

$$s(t) = K_{PG} \sum_{n=-\infty}^{\infty} |H(\omega_n)| p(t - nT_x)$$
$$\times \cos(\omega_0 t + n(\omega_n - \omega_0)T_x + \phi_n + \angle H(\omega_n)), \quad (2)$$

assuming that the changes from stability to instability happen at $t = nT_x$ and that we take one quench cycle per chip, i.e., $T_q = T_x$. The constant K_{PG} (pulse gain) corresponds to the constant K in [5], [8] while K will have a different meaning in this paper.

The expression given by (1) includes MSK making $p_c(t)$ a rectangular pulse occupying the whole chip length, and selecting the instantaneous frequency of the modulated signal as a function of the transmitted digital signal x_n as

$$\omega_n = \omega_c + \omega_d x_n, \qquad (3)$$

with $x_n = \pm 1$, $\omega_d = \omega_x/4$, and choosing ϕ_n such that phase continuity is ensured as corresponds to a continuous-phase FSK modulation [21].
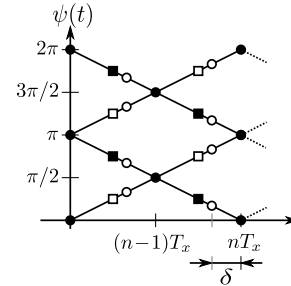

Fig. 1. Representation of the excess phase with respect to $\omega_c t$ as a function of data: black squares correspond to -1, white squares to 1. Black and white circles correspond to nominal or δ-advanced samples, respectively.

From the inspection of (2) we observe that the response is a train of RF pulses, each oscillating at ω_0. While on the transmitter side each chip has the same amplitude, in the received pulse train we observe that each pulse has an amplitude proportional to $|H(\omega_n)|$ which is dependent on the deviation between ω_n and ω_0. The small modulation index of MSK makes the amplitude variations induced by $|H(\omega_n)|$ insufficient for signal detection. These amplitude variations are even further reduced when the SRO is operating near saturation. Hence, suitable MSK detection schemes based on the SR principle rely on the instantaneous phase trajectories of $s(t)$ [8].

A representation of the phase trajectories resulting from an MSK signal at the SRO input is shown in Fig. 1. In the synchronized state, we will sample at multiples of T_x ($\delta = 0$) and the differences between successive phase observations, $\varphi_n = \psi_n - \psi_{n-1}$, will always be $\pm \pi/2$.

However, when acquiring synchronization, there will be an unknown δ added to the nominal sampling instants and φ_n will depend on the transmitted data:

$$\varphi_n(\delta) = \begin{cases} \pi/2 & \text{if } x_{n-1} = x_n = 1 \\ -\pi/2 & \text{if } x_{n-1} = x_n = -1 \\ \pi/2 - \delta\pi/T_x & \text{if } x_{n-1} = -1 \text{ and } x_n = 1 \\ -\pi/2 + \delta\pi/T_x & \text{if } x_{n-1} = 1 \text{ and } x_n = -1 \end{cases} \qquad (4)$$

We call *chip synchronization* the problem of estimating the value of $\delta \in [0, T_x)$.

The second synchronization problem is *symbol synchronization*. In burst-mode transmissions the training sequence in each burst often includes a sequence of known symbols to aid this process. The symbol synchronization problem consists in estimating an integer delay K, between the received and the local training sequences.

In the next section, we will derive a technique to solve both problems simultaneously (together with some comments on carrier synchronization). Frame synchronization will be addressed in Section IV.

III. SIMULTANEOUS SYNCHRONIZATION

Let's define **x** as the vector of N chips in the preamble,

$$\mathbf{x} = [x_0, x_1, \ldots, x_{N-2}, x_{N-1}]^T \qquad (5)$$

From (4), it follows that:

a) The positions n corresponding to two different consecutive chips, i.e., where $x_n \neq x_{n-1}$, give phase values that have a linear dependence with δ. After being filtered, these will be used to achieve *chip synchronization*.

b) The positions n corresponding to two equal consecutive chips do not depend on δ. So, irrespective on the current value of δ, these can be exploited to gain information suitable for *symbol synchronization*.

In order to separate both information sources, $\mathbf{x}$ will be decomposed in two orthogonal terms,

$$\mathbf{x} = \mathbf{i} + \mathbf{q} \qquad (6)$$

where $\mathbf{i}$ is related to the *chip synchronization* and is given by

$$\mathbf{i} = (\mathbf{x} - \mathbf{x_d})/2 \qquad (7)$$

and $\mathbf{q}$ is related to the *symbol synchronization* and is given by

$$\mathbf{q} = (\mathbf{x} + \mathbf{x_d})/2 \qquad (8)$$

with $\mathbf{x_d} = [x_{-1}, x_0, x_1, \ldots, x_{N-2}]^T$. It follows that $\mathbf{i}$ has its nonzero values whenever there are two different consecutive values in $\mathbf{x}$, and $\mathbf{q}$ has its nonzero values whenever there are two identical consecutive values in $\mathbf{x}$. A suitable synchronization preamble should have a significant number of nonzero entries in both terms in order to provide similar amounts of information for chip and symbol synchronization, i.e., $||\mathbf{i}||$ and $||\mathbf{q}||$ should be similar. Note that, formally, the first element of $\mathbf{x_d}$, x_{-1}, does not belong to the preamble and would be a random value if the preamble is preceded by noise. In practice however, the transmitters perform some kind of power ramping and this value is not random. For notational convenience, in what follows we will assume that $x_{-1} = x_{N-1}$.

A. Carrier Synchronization

When targeting a simple synchronizer suited for SR receivers, the carrier synchronization problem does not need to be addressed for many standards. We may take reasonable assumption that the transmitter derives data and carrier clocks from the same crystal. A frequency mismatch ϵ gives a phase error

$$\varphi_\epsilon = 2\pi f_c T_x \epsilon. \qquad (9)$$

Hence, an IEEE 802.15.4 receiver operating at 2.45 GHz at a chip rate of 2 Mchip/s will see phase errors of $0.441° \epsilon$(ppm). With the current availability of low cost crystals with frequency stabilities of 10 ppm, in the worst case, i.e., $\epsilon = 20$ ppm, phase errors of 8.82 ° are obtained, which have a limited effect on receiver performance. The effects of frequency stability are further discussed in Section IV.

B. Symbol and Chip Synchronization

Conceptually, the symbol synchronization process will consist in the following. After each received phase sample (φ_n), the vector $\boldsymbol{\varphi}_n = [\varphi_{n-(N-1)}, \ldots, \varphi_{n-1}, \varphi_n]^T$ is built. Then, the scalar product

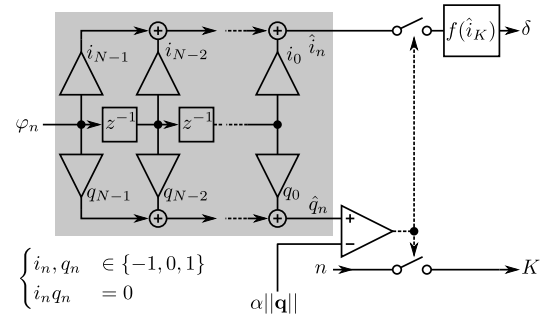$$\hat{q}_n = \frac{2}{\pi} \boldsymbol{\varphi}_n \cdot \mathbf{q}, \qquad (10)$$

Fig. 2. Block diagram to compute $\hat{i}_n$ and $\hat{q}_n$ (see text). The shaded part is the FIR filter part. The block labeled $f(\hat{i}_K)$ implements (15).

which measures the similarity with $\mathbf{q}$, is computed (lower signal path in Fig. 2). This is done for each new sample until a maximum is detected. If $\hat{q}_n$ exhibits a sharp peak with low sidepeaks this maximum is easily located.

Formally, in the absence of noise, we are looking for the displacement K that solves the equation

$$\hat{q}_K = ||\mathbf{q}|| \qquad (11)$$

where $|| \cdot ||$ denotes the euclidean norm.

Once the displacement K is found, the information on δ found by averaging the positions n where $x_n \neq x_{n-1}$, which, from (4), exhibit the property

$$x_n \varphi_n(\delta) = \pi/2 - \delta\pi/T_x. \qquad (12)$$

Making use of the vector $\mathbf{i}$ defined in (7), this is achieved through the scalar product

$$\hat{i}_n = \frac{2}{\pi} \boldsymbol{\varphi}_n \cdot \mathbf{i} \qquad (13)$$

which, in the absence of noise, will give

$$\hat{i}_K = ||\mathbf{i}|| \left(1 - \frac{2\delta}{T_x} \right), \qquad (14)$$

from which δ is directly obtained as

$$\delta = \frac{T_x}{2} \left(1 - \frac{\hat{i}_K}{||\mathbf{i}||} \right). \qquad (15)$$

The upper part of Fig. 2 illustrates this procedure.

C. Possible Ambiguities

Fig. 3 shows the qualitative behavior of $\hat{q}_n$ near the maximum for a range of current δ values. From this figure, it follows that, if the current value of δ is already zero, there is an ambiguity in the maximum. In the leftmost subfigure, (15) gives the new estimation as $\delta = T_x$. In the rightmost subfigure, (15) gives the new estimation as $\delta = 0$. Both results have the same meaning. Hence, in both cases, we get the same point.

In practice, (11) cannot be fulfilled exactly. Instead, we find the index K such that

$$\hat{q}_K > \alpha ||\mathbf{q}|| \qquad (16)$$

with $0 < \alpha < 1$ a threshold. A block diagram describing this procedure is shown in the lower signal path depicted in Fig. 2.
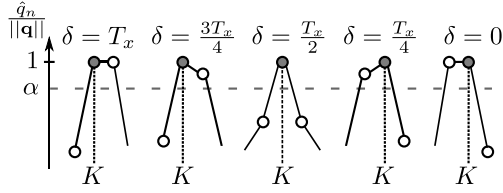
Fig. 3. Qualitative behavior of $\hat{q}_n/||\mathbf{q}||$ as a function of the current value of δ. The shaded circle indicates the chosen maximum.

Fig. 4. Format of the Physical Protocol Data Unit (PPDU) as mandated by [14].

As $\alpha < 1$, there is the possibility that the threshold is crossed by two consecutive samples. In the presence of noise, the sample giving the maximum value of $\hat{q}_n$ may be the wrong one. In Section IV-C we come back to this with simulations for a specific implementation.

The whole approach described up to here is valid for a wide range of standards. Implementation details and the effects of noise are strongly dependent on each particular case. In the following section we focus on the 802.15.4 case.

IV. IMPLEMENTATION EXAMPLE: IEEE 802.15.4

In what follows, we focus on the particular case of the IEEE 802.15.4 standard [14], where the features of SR reception may become attractive. This standard specifies an MSK (or, equivalently, O-QPSK) modulation in some of the bands. In the 2.45 GHz band, the standard specifies a PPDU format as shown in Fig. 4, and each 4-bit data symbol is mapped into a 32-chip PN sequence.

In particular, the synchronization header SHR is a five-octet field composed by two subfields. The first one (preamble) consists in the $\times 8$ repetition of the zero symbol

$$\mathbf{s_0} = [1, 1, -1, 1, 1, -1, -1, 1, 1, 1, -1, -1, -1, -1, 1, 1,$$
$$-1, 1, -1, 1, -1, -1, 1, -1, -1, -1, 1, -1, 1, 1, 1, -1], \tag{17}$$

giving a total preamble length of $N = 256$ chips. The preamble is followed by the octet corresponding to the SFD field, which has a value of `0x7A`.

Chip and symbol synchronization should be complete before the arrival of the SFD field, hence the available time is $256T_x$.

From (7) and (8), we get the following $\mathbf{q}$ and $\mathbf{i}$ vectors

$$\mathbf{q} = [0, 1, 0, 0, 1, 0, -1, 0, 1, 1, 0, -1, -1, -1, 0, 1, 0,$$
$$0, 0, 0, 0, -1, 0, 0, -1, -1, 0, 0, 0, 1, 1, 0] \times N_S \quad (18)$$
$$\mathbf{i} = [1, 0, -1, 1, 0, -1, 0, 1, 0, 0, -1, 0, 0, 0, 1, 0, -1, 1,$$
$$-1, 1, -1, 0, 1, -1, 0, 0, 1, -1, 1, 0, 0, -1] \times N_S, \quad (19)$$
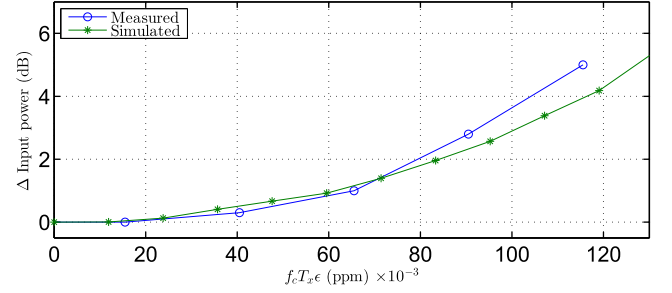

Fig. 5. Frequency deviation effect on synchronization. Increase in input power to keep PER $= 10^{-2}$ vs. ϵ with $\alpha = 0.65$. Simulation and experimental results.
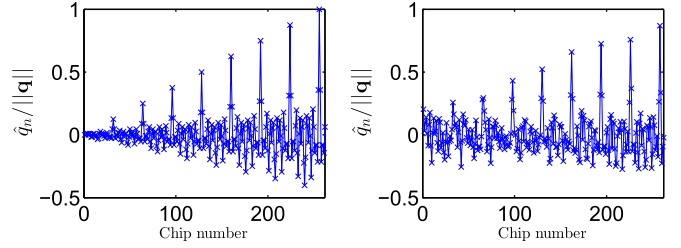

Fig. 6. $\hat{q}_n/||\mathbf{q}||$ in the absence of noise (left) and a single realization of $\hat{q}_n$ with SNR $= 3.3$ dB (right). $\delta = 0.5$ in both cases.

with the notation $\times N_S$ indicating N_S vector repetitions. From these we obtain $||\mathbf{i}|| = \frac{3}{4}N_S$ and $||\mathbf{q}|| = \frac{\sqrt{7}}{4}N_S$, with N_S the number of symbols chosen to be used for synchronization ($N_S \leq 8$). Note that the norms $||\mathbf{i}||$ and $||\mathbf{q}||$ are similar, which makes the IEEE 802.15.4 preamble suitable for the proposed synchronization scheme.

A. Carrier

For the sake of implementation simplicity, we have chosen to ignore the carrier synchronization problem. To validate this simplification, we have considered that data and carrier clocks are derived from the same crystal and have simulated (Fig. 5) the increase in input signal power required to keep a Packet Error Rate PER $= 10^{-2}$ as a function of the relative mismatch $f_c T_x \cdot \epsilon$ introduced in (9). Under IEEE 802.15.4 conditions, the loss in sensitivity with 10 ppm crystals in the worst case, i.e., $\epsilon(ppm) = 20$, is less than 0.2 dB and with 20 ppm crystals is less than 0.7 dB which may be acceptable in most applications.

B. Computation of K

With the preamble defined by the IEEE 802.15.4 standard [14], $\hat{q}_n$ exhibits eight very sharp peaks, corresponding to the repetition of each zero symbol (Fig. 6).

A static choice of the threshold α (16) required for symbol synchronization is not trivial. A high value $\alpha \simeq 1$ will work correctly for high SNR but will miss many packets as SNR decreases while, with a low value of α, the probability of false synchronizations increases.

To make a reasonable choice of the threshold value, we may investigate what happens in the case of a noise level that produces a given link quality. Specifically, the IEEE 802.15.4
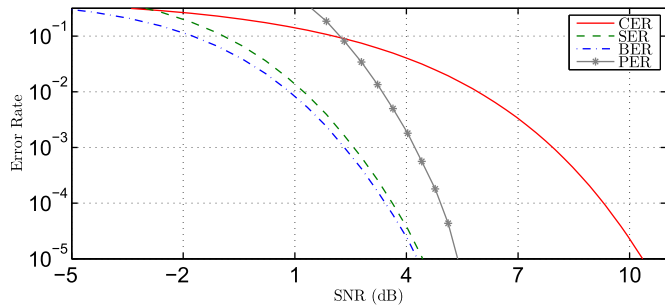
Fig. 7.   Simulated chip error rate, symbol error rate, bit error rate, and packet error rate as a function of SNR.
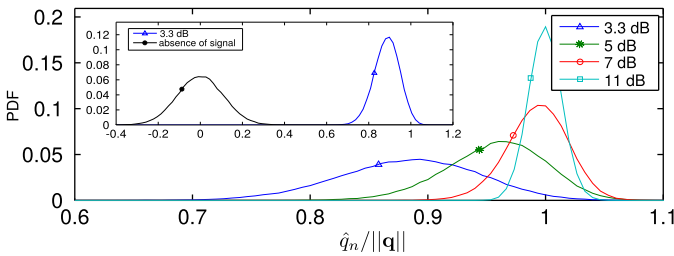

Fig. 8.   Probability density function of $\hat{q}_n/||\mathbf{q}||$ for different values of SNR. The inset depicts the PDF in absence of signal and with SNR = 3.3 dB.

Fig. 9.   Median and IQR value of $\hat{q}_n/||\mathbf{q}||$ vs. SNR.

Fig. 10.   Contour plot showing the probability distribution of estimated δ/T_x vs. true δ/T_x with SNR = 3.3 dB. Data are processed at the end of the 8th symbol (without threshold). Contour levels are at [1, 3, 5, 7].

standard specifies a minimum sensitivity to achieve PER = 10^{-2} with a PSDU length of 20 octets.

To simulate the effects of noise, we have considered Gaussian noise added to the in-phase and quadrature components of the input signal. Fig. 7 shows some simulation results as a function of SNR considering perfect synchronization. This figure shows curves for the raw chip error rate (CER), the symbol error rate (SER), the BER and the PER. From this graph, we conclude that the worst case scenario, corresponding to the sensitivity threshold given by PER = 10^{-2} is given by SNR = 3.3 dB.

We investigate the filter output $\hat{q}_n$ after the full preamble of $N_s = 8$ zero symbols. When the noise power is sufficiently low, we may expect a Gaussian distribution around the normalized maximum value of unity. An increase in noise level increases the output variance proportionally. However, as the noise level increases further the nonlinearity associated to the phase rollover outside the $-\pi \cdots \pi$ interval (which the detector is unable to account for) comes into play: phase values of $\pm(\pi + \varepsilon)$ are treated as $\pm(-\pi + \varepsilon)$. This effect is confirmed by the simulation results shown in the main plot in Fig. 8. This figure shows that, when the noise level increases, the variance of $\hat{q}_n$ increases as expected but, at the same time, the mean value decreases due to the effect of the nonlinearity.

The dependence of the median value and Interquartile Range (IQR) of $\hat{q}_n/||\mathbf{q}||$ with SNR is depicted in Fig 9. From the traces in Figs. 8 and 9 we see that the nonlinearity effect discussed before becomes relevant for SNR < 4 dB.

To set a reasonable worst-case threshold value for α we have simulated the PDF of $\hat{q}_n/||\mathbf{q}||$ in the presence of the highest noise level, i.e., SNR = 3.3 dB. The inset plot in Fig. 8 depicts the PDF of $\hat{q}_n$ with preamble plus noise and
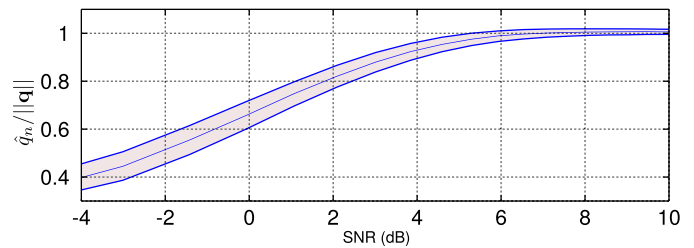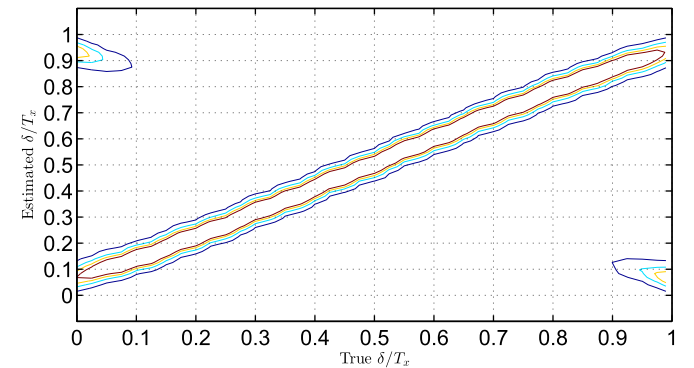
without signal (noise only). It follows that α may be assigned a wide range of values. When $\alpha < 0.35$ we start having a significant number of false synchronizations in the absence of preambles and with $\alpha > 0.65$ we start missing preambles. Instead of developing an adaptive threshold control scheme as, for instance, in [22], which would require additional receiver resources, we have chosen a fixed value of $\alpha = 0.65$, which allows synchronization for signal levels down to the sensitivity level.

For low noise (or high signal) levels, even the highest value $\alpha = 0.65$ will make the comparator fire before the full preamble has been processed. However, even in the presence of noise, $\hat{q}_n$ has very narrow peaks separated by one symbol (32 chips) (Fig. 6). Hence, the comparator may fire an integer multiple m of $\mathbf{s_0}$ symbols earlier, producing $K - 32m$ instead of K. This poses no problem, as the frame synchronization algorithm will search for the SFD, skipping eventual $\mathbf{s_0}$ symbols arising from an early synchronization.

C. Computation of δ

Once the comparator has fired, (15) is used to estimate the value of δ. The effects of noise have been simulated. First of all, we may consider Fig. 10, relating the true and the estimated values of δ/T_x, considering that the comparator fires at the end of the last symbol, i.e., without threshold. This figure has been computed for the case SNR = 3.3 dB and shows that the relation is not linear but becomes compressed. This is a consequence of the fact that high levels of noise reduce the range of $\hat{i}_n$ due to nonlinearities in a similar way as has been shown for $\hat{q}_n$. The reduction is dependent on the real
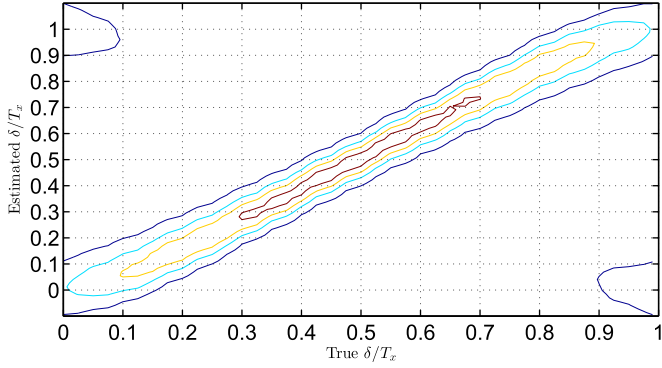
Fig. 11. Contour plot showing the probability distribution of estimated δ/T_x vs. true δ/T_x with SNR = 3.3 dB, firing when the threshold $\alpha = 0.65$ has been crossed and with the correction (21). Contour levels are at [1, 3, 5, 7].

value of δ. For $\delta = T_x/2$ the mean of $\hat{i}_n$ is zero, regardless of the noise level, and for $\delta = 0$ and $\delta \longrightarrow T_x$ maximum compression happens.

Also, in practice, we compute δ not at the end of the last symbol but whenever the threshold is crossed, which will often happen m symbols earlier than the last symbol. For $\delta = 0$ and $\delta \longrightarrow T_x$ this means that

$$\hat{i}_K < ||\mathbf{i}|| \tag{20}$$

and the range given by (15) will be limited, never reaching the extremes $\{0, T_x\}$ even in the absence of noise.

In an attempt to correct these effects, the estimated value of δ can be obtained from

$$\delta = \frac{T_x}{2}\left(1 - \frac{\hat{i}_K}{\alpha||\mathbf{i}||}\right). \tag{21}$$

The idea behind (21) is to reduce the norm of $\mathbf{i}$ by the same amount as the implicit reduction of $\mathbf{q}$ given by (16). This helps to restore the $[0..T_x]$ range of δ.

Fig. 11 shows the effect of the correction given by (21) on a numerical simulation taking the full synchronization process into account. This figure shows that the variance of the estimation of δ/T_x increases as a consequence of the amplification required to restore its dynamic range. Among the effects that are included in Figs. 10 and 11 there is the possibility of the ambiguities in the location of the maximum, as explained in Section III-C. As the noise level increases, for values of δ near zero or T_x there is a probability that the secondary peak, $K - 1$, rises above the main one, K, (Fig. 3). If the secondary peak is wrongly detected, the estimation of δ given by (15) is made with

$$\hat{i}_{K-1} = ||\mathbf{i}||\left(\frac{\delta}{T_x} - 1\right) \tag{22}$$

instead of $\hat{i}_K$. The wrong estimation of δ brings us from $-T_x - \delta$ to $-3\delta/2$ instead of to 0. As was mentioned before, when $\delta = 0$ the detection of a secondary peak gives no error. When $\delta \approx T_x/2$ there is only one maximum. The most critical point is around $\delta \approx T_x/3$ because (15) brings us to $-T_x/2$ where we easily get the previous chip instead of the current one (Fig. 1) while the probability to detect a wrong peak is still high.
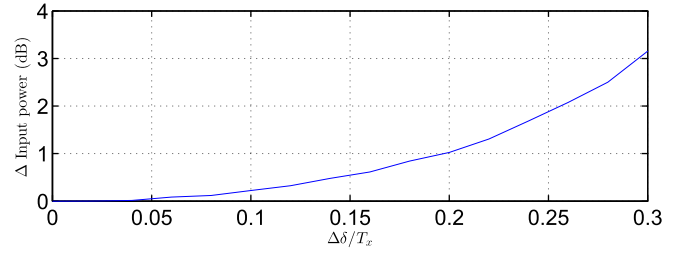

Fig. 12. Increase in input signal power required to keep PER = 10^{-2} vs. the mismatch $\Delta\delta/T_x$.
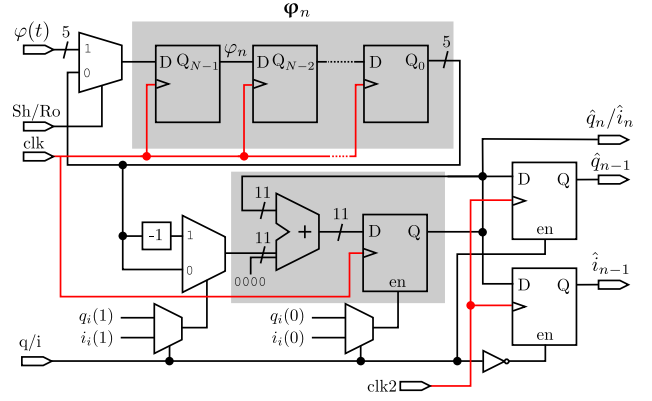

Fig. 13. Filter implementation.

Furthermore, we have investigated the effects of a mismatch in δ on receiver performance. The simulated PER has been computed for different values of $\Delta\delta/T_x$ and the signal power has been increased to achieve PER = 10^{-2}. Fig. 12 shows the increase in signal power needed to keep the link quality constant as a function of the mismatch $\Delta\delta/T_x$. It follows that even errors as high $\Delta\delta/T_x = 0.1$ have a limited effect on the overall performance.

D. SFD Detection

Once chip and symbol synchronization has been achieved, frame synchronization consists in locating the SFD `7A`. This takes place at the bit level. As the threshold is crossed at an unknown instant before the full preamble has been processed, we may have to wait up to m symbols to find the SFD. If the SFD is not detected within this time, the state machine controlling synchronization restarts the synchronization process.

V. FPGA IMPLEMENTATION

The whole technique has been described in VHDL and implemented on an FPGA. An MSK front-end, as described in [8] provides a stream of phase samples φ_n every T_x representing the interval $[-\pi, \pi)$, with the 20 integer values $[-10, 9]$ coded as `signed(4 downto 0)` signals. These phase samples are stored in a shift register to build the vector $\boldsymbol{\varphi_n}$ (upper shaded block in Fig. 13).

A. Filter

The digital implementation of the filters described in Fig. 2 is extremely simple, taking into account that the coefficients

TABLE I

THRESHOLD CROSSING DETECTOR

```
process(clk) begin
  if q_hat_prev > threshold then
    if q_hat> q_hat_prev then k<=n; else k<=n_prev;
end process;
```

TABLE II

QUENCH-PHASE GENERATING COUNTER

```
process(clk) begin
  if rising_edge(clk) then
      if rst='1' then cnt <= 0;
      else cnt <= cnt+1;
      end if;
  end if;
end process;
rst <= '1' when cnt = max_count or
  ((cnt=delta) and dosynch='1') else '0';
```


Fig. 14. Schematic of the data detection circuit.

are either 0 or ± 1. Both filter outputs are computed sequentially by the same circuit. An accumulator with an enable signal (for the 0 coefficients), adds the current phase sample or its inverted version (center shaded block in Fig. 13). To simplify the representation in Fig. 13, the same clock is fed to all the registers that store $\boldsymbol{\varphi}_n$. In the real implementation, there are additional enable signals. These allow, for instance, loading the phase samples every T_x and rotate them much faster to compute the filter outputs between each T_x.

In our implementation we have used only $N_S = 7$ symbols for synchronization. The last symbol of the preamble is used to adjust the receiver so that the SFD is detected with the correct synchronization. Vector $\boldsymbol{\varphi}_n$ has a length of 224 and to compute $\hat{q}_n$ and $\hat{i}_n$ we need 224×2 clock cycles.

In Fig. 2, the signals q_i and i_i are the filter coefficients of **q** and **i**, which are stored and rotated in 32-element shift registers. They appear as q_i (signed(1 downto 0)) and i_i (signed(1 downto 0)) in Fig. 13.

The previous values of $\hat{q}_n$ and $\hat{i}_n$ are also stored every T_x to be able to implement the following step.

B. Thresholds and δ Estimation

The threshold crossing detector is implemented with a digital comparator, as described in the code in Table I.

The value of δ is a function of the resulting $\hat{i}_K$ (signed(10 downto 0)), as shown in Fig. 2. Equation (21) has been implemented with a lookup table taking the 5 most significant bits of $\hat{i}_K$.

Regarding the estimation of δ it should be noted that the receiver is able to generate a finite number of different δ values, corresponding to different quench phases. This is equivalent to saying that the δ values are quantized. The end of the synchronization process should trigger the actual estimation of δ. This is indicated with rst from which the quench phase is derived as shown in Table II.

C. Data Receiver

Once synchronization is achieved, the phase φ_n corresponding to the n-th chip is quantized with one bit (hard decision) and stored in a 32 bit shift register. Then, these 32 chips are comp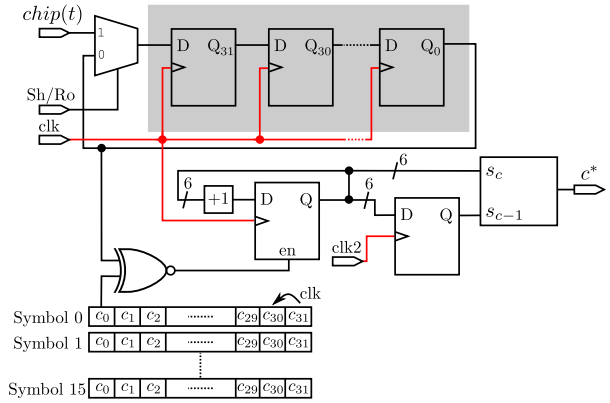ared with the 16 possible 32-chip sequences corresponding to the 16 symbols specified by the IEEE 802.15.4 standard. At the end of each symbol, the number of coincidences s_c is compared with the previous number of coincidences s_{c-1} and the index of the best symbol c^* is stored. This may be done serially with a counter with an enable signal. After cycling through all 16 possibilities, the stored index gives the most likely symbol and its corresponding 4 bits. This is described schematically in Fig. 14 where clk2 is clk divided by 32.

D. Resources as a Function of Data Rates

Operating at 10 kchip/s the FIR filter may operate serially at low clock speeds. As has been shown, to perform correlation 224×2 clock cycles (plus a few more for additional storage and processing) are required per chip. This translates into a clock frequency slightly over 4.48 MHz. The data detection block can also operate serially. As each symbol required 32×16 clocks, it follows that the clock frequency could be as low as 160 kHz.

Operating at 2 Mchip/s, the correlator should operate with 32 values of φ simultaneously. So, N_s clocks are required for each chip. Taking $N_s = 7$ this means that the clock frequency should be 28 MHz. As usual, clock frequency can be traded for area/circuit complexity: a full serial implementation would require a 896 MHz clock. The parallelization increases the accumulator width but does not increase significantly the number of registers, as the 224×5 bits of phase history are required in any case. The data detection block can operate serially with reasonable clocks: 32×16 clocks means 32 MHz clock frequency.

VI. EXPERIMENTAL TEST SETUP AND RESULTS

The experimental test setup is depicted in Fig. 15. It consists in a data generator module, a transmitter part, an RF signal generator, the SR receiver and a data analyzer module.

The data generator module consists in a Raspberry Pi [23] single-board computer (TxPi). The TxPi runs an application that talks at a high level to a transmitter FPGA (TxFPGA) through an SPI link. The TxFPGA embeds the 802.15.4 MAC layer [24] and the symbol to chip conversion. The TxFPGA generates the chip and clock signals to be MSK modulated with an Agilent E4431B RF generator.
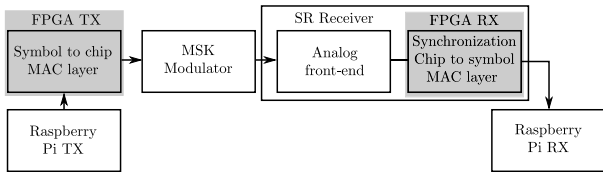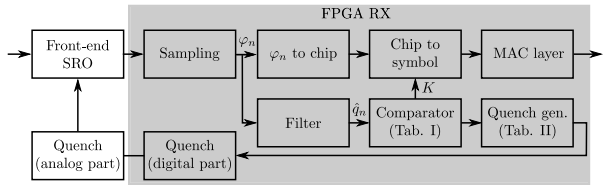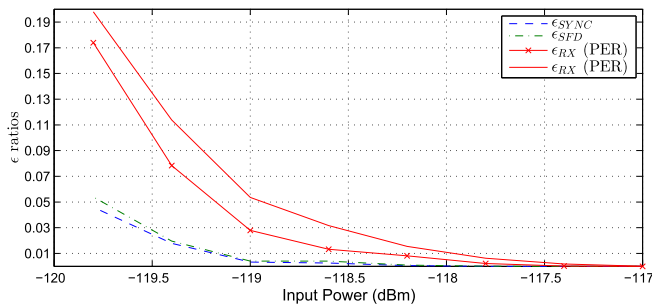
Fig. 15.   Experimental test setup.

Fig. 16.   Detail of the SR Receiver and FPGA RX blocks.

Fig. 17. ϵ_{SYNC}, ϵ_{SFD} and ϵ_{RX} (PER) versus input signal power with a threshold level $\alpha = 0.65$. The lower and upper ϵ_{RX} traces are obtained, respectively, with and without the correction given by (21).

The generator output is fed to the input of an SR receiver consisting in an analog front-end with an 1-bit ADC as described in [8], and the digital parts, described in this paper and in [8], have been implemented on an FPGA board (RxFPGA). The quench signal is generated on the same RxFPGA as described in [25]. The RxFPGA also includes the chip-to-symbol mapping circuitry and embeds an VHDL implementation of the 802.15.4 MAC layer [24].

Both TxFPGA and RxFPGA have full transceiver capabilities. They are Terasic DE0-Nano boards [26] containing a Cyclone IV EP4CE22 FPGA, belonging to the lowest-cost Altera product range. With no special efforts put into optimizing the FPGA usage and including several features just for testing, our implementation takes up 22% of the FPGA resources: 9% devoted to the MAC layer implementation and 13% to the transceiver.

With this test setup, we have done the following measurements. Fig. 17 depicts the experimental results corresponding to 10^4 transmitted packets with random waiting times between packets and a threshold $\alpha = 0.65$ operating at $f_x = 10$ kchip/s. Initially, no correction of $\hat{i}_K$ has been done, i.e., (15) has been used instead of (21). Specifically, this figure depicts the ratios $\epsilon_{SYNC} = (N_{TX} - N_{SYNC})/N_{TX}$, $\epsilon_{SFD} = (N_{TX} - N_{SFD})/N_{TX}$ and $\epsilon_{RX} = (N_{TX} - N_{RX})/N_{TX}$, with N_{TX}, the number of transmitted packets, N_{SYNC}, the number of times the threshold has been crossed (and synchronization detected), N_{SFD}, the number of SFD
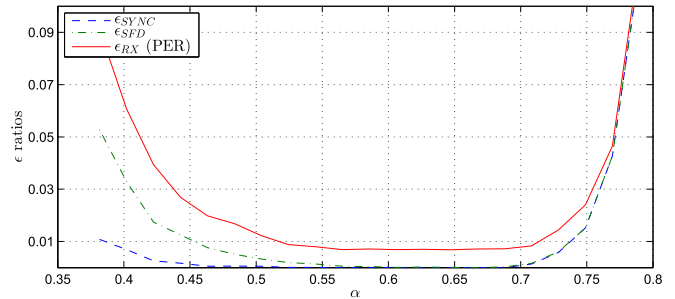
Fig. 18. ϵ_{SYNC}, ϵ_{SFD}. and ϵ_{RX} (PER) versus threshold level α.

delimiters detected, and N_{RX}, the number of correctly received packets. Note that $\epsilon_{RX} = $ PER. This figure shows that the synchronization preamble error rate ϵ_{SYNC} is less than 10^{-2} for an input power of -119.2 dBm. Here it may also be seen that PER $= 10^{-2}$ is achieved with an input power level of -118.2 dBm. This figure is 10 dB better than the bit-rate-adjusted sensitivity mandated by the IEEE 802.15.4 standard ($-85 - 10\log(2$ Mchip/s/10 kchip/s$) = -108$ dBm). The effect of taking a correction given by (21) is also shown on the same figure. It follows that this enhances the sensitivity by only 0.3 dB. The effects of crystal frequency mismatch have been measured and were shown in Fig. 5. For this measurement, an FPGA board with external clock input was used. It follows that the carrier synchronization problem can be neglected for commonly available crystals, simplifying the receiver design.

The effects of setting a different threshold level α on the resulting PER has also been investigated experimentally in Fig. 18. The figure shows that there is a wide range of quasi-optimum threshold values between $\alpha = 0.54$ and $\alpha = 0.7$. If the threshold is set higher we start missing packets. If the threshold is set lower, synchronization is achieved too early, which is equivalent to having a shorter correlating filter. This means that the output is noisier and the estimation of δ is worse. Also, as was shown in Fig. 8, a lower threshold means that false synchronization may arise from noise only.

VII. Conclusions

In this paper we have presented a technique to enable the reception of burst-mode MSK communications basing on an SR receiver core. We have presented a simple synchronization technique that is able to operate under the conditions imposed by IEEE 802.15.4 standard [14]. The principle is extensible to other simpler protocols based on MSK signaling with suitable **i** and **q** PN sequences. Basing on the MSK receiver core described in [8], we describe a simple, all-digital synchronizer which performs joint symbol and chip synchronization. This is followed by a frame synchronizer.

First, we have investigated the performance of the synchronizer in the ideal case. Then, emphasis has been put on an implementation suitable to detect the preamble defined by [14] and the performance of this implementation as a function of different noise levels has been investigated. The effects of the nonlinearity of the equivalent phase quantifier have also been investigated. Furthermore, the main points of the

FPGA implementation of the proposed technique have been described. In contrast to alternative architectures, the resulting SR MSK receiver requires no complex and expensive blocks such as multi-bit ADC converters and digital multipliers. The analog part is as simple as a preamplifier and an oscillator. The digital part is extremely simple with the most complex digital block being an accumulator. With the addition of the corresponding chip-to-symbol mapping and a suitable MAC layer protocol, a whole receiver has been implemented. Experimental results validate the practical feasibility of the described approach and yield an overall receiver sensitivity 10 dB better than is required by [14].

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