Heterogeneous Memristive Crossbar for In-Memory Computing

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MEMRISYS2015 Extended Abstract

The memristor represents one of today's latest technological achievements in circuits and systems, demonstrating advantageous characteristics which open new pathways for the exploration of advanced computing paradigms and beyond-Von Neumann architectures [1], [2], [3]. Most importantly, it provides with an unconventional computation framework which combines information processing and storage in the memory itself; i.e. the major distinction from the present day's computing technology [4]. Moreover, memristor-based crossbar nanoarchitectures are highly considered as candidate structures for future memory and logic applications, where the same physical devices are used either as storage elements or logic gates [5], [6], [7], [8], [9].

In this work we propose the design of a novel crossbar geometry, which is heterogeneous in terms of its cross-point devices, allowing for the realization of true in-memory digital logic computations. More specifically, it is a combination of two stacked crossbar arrays with a shared intermediate nanowire layer. The variety of available cross-points types allows the execution of parallel memristive logic computations, where the logic state variable is voltage [10]. Moreover, the utilization of insulating patterns in the crossbar arrays, at the expense of a small area-overhead, permits the simultaneous parallel read/write memory operation of two memory words [8]. Memory/logic operation is determined through control signals driven from the peripheral CMOS-based driving circuitry, which also comprises row/column decoders, tri-state drivers, and summing/sense amplifiers to allow for the proper programming/reading of the memristive cross-points. A simulation-based validation of read/write memory operations as well as of parallel memristive logic computations (half adder, sum of products, etc.) is performed using the PSPICE simulation environment and a device model of a threshold-type, voltage-controlled, bipolar memristor. The outcome of this work includes combined dense storage/computing nanoarchitectures, based on memristors, to be used in future electronic computing systems.

Tentative List of References

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