MASTER THESIS

Design and linearization of an efficient class-E power amplifier using a test bench based on development boards

Julieta Flomenbaum

SUPERVISED BY

Dr. Pere Lluis Gilabert Pinal
Dr. Gabriel Montoro López

Universitat Politècnica de Catalunya
Master in Aerospace Science & Technology
February 2017

This Page Intentionally Left Blank

Design and linearization of an efficient class-E power amplifier using a test bench based on development boards

BY

Julieta Flomenbaum

DIPLOMA THESIS FOR DEGREE

Master in Aerospace Science and Technology

AT

Universitat Politècnica de Catalunya

SUPERVISED BY:

Dr. Pere Lluis Gilabert Pinal
Dr. Gabriel Montoro López
Department of Signal Theory and Communications

This Page Intentionally Left Blank

ABSTRACT

Nowadays, with the increase in small satellites applications for Earth observation, the need for high efficient transmitters capable of delivering the required power, taking into account not only the power consumption limitations of small satellites (solar powered), but also the required linearity to allow high data rates in the downlink, has fostered the research on alternatives to the classical transmitter amplification.

This Master Thesis has the objective to mitigate the inherent trade-off between linearity and efficiency in communication transmitters by addressing the design of an efficient Power Amplifier (PA) combined with the implementation of Crest Factor Reduction (CFR) and Digital Predistortion (DPD) techniques. For this purpose, the deployment of a low-budget test bench based on development boards is proposed to carry out the PA evaluation and linearization avoiding the use of expensive laboratory equipment for signal generation and analysis.

The experimental campaign was carried out using CFR technique to limit the Peak to Average Power Ratio (PAPR) in addition to the DPD linearization, this method not only allowed us to reduce spectral regrowth and minimize in-band distortion, but also was a crucial approach to maximize power amplifier efficiency fulfilling the linearity requirement imposed by the communications standards.

The evaluation of the class-E PA designed (under the supervision of the *Communication Engineering* research group of the *University of Cantabria)* was performed using a LTE-like signal of 20 MHz employing Quadrature Amplitude Modulation (QAM) and Orthogonal Frequency-Division Multiplexing (OFDM). The measurements shown that it is possible to achieve an output power of 36,6 dBm with an efficiency about 50% in contrast to the typical class-AB PA efficiency figures ranging from 5-10% when operated with significant back-off levels to avoid saturation. Moreover, the Adjacent Channel Power Ratio (ACPR) is below -45 dB and the Error Vector Magnitude (EVM) is around 1,4% for a 64QAM signal in compliance with the communication standards.

This Page Intentionally Left Blank

ACKNOWDLEGMENT

In the first place, I want to thank my advisors Pere Gilabert and Gabriel Montoro for their valuable teachings and all the support given to me across this project. I would also like to appreciate the advices of David López Bueno (CTTC) and the collaboration of Jose Miguel in the laboratory.

Besides, I want to thank Jose Angel García García for his invitation to the University of Cantabria and the dedication shown during the supervision of the design of a class-E power amplifier. To Nieves and David for all their assistance and collaboration.

I want to thank my flatmates, Victoria, Belén and Gastón, for building together a place in Barcelona that we could call home throughout these months.

I want also to mention my friends, who find a way to be present every day despite being so far. To Belen, Ena, Soledad and Emilia for being always there among so many years.

I specially want to thank Julian for sharing this experience with me, giving me his unconditional support and understanding.

Finally, I want to thank my mother for her unconditional love and for supporting me in all the decisions I made. To my grandmother and Norma, for accompanying me at every step I give. To Marcelo and Zulema for being always ready to offer their help from wherever they are.

To finish with, I cannot conclude this acknowledgement without mention the BEC.AR program belonging to the Ministry of Modernization of Argentina which gave me the opportunity to attend this master.

This Page Intentionally Left Blank

CONTENTS

LIST OF FIGURES

LIST OF TABLES

Chapter 1

INTRODUCTION

Over the past half century, the improvements in spacecraft technology have been primarily in the areas of microelectronics for on-board processing, high frequency electronic devices, and integrated circuits for communications and navigation, solar cells and batteries for on-board power generation and storage among many others.

Hence, the term small satellite indicates the progression in technological innovations that has taken place, which has enabled satellite manufacturers to package a wide range of functionality into a small volume at an affordable cost and shorter development time.

Nowadays, most of the small satellite applications are found in low orbits, developed mainly for the purpose of Earth observation applications, communications and scientific research, creating new markets for high performance and high resolution remote sensing instruments to be deployed on smaller and lower-cost platforms.

Despite the fact that energy-storage technologies have advanced dramatically over the past years, it is found a big limitation regarding the power consumption requirement. While conventional large satellites are provided with several hundred Mbps downlink's systems which involves a huge power consumption of one or more hundreds of watts, a typical small satellite of 50 Kg can only generate around 100 W to cover the demand of the entire system [SIT+12].

The power required to operate for communication subsystems and its relation with the total power generated is detailed in *Table 1.1* considering a classification based in the overall mass [SG15] [Hal15].

Table 1.1: Small satellites power budget

Satellite Classification	Total [W]	Communications Subsystem[W]
Microsat (10 - 100 Kg)	100	20
Nanosat (1 - 10 Kg)	20	7
Picosat (0,1 - 1 Kg)	5	1,5

It can be noted that the communication subsystem consumption represents a higher proportion of the total available power while the mass decreases, for this reason the technology selected and its implementation have an important role for the mission capabilities.

Taking into account legal issues and local availability, the frequency band chosen depends mainly on the application, differentiating between telemetry and data downlink. Therefore, it must be also considered the limitation regarding the short visibily time that is reflected in the requirements of a higher data rate.

In *Figure 1.1*, it could be observed the current distribution of satellite's downlink communications band in use for operations of nano satellites. The figures are presented in number of communication modules since many satellites employed more than one bandwidth [Kul17].
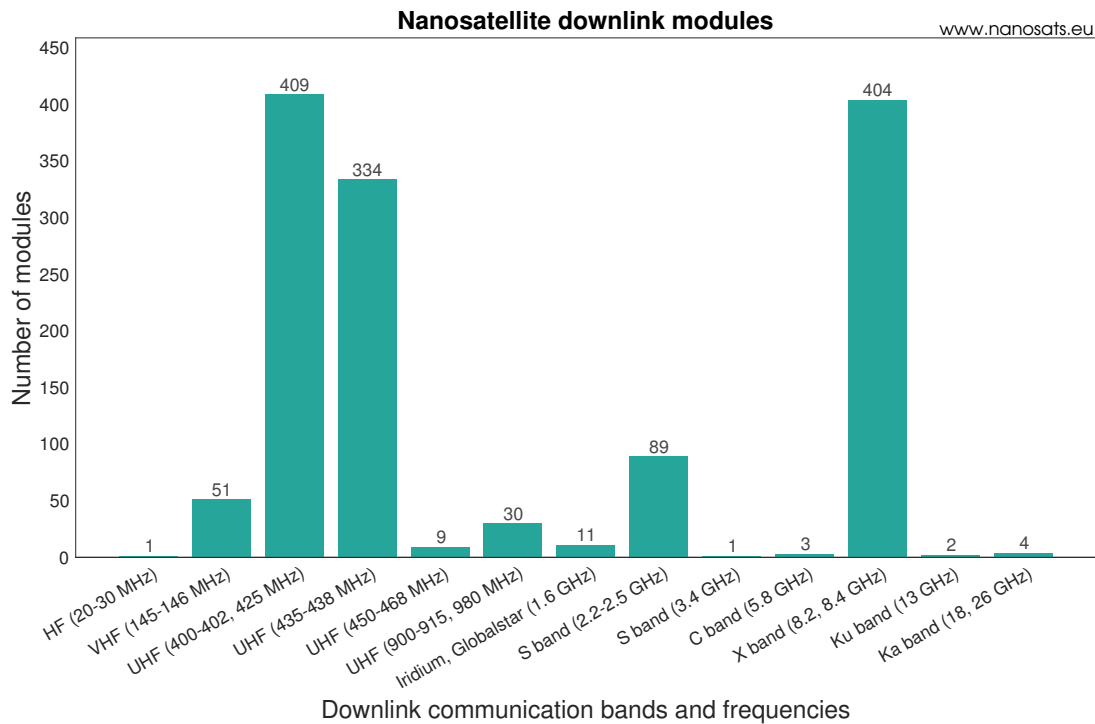
Figure 1.1: Downlink communication bands and frequencies

1.1. State of the Art of commercial S-Band transmitters for small satellites application

With the aim of becoming acquainted with the state of the art related with the devices employed for data downlink in the S-Band frequency, *Table 1.2* shows an overview of some comercial devices.

After analyzing the datasheets provided by the transmitter manufacturers, we noticed that we can find output power values ranging from 0,5 W to 8 W, presenting a wide variation in terms of efficiency from 4% up to 40%.

Table 1.2: Commercial S-Band transmitters

	Frequency [MHz]	Output Power [W]	Consumption [W]	Estimated Efficiency[%]
SLink IQ Wireless [Wir13]	2200-2290	0,5	12	~ 4
μSTDN-100 Space Micro [Mic16]	2200-2300	8	42	$\sim$20
SWIFT-SLX Tethers Unlimitedt [Unl16]	1500-3000	3	8,4	~ 35
Transmitter S-Band EnduroSat [End16]	2400-2480	2	5	~ 40

Among the devices analyzed, the most competitive option in terms of efficiency is the design of *EnduroSat* for 2400 to 2480 MHz, an output power of 2 W and an efficiency around 40%. Then, we will consider these values of frequency and output power as the starting requirements for the design of a high efficient amplifier looking to achieve an efficiency above 40%.

1.2. Motivation and objetives

Considering the power limitations discussed for small satellites applications, we can state that the demand of a high data rate downlink capability combined with an acceptable system efficiency makes the communication subsystem critical from the power and spectral efficiency point of view.

Among the many devices that are found in a communication subsystem, the Power Amplifier (PA) is not only one of the most power consuming components that can be found in a RF system, but it is also the responsible for the main nonlinear effects in the transmitter chain.

For the reasons mentioned above, it becomes important to study which are the techniques that allow us to work with high efficiency without losing linearity.

This Master thesis addresses the design of a high efficient power amplifier combined with the implementation of Crest Factor Reduction (CFR) and Digital Predistortion (DPD) techniques. Besides, the deployment of a low-cost test bench based on development boards is proposed to carry out the PA evaluation and linearization avoiding the use of expensive laboratory equipment for signal generation and analysis.

The work has been covered in stages following this order:

- A first approach to the signal processing and predistortion techniques literature and state of the art.

- Design, development and characterization of a class-E power amplifier.

- Deployment of a test bench based on development boards.

- Implementation of Matlab-based algorithms for signal generation and CFR and DPD techniques.

- Integration of the complete measurement environment, including the board-based test bench, the Matlab algorithms and the power amplifier as the DUT.

Thesis Outline

This work follows the same modular structure that was conceived during the development process.

In order to introduce the theoretical contents used throughout this project, Chapter 2 describes the nonlinear behavior of power amplifiers and the memory effect concept, next Chapter 3 details the principles of the linearization techniques, focusing on the CFR and DPD implementation.

The contributions of this Master thesis are presented in Chapter 4 with the experim en-tal design of a class-E PA and across Chapter 5 with the proposal of a test bench based on development boards for the evaluation and linearization of the PA using both CFR and DPD techniques.

Finally, Chapter 6 analyzes the results obtained during the experimental campaign and the conclusions are presented considering future improvements.

Chapter 2

NONLINEAR BEHAVIOR OF POWER AMPLIFIERS

The Power Amplifier (PA) is the main source of nonlinear effects in a transmission chain. In addition to the nonlinear distortion, the PA may also present a dynamic behavior.

A memoryless system can be described as a system where the output signal depends only of the instantaneous input signal. On the other hand, in a memory system, the output signal is a function of both the instantaneous and previous input/output signals.

Let us concentrate in nonlinear systems behavior, and how to represent and measure them.

2.1. Memoryless systems

Considering v_{in} and v_{out} as the amplifier input and output respectively, and g as a time independent constant gain, the *ideal memoryless* power amplifier transfer function can be expressed as:

$$v_{out}(t) = g.v_{in}(t) \tag{2.1}$$

Where the ideal linear amplification does not introduce in-band or out-of-band frequency components. However, the *linear distortion* appears when the gain does not behave as a constant and the phase does not present a linear expression either [GP08].

Nevertheless, in practice, a *nonlinear distortion* behavior is the responsible of spectrum distortion. Then, the PA output voltage signal v_{out} can be modeled by a polynomial expression consisting in a series of therms proportional to the input signal amplitude v_{in} and g_k the corresponding voltage gains [CP03].

$$v_{out}(t) = \sum_{k=1}^{\infty} g_k v_{in}^k(t). \tag{2.2}$$

It can be noted that the first term corresponds to the desired output signal, then the even order terms are responsible of introducing additional frequency componentes at multiples of the carrier frequency of the input signal, this is known as *Harmonic Distortion (HD)*.

Therefore, the odd terms introduce frequency components that can fall too close to the desired signal that are not easy to cancel by filtering. The intermodulation products introduces the *Intermodulation Distortion (IMD)*. While the *in-band distortion* is produced by specific nonlinear combinations that fall directly inside the interest signal bandwidth.

Two-tone Test

In order to analyze the impact of a nonlinear distortion introduced by a PA, a typical two-tone test is shown for a low-order power series model [SOGG08][BDS14].

Considering a two-carrier input signal:

$$v_{in}(t) = A_1 cos(\omega_1 t) + A_2 cos(\omega_2 t) \tag{2.3}$$

Where A_1, A_2 are the unmodulated carrier's amplitudes and ω_1, ω_2 their angular frequency. In order to simplify the analysis, a third-order power series is considered:

$$v_{out}(t) = g_1 v_{in}(t) + g_2 v_{in}^2(t) + g_3 v_{in}^3(t) \tag{2.4}$$

Introducing the input signal defined and employing trigonometrical relations, the general two-tone response will be:

$$
\begin{aligned}
v_{out}(t) = {} & \frac{g_2 A_1^2}{2} + \frac{g_2 A_2^2}{2} \\
& + A_1[g_1 + \frac{3g_3 A_1^2}{4} + \frac{3g_3 A_2^2}{2}]cos(\omega_1 t) \\
& + A_2[g_1 + \frac{3g_3 A_2^2}{4} + \frac{3g_3 A_2^3}{4}]cos(\omega_2 t) \\
& + \frac{g_2 A_1^2}{2}cos(2\omega_1 t) + \frac{g_3 A_2^2}{2}cos(2\omega_2 t) \\
& + g_2 A_1 A_2[cos((\omega_2 - \omega_1)t) + cos((\omega_2 + \omega_1)t)] \\
& + \frac{g_3 A_1^3}{4}cos(3\omega_1 t) + \frac{g_3 A_2^3}{4}cos(3\omega_2 t) \\
& + \frac{3g_3 A_1^2 A_2}{4}[cos((2\omega_1 t + \omega_2)t) + cos((2\omega_1 t - \omega_2)t)] \\
& + \frac{3g_3 A_2^2 A_1}{4}[cos((2\omega_2 t + \omega_1)t) + cos((2\omega_2 t - \omega_1)t)]
\end{aligned}
\tag{2.5}
$$

The expansion suggests the appearance of undesired spectral components additionally to the fundamental frequencies ω_1, ω_2 consisting on DC components, *HD* caused by the second and third harmonics $2\omega_1, 2\omega_2$ and $3\omega_1, 3\omega_2$ as well as *IMD* of second and third order caused by $\omega_1 \pm \omega_2$ and $2\omega_1 \pm \omega_2, 2\omega_2 \pm \omega_1$ respectively. Considering $A_1 = A_2$, the frequency components are shown in *Figure 2.1.*.
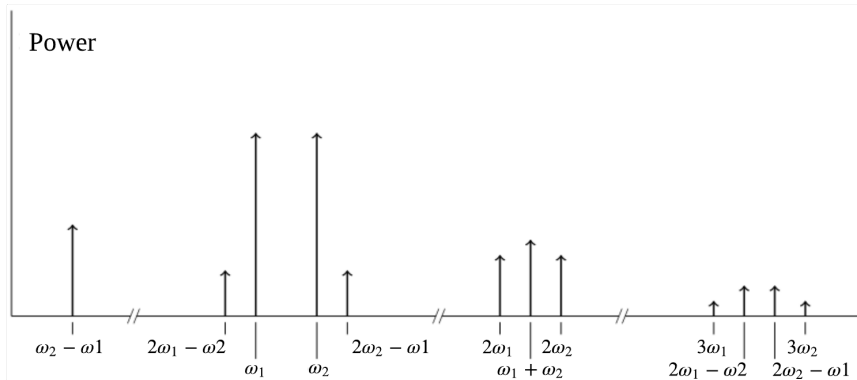

Figure 2.1: Frequency response based on a three-term memoryless power series PA [SOGG08]

.

If we extend the analysis to a modulated signal, the *Adjacent Channel Power Ratio (ACPR)* is a measure of the degree of signal spreading into adjacent channels, caused by nonlinearities in the power amplifier [Ken00].

The ACPR is defined as the ratio between the total power over the power delivered in the adjacent channels [SOGG08]:

$$ACPR = 10\log\left(\frac{\int_{f_{in-band}} |Y(f)|^2\,df}{\int_{f_{adj}} |Y(f)|^2\,df}\right)[dB],\tag{2.6}$$

where $Y(f)$ is the Fourier transform for $f_{in-band}$ corresponding to the channel frequencies as well as for f_{Adj} according to the standard first upper and lower adjacent channels.

In addition, if we consider non-constant envelope signals presenting schemes that modulate both amplitude and phase together like the *Quadarture Amplitude Modulation (QAM)*, the nonlinear distortion suffered during the amplification process can be measured with the *Error Vector Magnitude (EVM)* [GP08]. The EVM is defined as the square root of the ratio of the mean error vector power to the mean reference power expressed as a percentage:

$$EVM = \sqrt{\frac{\frac{1}{N}\sum_1^N(\Delta I^2 + \Delta Q^2)}{S_{max}^2}}[\%].\tag{2.7}$$

The ACPR and the EVM are figures of merit used by the communications standards to specify the spectral regrowth limitations and the maximum degradation permitted, depending on the modulation scheme employed and the use of any codification.

2.2. Memory systems

Observing RF power amplifiers presenting memory effects, it is found that its precise gain is not only a function of the input signal amplitude at the same instant, but also dependent of the recent history of the input-output signals as well.

When working with high-speed envelope signals presenting significant bandwidths it become important to reconsider the degradation resulting from memory effects which may appear in the form of asymmetries of the IMD products in the frequency domain and dispersion in the decision points of a constellation that can be observed in the time domain [MG11].

They can be traced to two main sources, the *Electrical Memory Effects* are caused by frequency-dependent envelope, fundamental or second harmonic node impedances. Besides the *Thermal Memory Effects* are caused by dynamic self-heating produced by electrothermal couplings which affect low modulation frequencies up to the megahertz range [VR03].

In addition to, the impedance variation and mismatching found in the input and output networks, the bias networks and the power supply of the transistor contribute to the emergence of memory effects as depicted in *Figure 2.2.*.
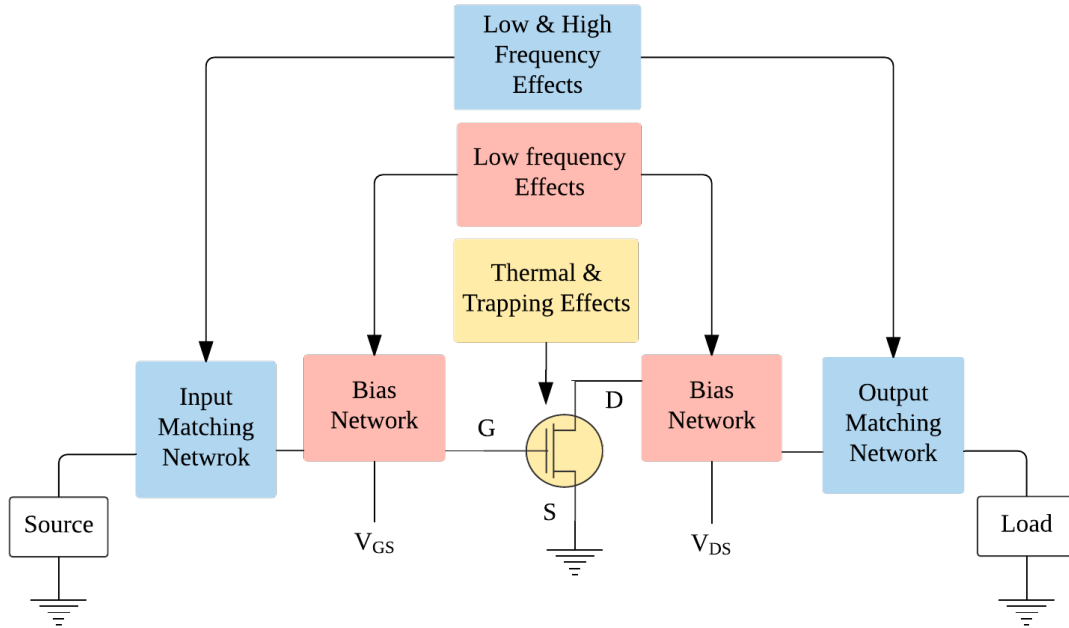
Figure 2.2: Memory Effects sources distribution adapted from [SA05]

2.3. Linearity measures

With the increase of spectrally efficient modulation techniques in mobile communications, the linearity of the RF power amplifier has become a critical design issue for digital modulation schemes with non-constant envelope-modulation techniques.

The *Peak to Average Power Ratio (PAPR)* is defined as the ratio between the maximum value of the instantaneous power P_{peak} and the average power of the signal P_{avg} [Ken00]:

$$PAPR = 10\log_{10}\left(\frac{P_{peak}}{P_{average}}\right)[dB], \tag{2.8}$$

Considering that a highly linear PA will be require to fulfill stringent spectral mask and modulation accuracy requirement, this is often achieved with significant PA back-off that considerably reduces the PA efficiency taking into account that the maximum efficiency performance is obtained near the saturation point.

The operation at a reduced power level known as *back-off* is defined as the difference between the saturation point and the average power level. It can be either defined as input back-off (IBO) and output bach-off (OBO) [SA05]:

$$IBO = P_{sat,in} - P_{avg,in} \tag{2.9}$$

and

$$OBO = P_{sat,out} - P_{avg,out}, \tag{2.10}$$

Where $P_{sat,in}$ and $P_{sat,out}$ are the input and output saturated power in dBm, and $P_{avg,in}$ and $P_{avg,out}$ the average input and output power in dBm.

In order to analyze the operation of the PA, *Figure 2.3.* shows some commonly used measures as the *saturation point* and the *1 dB compression point* P_{1dB} that refers to the output power

level at which the amplifier's transfer characteristic deviates from that of and ideal characteristic by 1 dB.
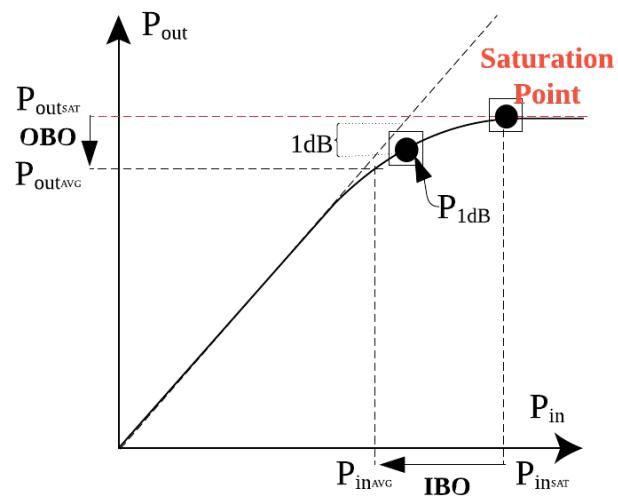

Figure 2.3: Amplifiers's transfer characteristic

Chapter 3

LINEARIZATION TECHNIQUES

The use of linearization techniques to deal with the trade-off between system linearity and power efficiency has been extensively studied during the last years in order to fulfill the linearity requirements imposed by the communications standards in the transmitter chain.

The objective consists in reducing in-band and out-of-band distortion, maximizing the power efficiency and allowing the operation with spectrally efficient modulation schemes.

3.1. Linearization methods

The *Circuit Level Linearization* consists in the implementation of linearization techniques directly to the power transistor, for example *Thermal compensation approach* to compensate memory effects distortion caused by temperature variations, *Active bias for dynamic power supply approach* in order to reduce power consumption and *Harmonic Terminations and Harmonic Injection* designing for a proper harmonic termination of the input and output ports. On the other hand, the *System Level Linearization* proposes the implementation of linearization techniques at a higher level providing a better distortion reduction. However, due to its high cost and size is commonly employed in professional equipments [GP08].

Linearizers aimed at reducing distortion, propose to measure the present distortion in the PA output and then try to reduce it, this include the *Feedback* and *Feedforward* techniques.

In contrast, the linearizers designed for avoiding distortion are focused on preventing the emergence of nonlinear effects at the PA output. To achieve this objetive among the many techniques that have been proposed we will consider:

- *Power back-off:* consists in adjusting the operation point of the PA to avoid working close to the compression point. (Low efficiency)

- *Predistortion*: introduces a device called predistorter preceding the PA in order to counteract its nonlinear behavior.

3.2. Digital Predistortion (DPD)

Without predistortion, the power amplifier operation is a trade-off between linearity and efficiency. Operating the amplifier at a power level near saturation improves efficiency but introduces severe nonlinearities.

The digital predistortion technique bring forward the concept of applying a nonlinear transformation to the digital signal that opposes the subsequent nonlinearity generated by the power amplifier.

Considering $u[n]$ the original input signal, $x[n]$ the predistorted signal and F_{DPD} the nonlinear predistortion function [Bra11]:

$$x[n] = F_{DPD}\{u[n]\}. \tag{3.1}$$

The predistorted signal may also be described as

$$x[n] = G_{DPD}(|u[n]|).u[n], \tag{3.2}$$

where $G_{DPD}(|u|)$ is the nonlinear gain of the DPD, controlled by a set of coefficients based on existing or real-time measurements of the PA nonlinearity. Converting the trade-off in efficiency versus DPD complexity.

Figure 3.1 shows the basic principles of an open-loop predistorter. In order to allow a more robust operation of the linealizer, most current predistortion solutions introduces some kind of feedback mechanism to implement *adaptative predistortion*.
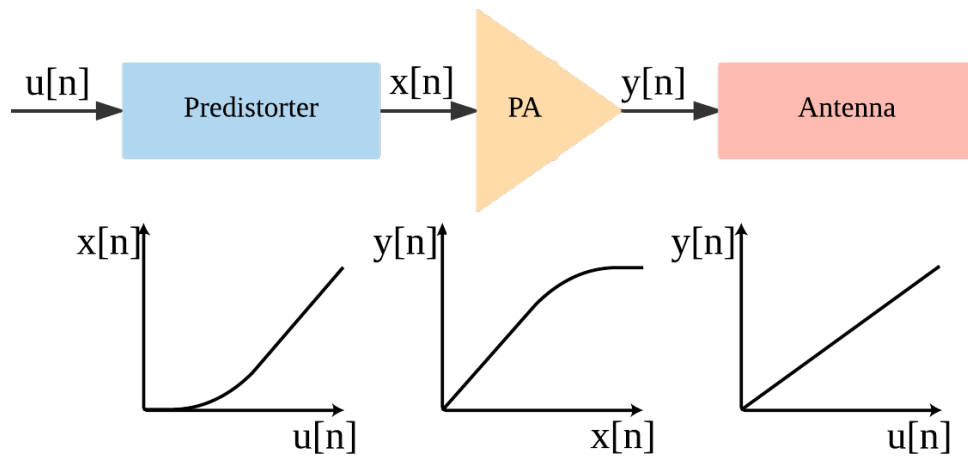

Figure 3.1: Principle of Predistortion

Taking into account the implementation of the predistorter, *Figure 3.2.* presents possible alternatives for its realization. According to the position of the predistorter in the complete transmitter, predistortion can be carried out at *radiofrequency*, *intermediate frequency* or *baseband* [MG11].

Considering the technology employed, *analog predistortion* consists in using circuitry to implement the predistoter. On the other hand, *digital predistortion* can achieve better results allowing corrections of possible unexpected unbalances. Nevertheless, the main drawbacks are related to power consumption and bandwidth limitations due to the capabilities of the Digital Signal Processor (DSP) employed.

Furthermore, two main approaches can be found in digital predistortion. The digital *data predistortion* technique is custom tailored to specific digital modulation formats and focus on compensating the constellation, such that the predistorter coeficients are optimized by minimizing the EVM decreasing the in-band distortion introduced by the PA. However, it does not directly compensate the out-band distortion.

In contrast, digital *signal predistortion* is aimed at cancelling both in-band and out-band distortion, as long as the saturation level of the PA permits it. This technique is totally independent from the PA technology, amplifier class, band of operation and signal modulation.
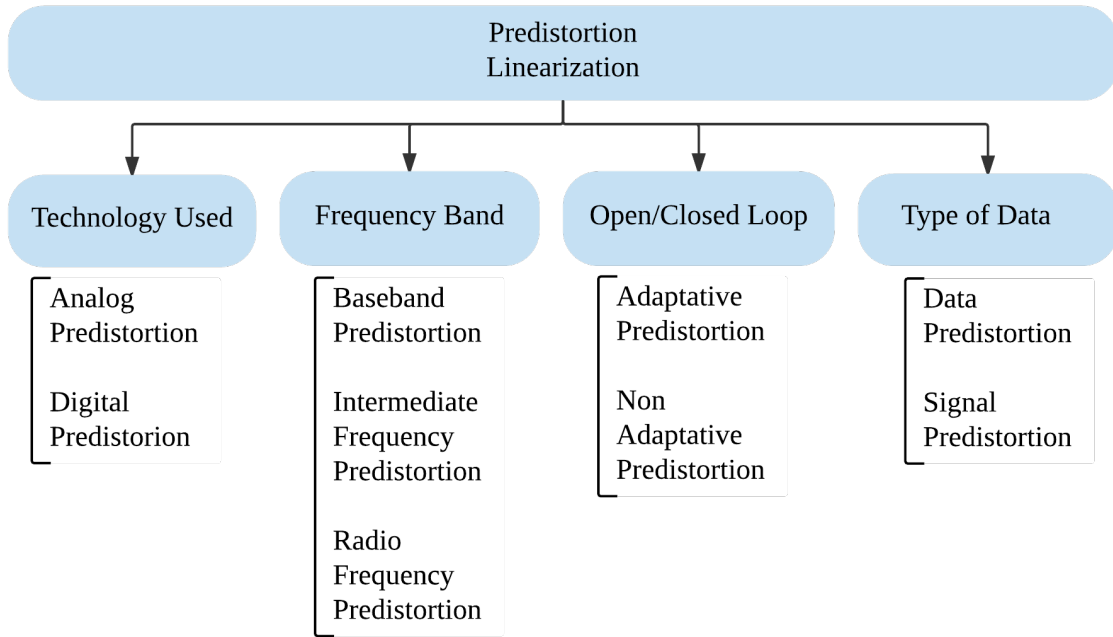
Figure 3.2: Predistorters classification adapted from [MG11]

3.2.1. Power amplifier behavioral modelling

Volterra Series

In order to include the memory effects in the PA model, the Volterra series proposes a combination of linear convolution and nonlinear power series, which can be used to describe the input/output relationship of a general nonlinear, causal and time-invariant system with fading memory [And11].

In the discrete time domain, a Volterra series can be written as [Sch80][MS00]:

$$v_{out}(n) = \sum_{p=1}^{\infty} \sum_{i_1=0}^{\infty} \ldots \sum_{i_p=0}^{\infty} h_p(i_1, \ldots i_p) \prod_{j=1}^{p} v_{in}(n - i_j), \tag{3.3}$$

where $v_{in}(n)$ and $v_{out}(n)$ represents the input and output signal respectively, and $h_p(i_1, \ldots, i_p)$ is called the pth order *Volterra kernel*.

Using the full Volterra series for modelling and DPD is generally not recommended, due to the high number of coefficients the problem rapidly becomes ill-conditioned. For these reasons, other models have been developed by truncation of the original series considering finite nonlinear order and finite memory length [EB16].

Memory polynomial

The *Memory Polynomial (MP)* proposed by Kim and Konstantinou [KK01] captures both memory effects and nonlinear behavior of a PA, describing the algorithms employed to obtain the DPD function based on the estimated model parameters.

Considering $x[n]$ as the input sequence and $\hat{y}[n]$ the estimated output [BDS14]:

$$\hat{y}[n] = \sum_{k=1}^{M} \sum_{p=1}^{P} a_{kp} \gamma_{kp}[n], \qquad (3.4)$$

where a_{kp} are the model coefficients and γ_{kp} is called the *basis functions*.

The selection of the *basis functions* set is important for the predistortion to achieve the required distortion cancellation [Bra13]:

$$\gamma_{kp}[n] = x[n - \tau_k] \, |x[n - \tau_k]|^{p-1}, \qquad (3.5)$$

and τ_k is the $k^{th} - component$ of the delay vector $\underline{\tau}$ defined as

$$\underline{\tau} = [\tau_1 \tau_2 ... \tau_M]. \qquad (3.6)$$

where each component of $\underline{\tau}$ is called *memory taps* and can be either consecutive or non-consecutive integer values.

On the other hand, the coefficients a_{kp} composed the coefficient-vector $\underline{a}$ which has a length equal to the number of memory taps times the order of the polynomial (MxP).

Then, the *Equation 3.4* can be written as:

$$\hat{\underline{y}} = \mathbf{F_x} \underline{a}, \qquad (3.7)$$

such that, $\hat{\underline{y}}$, $\underline{a}$ and the matrix $\mathbf{F_x}$ are given by

$$\hat{\underline{y}} = [\hat{y}(0) \hat{y}(1) ... \hat{y}(N-1)]^T, \qquad (3.8)$$

$$\underline{a} = [a_{11} a_{12} ... a_{MP}]^T, \qquad (3.9)$$

$$\mathbf{F_x} = [f_{11} f_{12} ... f_{MP}]^T, \qquad (3.10)$$

where N is the number of samples and $\mathbf{F_x}$ the matrix composed by the basis functions generated using the input signal $x[n]$, then each component $\underline{f_{kp}}$ is defined as:

$$\underline{f_{kp}} = \left[\gamma_{kp}(0) \gamma_{kp}(1) ... \gamma_{kp}(N-1) \right]^T, \qquad (3.11)$$

.

Finally, the coefficients $\underline{a}$ can be obtained employing the *Least Squares* method such that:

$$\underline{a} = \left(\mathbf{F_x}^H \mathbf{F_x} \right)^{-1} \mathbf{F_x}^H \underline{y}, \qquad (3.12)$$

where $(.)^H$ denotes the conjugate transpose of the matrix $\mathbf{F}$ and $\underline{y}$ the measured output.

Generalized memory polynomial

Furthermore, the *Generalized Memory Polynomial (GMP)* introduces a combination of the *Memory Polynomial* with cross terms between the signal and lagging and leading exponentiated envelope terms [MMK$^+$06] [GM12] .

$$
\begin{aligned}
\hat{y}[n] =& \sum_{l=0}^{L_A} \sum_{p=0}^{P_A} a_{pl} x[n - \tau_l^A] \left| x[n - \tau_l^A] \right|^p \\
&+ \sum_{l=1}^{L_B} \sum_{m=1}^{M_B} \sum_{p=0}^{P_B} b_{pml} x[n - \tau_l^B] \left| x[n - \tau_l^B - \tau_m^B] \right|^p \\
&+ \sum_{l=1}^{L_C} \sum_{m=1}^{M_C} \sum_{p=0}^{P_C} c_{pml} x[n - \tau_l^C] \left| x[n - \tau_l^C - \tau_m^C] \right|^p ,
\end{aligned}
\tag{3.13}
$$

The first term corresponds to the *Memory Polynomial* where L_A and P_A are the number of coefficients for aligned signal and envelope. Moreover, L_B, M_B and P_B are the number of coefficients for signal and lagging envelope and L_C, M_C and P_C for signal and leading envelope.

As we progress to the more advance variations of memory polynomials, the effectiveness of the predistortion implementation generally increases. However, the increase in computation complexity involved has to be taken into account in order to compare the effectiveness with other models behavior or linearization techniques.

Accuracy of the model behavior representation

In order to evaluate the accuracy of the model behavior representation, the *Normalized Mean Square Error (NMSE)* is defined as

$$
NMSE = 10 log \left(\frac{\sum_{n=1}^{L} |y_{real}[n] - y_{mod}[n]|^2}{\sum_{n=1}^{L} |y_{real}[n]|^2} \right) [dB],
\tag{3.14}
$$

considering the deviation between the PA measured output y_{real} and the model estimated output y_{mod}. This figure of merit tells us about the similarity between the model signal and the real measurement.

3.2.2.   Adaptative implementation

The process of identification contemplates the use of a weighted Least Squares method, such that the goal is to minimized the cost function defined as [GM12]:

$$
J[n] = |e[n] - \hat{e}[n]|^2
\tag{3.15}
$$

defined as the quadratic difference between the real error and the estimated error.

According to the definition of this error, the *Direct* and *Indirect Learning* adaptive implementations are proposed.

Direct learning

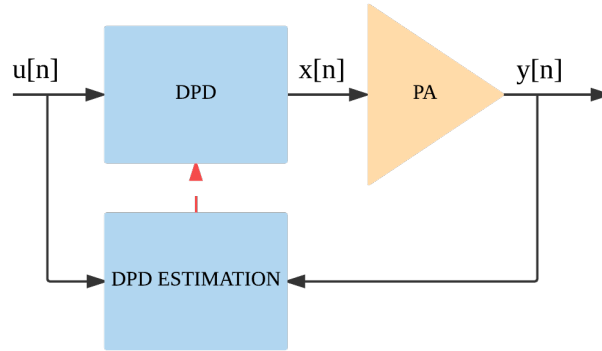Let us consider the following scheme shown in *Figure 3.3* [GM12]:

Figure 3.3: Direct learning method

The *Direct Learning* method proposed by Braithwaite [Bra13] as a Model Reference Adaptive System (MRAS) is analyzed below [BDS14].

The error $e[n]$ and the estimated error $\hat{e}[n]$ are defined as

$$e[n] = y[n]G_0^{-1} - u[n], \tag{3.16}$$

$$\hat{e}[n] = \mathbf{F_u}\underline{\Delta a_i}, \tag{3.17}$$

respectively, while G_0 represents the linear gain of the PA, $\mathbf{F_u}$ the basis waveforms matrix constructed with the original input signal $u[n]$ and $\underline{\Delta a_i}$ is the coefficients vector computed at the ith-iteration.

Then, the cost function to be minimize is the square of the difference between the real error and the estimated one

$$J[n] = |e[n] - \hat{e}[n]|^2. \tag{3.18}$$

Knowing the PA output, then it is possible to estimate the least-squares solution to calculate the estimated error and the coefficients needed for the adaptive process:

$$\underline{\Delta a_i} = (\mathbf{F_u}^H\mathbf{F_u})^{-1}\mathbf{F_u}^H\underline{e}, \tag{3.19}$$

$$\underline{a_{i+1}} = \underline{a_i} + \lambda\underline{\Delta a_i}. \tag{3.20}$$

The weight factor λ is a value between 0 and 1, usually reduced at each iteration as it converges. Therefore, the additive distortion $d[n]$ can be written as

$$d[n] = \mathbf{F_u}\underline{a_i}, \tag{3.21}$$

and the new PA input signal will be

$$x[n] = u[n] - d[n]. \tag{3.22}$$

For the first iteration, it must be considered $\underline{a_1} = \underline{\Delta a_0}$ and $x[n] = u[n]$.

Indirect learning

Following the procedure proposed for the *Direct Learning* method, let us focus on the scheme proposed in *Figure 3.4* for the *Indirect Learning* implementation [GM12][BDS14].
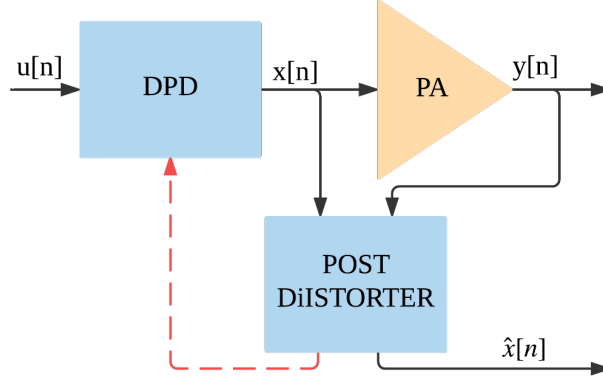

Figure 3.4: Indirect learning method

Where the error now is defined as the difference between the real and the estimated input signal:

$$e[n] = \hat{x}[n] - x[n], \tag{3.23}$$

and the cost function becomes

$$J[n] = |\hat{x}[n] - x[n]|^2. \tag{3.24}$$

For this implementation, the output is postdistorted in order to estimate the input signal. Therefore, the postdistorted estimated output signal can be obtain ed as

$$\hat{d}[n] = \mathbf{F_y}\underline{a_i}, \tag{3.25}$$

where $\mathbf{F_y}$ is the basis functions matrix constructed with the output signal $y[n]$.

Furthermore, the estimated PA input signal is defined as

$$\hat{x}[n] = y[n]G_0^{-1} - \hat{d}[n]. \tag{3.26}$$

And the error is used to estimate iteratively the coefficients needed to compute the new PA input.

$$\underline{\Delta a_i} = (\mathbf{F_y}^H \mathbf{F_y})^{-1} \mathbf{F_y}^H \underline{e} \tag{3.27}$$

$$\underline{a_{i+1}} = \underline{a_i} + \lambda \underline{\Delta a_i}. \tag{3.28}$$

To finish with, notice that the starting condition for the first iteration is $a_1 = 0$.

3.3. Crest Factor Reduction Technique (CFR)

Considering the trade-off between efficiency and linearity due to the high PAPR found in telecommunications signals nowadays, it is common to look at a PAPR reduction to the input signal $u[n]$. Hence, this solution becomes a trade-off between suppressing the peaks without compromising the information contained in the input signal.

Let us consider the *Scaled Peak Cancellation* technique [KCSK07] , where A represents the suppressing threshold and the clipper output $c[n]$ is defined as

$$c[n] = \begin{cases} \frac{A}{|u[n]|} & \text{if } |u[n]| > A, \\ 1 & \text{if } |u[n]| \leq A. \end{cases} \tag{3.29}$$

Therefore, the clipped pulse $p[n]$ is

$$p[n] = u[n] - u[n]c[n]. \tag{3.30}$$

To complete the process, the clipped pulse must be filtered with a low-pass filter. Finally, the PAPR-reduced signal $z[n]$ is obtained as follows

$$z[n] = u[n] - \alpha[n]c[n]h[n] \tag{3.31}$$

$$\alpha = \frac{max(|p[n]|)}{max(|p[n]*h[n]|)} \tag{3.32}$$

where $h[n]$ is the impulse response of the filter, * the convolution operation and α is a weight factor.
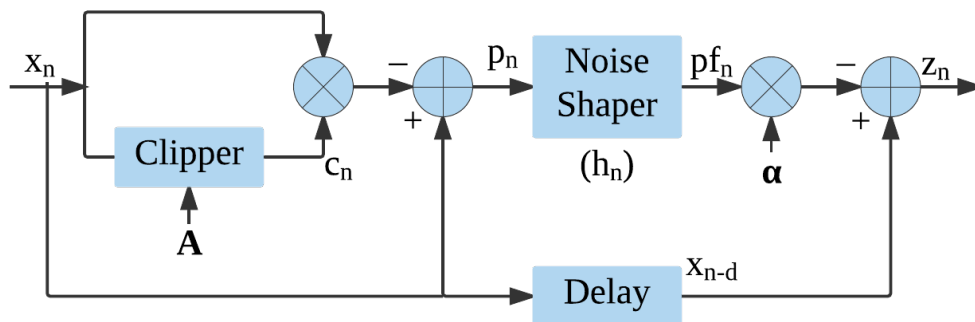

Figure 3.5: CFR Implementation adapted from [KCSK07]

Chapter 4

DESIGN OF A CLASS-E POWER AMPLIFIER

Taking into account that the PA found in the transmitter is the main responsible of the consumption of the available energy across the communication chain, a maximization efficiency focused design provides a solution in order to decrease the energy supplied to the system with the benefits of reducing the power dissipation while avoiding the componentes degradation and lengthening the life time [PGCT].

4.1. Linearity vs. Efficiency

Considering P_{out} as the output RF power and P_{DC} the power taken from the DC source, the *efficiency* can be defined as [VR03]:

$$\eta = \frac{P_{out}}{P_{DC}}. \tag{4.1}$$

Moreover, if the power of the input signal P_{IN} is considered, the *Power-Added Efficiency (PAE)* can be expressed by

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}}. \tag{4.2}$$

Therefore, it can be demonstrated that significant improvements in total efficiency can be obtained by improving the efficiency of the last amplifier stage.

The need to avoid nonlinear effects in the amplification requires to keep the peak amplitudes of the transmitted signal bellow the output peak of the amplifier, described as back-off operation, which degrades the average efficiency [GP08].

However, the PA efficiency depends also on the power transistor operation class and can be divided in two main groups considering the selection of the transistor operating point which determines the linearity response as well as the power handling and efficiency [SA05].

Amplifier Operation Classes

Among the *highly-linear* operation classes, *current-source* amplifiers (class-A, class-AB, B and C) are classified according to the conduction angle that defines the portion of the input RF voltage cycle that will be convert in output current depending on the polarization point of the transistor. They are commonly used for wireless communication based on non-constant envelope modulation.

On the other hand, *highly-efficient* amplifiers like the class-D, class-E and class-F among others are called *switched-mode* amplifiers since they work as a high speed switch. They are widely used by applications that require a high power output. Consequently, it is important to have a high level of efficiency to cover the efficiency specifications due to the power and cooling limitations [Cri99][MT+16].
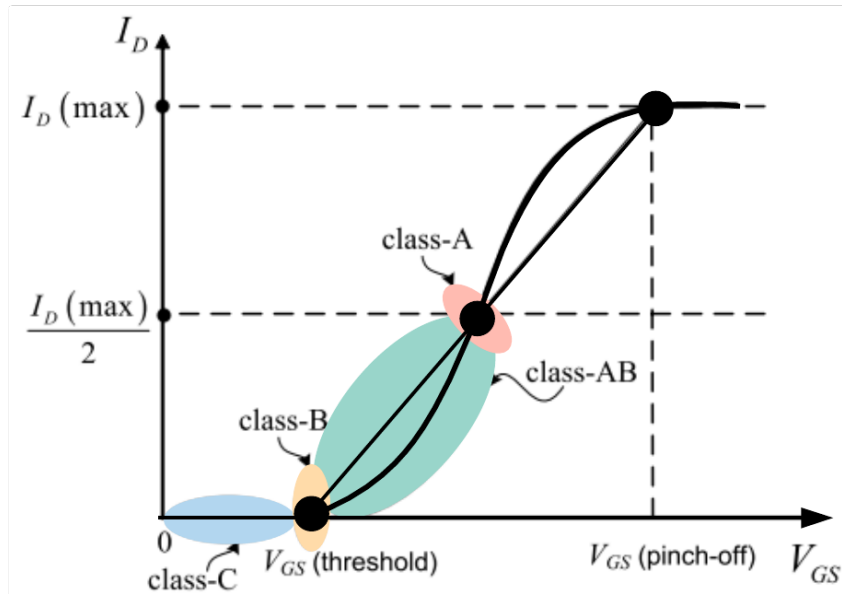
Figure 4.1: Power amplifiers classes adapted from [SA05]

It becomes clear that efficiency and linearity are opposite requirements in traditional power amplifier design, and if the goal is to achieve good linearity with reasonable efficiency, a linearization technique has to be employed.

The main idea of linearization is that the power amplifier itself is designed to achieve good efficiency at the expense of linearity. Then, in order to fulfill the linearity requirements it will be necessary to introduce some type of external linearization [VR03].

4.2. Principles of operation of a Class-E amplifier

The class-E power amplifier operates employing a single transistor in switch-mode and an output-tuned circuit in order to filter the unwanted harmonics generated across the non-linear amplification process as shown in *Figure 4.2* [SS75].

To simplify the analysis it is necessary to make some assumptions [Raa77] [PGCT]:

- First, let us suppose a duty cycle of 50% for an optimal performance of the circuit.

- Moreover, the ON resistance will be considered null and the OFF resistance as infinity.

- The capacitor C_s considers a linear parasitic output capacity.

- Lastly, the current through the load will be ideally sinusoidal at the fundamental frequency f_s.
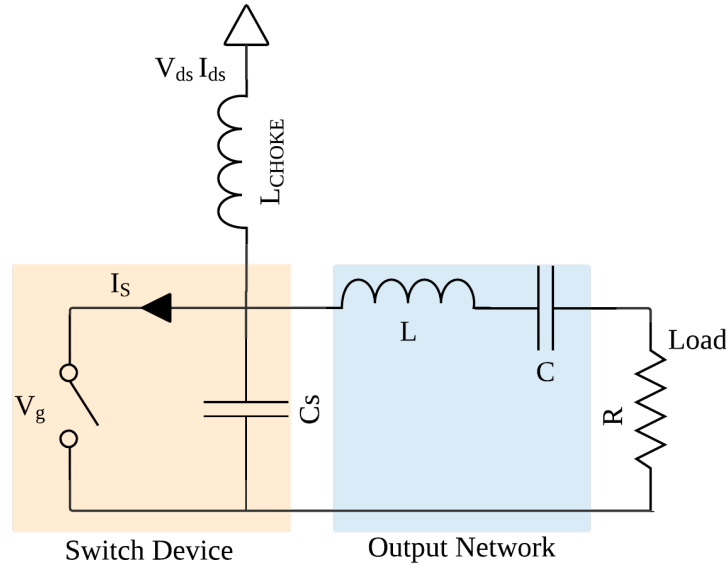
Figure 4.2: Original Topology of the high-efficient Class-E amplifier [SS75]

The operation of a *switch-mode* amplifier consists mainly in try to prevent that the current I_{ds} and the voltage V_{ds} become non-zero simultaneously in order to obtain a null dissipated power.

To minimum losses in the switching process, the switch voltage must comply the following conditions:

$$v(\omega t)|_{\omega t=2\pi} = 0 \tag{4.3}$$

and

$$\frac{dv(\omega t)}{d\omega t}\bigg|_{\omega t=2\pi} = 0 \tag{4.4}$$

Those conditions are known as *Zero Voltage Switching (ZVS)* and *Zero Voltage Derivative Switching (ZVS)*. The ZVS condition prevents losses due to the capacitor discharge during the OFF-ON transition while ZVDS avoid the current transfer from the capacitor to the switch until the transistor is not fully conducting [MT+16].

This switch behavior is obtained biasing the device close to pinch-off point and introducing a large amplitud input signal. Besides, it is important to ensure that the capacitor C_s remains unloaded during the state changes.

Then, the key factor to get a high efficiency amplifier in class-E operation is found in the output network design. It is essential that the load impedance seen from the switched output will be equal to Z_{net1} at f_s [Mad95]. Moreover, high impedance conditions must be ensure for all the higher harmonics generated in order to obtain, ideally, a pure sinusoidal signal at the fundamental frequency f_s at the output:

$$\begin{cases} Z_{net1}(\omega) \cong \frac{0,28015}{\omega_s C_s} e^{j49,0524°}; \\ \\ Z_{netN} = \infty, (N=2,3,...). \end{cases} \tag{4.5}$$

4.3. Design of a class-E power amplifier at 2,4 GHz

This section outlines the design of a class-E power amplifier at 2,4 GHz carried out at the *Department of Communications Engineering of the University of Cantabria* under the supervision of profesor José Angel García García.
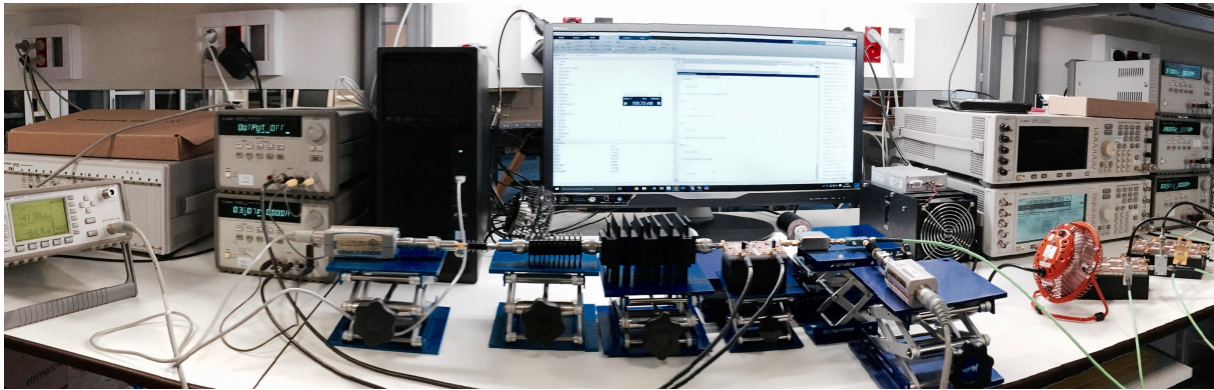

Figure 4.3: Experimental setup

It won't be possible to follow a theoretical class-E design since the transistor behavior for this frequency does not comply the model conditions expected, in other words it can not be represented by a switch in parallel with a capacitor as shown in *Figure 4.2*.

Nevertheless, the procedure followed consisted in optimizing the drain terminations for the fundamental frequency and its harmonics, considering the load-pull simulations for maximum efficiency employing the non-linear model provided by the transistor manufacturer. Finally, we can state that the resulting waveforms (especially the drain voltage) are fairly similar to those that could be expected within the continuity of class-E modes.

4.3.1. Simulation

The power amplifier design begins with the selection of the transistor. The CGH35030F is a gallium nitride (GaN) high electron mobility transistor (HEMT) designed specifically for high efficiency, high gain and wide bandwidth capabilities.

Taking as a starting point the CAD model of the transistor, the *I/V* curve is obtained for a drain voltage V_{ds} of 28 V, which is a standard available voltage at any communication system.

After analyzing the *I/V* curve, the gate voltage V_g is set just above the pinch-off voltage (-3,5 V) defining the operation mode.

The first approach consists in analyzing the S22 (output port voltage reflection coefficient) response for the configuration mentioned before for a wide frequency range regarding the output impedance shown by the transistor*(Figure 4.4)*.

To analyze the input power needed to work close to a saturation point, the desired theoretical load for a class-E Power Amplifier is calculated using the output capacitance taken from the S22 analysis at the fundamental frequency *(Equation 4.5)*.

$$z_{net1}(\omega) = \frac{0.1836}{\omega * C_out} + \frac{0.2116}{\omega * C_out} = 3,0773 + j3,5466 \tag{4.6}$$

Using this load impedance, the simulation consists in finding the highest power input before rectification. From this analysis a power input of 39 dBm is found.
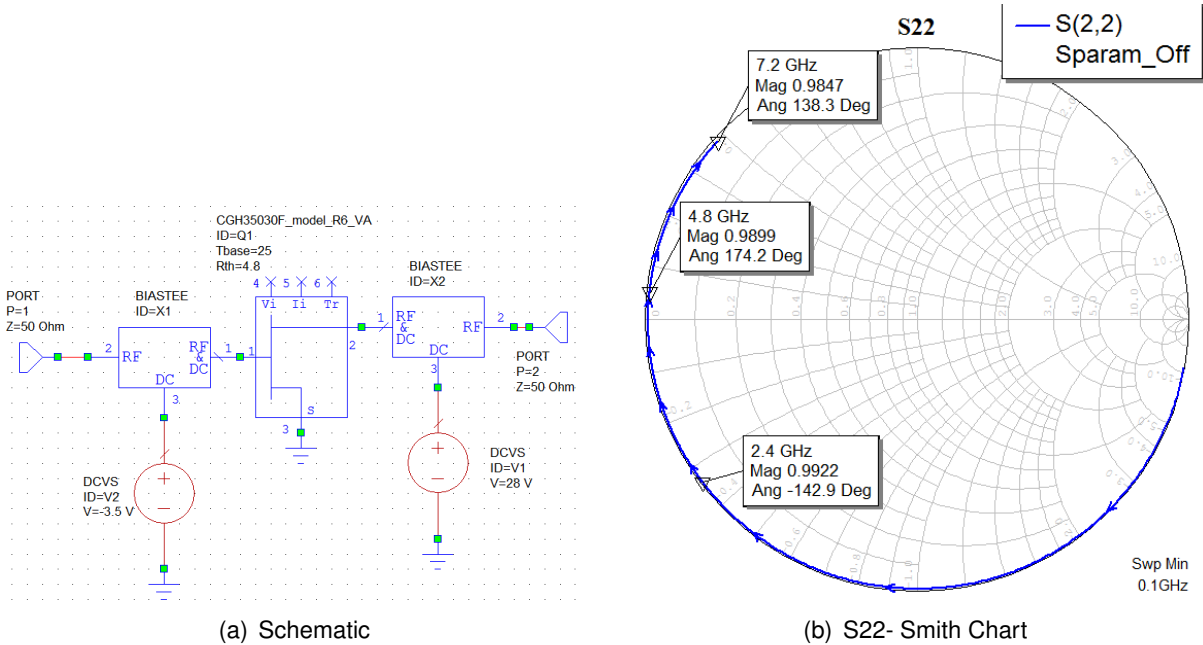

(a) Schematic

(b) S22- Smith Chart

Figure 4.4: S22 CGH35030F Analysis

Designing for optimum power transfer means to find the best output network in terms of power delivery to the load. To deal with, a load-pull analysis is performed to find the fundamental impedance for maximum efficiency. For this simulation many configurations of second and third harmonic impedance termination have been proven from shortcut to open circuit.
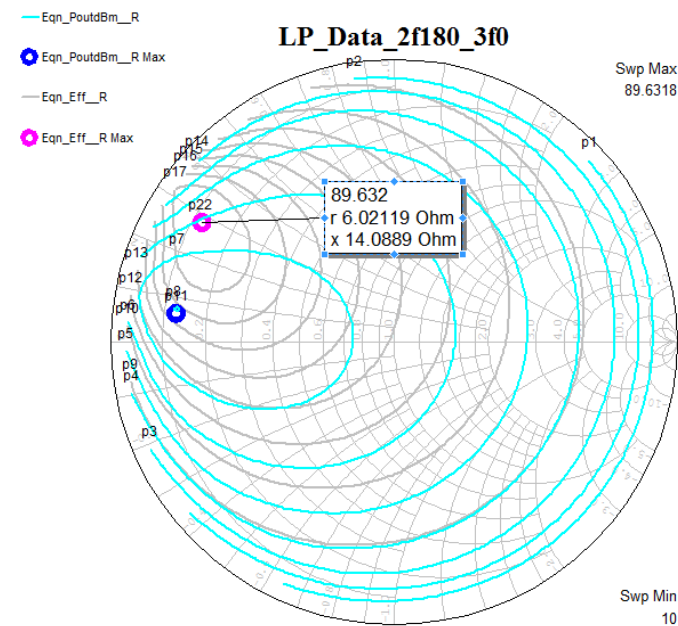

Figure 4.5: Load-pull simulation

After simulating many variations in the third harmonic termination without observing a considerable impact in efficiency, we decided to avoid the implementation of the third harmonic termination since it would be hard to obtain a good approximation employing lumped elements at 7,2 GHz without introducing considerable losses.

For the output network synthesis we considered:

- The first element introduced is a capacitor immediately after the drain output that allows us to fix a shortcut for 4,8 GHz.

- An inductance is introduced between the drain output and the supply in order to build a resonant circuit at 2,4 GHz. Its function consists on bringing the fundamental impedance termination near the center of the Smith Chart (50Ω) while avoiding the impact of the second harmonic termination at the fundamental frequency.

- To obtain the fundamental impedance found during the load-pull analysis for maximum efficiency, a second capacitor is introduced after testing different values and line length distances.

- Finally, the biasing network is introduced considering both inductance and capacitor real behavior. The capacitors have been chosen to present a resonance frequency close to 2,4 GHz to lower the losses. On the other hand, we look for a L_{CHOKE} that behaves like an open circuit at the fundamental frequency.

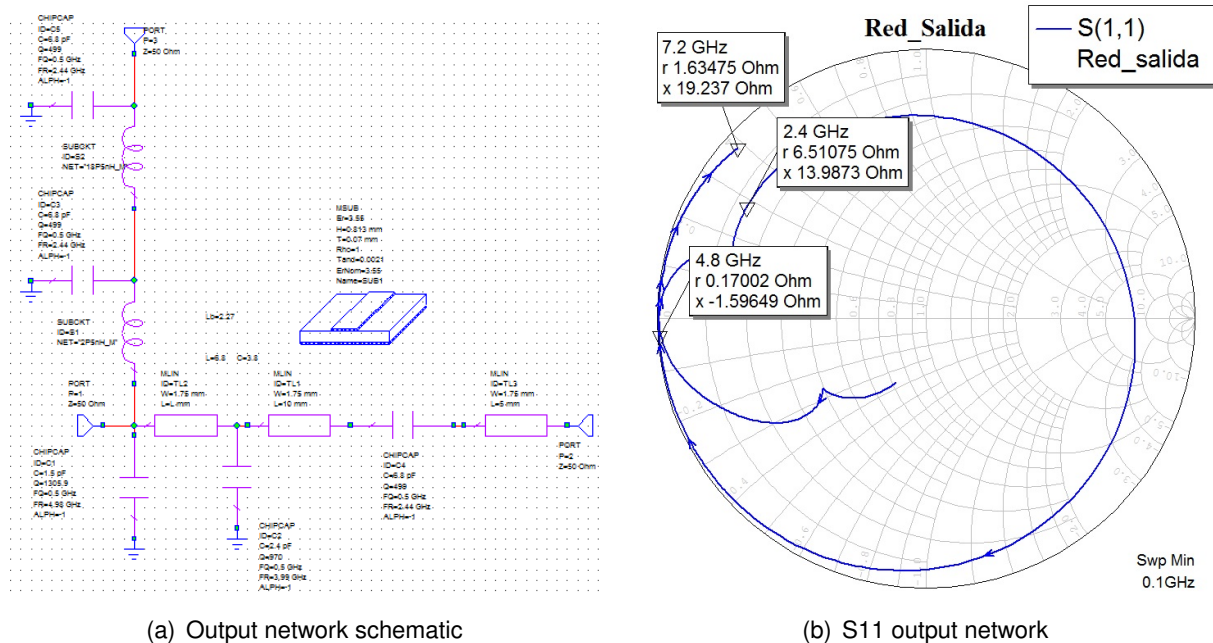(a) Output network schematic

(b) S11 output network

Figure 4.6: Output network synthesis

Considering the input reflection coefficient shown by the transistor with the output network designed, a conjugated matching network is implemented introducing a capacitor very close to the gate terminal. For gate biasing network, the design proposes the same values found for the drain biasing implementation.

After introducing the input network, a power input sweep is performed in other to evaluate the new maximum input power allowed before observing current at the gate terminal.

Design Results

The final design shown the following response for an input power sweep:
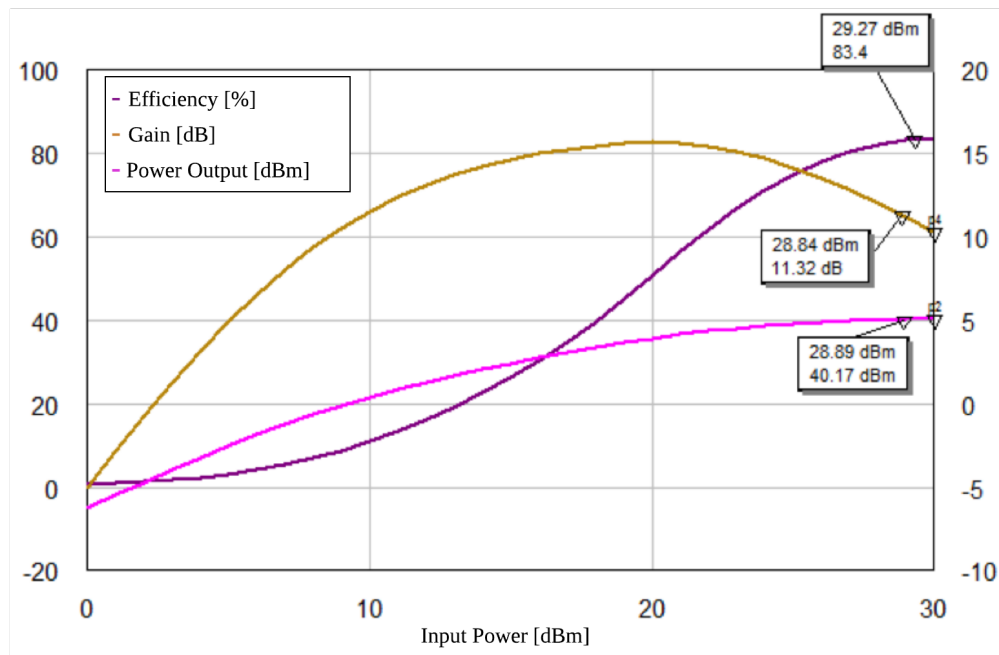

Figure 4.7: Final design simulation

It becomes clear that the best performance is obtained for the maximum input power as expected.

We conclude that a maximum efficiency of 83% can be obtained in simulation. In this point, the gain has already started to decrease taking a value around 11,5 dB and 40 dBm power output level.

4.3.2. Experimental Implementation

Considering the simulation as a starting point, the experimental implementation was carried out in a modular way by iterating between measurements and simulations. For this prototype, a generic PCB is employed for both input and output networks.

Taking into account the expected S11(input port voltage reflection coefficient) found in *Figure 4.6* for the output network, the procedure consists in introducing the elements step by step and verifying after each iteration the results obtained with the help of a network analyzer.

We began looking at the second harmonic termination starting from the simulated capacitor value in order to find the best short circuit, then the following elements were introduced

and tuned to reach the desired fundamental impedance. It should be noted that, the efficiency becomes very sensitive to the distance of the second capacitor introduced to fix the fundamental impedance. After finding the best configuration, the biasing network was introduced and checked.

For each iteration, the network-analyzer measure was introduced in the simulation as an output network block in order to have an approximation of the efficiency that could be reach. This method allow us to study the impact of the output network during development in the amplifier response before mounting the transistor.
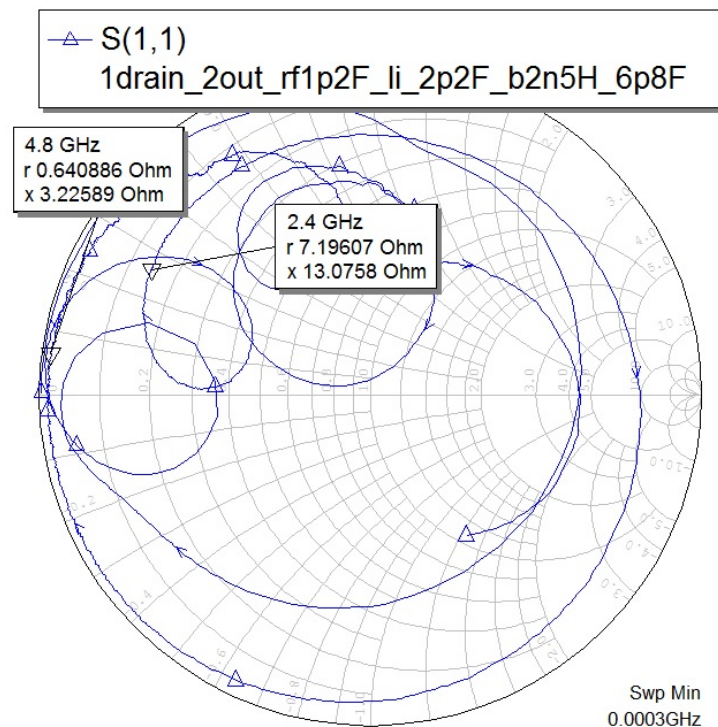

Figure 4.8: Experimental Output S11

The following step consisted in assembling the transistor to the output network including only the biasing input network without the matching network.

For the measurements, a pre-amplifier stage was introduced to reach the high input required level. Considering a V_{DS} of 28 V, we had begun with a -4 V gate voltage increasing it until a drain current is observed. Hence, a -3,6 V gate voltage had been employed.

Before proceeding, it was important to verify the absence of undesired output oscillations with a spectrum analyzer.

The last stage contemplated the addition of the input matching network. The best adjustment is found for a two-parallel configuration of capacitors close to the gate terminal, the tuning procedure consisted in comparing configurations in order to find the lowest power input level.

After introducing the input matching network, a last adjustment is performed to center the maximum efficiency point at 2,4 GHz.

It is important to note, that better results could be found implementing an input network designed using transmission lines. Nevertheless, the technique used has the advantage of having greater flexibility for adjustment avoiding iterative board design and manufacturing time.

Amplifier characterization for $V_G =$-3,6 V / $V_{ds} =$28 V.

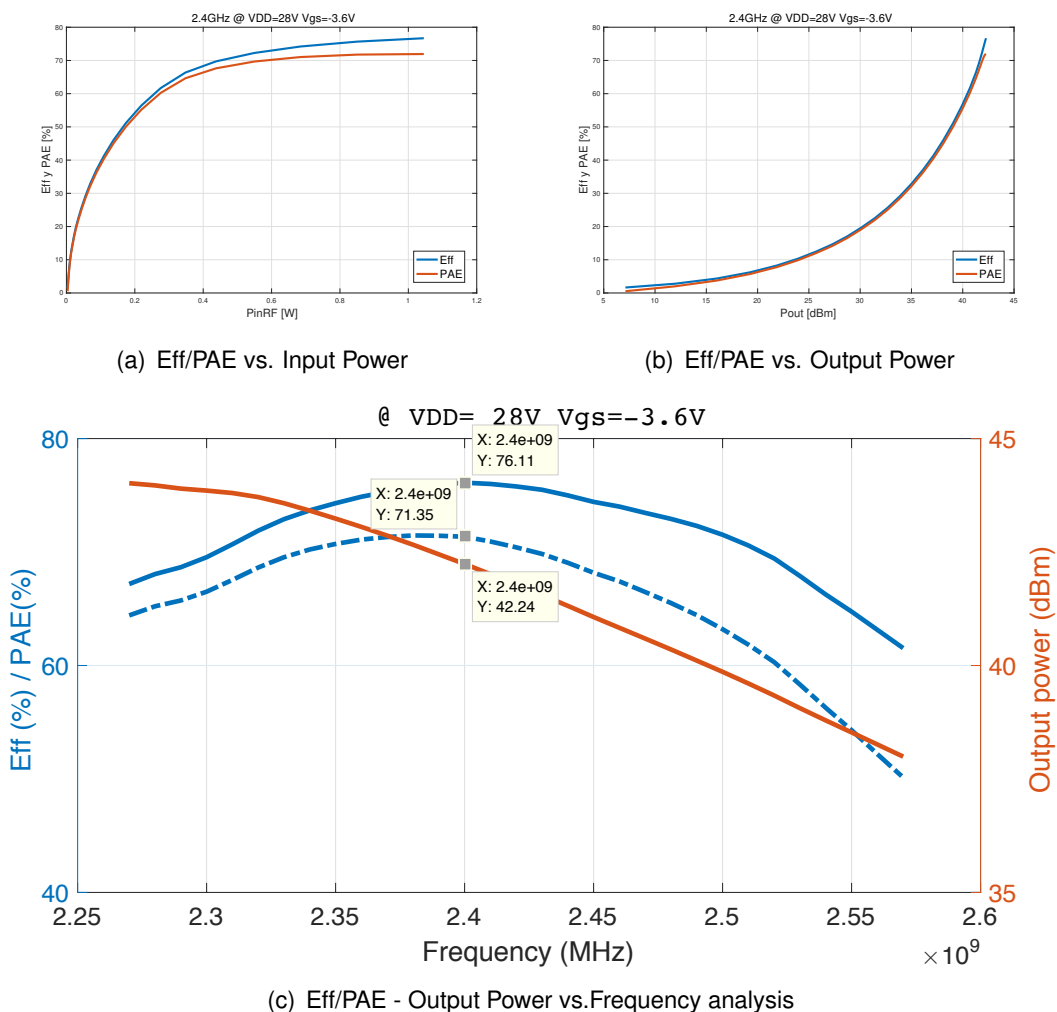(a) Eff/PAE vs. Input Power

(b) Eff/PAE vs. Output Power

(c) Eff/PAE - Output Power vs.Frequency analysis

Figure 4.9: $V_G =$-3,6 V / $V_{ds} =$28 V

Finding a linear operating point

Considering that the final application of the amplifier will include non-constant envelope modulated signals, it becomes necessary to find a more convenient operating point in terms of linearity.

In order to analyze the amplifier behavior, a test is performed sweeping the power input for different gate voltages in a network analyzer, obtaining the flattest curve for $Vg =$-2,9 V as shown in *Figure 4.10*. It must be taken into account that the input power axes reprents the power deliver by the network analyzer. Therefore, an approximately 30 dB gain introduced by the pre-amplifier must be consider.
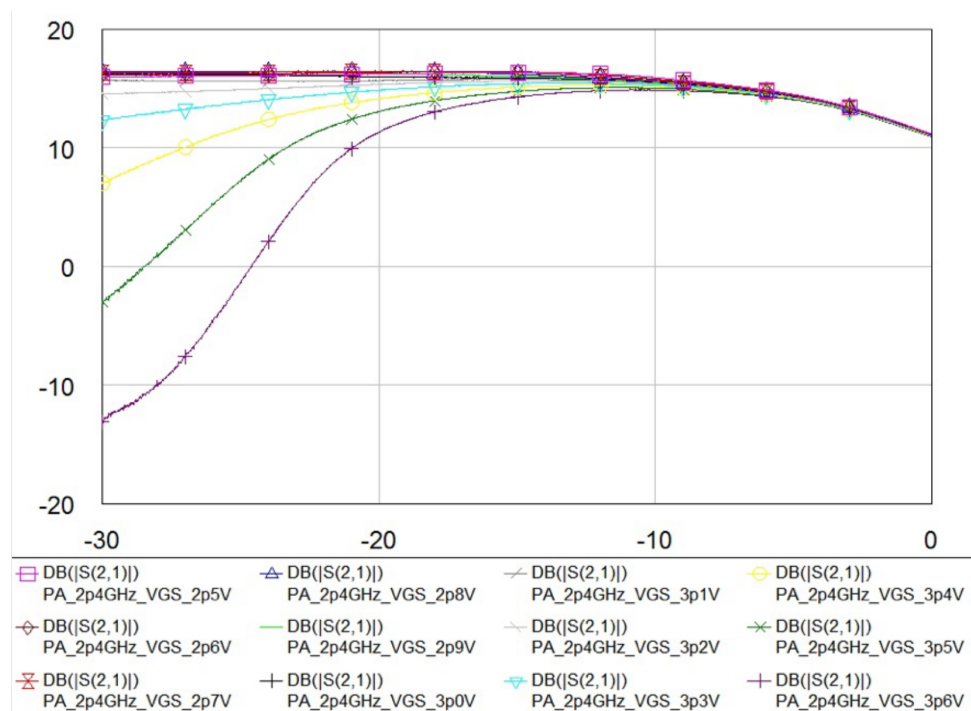
Figure 4.10: Gain vs. Power input for different gate voltage values

The selection of a gate voltage slightly above pinch-off enables us to pass from a gain profile of expansion-compression, with a markedly non-linear response, to a gain profile that shows a softer compression which facilitates the DPD implementation *Figure 4.11*.

Thus, the amplifier changes its operation class, from a switch-mode amplifier to a current-source mode obtaining a higher efficiency performance due to the optimized harmonic terminations than conventional linear operation designs.
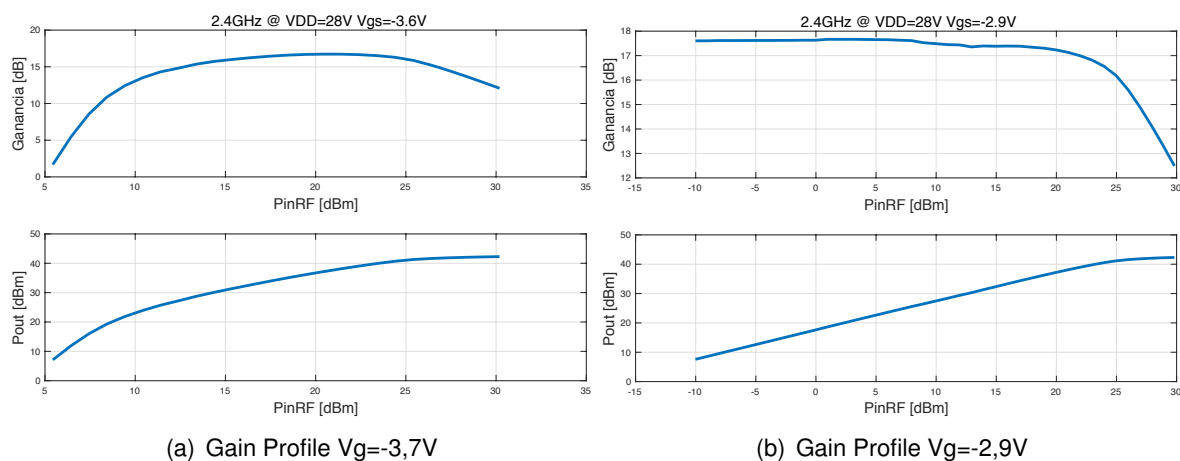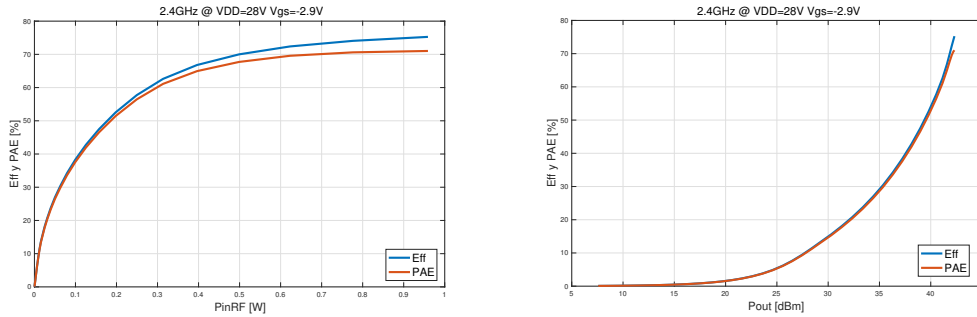

(a) Gain Profile Vg=-3,7V

(b) Gain Profile Vg=-2,9V

Figure 4.11: Gain profile comparison

After this analysis, the characterization measure was repeated for V_G=-2,9 V / V_{ds} =28 V shown in *Figure 4.12*, it can be noted that the efficiency and PAE profile are fairly similar to the one obtained for $V_G = -3,6V$ presenting a low efficiency loss in comparison.

(a) Power input analysis

(b) Power output analysis
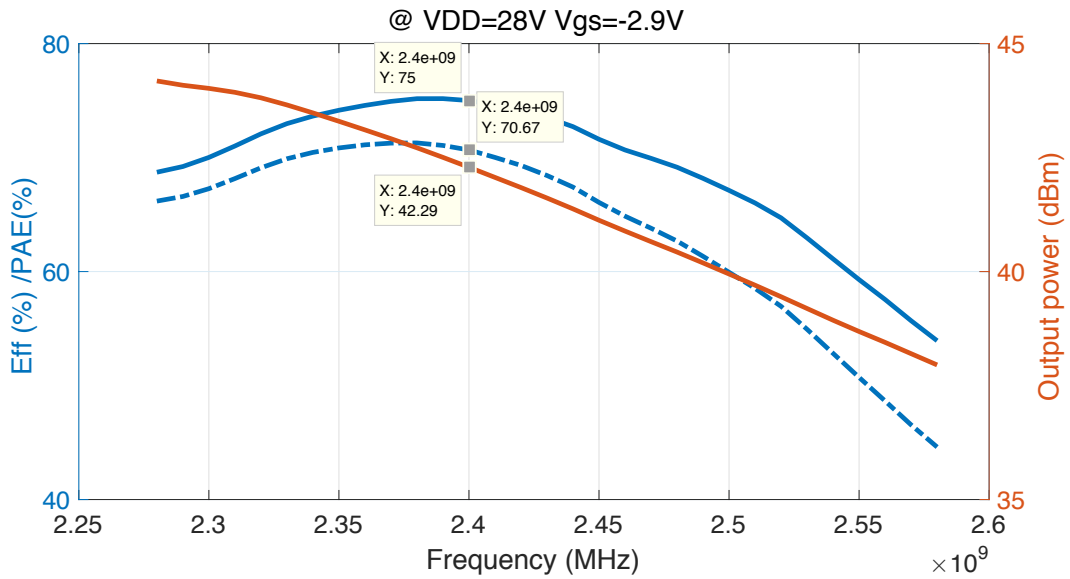
(c) Frequency analysis

Figure 4.12: V_G=-2,9 V / V_{ds} =28 V

To complete the description of the experimental implementarion, the final configuration for the class-E amplifier is shown in *Figure 4.13*.
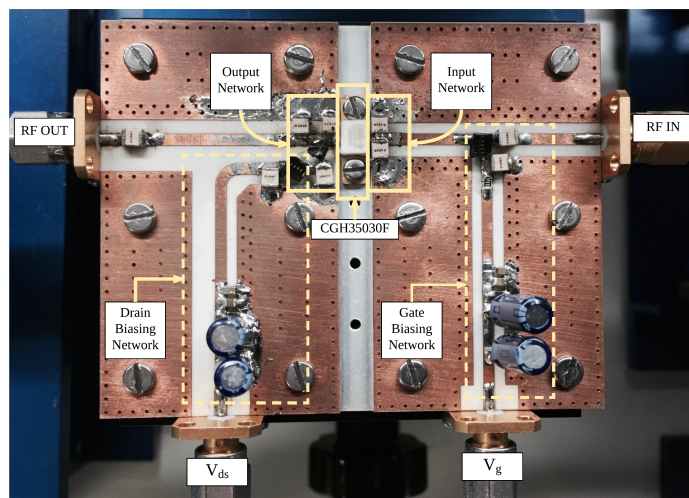

Figure 4.13: Class-E Power Amplifier

Chapter 5

TEST BENCH BASED ON DEVELOPMENT BOARDS

The main objective of this test bench based on development boards is to provide a low-budget solution for the evaluation of digital predistortion implementation in comparison to the use of expensive laboratory instruments.

5.1. Hardware description

The design is focused on generating and capturing the response of a test signal through a Device Under Test (DUT) for digital predistortion implementation.

For this purpose, a test bench employing development boards of Texas Instruments that will be controlled by Matlab is proposed in *Figure 5.1* and described below.

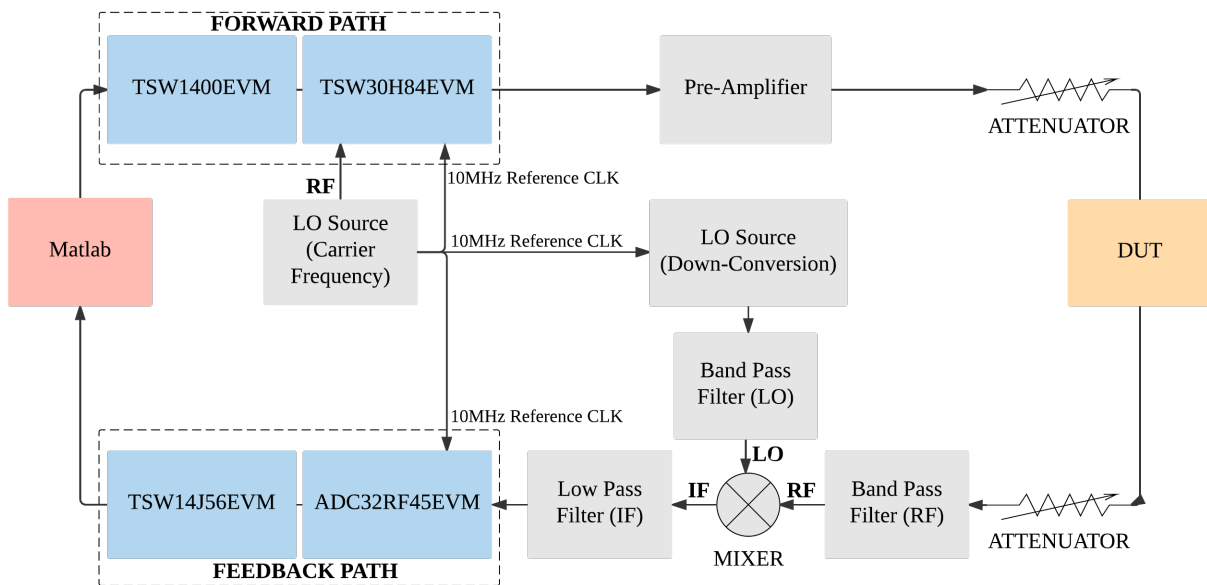Figure 5.1: Test bench configuration proposed

Forward Path

The test signal is generated in Matlab to evaluate the performance of the DUT. After generation, the signal is delivered to the *fordward path (Figure 5.2)*.

The *fordward path* consists in a pattern generator (TSW1400EVM) followed by a digital-to-analog converter and I/Q modulator (TSW30H84EVM), their main features are described in *Table 5.1*.
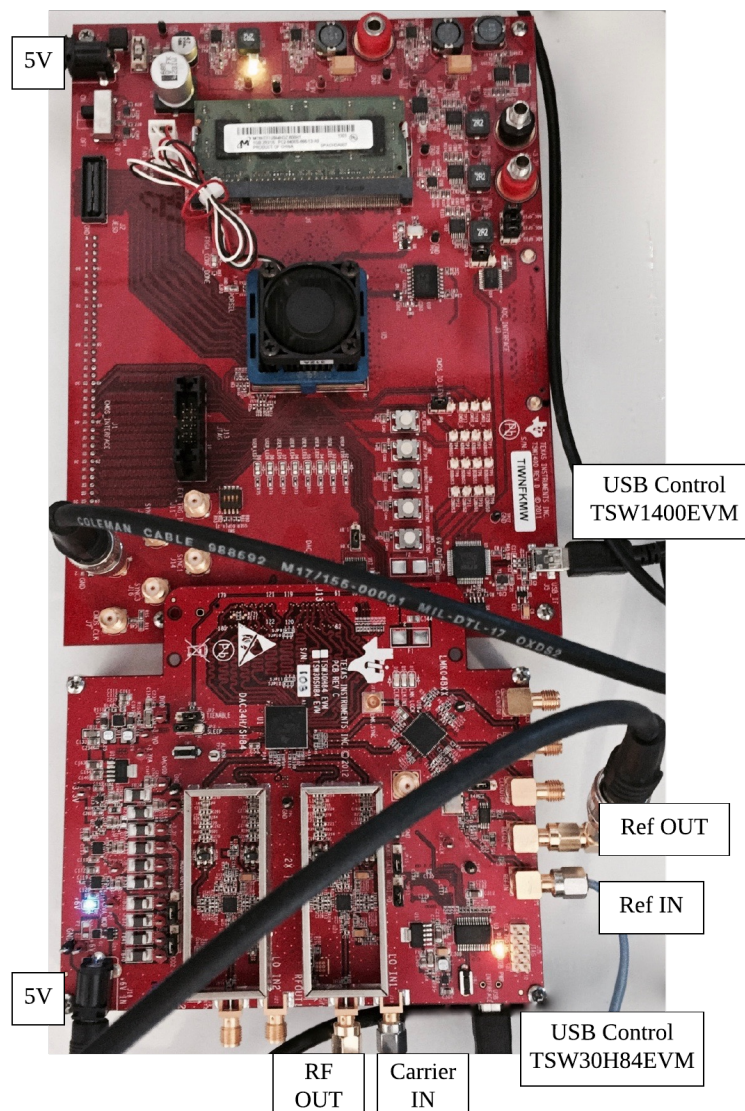
Figure 5.2: TSW30H84EVM + TSW1400EVM

Table 5.1: Forward path [TI16c]

	TI TSW30H84EVM
RF Output Frequency	300-4000 MHz
Output Channels	2
Bits per Channel	16
Max. Data Rate	625 MSa/s (614.4 MSa/s by default)
Pattern Generator support	TI TSW1400EVM - 649.00 USD
Price	499.00 USD

For this evaluation, a carrier signal of 2,4 GHz and 0 dBm amplitude is provided to the I/Q modulator employing an Agilent RF signal generator (N9310A) to enable the up-conversion of the base-band signal generated *(Figure 5.1 - LO source [Carrier Frequency])*.

Pre-Amplifier and DUT

The class-E PA build to work at the operation frequency of 2,4 GHz in *Chapter 4* will be used as a DUT in order to evaluate this test bench.

The power amplifier characterization measures have indicated that an input power of 30 dBm is expected to work at maximum efficiency. In order to comply with this requirement, a pre-amplifier (ZHL-16W-43-S+) has been introduced providing 40 dB of amplification *(Figure 5.1 - Pre-amplifier)*.

Both stages can be adjusted using connectorized attenuators to achieve a certain power condition. Considering the DUT's high output power, a 40 dB attenuation was attached to avoid damaging or saturating the following stages.
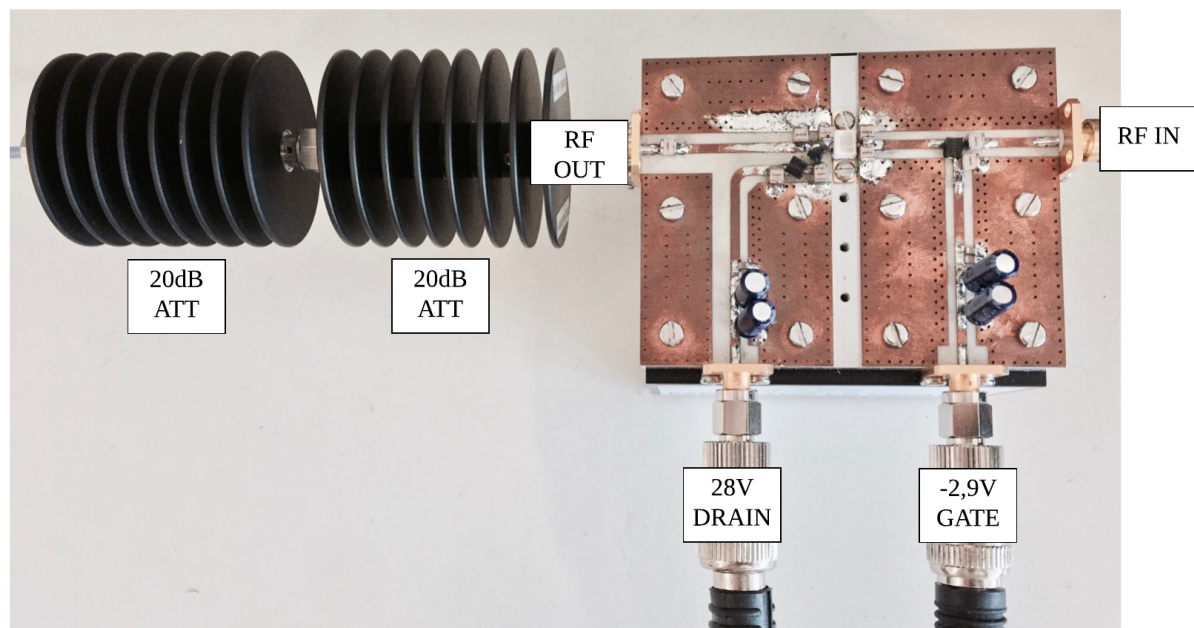

Figure 5.3: DUT+ Attenuators

To finish with, a band-pass filter *(Figure 5.1 - Band Pass Filter [RF])* centered closed to 2,4 GHz was introduced to avoid the undesired effects produced by the harmonics generated due to the amplification.

Analog Down-Conversion

The analog down-conversion block shown in *Figure 5.4* is proposed to convert the RF signal to an intermediate frequency (before acquisition) employing an active mixer (ADL5801EVM).

A standalone LO source (TSW3065EVM) provides a 2 GHz local oscillator. This signal is filtered and attenuated in order to deliver a 0 dBm LO to the mixer *(Figure 5.1 - LO Source [Down Conversion])*.

The Intermediate Frequency (IF) chosen is 400 MHz according to the maximum output frequency allowed by the mixer. This stage is followed by a low-pass filter *(Figure 5.1 - Low Pass Filter [IF])* of 800 MHz cut-off frequency to suppress the upper band conversion.

This evaluation-board LO source eliminates the need of an expensive signal generator providing a cheaper option while maintaining an acceptable performance [TI16b].
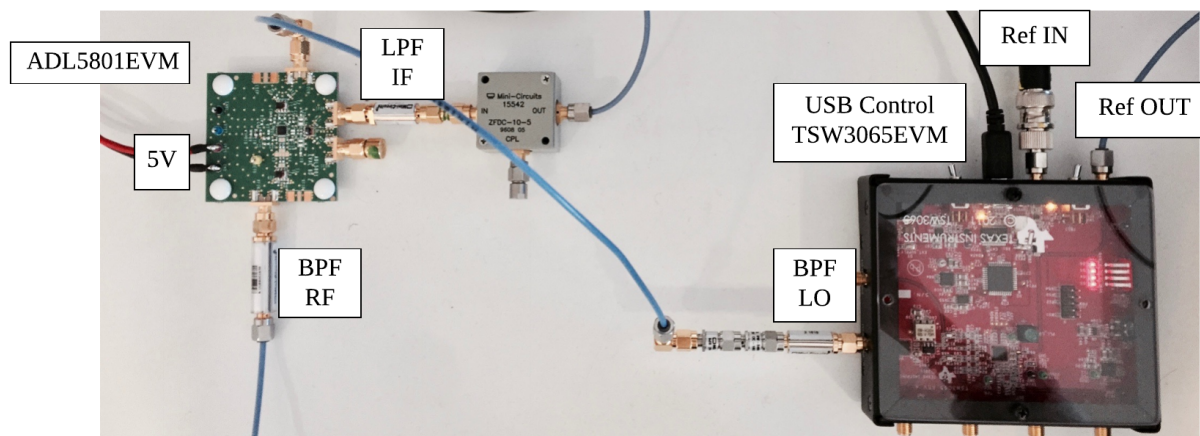

Figure 5.4: Down-Conversion

Feedback Path

The *feedback path* consists in an analog-to-digital converter (ADC32RF45EVM) in combination with a pattern generator (TSW14J56EVM) that allow us to capture the signal for digital processing *(Figure 5.5)*. The main features are described in *Table 5.2*.

Table 5.2: Feedback Path [TI16a]

	TI ADC32RF45EVM
Number of Inputs	2
Input BW	30-3000 MHz
Sampling Rate	3 GSa/sec
Number of bits	14
Pattern Generator support	TI TSW14J56EVM
Price	2499.00 USD

The sampling frequency has been chosen to comply with the Nyquist condition considering that in the *feedback path* we want to observe a bandwidth expansion between three or five times the signal bandwidth due to the PA nonlinear behavior. Moreover, a correct selection of the number of samples must be done.

The sampling frequency and the number of samples were fixed such that the observation time is the same as during generation.

$$t = \frac{Number\ of\ Samples\ [Generation]}{Sampling\ Frequency\ [Generation]} = \frac{61440}{614,4MHz} = 0,1ms \tag{5.1}$$

$$t = \frac{Number\ of\ Samples\ [Acquisition]}{Sampling\ Frequency\ [Acquisition]} = \frac{245760}{2457,6MHz} = 0,1ms \tag{5.2}$$
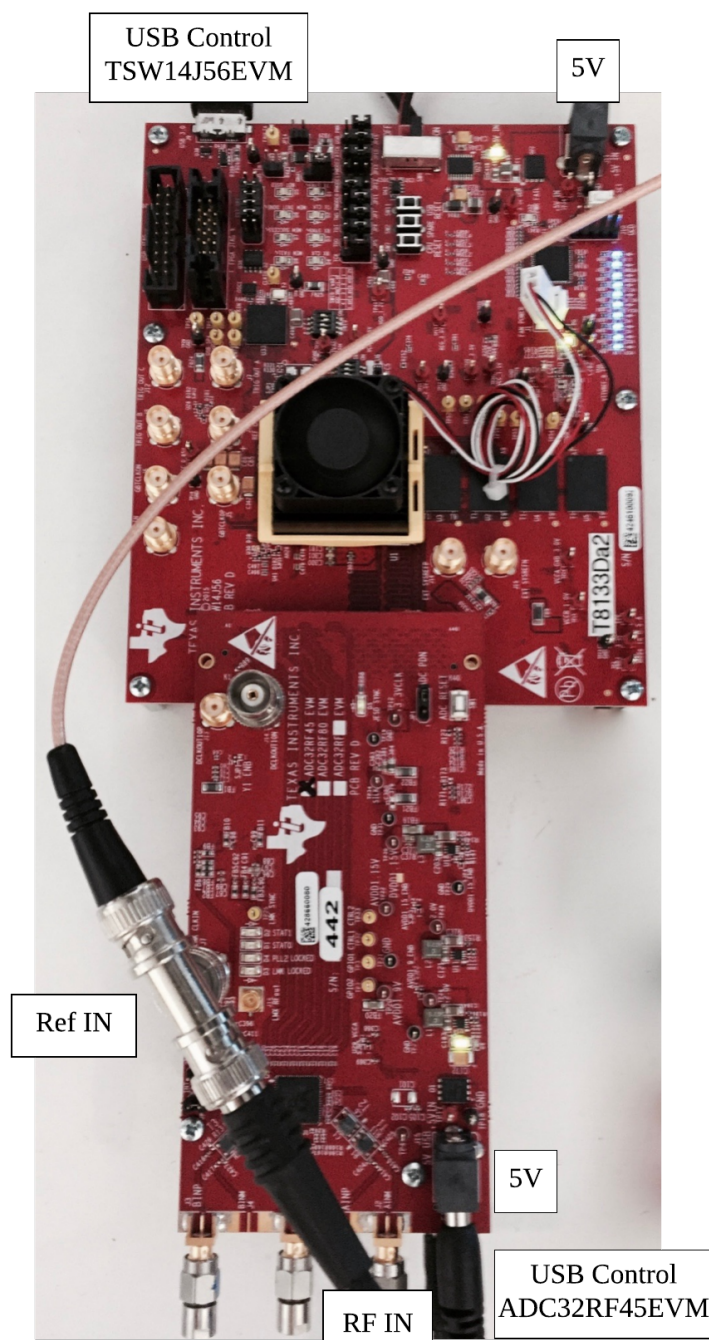
Figure 5.5: ADC32RF45EVM +TI TSW14J56EVM

Synchronism and calibration

An important consideration regarding synchronism is taken into account in order to have the best alignment between the *forward* and *feedback path*.

A 10 MHz reference signal is taken from the RF signal generator and delivered to the standalone LO source. Then, the input references for the ADC and the DAC are obtained such that the output reference of a previous stage is connected to the input reference of a next stage.

In order to be able to perform power measurements based on the acquisition file, it is necessary to evaluate the attenuation introduced by the ADC development board, for this task a signal of 0 dBm is introduced to obtain an experimental compensation value that will be used as a fixed

attenuation value for the following measurements.

On the other hand, the total attenuation introduced by the test bench after the DUT is measured in order to obtain its output power.

To complete this description, the hardware implementation of the *Figure 5.1 schematic* is shown in the following picture. This configuration will be employed for all the measurements proposed across this project.
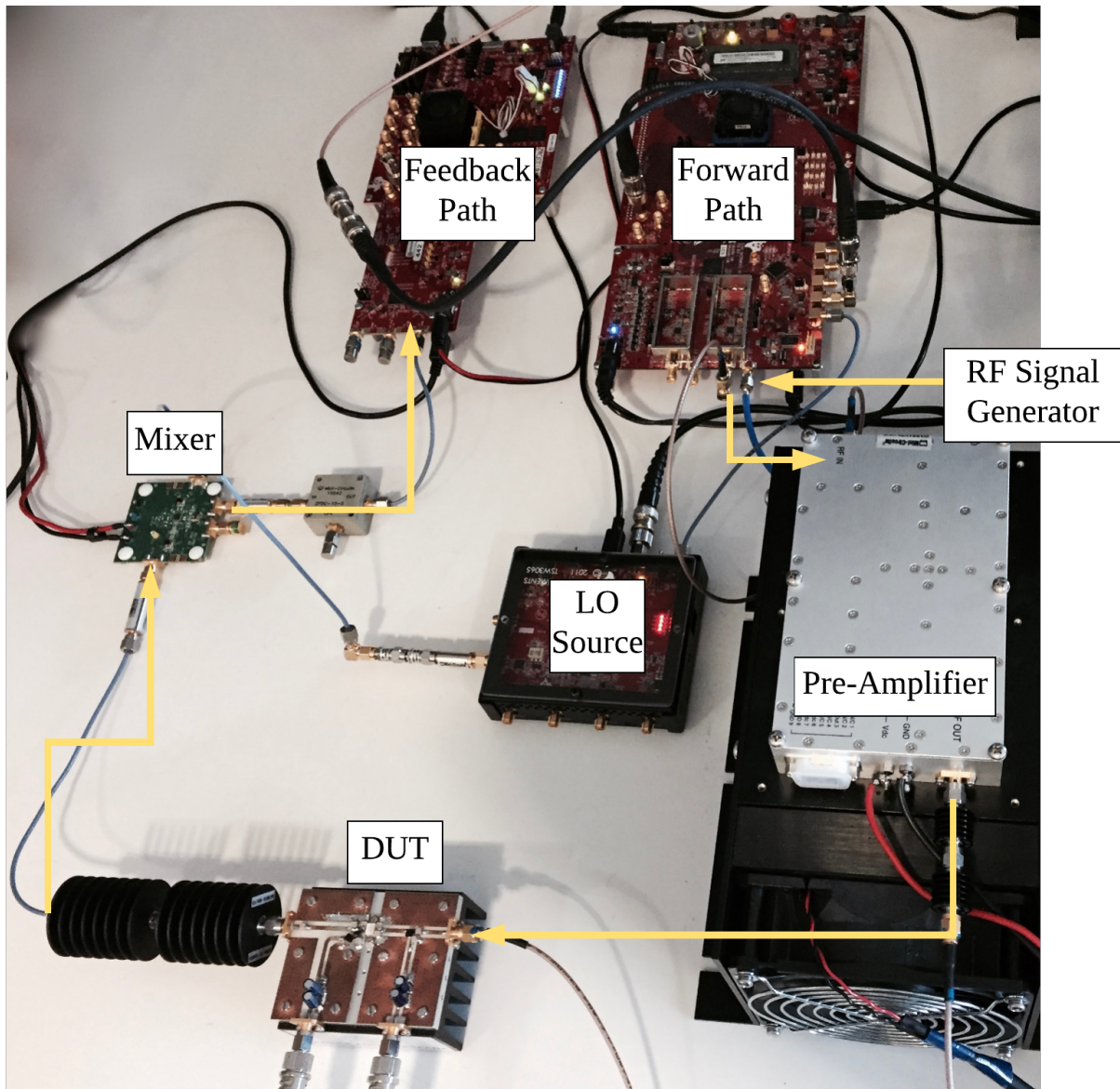

Figure 5.6: Final test bench configuration

5.2. Software description

Although this test bench will be controlled by Matlab during the measurements, before starting it is necessary to configure some parameters manually.

The TSW3084EVM needs to be set up employing a configuration file that includes the *DAC Gain* as well as the *Offset Adjustment* found during calibration.
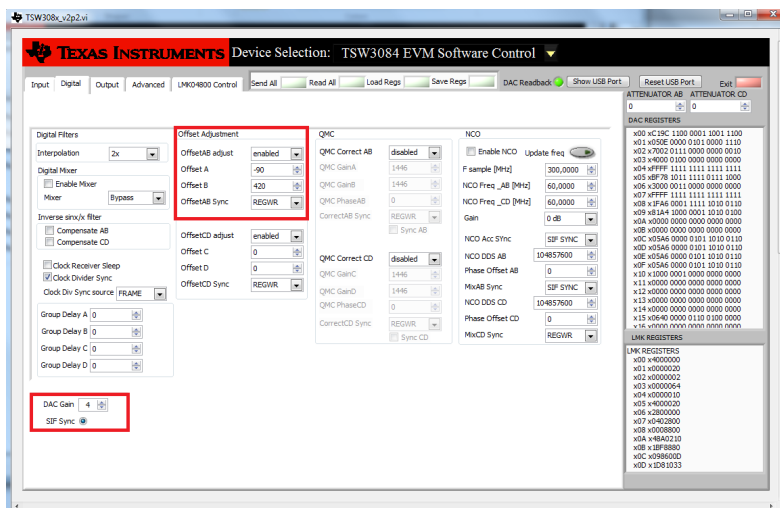
Figure 5.7: TSW3084 EVM Software Control

To enable the down-conversion, the standalone LO source is configured by the TSW3065 GUI, which allow us to program frequencies ranging from 300 MHz to 4,8 GHz and the output power with a combination of an amplifier and programmable attenuator. For this configuration, a 2 GHz local oscillator without attenuation is employed.

For acquisition, it is required to load the configuration files that enables the ADC to work according to the frequency sample internal clock chosen and the number of bits desired employing the interface software High Speed Data Converter Pro (HSDC Pro).

Figure 5.8: ADC32RFxx EVM revD GUI

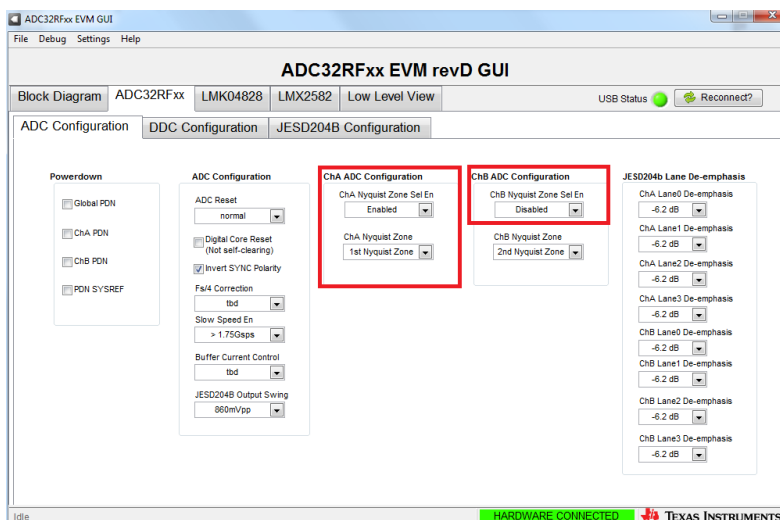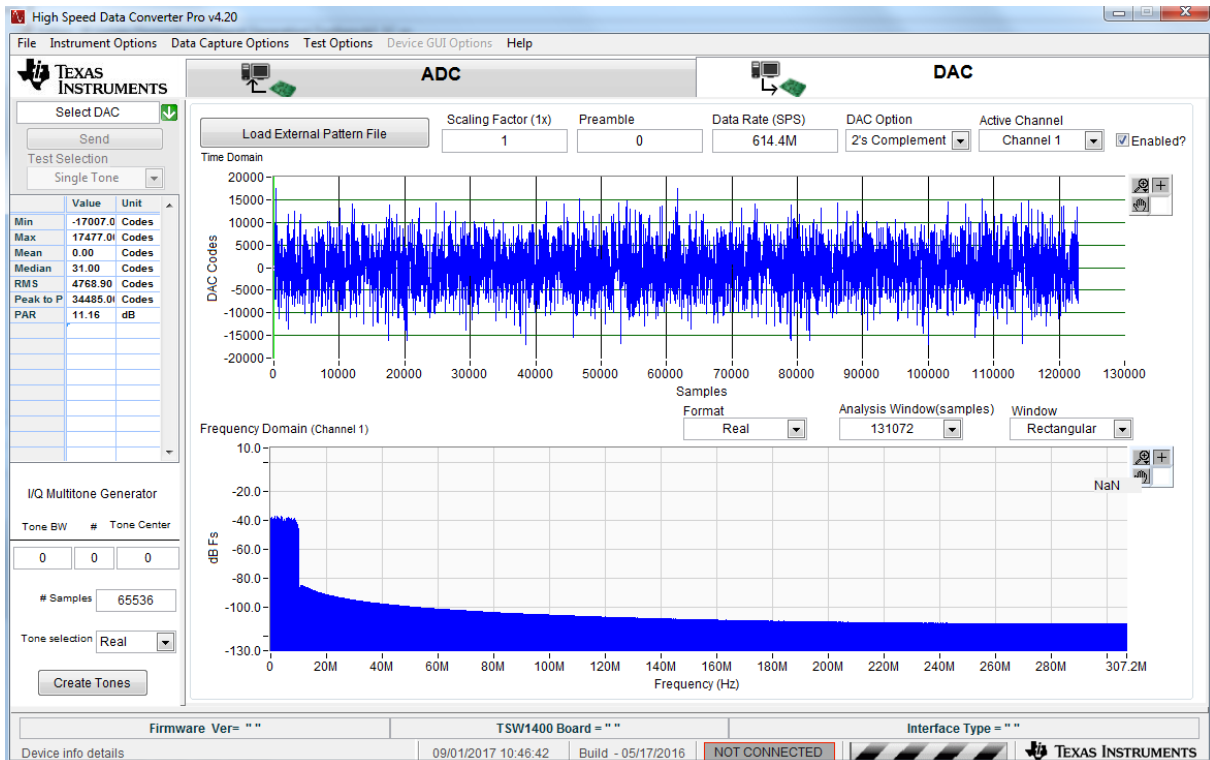In order to be able to control the evaluation boards, the manufacture provides the libraries and examples needed to call the interface software from Matlab, whence the GUI needs to remain open both for sending and capturing signal.

(a) Sending
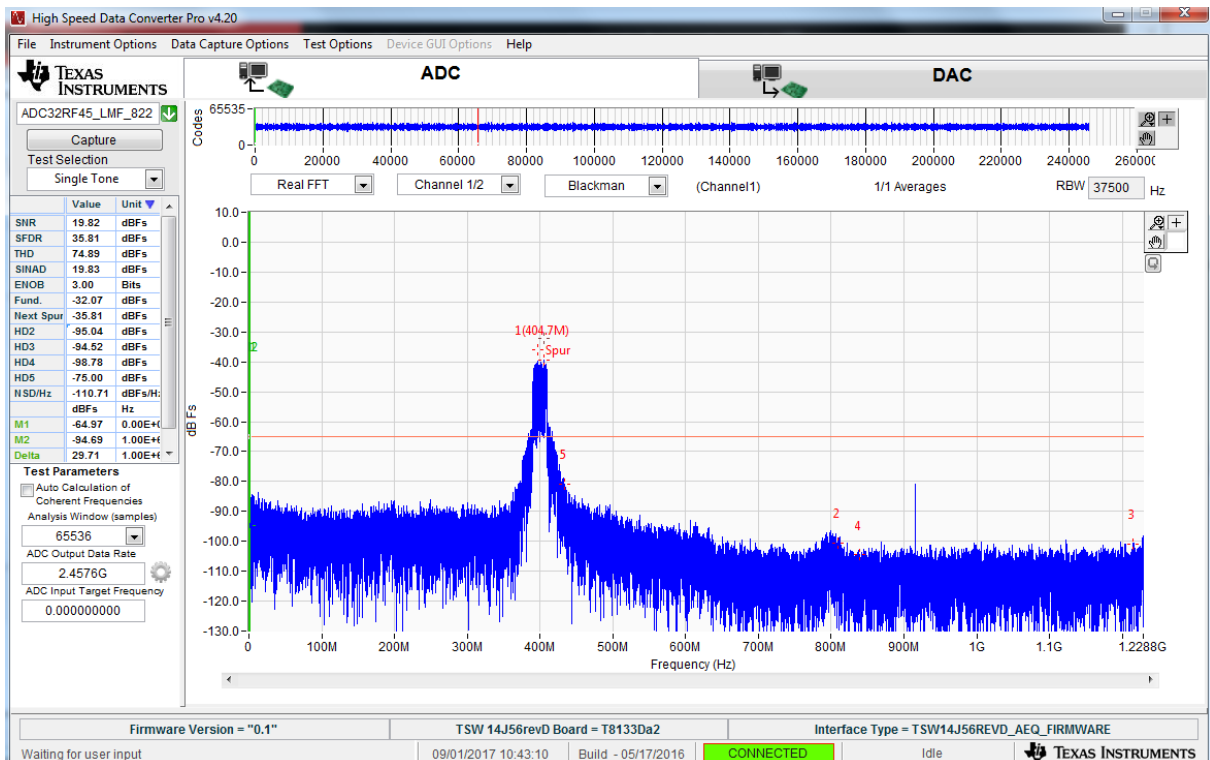
(b) Capturing

Figure 5.9: High Speed Data Converter Pro v4.2

5.3. Matlab implementation

A general flowchart of the signal generation, linearization and adaptation of the DPD coefficients is shown in *Figure 5.10* describing the functions that are carried out across each iteration.
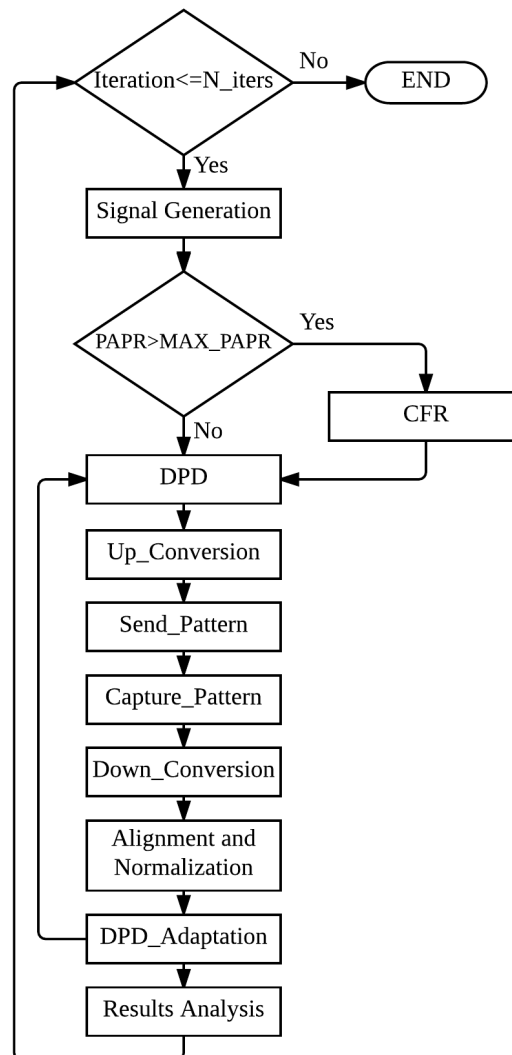
Figure 5.10: Direct Learning DPD Implementation Algorithm

To support this project, Matlab is used as a fundamental tool that offers an Integrated Development Environment (IDE) that allow us to work with matrix manipulation, data and function representation, algorithm implementation and communication with hardware devices.

The algorithm proposes the implementation of the direct learning DPD technique introduced in *Subsection 3.2.2.* for parameter estimation.

Considering the large envelope fluctuations commonly found in signals that implement spectrally efficient modulation techniques based on multicarrier signals, the first step consist in analyzing the resulting PAPR of the test signal generated for each iteration.

We propose to set a maximum PAPR target and the implementation of the CFR technique proposed in *Subsection 3.3.* for the cases that exceed this condition.

The impact of this peak cancellation technique must be taken into account in terms of signal degradation and will be evaluated across the experimental measurements.

In order to analyze the DPD implementation and reference the measurements, *Figure 5.11* details the variables employed.
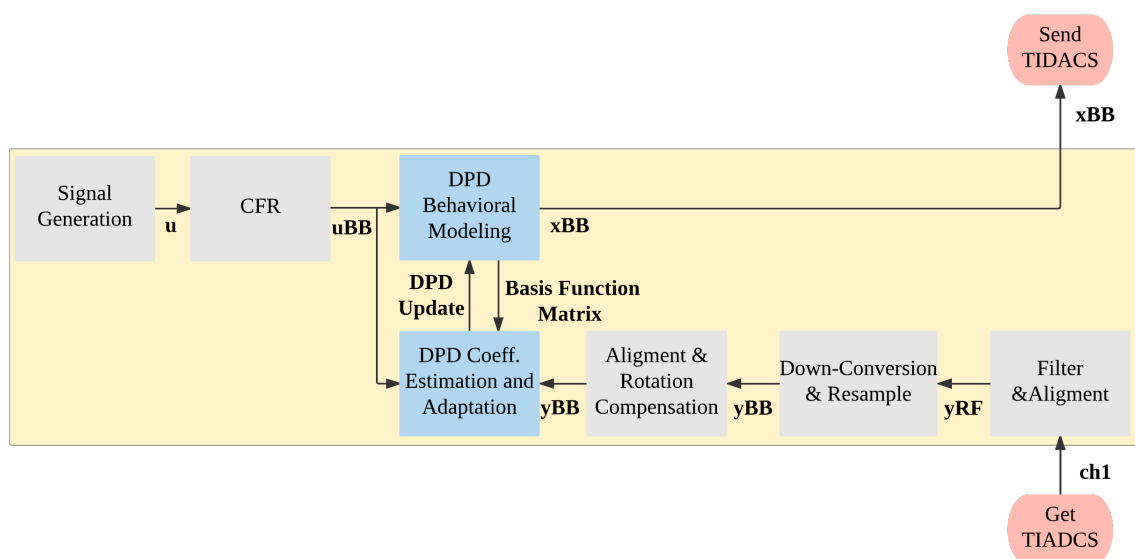
Figure 5.11: DPD algorithm and variables definition

We consider u the test signal generated for each iteration and uBB the clipped signal after the CFR implementation.

The feedback path return us the acquisition file $ch1$ executing the *Get TIADCS* function, after the first alignment and filtering, this signal become yRF. Furthermore, after the down-conversion and resample, the restored base band signal is called yBB. The final step consists in a second more accurate alignment and a rotation compensation.

The *DPD coefficients estimation and adaptation block* iteratively calculates the DPD coefficients employing the *basis function matrix* obtained in the *DPD behavioral modeling block*, minimizing the difference between uBB and yBB as explained in *subsection 3.2.2.* for the *Direct Learning* implementation.

Therefore, the DPD coefficients are sent to the *DPD behavioral modeling block*, which calculates the resulting predistorted signal xBB that that will be sent to the *forward path* employing the *Send TIDACS* function.

Chapter 6

EXPERIMENTAL CAMPAIGN

The test bench described in *Chapter 5* has been built and configured for this experimental campaign.

Figure 6.1: Test bench configuration for experimental campaign
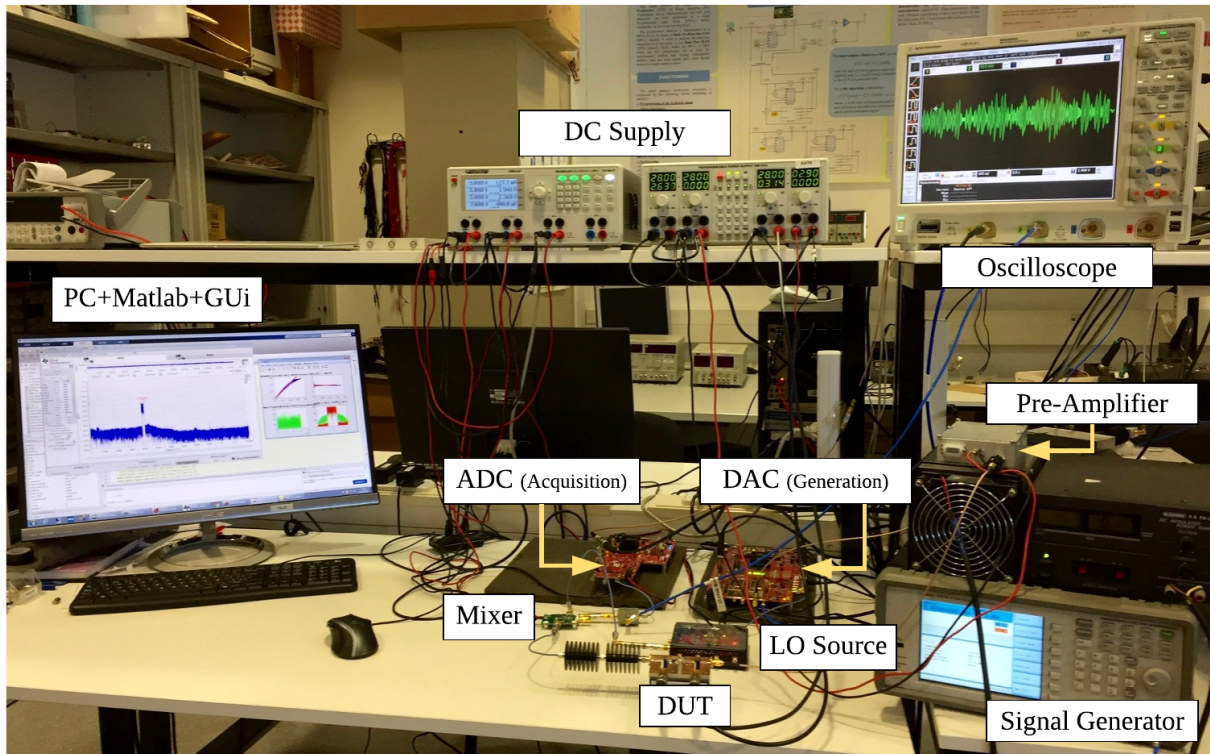
6.1.   Test signal

We consider a LTE-like signal of 20 MHz bandwidth, employing Quadrature Amplitude Modulation (QAM) and Orthogonal Frequency-Division Multiplexing (OFDM).

The OFDM consists in encoding digital data on multiple frequency carriers, in this case a test signal of 1550 useful active subcarriers has been consider *(Figure 6.2)*.
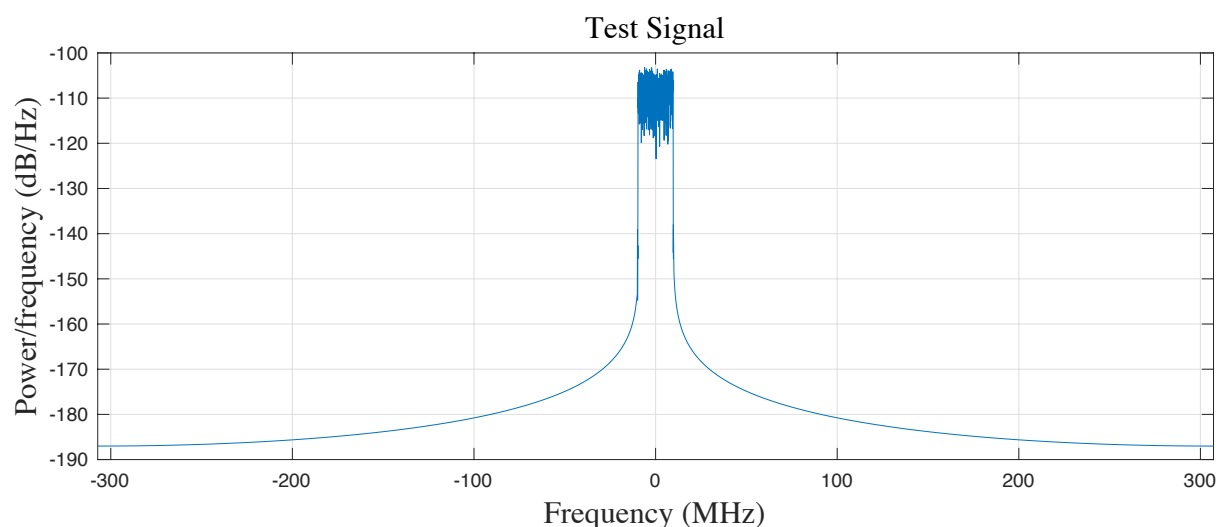
Figure 6.2: Base-Band test signal

6.2.   Test bench validation

In order to validate the test bench, it has been indispensable to check that each step introduced does not affect the linearity of the setup proposed.

The DAC output level has been chosen to avoid saturation (Gain=4), for this condition a gain compensation between I/Q channels output gain has been calibrated with the help of a spectrum analyzer in order to decrease as much as possible the carrier leakage. The pre-amplifier has been previously measured to check that it does not introduce significant nonlinearities and the nominal configuration of the mixer has been changed in order to increase the input power compression level, that allows us to work with a higher power signal that represents a benefit to take advantage of the dynamic range of the ADC.

To evaluate the performance, a *through* measurement is evaluated bypassing the DUT and employing a variable attenuation between the driver and the mixer to reproduce the same mixer input power that is observed with the DUT included. The test signal proposed in *Subsection 6.1.* is configured for 64QAM while a PAPR target of 8 dB is set.

Taking into account *Figure 5.11*, the NMSE is evaluated considering both u and uBB; likewise, the EVM is evaluated for both uBB and yBB signals in order to differentiate between the degradation on the signal quality produced by the CFR technique and the one introduced by the test bench. The ACPR measurement allow us to know if we are meeting standard requirement.

Table 6.1: test bench validation [64QAM - PAPR target=8 dB (CFR) - GMP (168 coefficients)

	Mean Power [dBm]	NMSE (u) [dB]	NMSE (uBB) [dB]	ACPR [dB]	EVM (uBB) [%]	EVM (yBB) [%]
Through	36,3	-33,56	-33,56	-45,7	0,25	1,29
With CFR+DPD	36,03	-31,38	-38,50	-50,81	1,05	1,27

As can be observed in *Table 6.1*, while the *through* measurement without linearization techniques is enough to cover the specifications required (-45 dB of ACPR), the implementation of both CFR and DPD technique shows a significant improvement in the ACPR ratio. Then, it can be considered that the nonlinearities introduced by the test bench are correctly modeled and reduced.

6.3. Experimental results

Considering the final test bench configuration shown in *Figure 5.6* and the variables adopted in *Figure 5.11*, the test signal proposed in *Subsection 6.1.* will be analyzed for different modulation schemes, employing different linearization techniques and DPD behavioral models.

Analysis of linearization techniques

In order to study the effect of the linearization techniques described in *Chapter 3*, the performances with and without linearization techniques are compared in *Table 6.2* looking at the same mean power output level.

Table 6.2: Linearization techniques analysis [64QAM - PAPR Target=8 dB (<15% PAPR reduction with CFR) - GMP (168 coefficients)]

Techniques	Mean Power [dBm]	NMSE (u) [dB]	ACPR [dB]	Efficiency [%]	EVM (yBB) [%]
Back-off	27,54	-31,02	-40,58	12,52	1,36
Without CFR / Without DPD	36,35	-18,35	-26,02	49,34	4,68
With CFR / Without DPD	36,60	-18,41	-26,28	48,93	4,72
Without CFR / With DPD	36,60	-26,09	-37,4	50,19	1,48
With CFR / With DPD	36,56	-30,34	-45,26	49,81	1,43

By analyzing the data obtained, it can be noted:

● It is not possible to meet the requirement of -45 dB of ACPR without the implementation of linearization techniques for this power output level.

● For the back-off test, the procedure differs from the rest since we were trying to achieve the best ACPR possible without linearization techniques. Hereby, it is necessary to decrease the Mean Power level, in consequence a low efficiency result is obtained (12,52%).

● The implementation of CFR technique only does not prove to be effective while the implementation of the DPD technique shows a great improvement in the figures of merit. However, it is not enough to achieve the -45 dB of ACPR for the output power chosen.

● Lastly, the combination between CFR and DPD techniques shows the best results in terms of linearity almost reaching a 50% of power efficiency.

After analyzing the benefits of the CFR technique, we have studied the degradation on the signal quality produced by the PAPR reduction for an ACPR below -45 dB in *Table 6.3*.

Table 6.3: CFR Analysis [64QAM - GMP (168 coefficients)]

PAPR Target [dB]	NMSE (u) [dB]	NMSE (uBB) [dB]	ACPR [dB]	EVM (uBB) [%]	EVM (yBB) [%]
4	-13,29	-20,34	-45,44	9,6	9,73
5	-17,6	-24,37	-45,44	5,86	5,99
6	-21,2	-28,46	-45,37	3,80	4,02
7	-25,79	-3319	-45,30	2,10	2,39
8	-30,24	-37,25	-45,26	1,05	1,43
9	-33,4	-40,81	-45,46	0,52	0,96
10	-34,66	-41,39	-45,42	0,27	0,8
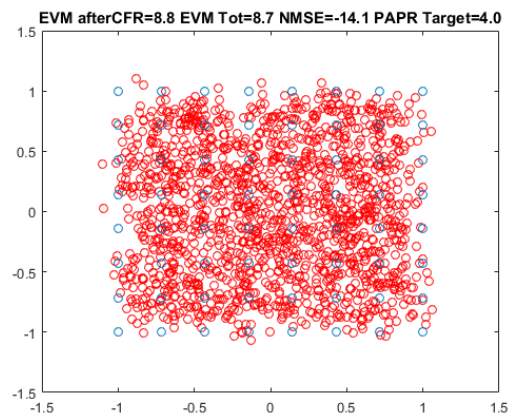
(a) PAPR Target: 4 dB
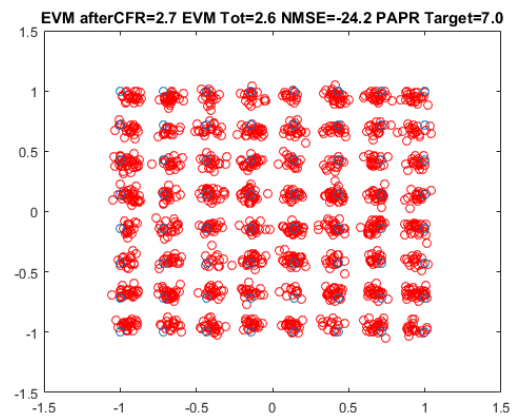
(b) PAPR Target: 6 dB
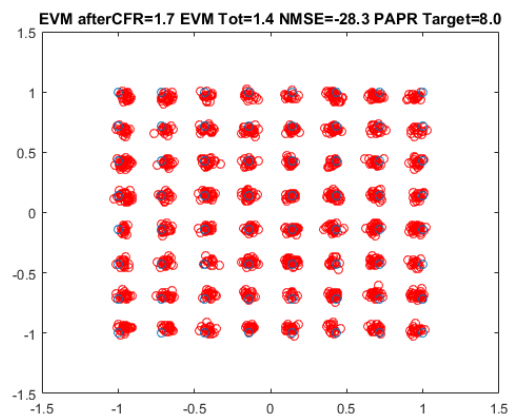
(c) PAPR Target: 7 dB
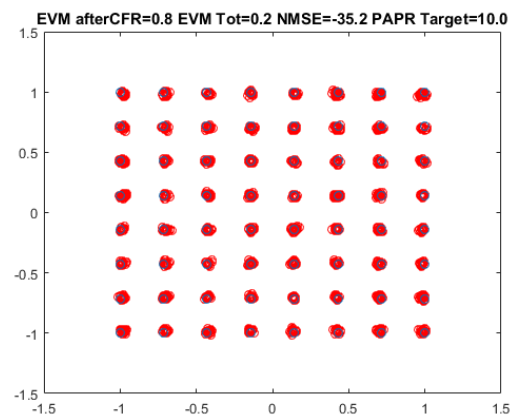
(d) PAPR Target: 10 dB

Figure 6.3: PAPR Reduction

We can conclude that:

- The higher PAPR reduction, as a consequence of the decrease of the PAPR target, the worse EVM and the NMSE.

- It should be taken into account the regulations according to the modulation scheme employed. For instance, the LTE standard for 64QAM allow a EVM degradation up to 9%. Then, the results obtain for a PAPR target of 4 dB are not acceptable.

We have also evaluated the performance for different modulation orders and DPD models behavior.

Table 6.4: Modulation analysis [PAPR Target=8 dB - GMP (168 coefficients)]

| Modulation	Power Mean [dBm]	NMSE (u) [dB]	NMSE (uBB) [dB]	ACPR [dB]	Efficiency [%]	EVM (uBB) [%]	EVM (yBB) [%]
16 QAM	36,60	-30,10	-37,17	-45,46	50,33	1,21	1,61
64 QAM	36,47	-30,55	-37,51	-45,49	49,11	1,05	1,41
256 QAM	36,58	-31,12	-38,24	-45,48	50,30	0,83	1,18

It should be noted that the number of coefficients and memory taps employed in the DPD behavioral models described in *subsection 3.2.1.* were not optimized. The order selection was done through trial-and-error iterations such that the convergence of the model is observed near the fifth iteration.

In order to obtain an optimized implementation there are *Model Order Reduction* techniques like those compared in [GMW$^+$16].

Table 6.5: DPD behavioral model analysis [64 QAM - MP (64 coefficients) - GMP (168 coefficients)]

Model Behavior	Power Mean [dBm]	NMSE (u) [dB]	NMSE (uBB) [dB]	ACPR [dB]	Efficiency [%]	EVM (uBB) [%]	EVM (yBB) [%]
Memory Polinomial	36,42	-30,43	-37,63	-45,84	48,9	1,05	1,41
General Memory Polinomial	36,57	-30,27	-37,57	-45,16	49,88	1,05	1,43

Without observing significant variations in NMSE, ACPR, EVM and efficiency, we can conclude that the DPD implementation proposed is fairly independent of the modulation type and the DPD behavioral model chosen.

Performance analysis for maximum efficiency

The following study cases are focused on the trade-off between linearity and efficiency with the purpose of obtaining a relation between the NMSE, ACPR and efficiency and different PAPR target values considering the maximum efficiency that can be reach without neglecting the -45 dB ACPR requirement.

The test signal proposed in *Subsection 6.1.* is configured for 64QAM while a GMP (168 coefficients) is chosen for the DPD implementation.

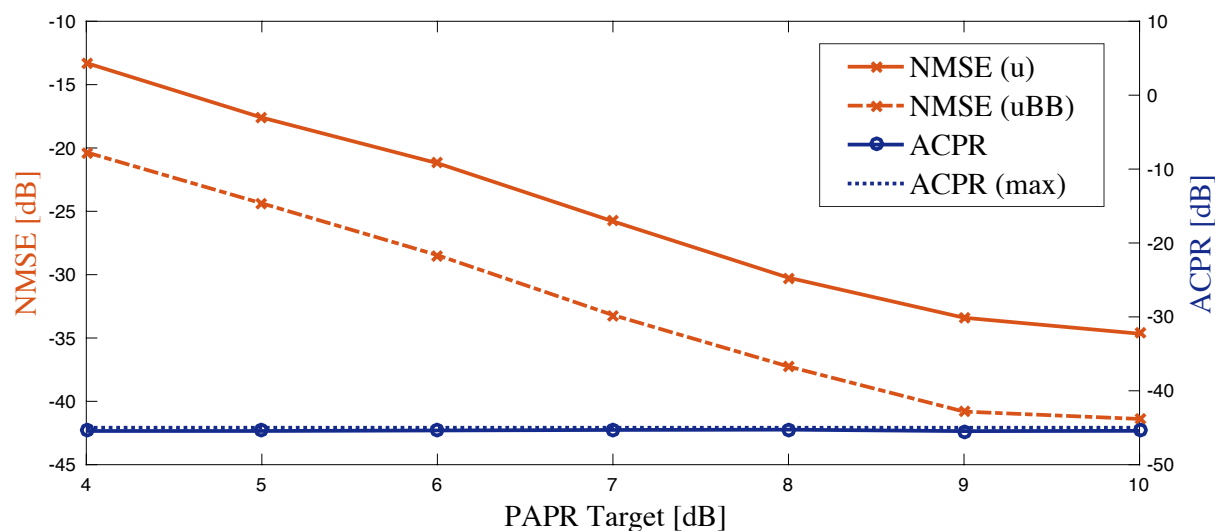The NMSE evaluated for both *u* and *uBB (Figure 5.11).*

Figure 6.4: NMSE/ACPR vs PAPR [64 QAM - GMP (168 coefficients)]

From *Figure 6.4* we observe that:

- As the PAPR is reduced, a degradation in the NMSE value is observed. This result is expected taking into account that the parameter most affected by the clipping signal is related to the in-band distortion, then the higher the PAPR reduction the worse NMSE.

- On the other hand, it can be noted that the additional degradation of the NMSE due to the DUT is more or less constant across the different PAPR target values.

For the same conditions, the relationship between Mean Power and efficiency has been studied in *Figure 6.5*:

- In order to meet the requirement of -45 dB ACPR, the Mean Power decreases with the increment of the PAPR target. As a consequence, the efficiency also decreases.

- With efficiency values ranging from 40 to 60%. It can be said that this behavior meets and even surpasses the specifications of commercial devices, specially for the lower PAPR values.
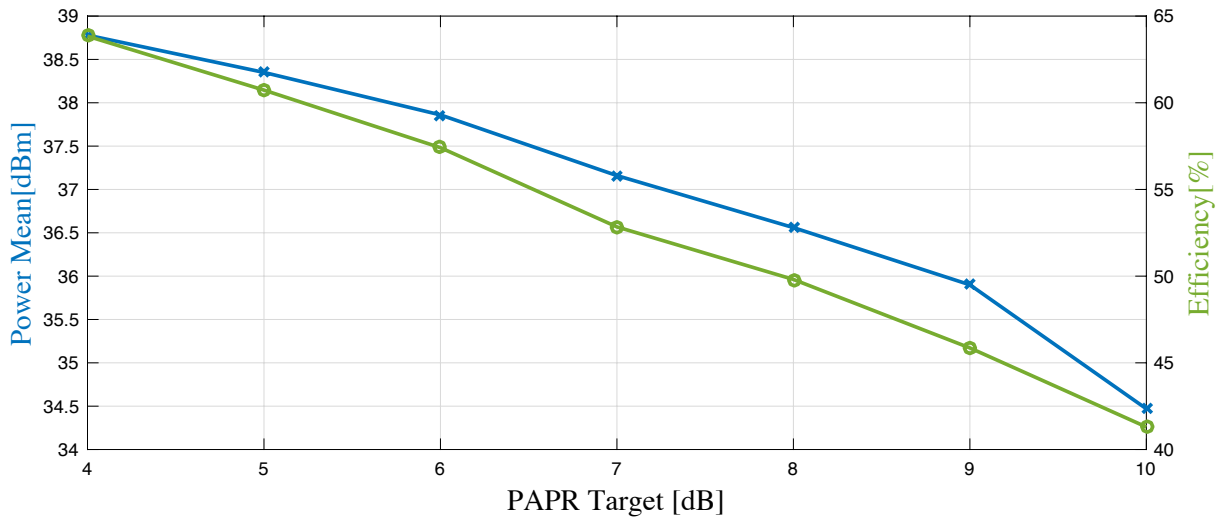
Figure 6.5: Mean Power/Efficiency vs PAPR [64 QAM - GMP (168 coefficients)]

To finish with the characterization of the performance analysis for maximum efficiency, the EVM degradation analysis aimed to compare the relation between the NMSE and the EVM caused by the PAPR reduction.
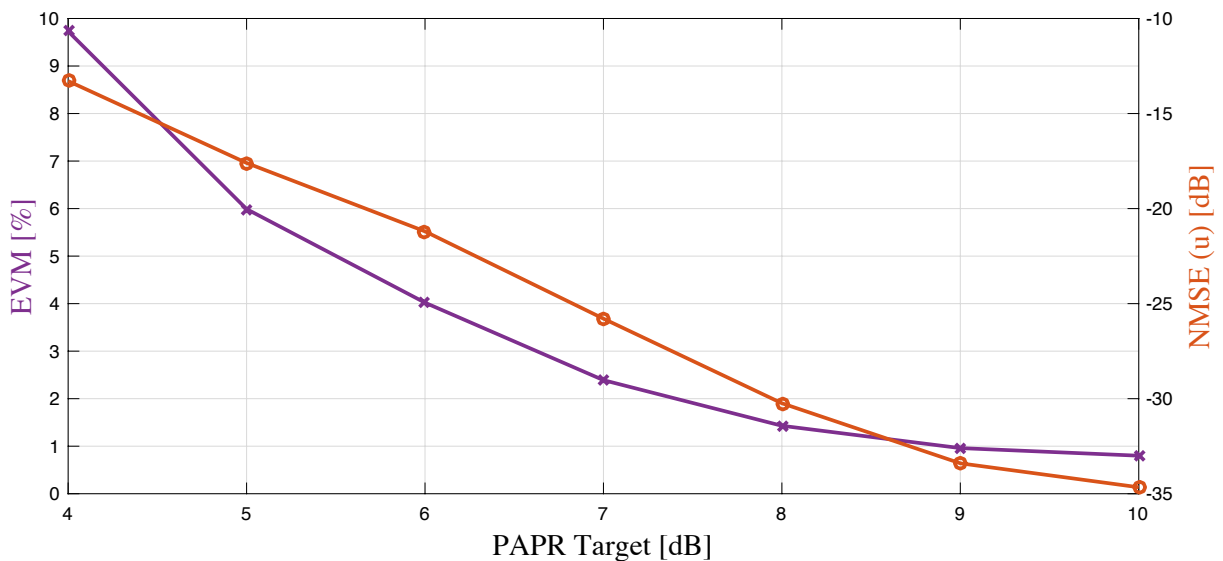
Figure 6.6: EVM/NMSE vs PAPR [64 QAM - GMP (168 coefficients)]

From *Figure 6.6*, we can conclude that:

- Both NMSE and EVM have worsened with the decrease of the PAPR target.

- This relationship allow us to analyze if the results obtained are compliant with the standards requirements in terms of signal degradation (EVM).

- Considering that for a 64QAM the maximum EVM allowed is 9%, this measurement pass the test for all the PAPR target values except for the 4 dB that implicates a PAPR reduction mean about 55%.

Performance analysis for fixed power level

For this measurement, we focus on analyzing the response for different PAPR target values fixing the Mean Power output level close to 36 dBm.

The test signal proposed in *Subsection 6.1.* is configured for 64QAM while a GMP (168 coefficients) is chosen for the DPD implementation.

The NMSE is evaluated for the original u signal while the EVM is calculated with yBB *(Figure 5.11)* in order to analyze the total distortion introduced by the test bench.
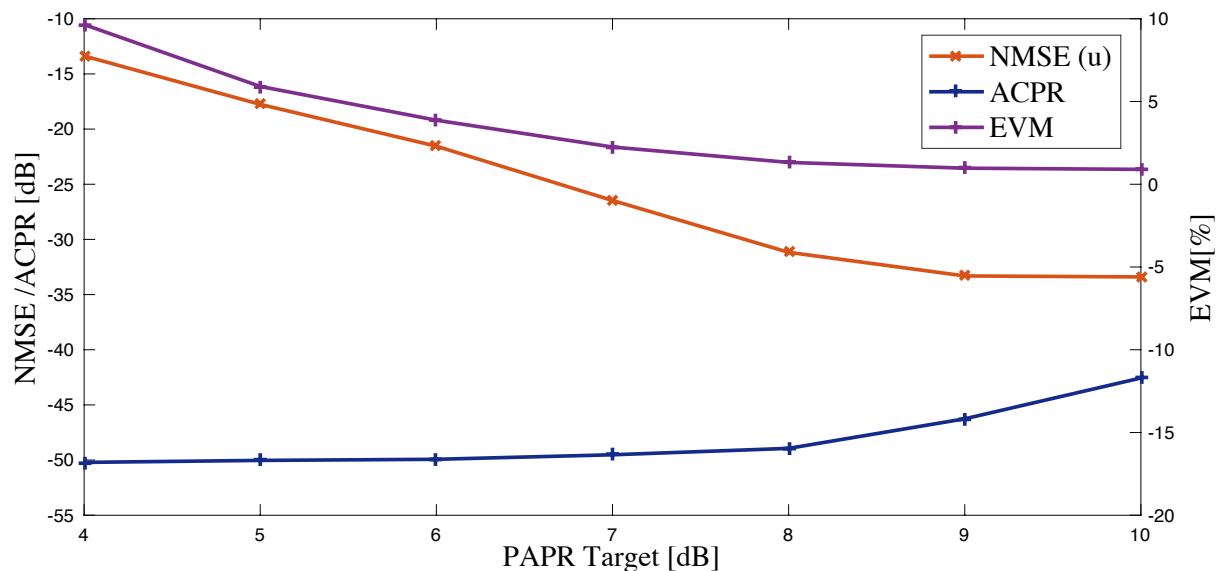
Figure 6.7: NMSE/ACPR vs PAPR [64 QAM - GMP (168 coefficients)]

After analyzing the results obtained in *Figure 6.7* we found that:

- It was difficult to achieve the same output power level for each PAPR target since the DPD algorithm employed is not so accurate. However, a power range with variations up to 1dB are considered.

- The efficiency takes values between 44,5 to 48,8%. Considering the fluctuations in the output power, it can not be distinguish a trend.

- It can be observed a marked improvement in the ACPR with the decrease of the PAPR target. On the other hand, both NMSE and EVM tend to worsen with the increase of the PAPR reduction.

Final statement

To conclude, *Figure 6.8* shown one of the most representative measurements that has been chosen from the *Performance Analysis for Maximum Efficiency*.

Figure 6.8: Analysis for maximum efficiency [64 QAM - PAPR Target=8 dB (CFR) - GMP (168 coefficients)]

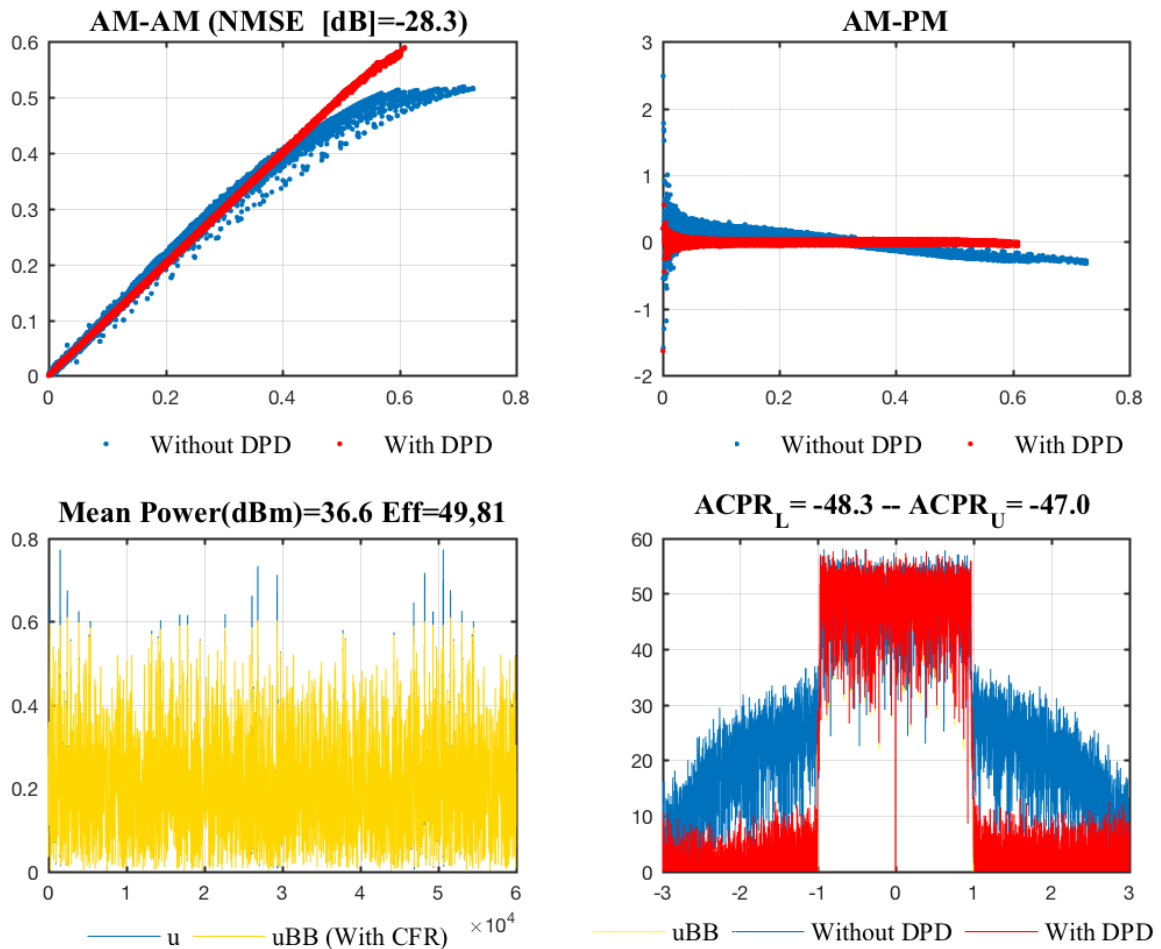It can be noted the impact of the implementation of linearization methods, including both CFR and DPD technique. These methodologies allow us to obtain an efficiency around 50% without compromising the signal quality, and obtaining profitable results both for the in-band distortion (NMSE) and the out-band distortion (ACPR).

After analyzing the results, we can conclude that the best working conditions complying specifications are found for signals with a PAPR between 6 dB and 8 dB.

Working above 8 dB of PAPR is not recommended due to the power efficiency decrease. On the other hand, below 6 dB of PAPR, a marked degradation in the signal quality is observed.

In practice, the PAPR target and modulation scheme will be chosen for a specific application considering the channels conditions.

Based on the tests presented throughout this chapter, it has been proven that it is possible to meet the communication standards requirements employing the based-board test bench proposed.

CONCLUSION

Taking into account the power limitations discussed for small satellites applications and its impact on the demand of high-efficient communications systems, the main objective of this project has been the design of an efficient power amplifier combined with the implementation of CFR and DPD techniques. Moreover, the deployment of a low-budget test bench based in development boards was proposed to carry out the PA evaluation and linearization avoiding the use of expensive laboratory equipment for signal generation and analysis.

The contributions of this work can be appreciated into three stages that have been assembled with the aim of providing a complete measurement environment.

To begin with, the design of a high efficient class-E power amplifier has been been addressed obtaining higher efficiency performance that conventional linear-based amplifiers design due to the optimized harmonic terminations.

Secondly, the hardware integration of the board-based test bench taking into account RF considerations for synchronism and calibration has been carried out as well as the signal processing concepts for a correct acquisition and restoration of the signal.

Finally, the implementation of CFR and DPD algorithms using Matlab has been extensively tested beginning with the evaluation in a instrument-based test bench with a commercial amplifier until the final integration with the proposed board-based test bench evaluating the designed class-E PA.

The linearization and the consequently efficiency improvement in the class-E power amplifier were achieved through the joint implementation of the CFR and DPD techniques in order to meet the linearity requirements imposed by the communications standards of -45 dB of ACPR.

Regarding the back-off operation, the maximum ACPR achieved was -40,6 dB for a power mean of 27,5 dBm and 12,5% of power efficiency considering a 64QAM OFDM test signal and a PAPR target of 8 dB. Thus, the peak cancellation technique in combination with the DPD implementation has been studied to decrease the back-off operation of the amplifier.

We managed to achieve about 50% of power efficiency for 36,6 dBm of power mean and a ACPR above -45 dB for the same test signal conditions. In addition, we can noticed that an EVM of 1,4% and a NMSE of -30,3 dB shows that the application of the CFR technique has not introduced significant distortions for a 8 dB PAPR target, moreover it has allowed us to work closer to the saturation point which entails a significant improvement in the efficiency.

We can consider that the best performance for operation are found between 6 dB and 8 db of PAPR, therefore the selection of the PAPR target and the modulation order will be chosen considering the channels conditions for a specific implementation.

To summarize, we conclude that the experimental campaign was satisfactorily. We demonstrate that it is possible to linearize a power amplifier obtaining EVM values and a spectral mask within the limits of the communications standards and using a low-cost board-based test bench.

Among the improvements that could be addressed in a future work, we should consider the optimization of the number of coefficients employed for the DPD behavioral model or the implementation of techniques focused on reducing the number of coefficients. This considerations would allow the implementation of a more efficient predistorter in terms of computational complexity.

BIBLIOGRAPHY

[And11]   Zhu Anding. *Fa-Long, Luo, editor, Digital Front-End in Wireless Communications and Broadcasting: circuits and signal processing.* Cambridge University Press, 2011. 13

[BDS14]   Pedro Miguel Brinco De Sousa. Digital predistortion of wideband communication signals with reduced observational bandwidth and reduced model order complexity. Master's thesis, Universitat Politècnica de Catalunya, 2014. 6, 14, 16, 17

[Bra11]   R. Neil Braithwaite. *Fa-Long, Luo, editor, Digital Front-End in Wireless Communications and Broadcasting: circuits and signal processing.* Cambridge University Press, 2011. 12

[Bra13]   R Neil Braithwaite. Model order selection for digital predistortion of a rf power amplifier when the distortion spectrum exceeds the observation bandwidth. *International Journal of Microwave and Wireless Technologies*, 5(02):163–170, 2013. 14, 16

[CP03]   NB Carvalho and José Carlos Pedro. Intermodulation distortion in microwave and wireless circuits. *Artect House, Boston*, 2003. 5

[Cri99]   SC Cripps. Rf power amplifies for wireless communications, artech house, 1999. *S. Cripps: Advanced techniques in RF power amplifier design. Artech House*, 1999. 19

[EB16]   Filipe Miguel Esturrenho Barradas. Modeling and digital predistortion of wireless radio frequency transmitters. Master's thesis, Universidade de Aveiro, 2016. 13

[End16]   EnduroSat. S-band / uhf transceiver user manual. http://www.endurosat.com, November 2016. 2

[GM12]   Pere L Gilabert and Gabriel Montoro. Design of Adaptive Digital Predistorter Linearizers for Envelope Tracking Power Amplifiers, 2012. 15, 16, 17

[GMW+16]   Pere L Gilabert, Gabriel Montoro, Teng Wang, M Nieves Ruiz, and José A García. Comparison of model order reduction techniques for digital predistortion of power amplifiers. In *Microwave Conference (EuMC), 2016 46th European*, pages 182–185. IEEE, 2016. 45

[GP08]   Pere Lluís Gilabert Pinal. *Multi look-up table digital predistortion for RF power amplifier linearization.* Universitat Politècnica de Catalunya, 2008. 5, 7, 11, 19

[Hal15]   Kamran Haleem. Study of space condition effect and analyzing digital techniques for improving rf power amplifier's linearity and efficiency for small satellites. Master's thesis, Universitat Politècnica de Catalunya, 2015. 1

[KCSK07]   Wan-Jong Kim, Kyoung-Joon Cho, Shawn P Stapleton, and Jong-Heon Kim. An efficient crest factor reduction technique for wideband applications. *Analog Integrated Circuits and Signal Processing*, 51(1):19–26, 2007. v, 18

[Ken00]   Peter B Kenington. *High linearity RF amplifier design*. Artech House, Inc., 2000. 7, 8

[KK01]   J Kim and K Konstantinou. Digital predistortion of wideband signals based on power amplifier model with memory. *Electronics Letters*, 37(23):1417–1418, 2001. 13

[Kul17]   Erik Kulu. Nanosatellite database. http://www.nanosats.eu, January 2017. 1

[Mad95]   Thomas B Mader. *Quasi-optical class-E power amplifiers*. PhD thesis, University of Colorado, 1995. 21

[MG11]   Gabriel Montoro and Pere L. Gilabert. *Fa-Long, Luo, editor, Digital Front-End in Wireless Communications and Broadcasting: circuits and signal processing*. Cambridge University Press, 2011. v, 7, 12, 13

[Mic16]   Space Micro. μstdn-100 transponder. http://www.spacemicro.com, June 2016. 2

[MMK$^+$06] Dennis R Morgan, Zhengxiang Ma, Jaehyeong Kim, Michael G Zierdt, and John Pastalan. A generalized memory polynomial model for digital predistortion of rf power amplifiers. *IEEE Transactions on signal processing*, 54(10):3852–3860, 2006. 15

[MS00]   V John Mathews and Giovanni L Sicuranza. *Polynomial signal processing*, volume 27. Wiley-Interscience, 2000. 13

[MT$^+$16] Reinel Marante Torres et al. Diseño de circuitos y esquemas de transmisión con alta eficiencia en tecnología gan hemt. 2016. 19, 21

[PGCT]   Roberto Peña, José Ángel García, M Chaibi, and NA Touhami. Diseño de un amplificador de alta eficiencia clase-e@ 2ghz. 19, 20

[Raa77]   Frederick Raab. Idealized operation of the class e tuned power amplifier. *IEEE transactions on Circuits and Systems*, 24(12):725–735, 1977. 20

[SA05]   Abdulrhman Mohammed Salman Ahmed. *Analysis, Modelling and Linearization of Nonlinearity and Memory Effects in Power Amplifiers Used for Microwave and Mobile Communications*. Kassel University Press, 2005. v, 8, 19, 20

[Sch80]   Martin Schetzen. *The Volterra and Wiener theories of nonlinear systems*. Wiley, 1980. 13

[SG15]   Rainee N Simons and Kavita Goverdhanam. Applications of nano-satellites and cube-satellites in microwave and rf domain. In *Microwave Symposium (IMS), 2015 IEEE MTT-S International*, pages 1–4. IEEE, 2015. 1

[SIT$^+$12] Hirobumi Saito, Naohiko Iwakiri, Atsushi Tomiki, Takahide Mizuno, Hiromi Watanabe, Tomoya Fukami, Osamu Shigeta, H Nunomurac, Yasuaki Kanda, K Kojimae, et al. High-speed downlink communications with hundreds mbps from 50kg class small satellites. *2012IAC, IAC-12-B2*, 3, 2012. 1

[SOGG08] Dominique Schreurs, Máirtín O'Droma, Anthony A Goacher, and Michael Gadringer. *RF power amplifier behavioral modeling*. Cambridge University Press New York, NY, USA, 2008. v, 6, 7

[SS75]   Nathan O Sokal and Alan D Sokal. Class ea new class of high-efficiency tuned single-ended switching power amplifiers. *IEEE Journal of solid-state circuits*, 10(3):168–176, 1975. v, 20, 21

[TI16a]   TI. Adc32rf45 dual-channel, 14-bit, 3.0-gsps, analog-to-digital converter (rev. c), December Revised 2016. vii, 34

[TI16b]   TI. Tsw3065evm standalone local oscillator source, August Revised 2016. 34

[TI16c]   TI. Tsw308x evaluation module, May Revised 2016. vii, 32

[Unl16]   Theters Unlimited. Flexible high-performance l- and s-band communications. http://www.tethers.com, October 2016. 2

[VR03]   Joel Vuolevi and Timo Rahkonen. *Distortion in RF power amplifiers*. Artech house, 2003. 7, 19, 20

[Wir13]   IQ Wireless. Slink. http://www.iq-wireless.com, December 2013. 2