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High-temperature characteristics of zone-melting recrystallized silicon-on-insulator MOSFETs

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Abstract. The characteristics of enhancement-mode MOS transistors fabricated on zone-melting recrystallized (ZMR) silicon-on-insulator (SOI) films were systematically experimentally investigated in the temperature range 25–300°C. The main temperature-dependent parameters (the threshold voltage, the channel mobility, subthreshold slope, off-state leakage currents) of ZMR SOI MOSFETs are described and compared with both theory and SIMOX devices. It is shown that high carrier mobilities and low off-state leakage currents can be obtained in thin-film ZMR SOI MOSFETs at elevated temperatures. At T = 300°C, far beyond the operating range of bulk silicon devices, the off-state leakage current in ZMR SOI MOSFETs with a 0.15 μm-thick silicon film was only 0.5 nA/μm (for V_D = 3 V), that is 3–4 orders of magnitude lower than typical values in bulk Si devices. The presented results demonstrate that CMOS devices fabricated on sufficiently thin ZMR SOI films are well suited for high-temperature applications.

Keywords: Silicon-on-insulator**,** high-temperature, MOS-devices.

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1. Introduction

Many applications of CMOS integrated circuits require operation at elevated temperatures. Conventional bulk silicon MOS integrated circuits can only be used at moderate temperatures (as a rule, up to 200°C). At higher temperatures bulk silicon CMOS devices usually fail because of thermally-induced latch-up, threshold voltage shifts, dramatically increased junction leakage. Due to the possibility of latch-up free operation, much lower leakage currents, smaller threshold voltage shifts, thin-film, fully-depleted SOI MOS devices are considered to be very attractive for high-temperature applications [1, 2]. High-temperature characteristics of MOSFETs fabricated on SIMOX (separation by implanted oxygen) SOI films have been reported in several papers [3–5]. Zone-melting recrystallization (ZMR) is an alternative approach for the SOI wafer preparation [1, 6]. The major advantage of the ZMR technology is an essentially lower SOI wafer cost. In this paper, a systematic experimental investigation of the high-temperature characteristics of MOS transistors realized on thinned ZMR SOI films has been performed. The presented results demonstrate the suitability for high-temperature applications of MOS devices fabricated on sufficiently thin ZMR SOI films.

2. Device Fabrication

The SOI films used in this study were prepared by the laser zone-melting recrystallization technique [6]. A linear molten zone was formed by a high-power CW YAG:Nd laser A circular laser beam was transformed into a linear spot by using special cylindrical lenses. The linear spot exceeds 100 mm in length. In order to provide «a low thermal gradient regime», a wafer was heated up to 1300°C from the backside by a set of halogen lamps. The scanning speed of the molten zone was 1 mm/s. Recrystallization was performed in a single pass.

Recrystallized structure was composed of a 0.4-μm thick polysilicon film deposited on an oxidized silicon wafer and covered by a SiO_2 cap layer to prevent agglomeration of the molten zone.

The obtained ZMR silicon films consisted of a small number of highly oriented crystals (grains) extended along the whole wafer and having (100) orientation with <100> axes close to the scan direction. The main defects in such films are low-angle grain boundaries (sub-boundaries). which are associated with misorientations of 1 deg or less and spaced 10–20 μm from one another.

After the recrystallization process the silicon films were thinned by oxidation and oxide etching. The final silicon film

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thickness was adjusted to 0.15 µm. N- and p-channel enhancement-mode devices were fabricated using a standard polysilicon gate CMOS process. For comparison purposes, devices were also fabricated in 0.4 µm-thick silicon films. Gate electrodes in both p- and n-channel devices are n^+-polysilicon. The gate oxide and buried oxide thicknesses are 0.08 and 1.0 µm, respectively. Long channel devices (L = = 20 µm) are used to avoid short channel effects. The doping level of the channel region is 1×10^{16} cm^{-3} for both p- and n-channel devices. Given doping level was used to ensure full-depletion operation of the devices with a 0.15 thick silicon film up to 300°C. P-channel devices were formed also on undoped silicon films having a residual donor concentration of 2×10^{15} cm^{-3}.

For comparison, the measurements were also performed on SIMOX MOSFETs fabricated on commercially available SIMOX SOI wafers with 0.4 µm buried oxide. The gate oxide and silicon film thickness in SIMOX devices are 0.03 and 0.08 µm, respectively. The doping level of the channel region is 5×10^{16} cm^{-3}.

3. Device Parameters

Temperature-dependent MOSFET parameters were obtained from the measurements of drain current (I_D) versus the front-gate voltage (V_{gf}) measured for different drain voltages (V_D) and back-gate voltages (V_{gb}) at various temperatures. The I_{gf} (V_{gf})-characteristics of the n-channel device measured at various temperatures are shown in fig. 1 in a semilog scale for I_D.

A. Transconductance and Mobility

Fig. 2 shows static front-gate voltage transconductance characteristics measured for n- and p-channel devices in the ohmic region of operation at various temperatures. The normalized transconductance curves actually represent the effective field-effect mobility. The transconduc-tance peak is proportional to the low-field mobility, and the position of the transconductance peak is roughly located at the threshold voltage V_{th}. The decrease in the transconductance following after the peak is associated with the mobility reduction caused by the increase of the normal electric field in the inversion channel. The effective mobility μ_{eff} is usually given by the empirical law: [7]

$$\mu_{eff} = \frac{\mu_0}{1+\theta\cdot(V_{gf}-V_{th})} \quad (1)$$

where μ_0 is the low-field mobility, θ is the mobility reduction factor.

The low-field mobilities in n- and p-channel devices extracted from the transconductance curves $g_m(V_{gf})$ for $V_{gf} = V_{th}$ are shown in fig. 3 as a function of temperature. For reference, the mobilities obtained in SIMOX SOI MOSFETs are also plotted on the same figure. One could expect that the mobility and the mobility reduction factor in ZMR SOI MOSFETs would be adversely affected by subgrain boundaries and the surface waviness inherent to ZMR silicon films. However, as can be seen from fig. 3, the carrier mobilities in

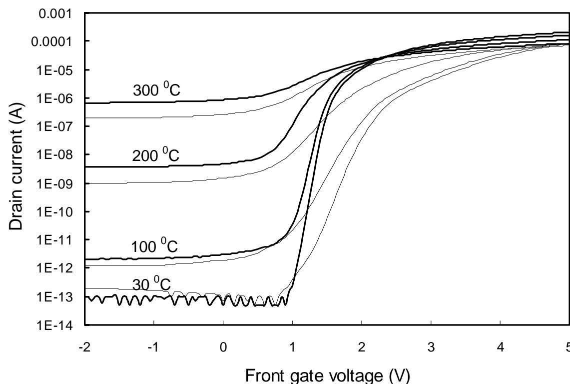

Fig. 1. Drain current vs front gate voltage characteristics of the n-channel SOI MOSFET with a 0.15-µm silicon film (Z/L = 500/20) measured at various temperatures with V_D = 3 V and V_{gb} = 0 V (bold line) and V_{gb} = –10 V (thin line).

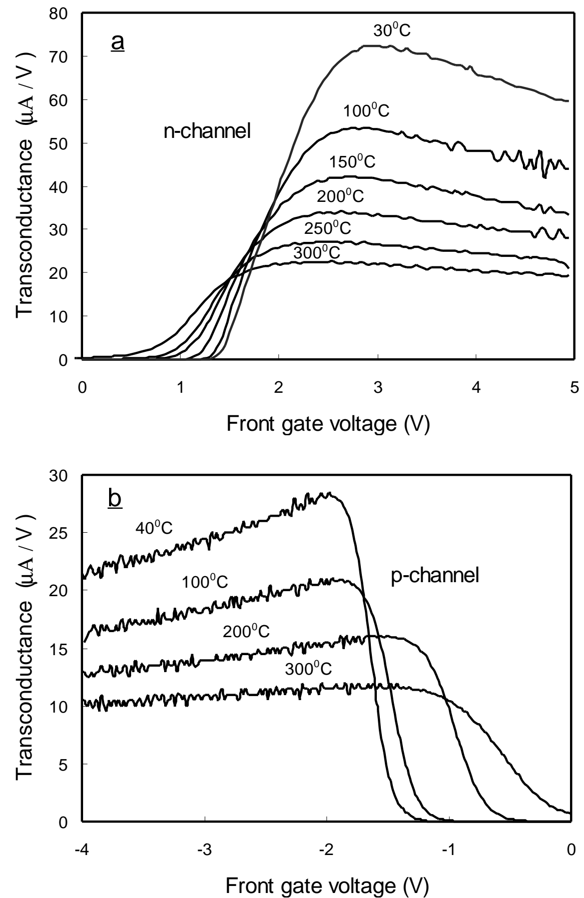

Fig. 2. Front-gate transconductance characteristics measured for n-channel ZMR SOI MOSFET (a) and p-channel ZMR SOI MOSFET (b) in the ohmic region of operation at various temperatures (Z/L = 500/20, d_{Si} = 0.15 µm, V_D = 100 mV, V_{gb} = 0 V).

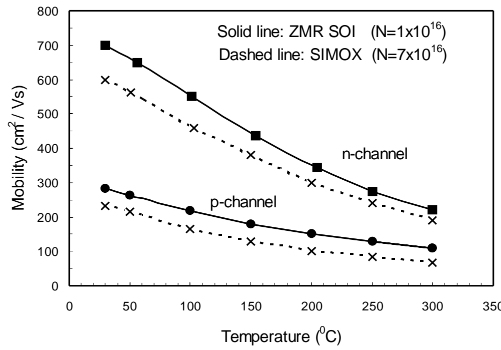

Fig. 3. The temperature dependence of the low-field mobilities obtained from the transconductance curves for $V_{gf} = V_{th}$ in n- and p-channel ZMR and SIMOX SOI MOSFETs ($V_{gb} = 0$ V).

ZMR MOSFETs are rather high and even exceed the mobility values in SIMOX devices (the latter can be attributed to the reduced doping level of the ZMR silicon film). This means that subgrain boundaries have little or no effect on the carrier mobility, at least at room and elevated temperatures. From fig. 3 it follows that the carrier mobility in ZMR SOI devices varies with temperature as in SIMOX SOI or as in bulk devices [2–5]:

$$\mu_0(T) = \mu_0(273) \cdot \left(\frac{T}{273}\right)^{-m} \tag{2}$$

with $m = 1.7$–1.9.

The temperature dependence of the mobility reduction factor is shown in fig. 4. The values obtained for the mobility reduction factor θ in ZMR MOSFETs are 2–3 times greater than typical values reported for SIMOX devices, which is most likely due to the surface roughness of the ZMR silicon film. From Fig. 4 it can be noted that the mobility reduction factor decreases with temperature in a similar way similar to SIMOX SOI devices [4]. This is due to a lowering of the perpendicular electric field in the inversion channel.

B. Threshold Voltage

The temperature dependence of the threshold voltage V_{th} in a bulk or partially depleted SOI MOSFET (on the assumption that the Si bandgap and oxide charge density are independent on temperature) can be written as [1]:

$$\frac{dV_{th}}{dT} = \frac{d\phi_F}{dT}\left(1 + \frac{q}{C_{of}}\sqrt{\frac{\varepsilon_{Si} \cdot N}{kT \cdot \ln(N/n_i)}}\right) \tag{3}$$

where Φ_F is the Fermi potential, C_{of} is the front gate oxide capacitance, N is channel doping, n_i is the Si intrinsic concentration, and the other symbols have their usual meaning. In bulk or partially depleted SOI devices the threshold voltage shift with temperature is predominantly due to the variation of the depletion layer width in strong inversion (the second term in brackets), which does not happen in fully depleted SOI devices. The temperature coefficient of the threshold voltage dV_{th}/dT in SOI fully depleted devices with depleted back interface is expected to be approximately equal to $d\Phi_F/dT$ [1]. As a result, the variation of the threshold voltage with temperature in SOI fully depleted devices is at least two or three times less than that in bulk devices (depending on channel doping and the gate oxide thickness) [1–3].

Fig. 5 shows the temperature dependence of the threshold voltage for n- and p-channel devices with a 0.15-μm-thick silicon film. For n-channel devices at temperatures below 200°C dV_{th}/dT is equal 0.9 mV/°C, that is in a good agreement with the value of 0.89 mV/°C predicted by equation (3). For p-channel devices dV_{th}/dT is about 1.5 mV/°C, that is higher than the predicted value. However, the temperature coefficient of the threshold voltage in both n- and p-channel SOI devices is essentially lower than is predicted to be in a bulk device (for a given gate oxide thickness and channel doping of 1×10^{16} cm^{-3} the dV_{th}/dT should be about 3 mV/°C). The increase of dV_{th}/dT above 200°C in the devices with channel doping of 1×10^{16} cm^{-3} is believed to be caused by the transition of the devices from the fully depleted to the partially depleted mode [1]. A simi-

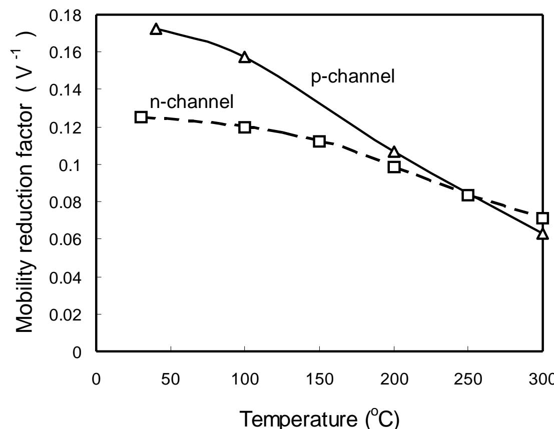

Fig. 4. The temperature dependence of the mobility reduction factor θ in p- and n-channel ZMR SOI MOSFETs ($V_{gb} = 0$ V).

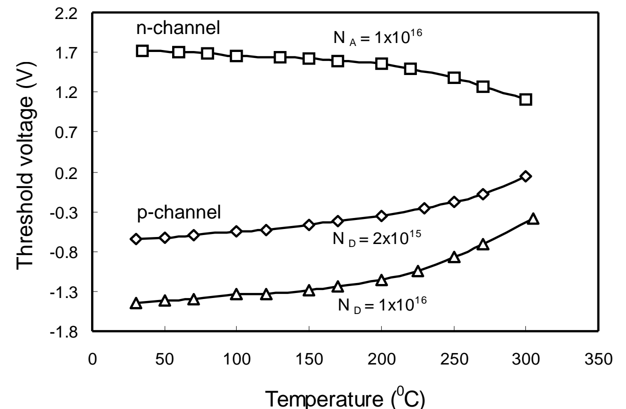

Fig. 5. The temperature dependence of the threshold voltage for n- and p-channel devices with a 0.15 μm silicon film measured for $V_D = 100$ mV, $V_{gb} = 0$ V.

lar increase of the dV_{th}/dT is observed in the devices with channel doping of 2×10^{15} cm^{-3}, which are certain to remain fully depleted (by a conventional definition) up to 300°C. This is likely due to the fact that the strong inversion model [8] is no longer valid when the silicon film becomes near-intrinsic.

C. Subthreshold Slope

The subthreshold swing (inverse subthreshold slope) in a SOI MOSFET is given by the following expression [7,9]:

$$S = \frac{dV_{gf}}{d(\log I_D)} = \frac{kT}{q} \cdot \ln(10) \cdot \left(1 + \frac{C_{tf}}{C_{of}} + \alpha \cdot \frac{C_d}{C_{of}}\right), \quad (4)$$

where $C_{tf} = qN_{tf}$ is the capacitance due to the front interface state density N_{tf}, C_d is the capacitance of the depleted silicon film $C_d = \frac{\varepsilon_{Si}}{d_{Si}}$ (d_{Si} is the silicon film thickness), α is the coupling coefficient, which accounts for the back interface conditions, for the case of accumulation at the back interface $\alpha \approx 1$, for the case of depletion at the back interface:

$$\alpha = \frac{C_{ob} + C_{tb}}{C_d + C_{ob} + C_{tb}}, \quad (5)$$

with $C_{tb} = qN_{tb}$ being the capacitance due to the back interface state density N_{tb}. From eq. (4), in a fully depleted SOI device, S is expected to increase linearly with temperature.

The experimental temperature dependence of the subthreshold swing measured in the ZMR devices with channel doping of 1×10^{16} and 2×10^{15} cm^{-3} is shown in fig. 6. The measurements are performed for zero back-gate bias. For these conditions, when a weak inversion region is formed at the front interface, the back silicon film interface is in depletion. For this case, as follows from eqns.(4)–(5), the value of S reflects the influence of the quality of both silicon film interfaces. The dashed line in fig. 6 presents the $S(T)$-dependence calculated ignoring the interface states at both interfaces. One can note that at moderate temperatures experimental results agree well with calculation, indicating the relatively low interface state densities at both interfaces. As can be seen in fig. 6, the subthreshold swing exhibits the expected linear temperature dependence only up to T ≤ 150°C and rapidly rises with further increase in temperature, in spite of the fact that devices with such parameters should remain fully depleted (by a conventional definition) up to 300°C. Similar behavior of the subthreshold swing was reported in the literature for SIMOX SOI devices [5]. Therefore, the observed nonlinear $S(T)$- dependence at high temperatures is unrelated to the SOI material used. It is probable that at high temperatures eq. 4, which, in fact, is based on the depletion approximation and a charge sheet model, is no longer valid. However, this is beyond the scope of the present work.

D. Off-state Leakage Current

The increase in the off-state leakage current with temperature is one of the main factors limiting the upper operating temperature of bulk silicon CMOS devices. Much smaller high-temperature off-state currents are expected to be in SOI devices due to smaller source-drain junction areas and due to elimination of very large well-to-substrate junction leakages.

In general case, the off-state leakage current (I_{off}) in an enhancement-mode SOI MOSFET involves generation current (I_{gen}) in the depleted region of the reverse-biased drain junction and diffusion current (I_{diff}) from undepleted portion of the film:

$$I_{gen.} = \frac{q \cdot n_i \cdot W_g(V_D)}{\tau_g} d_{Si} \cdot Z, \quad (6)$$

where τ_g is the minority carrier generation lifetime, W_g is the generation layer width, Z is the device width.

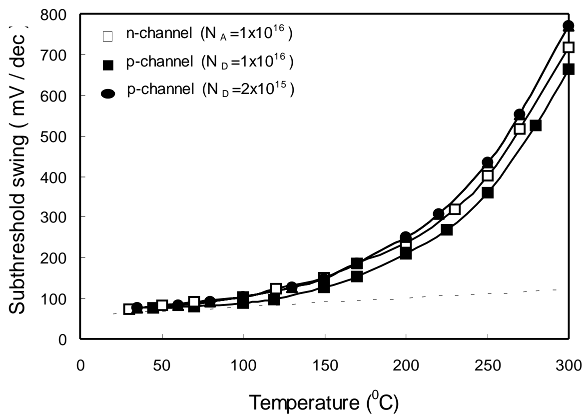

Fig. 6. The experimental temperature dependence of the inverse subthreshold slope factor S in ZMR SOI devices with a 0.15 μm silicon film (V_D = 100 mV, V_{gb} = 0 V). The dashed line shows the $S(T)$-dependence calculated from the classical model for fully depleted SOI MOSFET with depleted back interface.

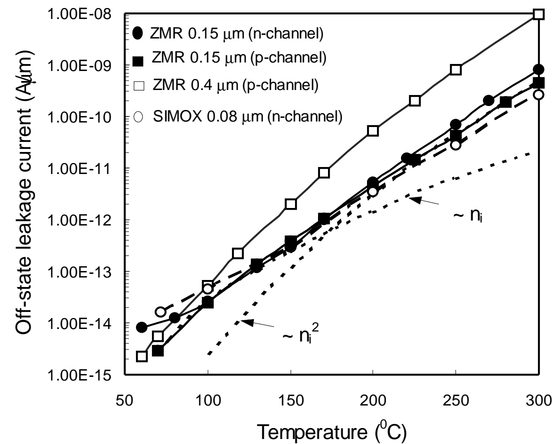

Fig. 7. The temperature dependence of the off-state leakage current per unit gate width in ZMR SOI devices with a 0.15 and 0.4 μm-thick silicon film measured with both front and back gates strongly biased in off-direction for $|V_D|$ = 3 V. The dashed line shows the off-state leakage current in the SIMOX device.

The diffusion current in a n-channel SOI MOSFET can be written as[10]:

$$I_{diff} = q \cdot Z \cdot \sqrt{\frac{D_n}{\tau_{rn}}} \cdot \left(1 - e^{\frac{-qV_D}{kT}}\right) \cdot \int_0^{d_{Si}} \frac{n_i^2}{N_A} \cdot e^{\frac{q \cdot \varphi(x)}{kT}} dx , \qquad (7)$$

where D_n is the electron diffusivity, τ_{rn} is the electron recombination lifetime in the p-type Si film, $\varphi(x)$ is the potential distribution across the Si film thickness in undepleted body film.

The off-state current was measured as a function of drain and back-gate biase at various temperatures. It was experimentally observed that at high temperatures biasing the back-gate in off-direction (or in accumulation) resulted in a decrease in the off-current (approximately, by a factor of three) followed by quasi-saturation (see fig. 1). Fig. 7 shows the temperature dependence of the off-state current measured in ZMR SOI devices with a 0.15 and 0.4 μm-thick silicon film, when both front and back gates were strongly biased in off-direction. Under these conditions the off-state current reaches its minimum value. For comparison, the off-state current measured in a SIMOX MOSFET for similar conditions is shown on the same figure. One can see that at high temperatures in the device with a 0.15 μm-thick film the off-state current is substantially (more than an order of magnitude) lower than that in the device with a 0.4 μm-thick film and is only slightly higher than that in the SIMOX MOSFET. At T = 300°C for d_{Si} = 0.15 μm the off-state current per unit gate width is only 0.5 nA/μm (V_D = 3 V), that is 3–4 orders of magnitude lower than that in bulk devices. Although at room temperature, because of the relatively low value of the carrier generation lifetime ($\tau_g \approx 1$ μs) in the ZMR silicon film, the leakage current in the ZMR SOI MOSFETs was larger than in bulk devices [11].

It is seen from fig. 7 that in the device with a 0.15 μm-thick film in the temperature range 50–150°C the $I_{off}(T)$-dependence follows $n_i(T)$, suggesting the predominance of the generation current component. At temperatures above 150°C the off-current varies with temperature as $n_i^2(T)$, indicating that diffusion mechanism dominates. In the device with a 0.4 μm-thick film diffusion current becomes dominant at approximately 100°C. These results support the view that in SOI MOSFETs at high temperatures (above 100–150°C, depending on the drain voltage and the Si film thickness) diffusion mechanism is responsible for the observed off-state leakage currents. Therefore, the main trends of the high-temperature off-current can be understood from the analysis of eq. (7).

From eq. (7) it follows that in off-state of a SOI MOSFET diffusion current is determined by the potential and minority carrier concentration distributions, which vary with back-gate bias and the Si film thickness. By numerical simulation it has been shown that biasing the back gate in off-direction results in a decrease in the total minority carrier density in the Si film contributing in diffusion current [10]. This explains the observed back-gate voltage dependence of the off-state current.

The Si film thickness dependence can be understood from the analysis of Fig.8, which presents the calculated minority carrier concentration distributions in SOI films with different film thickness and doping of 1×10^{16} cm^{-3} at T = 300°C, when both front and back gates are strongly biased in the off-direction. Under these conditions both Si film interfaces are in strong accumulation. For reference, the minority carrier concentration in quasi-neutral Si with the same doping at the same temperature is shown by dashed line. It is evident that the carrier distribution in a SOI film is nonuniform across the film thickness and highly depends on the film thickness. Moreover, an average concentration is essentially lower than n_i^2/N_A, even in rather thick films. As a result, the total minority carrier density (integrated over the film thickness), which is responsible for off-state diffusion current, exhibits a strong (nonlinear) dependence on the Si film thickness, as shown in fig. 9. This provides an explanation for the essentially different values of the high-temperature off-state currents in SOI devices with different film thickness.

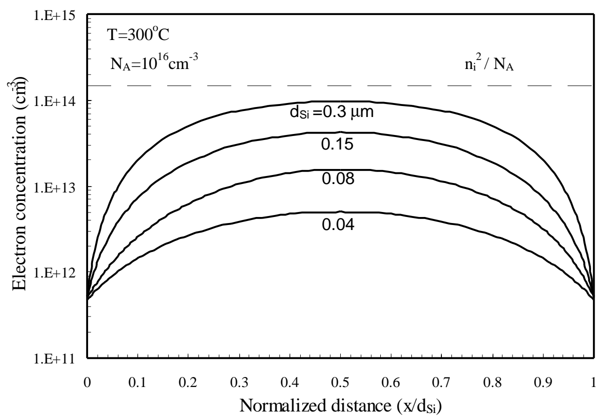

Fig. 8. The calculated minority carrier concentration distributions in SOI films with different film thickness and doping of 1×10^{16} cm^{-3} at T = 300°C, when both front and back silicon film interfaces are strongly accumulated.

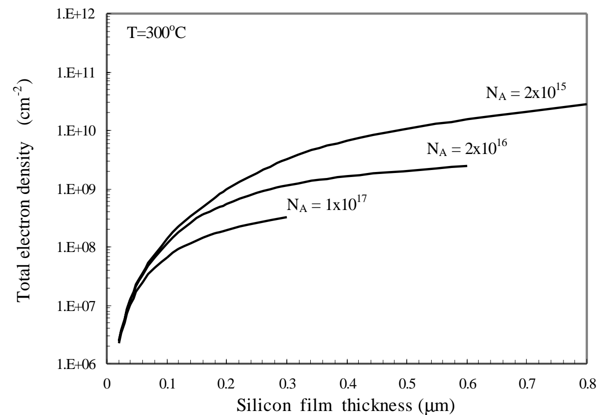

Fig. 9. The total minority carrier density in a SOI film (with both Si film interfaces strongly accumulated) as a function of the Si film thickness calculated for different film doping levels for T = 300°C.

It can be seen from fig. 9 that in relatively thin-film devices the off-state diffusion current should only slightly depend or not depend on the film doping.

When analyzing the off-state leakage current, it worth noting that the generation current is proportional to $1/\tau_g$, whereas diffusion current is proportional to $(1/\tau_{rn})^{1/2}$. Besides, from eq. (7) follows that in relatively short-channel devices, in which the channel length (L) is less than the carrier diffusion length ($L_n \equiv \sqrt{D_n \cdot \tau_{rn}}$), diffusion current and thus the high-temperature off-state current should not depend on τ_{rn} or L_n. Therefore, in terms of leakage current the silicon film quality is expected to be more important at room temperatures, than at high temperatures, when diffusion current is dominant.

From the above it may be concluded that the Si film thickness is the key parameter to minimize the high-temperature off-state leakage current.

4. Conclusion

The results presented in this paper demonstrate that the ZMR SOI technology, which is cheaper than the SIMOX technology, is suitable for fabrication of CMOS devices for high-temperature applications. The parameters of long-channel thin-film SOI MOSFETs fabricated using the laser ZMR-technique (with backside wafer heating up to 1300°C) are as good as SIMOX devices. The subgrain boundaries present in the ZMR SOI films seem to have little or no effect on the carrier mobility, at least at room and elevated temperatures. It is shown that the off-state .diffusion current in a SOI MOSFET strongly nonlinearly depends on the Si film thickness. Therefore, the Si film has to be thin enough to provide sufficiently low off-state leakage currents at high temperatures. It is also demonstrated that, in spite of relatively poor carrier lifetime ($\tau_g \approx 1$ µs) in the ZMR silicon film, in the device with a 0.15 µm-thick silicon film at T = 300°C for $V_D = 3$ V the off-state leakage current is only 0.5 nA/µm, that is 3–4 orders lower than in bulk Si devices. Moreover, preliminary results have shown that optimization of the initial recrystallized structure allows one to obtain sufficiently uniform ZMR SOI films with 0.1 µm silicon film. Thus, further improvement of high-temperature characteristics of ZMR SOI devices seems to be possible.

Acknowledgment

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ВИСОКОТЕМПЕРАТУРНІ ХАРАКТЕРИСТИКИ РЕКРИСТАЛІЗОВАНОГО ЗОННИМ ВИТОПЛЕННЯМ КРЕМНІЙ-НА-ІЗОЛЯТОРІ MOSFETS

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Резюме. Проведені кропіткі експериментальні дослідження високотемпературних (25-300°C) характеристик МОН транзисторів на базі КНІ-структур, виготовлених методом зонної лазерної перекристалізації. Розглянута поведінка основних температрно-залежних параметрів КНІ МОН транзисторів (порогової напруги, рухливості носіїв, підпорогового нахилу та струму витоку). Проведено порівняння отриманих результатів з теорією та аналогічними параметрами приладів, створених за допомогою ЗІМОХ технології. Показано, що при підвищених температурах тонкоплівкові транзистори, отримані лазерною зонною перекристалізацією, виявляють високу рухливість носіїв і низькі струми витоку закритого транзистора. При T = 300°C, що значно перевищує робочий діапазон приладів на об'ємному кремнії, струм витоку в КНІ транзисторах з плівкою Si товщиною 0.15 мкм становить всього лишу 0.5 nA/µm (при V_D = 3В), що на 3-4 порядка нижче типових величин для приладів на об'ємному кремнії. Наведені результати свідчать, що тонкі плівки КНІ, створені методом лазерної зонної перекристалізації, можуть успішно використовуватись для створення КМОН ІС для високотемпературних застосувань.

ВИСОКОТЕМПЕРАТУРНЫЕ ХАРАКТЕРИСТИКИ РЕКРИСТАЛЛИЗОВАННОГО ЗОННЫМ ВЫТАПЛИВАНИЕМ КРЕМНИЙ-НА-ИЗОЛЯТОРЕ MOSFETS

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Резюме. Проведено детальное экспериментальное исследование высокотемпературных (25-300°C) характеристик МОП транзисторов на основе КНИ-структур, изготовленных методом лазерной зонной перекристаллизации. Рассмотрено поведение основных температурно-зависимых параметров КНИ МОП транзисторов (порогового напряжения, подвижности носителей, подпорогового наклона и тока утечки). Проведено сравнение полученных результатов с теорией и аналогичными параметрами приборов, созданных SIMOX технологией. Показано, что при повышенных температурах тонкопленочные транзисторы, полученные лазерной зонной перекристаллизацией, проявляют высокую подвижность носителей и низкие токи утечки закрытого транзистора. При T = 300°C, значительно превышающей рабочий диапазон приборов на объемном кремнии, ток утечки в КНИ транзисторах с пленкой Si толщиной 0.15 мкм составляет всего лишь 0.5 nA/µm (при V_D = 3B), что на 3-4 порядка ниже типичных величин для приборов на объемном кремнии. Приведенные результаты свидетельствуют, что тонкие пленки КНИ, полученные методом лазерной зонной перекристаллизации, могут успешно использоваться для создания КМОП ИС для высокотемпературных применений.