LOW POWER ANALOG TO DIGITAL CONVERTERS IN ADVANCED CMOS TECHNOLOGY NODES

A Dissertation

by

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ABSTRACT

The dissertation presents system and circuit solutions to improve the power efficiency and address high-speed design issues of ADCs in advanced CMOS technologies.

For image sensor applications, a high-performance digitizer prototype based on column-parallel single-slope ADC (SS-ADC) topology for readout of a back-illuminated 3D-stacked CMOS image sensor is presented. To address the high power consumption issue in high-speed digital counters, a passing window (PW) based hybrid counter topology is proposed. To address the high column FPN under bright illumination conditions, a double auto-zeroing (AZ) scheme is proposed. The proposed techniques are experimentally verified in a prototype chip designed and fabricated in the TSMC 40 nm low-power CMOS process. The PW technique saves 52.8% of power consumption in the hybrid digital counters. Dark/bright column fixed pattern noise (FPN) of 0.0024%/0.028% is achieved employing the proposed double AZ technique for digital correlated double sampling (CDS). A single-column digitizer consumes total power of 66.8μW and occupies an area of 5.4 μm x 610 μm.

For mobile/wireless receiver applications, this dissertation presents a low-power wide-bandwidth multistage noise-shaping (MASH) continuous-time delta-sigma modulator (CT-ΔΣM) employing finite impulse response (FIR) digital-to-analog converters (DACs) and encoder-embedded loop-unrolling (EELU) quantizers. The proposed MASH 1-1-1 topology is a cascade of three single-loop first-order CT-ΔΣM

stages, each of which consists of an active-RC integrator, a current-steering DAC, and an EELU quantizer. An FIR filter in the main 1.5-bit DAC improves the modulator's jitter sensitivity performance. FIR's effect on the noise transfer function (NTF) of the modulator is compensated in the digital domain thanks to the MASH topology. Instead of employing a conventional analog direct feedback path, a 1.5-bit EELU quantizer based on multiplexing comparator outputs is proposed; this approach is suitable for high-speed operation together with power and area benefits. Fabricated in a 40-nm low-power CMOS technology, the modulator's prototype achieves a 67.3 dB of signal-to-noise and distortion ratio (SNDR), 68 dB of signal-to-noise ratio (SNR), and 68.2 dB of dynamic range (DR) within 50.5 MHz of bandwidth (BW), while consuming 19 mW of total power (P). The proposed modulator features 161.5 dB of figure-of-merit (FOM), defined as FOM = SNDR + 10 log10 (BW/P).

DEDICATION

To my parents and Xin

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First of all, I would like to express my sincere appreciation to my advisor, Dr. Jose Silva-Martinez. Without his guidance, my research and dissertation will not be possible. During my research and study, he is always patient and supportive when I have problems. I have learnt from him, not just limited to technical aspect, but also from his personality. He is an extremely nice person and also a wonderful friend.

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Contributors

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The work for the Section III of the dissertation was completed by the student, in collaboration with Alexander Edward, under the advisement of Dr. Jose Silva-Martinez of the Department of Electrical and Computer Engineering together with Dr. Martin Kinyua and Dr. Eric G. Soenen from TSMC Technology, Inc.

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I. INTRODUCTION

1.1. Motivation

At a time of the information technology revolution, one of the main driving sources for the revolution of modern human society is the trend of moving functionality into the digital domain. Faster digital signal processers (DSPs) capable of performing numerous complex functions are developed thanks to advanced CMOS technologies. However, the "bridge" between the analog and the digital world, analog-to-digital converters (ADCs), are facing design challenges to meet the wide-bandwidth, high-resolution and low-power consumption targets. With the added speed of new generations of DSPs implemented in advanced technology nodes, the bandwidth of ADCs is becoming the bottleneck for the overall system. Reduced supplies mean reduced signal range, which generally demands higher accuracy for the same dynamic range (DR) target. As a potentially power hungry component, the ADC power needs to be reduced to improve the battery life of portable devices.

ADCs are widely used in the market for sensors, wireline/wireless communication, computers and consumer electronics. The resolution and bandwidth requirement for different applications are shown in Fig. 1.1. Different applications demand different ADC topologies and the specifications and design challenges are also different.

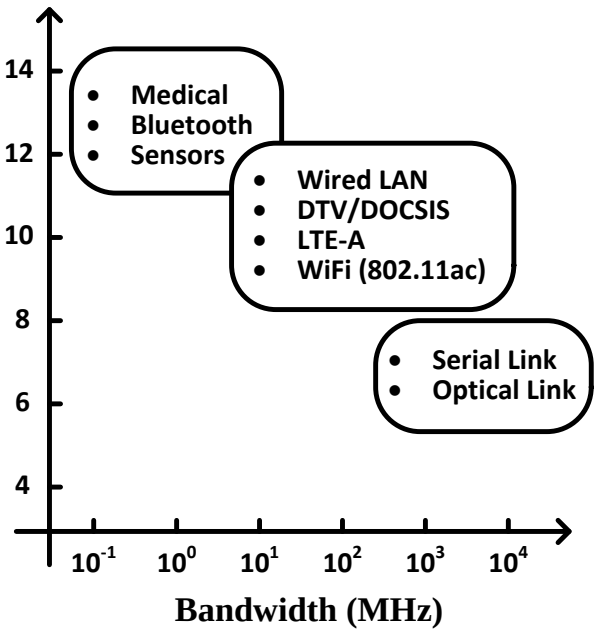


Fig. 1.1 Resolution and bandwidth requirements for different applications.

One focus of the dissertation is on low-power ADC design for image sensor readout applications where the demanded resolution is around 12 bit. If global ADC architecture is employed for the entire 16-Mpixel, 8000 (H) x 2000 (V) array at a frame rate of 60 fps, the ADC sampling speed needs to be close to GHz Sample/s range. The simple calculation assumes the entire readout period is used for the analog-to-digital conversion. However this is not the real case in the application and thus even higher speed ADCs may be demanded. Another topology of using one single-slope ADC dedicated for each column can significantly lower down the speed requirement. The single-slope ADC array topology has the benefit of being very simple with only the comparator and the ramp as analog circuits. The counter and the logic are all implemented in digital. As an ADC array, the ramp can be shared and generated globally which can further improve

the power efficiency of the topology. However, even with such benefits, the readout circuit still consumes a large portion of power in the image sensor chip especially under high-frame mode, due to the high-speed refreshing scheme in conventional counter implementation. Thus, to be able to achieve low-power readout for the next generation imagers operating at 120 fps or higher, effective techniques are demanded.

Another application of focus is on the low-power ADC design in mobile/wireless receivers. In LTE-Advanced, with the carrier aggregation technique added to conventional LTE, the up and down link speed has been improved based on aggregating the component carriers with bandwidth of 1.4, 3, 5, 10, 15 or 20 MHz. The same carrier aggregation concept is applied to WiFi 802.11ac to boost its link speed. The next generation 5th-Generation (5G), further improvement in the link speed is demanded which mains wider band ADCs in receivers will be in huge demand. Conventionally, single-loop continuous-time delta-sigma ADC is the most popular choice in the mobile/wireless receiver due to its high dynamic range capability, implicit anti-aliasing behavior, and tolerance of out-of-band blockers. However, there is still stability and overload recovery issue in high-order modulators demanding new techniques to handle.

1.2. Research Contribution

The dissertation presents system and circuit solutions to improve the power efficiency and address high-speed design issues of ADCs in advanced CMOS technologies.

For image sensor applications, a high-performance digitizer prototype based on column-parallel single-slope ADC (SS-ADC) topology for readout of a back-illuminated 3D-stacked CMOS image sensor is presented. To address the high power consumption issue in high-speed digital counters, a passing window (PW) based hybrid counter topology is proposed. In this approach, the memory cells in the digital counters of SS-ADCs are disconnected from the global bus during non-relevant timing. To address the high column FPN under bright illumination conditions, a double auto-zeroing (AZ) scheme is proposed. In this technique, the AZ process is employed twice at reset and signal level, respectively. The double AZ scheme not only allows the comparator to serve as a crossing detector around the common-mode level, but it also enables low-voltage comparator design. The proposed techniques are experimentally verified in a prototype chip designed and fabricated in the TSMC 40 nm low-power CMOS process. The PW technique saves 52.8% of power consumption in the hybrid digital counters. Dark/bright column fixed pattern noise (FPN) of 0.0024%/0.028% is achieved employing the proposed double AZ technique for digital correlated double sampling (CDS). A single-column digitizer consumes total power of 66.8μW and occupies an area of 5.4 μm x 610 μm.

For mobile/wireless receiver applications, this dissertation presents a low-power wide-bandwidth multistage noise-shaping (MASH) continuous-time delta-sigma modulator (CT-ΔΣM) employing finite impulse response (FIR) digital-to-analog converters (DACs) and encoder-embedded loop-unrolling (EELU) quantizers. The proposed MASH 1-1-1 topology is a cascade of three single-loop first-order CT-ΔΣM stages, each of which consists of an active-RC integrator, a current-steering DAC, and an EELU quantizer. An FIR filter in the main 1.5-bit DAC improves the modulator's

jitter sensitivity performance. FIR's effect on the noise transfer function (NTF) of the modulator is compensated in the digital domain thanks to the MASH topology. Instead of employing a conventional analog direct feedback path, a 1.5-bit EELU quantizer based on multiplexing comparator outputs is proposed; this approach is suitable for high-speed operation together with power and area benefits. Fabricated in a 40-nm low-power CMOS technology, the modulator's prototype achieves a 67.3 dB of signal-to-noise and distortion ratio (SNDR), 68 dB of signal-to-noise ratio (SNR), and 68.2 dB of dynamic range (DR) within 50.5 MHz of bandwidth (BW), while consuming 19 mW of total power (P). The proposed modulator features 161.5 dB of figure-of-merit (FOM), defined as FOM = SNDR + 10 log10 (BW/P).

1.3. Dissertaton Organization

The dissertation is organized as follows: Chapter II discusses about different ADC implementation topologies. Chapter III presents a low power digitizer for back-illuminated 3D-stacked CMOS image sensor readout with passing window and double auto-zeroing techniques. Chapter IV presents A 50-MHz BW 67.3-dB SNDR MASH 1-1-1 CT ΔΣ modulator with FIR DAC and EELU quantizer. Chapter V concludes the dissertation.

II. ANALOG-TO-DIGITAL CONVERTER TOPOLOGIES

2.1. Introduction

There are several major types of ADC architectures that could be used for broadband communications. Each type entails different trade-offs among resolution, speed, power and area. Overall, there are two main categories to classify these ADCs according to the ratio between the sampling frequency and signal bandwidth: Nyquist ADCs and Oversampling ADCs. In recent years, Hybrid ADCs combining different stand-alone ADC topologies have shown great potential to achieve better performance for certain application areas.

2.2. Nyquist ADCs

In Nyquist ADCs the sampling frequency is twice the value of the maximum input frequency wanted to be digitized as shown in Fig. 2.1.

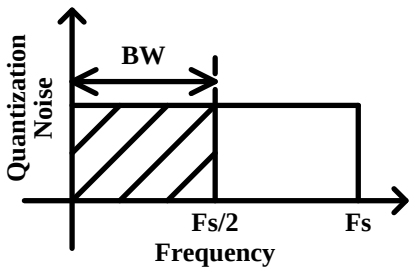


Fig. 2.1. Quantization noise ADC.

There are many different types of Nyquist ADCs that can be used. The most popular ones are, sloping, flash, successive approximation register (SAR), and pipeline ADCs.

2.2.1. Sloping ADC

In a sloping ADC as shown in Fig. 2.2, the voltage signal is first compared with a reference of ramp signal and thus converted into a pulse width signal. The pulse width signal is measured and converted into digital bits through a time-to-digital (TDC) converter. One simple example of TDC is a ripple counter which starts counting at start of the ramp signal and ends when the input voltage crosses with the ramp signal.

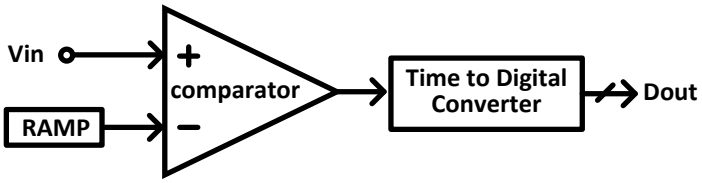


Fig. 2.2. Sloping ADC architecture.

The sloping ADC typically provides benefits of high-resolution and low area. However, the speed of operation is usually low due to the monotonic thermometer code like counting behavior. The worst condition happens when the input signal is full-scale. The counter needs to count up to close to its full-count, which takes time and power. One clear target to address the issue is to lower down the number of counting cycles to complete the conversion process. In [1], a pulse position modulation sloping ADC architecture employing two-step TDC topology is proposed, as shown in Fig. 2.3. The 5

bit course time quantizer, formed using a counter measures the number of reference clock cycles while the counter_enable signal is high, thus measures t_c. The fine TDC measures the time t_f defined as the time between the stop signal and clk_stop rising edges. The timing scheme is shown in Fig. 2.4 and the reference clock frequency is lowered by 16 times to achieve the same time resolution. Another possible solution is to employ a multiple ramp topology [2]. The basic concept of a multi-ramp single slope ADC is that the ramp voltage, which spans the entire input voltage range in the single slope architecture, is divided into m steps, each of which spans 1/m of the input range. The timing operation of the multi-ramp architecture is shown in Fig. 2.5. In the coarse phase, the comparator is connected to a single course ramp voltage, and the first conversion is performed. Next, the coarse conversion result is fed back into the ramp generator to decide the range for the fine conversion range. In the fine conversion, the ramp only has to span 1/m times the ADC input range, and therefore the conversion can be much faster.

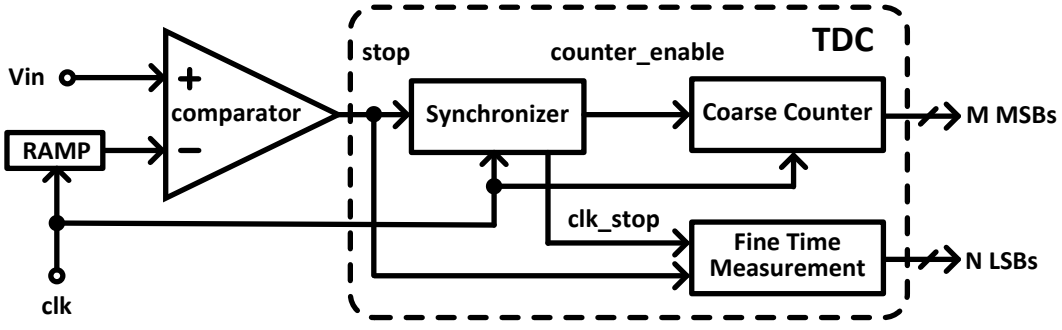


Fig. 2.3. Pulse-position modulation sloping ADC architecture (adapted from [1]).

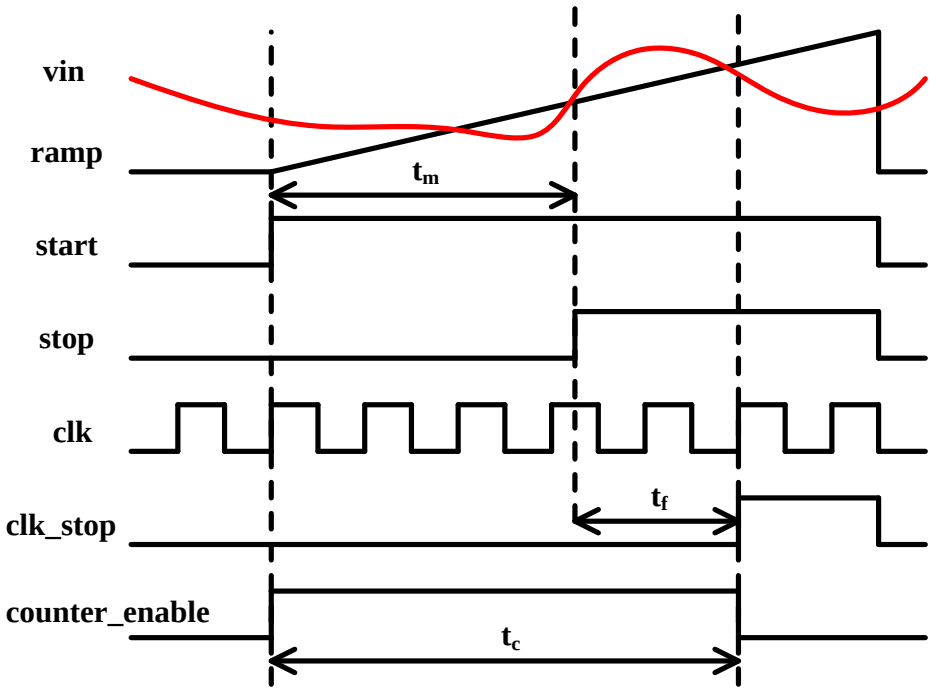


Fig. 2.4. Pulse-position modulation sloping ADC timing scheme (adapted from [1]).

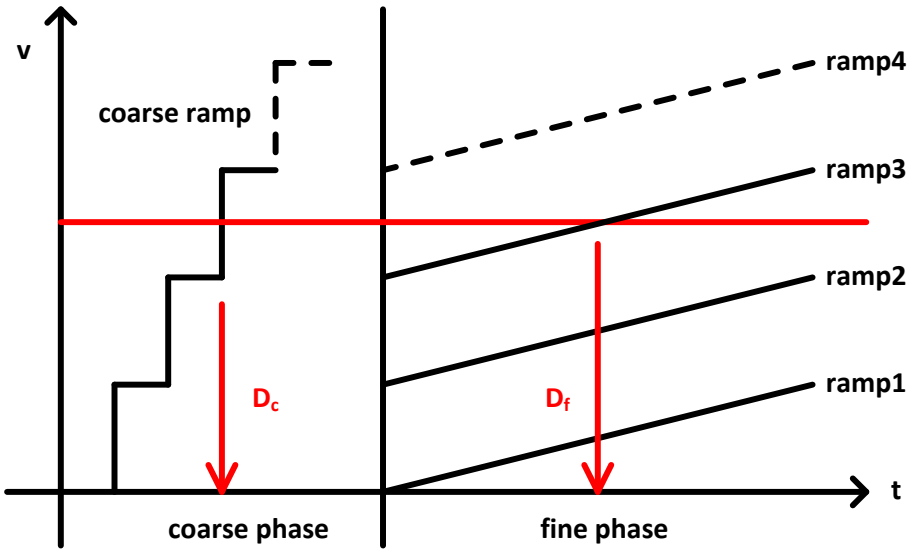


Fig. 2.5. Multi-ramp single-slope ADC timing scheme (adapted from [2]).

2.2.2. Flash ADC

A flash ADC uses parallel comparators to compare the input signal with all transition points between adjacent quantization intervals. The result of these comparisons highlights the limit at which the input is larger than on of the thresholds giving information that can then be transformed into digital codes. The output is obtained in thermometer code, which is typically converted into a binary digital output. Since the comparators operate in parallel, the latency of the output is less than one clock cycle, making this architecture suitable for speeds of several GHz. However, a flash ADC suffers from limited resolution, the number of comparators and references required increases exponentially with the number of bits. For an N-bit flash ADC, (2^N-1) comparators and reference voltages are required as shown in Fig. 2.6.

Also, the offset requirement for the comparators and matching of the references increases exponentially, demanding more area and power consumption making the design of high resolution flash unreliable. Thus, it is not practical to implement a flash ADC with resolution higher than 7 bit.

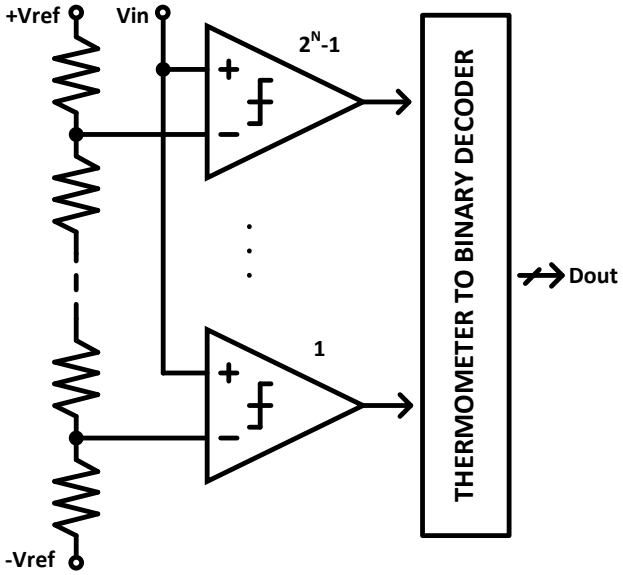


Fig. 2.6. Flash ADC architecture.

2.2.3. SAR ADC

A SAR ADC uses a single comparator to quantize the input signal based on binary search algorithm. As shown in Fig. 2.7, the ADC consists of a comparator, a SAR digital decision logic, and DAC. During the conversion process, the DAC output gradually approaches the input voltage.

SAR ADCs require multiple clock cycles to complete the digital output. For N-bit SAR ADC, N clock cycles are necessary. Therefore, the SAR ADCs are typically slower compared to flash ADCs. The SAR logic adjusts the reference voltage provided the DAC, which defines the resolution of the ADC and is normally implemented by capacitors or resistors. Thus, for high resolution the area of the SAR is dominated by the DAC, which is sized depending on the matching requirements. To achieve high-speed

operation, however, smaller capacitor array is more desirable. Thus, there is a fundamental trade-off between speed and accuracy for SAR ADCs.

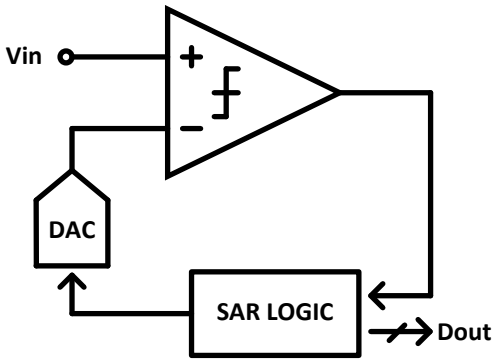


Fig. 2.7. SAR ADC architecture.

The conventional implementation of the SA logic relies on a synchronous clock to divide the time into a signal tracking phase and conversion phase which processes from the MSB to the LSB as shown in Fig. 2.8. Each clock cycle has to tolerate the worst case comparison time, which is composed of maximum DAC settling time and comparator resolving time depending on the minimum resolvable input level. Therefore, the power and speed limitation of a synchronous SAR design come largely from the high-speed internal clock. Using asynchronous processing of the internal comparisons removes the need for such a clock and substantially improves the power efficiency of SAR ADCs. The concept of asynchronous processing is to trigger the internal comparison from MSB to LSB like dominoes [3]. As shown in Fig. 2.9, whenever the current comparison is complete, a ready signal is generated to trigger the next comparison process.

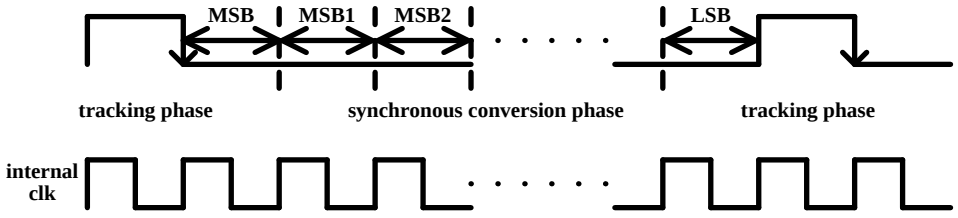


Fig. 2.8. Synchronous conversion for SAR ADCs (adapted from [3]).

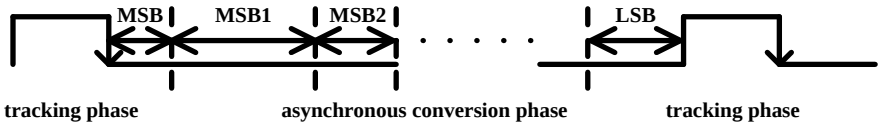


Fig. 2.9. Asynchronous conversion for SAR ADCs (adapted from [3]).

Efforts have also been made in the SAR algorithm to improve its switching energy efficiency and reduce the total capacitance. In [4], a monotonic capacitor switching procedure is proposed as shown in Fig. 2.10. After the sampling switches turn off, the comparator directly performs the first comparison without switching any capacitor. The subsequent switching subsequent switching sequence is also more efficient than the conventional scheme which leads to an average switching energy saving of 81%. However, in the monotonic switching topology the input common-mode gradually converges to ground. Thus a comparator with low sensitivity to the signal-dependent offset caused by the input common-mode voltage variation is demanded.

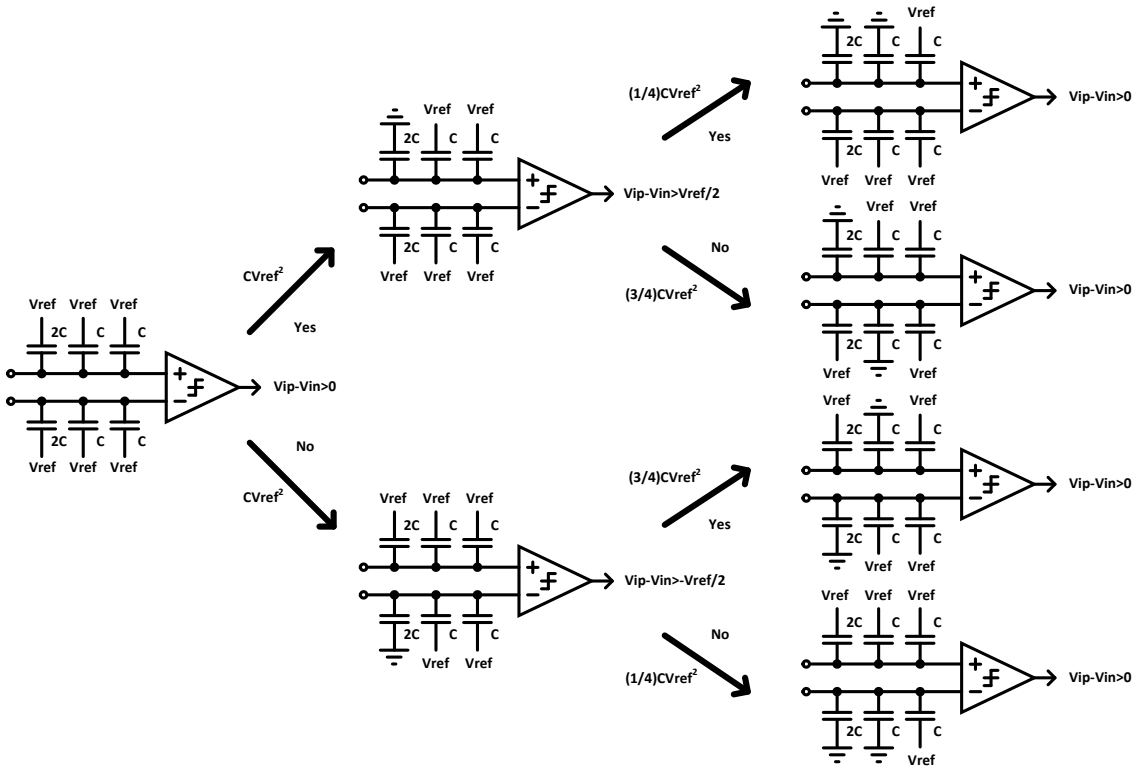


Fig. 2.10. Monotonic capacitor switching procedure (adapted from [4]).

Compared with flash ADC, SAR topology is very attractive for its superior power efficiency. Time interleaving techniques are proposed to speed up the operation of SAR ADCs into GHz Sample/s. In [5], a 10 bit time-interleaved SAR ADC with background time-slew calibration in 40 nm CMOS technology is presented, as shown in Fig. 2.11. The entire interleaved ADC consists of 16 main ADCs and 8 auxiliary ADCs for skew correction, which operate at 1/16 and 1/8 of the sampling frequency, respectively. The reported ADC demonstrates a digital timing-skew correction technique incorporated with a delta-sampling technique, and achieves a 2.6 GHz sampling rate and a wide signal bandwidth up to Nyquist.

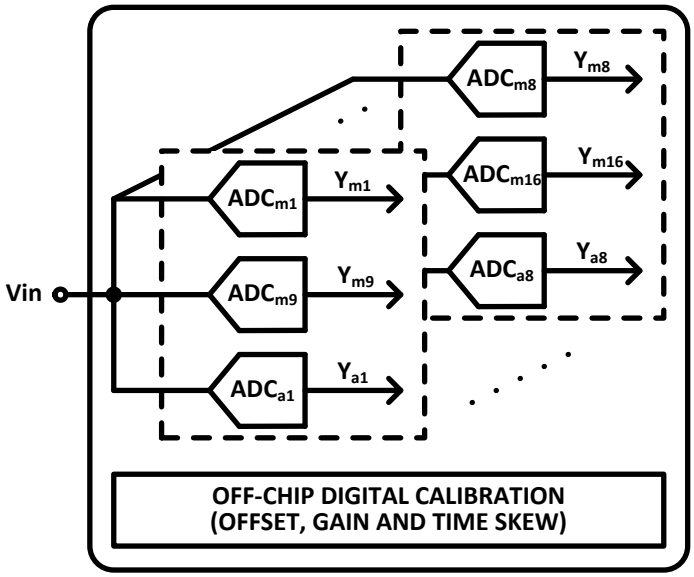


Fig. 2.11. Time-interleaved SAR ADC (adapted from [5]).

2.2.4. Pipeline ADC

A pipeline ADC takes advantage of the speed of a flash ADC, and eliminates the exponential increase in complexity by cascading multiple stages of low resolution flash ADCs. A sample and hold (S&H) function in each stage allows all stages to operate concurrently, giving a throughput of one output sample per clock cycle. Fig. 2.12 shows that besides the sub ADC, a DAC, a subtractor, and an OpAmp are required for each stage.

The operation is described as follow: First, the input signal is quantized by the sub ADC each stage includes a DAC to convert the quantized signal to analog, a residue calculator obtains the difference between the analog input signal and the quantized

signal, then the residue is amplified to adjust the swing for the full-scale of the next stage, the amplified residue becomes the input of the next stage. The process is successively replicated until the last pipelined stage. The number of stages depends on the number of bits solved per stage, and the total number of bits target. Since all pipelined stages work simultaneously, the conversion speed of the pipeline ADC is close to the conversion speed of its single stage. However, since the input signal is quantized successively by the stages, the output has a latency delay equal to the number of stages. The limitation of the pipeline ADC is the high power consumption required for the calculation of the residue. Pipeline ADCs can reach resolution between 8 bit to 12 bits and speeds up to several GHz Sample/s.

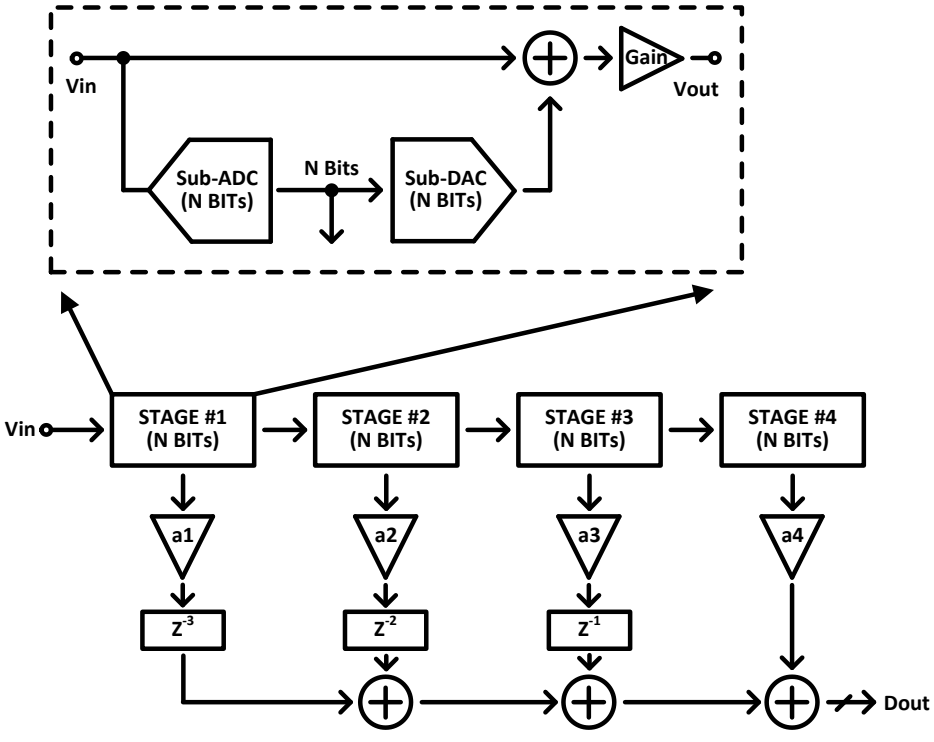


Fig. 2.12. Pipeline ADC architecture.

In early implementations, the resolution of the sub-ADC is typically chosen to be 1.5 bit per stage for two reasons [6]. The first reason in to maximize the bandwidth of the S&H/residue-amp switched capacitor circuit which limits the overall conversion rate. Second, with the use of digital correction algorithm in 1.5 bit per stage pipeline architecture, the overflow of present stage output from the input range of the following stage can be prevented even with the presence of a large comparator offset up to 1/4 of the reference voltage, so that this offset error amplified down the pipeline can be detected for correction.

However, in recent implementations, 3 or 4 bit per stage topology gains more popularity. Compared with 1.5 bit per stage implementations, adding more bits in the first stage leads to less requirement on latter stages and thus results in lower power dissipation overall. However, as the feedback factor for the residue amplifier drops, higher gain-bandwidth product (GBW) is demanded. Thus, precision amplifiers dominate the power consumption in most high-speed pipeline ADCs. In [7], a digital background calibration technique is proposed, enabling to replace precision amplifiers by simple power efficient open-loop stages. In the multibit first stage of a 12-bit 75-MS/s proof-of-concept prototype, 60% residue amplifier power savings over a conventional implementation is achieved.

Pipeline ADC can also be time-interleaved to further improve the operation speed. In [8], a 5.4 GS/s 12 bit two-way interleaved pipeline ADC is presented, as shown in Fig. 2.13. It employs a complementary switched-capacitor amplifier topology to double the GBW without increasing power. The ping-pong amplifier sharing configuration doubles

the sampling rate, whereas the sub DAC equalization digitally corrects the settling error and other dynamic errors in the ping-pong architecture.

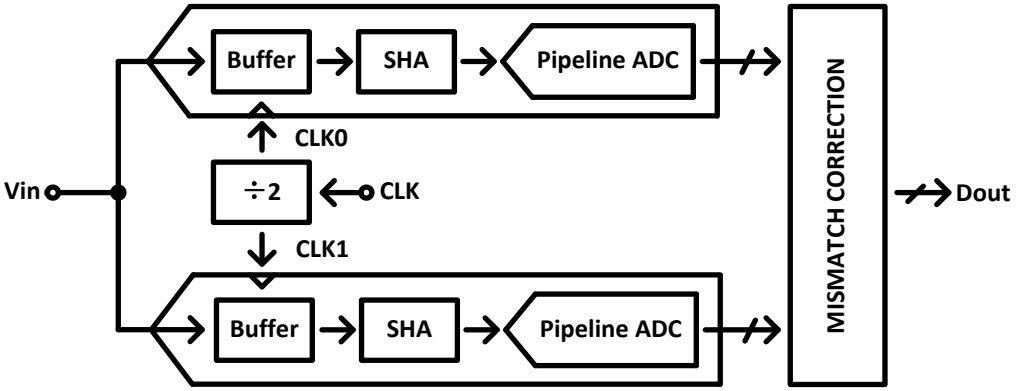


Fig. 2.13. Time-interleaved pipeline ADC architecture (adapted from [8]).

2.3. Oversample ADCs

In oversample ADCs, the bandwidth of the input signal is less than half the bandwidth of the sampling frequency. However, the most widely-used architecture taking good advantage of the oversampling benefit is delta-sigma ADC.

2.3.1. Delta-Sigma ADC

A delta-sigma ADC achieves high resolution by combining the techniques of: oversampling and closed loop noise shaping. Fig. 2.14 shows the basic architecture of a delta-sigma ADC. A delta-sigma modulator consists of a loop filter, a sub ADC, a DAC, and a digital filter.

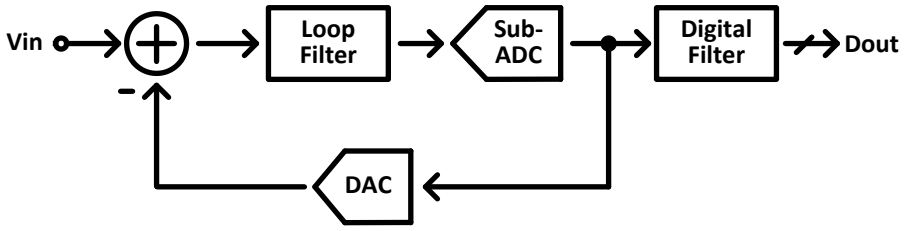


Fig. 2.14. Delta-Sigma ADC.

The effect of oversampling spreads the quantization from the sub ADC over a wider frequency. Therefore, if the oversampling ratio increases the quantization noise inside the desired bandwidth will reduce as shown in Fig. 2.15 (a). Moreover, the quantization noise level inside the desired bandwidth is shaped by the effect of the feedback loop around the sub ADC, such that most of the noise is shifted out of the bandwidth of interest as shown in Fig. 2.15 (b). The former made the delta-sigma ADC a perfect architecture for high resolution applications. However, the speed of the ADC is typically limited comparing with Nyquist ADCs due to the oversample behavior. Nonetheless, advance in process technology has allowed delta-sigma ADCs to reach the hundreds of MHz of bandwidth range, employing continuous-time implementation topologies.

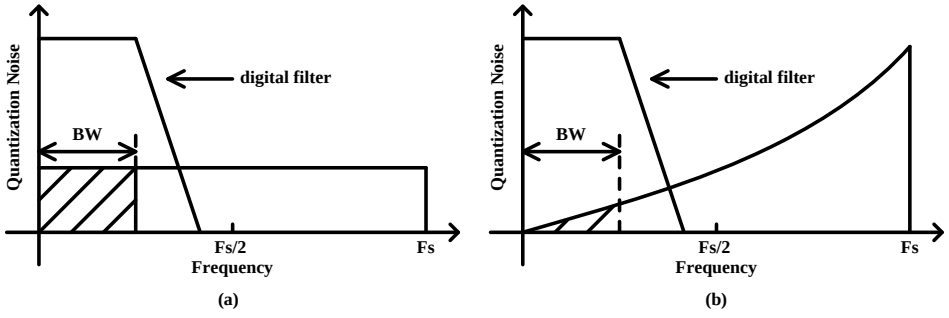


Fig. 2.15. Quantization noise: (a) oversample ADC; (b) delta-sigma ADC.

2.3.2. Discrete-Time Delta-Sigma Modulator (DT-ΔΣM)

In discrete-time delta-sigma modulators, the input voltage is sampled first and then processed by the modulator. Fig. 2.16 shows the block diagram of the second-order discrete-time delta-sigma modulator (ΔΣM). A forward path delay is included in both integrators, thus simplifying the implementation of the modulator with straightforward sampled-data analog circuits. Each integrator is preceded by an attenuation of 0.5, to address the swing issue at the integrator output nodes. The circuit implementation of the ΔΣM employing switch capacitor integrators and a single-bit comparator is shown in Fig. 2.17. The comments on the non-idealities affecting the performance of the DT-ΔΣM are as follows [9]:

a. OFFSET: Offset is minor concern in many signal acquisition systems, as long as the quantization is uniform. The offset at the input of the first integrator is the only significant contributor because offsets in the second stage and comparator are suppressed by the large low-frequency gain of the integrator.
b. SAMPLING JITTER: Oversampled ADC put considerably less stringent requirements on the filter than Nyquist ADCs since the signal is sampled at a frequency far exceeding its bandwidth.
c. NOISE: Noise injected at the modulator input is the dominant source. Input-referred noise from the comparator undergoes the same second-order noise shaping as the quantization noise. The noise sources at the input of the second integrator are subjected to first-order noise shaping behavior. Out-of-band noise

is eliminated by the decimation filter, but high-frequency noise at multiples of the sampling frequency will be aliased in band.

d. INTEGRATOR DC GAIN: The performance penalty incurred is on the order of 1 dB when the integrator dc gain is comparable to the oversampling ratio (OSR).

e. INTEGRATOR BANDWIDTH: Integrator implementations using operational amplifiers (OPAMP) with bandwidths considerably lower than the sampling frequency, thus with correspondingly inaccurate settling, will not impair the ΔΣM performance as long as the settling process is linear.

f. INTEGRATOR SLEW: Slewing distortion appears when the peak rate of change in the impulse response exceeds the maximum slew rate the integrator can support.

g. COMPARATOR HYSTERESIS: The sensitivity of ΔΣMs to comparator hysteresis is several orders of magnitude smaller than that of Nyquist ADCs attributed to the negative feedback with high loop gain topology.

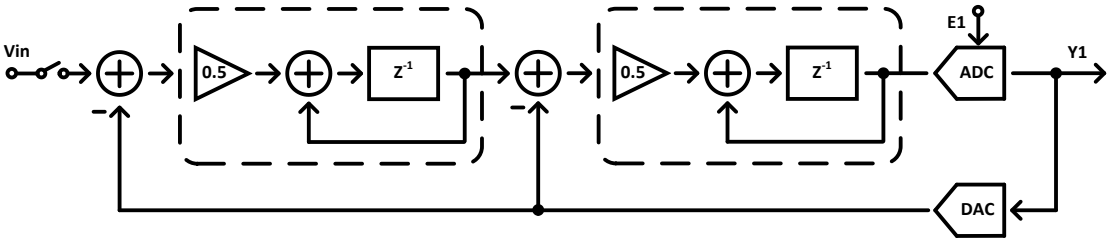


Fig. 2.16. Block diagram of second-order DT-ΔΣM.

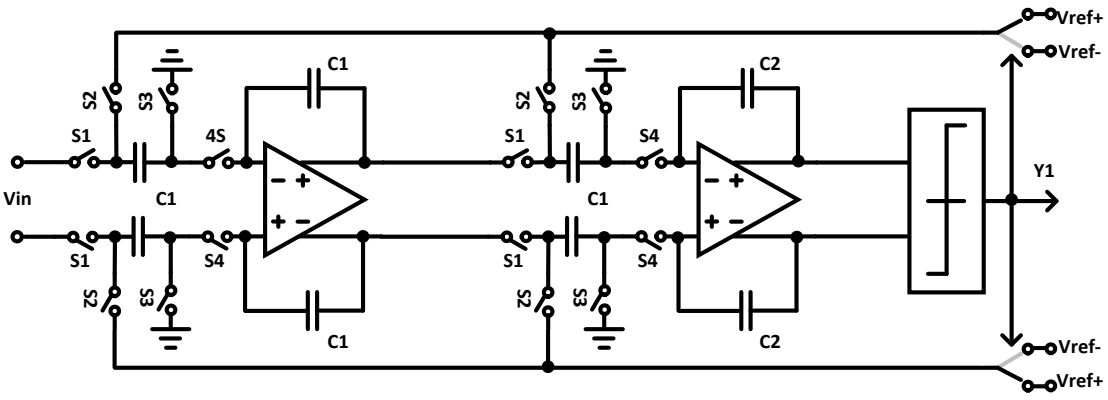


Fig. 2.17. Second-order DT-ΔΣM implementation.

2.3.3. Continuous-Time Delta-Sigma Modulator (CT-ΔΣM)

As mentioned above, in DT-ΔΣMs, high-frequency noise, aliases and blockers at multiples of the sampling frequency will fold in band. However, in CT-ΔΣM, the situation is quite different. The CT-ΔΣM does not demand a dedicated sampler at the ADC input since the loop filter directly process the input signal. The impulse sampling operation occurs at the input of the quantizer after the loop filter. In addition, the feedback path is operating to convert the quantized impulse into time-domain waveforms for integration in the loop filter. A simple example on the analysis of a first order CT-ΔΣM is possible based on the time-domain model shown in Fig. 2.18 (a). By splitting the feedforward path for the signal and the feedback path for the output impulse sequence, the model in Fig. 2.18 (a) can be redrawn as in Fig. 2.18 (b). In the feedback path, based on impulse invariant, it is possible to find z-domain filter H(z) equivalent to the original s-domain paths including the DAC, s-domain loop filter H(s) and the impulse sampler at

the quantizer input. The impulse invariant methodology significantly simplifies the analysis and is widely used in the design of CT-ΔΣMs.

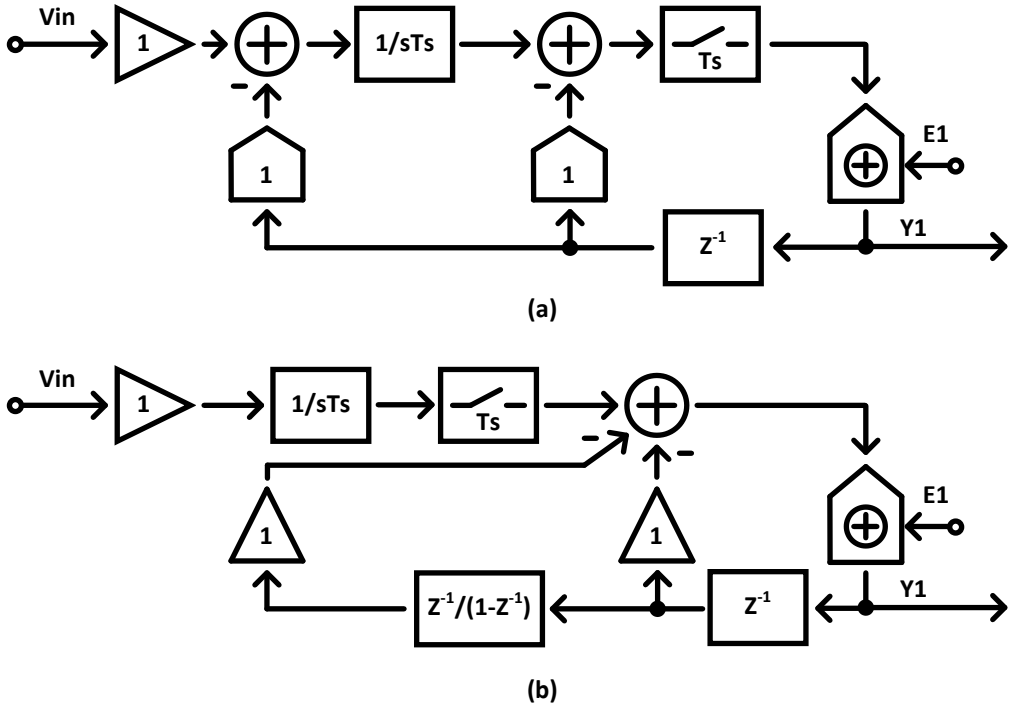


Fig. 2.18. Block diagram of first order CT-ΔΣM: (a) time-domain model; (b) linearized time-domain model splitting signal feedforward and output feedback paths.

Compared to DT-ΔΣMs, the main advantages of CT-ΔΣMs [10] are:

a. Implicit anti-aliasing filter

b. Noise shaping on S&H

c. Possibly higher sampling rate

d. Less digital switching noise

For the reasons above, CT-ΔΣMs are generally more favored in mobile/wireless applications. However, there are still design challenges mainly in the following aspects:

a. Sensitive to clock jitter
b. Sensitive to excessive loop delay (ELD)
c. Sensitive to DAC waveform error
d. Less accurate analog transfer function

2.4. Hybrid ADCs

Different ADC topologies were briefly discussed highlighting their architecture, advantages and issues. Rather than stick to certain fixed ADC topology, designers have the option to break the boundary and combine some of the topologies and techniques to further improve the ADC performance.

2.4.1. Pipelined SAR ADC

SAR ADC architectures are popular for achieving high energy efficiency but they suffer from resolution and speed limitations. On the other hand, pipeline ADC architectures usually achieve high resolution and speed but have lower energy-efficiency. Fig. 2.19 shows one possible combination of the two topologies named pipelined SAR ADC [11]. The flash sub-ADC of a conventional pipeline ADC is replaced by a SAR sub-ADC. The sub-DAC input sampling capacitor array is also utilized by the SAR sub-ADC by connecting a single comparator to the top plate of the input capacitor array. The problem of sampling path mismatch in conventional pipeline ADC is eliminated

because the SAR sub-ADC and the sub-DAC share the same sampling path. The single comparator quantizes the static signal stored on the capacitor array, hence aperture error is also absent. The sub-DAC capacitor array is also used for sampling purpose and there is no need for an active front-end S&H circuit. At the end of the entire successive approximating cycle, the voltage left as the input of the comparator is the residue which needs to be amplified and processed by later stages.

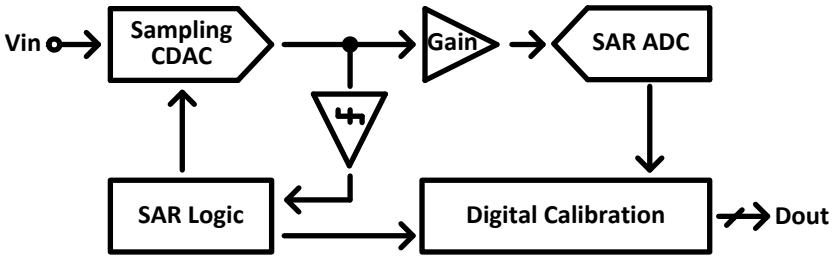


Fig. 2.19. Pipelined SAR ADC (adapted from [11]).

Fig. 2.19 shows a state-of-the-art implementation of a 13 bit 50 MS/s pipelined-SAR ADC in 65 nm CMOS [11], A fully differential ring amplifier with high gain, fast slew based charging and an almost rail-to-rail swing is used for a switched capacitor (SC) inter-stage residue amplifier to achieve accurate amplification without calibration. A floated detect-and-skip (FDAS) witching scheme is introduced to reduce the switching energy loss and improve the linearity of the SAR capacitor DAC. The prototype ADC achieves signal to noise and distortion ratio (SNDR), signal to noise ratio (SNR) of 70.9 dB and 71.3 dB, respectively at Nyquist input frequency.

2.4.2. Noise Shaping SAR ADC

Although SAR ADCs are highly efficient, comparator noise and other effects limit the most efficient operation to below 10 to 12 bit effective number of bits (ENOB). In [12], a noise-shaping concept from ΔΣM is introduced to filter out the in-band noise, as shown in Fig. 2.20. The noise shaping scheme shapes both comparator noise and quantization noise, thereby decoupling comparator noise from ADC performance. The loop filter is comprised of a cascade of a two-tap charge-domain finite impulse response (FIR) filter and infinite impulse response (IIR) based on a low-quality integrator.

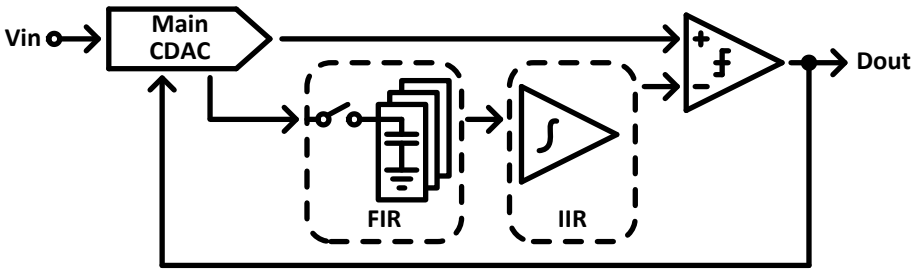


Fig. 2.20. Noise-shaping SAR using FIR and IIR filter (adapted from [12]).

In [13], a similar noise shaping concept together with mismatch error shaping for the capacitor DAC are employed to achieve 105 dB of in-band spurious free dynamic range (SFDR) without calibration, as shown in Fig. 2.21. The prototype incorporates the concepts of flash, SAR and ΔΣM and can be configured into conventional and oversampling modes.

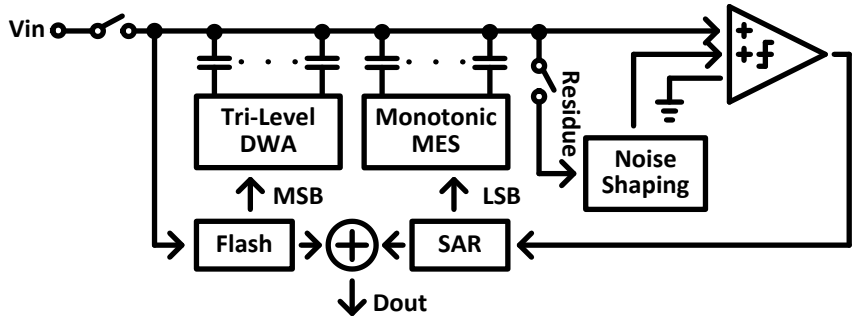


Fig. 2.21. Noise and mismatch shaping SAR with segmented DAC (adapted from [13]).

2.4.3. Delta-Sigma Modulator Employing SAR as Quantizer

Conventionally, flash ADC is typically the choice to implement the quantizer inside of ΔΣM. However, replacing the flash quantizer with an a-synchronous SAR quantizer has shown potential to further improve the power efficiency of CT-ΔΣM [14], [15]. In [14], by using a 6 bit a-synchronous SAR quantizer, the sampling frequency is lowered, which reduces the design efforts both in system level and circuit level as shown in Fig. 2.22. However, as it is not practical to feedback a 64 level DAC signal, a digital delta-sigma truncator is employed to truncate the feedback into only 9 levels. Compared with the same order loop filter without delta-sigma truncation, only 2 dB of 2 dB degradation in in-band noise is noticed.

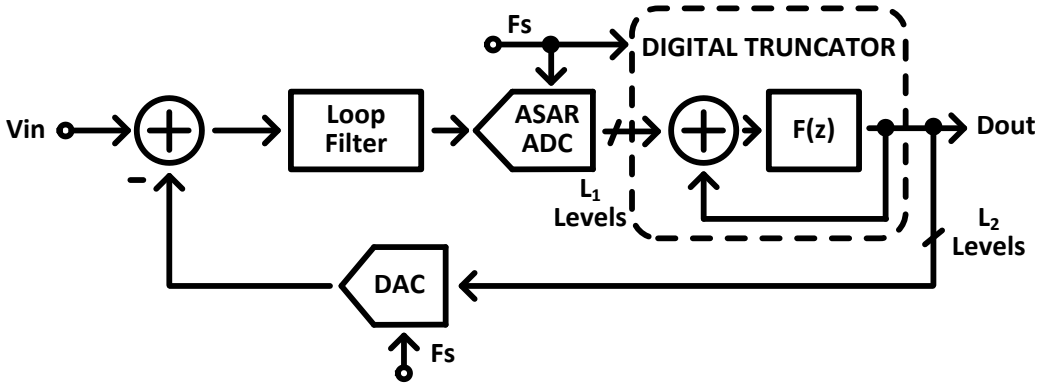


Fig. 2.22. A-synchronous SAR based CT-ΔΣM with digital delta-sigma truncator (adapted from [14]).

The noise shaping SAR concept can also be used to build the quantizer inside a CT-ΔΣM. Fig. 2.23 shows the block diagram of the modulator using a 4th-order feed-forward architecture with a 4-bit asynchronous SAR quantizer [15]. The 2nd-order noise coupling and ELD structures are integrated into the 4-bit asynchronous SAR. Thus, 6th-order of total noise shaping is obtained and the measured SNDR of the CT-ΔΣM is improved from 53.9 dB to 75.3 dB enabling noise coupling and DAC calibration.

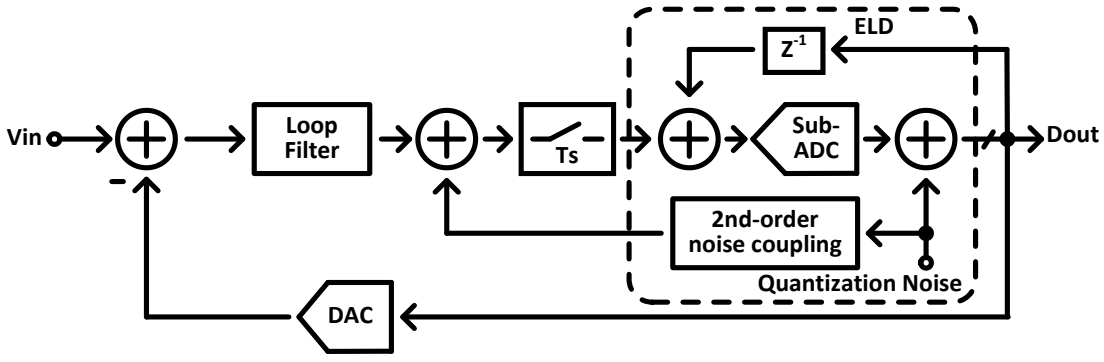


Fig. 2.23. SAR-assisted CT-ΔΣM with 2nd-order noise shaping (adapted from [15]).

2.4.4. Hybrid Delta-Sigma/Pipelined Modulator

Similar to employing a SAR ADC as the quantizer of a ΔΣM, pipeline ADC can also be integrated in a delta-sigma loop and operates as a high-resolution quantizer. In [16], a hybrid delta-sigma/pipelined (HDSP) modulator is presented. The proposed modulator takes advantage of the high resolution and distributed pipelined quantization and combines it with the noise shaping property of a ΔΣM. The latency issue of the pipeline ADC is addressed by adding additional feedback paths from the last stage of the pipeline ADC to its internal nodes as shown in Fig. 2.24. Since the quantizer noise of the pipeline ADC is available in analog form as the residue, it can be used for generating the feedback terms.

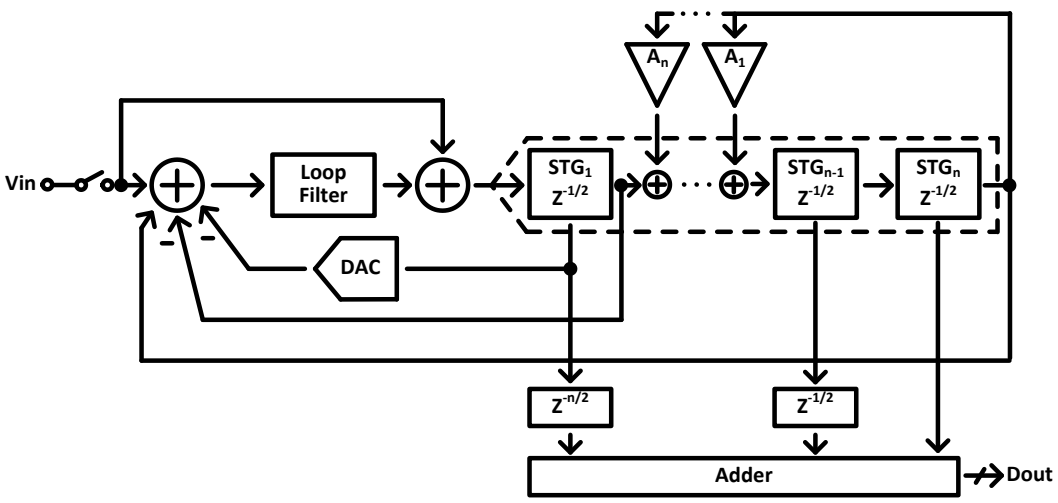


Fig. 2.24. Hybrid delta-sigma/pipelined (HDSP) modulator (adapted from [16]).

2.4.5. 0-N/N-0 MASH Delta-Sigma ADC

Instead of allocating a pipeline ADC as the quantizer of ΔΣM, other topologies by cascading ΔΣM and Nyquist ADC is presented in [17], [18]. There are basically two category of topologies, namely 0-N MASH and N-0 MASH. Fig. 2.25 shows the block diagram of a 0-N MASH concept [17]. The first stage is a zero-order quantizer, while the second stage is an N-th order single-loop ΔΣM with an internal quantizer. The main benefit of 0-N MASH topology is allowing a larger input-signal which results in an improvement in the achievable performance and an enhancement in the modulator efficiency. In addition, its ability to let the ΔΣM process quantization noise only, relaxes the headroom and linearity requirements of its opamps.

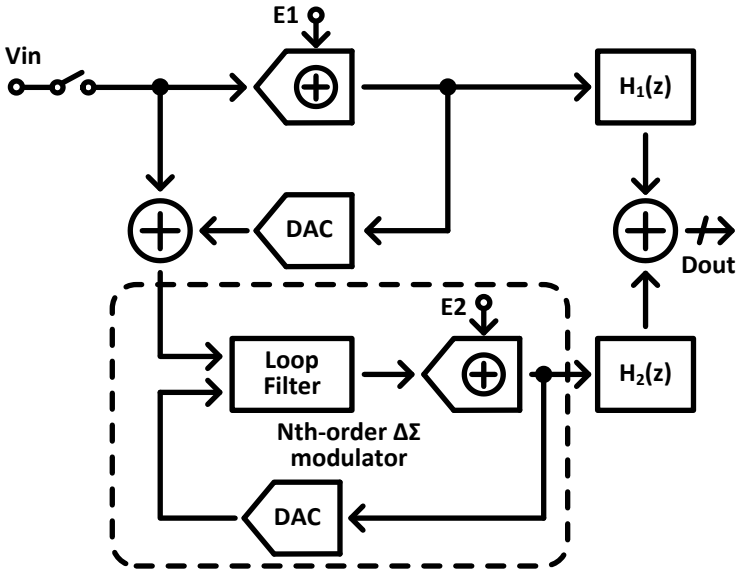


Fig. 2.25. The 0-N MASH ΔΣM concept (adapted from [17]).

Fig. 2.26 shows a 15 MHz 1-0 MASH ΔΣM with nonlinear memory error calibration [18]. A two-tap sequential polynomial derived from an output-referred error analysis accurately models the no-ideality of a first-order ΔΣM. The model parameters are extracted by correlating various moments of the ADC digital output with a one-bit pseudorandom noise (PN) superimposed on the input, largely reducing the circuit overhead associated with the nonlinear calibration. The proposed calibration scheme effectively improves the third-order intermodulation product (IM3) by 30 dB to 87.1 dBc.

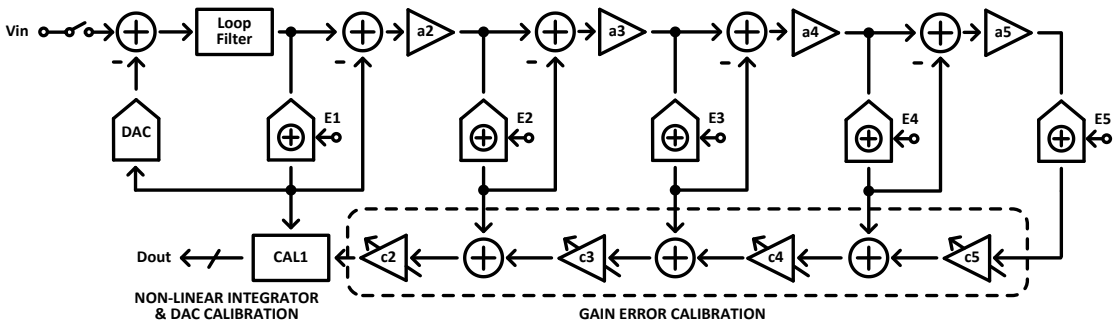


Fig. 2.26. The 1-0 MASH ΔΣM with nonlinear memory error calibration (adapted from [18]).

2.5. Conclusion

In this section, various ADC topologies are visited including both conventional stand-alone ADC and Hybrid ADC topologies. Each type of ADC has its own unique advantage and shortcoming. In image sensing readout applications, implementation based on different ADC topologies, like sloping, SAR, pipeline, pipelined SAR, ΔΣM

and so on, have been reported in literature. In mobile/wireless communication receivers, even though CT-ΔΣM is the current dominant option, there is still fierce competition from other ADC topologies, like SAR, pipeline, pipelined SAR etc. In addition, processing analog signal in the domains other than voltage, like time, charge, and current, also adds more diversity in architectures for the analog-to digital conversion.

III. A LOW POWER DIGITIZER FOR BACK-ILLUMINATED 3D-STACKED CMOS IMAGE SENSOR READOUT WITH PASSING WINDOW AND DOUBLE AUTO-ZEROING TECHNIQUES

3.1. Introduction

Recent innovations on back-illuminated 3D-stacked process for CMOS image sensors [19]–[30] have stimulated a new leap forward in the image sensor industry. The separation of the conventional image sensor process for pixels and the logic process for the readout circuits enables independent performance optimization leading to cost reduction. Instead of sticking to an image sensor process, advanced logic technology nodes are applicable choices for the image sensor digitizer which infers both power and benefits with process scaling.

* Reprinted, with permission, from "A low power digitizer for back-illuminated 3D-stacked CMOS image sensor readout with passing window and double auto-zeroing techniques," Q. Liu, A. Edward, M. Kinyua, E. G. Soenen, and J. Silva-Martinez, IEEE Journal of Solid-State Circuits, accepted in Jan 2017 and to be published.

The most critical building block of an image sensor digitizer is the analog-to-digital converter (ADC). Diverse topologies of ADCs integrated at different levels have been reported targeting high-speed, low-power and area-efficient implementation [19], [22], [28]–[30], [31]–[39]. Binary-search algorithm-based ADCs like cyclic [30], [31], [32] and successive approximation registers (SARs) [35]–[37] are typically faster compared with ramp-based ADCs [19], [21], [28], [29], [38], [39] and oversampling ADCs [33], [34]. However, cyclic ADCs demand amplifiers with precise gain while SAR ADCs require well-matched capacitor digital-to-analog converters (DACs) to achieve high resolution. Forcing cyclic/SAR ADCs into a column-parallel array with a small pixel pitch results in significant layout complexity and column non-uniformity [35]. Furthermore, issues in reference voltage and power supply distribution can degrade far-end ADC performance [37]. Employing a single chip-level pipelined SAR ADC to read out the entire pixel array avoids the area and the analog voltage distribution issues, but the frame rate of the image sensor is limited by the speed of the ADC [36]. Column-parallel oversampling ADCs with noise filtering can achieve low random noise and wide dynamic range, but complicated decimation filters are usually demanded. On the contrary, single-slope ADCs (SS-ADCs), working in column-parallel array and sharing the same ramp signal, have superior fitness for fine-pitch-pixel readout. With only comparators in the analog domain, SS-ADCs benefit from the 3D-stacked process revolution because of their simplicity. Another advantage of an SS-ADC is its good differential non-linearity (DNL) performance without large spikes, which is common problem in cyclic/SAR ADCs [37]. In addition, the digital CDS technique has proven

effective in SS-ADC, resolvisng a number of limiting issues like resetting KT/C noise, pixel and readout FPN, clock skew, and ramp delay [38].

However, employing SS-ADC architecture as a digitizer for CMOS image sensor application comes with two obstacles. A high-speed SS-ADC demands a fast-counting clock, which implies high power consumption in the digital counters lumped to each column [38]. In [29], [39], by sharing a global 5-bit least significant bit (LSB) counter between every 248 columns and put memory cells in columns, the power consumption of the digital counter was reduced. However, if the memory cells in columns are implemented as transparent standard-cell latches [29], the continuous refreshing of the memory cells before the real latching moment will lead to large amount of power waste. Secondly, in the conventional CDS scheme [38], during auto-zeroing (AZ), the offset and delay information stored for cancellation purpose only corresponds to small pixel information levels. Nevertheless, under bright illumination conditions, the input of the comparator [38] crosses at a much lower voltage level which corresponds to a different offset and delay information. For the aforementioned reasons, the digital CDS subtraction introduces a cancelation error, which results in large column fixed pattern noise (FPN) left under bright illumination conditions.

In this paper, passing window (PW) and double auto-zeroing (AZ) techniques are presented to address these two issues. The LSB memory cells in the hybrid digital counters of SS-ADCs are only connected to the global buses during an auto-generated PW. This allows power saving in both LSB memories and global data bus drivers. First attempt of employing double AZ concept to solve bright column FPN was made in this

design. The AZ process of comparator is employed twice during reset and signal readout phase, respectively, such that the comparator operates as a crossing detector only around the same common-mode level. With a double AZ scheme, an effective comparator offset and delay cancelation with digital CDS can be achieved even under bright illumination. Normally dark image column FPN is more visible than bright column FPN. However, as when designers lower down the power supply aiming to save power, the bright column FPN performance gets worse and becomes more noticeable.

The paper is organized as follows: Section II describes the overall architecture of the image sensor chip. Section III describes the proposed PW and double AZ techniques. The circuit-level implementations of the most relevant building blocks of the digitizer are detailed in Section IV. The measurement results are discussed in Section V, and Section VI concludes this paper.

3.2. Sensor Architecture

A typical CMOS image sensor system consists of a pixel array, a digitizer, a row decoder and driver, a timing controller, a phase-locked loop, and a data transfer circuit. In a conventional 2D implementation, the pixel array is arranged at the center of the chip and the peripheral circuits have to be designed using the same process optimized for the pixels. This arrangement limits the performance of the peripheral circuits and degrades the silicon area efficiency. The first commercial product of a back-illuminated 3D-stacked image sensor was reported in [19]. The connection between the interconnect layers between the top and bottom parts was realized with through-silicon vias (TSVs)

outside the pixel array. In [28]–[30], [40], with direct connection of top and bottom wafers with Cu-Cu bonding, the pixel array to chip area ratio is improved because the connection position can be under the pixel array.

Fig. 3.1 (a) shows a back-illuminated 3D-stacked CMOS image sensor with direct interconnection between top and bottom wafers [28]. While the design techniques are eventually targeting at entire multi-megapixel image sensor readout, in this prototype, only 96 columns of readout circuits are implemented as shown in Fig. 3.1 (b), in order to focus on the characterization of the digitizer design. The source followers, together with switches multiplexing between reset voltage and signal voltage, are employed to mimic the pixel operation. No column gain amplifiers are used and the source follower outputs are directly connected to the column SS-ADCs. The main counting 1.7 GHz clock is generated externally and buffered on chip, while both the timing control and the global ramp are generated on chip.

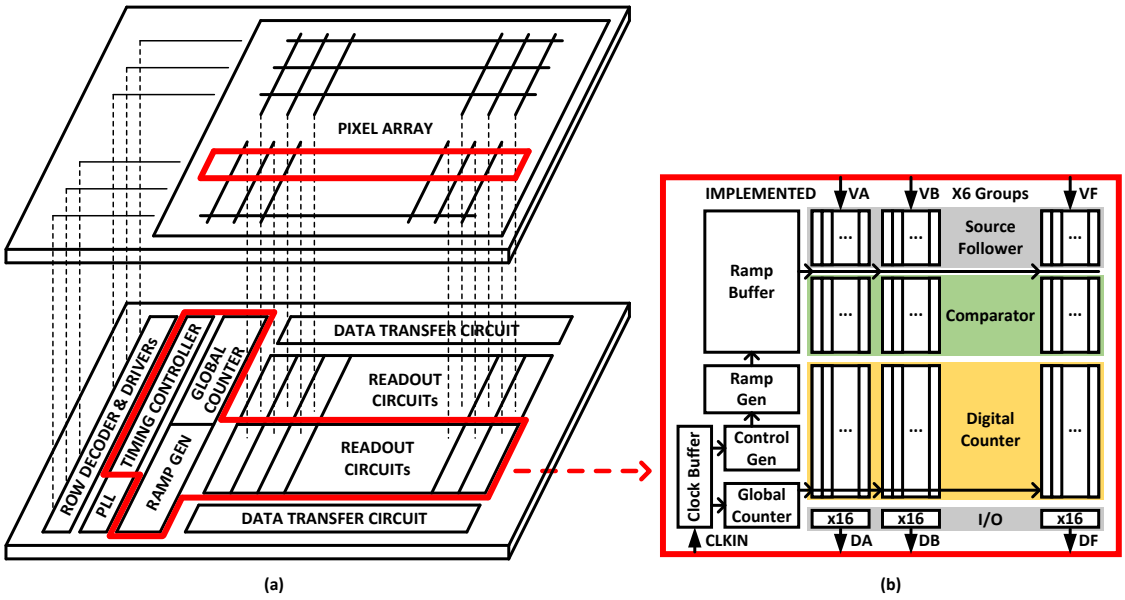


Fig. 3.1. Block diagram of (a) 3D image sensor chip; (b) 96-column digitizer prototype.

3.3. Proposed Techniques

The column-parallel digital counters and comparators are critical blocks for digitizing the analog pixel information level into digital numbers (DNs). The two proposed techniques, passing window (PW) and double auto-zeroing (AZ), are dedicated to improving the performance of digital counters and comparators, respectively.

3.3.1. Passing Window Compatible with CDS

In the conventional SS-ADC, the ripple counter topology [38] is a popular choice for the digital counter. First, the architecture is simple with only a single line of cascaded D-flip flops resulting in an area efficient solution. Second, no synchronization circuits are demanded. Thirdly, a ripple counter capable of doing both up and down counting makes

digital CDS subtraction possible in every column. However, a main issue with ripple counter topology in high-speed SS-ADCs is that the lower-bit D-flip flops are always counting at high frequency until the STOP signal from the comparator is generated.

To address this issue, a hybrid column counter scheme was proposed first in [39]. The digital counter is divided into two parts: 1) a lower 5-bit global counter shared by 248 column memories and 2) an upper 9-bit column-based ripple counter. In this partitioning manner, replacing 5-bit continuous running D-flip flops with memory cells sharing one global counter, power can be saved. However, if the memory cells in columns are implemented as transparent standard-cell latches [29], before the comparator output flips, the high-speed LSB data buses are always refreshing the memory cells. As the comparator output can flip at any time, the memory cells in [29] needs to be connected to the global LSB counter bus all the time before the latching moment. The power needed for charging and discharging the capacitors in the memory cells is wasted, as the relevant counting information is only captured at the latching instant STOP as shown in Fig. 3.2 (a). Only after the latching signal is generated can the memory cells be latched to the data and saved for readout before the next horizontal scan.

Fig. 3.2 (b) shows the improved latching scheme with the proposed PW technique. The PW digital switch disconnects the memory cells from the global data bus during non-relevant timing which not only allows power minimization in the column memories, but also enables power savings due to the lower capacitance driven by the data bus drivers. It is possible to generate a PW based on delaying the comparator output [20] as shown in Fig. 3.2 (b). However, with this method, the real latching moment is also

delayed which introduces a PVT dependent offset and affects the performance of the SS-ADC. In [28], a look-ahead (LA) circuit consisting of a dynamic comparator (D-CMP) and logic in each column together with a globally shared early ramp generator, was proposed to cut unnecessary power consumed by the static comparator (S-CMP) and digital counter. This approach, however, requires complex circuitry. Moreover, the power saved through gating the high-speed clock until decision of D-CMP is limited.

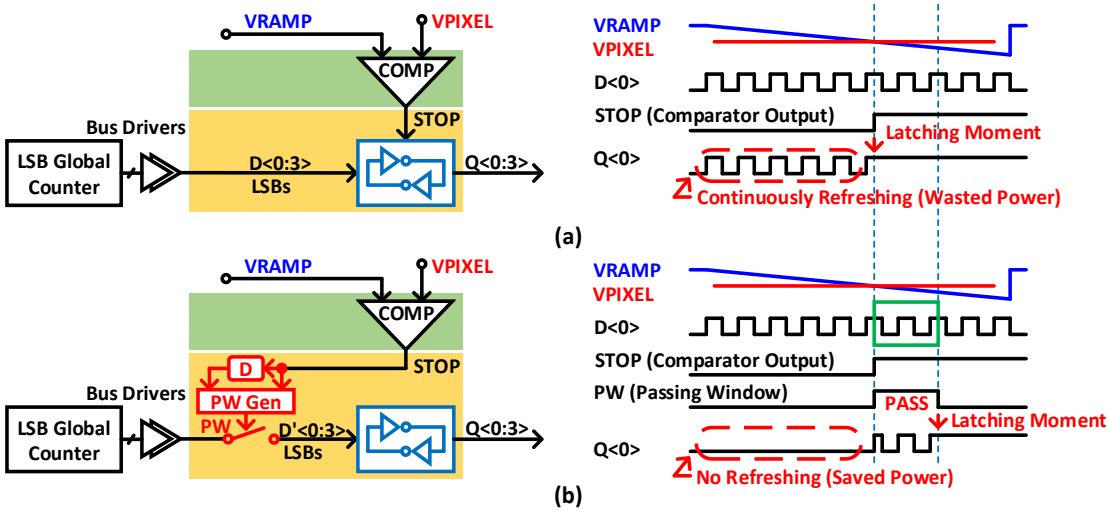


Fig. 3.2. Global counter latching scheme: (a) without passing window; (b) with passing window.

In this design, the hold-and-go counting scheme as defined in [41] is adjusted to generate the PW, which makes the proposed PW technique fully compatible with the digital CDS. Fig. 3.3 (a) and (b) show the proposed CDS timing scheme of the SS-ADC within one horizontal scan under bright and dark illumination condition, respectively. The column-parallel digital counter contains a FLAG generation circuit, a reset counter

and a signal counter composed of LSB memories and a most significant bit (MSB) counter. The conventional digital CDS operation demands the following procedures: 1) Quantize the reset information corresponding to T1 in the reset readout phase (Φ_{rst}); 2) Quantize the signal information corresponding to T3 in the signal readout phase (Φ_{sig}); 3) Subtract the reset information (T1) from the signal information (T3) in the digital domain. In the proposed CDS scheme, by splitting T into T1 and T2, T3 into T and T4, the real pixel information level can be expressed as:

$$\mathrm{Tpixel} = \mathrm{T3} - \mathrm{T1} = (\mathrm{T4} + \mathrm{T}) - (\mathrm{T} - \mathrm{T2}) = \mathrm{T4} + \mathrm{T2} \tag{3.1}$$

where T is the full counting time of the reset counter, T2 is the time left for the reset counter to count to full starting from T1. T4 is defined as the time difference from the moment when the signal counter start counting to the moment when the comparator output flips during Φ_{sig}. Based on this definition, T4 is always equal to $\mathrm{T3} - \mathrm{T}$ and can become negative when T3 < T under dark illumination condition as shown in Fig. 3.3 (b). Thus instead of quantizing T1 and T3 separately, single capture of T4 + T2 in the signal counter is possible following the procedures below:

1) During Φ_{rst}, the reset counter is enabled at the same moment that the ramp starts and stops when VRAMP crosses with VPIXELrst. T1 is then saved on the reset counter.
2) During Φ_{sig}, the signal counter and the LSB global counter start counting time of T later than the start of the ramp. When VRAMP crosses with VPIXELsig, the reset counter resumes counting from saved T1. The PW switches are then closed allowing

the LSB data buses to refresh the LSB memory cells in the signal counter.

3) During Φ_{sig}, the state when the reset counter counts to its full range is detected by the FLAG generation circuit. The generated DATASTOP signal opens the PW switches and disconnects the LSB memory cells from the LSB data buses. As the LSB memory cells are latched, the cascaded MSB counter also stops.

After finishing the procedure above, the targeted digitized pixel information level after CDS corresponding to time T4 + T2 is stored in the signal counter. The real latching moment is defined by the FLAG generation, and time T2 after the comparator output flips. Thus, the PW of T2 is created automatically using the comparator output together with the DATASTOP signal without introducing any additional offset or complex digital circuitry. The PW technique is proposed to save the power spent in driving and refreshing the column memory cells, and thus more effective for bright illumination condition when more time of driving and refreshing is needed before the latching moment. Under dark illumination, if the demanded counting time is smaller than the passing window as the case shown in Fig. 3.3 (b), the power saving benefit of the proposed PW technique is less compared to the case of bright illumination.

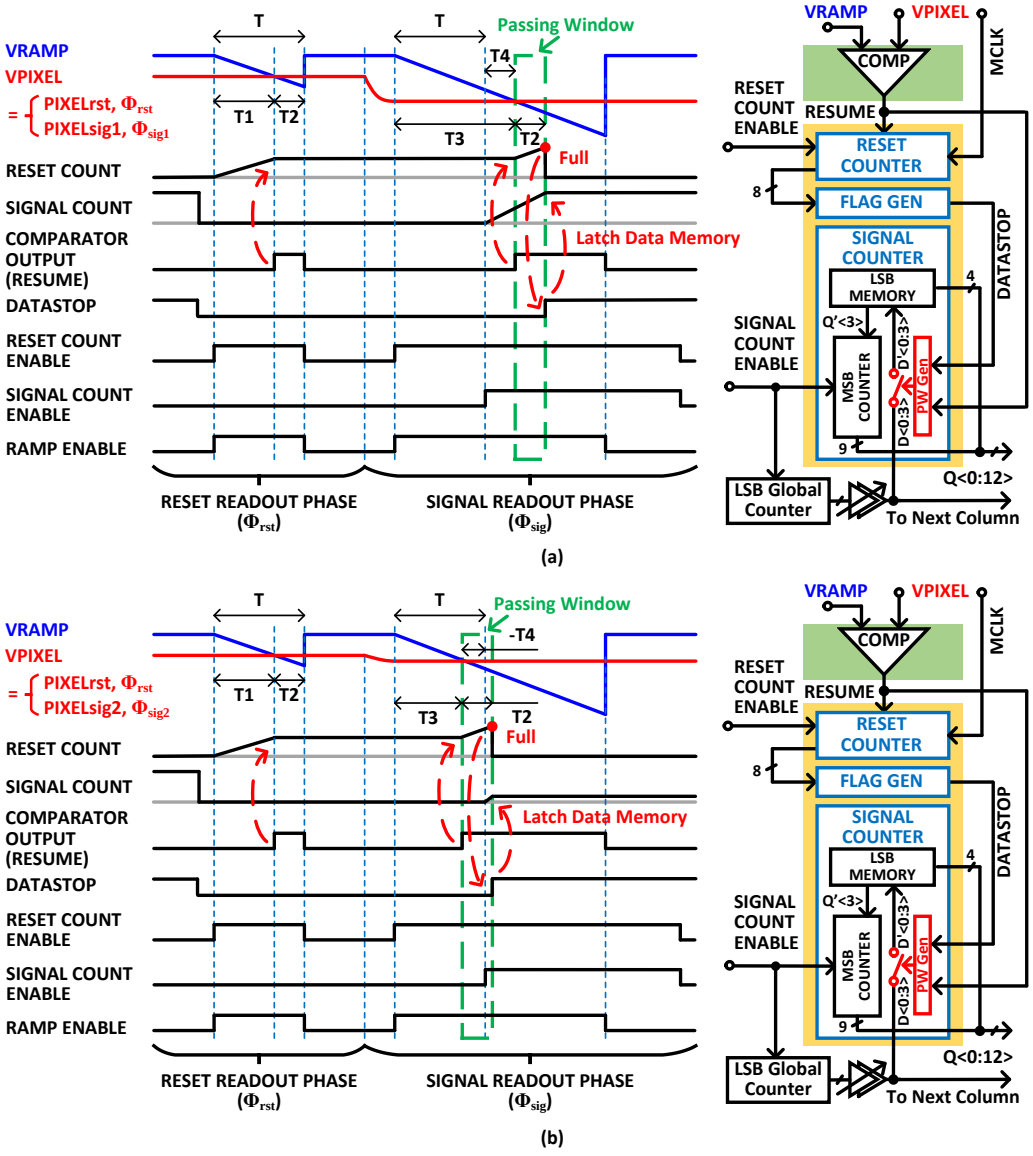


Fig. 3.3. CDS timing scheme for one horizontal scan: (a) under bright illumination condition; (b) under dark illumination condition.

3.3.2. Double Auto-Zeroing

In a conventional CDS scheme, the AZ of the comparator is employed only once in

Φ_{rst} as shown in Fig. 3.4 (a) [38], [42]–[45]. A modified implementation of the comparator in Fig. 3.4 (a) with a fully differential first stage to avoid systematic offset is shown in Fig. 3.4 (b). One critical drawback of the topologies shown in Fig. 3.4 (a) and (b) is that the offset and delay information of the comparator saved in the capacitors for cancellation purpose during Φ_{rst} only corresponds to dark illumination conditions. During Φ_{sig}, the comparator makes the critical decision at very different voltage levels. If the offset and delay of analog comparators vary much with its input voltage crossing level, the conventional CDS scheme is not quite effective, especially under bright illumination conditions, when the difference between pixel reset voltage and pixel signal voltage can be full-scale. The imperfect digital CDS induced cancellation error results in large column fixed pattern noise (FPN) left under bright illumination condition. Even though shot noise and pixel FPN dominate, column FPN can be noticeable to human eyes, especially when the comparator input common-mode range is very limited under low power supply.

Designing a low-power comparator under low supply voltage with a constant offset and constant time delay over the entire pixel information range in the presence of process-voltage-temperature (PVT) variations can be challenging and power demanding. Instead, an improved topology as shown in Fig. 3.4 (c) [29] was proposed to avoid this problem by maintaining the input crossing point of the comparators always at AZ level. However, the charge sharing structure demands well matched capacitor ratios of C1 and C2 among columns to achieve low column FPN. The charge recombination present at node VCP reduces the error signal by 6dB leading to SNR degradation. Finally, even

though a dynamic inverter-based comparator in [29] offers the benefit of simplicity and almost zero static power, the single-ended circuit is very sensitive to substrate and supply noise sources and PVT variations.

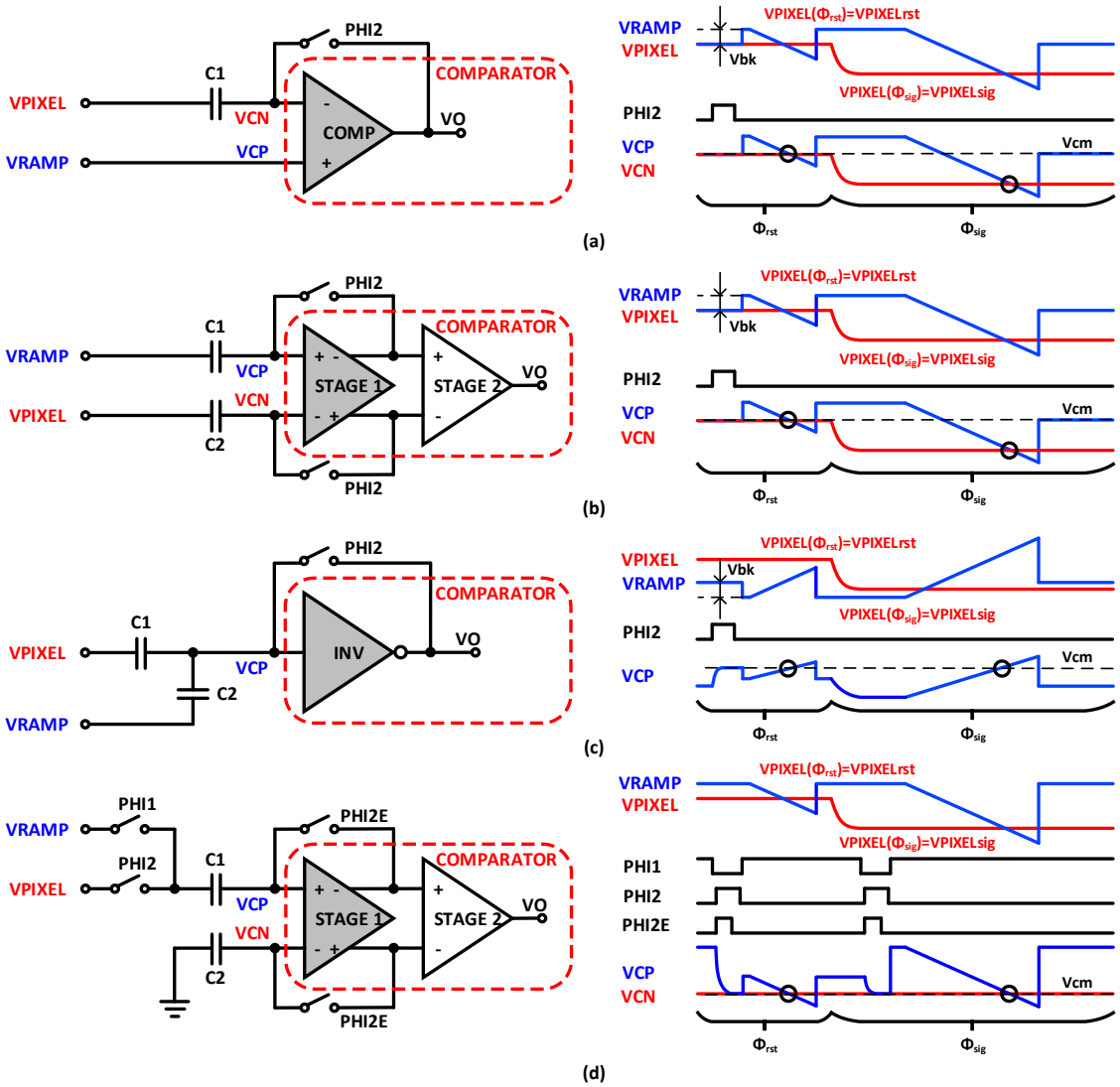


Fig. 3.4. Column comparator topologies.

In the proposed design, a double AZ scheme is employed to resolve the comparator

input crossing point issue while avoiding the additional issues present in the topology as shown in Fig. 3.4 (c). In Fig. 3.4 (d), the AZ process is employed twice, once during Φ_{rst} and the other during Φ_{sig}. During the first AZ phase, the left terminal of C1 is connected to VPIXEL, while the right terminal is connected to common-mode voltage Vcm defined by the comparator with its first stage in unity gain feedback. The voltage across the capacitor, VPIXELrst – Vcm, together with the non-idealities to cancel is saved on C1. After the first AZ phase, the left terminal of C1 is switched to connect to VRAMP. VCP will follow the ramping down of VRAMP until it crosses with Vcm and then the comparator output flips. During the second AZ phase, the procedure is similar to that in the first AZ phase. The only difference is that now the voltage across the capacitor, VPIXELsig – Vcm, together with the non-idealities is saved on C1. After the second AZ phase, the left terminal of C1 is switched to connect to VRAMP, and the comparator output flips again when VCP crosses with Vcm. After digital CDS subtraction, the real pixel information level is VPIXELrst – VPIXELsig with the system non-idealities well cancelled. With this method [46]–[48], the comparator only needs to be optimized around the input common-mode Vcm which accommodates low supply voltage design in advanced technology nodes. The matching of C1 and C2 is less critical since the proposed approach does not rely on charge recombination; however matching is still desirable for PSRR considerations. As the un-correlated sampling noise power gets doubled at final output after subtraction of the two samples converted during Φ_{rst} and Φ_{sig}, respectively, C1 and C2 still needs to be sized large enough based on KT/C noise requirements.

3.4. Circuit Implementation

3.4.1. Pixel Source Follower / Ramp Buffer

To emulate one column of active pixel sensors (APS) in a multi-mega pixel array, a pixel source follower as shown in Fig. 3.5 (a) is built with eight source follower unit cells, a column bias current mirror circuit, together with an additional capacitor of 8 x 64 fF added to mimic the loading from the rest of the source follower unit cells which are not implemented in this prototype. The source follower unit cell consists of a source follower transistor, Nsf, a row selection transistor, Nrow, controlled by ROW<0:7>, and the input selection multiplexer. RST and TX, which are two non-overlapping digital signals that control the transmission gate multiplexer selecting VPIXELrst or VPIXELsig during Φ_{rst} or Φ_{sig} clock phases, respectively. The same topology in Fig. 3.5 (b) enables the global ramp buffer (one for all columns) to track the pixel source follower over PVT and therefore reduce the demanded reset counting range and improve the INL performance of the digitizer. For the global ramp buffer, the multiplexer always passes the RAMP to the gate of Nsf and the same ROW<0:7> controls which source follower unit cell to turn on.

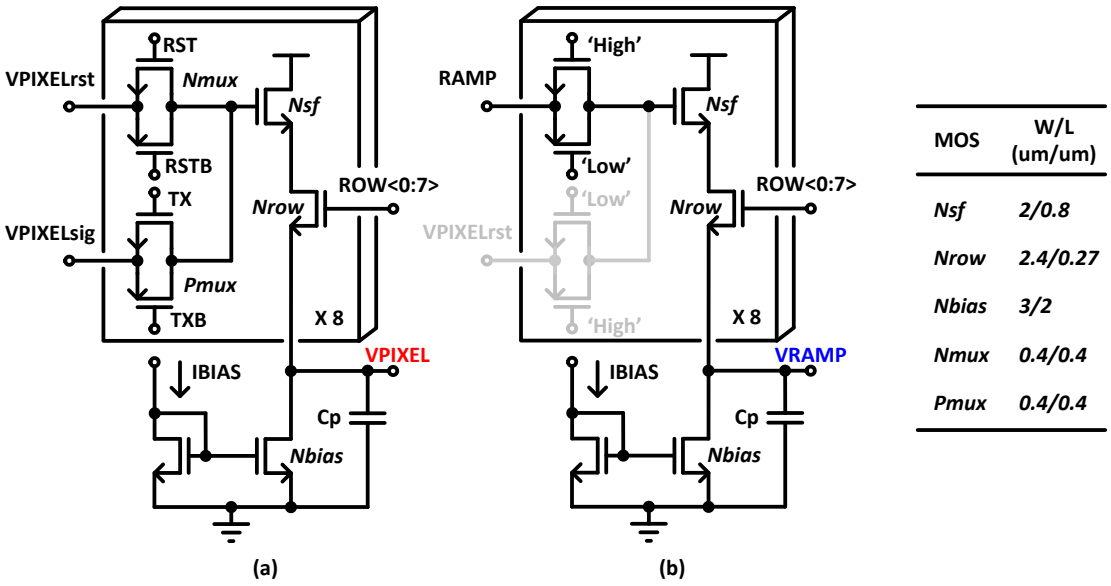


Fig. 3.5. (a) Pixel source follower; (b) Ramp buffer.

3.4.2. PW-based Hybrid Digital Counter

The implementation and timing scheme of the proposed PW-based hybrid digital counter introduced in Fig. 3.3 are detailed in Fig. 3.6 (a) and (b), respectively. The hybrid digital counter is built with a FLAG generation circuit and two counters containing an 8-bit reset counter and a 12-bit signal counter. The signal counter consists of a 4-bit LSB global counter combined with in-column LSB memory cells and 9-bit in-column MSB ripple counters. This segmentation of the signal counter is good enough for power saving considering that the 5th-bit LSB of the conventional counter counts at a low speed that is 1/32 of its 1st-bit LSB counterpart.

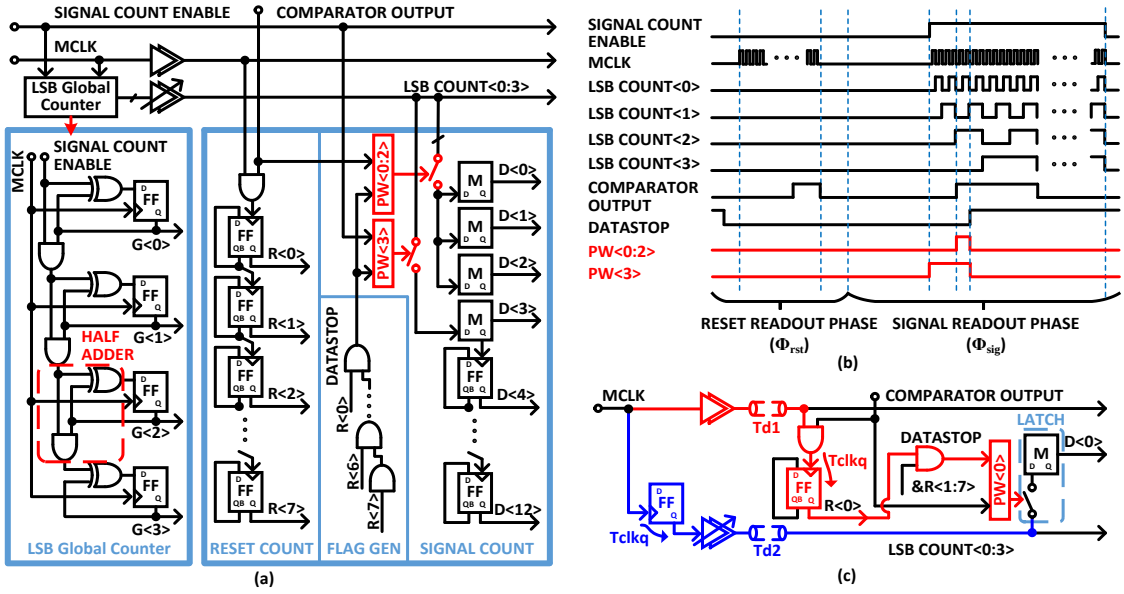


Fig. 3.6. Proposed digital counter: (a) architecture; (b) timing scheme; (c) delay paths.

For the global counter, synchronous grey-code and delay-line based counter topologies are welcomed for their property wherein only a single bit changes from count to count [29], [43]. This feature enables power savings as the frequencies of LSB data buses are lowered. However, the proposed PW technique can push this benefit to its extreme by avoiding all unnecessary data transfer outside of predetermined small PW as shown in Fig. 3.6 (b). In this design, a simple but robust synchronous binary counter based on half-adders and D-flip flops from a standard cell library is employed as the LSB global counter. As shown in Fig. 3.6 (c), DATASTOP is generated using the LSB D-flip flop of the ripple counter which is already synchronized with the master clock (MCLK); hence a power-consuming circuit to synchronize the comparator output is avoided. However, to ensure a proper latching moment of LSB data into memory cells, the delay of the two paths, data signal path in blue and latch signal path in red, still needs

to be properly controlled. The delay of buffers for four LSB data buses is made adjustable to compensate for the delay of the logic circuits which only exists in the red path. In addition, special care has been taken on the 520μm routing of MCLK together with the four LSB data buses to maintain their delay to the same column, Td1 and Td2, close to each other. Multiple global counters are required for readout of a complete multi-mega pixel readout circuits because the delay matching of clock and data buses at different frequencies cannot be guaranteed for long distance routing.

The reset counter is implemented using a ripple counter topology for the benefits explained in Section III. To cover the PVT variations on VPIXELrst, the reset counter needs resolution of 8 bit which corresponds to 2.55 us in time domain with T1 and T2 arranged to be equal. Since the reset counting time T is short (256 cycles), the power consumption is only a small portion of the entire digital counter, unlike the signal counter (4096+256 cycles). Instead of using a latch for its LSB counting [38], the reset counter still employs a D flip-flop for two reasons: 1) it offers better delay matching between the red and blue paths shown in Fig. 3.6 (c); 2) The latch can result in meta-stability issues depending on the comparator output flipping moment [29]. The outputs of the reset counter are sent to a cascading line of AND gates and DATASTOP signal is generated when the counter is at full count.

As shown in Fig. 3.6 (b), PW<0:2> generated using comparator output together with DATASTOP is applied to control the connection of the last 3-bit LSB memory cells in the signal counter to their corresponding data buses. PW<3> for controlling the connection of the 4th-bit LSB memory cell to its data bus needs to be generated based on

SIGNAL COUNT ENABLE and DATASTOP. This is because the memory cell needs to be all transparent to its input until DATASTOP is achieved so as to trigger and stop the column-based MSB ripple counter.

3.4.3. Double AZ Comparator

Fig. 3.7 shows the detailed implementation of the proposed comparator with double AZ scheme introduced in Section III Part B. The topology in Fig. 3.4 (d) is modified by connecting the left terminal of C2 to VPIXEL instead of ground to make the comparator fully symmetrical. Non-overlapping PHI1 and PHI2 controlled dummy switches are added between C2 and VPIXEL to reduce non-idealities introduced by clock feedthrough and charge injection. The first stage of the comparator is implemented using a fully differential topology [41]. During the AZ phase, the comparator in unity gain feedback operates at a nominal common-mode voltage of 0.93 V, which is well-defined by the tail current and diode connected transistors N1-N4. The differential gain of the first stage is around 29.4 dB achieved by the cross-couple transistors N1 and N2. The high gain in the first stage relaxes the offset and noise requirement of the second stage. The first stage consumes 16 μA current from a 2 V analog supply and achieves a bandwidth of around 8.46 MHz, which enables: 1) fast tracking and settling during the AZ phase and 2) small delay variation at different input crossing levels. Since only the first stage with a single pole at output is placed in closed loop during the AZ phase, closed loop stability is not an issue. The second stage possesses a lower bandwidth to help filter out some high frequency noise. The overall gain and bandwidth of the analog

comparator is around 66.7 dB and 3.55 MHz, respectively.

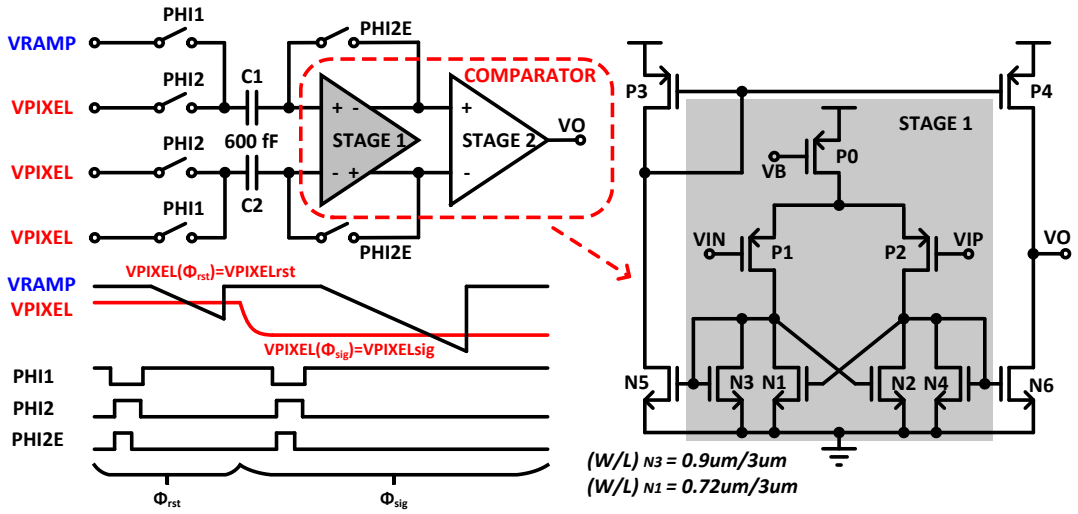


Fig. 3.7. Proposed comparator with double AZ scheme.

To validate the concept of the proposed double AZ method, two test-benches simulating RCCC-extracted view of the transistor level comparator including all components shown in Fig. 3.7 are run under various timing schemes. In the first test-bench shown in Fig. 3.8, the AZ process is done only once for a single readout without CDS. The single AZ happens during Φ_{rst} as shown in Fig. 3.8 (a); thus, the VCP/VCN does not cross at Vcm when realizing comparing the two signals. While in Fig. 3.8 (b), a single AZ is completed during Φ_{sig}, and this time, when decision is made, the VCP/VCN crossing happens at Vcm. As shown in Fig. 3.8 (c), the equivalent column FPN, caused by the comparator delay variations alone under different pixel information levels is characterized based on Monte-Carlo simulations with a global variation model. The column FPN for Fig. 3.8 (a) goes up to 0.83% (33.91 LSB) and 0.34% (14.11 LSB)

under an input signal level of 0.8 V and 0.7 V, respectively. This is caused by the fact that when a very low crossing voltage is applied to the comparator input, the differential pair consisting of P1 and P2 is too close to the triode region. Sample images under bright illumination with 1% pixel FPN, 1.56% shot noise, together with column FPN of 0.83% and 0.34% are shown in Fig. 3.8 (d) and the vertical strips are clearly noticeable. Nevertheless, the column FPN for Fig. 3.8 (b) stays below 3.86LSB throughout the entire input signal range benefiting from the constant VCP/VCN crossing level. The second test-bench introduces the effect of CDS to the first test-bench as shown in Fig. 3.9. In Fig. 3.9 (a), a single AZ is employed in Φ_{rst} and the topology becomes the same as shown in Fig. 3.4 (b); thus, VCP/VCN crosses at Vcm for the reset readout, while remaining at a signal-dependent level for the signal readout. On the contrary, in the proposed double AZ scheme as shown in Fig. 3.9 (b), VCP/VCN always crosses at Vcm. Fig. 3.9(c) shows that the column FPN is improved from 0.65% (26.78 LSB) to 0.004% (0.163 LSB) at the 0.8 V input level using the proposed double AZ method. Sample images in Fig. 3.9 (d) further illustrate the effect of the proposed method in cancelling out the noticeable strips under bright illumination conditions. With the help of CDS, the dark column FPN is improved from around 3.9 LSB to below 0.3 LSB.

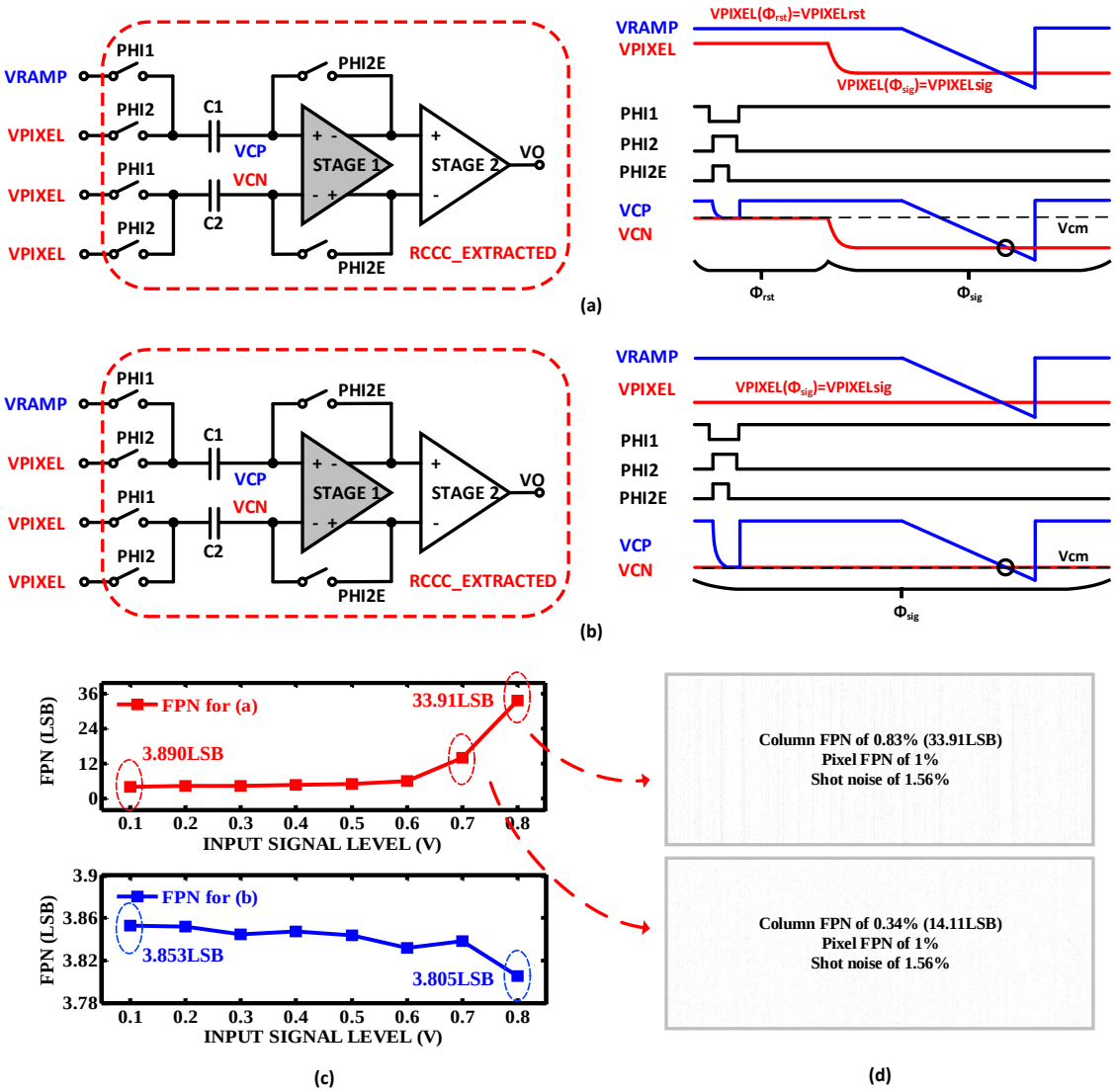


Fig. 3.8. Column FPN caused by comparator delay variations without CDS: (a) VCP/VCN does not cross at comparator common-mode voltage Vcm; (b) VCP/VCN crosses at comparator common-mode voltage Vcm; (c) column FPN under various input signal level for (a) and (b); (d) sample images with column FPN of 0.83% (33.91 LSB) and 0.34% (14.11 LSB) respectively.

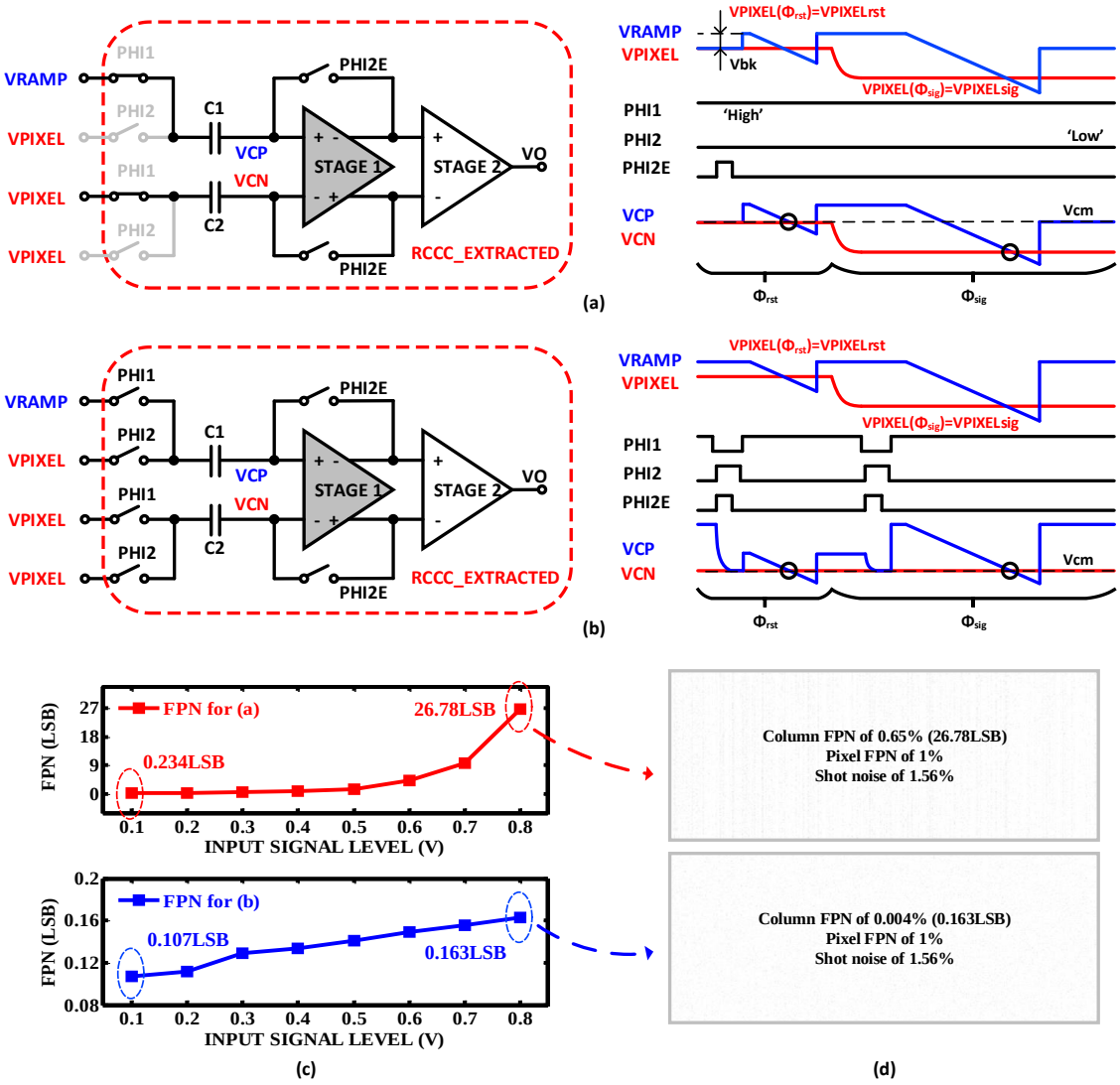


Fig. 3.9. Column FPN caused by comparator delay variations with CDS: (a) VCP/VCN does not cross at comparator common-mode voltage Vcm; (b) VCP/VCN crosses at comparator common-mode voltage Vcm; (c) column FPN under various input signal level for (a) and (b); (d) sample images with column FPN of 0.65% (26.78 LSB) and 0.004% (0.163 LSB) respectively.

3.4.4. Ramp Generator

The ramp generator in this design is implemented using a current-charging-capacitor topology as shown in Fig. 3.10. A switch controlled by the RAMP ENABLE signal is used to pull the RAMP voltage to its top value when necessary. The capacitor is implemented using metal-oxide-metal (MOM) topology for its good linearity performance at the cost of relatively lower area efficiency. The current source is digitally controllable with 4-bit binary-weighted current branches for ± 100% current control to compensate for the slope variations with PVT. The 'High' voltage controlling the differential switches of the current branches is designed to be 1.8 V, so as to achieve high output impedance by cascading three transistors in saturation. A distributed RC filter is needed in front of the gate of the tail transistor in the current branches to filter out the noise from the bias circuitry.

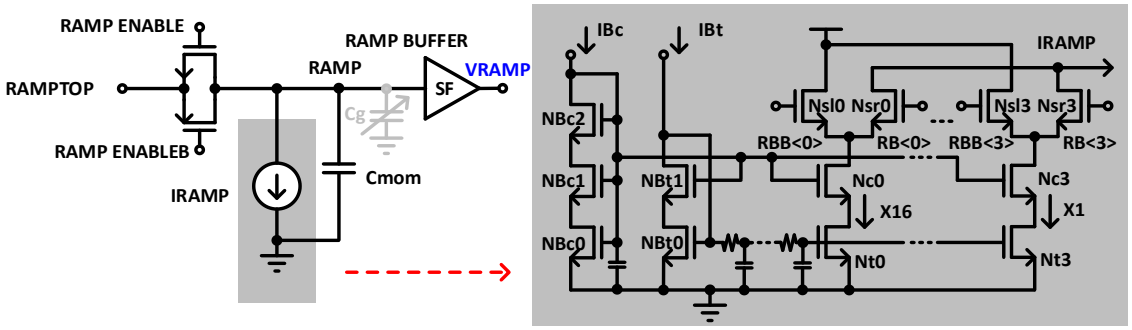


Fig. 3.10. Proposed ramp generator.

3.5. Measurement Results

The image sensor digitizer prototype is fabricated in 40 nm low-power CMOS process, and Fig. 3.11 shows the microphotograph of the chip. The SS-ADC array of the 96-column digitizer is implemented within a column pitch of 5.4 μm and a vertical length of 325 μm and 290 μm for the comparator and digital counter, respectively.

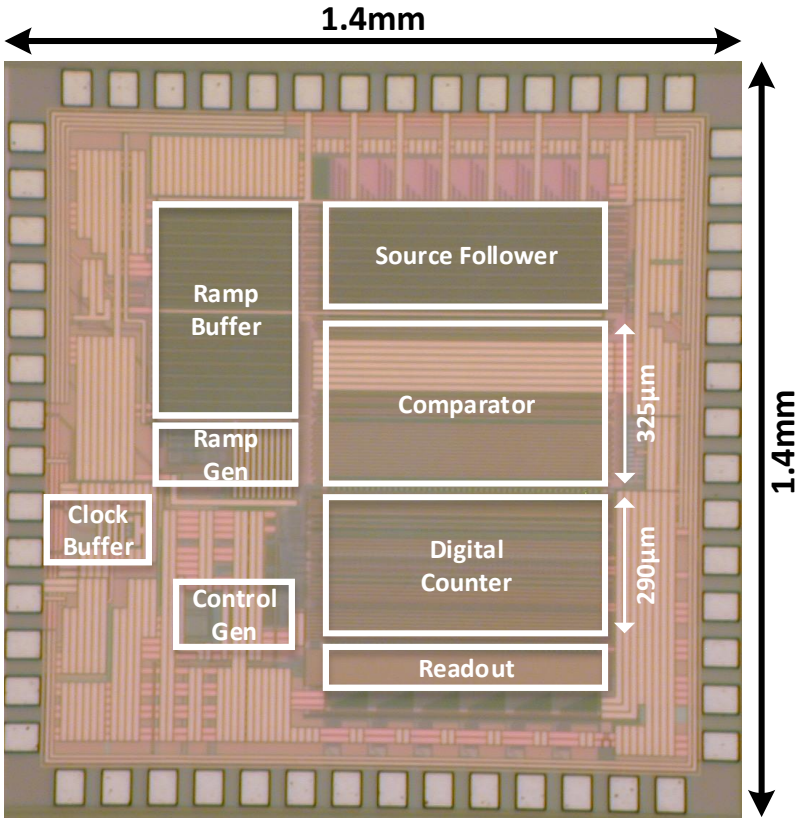


Fig. 3.11. Microphotograph of image sensor digitizer chip.

By emulating active pixels using external voltage sources together with on-chip pixel

source followers and timing control, the entire readout chain including the pixel source follower and the digitizer is tested based on a single die in SS corner at room temperature. One horizontal scan for the 12-bit digitizer is 6.02 μs, while the proposed PW-based hybrid digital counter counts at 1.7 GHz. Even though the double AZ timing scheme is fixed and not possible to bypass it in the implemented prototype, by setting VPIXELrst higher than VRAMP during the entire phase Φ_{rst}, the comparator will not flip and thus the reset read out is disabled. Benefiting from this setup, we are able to get measured data under no CDS condition for comparison purposes.

Fig. 3.12 shows the measured random noise performance of the designed image sensor readout array with and without the proposed CDS scheme, shown in red and blue, respectively. The random noise with CDS scheme is roughly $\sqrt{2}$ times higher than the same condition but without CDS over the entire input signal range, which is attributed to its double sampling behavior. Under a dark illumination condition, the random noise voltages through the entire readout chain are 261.5 μV and 202 μV with and without CDS, respectively. The dynamic range of the readout chain is calculated to be 71.8 dB without any column gain stages under CDS scheme.

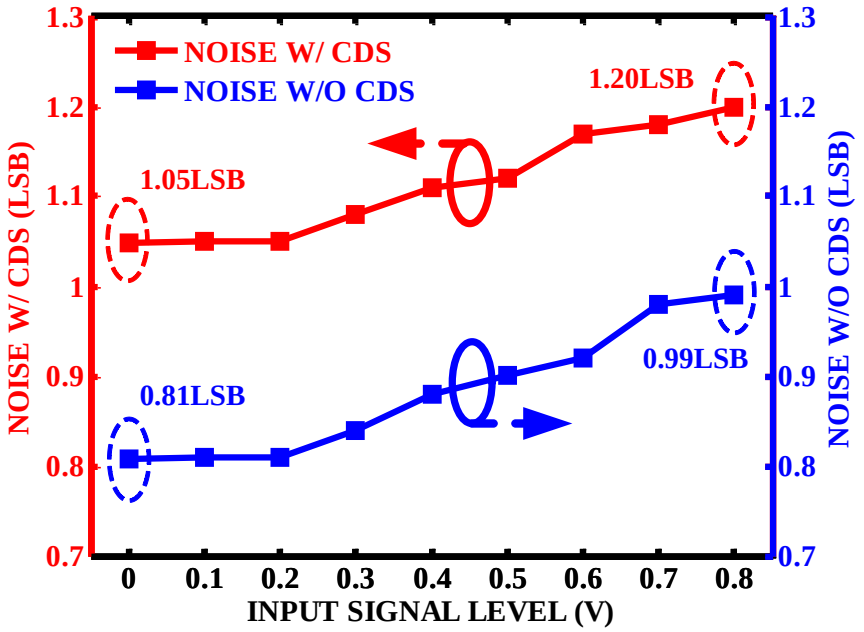


Fig. 3.12. Measured random noise performance.

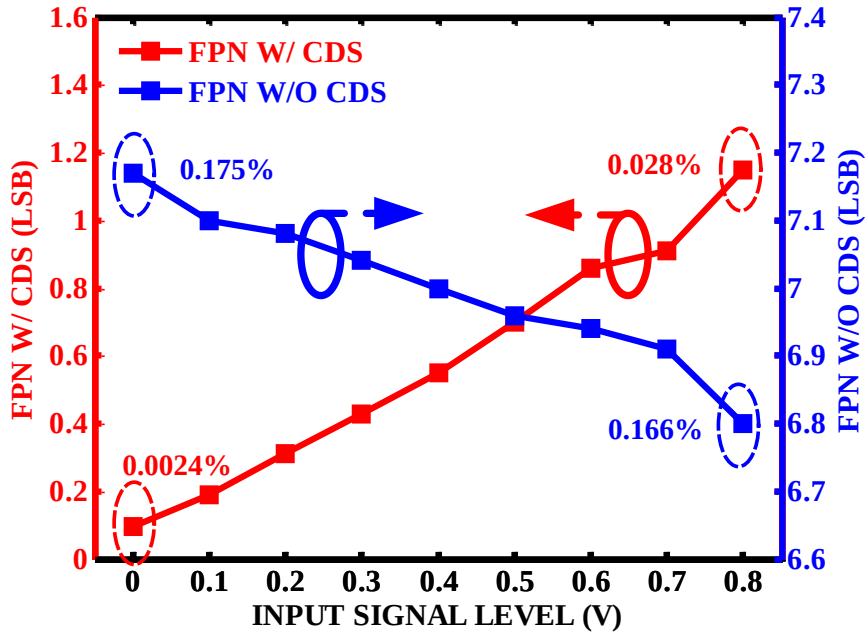


Fig. 3.13. Measured column FPN performance.

Fig. 3.13 shows the measured column FPN performance of the designed image sensor readout array with and without the CDS scheme, shown in red and blue, respectively. In both cases, the crossing happens at the AZ level, and the variation of column FPN with input signal level is very small. Combining the proposed double AZ scheme with the CDS scheme, the dark and bright column FPN performance of 0.0024% and 0.028% is achieved in this design, respectively. Fig. 3.14 (a) and (b) show the DN distribution behavior of the 96 readout chains with a unified input level under dark illumination and bright illumination, respectively. By controlling 'SIGNAL COUNT ENABLE' independently, the design can be improved to tolerate the condition when the image sensor has negative output level due to random noise.

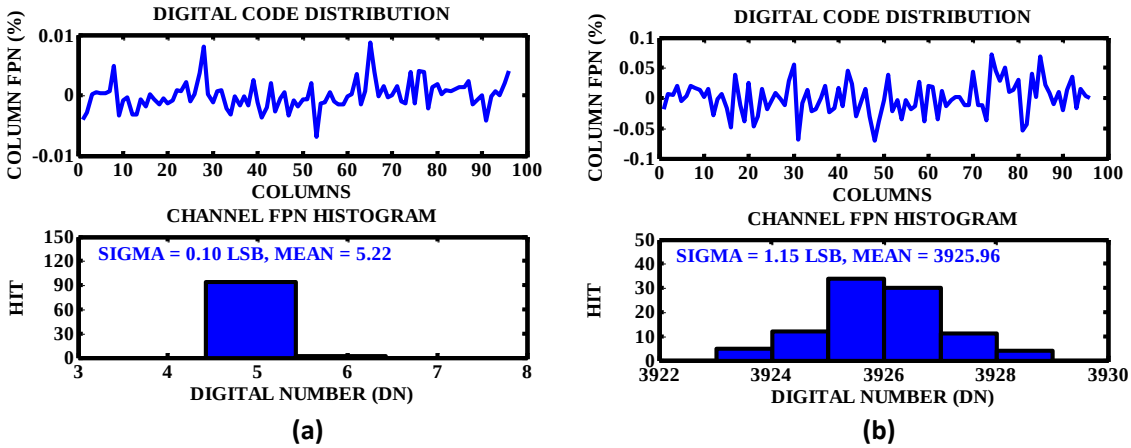


Fig. 3.14. Measured column FPN under condition of (a) dark illumination; (b) bright illumination.

Fig. 3.15 shows the measured linearity performance of the near-end and far-end

column readout chain, shown in red and blue, respectively. The far-end column is expected to be the worst case with DNL and INL of +0.32/–0.28 LSB and +4.21/–0.94 LSB, respectively. The INL performance is believed to be limited by the linearity of the ramp. Even though linear MOM caps are used as the main capacitor for current charging, the non-linear gate capacitance from the ramp buffer degrades the INL performance.

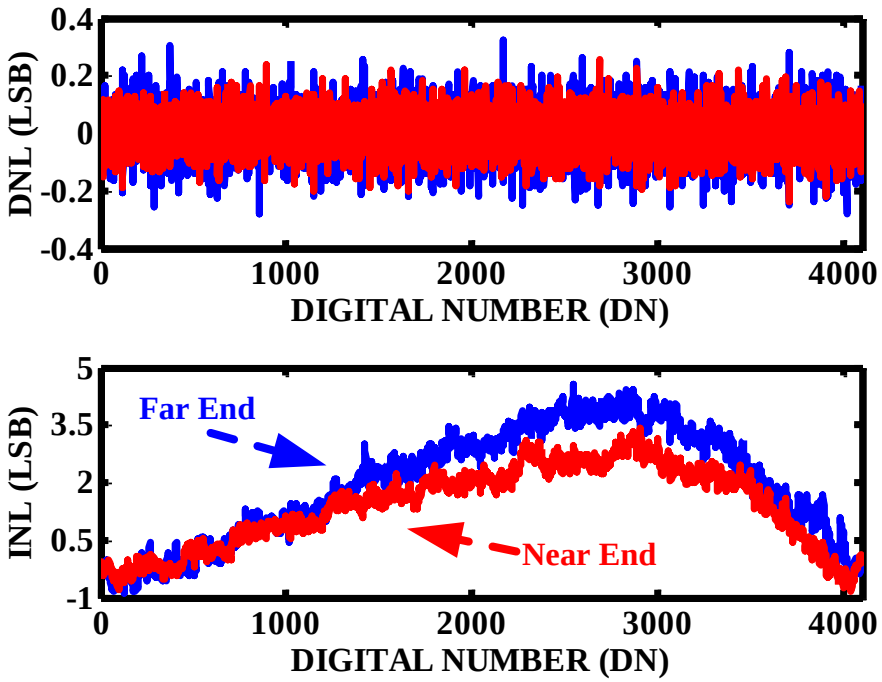


Fig. 3.15. Measured linearity performance.

Fig. 3.16 illustrates the power consumption of the column-parallel digital counter. In the conventional hybrid counter topology [29], [39], the most power demanding component is the signal counter which consumes 23.48 μW under bright illumination

conditions. Nevertheless, with the proposed PW technique, this power can be reduced to 8.88 µW under the same condition. A power saving of 52.8% in the entire hybrid digital counter is obtained using the proposed PW technique without introducing any additional circuitry. As the design is not reconfigurable to disable PW, the detailed comparison of the power consumption of single-column counter with and without PW shown in Fig. 3.16 is based on post-layout simulations scaled to match the measured total power. As there is no dedicated supply for each block, the power consumption values shown for signal counter, reset counter and FLAG GEN are calculated based on their percentage attained from post-layout simulations and measuring the total power consumption of single column counter.

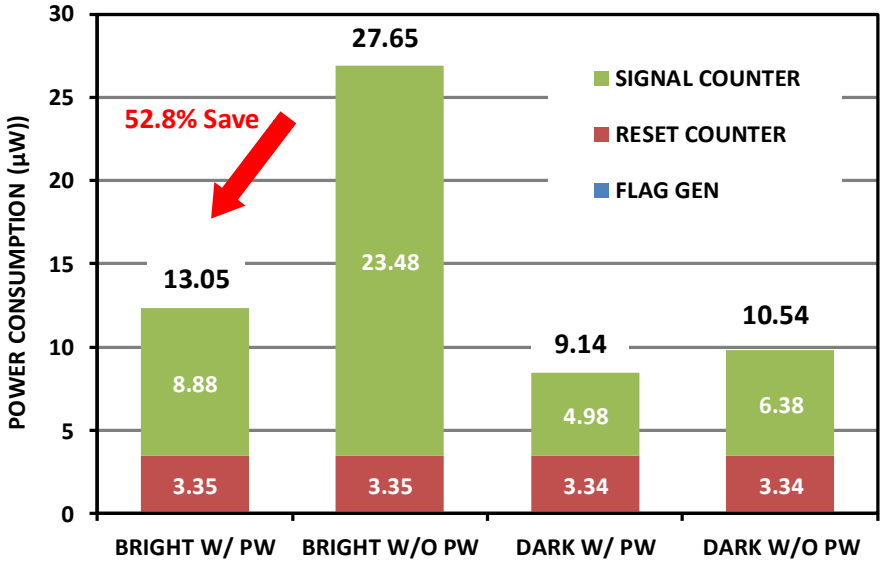


Fig. 3.16. Power consumption of single-column digital counter.

Fig. 3.17 shows the power breakdown of a single-column digitizer with a total power

of 66.8 μW. For the global counter, the ramp and ramp buffer, their equivalent single-column power is calculated by dividing their entire power over the number of columns. In this design, the column comparator power dominates as it is a conservative design still covering a full-scale input signal level range.

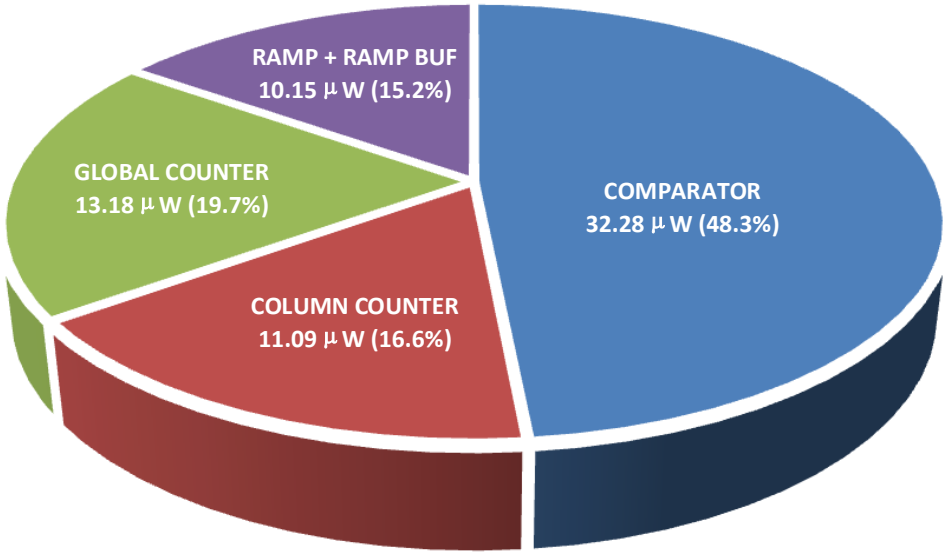


Fig. 3.17. Power breakdown of single-column digitizer.

Table 3.1 summarizes the performance of the implemented image sensor digitizer. Single-column-wise comparison with the state-of-the-art implementations for image sensors can be made even though this design does not include an entire multi-megapixel readout array. For fair comparison purposes, only the ADC power is considered. Compared with the cyclic/SAR ADC based implementations in [30], [32], [37], the proposed design appears to be slower as additional time is needed for completing the digital CDS procedure. Nevertheless, the proposed digitizer achieves high dynamic

range, the lowest per-column power consumption, the smallest area, and competitive Schreier FOM of 162.75 dB.

Table 3.1: Performance summary and comparison with the state of the art

		This Work	[28]	[32]	[37]	[40]
Processs		**40nm CMOS**	65nm CIS/ 65nm CMOS	180nm CIS	180nm CMOS	40nm CIS/ 65nm CMOS
Power Supply		**2.5V/2V/1.1V**	2.5V/1.8V/1.2V	3.3V/1.8V	3.3V/1.8V	2.8V/2.5V/1.2V
Digitizer Topology		**Column-Parallel SS**	Column-Parallel PGA+SS	Column-Parallel CDS+2-Stage-Cyclic	32-Column-Shared CMR+SAR	Column-Parallel CDS+Cyclic-Cyclic-SAR
1 Horizontal Time (T_{1h})		**6.02µsec**	10µsec	1.92µsec	1.85µsec	0.92µsec
ADC Conversion Time		**2.7µsec**	5µsec	1.92µsec	55.7nsec	0.92µsec
ADC Resolution (N)		**12bit**	11bit	12bit	12bit	12bit
ADC Area		**5.4µm x 610µm**	N/A	5.6µm x 1770µm	N/A	4.4µm x 920µm
Digital CDS		**Y**	Y	N	N	N
DNL		**+0.32/-0.28LSB**	N/A	+0.5/-0.7LSB	+6/-1.0LSB	+0.82/-0.88LSB
INL		**+4.21/-0.94LSB**	N/A	+86/0LSB	N/A	+1.04/-11.75LSB
Column FPN		**0.0024%(Dark) 0.037%(Bright)**	N/A	0.31%(Dark) before off-chip calibration	N/A	N/A
Random Noise (V_n)		**261.5µVrms (0dB Gain)**	N/A	320µVrms (0dB Gain)	614.4µVrms (6dB Gain)	414µVrms (0dB Gain)
Dynamic Range (DR)		**71.8dB**	N/A	62.9dB	62.3dB	62.1dB
Per Column Power (P)	Total	**66.8µW**	N/A	161µW	242.1µW	N/A
	Breakdown	**ADC(66.8µW)**	PGA(32.5µW) S-CMP(4µW)	CDS(59.9µW) ADC(101µW)	CMR(134.3µW) ADC(107.8µW)	ADC(120µW)
FoM1[a] [V·pJ]		**0.105**	N/A	0.099	0.275	N/A
FoM2[b] [V·fJ/step]		**0.026**	N/A	0.024	0.134	N/A
FoM3[c] [dB]		**162.75**	N/A	154.9	152.8	N/A

[a] FoM1 = $P \cdot V_n \cdot T_{1h} \cdot 10^{12}$ [V·pJ] (Image Sensor FoM1from [40])

[b] FoM2 = $P \cdot V_n \cdot T_{1h}$ Gain $\cdot 10^{15}/2^N$ [V·fJ/step] (Image Sensor FoM2 from [40])

[c] FoM3 = DR+10log10(1/(2·T_{1h}·P)) [dB] (Schreier ADC FoM3)

3.6. Conclusion

A 66.8 µW-per-column image sensor digitizer based on SS-ADC topology was designed and implemented in a 40 nm low-power CMOS process. The proposed PW technique enables a power saving of 52.8% in the hybrid digital counter, while maintaining the capability of completing digital CDS in column. A dark/bright column FPN of 0.0024%/0.028% from the readout circuit is achieved with the proposed double AZ technique without any off-chip processing. The proposed design achieves low readout noise and a wide dynamic range of 71.8 dB without any column gain stages. The proposed techniques are suitable for readout of back-illuminated 3D-stacked CMOS image sensor pixel array and exportable to other architectures.

IV. A 50-MHZ BW 67.3-DB SNDR MASH 1-1-1 CT ΔΣ MODULATOR WITH FIR DAC AND EELU QUANTIZER IN 40-NM CMOS

4.1. Introduction

In modern LTE-Advanced (LTE-A) receivers, to boost user throughput and increase network capacity, low power (P) wide bandwidth (BW) analog-to-digital converters (ADCs) are in critical demands [49]. The continuous-time delta-sigma modulator (CT-ΔΣM) is the popular architecture of choice for its high dynamic range (DR) capability, implicit anti-aliasing behavior, and tolerance to out-of-band blockers [50]–[71].

State-of-the-art single-loop CT-ΔΣMs are facing design challenges in achieving wide bandwidth and good power efficiency [50]–[63]. In a high-order single-loop ΔΣM, there is no guarantee that it will return to stable operation after an overload experience. This situation can happen when an agile large blocker comes in or near band; detection and reset mechanisms are required for overload recovery. On the other hand, MASH CT-ΔΣMs [64]–[69] offer high-order in-band noise shaping by cascading low-order single-loop CT-ΔΣMs. They have superior stability and overload recovery capability compared to high-order single-loop ΔΣMs. Therefore, MASH ΔΣMs tolerate more out-of-band (OOB) gain, provide more aggressive in-band noise shaping and, thus, present a potential for wider bandwidth and lower power capability. However, the noise cancellation of MASH ΔΣM architecture relies on critical matching between an analog noise transfer function (NTF) and a digitally implemented noise cancelling filter (NCF)

[66].

Most modulators employ a multi-bit quantizer, which provides lower quantization noise level, better stability and superior clock jitter sensitivity performance compared to single-bit quantizer implementation [50], [52], [56]–[71]. However, the power, silicon area and input capacitance of the multi-bit quantizer increase exponentially with the quantizer's number of bits. In addition, it becomes difficult for the multi-bit feedback digital-to-analog converter (DAC) to satisfy the matching requirements especially at high-speed sampling frequencies. The dynamic element matching (DEM) techniques, effective for low-speed high resolution DACs, are not applicable in high sampling-rate modulators because extra delay is no longer tolerable in high-speed feedback paths. In some implementations, higher supply voltage is required to meet the stringent matching requirements [50], [52], [56], [66]–[69]. Look-up table based calibration techniques are proposed in [59]; however, this scheme demands complex digital hardware implementation.

On the other hand, a single-bit modulator topology simplifies the quantizer, DAC and clock generation circuits compared with multi-bit implementations [51], [53]–[55]. A single-bit DAC is inherently linear and no DEM is required, which reduces excess loop delay (ELD) and enables a higher sampling rate [51]. However, there are three critical issues in employing a single-bit DAC in CT-ΔΣM: (1) a single-bit feedback DAC is quite sensitive to clock jitter; (2) the full-scale (FS) swing of the feedback signal in the single-bit case is hard for the operational amplifier (OA) to handle; (3) the OOB gain needs to be restricted for stability consideration.

The concept of employing FIR DAC in a single-bit CT-ΔΣM has already been proposed to address the three critical issues just mentioned [51], [53]–[55]. Thanks to the noise suppression around half the sampling frequency, the FIR logic improves the jitter sensitivity performance of the modulator. The feedback FIR DAC generates multi-level current pulses like those found in multi-bit DAC, which relaxes the requirement on the slew rate of OA in the first integrator. However, directly adding FIR logic introduces additional delay in the feedback path, which affects the original NTF of the modulator and usually degrades the in-band noise performance [53]–[55]. In [51], a single FIR compensation path is provided to the third integrator, whose non-idealities are attenuated by the gain of the previous two integrators. The low-frequency gain of the compensation path is made small, thereby reducing its impact on the in-band signals. However, the poor matching between the FIR logic and the analog-based compensation filter may degrade the compensation and limit the noise-shaping and stability performance of the modulator.

Compared to the previously mentioned single-loop implementation, the MASH CT-ΔΣM topology based on the quantization noise cancellation scheme provides a unique convenience in the NTF compensation for FIR DAC in the feedback path of the modulator's first stage. The degradation in the first stage noise transfer function, NTF1, can usually be tolerated due to its low-order implementation and superior stability compared with single-loop high-order modulators. Simple adjustment in the noise cancellation of the first stage, NCF1, still ensures a solid cancellation of the first stage quantization noise in the end.

In this paper, a low-power wide-bandwidth MASH 1-1-1 CT-ΔΣM is proposed, cascading three first order feedback single-loop CT-ΔΣMs. To address the mismatch issue of multi-bit DAC, a single-current-source 1.5-bit DAC is employed. An FIR filter is added to the DAC in the feedback path to relax the integrator design and improve the jitter sensitivity performance of the modulator. A simple adjustment in the first-stage NCF by adding the same FIR logic maintains the properties of the overall modulator's NTF. Instead of employing a conventional high-speed direct feedback path consisting of an analog summer and a fast DAC, an encoder embedded loop-unrolling (EELU) 1.5-bit quantizer based on multiplexing comparator outputs is proposed. The proposed techniques improve the robustness and power efficiency of the modulator and make the MASH 1-1-1 CT-ΔΣM a potential candidate for the next generation of radio applications.

The paper is organized as follows: Section II describes the overall architecture and system-level design of the proposed MASH 1-1-1 CT-ΔΣM. The circuit-level implementations of the most relevant modulator's building blocks are detailed in Section III. The measurement results are discussed in Section IV, and Section V concludes this paper.

4.2. Modulator Architecture

4.2.1. MASH 1-1-1 CT-ΔΣM Architecture

The architecture of a MASH 1-1-1 CT-ΔΣM including all inter-stage connection possibilities is shown in Fig. 4.1. The modulator is built by cascading three stages of

first-order feedback single-loop CT-ΔΣMs. Each stage is comprised of an integrator, a main feedback DAC, and a loop-unrolling quantizer, aiming to provide first-order noise shaping with zeros placed at dc.

The blocks and connections in blue will be implemented in the digital domain, while those in black remain in the analog domain. The fast feedback path and the summer around the quantizer set to achieve ELD compensation can actually be implemented in the digital domain as part of the proposed EELU quantizer. Therefore, the nodes B1 and B2 become internal digital nodes of the proposed EELU quantizer and are available for inter-stage connection. The FIR filter is added before the main feedback DAC with coefficient k_{11} in the first stage to improve its jitter sensitivity and relax the requirement of the first stage integrator. The FIR logic affects NTF1, and consequently the overall NTF, whose effect is compensated by adjusting NCF1 in the digital domain.

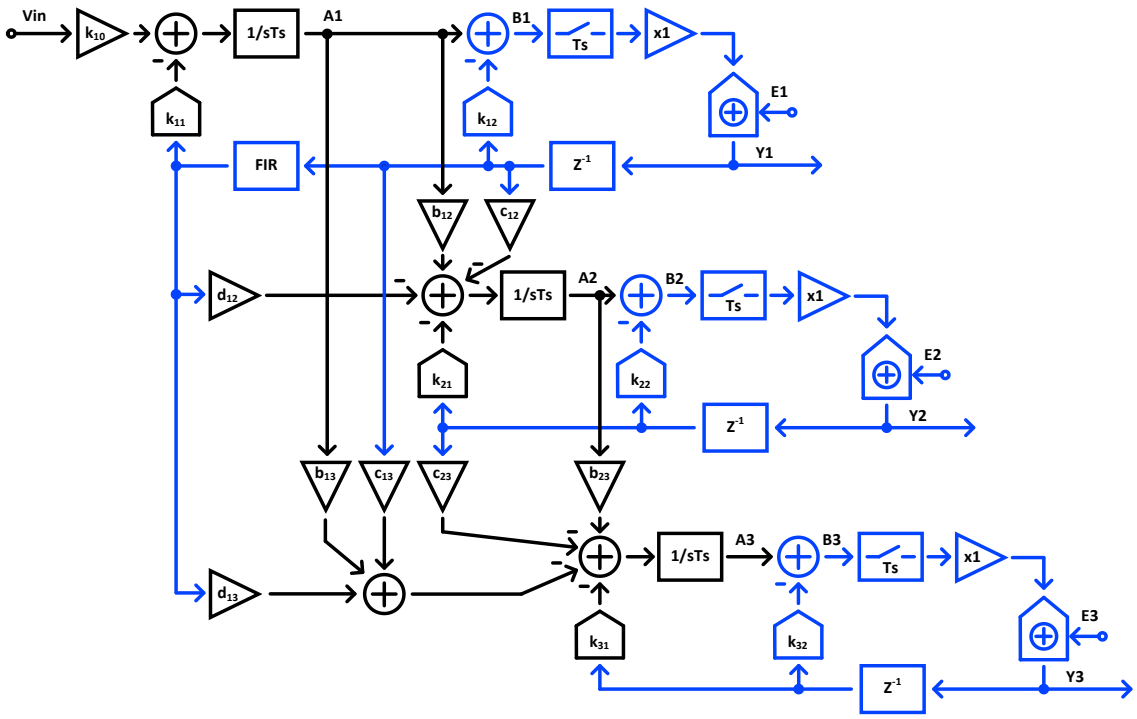


Fig. 4.1. Architecture of a MASH 1-1-1 CT-ΔΣM including all inter-stage connection possibilities.

4.2.2. MASH Coefficient Synthesis and NCF

The MASH 1-1-1 modulator can be analyzed quantitatively employing the impulse invariant transformation. The impulse response of the feedback path going through NRZ DAC, continuous-time filter H(s) and an impulse sampler is equivalent to a discrete-time filter H(z) as shown in Fig. 4.2 [65], [66], [70], [71]. By identifying the three different paths: feed-in path (FF), feed-back path (LG) and connecting path (CLF), and after calculating their equivalent digital equivalent transfer functions, the impulse invariant model of the MASH 1-1-1 modulator with its NCFs can be found as shown in Fig. 4.3

[70]. The derived digital equivalent paths include:

a) Feedback paths:

$$\mathrm{LG1} = k_{11}FIR\left(\frac{z^{-2}}{1-z^{-1}}\right)+k_{12}z^{-1} \tag{4. 2}$$

$$LG2 = k_{21}\left(\frac{z^{-2}}{1-z^{-1}}\right)+k_{22}z^{-1} \tag{4. 3}$$

$$LG3 = k_{31}\left(\frac{z^{-2}}{1-z^{-1}}\right)+k_{32}z^{-1} \tag{4. 4}$$

b) Connecting paths:

$$CLF12 = k_{11}b_{12}FIR\left(\frac{z^{-2}(1+z^{-1})}{2(1-z^{-1})^2}\right)+(c_{12}+d_{12}FIR)\left(\frac{z^{-2}}{1-z^{-1}}\right) \tag{4. 5}$$

$$\begin{aligned} CLF13 = {} & k_{11}b_{12}b_{23}FIR\left(\frac{z^{-2}(1+4z^{-1}+z^{-2})}{6(1-z^{-1})^3}\right) \\ & +b_{23}(c_{12}+d_{12}FIR)\left(\frac{z^{-2}(1+z^{-1})}{2(1-z^{-1})^2}\right) \\ & +k_{11}b_{13}FIR\left(\frac{z^{-2}(1+z^{-1})}{2(1-z^{-1})^2}\right) \\ & +(c_{13}+d_{13}FIR)\left(\frac{z^{-2}}{1-z^{-1}}\right) \end{aligned} \tag{4. 6}$$

$$CLF23 = k_{21}b_{23}\left(\frac{z^{-2}(1+z^{-1})}{2(1-z^{-1})^2}\right)+c_{23}\left(\frac{z^{-2}}{1-z^{-1}}\right) \tag{4. 7}$$

To achieve the targeted overall NTF of the modulator, $\mathrm{NTF} = (1-\mathrm{z}^{-1})^3$, the third

stage noise-cancelling filter is implemented as:

$$\mathrm{NCF3} = (1 - \mathrm{z}^{-1})^2 \tag{4. 8}$$

The quantization noise of the first two stages needs to be completely cancelled, which means:

$$\mathrm{NTF(E2 \rightarrow Y2)\ NCF2 + NTF(E2 \rightarrow Y3)\ NCF3} = 0 \tag{4. 9}$$

$$\mathrm{NTF(E1 \rightarrow Y1)\ NCF1 + NTF(E1 \rightarrow Y3)\ NCF3} = 0 \tag{4. 10}$$

Thus, the expression of the NCFs can be computed as:

$$\mathrm{NCF2} = (1 - \mathrm{z}^{-1})[\left(\mathrm{c}_{23} + \frac{1}{2}k_{21}b_{23}\right)z^{-2} + (-c_{23} + \frac{1}{2}k_{21}b_{23})z^{-3}] \tag{4. 11}$$

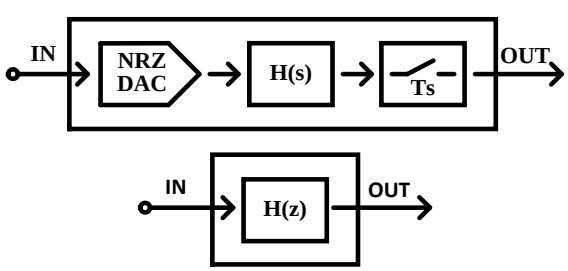
$$\begin{aligned} NCF1 = (1 - z^{-1})^3\{&k_{11}b_{12}b_{23}FIR\frac{z^{-2}(1 + 4z^{-1} + z^{-2})}{6(1 - z^{-1})^3} \\ &+[(k_{11}b_{13} + d_{12}b_{23})FIR + c_{12}b_{23}]\frac{z^{-2}(1 + z^{-1})}{2(1 - z^{-1})^2} \\ &+(d_{13}FIR + c_{13})\frac{z^{-2}}{1 - z^{-1}}\} \end{aligned} \tag{4. 12}$$

For this design, the coefficients c_{12}, c_{13} and b_{13} are set to zero. Special care is needed on the inter-stage gain coefficients considering the output swing of the integrators. The other coefficients are computed to simplify the NCFs and provide first-order noise

shaping with zeros placed at dc in each individual stage. The updated topology of the proposed MASH 1-1-1 CT-ΔΣM is shown in Fig. 4.4 and its coefficients are listed in Group I of Table 4.1. Fig. 4.5 shows the schematic of the NCFs of the proposed modulator, which is simple and easy to implement in digital domain. The FIR filter is as simple as a 4-tap delay averaging logic [53].

Table 4.1: Coefficients for the proposed MASH 1-1-1 CT-ΔΣM

Coefficients	a	g	k_{10}	k_{11}	k_{12}	k_{21}	k_{22}	k_{31}	k_{32}	b_{12}	b_{23}	c_{23}	d_{12}	d_{13}
Group I	1	1	1	1	1	1	1	1	1	1/2	3/4	3/8	1/2	1/8
Group II	**1/2**	2	**1/2**	1	**1/2**	1	**1/2**	1	**1/2**	**1**	**3/2**	3/8	1/2	**0**



$H(s)$	$\frac{1}{sTs}$	$(\frac{1}{sTs})^2$	$(\frac{1}{sTs})^3$
$H(z)$	$\frac{z^{-1}}{1-z^{-1}}$	$\frac{z^{-1}(1+z^{-1})}{2(1-z^{-1})^2}$	$\frac{z^{-1}(1+4z^{-1}+z^{-2})}{6(1-z^{-1})^3}$

$$H(z) = (\sum_{n=-\infty}^{\infty} \mathcal{L}^{-1}\left\{\frac{H(s)}{s}\right\}(nTs)z^{-n})(1-z^{-1})$$

Fig. 4.2. Equivalent circuit to compute equivalent discrete loop transfer function using impulse invariant transformation.

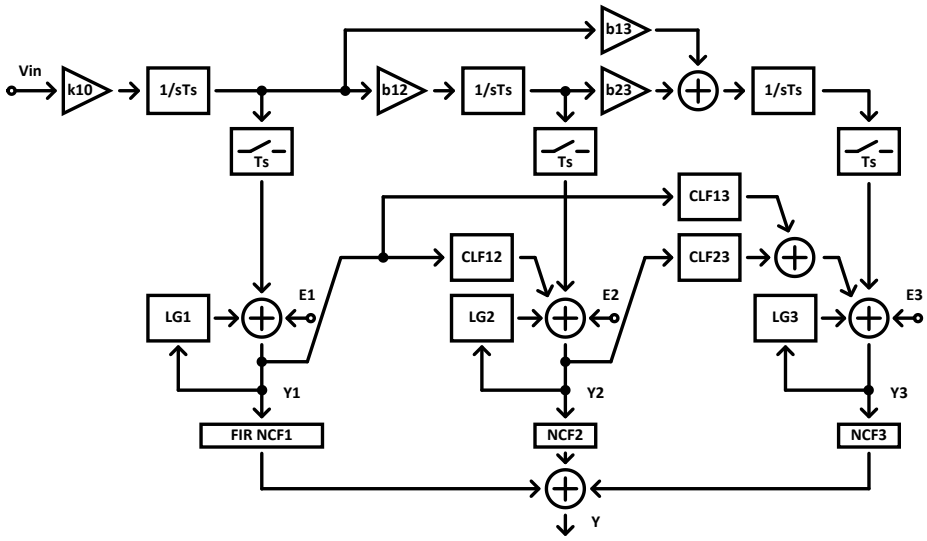


Fig. 4.3. Equivalent model of the CT-ΔΣM shown in Fig 4.1 with NCFs.

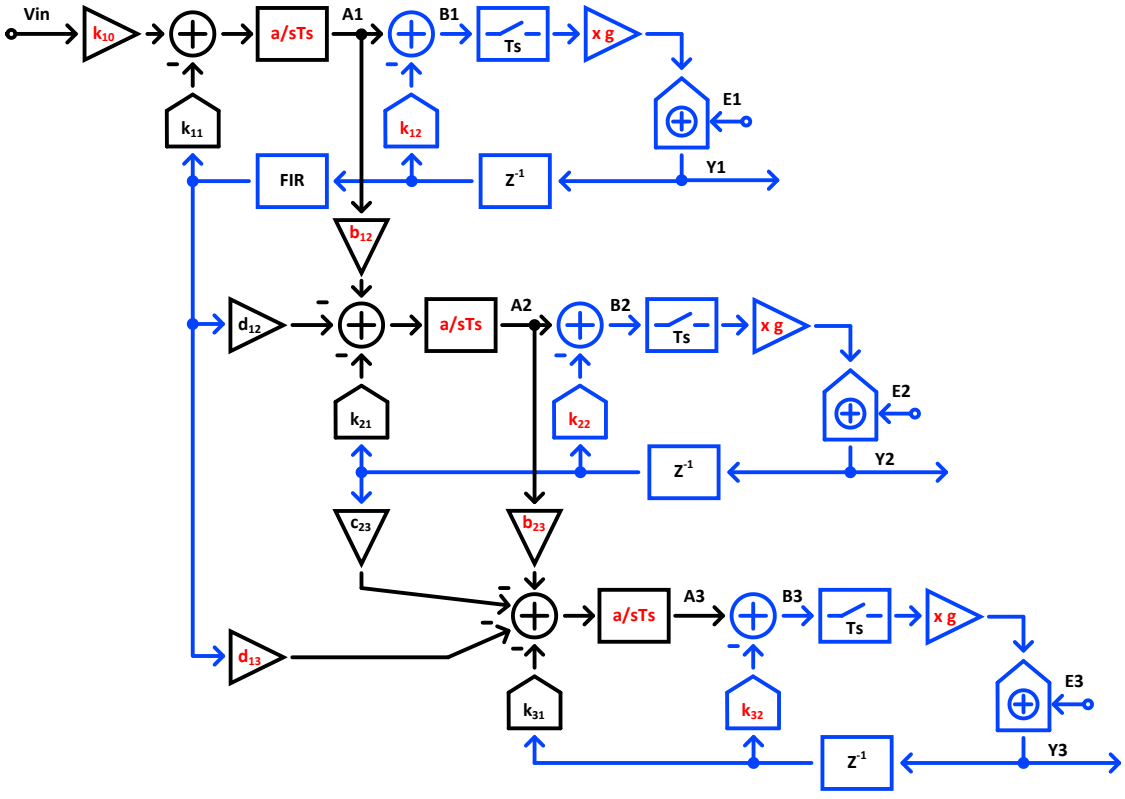


Fig. 4.4. The proposed MASH 1-1-1 CT-ΔΣM.

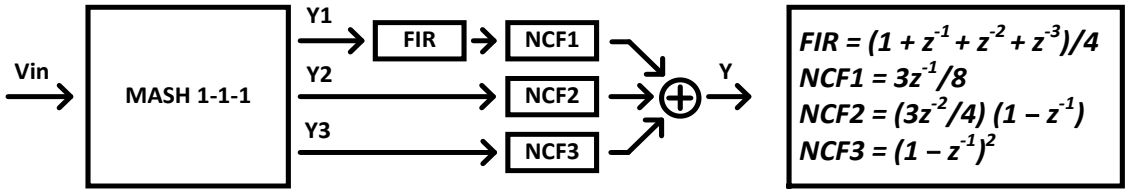


Fig. 4.5. NCFs of the proposed MASH 1-1-1 CT-ΔΣM.

A shortcoming of the ELD compensation scheme with fast feedback path coefficient k_{12}, k_{22} and k_{23} equal unity is that the voltage swings at the output of the integrators at nodes A1, A2 and A3 are twice the full-scale of the quantizer. To address the signal swing issue, the 1.5-bit quantizer topology is employed instead of a single-bit giving the freedom to control the gain of the quantizer to two. This is obtained by reducing the full-scale range Vref of the quantizer with respect to that of the modulator and by doubling the capacitor value in the active RC integrator [74]. In addition, the lowered bandwidth of the integrator relaxes the unity-gain frequency requirement of the OA. The updated coefficients of the proposed MASH 1-1-1 CT-ΔΣM after quantizer gain scaling are listed in Group II of Table 4.1. The digital feedforward path from the first stage to the third stage is eliminated ($d_{13} = 0$) in the circuit implementation to save power with negligible impact on the NTF of the modulator.

Clocked at 3.0 GHz sampling frequency (Fs), the proposed MASH 1-1-1 CT-ΔΣM, employing a 1.5-bit FIR DAC, and 1.5-bit loop-unrolling quantizer, achieves a signal to quantization noise ratio (SQNR) of 78.7 dB in a BW of 50.5 MHz, with an input signal level of -2.5 dBFS. The simulated output spectrum of the proposed MASH 1-1-1 CT-

ΔΣM is shown in Fig. 4.6 (a). Without the proposed FIR compensation scheme in NCF1, the SQNR of the modulator reduces down to 60.7 dB as shown in Fig. 4.6 (b).

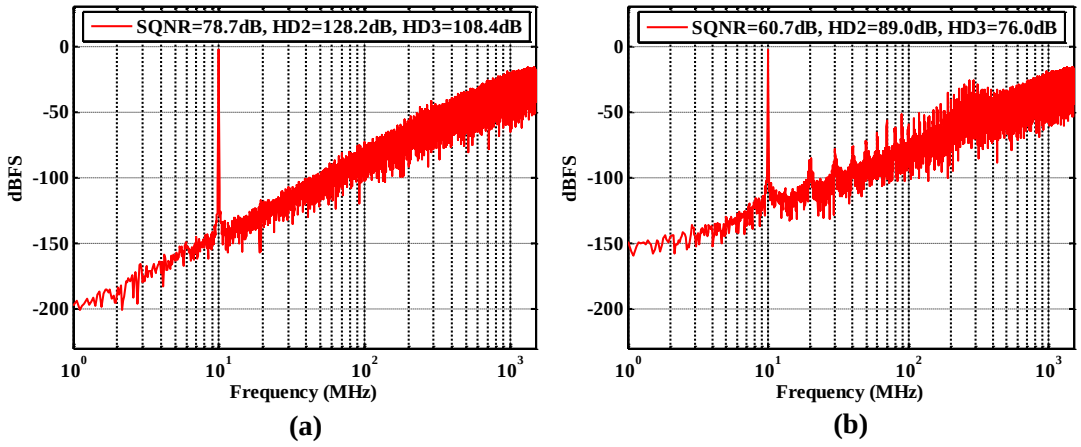


Fig. 4.6. Simulated output spectrum of the proposed MASH 1-1-1 CT-ΔΣM: (a) w/ FIR compensation logic in NCF1; (b) w/o FIR compensation logic in NCF1.

4.2.3. Coefficient Variation

Extensive simulations verified the impact of coefficient variations on the noise floor (NF) of the proposed modulator architecture. Fig. 4.7 shows the simulated quantization NF of the proposed MASH 1-1-1 CT-ΔΣM with RC time-constant variations. To ensure the NF of the modulator below − 70 dBFS, the global RC time-constant variations need to stay within − 6.8% and 4.6%. Therefore, RC time-constant calibration is mandatory because the expected variations of the absolute values of R and C can be as large as ± 20%. In addition to the RC time-constant variation, the DAC current also affects the

coefficients; thus, its variations must be minimized as well. The inter-stage coefficient variations are compensated by adjusting the capacitor value in the active RC integrator externally.

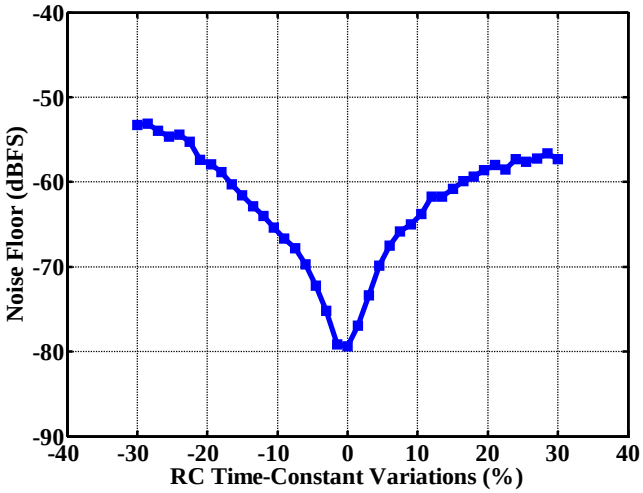


Fig. 4.7. Quantization NF as function of RC time-constant variations.

4.2.4. Clock Jitter

Clock jitter has a critical impact on the performance of CT-ΔΣMs [72]. The DAC k_{11} in the first stage of the modulator is the most sensitive block, since in-band signal processing strongly depends on the quality of this loop, and its jitter noise is injected into the modulator equivalent to a noise source added directly to the modulator's input. Due to the lack of an on-chip PLL, the prototype chip relies on the performance of an external clock source. The interface importing the external clock on chip may add more jitter and degrade the performance of the modulator if not managed properly. As shown

in Fig. 4.8, without the FIR DAC, the jitter-induced modulator's NF is limited to around − 63 dBFS when the external clock shows a white rms jitter of 1 ps (0.3% of the clock period Ts). Thus, the proposed FIR filter is mandatory to improve the modulator's jitter sensitivity. Without the FIR filter, the original 1.5-bit DAC only provides three feedback current levels; however, with the FIR filter, the number of current levels increases to nine, as shown in Fig. 4.8. To achieve a − 70 dBFS NF for the proposed MASH 1-1-1 CT-ΔΣM with FIR DAC, the clock rms jitter requirement is relaxed to 2.33 ps, which corresponds to 0.7% of the clock period.

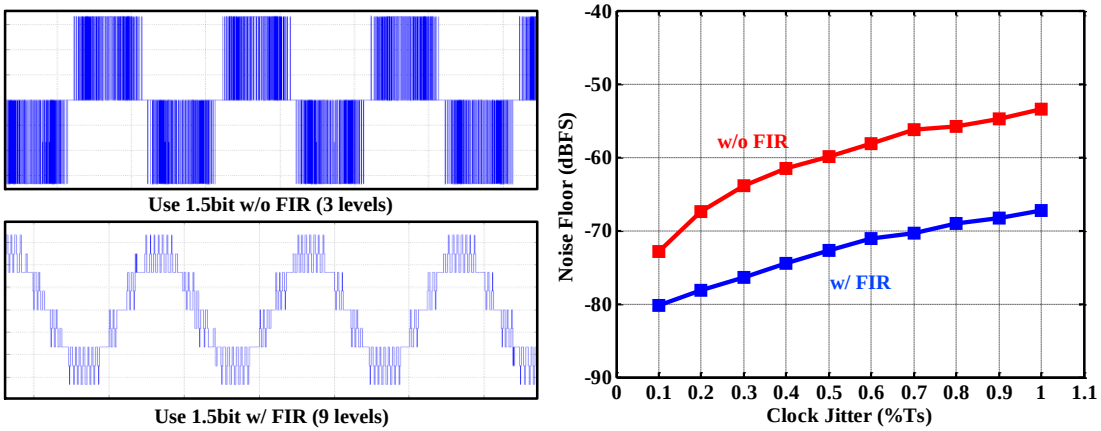


Fig. 4.8. Clock jitter effect on the NF with and without FIR DAC.

4.3. Circuit Implementation

Fig. 4.9 shows the top-level circuit implementation of the proposed MASH 1-1-1 CT-ΔΣM. The modulator consists of three active-RC integrators, five 1.5-bit current-

steering DACs and three 1.5-bit EELU quantizers. The noise cancelling filters and the digital summer are off chip in MATLAB. The following sub-sections describe the key building blocks of the proposed modulator.

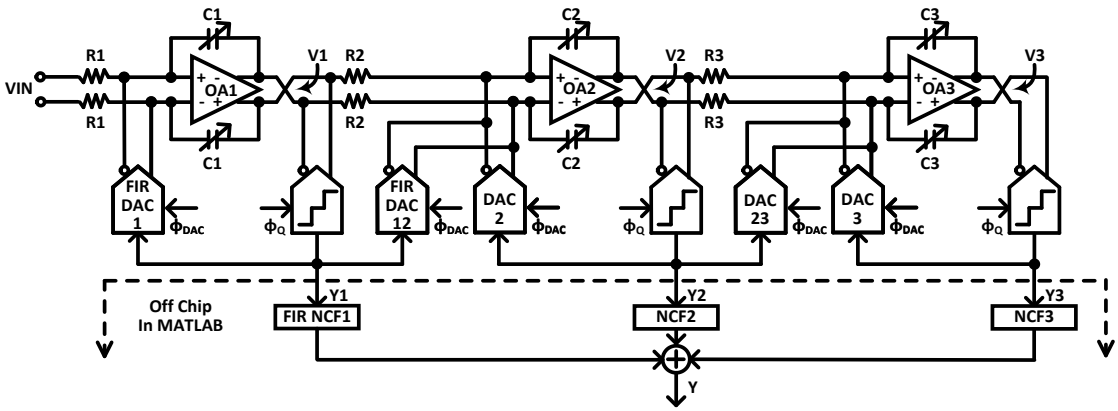


Fig. 4.9. Top-level circuit implementation of the proposed MASH 1-1-1 CT-ΔΣM.

4.3.1. Operational Amplifier (OA)

For CT-MASH modulators, the OA gain must be high enough in the signal band to meet the distortion targets and to ensure sufficient coefficient accuracy. The circuit implementation for OA is shown in Fig. 4.10 (a). The four-stage OA is compensated using the no capacitor feedforward (NCFF) scheme [52], [62], [66], [67], [69], [73]. The fourth-order cascaded path consists of the transconductors Gm1-4, which provide a high gain at low frequencies under low power supply voltage. At high frequencies, the first-order path through the transconductor Gm14 dominates the OA frequency response to guarantee closed-loop stability. The second- and third-order paths through the

transconductors Gm12 and Gm13 provide a smooth transition for the OA frequency response at intermediate frequencies. The bandwidth of each stage is optimized to provide a high gain up to the modulator bandwidth of 50 MHz while maintaining an adequate phase margin. Additional NMOS capacitors are added to the first- and second-stage outputs to achieve the optimal frequency response and low noise performance. Their non-linearity requirements are not a big concern due to small signal swings at internal nodes.

Gm1-3 and Gm12-13 in the OA share a similar schematic as shown in Fig. 4.10 (b). The input transistors M1 use small channel length transistors, and the cascode transistors M2 are added to improve the output resistance. More headroom is allocated for M3 to lower their noise contribution without adding cascode transistors. The single-stage amplifier is self-biased with R1 and C1 forming a common-mode feedback (CMFB). The transconductor Gm4 and Gm14 are formed by the transistors M3 and M2 as shown in Fig. 4.10 (c), respectively. A two-stage Miller compensated CMFB loop with a nulling resistor is used. The error amplifier (EA) is implemented using a folded-cascode topology with NMOS input as shown in Fig. 4.10 (d).

Fig. 4.11 shows the post-layout simulated Bode plot of OA1. The loop gain is obtained by Cadence stb analysis when OA1 is used in closed loop as the first integrator, whereas OA gain is obtained when OA1 is used in open loop including the integrator feedback network as its loading. The unity gain frequency of the loop response is 1.6 GHz, slightly higher than Fs/2, and its phase margin is around 51 deg. At 50 MHz BW boundary, a gain of 65 dB is provided by the OA1 to satisfy both the linearity and

quantization noise leakage specifications. The requirement of gain at Fs/2 is relaxed for a lowered integrator bandwidth after the quantizer gain adjustment.

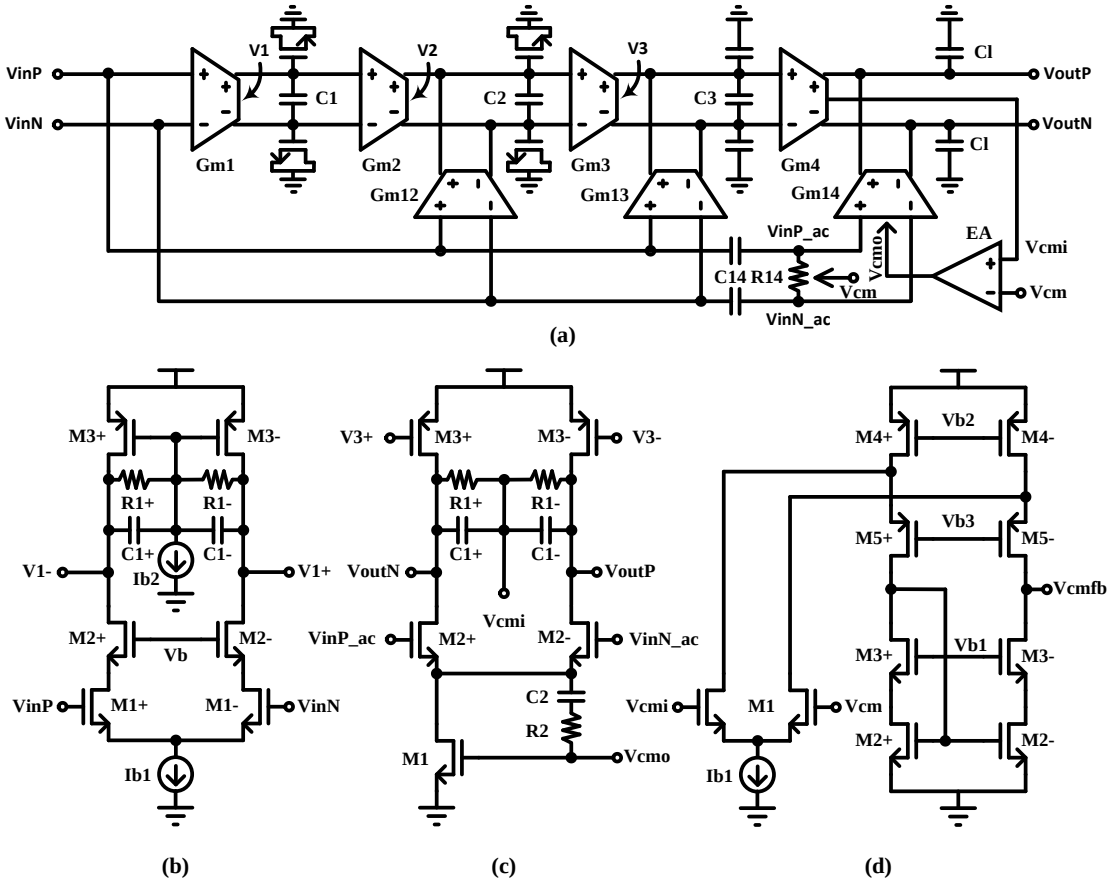


Fig. 4.10. Circuit implementation for OA: (a) NCFF topology; (b) transconductor Gm1; (c) transconductor Gm4 and Gm14; (d) error amplifier (EA) required for CMFB loop.

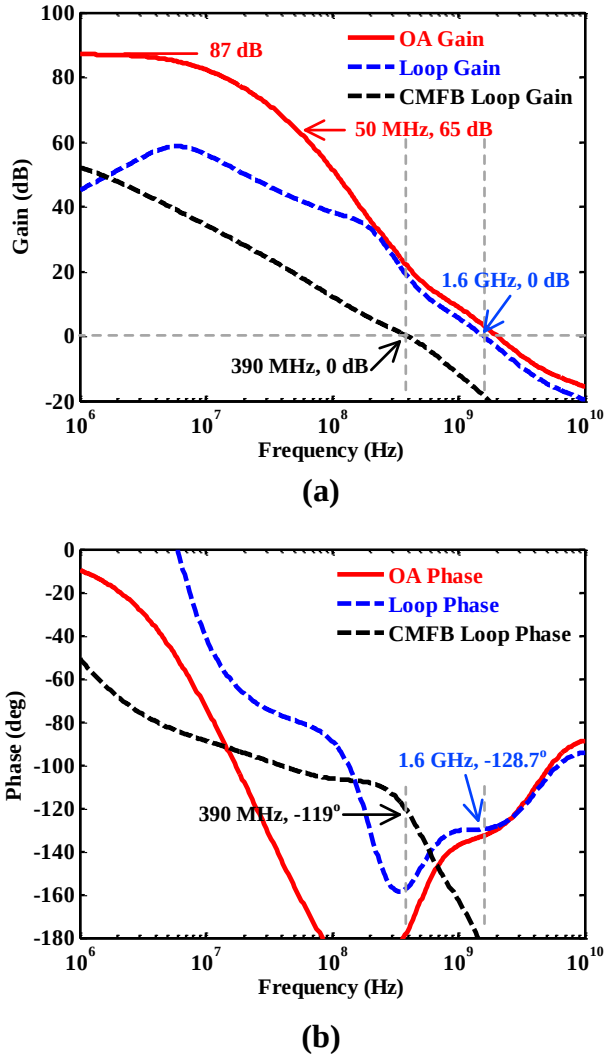


Fig. 4.11. Post-layout simulated OA1's Bode plot: (a) gain; (b) phase.

4.3.2. Digitally Tunable Capacitor

To compensate for RC time-constant variations, digitally tunable capacitors are employed in the integrators. Table 4.2 shows the digitally tunable capacitors for the loop filter capacitors. The capacitor in the first integrator is controlled independently, while

the capacitors in the last two stages share the same digital control bus. The switch on-resistance is low enough to minimize the NTF out-of-band peaking; on the other hand, the transistor dimensions are limited to maintain small enough parasitic capacitances.

Table 4.2: Digitally tunable capacitors

Capacitor	Capacitance (pF)
C1	2.5 (1.8 to 4.0 tunable)
C2	0.625 (0.4 to 1.0 tunable)
C3	0.625 (0.4 to 1.0 tunable)

4.3.3. Encoder-Embedded Loop-Unrolling (EELU) Quantizer

Fig. 4.12 (a) shows the conventional analog implementation of the ELD compensation path, highlighted in the blue block. The analog feedback path is composed of a fast feedback DAC and a summing amplifier [71]. The nth-sampled analog voltage at the input of the quantizer B(n) is then computed as:

$$B(n) = A(n) - C(n)\,R_2; \tag{4. 13}$$

where A(n) is the analog voltage at the output of the integrator at the nth sampling instant and C(n) is the nth feedback current level of the fast DAC. The 3-level 1.5-bit quantizer then resolves B(n) by comparing it with ± Vref/3 at the rising edge of Φ_Q and generates the digital output Y(n):

$$\mathrm{Y(n)} = \begin{cases} '11', & if\ B(n) > Vref/3; \\ '01', & if -Vref/3 \le B(n) \le Vref/3; \\ '00', & if\ B(n) < -Vref/3; \end{cases} \quad (4.\ 14)$$

Since the quantizer resolves 1.5 bits, the fast DAC has 3 different current levels: $2\mathrm{Vref}/(3\mathrm{R}_2)$, 0 and $-\ 2\mathrm{Vref}/(3\mathrm{R}_2)$. The value of DAC current C(n) depends on the previous quantizer output:

$$\mathrm{C(n)} = \begin{cases} 2Vref/(3R_2), & if\ Y(n-1) = '11'; \\ 0, & if\ Y(n-1) = '01'; \\ -2Vref/(3R_2), & if\ Y(n-1) = '00'; \end{cases} \quad (4.\ 15)$$

To achieve effective ELD compensation, the operation of the entire feedback path needs to be completed within clock period Ts. However, it is power and area demanding to meet the high gain-bandwidth product (GBW) requirement of the OA in the summing amplifier.

To address the issue, a digital domain loop-unrolling concept inspired on decision feedback equalization (DFE) in wireline communication systems [75] is employed. The proposed realization circuit multiplexes among the output of a group of sub-quantizers with pre-determined comparison references based on the previous comparison results [76], [77]. As shown in Fig. 4.12 (b), the 1.5-bit loop-unrolling quantizer is composed of three sub-quantizers, a digital MUX, and a unity delay element. The digital outputs of the sub-quantizers are computed based on the following rules:

$$Y_{11}(\mathrm{n}) = \begin{cases} '11', & if\ A(n) > Vref; \\ '01', & if\ Vref/3 \le A(n) \le Vref; \\ '00', & if\ A(n) < Vref/3; \end{cases} \quad (4.16)$$

$$Y_{01}(\mathrm{n}) = \begin{cases} '11', & if\ A(n) > Vref/3; \\ '01', & if\ -Vref/3 \le A(n) \le Vref/3; \\ '00', & if\ A(n) < -Vref/3; \end{cases} \quad (4.17)$$

$$Y_{00}(\mathrm{n}) = \begin{cases} '11', & if\ A(n) > -Vref/3; \\ '01', & if\ -Vref \le A(n) \le -Vref/3; \\ '00', & if\ A(n) < -Vref; \end{cases} \quad (4.18)$$

These rules show that the references of the sub-quantizer with digital output Y11(n) are shifted up by 2Vref/3 compared with the conventional values ±Vref/3. Similarly, the comparison reference of the sub-quantizer with digital outputs, Y01(n) and Y00(n), are shifted by 0 and − 2Vref/3, respectively. The final digital output of the loop-unrolling quantizer with embedded digital ELD compensation path is achieved by multiplexing among the digital outputs of the sub-quantizers. All three potential quantizations are realized and the correct one is selected by the bits associated with the previous output result. If the previous comparison result is '11', '01' or '00', the final digital output is chosen to be equal to Y11, Y01, or Y00, respectively, which means:

$$Y(\mathrm{n}) = \begin{cases} Y_{11}(\mathrm{n}), & if\ Y(\mathrm{n}-1) = '11'; \\ Y_{01}(\mathrm{n}), & if\ Y(n-1) = '01'; \\ Y_{00}(\mathrm{n}), & if\ Y(\mathrm{n}-1) = '00'; \end{cases} \quad (4.19)$$

The operation flow of a 1.5-bit loop-unrolling quantizer is detailed in Fig. 4.12 (c).

During the succeeding clock cycles, the integrator output voltage A is assumed to be constant for cycle N and N − 1. The two succeeding cycles N − 1 and N operate as follows: 1) During cycle N − 2, assuming the previous comparison result is '01', the reference levels for 1.5-bit quantization are ± Vref/3. 2) If A(n − 1) is higher than Vref/3, the output during cycle N − 1 should be '11'. 3) Thus, the fast DAC will feedback 2Vref/3, and in cycle N, the comparison should be between A(n) − 2Vref/3 and the default reference levels ± Vref/3. This is equivalent to compare A(n) with shifted up references Vref/3 and Vref. 4) If the input voltage A(n) is higher than Vref/3, but lower than Vref, the output during cycle N should be '01'. The 1.5-bit loop-unrolling quantizer achieves the same functionality as the conventional analog implementation counterpart.

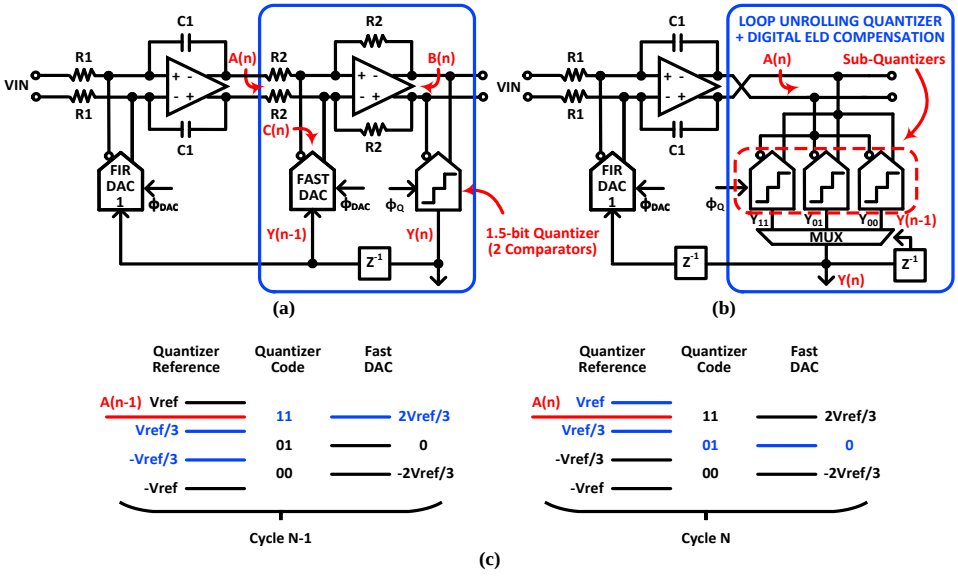
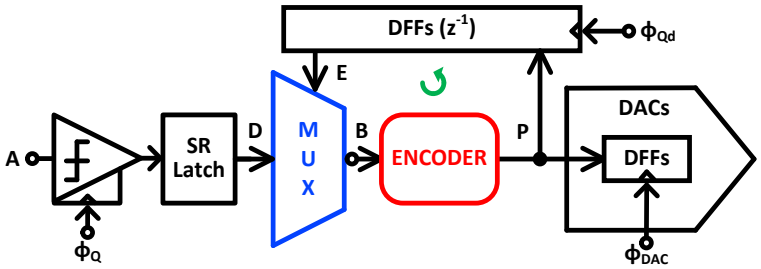
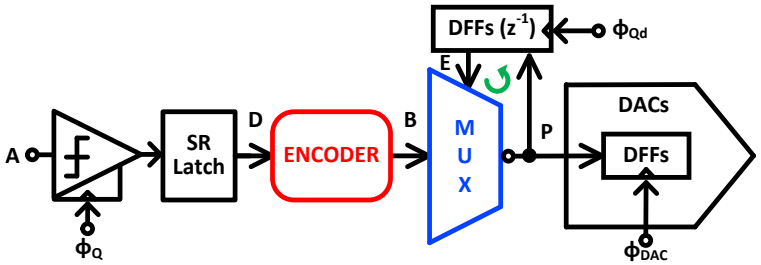


Fig. 4.12. ELD compensation path: (a) with conventional analog implementation; (b) with loop-unrolling digital implementation; (c) operation flow example.

To provide the 3-bit digital control signal for the 1.5-bit DAC, a simple digital encoder built with NAND gates is required in the feedback path. The encoder can be arranged after the MUX or before the MUX, which results in two different topologies as shown in Fig. 4.13 (a) MUX-ENCODER topology and (b) ENCODER-MUX, respectively. The local cycling loop of the ENCODER-MUX topology operates faster, as the encoder block is no longer a part of the loop, as in the MUX-ENCODER topology. Thus, in the ENCODER-MUX topology, the final quantizer output data P gets ready earlier and holds valid for a larger percentage of the clock cycle for the DAC DFFs to capture, compared with the MUX-ENCODER topology. It is then beneficial to allocate the encoder block before the MUX for its higher speed operation potential. The complete top-level schematic of the proposed 1.5-bit EELU quantizer based on the ENCODER-MUX topology is shown in Fig. 4.14. On the left part of the figure, there are three sets of reference-level-shifted sub-quantizers, each of which consists of two StrongARM comparators. However, only four comparators in total are realized, as the other two are redundant. The tri-stage gates encompass the encoder as part of the MUX to reduce the delay in the signal path. The inverter-chain buffers ensure driving capability of the long-distance routing interconnections between the EELU quantizers and DACs.



(a)



(b)

Fig. 4.13. Loop-unrolling quantizer employing: (a) MUX-ENCODER topology; (b) ENCODER-MUX topology.

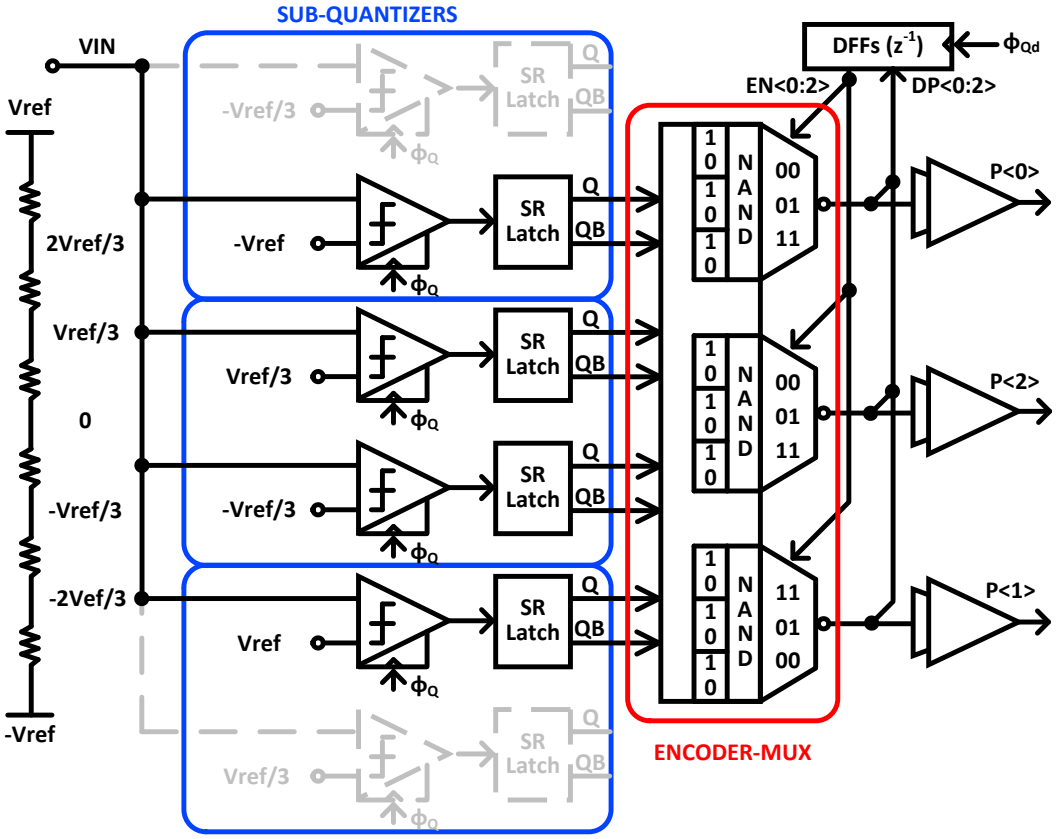


Fig. 4.14. 1.5-bit encoder-embedded loop-unrolling (EELU) quantizer topology.

4.3.4. FIR DAC

The detailed implementation of the 1.5-bit FIR current-steering DAC is shown in Fig. 4.15. The total DAC current I_{DAC} is segmented into four equal sections with one clock cycle delayed digital control between each [53]. Analog drivers (NDR and PDR) placed after the DFFs adjust the on/off voltage limits and the crossing voltage levels to improve the switching performance of the DAC segments. A complementary N-P DAC topology under low voltage supply of 1.2 V is employed for its good power efficiency

compared with N or P alone DAC topologies [56], [67]–[69]. Different from a multi-bit DAC that demands stringent matching between segments, each segment of the FIR DAC is inherently linear for its single current source topology. On the other hand, a 1% current matching among the DAC segments is desirable for the FIR coefficient accuracy and quantization noise cancellation, based on a 500-run Monte-Carlo simulation as shown in Fig. 4.16. The DAC current $I_{DAC}/4$ is mirrored from a biasing current generated by a reference voltage over resistor. External 10 μF ceramic capacitors are used to decouple the common-mode noise from the biasing circuitry. The biasing resistor is placed close to the integrator resistors in layout to improve matching [66]. A 90-dB dc gain telescope amplifier is employed to achieve decent current resistance product accuracy. The 1.5-bit DAC current is routed towards VCM when its digital control code is '01'. Thus, the noise performance of the 1.5-bit DAC is better compared with the conventional 1-bit design in which the DAC noise is always injected into the modulator.

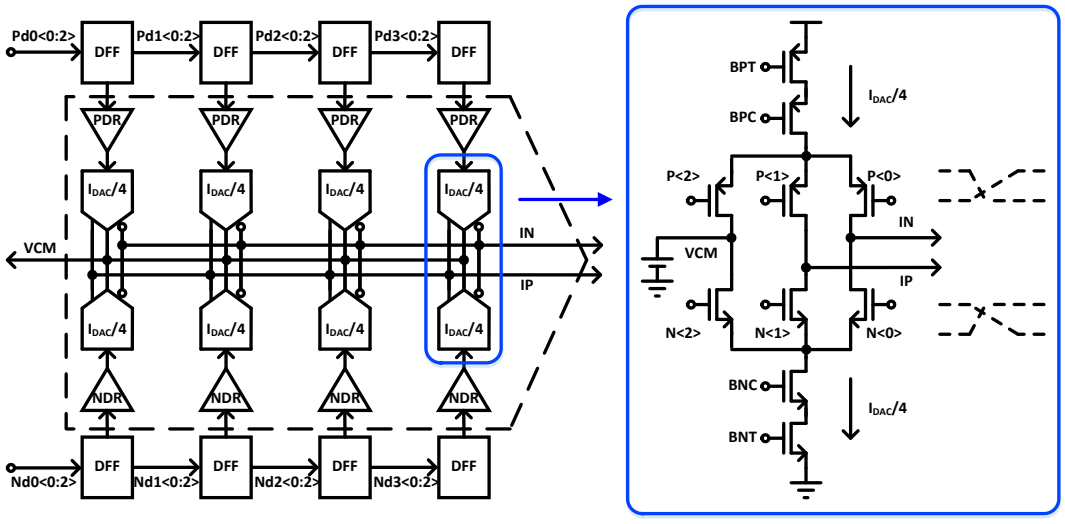


Fig. 4.15. 1.5-bit FIR DAC implementation.

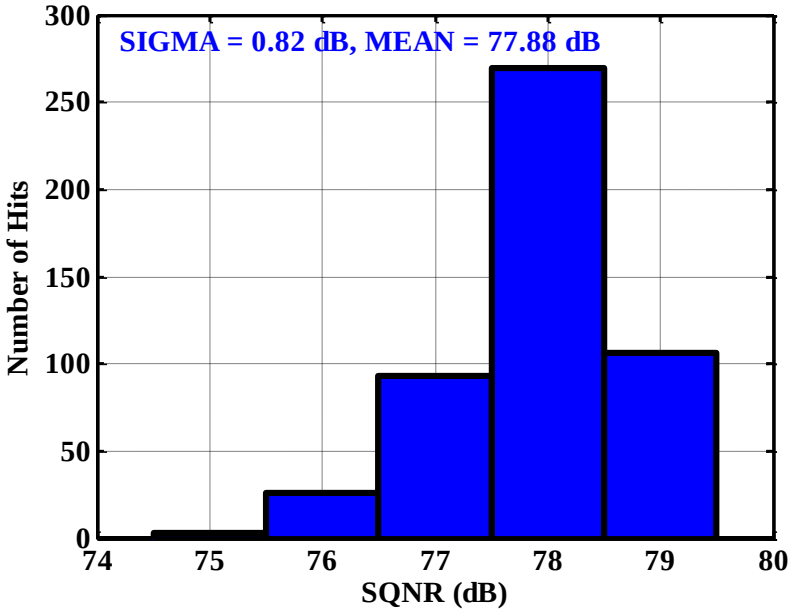


Fig. 4.16. 500-run Monte-Carlo simulated distribution of SQNR with 1% current mismatch among segments of FIR DAC.

4.4. Measurement Results

The prototype MASH 1-1-1 CT-ΔΣM was fabricated in a 40-nm low-power CMOS process; Fig. 4.17 shows the microphotograph of the chip. The total area of the prototype modulator is 0.177 mm^2 in which the modulator core occupies 0.127 mm^2. The modulator is clocked at 3 GHz generated using an external clock source from Agilent N5171B and on-chip clock buffers. The 3 GHz digital data of the modulator are sent out of chip using pulse amplitude modulation (PAM-4) and captured using high-speed oscilloscope Agilent DSA91304A.

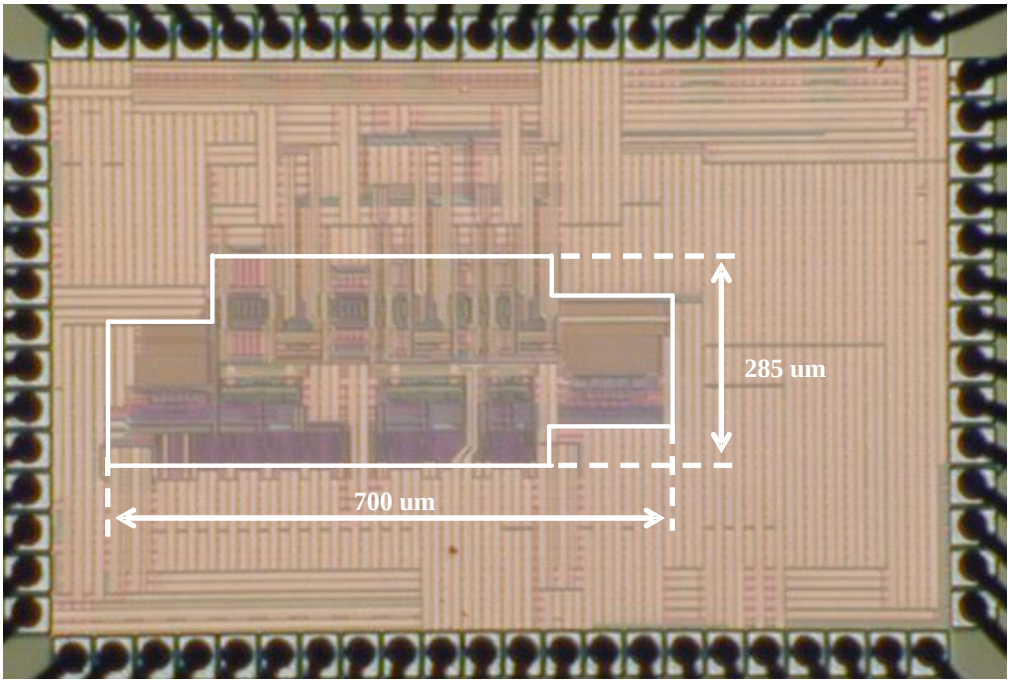


Fig. 4.17. Microphotograph of the prototype chip.

Fig. 4.18 shows the measured fast Fourier transform (FFT) spectrum of the prototype MASH 1-1-1 CT-ΔΣM output for a 10 MHz single-tone sinusoidal input signal provided by Agilent E8267D and filtered by a KR Electronics 2796-SMA bandpass filter. The measured peak signal-to-noise and distortion ratio (SNDR) and peak signal-to-noise ratio (SNR) are 67.3 dB and 68 dB, for an input amplitude of − 2.8 dBFS and − 1.6 dBFS, respectively. Under peak SNDR condition, the second and third order harmonic distortion components HD2 and HD3 are at − 80 dB and − 80.1 dB levels, respectively. Since the bandwidth of the modulator is set at 50.5 MHz, the SNDR integration includes up to a fifth-order distortion harmonic component. Fig. 4.19 shows the measured SNR

and SNDR vs single-tone sinusoidal input signal amplitude at a frequency of 10 MHz. The measured dynamic range of the modulator is 68.2 dB.

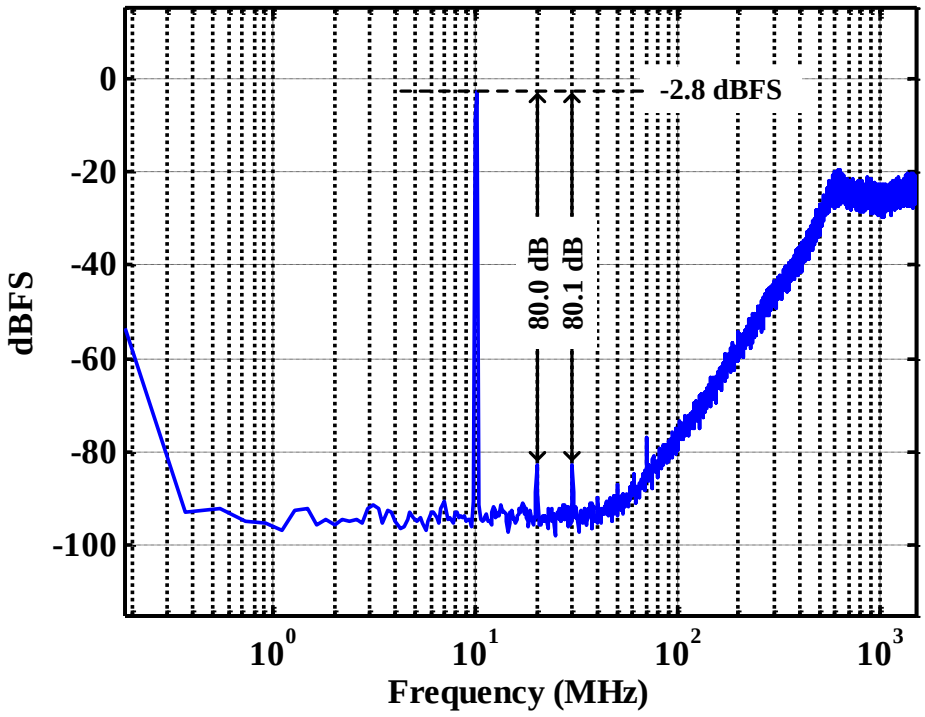


Fig. 4.18. Measured single-tone FFT spectrum.

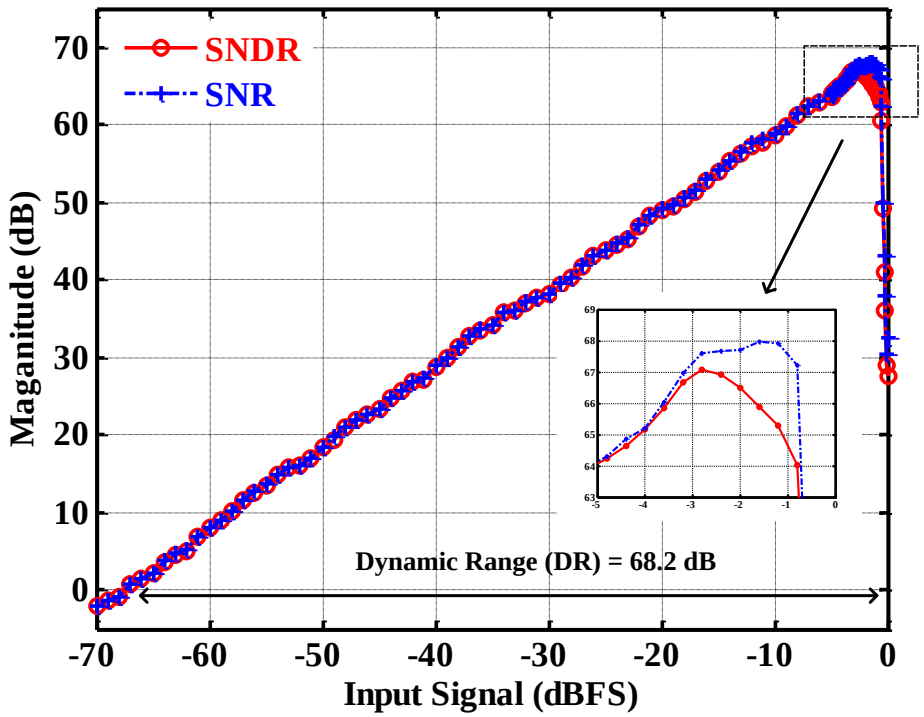


Fig. 4.19. Measured SNR and SNDR versus the modulator's input signal level.

Fig. 4.20 shows the measured FFT spectrum for two-tone sinusoidal input signals at frequencies of 38 MHz and 42 MHz; the amplitude of each tone corresponds to − 8.8 dBFS. The two-tone input signals are combined by a power combiner and filtered by the KR Electronics 2510-SMA bandpass filter. The measured third-order intermodulation is 78.8/78.4 dB. The harmonic distortion components are very close to the noise level of the setup, demonstrating the outstanding linearity of the architecture.

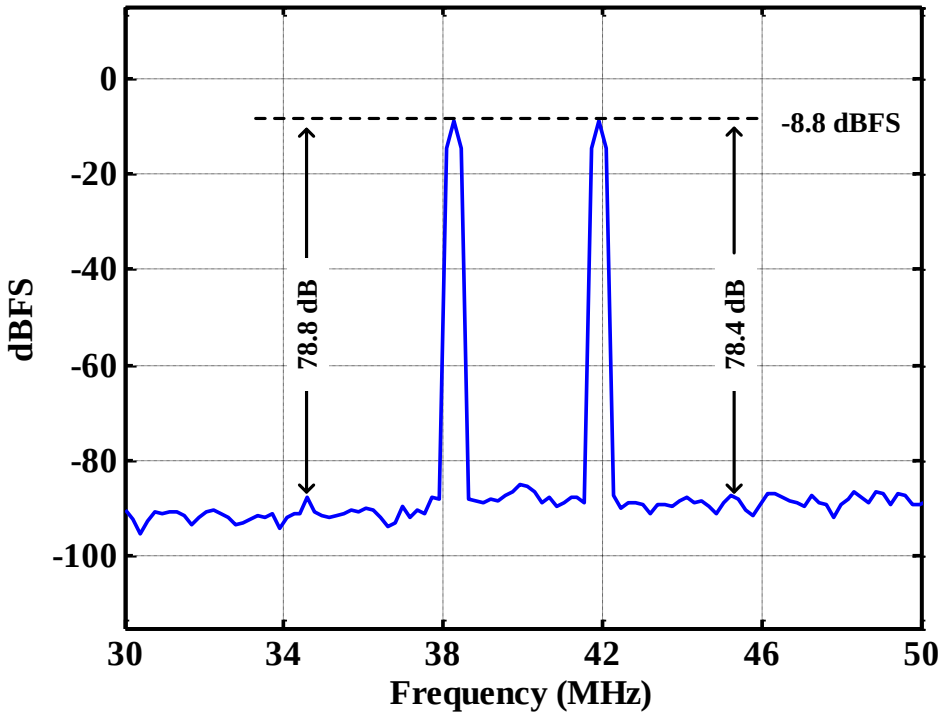


Fig. 4.20. Measured two-tone FFT spectrum.

Fig. 4.21 shows the measured noise floor versus the RC time-constant control code of the first stage of the prototype modulator. The control code adjusts the digitally tunable capacitor in the active RC integrator. The digital code for the modulator's first stage was swept over its entire range while keeping the last two stages at their nominal value.

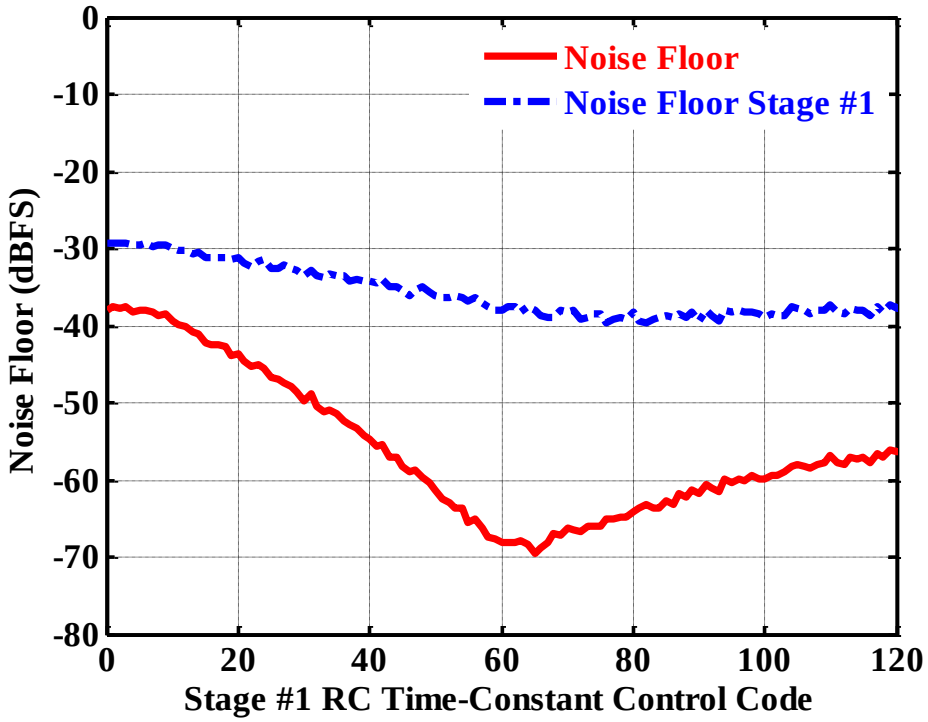


Fig. 4.21. Measured NF versus the first stage RC time-constant control code.

Fig. 4.22 illustrates the measured power consumption of the prototype modulator. The total power of the modulator is 18.98 mW. The modulator's core composed of the integrator OAs, the FIR DACs and the EELU quantizer is powered with a 1.2 V voltage supply. Only the biasing circuitry uses a 2.5 V supply to provide a biasing current with good accuracy.

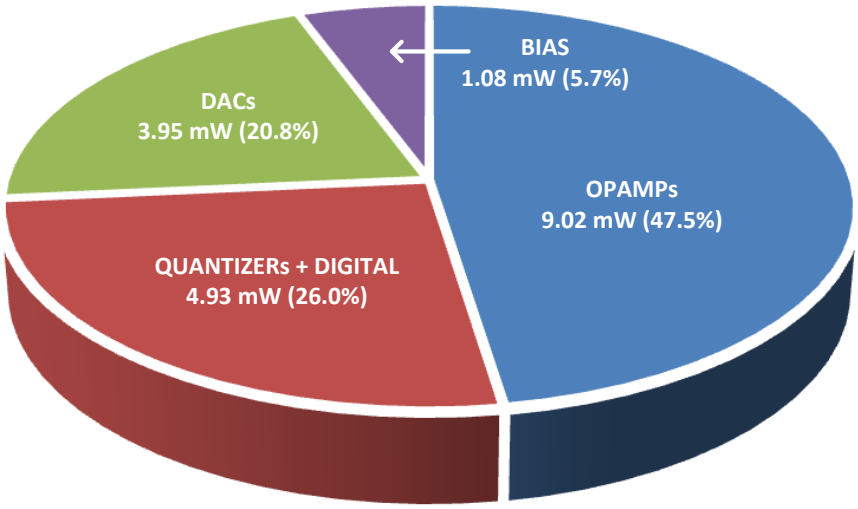


Fig. 4.22. Measured power consumption breakdown.

4.5. Conclusion

This work demonstrates a MASH 1-1-1 CT-ΔΣM employing FIR DACs and EELU quantizers. An FIR filter in an inherently linear 1.5-bit DAC improves the modulator's jitter sensitivity performance. The MASH topology compensates the FIR's effect on the modulator's NTF. A 1.5-bit EELU quantizer topology based on multiplexing comparator outputs achieves high-speed encoding and ELD compensation, eliminating the need of a fast analog summing block. The modulator's prototype fabricated in a 40-nm CMOS technology, achieves 67.3 dB of SNDR, 68 dB of SNR, and 68.2 dB of DR in 50.5 MHz BW with a total power consumption of 19 mW. The proposed modulator features a 161.5 dB of figure-of-merit (FOM), defined as FOM = SNDR + 10 $\log_{10}$ (BW/P). Table 4.3 summarizes the performance of the modulator and shows that this design is competitive compared to state-of-the-art CT-ΔΣMs.

Table 4.3: Performance summary and comparison with state-of-the-art CT-ΔΣMs

	This Work	[69]	[68]	[67]	[66]	[61]	[60]	[57]	[56]	[51]
Technology (nm)	**40**	28	28	28	40	16	65	65	20	90
MASH	**Yes**	Yes	Yes	Yes	Yes	No	No	No	No	No
Fs (GHz)	**3**	6	1.8	3.2	1	2.88	1.2	1.28	2.184	3.6
BW (MHz)	**50.5**	350	50	53.3	50.3	160	50	50	80	36
Peak SNR (dB)	**68**	66.8	76.8	83.1	75.8	68.1	71.7	71	70	76.4
Peak SNDR (dB)	**67.3**	64.8	74.9	71.4	74.4	65.3	71.5	64	67.5	70.9
DR (dB)	**68.2**	72.8	85	88	76.8	72.1	72	75	73	76.4
Power Supply (V)	**1.2** **2.5**	-1 1 1.8	1.3 1.5	-1 0.9 1.8	1.1 1.15 2.5	0.8 1.4 1.5	N/A	1.2 1.5	1 1.2 1.5	1.2
Area (mm^2)	0.177	1.4	0.337	0.9	0.265	0.155	0.5	0.49	0.1	0.12
Power (P) (mW)	18.98	756	80.4	235	43	40	54	38	23	15
FOM[a](dB)	**161.5**	151.5	162.8	154.9	165.1	161.3	161.2	155.2	162.9	164.7
FOM_S[b] (dB)	**162.4**	159.5	172.9	171.5	167.5	168.1	161.7	166.2	168.4	176.8
FOM_W[c] (fJ/c-s)	**99.2**	761.1	177.1	730.8	99.8	82.8	176	293.6	74.2	72.7

[a] $FOM=SNDR+10\times\log_{10}(BW/P)$

[b] $FOM_S=DR+10\times\log10(BW/P)$

[c] $FOM_W=P/(2\times BW\times 2\text{^}((SNDR-1.76)/6.02))$

V. CONCLUSION

In this dissertation, two prototype chips with techniques targeting lower power ADC design in advanced CMOS technology nodes are presented.

A 66.8 µW-per-column image sensor digitizer based on SS-ADC topology was designed and implemented in a 40 nm low-power CMOS process. The proposed PW technique enables a power saving of 52.8% in the hybrid digital counter, while maintaining the capability of completing digital CDS in column. A dark/bright column FPN of 0.0024%/0.028% from the readout circuit is achieved with the proposed double AZ technique without any off-chip processing. The proposed design achieves low readout noise and a wide dynamic range of 71.8 dB without any column gain stages. The proposed techniques are suitable for readout of back-illuminated 3D-stacked CMOS image sensor pixel array and exportable to other architectures.

A MASH 1-1-1 CT-ΔΣM topology employing FIR DACs and EELU quantizers is proposed for wide-band mobile/wireless communication circuits. An FIR filter in an inherently linear 1.5-bit DAC improves the modulator's jitter sensitivity performance. The MASH topology compensates the FIR's effect on the modulator's NTF. A 1.5-bit EELU quantizer topology based on multiplexing comparator outputs achieves high-speed encoding and ELD compensation, eliminating the need of a fast analog summing block. The modulator's prototype fabricated in a 40-nm CMOS technology, achieves 67.3 dB of SNDR, 68 dB of SNR, and 68.2 dB of DR in 50.5 MHz BW with a total power consumption of 19 mW.

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