A FAST RESPONSE DUAL MODE BUCK CONVERTER WITH AUTOMATIC MODE TRANSITION

A Thesis

by

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ABSTRACT

Dual mode DC-DC converters utilizing PWM and PFM modes of operation have been widely used to improve the efficiency over a wide range of the load current. Due to the highly varying nature of the load, it is beneficial to have the converter switch between the modes without an external mode select signal. This work proposes a new technique for automatic mode switching which maintains very high efficiency at light loads and at the same time, keeps the output well regulated during a load transient from sleep to the active state. The Constant On-time PFM scheme and a zero current detector avoids the use of an accurate current sensing block. The power supply rejection is also improved using feed-forward paths from the supply in both the PWM and PFM modes. A new implementation of the PWM controller with clamped error voltage required to meet the specifications is also shown. The proposed feedback implementation using a programmable current source and resistance provides smooth output programming.

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Finally, thanks to my family for their love and encouragement which helped me sail through the tough times.

NOMENCLATURE

CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
F_{SW}	Switching Frequency
I_Q	Quiescent Current
MLCC	Multi-Layered Ceramic Capacitors
PFM	Pulse Frequency Modulation
PID	Proportional-Integral-Derivative
PWM	Pulse Width Modulation
SMPS	Switching Mode Power Supply
ZCD	Zero Current Detector

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CHAPTER I

INTRODUCTION & MOTIVATION

The tremendous increase in the use of battery operated devices has called for efficient power management to extend the battery life. Figure 1 shows the Block diagram of a cellular handset with required supply voltages [1]. The various blocks are designed and optimized for maximum performance at different supply voltages. Since the typical Li-ion Battery voltage is around 3.7V or 4.2V and vary depending on the state of charge, supply regulators are used to interface with the blocks, so as to provide a stable supply. The motivation of this thesis is to design a supply regulator with following characteristics:

- **Output Regulation**
  - DC Regulation: The steady state value of the output voltage should be maintained constant with varying Supply and Load conditions.
  - Transient Regulation: These supply regulators encounter sudden changes in the load current during the block power-up/ sleep to active mode change etc. The instantaneous value of the output should always be maintained within a certain band during these step changes, so that it doesn't affect the functionality of the block. This specification is becoming tighter as the current slew rates are increasing (and hence the additional drop due to the non-idealities in interconnect has to be mitigated) [2, 3].

  - Dynamic Voltage Scaling: The modern day power management units incorporate DVS, whereby the supply to the blocks is varied depending on the performance need; so as to improve the overall system efficiency. This necessitates supply regulators to have programmable output [4].

- **Efficiency**: The supply regulators, being only an interface between the battery and the actual load, should not consume much power. Since these battery operated devices are often in standby/sleep mode, these supply regulators should have high efficiency throughout the load range to extend the battery life.
- **Area/Cost/Integration**: As more and more functionalities get added to these devices with the overall size kept same or even lowered, the area overhead of the regulators and, the size and number of external passive components required by the regulators should be kept to a minimum.

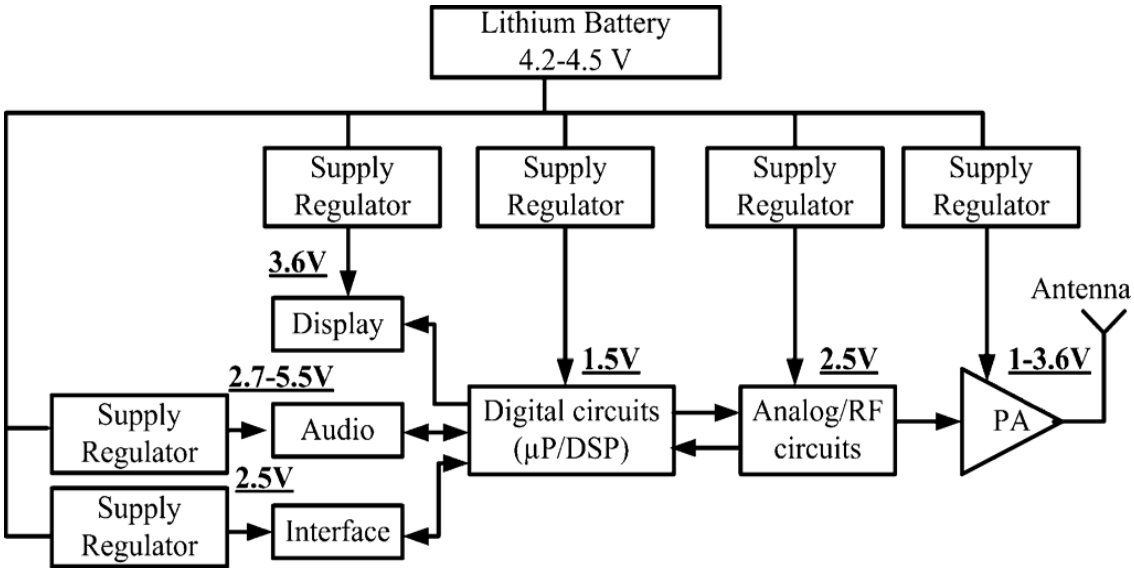


Figure 1. Block diagram of a cellular handset with required supply voltages [1]

Inductor switching step-down DC-DC (Buck) converter [5] is the most popular choice for the supply regulators given their high efficiency compared to linear regulators. Hence the focus of this thesis would be to design a Buck Converter with tight transient specifications and high efficiency throughout the load range. Chapter II gives a brief description of the Buck Converter fundamentals. It includes the steady state analysis, AC small signal modeling, and a study on the loss contributors in the actual implementation. Chapter III talks about the various control schemes adopted to regulate the output of a buck converter - mainly the PWM and the PFM scheme. Few modifications to the PWM loop to ensure the transient regulation under all circumstances is proposed. It also shows the output programming implementation that allows for smooth transition. A simple but effective implementation that varies the ON-time with supply and output voltage setting to keep the maximum load support and voltage ripple constant in the PFM mode is introduced. The efficiency improvement achieved over a wide load range using the Dual mode control (which incorporates both schemes) is also explained.

Chapter IV studies the limitations of the existing mode transition schemes in Dual mode converters and proposes a new scheme which provides fast transient without requiring an accurate current sense block. Chapter V is dedicated to the actual design procedure. Even though a supply of 1.6V to 5.5V would have been ideal, due to the non-availability of fabrication support, a Buck converter with 1.8V supply is designed and tested to show the proposed improvements. Chapter VI discusses the experimental results and the conclusion and future improvements are mentioned in Chapter VII.

CHAPTER II

BUCK CONVERTER FUNDAMENTALS

While a linear regulator maintains the desired output voltage by dissipating excess power in a "pass" transistor [6], the Buck converter rapidly switches a power transistor between linear (ON) and cutoff (OFF) regions to supply the load with a variable duty cycle such that average is the desired output voltage [5]. The resulting rectangular waveform is low-pass filtered with an inductor and capacitor before being applied to the load as shown in Figure 2. A control loop is used to determine the On-time of the switches such that the output is well regulated even during variations in the supply voltage, load current etc.

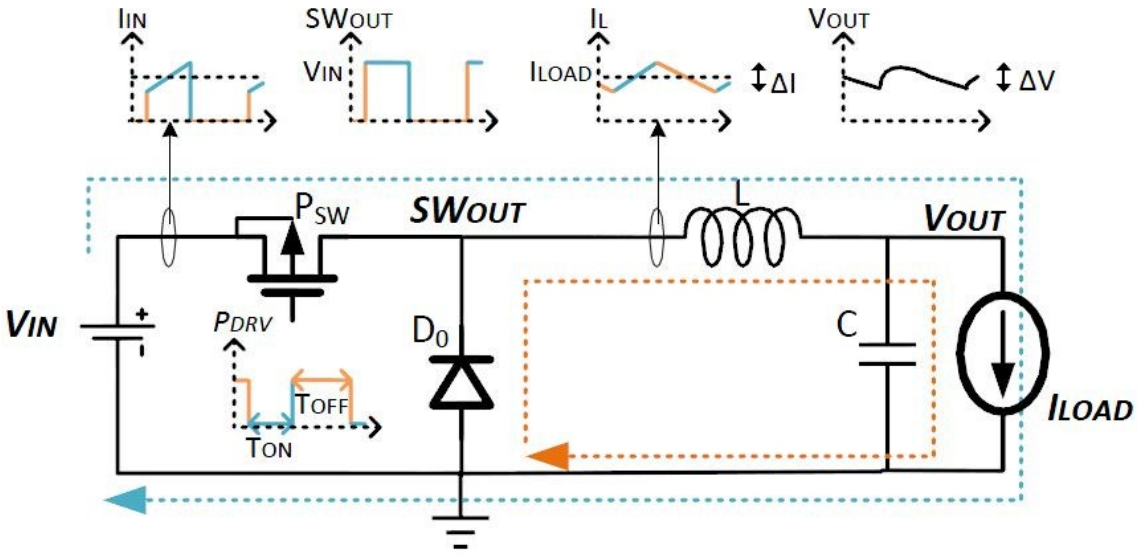


Figure 2. Asynchronous buck converter and related waveforms.

During phase 1 (represented by the blue path), P_{SW} is turned ON for T_{ON} time duration and the input supply is connected to the output filter. Assuming the output voltage ripple to be very small, the voltage across the inductor during this time would be, $V_{L1} = (V_{IN} - V_{OUT})$ and the inductor current would ramp up with a slope, $m_1 = (V_{IN} - V_{OUT})/L$. Until the inductor current (I_L) becomes greater than the load current (I_{LOAD}), the capacitor (C) discharges to support the load; and output voltage keeps dropping. Once higher, the inductor current charges the capacitor and provides the load. During phase 2 (represented by the brown path), P_{SW} is turned OFF for T_{OFF} time duration and to prevent sudden change in the inductor current, the diode (D_0) turns ON connecting the output filter to ground. The inductor current ramps down with a slope, $m_2 = -V_{OUT}/L$.

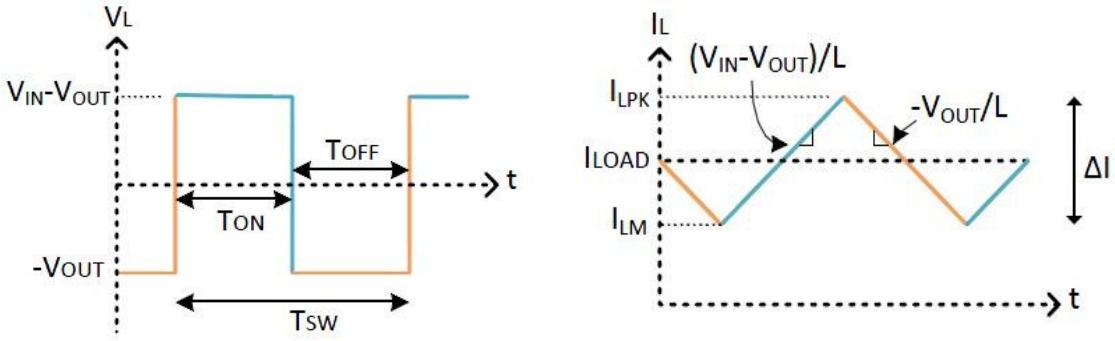


Figure 3. Inductor voltage and current waveforms in steady state.

In steady state (DC), the average value of inductor current should be equal to the load current as the capacitor blocks DC. Also, the inductor current value at the beginning of T_{ON} and at that at the end of T_{OFF} would be the same at steady state as depicted in

Figure 3. For this to happen, the average voltage across the inductor in steady state should be zero.

$$(V_{IN} - V_{OUT}) * T_{ON} - V_{OUT} * T_{OFF} = 0$$

$$V_{OUT} = \frac{T_{ON}}{T_{SW}} * V_{IN} \quad ; where\ T_{SW} = T_{ON} + T_{OFF} \qquad [Eq.\ 2.1]$$

The inductor current ripple is given by,

$$\Delta I = \frac{V_{IN} - V_{OUT}}{L} * T_{ON} = \frac{V_{OUT}}{L} * T_{OFF}$$

$$I_{LM} = I_{LOAD} - \frac{\Delta I}{2} = I_{LOAD} - \frac{V_{IN} - V_{OUT}}{2L} * T_{ON} \qquad [Eq.\ 2.2]$$

$$I_{LPK} = I_{LOAD} + \frac{\Delta I}{2} = I_{LOAD} + \frac{V_{IN} - V_{OUT}}{2L} * T_{ON} \qquad [Eq.\ 2.3]$$

The inductor maintains a continuous current in the converter if $I_{LM} > 0$. This mode of operation is called the Continuous Conduction Mode (CCM) and the output is independent of the load in this mode. As the load current reduces, the inductor current may go to zero at the end of each cycle depending on the values of V_{IN}, V_{OUT}, L and T_{SW} as depicted in Figure 4. The diode (D_0) gets reverse biased and prevents the inductor current flow in the opposite direction to ground. This prevents unnecessary discharge of the output capacitor. The converter is then said to be in Discontinuous Conduction Mode (DCM) and the characteristics of the converter is different from that in CCM.

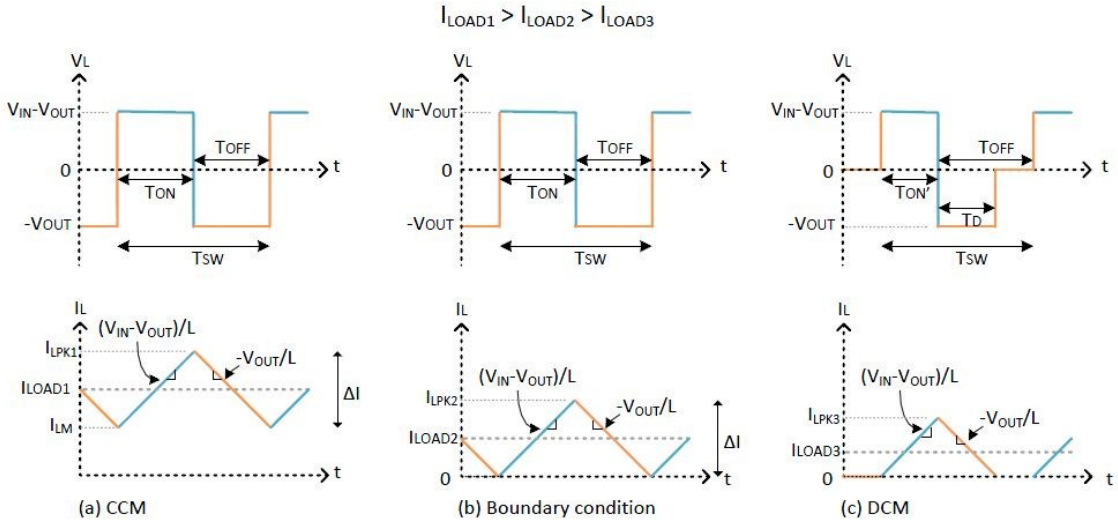


Figure 4. Inductor voltage and current waveforms in steady state for different loads.

Applying the inductor volt-sec balance in Fig 4(c),

$$(V_{IN} - V_{OUT}) * T_{ON'} - V_{OUT} * T_D = 0$$

$$T_D = \frac{(V_{IN} - V_{OUT})}{V_{OUT}} * T_{ON'} \qquad [Eq.\ 2.4]$$

Knowing that the average inductor current should be equal to the load, we can write,

$$\frac{V_{IN} - V_{OUT}}{2L} * \frac{T_{ON'} + T_D}{T_{SW}} = I_{LOAD3}$$

Substituting for T_D, V_{OUT} in DCM can be expressed as,

$$V_{OUT} = \frac{V_{IN}}{1 + \frac{2LI_{LOAD}T_{SW}}{V_{IN}T_{ON}}} \qquad [Eq.\ 2.5]$$

If a resistive load is considered, such that $I_{LOAD} = V_{OUT}/R_{LOAD}$

$$V_{OUT} = \frac{2V_{IN}}{1 + \sqrt{1 + \frac{8LT_{SW}}{R_{LOAD}T_{ON}^2}}} \qquad [Eq.\ 2.6]$$

Thus for a given T_{ON}, V_{OUT} is also a function of the load in DCM. Hence the Control loop would have to vary the ON time in accordance with the load such that the output voltage is maintained constant. The load below which a converter operates in DCM (Boundary condition) can be found by equating $I_{LM} = 0$ in Eq. 2.2.

$$I_{LOAD|boundary} = I_{CDB} = \frac{\Delta I}{2} = \frac{V_{IN} - V_{OUT}}{2L} * T_{ON} \qquad [Eq.\ 2.7]$$

The high frequency ripple component in the inductor current flows through the output capacitor generating a voltage ripple. For a given V_{IN}, V_{OUT}, L, C and T_{SW}, the current ripple would be smaller in DCM and so would be the voltage ripple. Integrating the current through the capacitor in CCM,

$$\Delta V = \frac{\Delta I * T_{SW}}{8C} \qquad [Eq.\ 2.8]$$

The diode (D_0) in Figure 2 could be replaced by an NMOS switch to have a CCM operation throughout as shown in Figure 5. Such a converter is often termed as a Synchronous Buck converter. At light loads, a portion of the charge dumped on the output capacitor is returned to supply and ground degrading the efficiency in these converters. Hence, a Zero Current Detector (ZCD) block is often incorporated to sense the inductor current going to zero and turn OFF the NMOS, so as to force DCM operation at light loads.

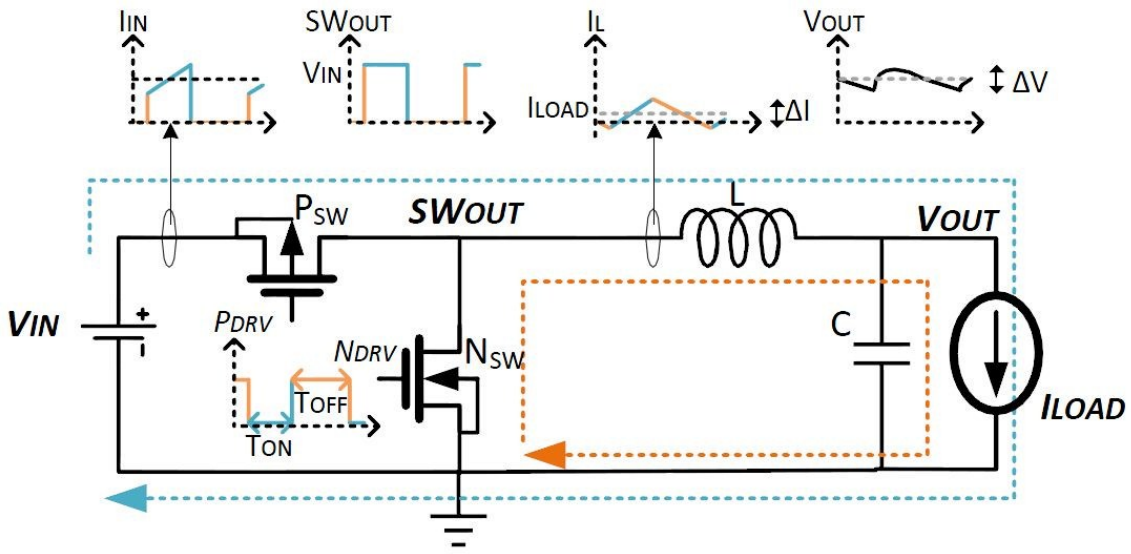


Figure 5. Synchronous buck converter with CCM at light load**.**

The Analysis done till now has been on an ideal Buck converter. Due to the turn ON and turn OFF delays in the actual switch, both the P_{SW} and N_{SW} could be potentially ON at the same time resulting in a large shoot-through current from supply to ground during switching. To prevent this, the gate drives (P_{DRV} and N_{DRV}) have a non-overlap region such that both switches are OFF for a short duration between switching (termed as the dead-time, T_{DT}). The body diode of the switches turns ON during this time to maintain the current through the inductor.

2.1 Small signal modeling

To build a stable loop around the buck converter, we need to know the small signal behavior of the converter to perturbations in the control inputs like the supply voltage and the on-time (T_{ON}). The switching converters are time varying systems, but if the frequency of perturbations is much lower than the switching frequency, we can assume them to be constant during one switching period and use an averaged model. The switch network is considered as a two port network and the waveforms across the port are averaged to develop what is called the Averaged Switch Model [7-9]. An important feature of this approach is that the same model can be used in many different converter configurations without the need for re-derivation. The key step in circuit averaging is to replace the converter switches with voltage and current sources, to obtain a time invariant circuit topology. The waveforms of the voltage and current generators are defined to be identical to the switch waveforms of the original converter. Once a time-invariant circuit network is obtained, then the converter waveforms are averaged over one switching period to remove the switching harmonics. Any non-linear element in the averaged circuit model can then be perturbed and linearized, leading to the small signal ac model [5].

The Synchronous Buck converter waveforms with the non-idealities considered can be represented as shown in Figure 6. 'R_P' denotes the overall resistance in the ON (supply) path and 'R_N' represents the resistance in the OFF (ground) path. This includes the MOS switch resistance, layout, bond-wire and PCB routing resistances. 'R_L' denotes

the resistance in the SW_{OUT} path including the inductor DC resistance. R_{ESR} is the effecting series resistance of the capacitor.

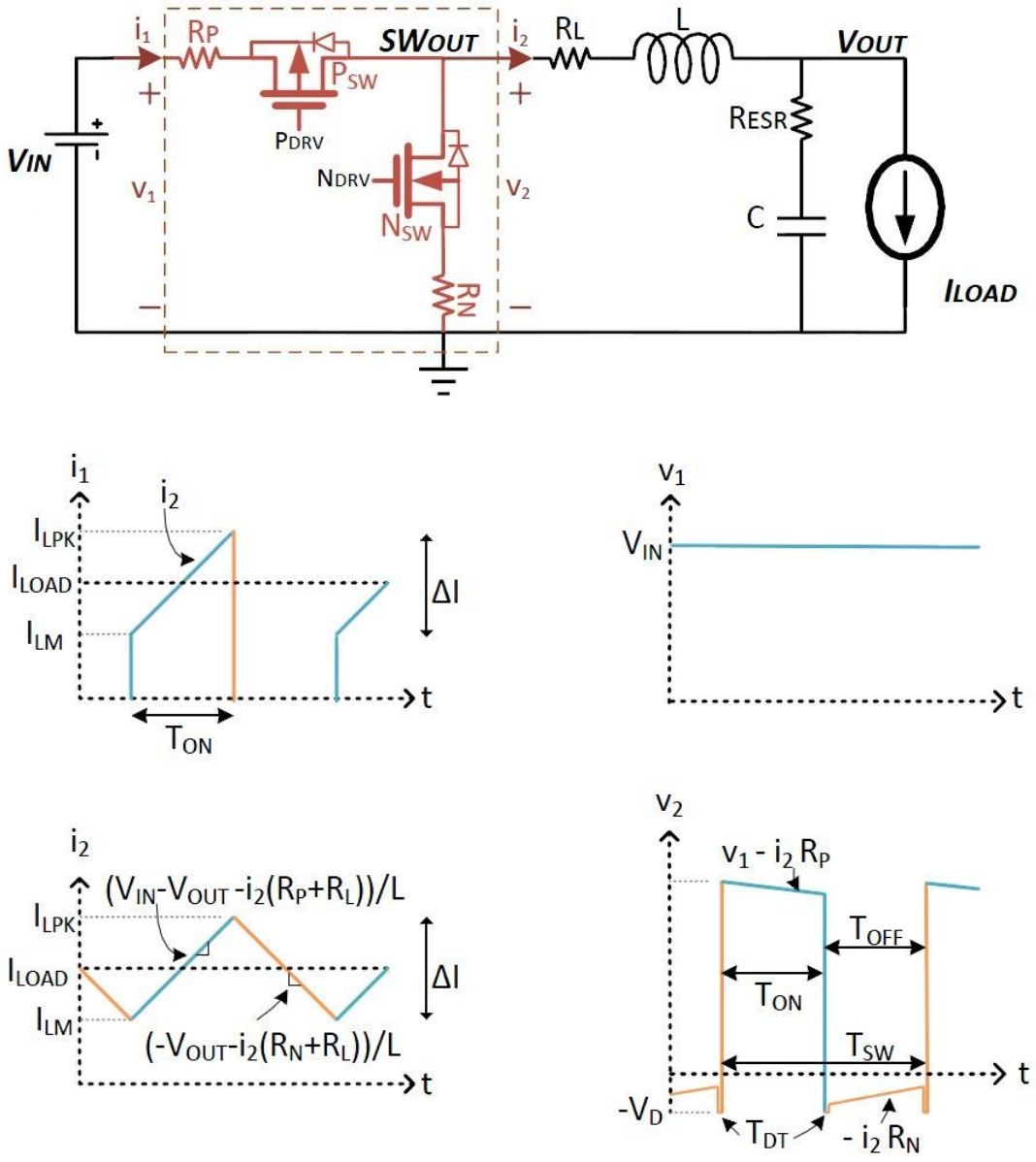


Figure 6. Synchronous buck converter (non-ideal) and associated waveforms in CCM.

The switch network is converted to a two port network with the terminal current and voltage waveforms as shown in Figure 6. As with any two port network, two of the four terminal voltages and currents can be taken as independent inputs to the switch network and the remaining two are viewed as dependent outputs of the switch network. Assuming $v_1(t)$ and $i_2(t)$ to be the independent port parameters, and averaging the waveforms over a switching time period to get rid of the switching ripples in the analysis, we can write

$$< v_1(t) >=< v_{IN}(t) > \qquad [Eq.\ 2.9]$$

$$<i_2(t) > = \ < i_L(t) > = < i_{LOAD}(t) > \qquad [Eq.\ 2.10]$$

$$< i_1(t) > = \frac{t_{ON}(t)}{T_{SW}} < i_2(t) > \qquad [Eq.\ 2.11]$$

$$<v_2(t)> \ = \frac{t_{ON}(t)}{T_{SW}} <v_1(t)> \ - \left\{ \frac{t_{ON}(t)}{T_{SW}} R_P \ + \frac{1 - t_{ON}(t)}{T_{SW}} R_N \right\} <i_2(t)>$$

$$\gg \qquad [Eq.\ 2.12]$$

The above equations assume a constant switching frequency and neglect the effect of the dead-time assuming it is insignificant compared to the switching time period. As can be seen, the equations involve the multiplication of time varying quantities which makes it nonlinear. To get a small signal ac model at a quiescent operating value (I,V) we assume that the input voltage ($v_{IN}(t)$), inductor current ($i_L(t)$) , and ON time (t_{ON}) are equal to some given quiescent values V_{IN} , I_{LOAD} and T_{ON} plus some superimposed small ac variations as shown:

$$< v_1(t) >= V_{IN} + \hat{v_{IN}}(t)$$

$$<i_2(t) > = I_{LOAD} + \hat{i_L}(t)$$

$$t_{ON}(t) = T_{ON} + \hat{t_{ON}}(t)$$

Assuming the perturbations to be small, the other averaged parameters would also be equal to their corresponding quiescent values plus small ac variations in response to these inputs. The non-linear equation can then be linearized ignoring the second order terms in the expansion. This gives the linearized equations as

$$< i_1(t) > = \frac{T_{ON} + \hat{t_{ON}}(t)}{T_{SW}} [I_{LOAD} + \hat{i_L}(t)]$$

$$I_1 + \hat{i_1}(t) = \left[\frac{T_{ON}}{T_{SW}} I_{LOAD}\right] + \left[\frac{\hat{t_{ON}}(t)}{T_{SW}} I_{LOAD} + \frac{T_{ON}}{T_{SW}} \hat{i_L}(t)\right] \qquad [Eq.\ 2.13]$$

$$\begin{aligned} <v_2(t)> \quad = \quad & \frac{T_{ON} + \hat{t_{ON}}(t)}{T_{SW}} [V_{IN} + \hat{v_{IN}}(t)] \\ & - \left\{\frac{T_{ON} + \hat{t_{ON}}(t)}{T_{SW}} R_P + \frac{1 - T_{ON} - \hat{t_{ON}}(t)}{T_{SW}} R_N\right\} [I_{LOAD} + \hat{i_L}(t)] \end{aligned}$$

$$\begin{aligned} V_2 + \hat{v_2}(t) \; = \quad & \left[\frac{T_{ON}}{T_{SW}} V_{IN} - \left(\frac{T_{ON}}{T_{SW}} R_P + \frac{1 - T_{ON}}{T_{SW}} R_N\right) I_{LOAD}\right] \\ & + \left[\frac{T_{ON}}{T_{SW}} \hat{v_{IN}}(t) + \{V_{IN} - (R_P - R_N) * I_{LOAD}\} \frac{\hat{t_{ON}}(t)}{T_{SW}}\right. \\ & \left. - \left(\frac{T_{ON}}{T_{SW}} R_P + \frac{1 - T_{ON}}{T_{SW}} R_N\right) \hat{i_L}(t)\right] \qquad [Eq.\ 2.14] \end{aligned}$$

Reconstructing the switch network from these averaged equations, we obtain the small signal ac model for the converter operated in CCM as shown in Fig 7. 'd(t)' represents the small signal variations in the duty cycle ($D = T_{ON}/T_{SW}$). For a constant switching frequency, $d(t) = \hat{t}_{ON}(t) / T_{SW}$.

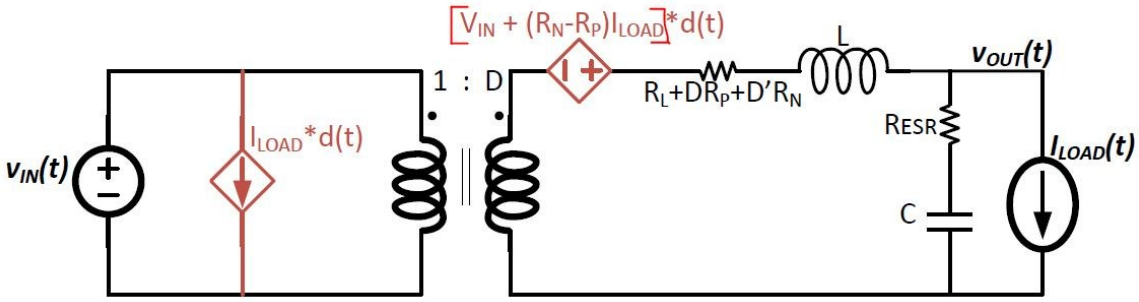


Figure 7. Small signal model of synchronous buck converter in CCM**.**

Since most converters operate in the discontinuous conduction mode at light load conditions, small signal ac DCM models are needed to ensure that the control loop is correctly designed. As seen before, the output voltage depends on the load in DCM. So the converter no longer has a voltage source output characteristics; hence the dc transformer model is less appropriate. Here we have developed a "loss free" model of the DCM buck using the averaged switch modeling technique. The port waveforms associated with a synchronous converter in forced DCM can be found in Figure 8. As in CCM analysis, $v_1(t)$ and $i_2(t)$ are assumed to be the independent port parameters and are given by Eq. 2.9 and Eq. 2.10. The average value of output $\langle v_{OUT} \rangle$ is also used here as an external parameter to determine the N_{SW} conduction time T_D.

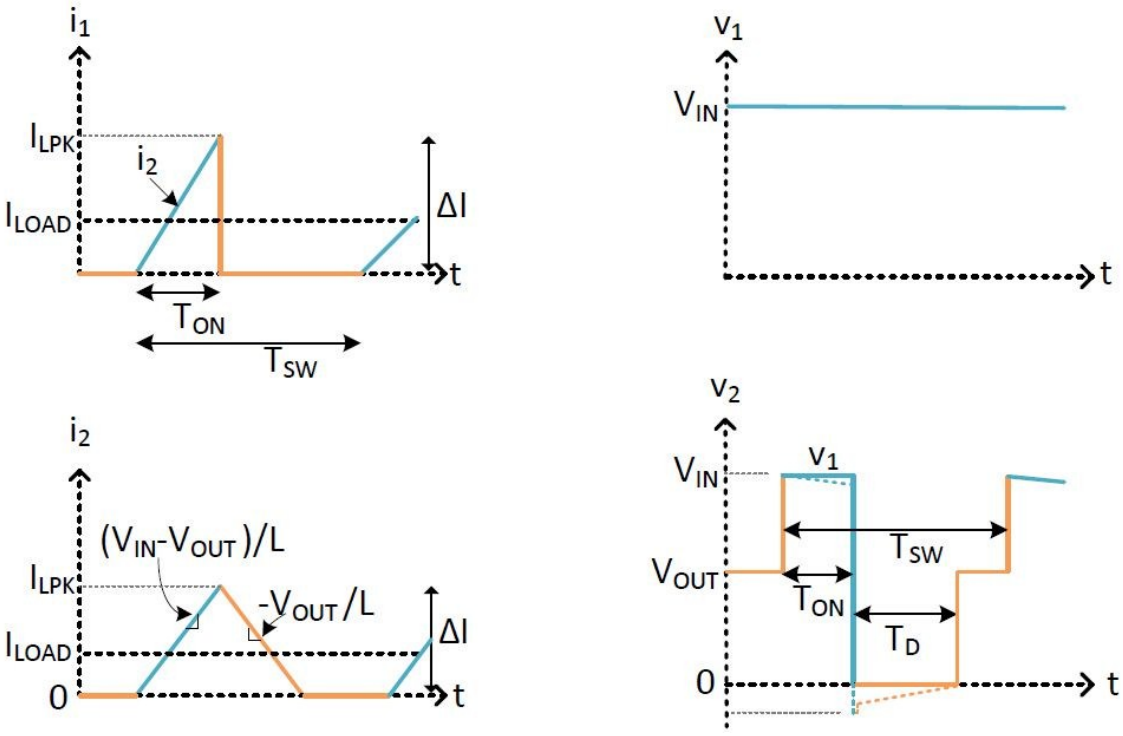


Figure 8. Ideal and actual buck converter port waveforms in DCM**.**

$$< i_1(t) > = \frac{< v_{IN}(t) > - < v_{OUT}(t) >}{2L} * \frac{t_{ON}^2(t)}{T_{SW}} \qquad [Eq.\ 2.15]$$

$$< v_2(t) > = \frac{t_{ON}(t)}{T_{SW}} < v_1(t) > + \left\{1 - \frac{t_{ON}(t)}{T_{SW}} - \frac{t_D(t)}{T_{SW}}\right\} < v_{OUT}(t) > \quad [Eq.\ 2.16]$$

From the inductor current waveform in Figure 8, we can write,

$$< i_2(t) > = \frac{< v_{IN}(t) > - < v_{OUT}(t) >}{2L} * \frac{t_{ON}(t)\{t_{ON}(t) + t_D(t)\}}{T_{SW}}$$

⇨

$$< t_D(t) > = \frac{2LT_{SW} < i_2(t) >}{t_{ON}(t)(< v_{IN}(t) > - < v_{OUT}(t) >)} - t_{ON}(t) \qquad [Eq.\ 2.17]$$

Applying this in Eq. 2.16,

$$<v_2(t)> = <v_{OUT}(t)> + \frac{t_{ON}(t)}{T_{SW}}<v_1(t)> - \frac{2LT_{SW}<i_2(t)>}{<v_{IN}(t)> - <v_{OUT}(t)>} * \frac{<v_{OUT}(t)>}{t_{ON}(t)} \quad [Eq.\ 2.18]$$

Using linearized Taylor series expansion for Eq. 2.15 and Eq. 2.18,

$$I_1 + \hat{i_1}(t) = \left[\frac{(V_{IN} - V_{OUT})T_{ON}^2}{2LT_{SW}}\right] + \left[\frac{T_{ON}^2}{2LT_{SW}}\left(\hat{v_{IN}}(t) - \hat{v_{OUT}}(t)\right) + \frac{(V_{IN} - V_{OUT})T_{ON}}{LT_{SW}}\hat{t_{ON}}(t)\right] \quad [Eq.\ 2.19]$$

$$V_2 + \hat{v_2}(t) = \left[V_{OUT} + \frac{T_{ON}V_{IN}}{T_{SW}} - \frac{2LI_{LOAD}V_{OUT}}{T_{ON}(V_{IN} - V_{OUT})}\right] + \left[\left(\frac{T_{ON}}{T_{SW}} + \frac{2LI_{LOAD}V_{OUT}}{T_{ON}(V_{IN} - V_{OUT})^2}\right)\hat{v_{IN}}(t) + \left(1 - \frac{2LI_{LOAD}V_{IN}}{T_{ON}(V_{IN} - V_{OUT})^2}\right)\hat{v_{OUT}}(t) + \left(\frac{V_{IN}}{T_{SW}} + \frac{2LI_{LOAD}V_{OUT}}{T_{ON}^2(V_{IN} - V_{OUT})}\right)\hat{t_{ON}}(t) - \frac{2LV_{OUT}}{T_{ON}(V_{IN} - V_{OUT})}\hat{i_L}(t)\right] \quad [Eq.\ 2.20]$$

For an ideal converter in steady state, $V_2 = V_{OUT}$.

$$\frac{T_{ON}V_{IN}}{T_{SW}} = \frac{2LI_{LOAD}V_{OUT}}{T_{ON}(V_{IN} - V_{OUT})} \qquad [Eq.\ 2.21]$$

$$V_{OUT} = \frac{2V_{IN}}{1 + \sqrt{1 + \frac{8LT_{SW}}{R_{LOAD}T_{ON}^2}}} \quad for\ a\ resistive\ load\ as\ shown\ earlier.$$

From Eq. 2.17 and Eq. 2.21, in steady state,

$$T_{ON} = \sqrt{\frac{2LT_{SW}I_{LOAD}V_{OUT}}{V_{IN}(V_{IN} - V_{OUT})}} \quad and \quad T_D = T_{ON} * \frac{V_{IN} - V_{OUT}}{V_{OUT}} \qquad [Eq.\ 2.22]$$

Applying Eq. 2.21 in Eq. 2.19 and Eq. 2.20, we can obtain a simplified form and derive the small signal DCM model for the ideal converter as shown in Figure 9. It is to be noted that the parasitic resistances in the circuit is ignored for this analysis.

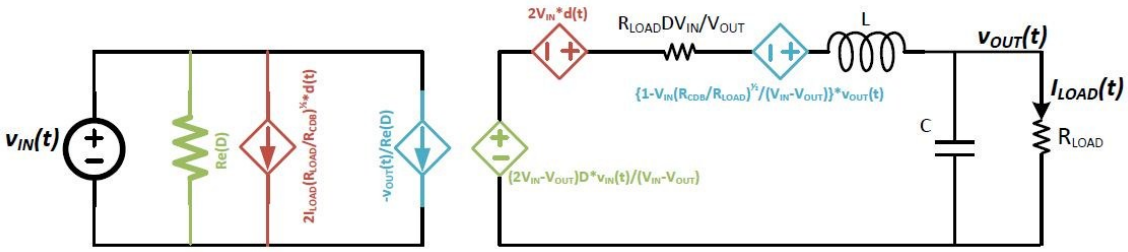


Figure 9. Small signal model of ideal buck converter in DCM**.**

The CCM and DCM models mentioned here provides an easy way to analyze the converter in frequency domain and design a stable compensation network when the bandwidth of the overall system is kept well below the switching frequency. When bandwidths higher than $F_{SW}/10$ are to be designed, the phase degradation due to the sampling effect has to be considered. The sampled-data analysis [10] and its approximations would come handy in such scenarios.

2.2 Power loss estimation

As mentioned earlier, practical implementation of the buck converter suffers from non-idealities in the switches and the passive components, which lead to power loss in the converter. Figure 10 shows the implementation of a complete buck converter. The major contributors to loss can be classified as in [11-13].

2.2.1 Conduction losses

These depend on the RMS value of the inductor current and the resistances in the power flow paths weighted in proportion to their ON time. The resistance seen during T_{ON} is (R_P+R_L) and that during T_{OFF} (T_D in DCM) is (R_N+R_L). The relative contributions of these resistors remain the same in both CCM and DCM and can be approximated as,

$$R_{DC} = \frac{V_{OUT}}{V_{IN}} R_P + \frac{V_{IN} - V_{OUT}}{V_{IN}} R_N + R_L$$

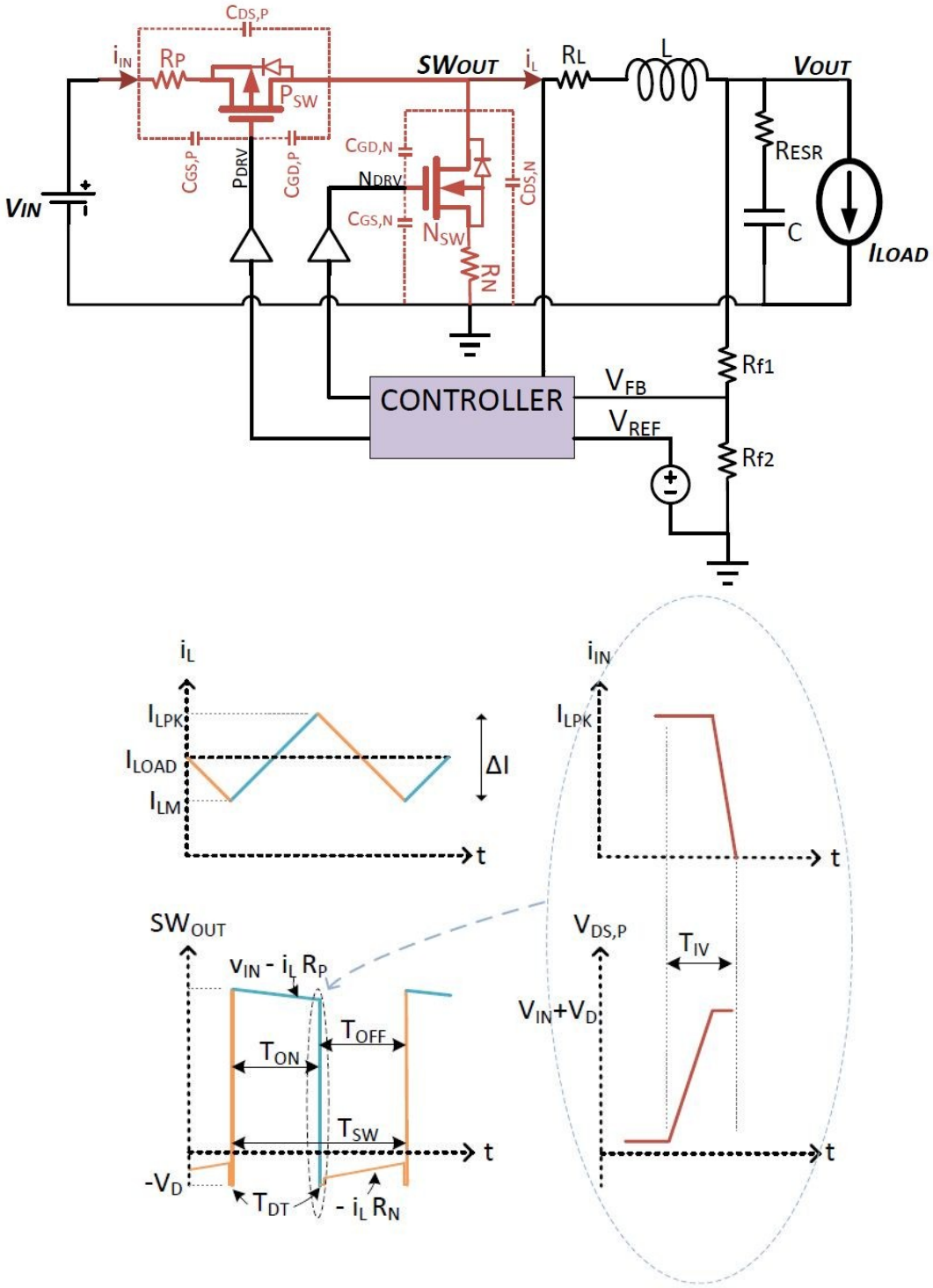


Figure 10. Closed loop buck converter with loss contributors and corresponding waveforms.

Only the ripple component in the inductor current flows through R_{ESR} and hence the conduction loss is expressed as the summation of the DC and AC components in Eq. 2.23. The equivalent AC resistance, $R_{AC} = R_{DC} + R_{ESR}$

$$P_{COND} = P_{C_{DC}} + P_{C_{AC}} = I_{LOAD}^2 R_{DC} + I_{AC,RMS}^2 R_{AC} \qquad [Eq.\ 2.23]$$

For CCM operation, $I_{AC,RMS}^2 = \frac{\Delta I^2}{12}$, where ΔI is the peak − peak current ripple

$$P_{COND_{CCM}} = I_{LOAD}^2 R_{DC} + \frac{(V_{IN} - V_{OUT})^2 V_{OUT}^2}{12 L^2 V_{IN}^2 F_{SW}^2} R_{AC} \qquad [Eq.\ 2.24]$$

To reduce the conduction loss at a given load, the resistance should be minimized and/or the current ripple should be reduced. Reducing the resistance involves huge MOSFET switches and wide routing; both of which consumes more area and add larger parasitic capacitance. To reduce the current ripple, the inductance (L) and/or the switching frequency (F_{SW}) would have to be increased. For DCM operation,

$$I_{AC,RMS}^2 = I_{L,RMS}^2 - I_{L,AVG}^2 = \frac{I_{LPK}^2}{3} * \frac{T_{ON} + T_D}{T_{SW}} - I_{LOAD}^2 \qquad [Eq.\ 2.25]$$

By equating the average inductor current to load current in Figure 8, the peak inductor current in DCM, I_{LPK} can be expressed as:

$$I_{L,PK} = \frac{2 I_{LOAD} T_{SW}}{T_{ON} + T_D} \qquad [Eq.\ 2.26]$$

Substituting Eq. 2.22 and Eq. 2.26 in Eq. 2.25,

$$I_{AC,RMS}^2 = \frac{4}{3} I_{LOAD}^{1.5} \sqrt{\frac{(V_{IN} - V_{OUT})V_{OUT}}{2LF_{SW}V_{IN}}} - I_{LOAD}^2$$

The conduction losses in DCM can therefore be expressed as:

$$P_{COND_{DCM}} = I_{LOAD}^2 R_{DC} + \left(\frac{4}{3} I_{LOAD}^{1.5} \sqrt{\frac{(V_{IN} - V_{OUT})V_{OUT}}{2LF_{SW}V_{IN}}} - I_{LOAD}^2 \right) (R_{DC} + R_{ESR})$$

$$\rightarrow \qquad [Eq.\ 2.27]$$

If capacitor with negligible ESR (MLCCs) is used at output, the conduction loss in DCM is proportional to 1.5th power of I_{LOAD} and inversely proportional to the root of the switching frequency as shown in Eq. 2.28.

$$P_{COND_{DCM}} = \frac{4}{3} I_{LOAD}^{1.5} \sqrt{\frac{(V_{IN} - V_{OUT})V_{OUT}}{2LF_{SW}V_{IN}}} R_{DC} \qquad [Eq.\ 2.28]$$

2.2.2 Switching losses

These happens during each switching of the power MOSFETs and is hence proportional to the switching frequency. The parasitic gate-source and gate-drain capacitances of P_{SW} and N_{SW} needs to be charged and discharged by the driving circuitry through a resistive switch. The energy required is given by $\Sigma C_i \Delta V_i^2$, where C_i denotes each parasitic capacitance and ΔV_i denotes the voltage change across it during switching.

Determining the ΔV_i associated with each capacitor from the waveforms in Fig 6,8 and 10; we can write the Gate Drive Power losses as,

$$P_{SW_{GD}} = \left[\left(C_{GS_{PSW}} + C_{GS_{NSW}}\right)V_{IN}^2 + C_{GD_{PSW}}(2V_{IN} + V_D)^2 + C_{GD_{NSW}}(V_{IN} - V_D)^2\right]F_{SW}$$

Assuming the diode drop to be much less than V_{IN} ,

$$P_{SW_{GD}} = \left(C_{GS_{PSW}} + C_{GS_{NSW}} + 4C_{GD_{PSW}} + C_{GD_{NSW}}\right)V_{IN}^2 F_{SW} \qquad [Eq.\ 2.29]$$

The inductive load seen by the switches causes overlap between current (i_D) and voltage across the switch (v_{DS}) during transition. The current in P_{SW} has to rise to I_{LM} before the N_{SW} body diode turn OFF and SW_{OUT} node ramps to V_{IN} in CCM. Similarly, the voltage across P_{SW} has to increase to V_{IN}+V_D before the body diode can turn ON and supply the inductor current as shown in the zoomed box in Figure 10. IV overlap loss also occurs during N_{SW} turn ON and OFF, but the magnitude is much lower as the voltage swing is only V_D (due to the non-overlap time in between). Neglecting the clamping effect due to the parasitic inductances [14], IV overlap loss in CCM can be written as,

$$P_{SW_{IV,CCM}} = \left[\frac{1}{2}(V_{IN} + V_D)I_{LM}t_{IV_{Pon}} + \frac{1}{2}(V_{IN} + V_D)I_{LPK}t_{IV_{Poff}} + \frac{1}{2}V_D I_{LPK}t_{IV_{Non}} + \frac{1}{2}V_D I_{LM}t_{IV_{Noff}}\right]F_{SW} \qquad [Eq.\ 2.29]$$

Where $t_{IV\ Pon}$, $t_{IV\ Poff}$, $t_{IV\ Non}$ and $t_{IV\ Noff}$ are the overlap time during P_{SW} ON, P_{SW} OFF, N_{SW} ON and N_{SW} OFF respectively. Assuming all of them to be same (t_{IV}) and knowing that the average inductor current is the load current,

$$P_{SW_{IV,CCM}} = \quad (V_{IN} + 2V_D) I_{LOAD} t_{IV} * F_{SW} \qquad [Eq.\ 2.30]$$

In forced DCM, N_{SW} turns OFF when the inductor current reaches zero (ZCD output) and P_{SW} turns ON at zero current. The IV overlap loss is DCM can thus be obtained by using $I_{LM} = 0$ in Eq. 2.29 to give,

$$P_{SW_{IV,DCM}} = \frac{1}{2}(V_{IN} + 2V_D) I_{LPK} t_{IV} * F_{SW}$$

Substituting I_{LPK} from Eq. 2.26 and T_{ON} from Eq 2.22,

$$P_{SW_{IV,DCM}} = (V_{IN} + 2V_D) t_{IV} \sqrt{\frac{V_{OUT}(V_{IN} - V_{OUT})}{2LV_{IN}}} * \sqrt{I_{LOAD} F_{SW}} \qquad [Eq.\ 2.31]$$

As seen from Eq. 2.30 and Eq. 2.31, IV overlap loss is proportional to I_{LOAD} and F_{SW} in CCM and proportional to their square root in DCM.

The dead-time (t_{DT}) introduced to prevent large shoot through current during switching results in power loss ($P_{SW,DT}$). Similar to the earlier observation, the dependence of this loss vary in CCM and DCM as shown by Eq. 2.32 and Eq. 2.33.

$$P_{SW_{DT}} = (I_{LPK} + I_{LM}) V_D t_{DT} * F_{SW}$$

$$P_{SW_{DT,CCM}} = 2I_{LOAD}V_D t_{DT} * F_{SW} \quad [Eq\ 2.32]$$

$$P_{SW_{DT,DCM}} = V_D t_{DT}\sqrt{\frac{V_{OUT}(V_{IN}-V_{OUT})}{2LV_{IN}}} * \sqrt{I_{LOAD}F_{SW}} \quad [Eq.2.33]$$

Since the pre-driver stage does not have an inbuilt dead-time, they would have some shoot through current; but is neglected in this analysis. Thus the overall switching losses can be written as,

$$P_{SW} = P_{SW_{GD}} + P_{SW_{IV}} + P_{SW_{DT}}$$

$$P_{SW_{CCM}} = C_{G_{eff}}V_{IN}^2 F_{SW} + \{(V_{IN} + 2V_D)t_{IV} + 2V_D t_{DT}\} * I_{LOAD}F_{SW}$$

$$P_{SW_{DCM}} = C_{G_{eff}}V_{IN}^2 F_{SW} + \{(V_{IN}+2V_D)t_{IV} + V_D t_{DT}\}\sqrt{\frac{V_{OUT}(V_{IN}-V_{OUT})}{2LV_{IN}}}\sqrt{I_{LOAD}F_{SW}}$$

2.2.3 Quiescent current losses

This is associated with the additional power required by control circuitry. This would include the reference generators, clock generator, error amplifier, comparators, protection circuits etc. depending on the implementation and the mode of operation. Since most of these blocks work from the same supply voltage, the quiescent power loss can be expressed as (ignoring the component that depends on switching frequency),

$$P_{IQ} = V_{IN} * I_Q \quad [Eq.\ 2.34]$$

CHAPTER III

CONTROL STRATEGIES

In a DC-DC converter application, it is desired to keep the output voltage fixed in spite of the variations in circuit elements, input voltage, and load current. This cannot be expected of a converter with fixed duty cycle; we require a negative feedback. But before designing a negative feedback control system, it is necessary to understand the variations of output voltage with respect to these parameters without the feedback viz. the transfer functions in open loop. From the small signal models derived in chapter II, we could find the response of the converter in CCM and DCM to perturbations in v_{IN} or *d*, keeping the other constant. Figure 11 shows the bode plot of the converter response to *d* variations in CCM and DCM operation. As shown by Eq. 3.1 and 3.2, assuming $R_{DC} << R_{LOAD}$, the CCM response has a double pole at the LC frequency while the DCM converter has a load dependent single pole response owing to reset of the inductor current every cycle.

$$G_{vd}(s) = \frac{\hat{v_{OUT}}(s)}{\hat{d}(s)} \Big|_{\hat{v_{IN}}(s)=0}$$

$$G_{vd}(s)|_{CCM} = \frac{V_{IN}(1 + sR_{ESR}C)}{1 + s\left(\frac{L}{R_{LOAD}} + R_{AC}C\right) + s^2LC} \qquad [Eq.\ 3.1]$$

$$G_{vd}(s)|_{DCM} \approx \frac{\frac{2V_{IN}(V_{IN} - V_{OUT})}{(2V_{IN} - V_{OUT})}\sqrt{\frac{R_{LOAD}}{R_{CDB}}}(1 + sR_{ESR}C)}{\left\{1 + \frac{s(V_{IN} - V_{OUT})R_{LOAD}C}{2V_{IN} - V_{OUT}}\right\}\left\{1 + \frac{sL}{\sqrt{R_{CDB}R_{LOAD}}}\right\}} \qquad [Eq.\ 3.2]$$

Where R_{CDB} is the load corresponding to CCM-DCM boundary and is given by (in ideal converter),

$$R_{CDB} = \frac{V_{OUT}}{I_{CDB}} = \frac{2LV_{IN}}{(V_{IN} - V_{OUT})T_{SW}} \qquad [Eq.\ 3.3]$$

The DC gain is dependent on the supply voltage VIN and is very low in CCM. The CCM response has a Gain peaking at the LC frequency and the phase drops drastically. The Switch, Inductor and routing resistance in the power flow path provides damping. The Powerstage in DCM has higher DC Gain but very low bandwidth which depends on the load. Since MLC Capacitors have very low ESR, 2mΩ was used in simulation. L=1uH, C=10uF, T_{sw}= 333ns was used. The ESR zero was at high frequency and hence didn't provide any phase improvement around the UGB.

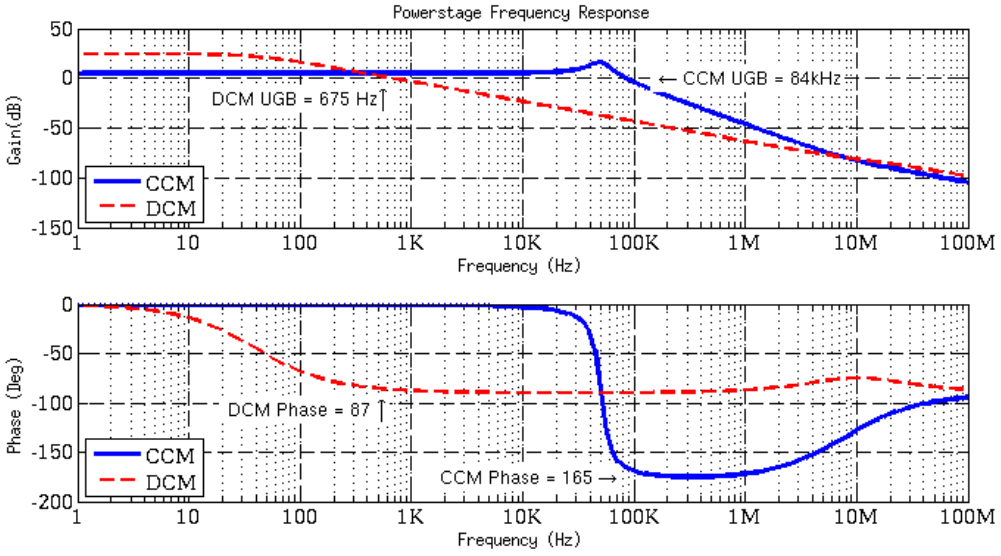


Figure 11. Buck converter AC Response in CCM and DCM.

3.1. PWM control

The constant frequency PWM is most widely used control strategy for the DC-DC converter. Figure 12 shows a PWM controlled buck converter. The output voltage is level shifted using the feedback network and applied to an error amplifier which compares it with the required reference and generates an error signal. Proper frequency compensation is applied to this signal so as to achieve a stable control loop. This error signal is then compared with a ramp signal of the required switching frequency to generate a pulse width modulated control signal to the power switches.

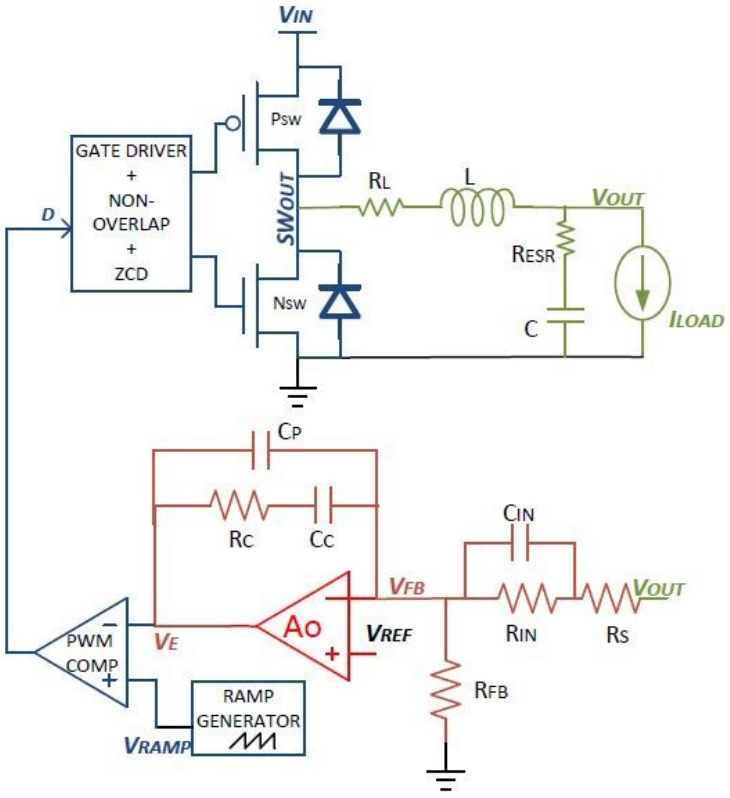


Figure 12. Type III PWM voltage mode loop.

Depending on how the Ramp signal is generated, we have:

(i) Voltage Mode Control – Ramp signal independent of output voltage and current

(ii) Current Mode Control – Ramp signal generated from the inductor current ramp. It requires additional circuitry to sense the inductor current which can also be used for over current protection. It also needs an artificial ramp signal to be superimposed on the inductor current ramp for stability in higher duty cycle operation. Since the inductor current is controlled using a loop, the converter has a single pole response which greatly simplifies the compensation.

(iii) V^2 Control– Ramp signal is generated from the output waveform [15]. Since the high frequency information in the output is processed directly without the error amplifier, the error amplifier design is relaxed and can be optimized independent of the transient performance requirements of the loop. This control however requires a high ESR capacitor to generate a ramp signal of sufficient amplitude and hence cannot be implemented with cheap MLCC. There are modifications proposed which resemble the current mode control.

To lower the quiescent current, the current sense circuitry is avoided and a Voltage mode control loop is utilized in this work [16]. The Control loop should introduce sufficient low frequency gain to achieve good output accuracy. To mitigate the phase degradation due to the LC double pole, sufficient frequency compensation needs to be added at higher frequencies. The Unity Gain Bandwidth needs to be kept well below the switching frequency to avoid the aliasing effects of the sampled system. Type III compensation as shown in Figure 12 is well suited for high bandwidths with good phase

margin, especially when low ESR capacitors are used at output [17]. Eq. 3.4 gives the open loop transfer function of the control circuitry in CCM. Figure 13 shows the Bode plot for the loop Gain along with that for each block.

$$G_{v_{OL}}(s)|_{CCM} = \frac{(1+sR_CC_c)(1+sR_{IN}C_{IN})}{s(C_P+C_C)(R_S+R_{IN})\left(1+\frac{sR_CC_PC_C}{C_P+C_C}\right)\left(1+\frac{sR_{IN}R_SC_{IN}}{R_{IN}+R_S}\right)}$$

$$* \left(\frac{V_{IN}}{V_{RAMP}}\right) \frac{(1+sR_{ESR}C)}{1+s\left(\frac{L}{R_{LOAD}}+R_{AC}C\right)+s^2LC} \qquad [Eq.\ 3.4]$$

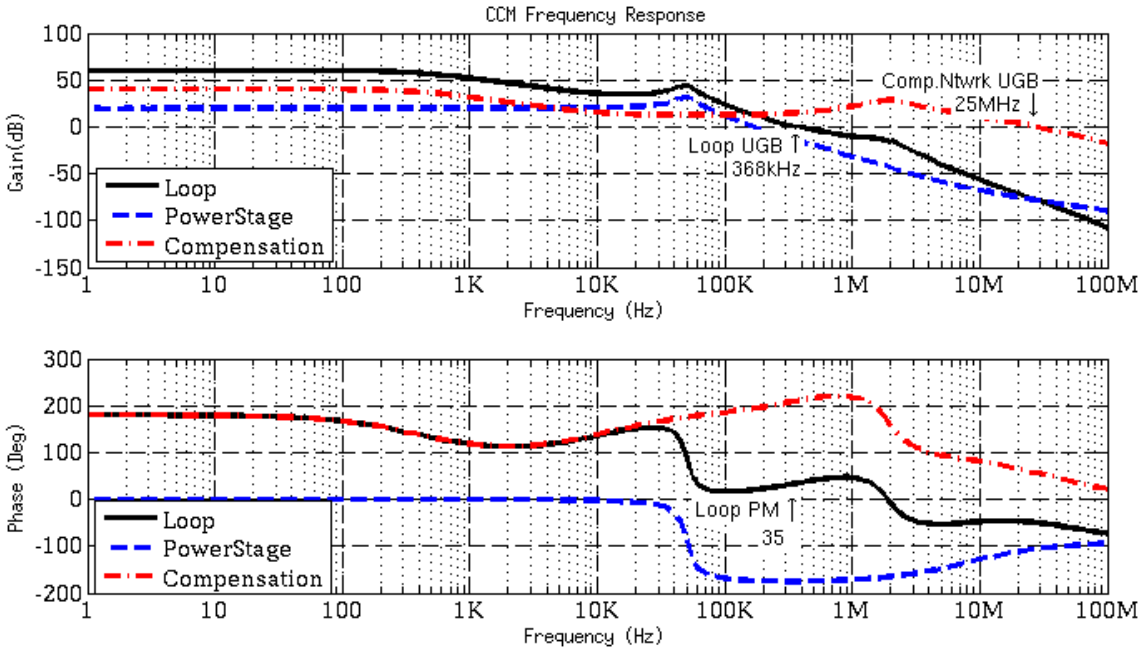


Figure 13. Bode plot for Type III compensation in CCM.

3.1.1 DC accuracy

Assuming very high DC Gain for the error amplifier, the closed loop tries to maintain the level shifted output voltage (V_{FB}) equal to the reference (V_{REF}) at DC.

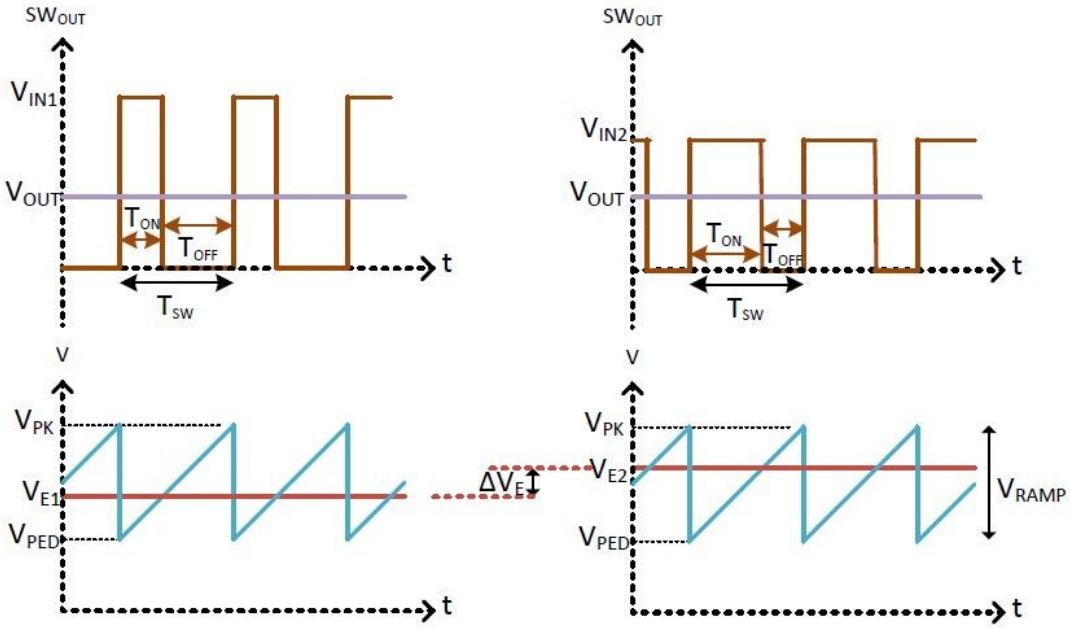
$$V_{OUT} * \frac{R_{FB}}{R_{FB}+R_S+R_{IN}} = V_{REF} \quad \text{or} \quad V_{OUT} = V_{REF} * \frac{R_{FB}+R_S+R_{IN}}{R_{FB}} \qquad [Eq.\ 3.5]$$

The overall loop DC Gain can be expressed as

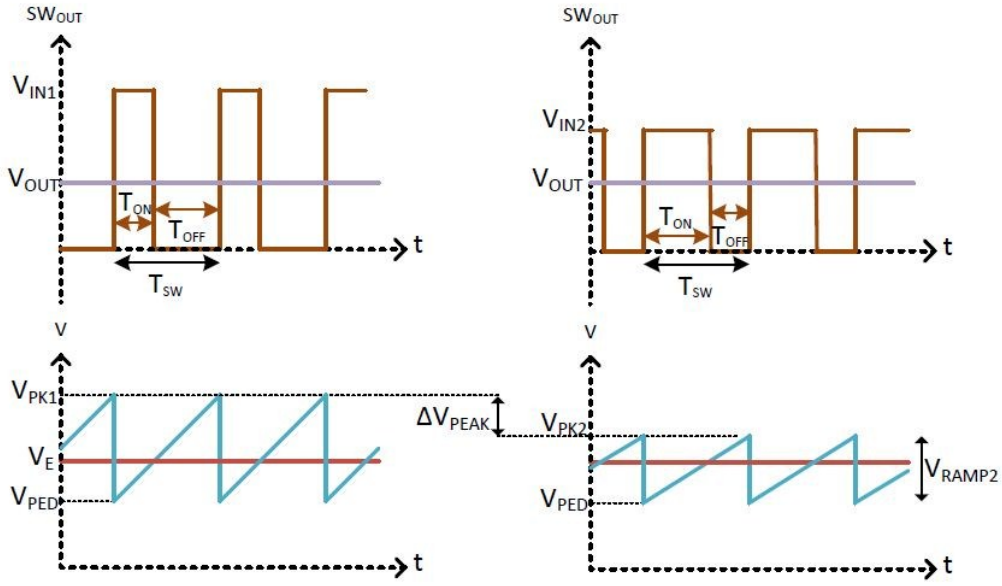
$$A_{OL} = A_{EA} * \beta * \frac{V_{IN}}{V_{RAMP}} \text{ ; Where feedback factor, } \beta = \frac{R_{FB}}{R_{FB}+R_S+R_{IN}} \qquad [Eq.\ 3.6]$$

Ignoring the mismatches, Accuracy is depended on Gain in the loop. That is, Higher Loop Gain corresponds to better Accuracy. For 1% Accuracy, we need a min. Loop Gain of 40dB (100 V/V). The mismatch generates additional error which could be trimmed to a great extent.

As the Supply voltage changes, the error voltage should change so as to change the duty cycle and maintain output constant. For a ΔVe change in the error voltage, the input of the amplifier needs a $\Delta Ve/A_{EA}$ change. To improve the Line regulation, a supply dependent Ramp is proposed [18]. This ensures the same steady state value of error voltage and thus improves the line regulation as shown in Figure 14. The Output Impedance and supply dependency of a closed loop converter is inversely proportional to the loop Gain. Thus by increasing the loop gain, we can improve Line/Load Regulation.



(a)



(b)

Figure 14. Error voltage variation with supply in (a) constant ramp and (b) supply dependent ramp scenario.

3.1.2 Transient regulation

To improve the transient performance we should have a high enough UGB and Phase margin for the loop. The highest UGB that could be designed is limited to $F_{SW}/5$ due to nyquist criterion (being a sampled data system). In many power supplies, the output capacitor determines how effective raising the crossover frequency will be. If the main performance objective is driven by step load requirements, there is no benefit in raising the crossover frequency above the output capacitor ESR frequency [19].

$$F_{cmax} < \min\left\{\frac{\mathrm{Fsw}}{5}, \frac{1}{2\pi\, \mathrm{R_{ESR}C}}\right\} \qquad [Eq.\ 3.7]$$

The lower limit on UGB is set by the LC frequency. As Voltage mode control drives the LC filter through controlled switching, it is prone to oscillate at the resonant frequency. To avoid this, we need to have high gain in the loop at this frequency.

For a sudden load step, the excess charge is supplied by the output capacitor till the loop responds and hence the output drops. For a load step of ΔI, the output would drop by $\Delta V = \Delta I * \frac{t_{res}}{C}$ with a response time of t_{res}. Hence, to lower the voltage dip for a given load step and capacitance, we need to minimize the response time. The response time of the loop is determined by its bandwidth and the inductor value.

$$\mathrm{t_{res}} < \frac{\Delta \mathrm{V} * \mathrm{C}}{\Delta \mathrm{I}}$$

$$F_{cmin} \gg \max\left\{\frac{3}{\{2\pi\sqrt{LC}\}}, \frac{1}{2\pi t_{res}}\right\} \qquad [Eq.\ 3.8]$$

There has been a lot of study done on the transient response of the control loop based on the output impedance, loop bandwidth, output filter parameters etc [20-28]. These analyses do not give a complete picture when the load change is associated with a change in the operating mode of the converter. For e.g. a load change from 1mA to 400mA may be associated with a change from DCM to CCM (when the inductor current is not allowed to be reversed in the converter). The circuit has different bandwidths at 1mA and 400mA loads and the ramp up of inductor current to the final state would depend on the supply, output and the inductance to some extend which is not predicted in the above analysis. To reduce this time and to speed up the inductor current ramp rate, a lower inductance is chosen at the expense of higher current ripple.

The transient response also depends on the state of the error voltage with respect to the ramp in PWM mode. The converter considered for this discussion operates in PWM and has forced DCM at light loads (Asynchronous or Synchronous with reverse current detection). A PID Controller as shown in Figure 12 is used, which enables the use of low ESR MLC capacitors at the output. A load change from 400mA to 1mA causes a fast responding control loop to switch OFF the P_{SW} in the supply path for the future switching cycles. The energy stored in the inductor during 400mA condition would now be discharged onto the output capacitor raising the output voltage. Since the inductor ramp down slope is Vout/L, the associated overshoot can be computed as in Eq 3.9.

$$\Delta V = \frac{1}{2} \frac{\Delta I^2}{\left(\frac{V_{OUT}}{L}\right) C} \qquad [Eq.\ 3.9]$$

The overshoot during a high to low load transient is governed by the inductor and output voltage for a very fast loop. As the inductor current is prevented from reversing, this extra charge dumped on the output is discharged only by the 1mA load. As a result, the feedback voltage remains above reference for a long time and this causes the error voltage to decrease much below the ramp voltage till it saturates. To change the error voltage and bring the loop back into regulation, the output needs to drop below the reference as shown by the red plots in Figure 15. The response of the converter to any transients during this unsettled time would be slow and overdesigning for such a condition is not practical. To tackle this slow settling during high to low load transient some have proposed – (i) to let the inductor current reverse for a few cycles [29], (ii) non-linear gain amplifiers [27] etc.

To make sure the voltage dip during a step change is maintained within limit all the time using PWM control, this paper proposes clamping the error voltage at the min/max values of the ramp signal. Figure 15 shows the advantage of clamping the error voltage with a load transient applied before the loop settles (from a high to low load transient). The loop becomes open as the error voltage is clamped. As soon as V_{OUT} drops to the required value, the loop kicks in back and regulation in achieved. Almost 70mV reduction in the voltage dip is achieved (blue plots) by keeping the error voltage clamped at the bottom of the ramp.

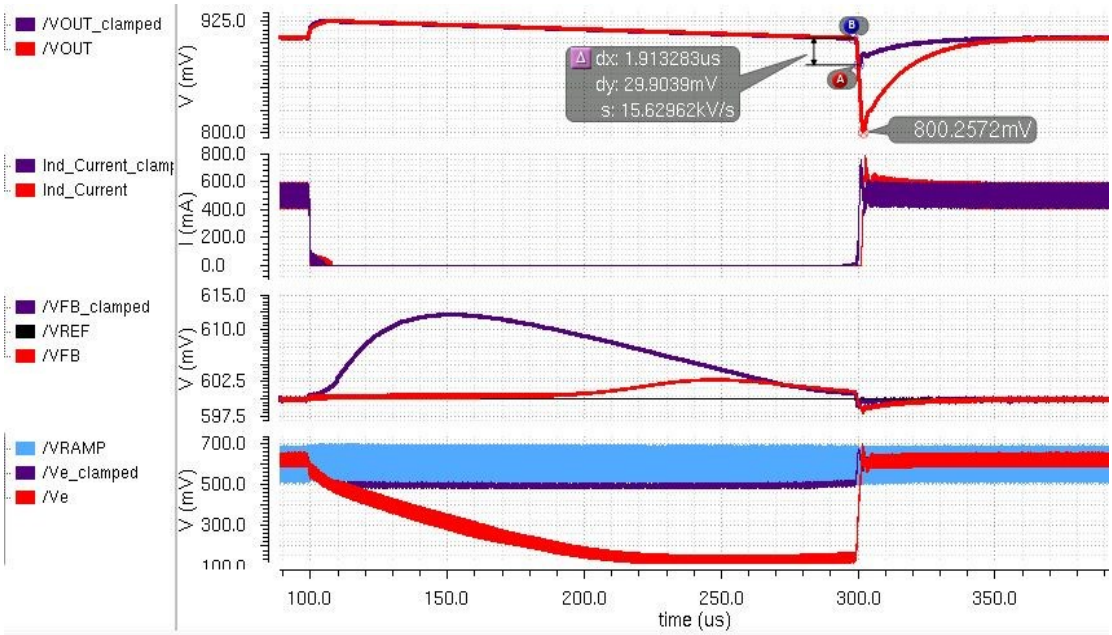


Figure 15. Load transient with (blue) and without (red) error voltage (Ve) clamp.

3.1.3 Output programmability (DVS)

Most of the present day DC-DC converters incorporate DVS (Dynamic Voltage Scaling) where-in the output of the converter is programmed on the run. This is generally done using programmability in the – (i) reference voltage (ii) resistive feedback ladder. We would need an amplifier with large input common mode range if we use reference programming. Using switches to tap a different node in the resistor ladder to change the feedback factor often result in unwanted transient behavior before settling. There can also be a stability concern as the overall loop gain depends on the feedback factor in certain architectures. This is often taken care of by changing the compensation values along with output programming.

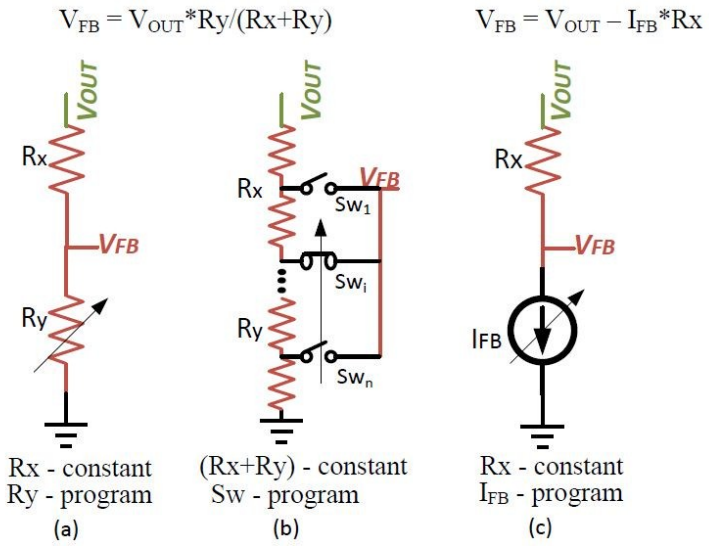


Figure 16. Existing (a,b) and proposed (c) feedback signal generator.

This work proposes an IR drop shift of the output to generate the required feedback signal as shown in Figure 16. Since there is no change in any resistance or capacitance values, the AC response remains the same with output programming. By adjusting I_{FB} smoothly (ramp up/down slower than loop bandwidth) we can ensure smooth output programmability.

$$V_{FB} = V_{OUT} - (R_S + R_{IN}) * I_{FB} \qquad [Eq.\ 3.10]$$

$$\frac{\partial V_{FB}}{\partial V_{OUT}} = 1 - (R_S + R_{IN}) * \frac{\partial I_{FB}}{\partial V_{OUT}} \sim 1$$

The current sources when implemented properly would have little dependence on V_{OUT}. When using type III compensation with a closed loop amplifier, the V_{FB} node is actually a virtual node and this prevents any V_{DS} mismatch across output programming. The implementation surely adds more capacitance at the V_{FB} node and amplifier design

should incorporate that. One disadvantage of this methodology would be larger area, as the current mirrors would need to be sized accordingly for the mismatch. Resistor implementations have better matching inherently.

The Figure 17 shows the PWM loop response to output programming trigger (black curve) of 0.9V to 1.2V. As can be seen, the output ramps up/down to the programmed value in 20us in a synchronous operation. However, forcing DCM operation slows down the ramp down rate depending on the load current (blue curve). A higher load current would discharge the output capacitor faster to the new lower value resulting in a lower settling time. This dependency can be avoided if we let the inductor current reverse in a synchronous converter.

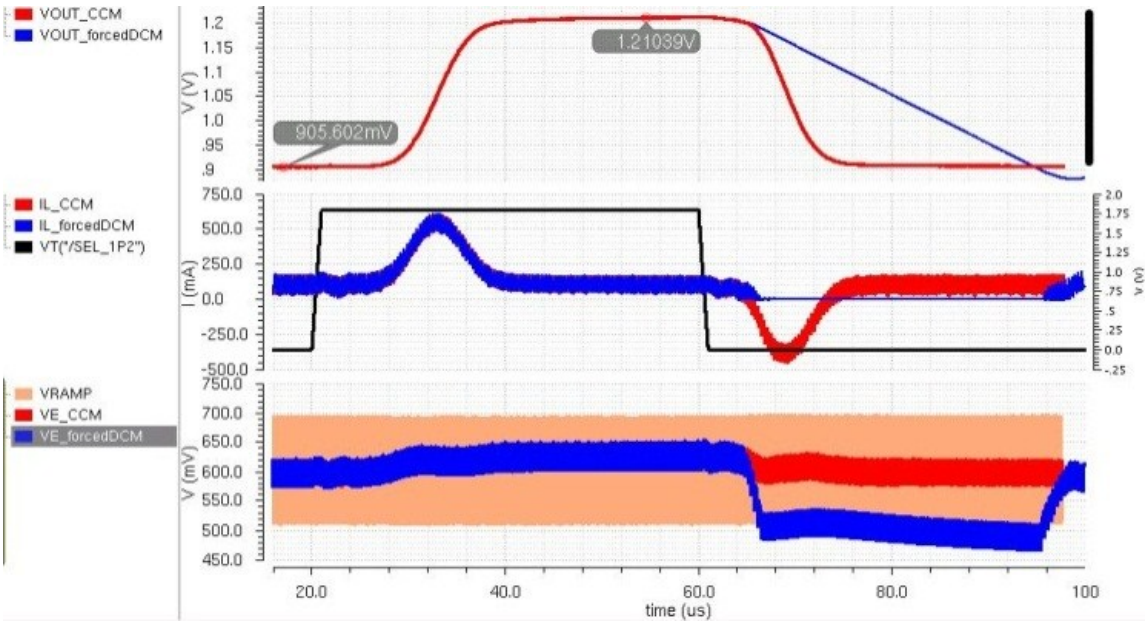


Figure 17. Output settling during proposed DVS in CCM (red) and DCM (blue).

3.1.3 Efficiency

The Efficiency of a buck converter can be computed as,

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}}$$

$$\eta = \frac{V_{OUT} I_{LOAD}}{V_{OUT} I_{LOAD} + \{P_{C_{DC}} + P_{C_{AC}} + P_{SW_{GD}} + P_{SW_{IV}} + P_{SW_{DT}} + P_{IQ}\}}$$

The equations derived in chapter II could be used to compute the efficiency of the converter operating in PWM mode. When the converter is operated in CCM, the power loss can be written as in Eq 3.11. Since the frequency of operation remains constant, the power loss has a quadratic relationship with the load current. At low load currents the high fixed losses result in very poor efficiency.

$$P_{LOSS_{CCM}} = I_{LOAD}^2 * R_{DC} + I_{LOAD} * \{(V_{IN} + 2V_D)t_{IV} + 2V_D t_{DT}\}F_{SW} + \frac{(V_{IN} - V_{OUT})^2 V_{OUT}^2}{12L^2 V_{IN}^2 F_{SW}^2} R_{AC} + C_{G_{eff}} V_{IN}^2 F_{SW} + V_{IN} I_{Q_{PWM}} [Eq.\ 3.11]$$

By forcing DCM operation in the given switching frequency at light loads, the inductor ripple reduces. The dead-time and IV overlap losses are also lower due to zero current switching (Eq 3.12). The constant losses are still the same since the F_{SW} and the I_Q remain the same. Thus just by forcing DCM operation in PWM gives better efficiency at

low-intermediate loads; but cannot improve efficiency below certain load as shown in Figure 18.

$$P_{COND\,DCM} = I_{LOAD}^{1.5} * \frac{4}{3}\sqrt{\frac{(V_{IN} - V_{OUT})V_{OUT}}{2LF_{SW}V_{IN}}}R_{DC}$$

$$+ I_{LOAD}^{0.5}\{(V_{IN}+2V_D)t_{IV} + V_D t_{DT}\}\sqrt{\frac{V_{OUT}(V_{IN} - V_{OUT})F_{SW}}{2LV_{IN}}}$$

$$+ C_{G_{eff}}V_{IN}^2 F_{SW} + V_{IN}I_{Q\,PWM} \qquad [Eq.\ 3.12]$$

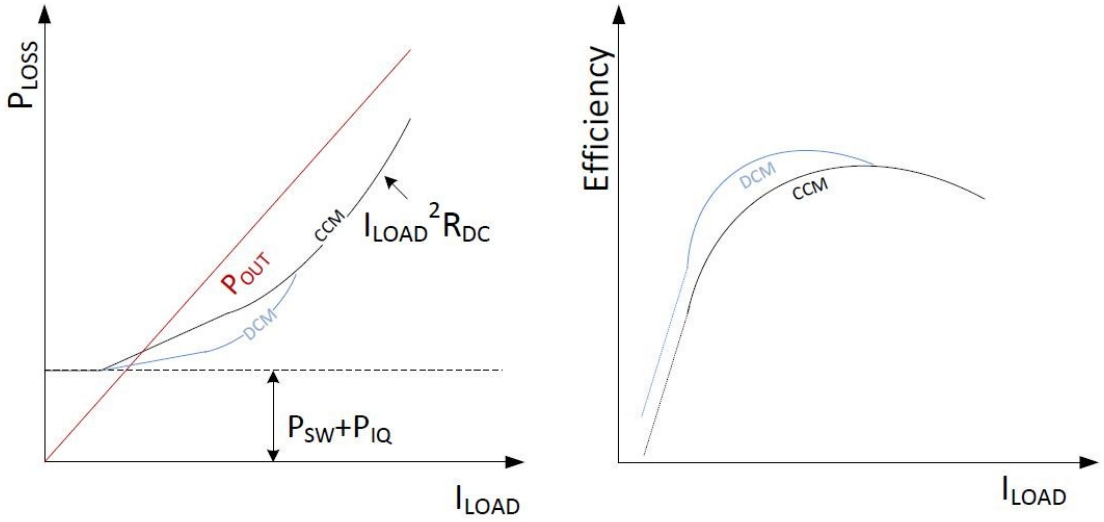


Figure 18. Efficiency as a function of load in CCM and forced DCM at given F_{SW}.

3.2 PFM control

A basic PFM controller checks for the output going lower than a pre-determined reference to turn ON the P_{SW} and charge the output; it then turns it OFF once the output has crossed a higher threshold. As the rate of discharge of the output capacitor is depended on the load current, the switching frequency varies with load and hence the name "Pulse-Frequency Modulation". The comparator delay also plays a major role in determining the Ripple voltage and frequency of operation in this kind of a control. The inductor current built up during the ON phase, discharge to the output even after the switches are turned OFF, increasing the output ripple. This necessitates a very fast comparator in-order to achieve control over the voltage ripple [30].

This thesis uses a Constant-On time (whenever output drops below a set reference) to charge the output back to the required value and thus makes the frequency of operation a linear function of the load and independent of the comparator delay [31]. Figure 19 shows the working principle.

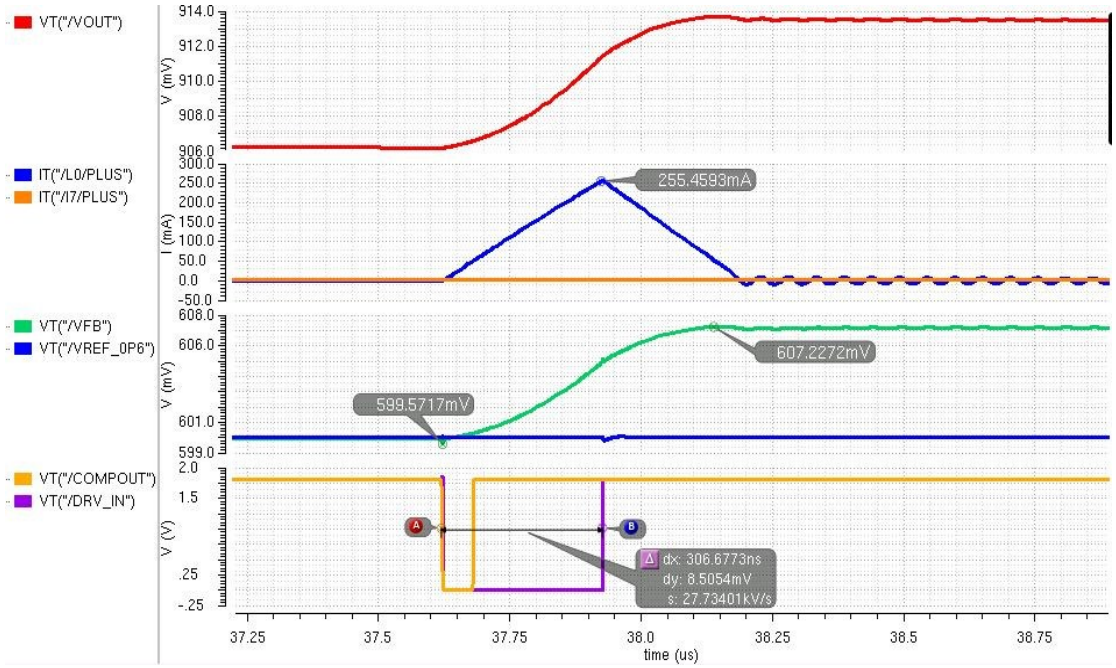


Figure 19. Constant On-Time PFM control waveforms at light loads.

Reference voltage (VREF_0P6) and feedback signal (VFB) are the inputs to the comparator. The PFM comparator output (COMPOUT) goes low when the feedback voltage drops below the reference voltage, P_{SW} is turned ON for a predetermined amount of time (T_{ON}) and the inductor current ramps up. The difference between the inductor current (L0/PLUS) and the load current (I7/PLUS) flows through the output capacitor and increases the output (V_{OUT}) and the feedback signal. The maximum output voltage ripple occurs at the minimum load current condition when all of the charge from the supply is dumped on the output capacitor during T_{ON} to raise the output voltage.

$$\Delta V_{OUT,max} = \frac{\Delta Q}{C} = \frac{T_{ON}^2 (V_{IN} - V_{OUT}) V_{IN}}{2 V_{OUT} L C} \qquad [Eq.\ 3.13]$$

As the load current requirement increases, a portion of this charge is supplied to the load and the output voltage ripple reduces. Above a certain load, the charge supplied and thus the voltage rise becomes insufficient for the comparator to resolve as shown in Figure 20.

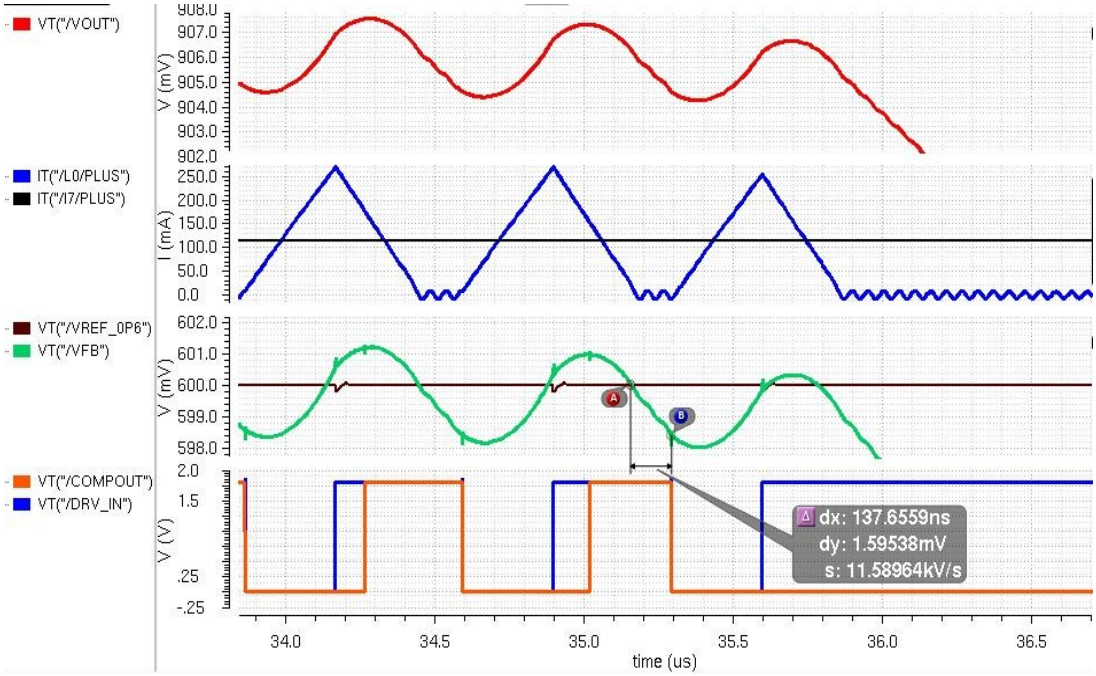


Figure 20. Constant On-Time PFM control waveform at maximum functional load.

At higher load currents, a small comparator delay results in a substantial dip in the output voltage before the inductor current can ramp up. Figure 20 shows a 2mV dip for 137ns delay in the comparator. The charge supplied during T_{ON} should be able to compensate for this. If not, the On-time generator would not receive a falling edge at the comparator output and the control mechanism would fail. Additional control would have to be used to detect this and modify the control. Few works suggest an (i) adaptable ON-

time [32] (ii) more constant On-time pulses [18] etc. Building a fixed frequency constant on time control with frequency compensation [33-35] seems to be a developing research topic.

The maximum load a given On-time can support is a function of the comparator delay and the charge dumped into the output capacitor during this ON-time. Ignoring ESR of the output capacitor, the condition to be satisfied can be represented as in Eq 3.14. In reality the voltage could rise even after T_{ON} , as long as $I_L > I_{LOAD}$, but that is assumed to be the margin to compensate for comparator offset and delay.

$$\Delta V = \left\{\frac{1}{2} I_{L,PK} T_{ON} - I_{LOAD}\left(T_{ON} + T_{dcomp}\right)\right\} * C > 0 \qquad [Eq.\ 3.14]$$

$$\frac{(V_{IN} - V_{OUT})}{2L} T_{ON}^2 - I_{LOAD}\left(T_{ON} + T_{dcomp}\right) > 0$$

$$I_{LOAD\,maxPFM} = \frac{(V_{IN} - V_{OUT})}{2L\left(T_{ON} + T_{dcomp}\right)} T_{ON}^2 \qquad [Eq. 3.15]$$

As shown by Eq 3.13 and Eq 3.15, the voltage ripple and the max load support of this scheme is dependent on (V_{IN}-V_{OUT}), T_{ON} and L. To keep the maximum load support/voltage ripple of the scheme a constant, we would need the ON-time to track the changes in supply and output voltage settings [36]. This work proposes a circuit implementation which tracks both supply and output as shown conceptually in Figure 21.

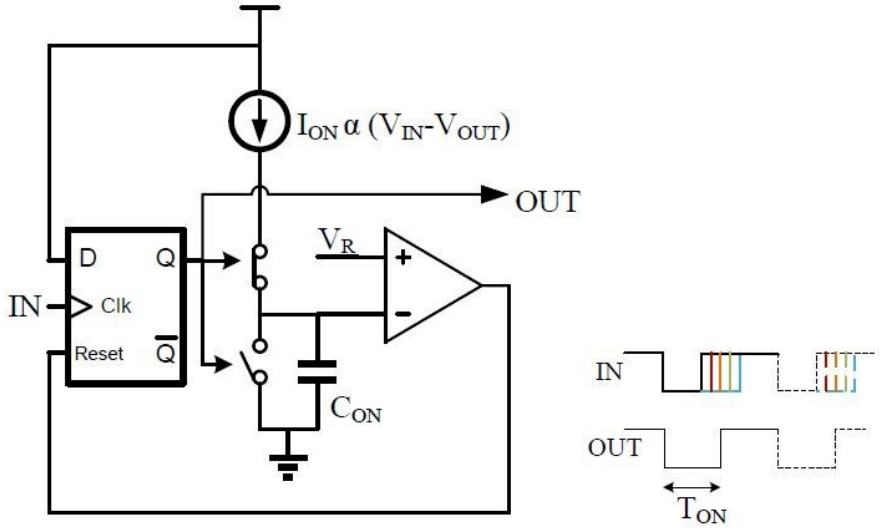


Figure 21. On-Time generation with V_{IN}/V_{OUT} tracking.

A Current proportional to (V_{IN}-V_{OUT}) is pumped onto a capacitor to create a voltage ramp when the PFM comparator outputs a LOW. This is compared with a reference (V_R) to determine T_{ON} as in Eq. 3.16. Exact cancellation of ripple and load support variation is still not achieved.

$$\frac{I_{ON}T_{ON}}{C_{ON}} = V_R \quad \rightarrow \quad T_{ON} = \frac{V_R R_{PROG} C_{ON}}{V_{IN} - V_{OUT}} \qquad [Eq.\ 3.16]$$

3.3 Dual mode

The constant frequency PWM is most widely used control strategy for the DC-DC switching converter. The switching frequency of these converters are kept high to tolerate smaller filter components (L & C) with acceptable ripple and also to support a high enough loop bandwidth for given transient regulation ($F_{BW} < F_{SW}/5$). At light loads (low output power) this mode of control has poor efficiency in a synchronous converter owing to the dominant switching losses and reversal of the inductor current and associated discharge of the output capacitor to ground. The methods adopted to reduce the switching losses (CV^2F_{SW}) include – (i) programming the driver size [37,38], (ii) altering the gate drive voltage [39,40], (iii) reducing the switching frequency [41], (iv) optimizing the dead time [42] or a combination of all [43] in accordance with the sensed loading condition. To prevent the unnecessary discharge of output capacitor to ground in a synchronous converter, a Zero current detector (ZCD) block is often used to switch off the N_{SW} when inductor current drops to zero; thereby forcing a DCM operation [44, 45]. Even with the above techniques implemented, the efficiency at very light loads is limited by the quiescent current used by the control blocks. To improve the efficiency in this regime, the current consuming blocks in the control circuitry have to be powered down. To improve the battery life of present day hand held electronic devices, it is necessary to reduce the losses within the power converters. As many of these devices are in the standby/sleep mode during most of the time, improvement of efficiency at these light loads is also very important.

A Dual mode Buck Converter which operates in constant frequency PWM mode at high loads (providing low ripple and good regulation) and a variable frequency Constant On-Time PFM mode at light loads (tolerating higher ripple) is the solution proposed. The efficiency improvement obtained by this technique is represented in Figure 22. The main challenge addressed in this thesis is the transient regulation during a sudden load step when the converter has to wake up from a low quiescent current mode where most blocks are powered down.

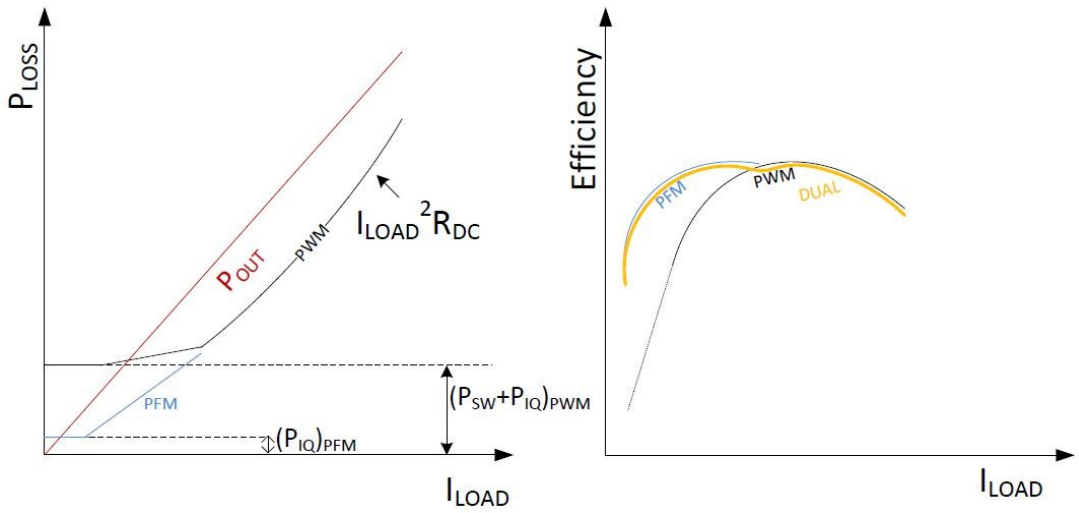


Figure 22. Efficiency improvement across load using a dual mode converter.

CHAPTER IV

MODE SWITCHING LOGIC

Since the use of dual mode has existed for long, there have been techniques used to switch between the modes to optimize efficiency curve. But the ones that have very good efficiency at ultra-light loads suffer during a large load transient and the ones that meet stringent over/undershoot specifications often burn more power resulting in reduced efficiency at very light loads. As explained earlier, this mode switching should be dependent on the load current.

4.1 Existing solutions

For a transition from PWM to PFM, most of the existing solutions use the zero current detector output [46, 47]. As long as the PWM loop is stable at light loads and can keep the transient overshoot (during high to low load transient) within limits, this is a fine strategy. This technique however cannot initiate a mode transition if it is required at a load higher than the DCM value. If the choice of Inductor and the DCM boundary is made so as to keep the frequency constant and ripple small at those loads, this strategy would hold good. Few others [18, 48-50] use a current sensor to detect a low load condition. This current sensor can also be reused for over current protection. The accuracy and power consumption of such a sensor is a concern especially at very high switching frequencies.

The transition from PFM to PWM has been the bottleneck. [46, 47] uses an additional comparator to detect a voltage dip to switch to PWM. If the PWM blocks were powered down, this scheme assumes that the PFM comparators are fast enough to regulate the output at higher load currents as well, implying more quiescent current. [18] provide a burst of Constant On-time pulses once the inductor current dies down to zero and switches to PWM based on the number of pulses required or on an additional lower reference comparator output. In [48] a loading potential detector is used to sense the current and switch between the modes. There are other current sensors reported to sense the inductor/switch current as an indicator of the load current [50-53]. These however can detect a load change only after the loop has corrected for it. Since the detection is slower, the control used at light loads should be able to work even at higher loads to maintain regulation. The quiescent current of this detector affects the light load efficiency. An Iq of 4uA is reported in [54], but it requires external pin to select the mode.

4.2 Proposed strategy

Figure 23 shows the architecture of the proposed dual mode buck converter. The feedback and reference are connected to both the Error Amplifier (through a switch) and the PFM comparator. During PWM operation, the V_{FB} node acts like a virtual ground; this prevents the comparator from toggling due to the switching ripple and other high frequency components in the output. During PFM operation, the error amplifier is

disconnected and V_{FB} tracks V_{OUT} with a DC level shift. The outputs from the PWM and PFM blocks are muxed based on 'SEL_PWM' from the 'Mode Sel Logic' block; and supplied to the driver for switching the power stage. During the PFM mode, the PWM blocks are powered down using the 'PD_PWM' signal.

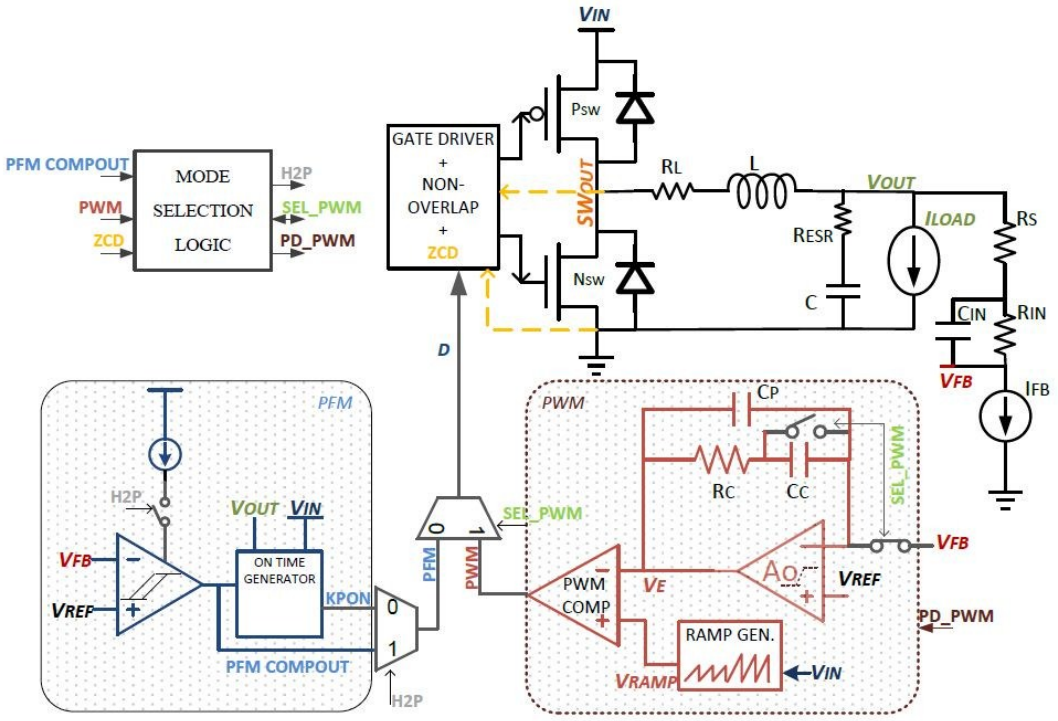


Figure 23. Proposed dual mode buck converter.

Continuous assertion of the ZCD output is checked for a few cycles (16 cycles) to ensure a light load condition and to transition from PWM to PFM. This is similar to earlier works. To transition from PFM to PWM, the technique proposed in this paper uses the zero current detectors and the inherent limited load support feature of the constant on-time scheme. By avoiding a separate current sensing block/comparator and

by powering down the PWM blocks, the quiescent current at light loads are kept to a minimum improving the efficiency further. The blocks operational during PFM are (i) PFM Comparator (ii) Tracking On-time generator (iii) Few bias generators and (iv) Zero current comparator. The Zero current detector is switched ON during the start of N_{SW} power switch ON time and turned OFF once the detection is done. Since this ON time is very short in comparison with the switching frequency at light loads, the average current consumption of this block becomes negligible.

As the load current increases above the limit, the On-time provided would be insufficient to bring the output back into regulation and the output voltage would drop indefinitely. Instead of using another comparator to detect this voltage drop (which would add to the power consumption and incur additional delay), the 'Low to High' edge at zero current detector output is used to check if the primary PFM comparator still outputs a LOW (indicating output lower than required). Ideally the fastest detection point is when inductor current has reduced below the load current (after which output cannot increase); nonetheless, the present approach works fine considering the delay in the comparators. To bring the output back into regulation as soon as possible without further drop, the current in the PFM comparator is increased (to reduce its delay) and its output directly fed to the driver using the H2P signal as shown in Figure 23. Meanwhile, the PWM blocks are powered up.

Once the PWM blocks 'UP' signal is received (after a programmed number of PWM clock pulses), the control shifts to PWM soon after the next PFM comparator HIGH (output above the required value). SEL_PWM signal goes HIGH and it connects

the V_{FB} node to the error amplifier and C_C into the feedback path. During power up, the error amplifier is connected in a unity feedback configuration forcing V_E to be equal to V_{REF} [46]. The positioning of the Ramp pedestal value is done in such a way that this error value is close to the required duty cycle (or at the mid value of the ramp). These small but effective modifications help reduce the voltage dip/overshoot during the mode transitions.

Since the transitions back and forth are based on different control signals, there should be some hysteresis built into this mode transition as shown in Figure 24 such that the converter does not keep switching between the mode at any constant load.

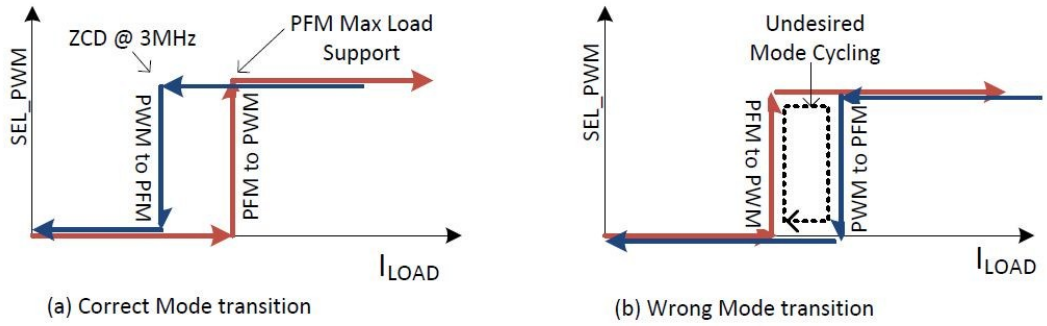


Figure 24. Mode transition signal (SEL_PWM) hysteresis during load change.

CHAPTER V

DESIGN PROCEDURE

To validate the proposed improvements a buck converter was designed to meet the specifications shown in Table 1. Since only 1.8V devices were readily available for tapeout, the supply voltage was kept to a max of 2V. The lower extreme for supply was chosen to be 1.4V to provide enough range to show the improvement in supply rejection. The output was made programmable between 0.9V and 1.2V to test the new feedback architecture and its benefits.

The output filter values were restricted at 1uH and 10uF to lower the area. Multi-Layered Ceramic Capacitance was planned to be used because of the cost/area reduction and the very low ESR. The required switching frequency was determined based on the given LC values and transient specifications unlike the regular method of determining LC values from the given switching frequency. The transient voltage dip/overshoot durng a load transient was set to be no more than 50mV. The low output filter capacitance and the tight transient spec neccesitates very high bandwiths for the loop and hence a higher switching frequency. Another challenge is the high efficiency across a load range from 1mA to 500mA. The converter was supposed to transition between the modes automatically with a very low quiscent current.

Table 1. Specifications for the buck converter design.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Voltage	V_{IN}		1.4		2	V
Output Voltage	V_{OUT}			0.9/1.2		V
Output Ripple Voltage (peak to peak)	V_{RIPPLE}	MAX. in standby TYP in PWM.		2	15	mV
Quiescent Current	Iq	V_{IN}=1.8V,I_{OUT}= 0mA (PFM mode)		20		uA
Load Regulation		I_{OUT}=10mA to 400mA at V_{IN}=1.8V	-0.2		0.2	%
Line Regulation		V_{IN}=1.4V to 2.0V at I_{OUT}=200mA	-0.2		0.2	%
Transient Regulation		I_{OUT}=1mA to 400mA and back in 1us	-50		50	mV
Load current	I_{OUT}	PWM mode PFM mode			500 100	mA mA
Inductor ESR	L_{ESR}	L= 1µH			0.05	Ω
Capacitor ESR	C_{ESR}	C=10µF			0.015	Ω
Switching Frequency	f_S			3		MHz
Efficiency		V_{OUT}=1.2V V_{IN}=1.8V,IOUT=500mA V_{IN}=1.8V,I_{OUT}=200mA V_{IN}=1.8V,I_{OUT}=1mA (PFM)	 85 90 85			%
Startup Current					100	mA

5.1 Voltage ripple

For the given V_{IN}, V_{OUT}, L and C values, assuming negligible capacitor ESR, we could calculate the switching frequency required in PWM to keep the ripple under specification as shown in Eq 5.1. This is derived from Eq. 2.7 and 2.8. The required value comes around 650KHz. In PFM mode, the max value of T_{ON} at 1.8V/0.9V is determined by the voltage ripple specification as shown in Eq 5.2 to be 408ns. The On-time would track V_{IN} and V_{OUT} to keep the ripple constant.

$$F_{SW\_min} = \sqrt{\frac{(V_{IN} - V_{OUT})V_{OUT}}{8V_{IN}LC\Delta V_{pp}}} = \sqrt{\frac{(2 - 0.9)0.9}{8 * 2 * 1u * 10u * 0.015}} \qquad [Eq\ 5.1]$$

$$T_{ON,max} = \sqrt{\frac{2\Delta V_{pp}V_{OUT}LC}{(V_{IN} - V_{OUT})V_{IN}}} = \sqrt{\frac{2 * 0.015 * 0.9 * 1u * 10u}{(1.8 - 0.9)1.8}} \qquad [Eq.\ 5.2]$$

5.2 Quiescent current

Quiescent current is defined as the total current taken by the control circuitry at no output load (and hence, it ignores any Power switching). To have a very low quiescent current, we need to achieve regulation with minimum number of blocks. The PFM mode uses just a comparator and the On-time generator and helps in achieving this goal at low load currents. Other blocks in the converter that might need to be operational are the reference generators, current and voltage bias circuitry and ZCD. Since the ZCD is switched only during N_{SW} ON, the current consumption of this block is reduced to just

the bias values at no-load. Thus we could allocate current to various blocks as shown in Table 2. In this work, an external voltage reference is used and the extra current is used for the PFM control blocks to reduce the delay of the comparators.

Table 2. Current budgeting for Iq

Block	**Current**
Reference generator	5uA
Bias/FB Circuitry	2uA
PFM Comparator	4uA
On-Time Generator	6uA
ZCD standby	3uA
Total (Iq)	**20uA**

5.3 Accuracy and stability of PWM loop

As mentioned earlier, the accuracy of output depends on the accuracy of the reference and the loop gain of the converter. The inherent offsets in the control path are assumed to be trimmed by varying the reference. For 0.1% accuracy, we need a loop gain of over 60dB at low frequencies. The following section analyses the transfer function of the loop to achieve a stable control with this DC gain.

The buck converter transfer function from change in compensated error voltage, Ve to Vout in CCM is given by (Assuming negligeble R_{ESR}):

$$\frac{V_{OUT}(s)}{V_E(s)} = \left(\frac{V_{IN}}{V_{RAMP}}\right) * \frac{1}{1 + s\left(\frac{L}{R}\right) + s^2LC} \qquad [Eq.\ 5.3]$$

The Gain is limited to V_{IN}/V_{RAMP} and it has a double pole at $\frac{1}{2\pi\sqrt{LC}}$. . To improve the DC Gain and obtain good phase margin a lead-lag (Type III) compensator was used as shown in Figure 25.

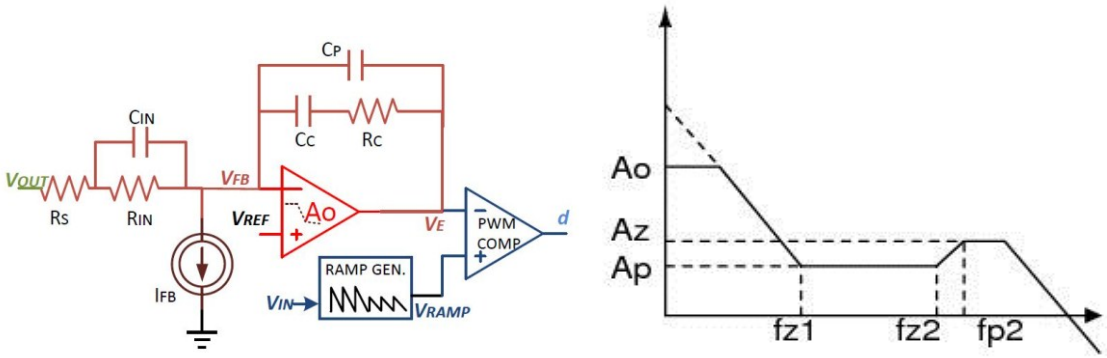


Figure 25. Type III compensation architecture and corresponding transfer function.

$$V_E(s) = Z_{FB}(s) * I_{FB}(s) + V_{REF}(s) * \left(1 + \frac{Z_{FB}(s)}{Z_{IN}(s)}\right) + V_{OUT}(s) * \frac{Z_{FB}(s)}{Z_{IN}(s)}$$

Where (ignoring C_P),

$$Z_{FB}(s) = \frac{(1 + sR_CC_C)}{sC_C} Z_{IN}(s) = (R_S + R_{IN}) * \frac{(1 + s(R_S||R_{IN})C_{IN})}{(1 + sR_{IN}C_{IN})}$$

Assuming I_{FB} to be open for AC and V_{REF} to be an AC short;

$$V_E(s) = V_{OUT}(s) * \frac{Z_{FB}(s)}{Z_{IN}(s)}$$

$$\frac{V_E(s)}{V_{OUT}(s)} = \frac{(1 + sR_C C_C) * (1 + sR_{IN} C_{IN})}{s(R_S + R_{IN})C_C * (1 + s(R_S||R_{IN})C_{IN})} \qquad [Eq.\ 5.4]$$

Ao is the open loop gain of the differential amplifier. The Plateau Gain, Ap is fixed at $R_C/(R_S+R_{IN})$.

$$f_{z1} = \frac{1}{2\pi R_C C_C}$$

$$f_{z2} = \frac{1}{2\pi R_{IN} C_{IN}}$$

$$f_{p2} = \frac{1}{2\pi (R_S||R_{IN}) C_{IN}}$$

The first pole zero pair is used to set the high DC/Low frequency gain. The second zero (fz2) is used to provide the phase improvement around the UGB, assuming the amplifier has higher openloop bandwidth. The phase improvement also depends on the positioning of the second pole (fp2). At higher frequencies , the gain would roll-of due to the limited bandwidth of the amplifier (UGB_{A_OL}) and hence we do not need a separate 'Cp' as shown in Figure 25.

Since the basic converter had a gain of 10, the openloop gain of the amplifier, **Ao>100** for the overall loop to have 60dB gain. From Eq 3.18, the required openloop UGB was calculated to be **320KHz** (inc. margin) to meet the given spec for load transient and to have some gain around the LC frequency (50KHz). This necessitates a switching frequency of **3MHz**. The second zero was placed just outside the UGB so that bandwidth variation due to the RC tolerances are controlled. This would limit the

maximum attainable phase margin to be less than 45degree. The same analysis was done with a buck ac model for DCM. At lighter loads, when the converter is in DCM, the double pole splits into two separate poles and one of them moves into lower frequency with decrease in load. The first zero was placed much before the LC frequency (10KHz) to regain all the phase dropped due to the integrator in CCM mode and also to provide some phase margin in DCM light load condition. PWM switch model was used to study the AC response of the power stage in both the modes. The R/C values obtained from the analysis are listed in Table 3. Figure 26 shows the overall loop response for CCM and DCM (1mA) condition. Since the characteristics are different and the response is slower in DCM than that predicted by the CCM bandwidth, the voltage dip/overshoot would be higher for a similar load step involving DCM load as shown in Figure 27.

Table 3. PWM loop compensation RC values

R_S	5KΩ	R_C	320KΩ
R_{IN}	75KΩ	C_C	50pF
C_{IN}	5pF	V_{IN}/V_{RAMP}	10 V/V
Ao	>200 V/V	UGB_{A_OL}	1MHz

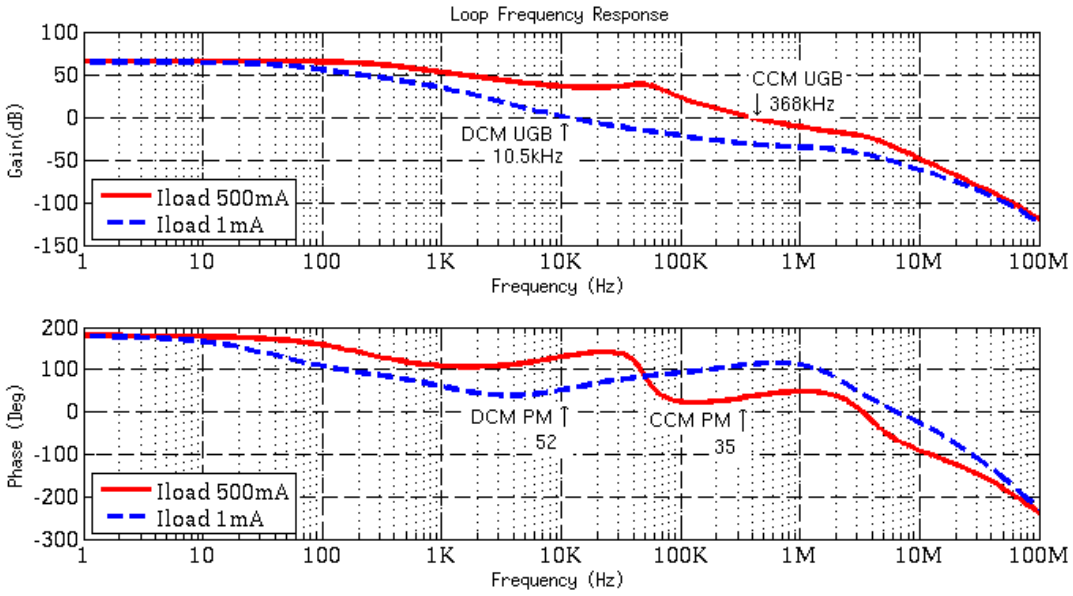


Figure 26. AC response of PWM loop.

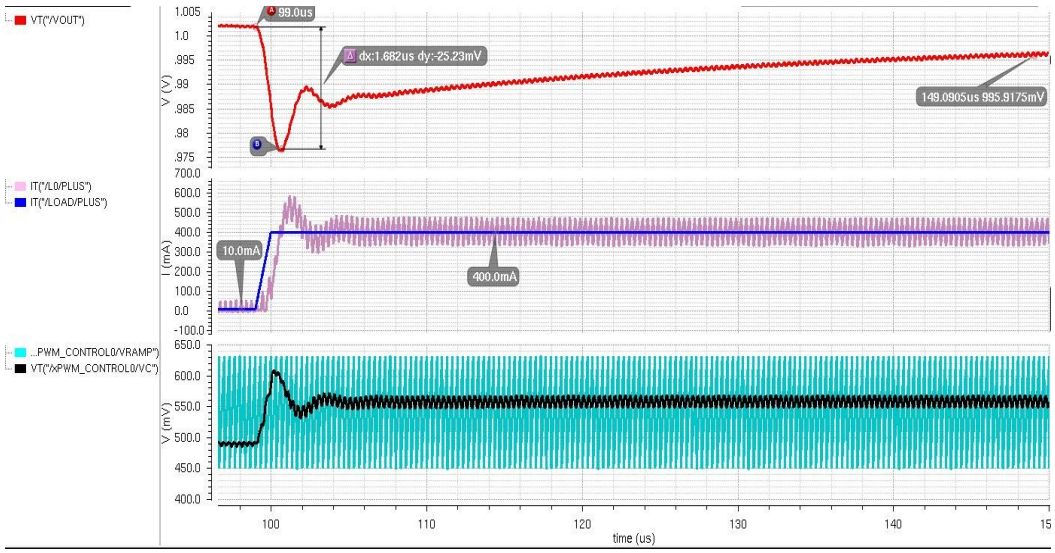


Figure 27. Transients for 1mA to 400mA in 1us. (i) RED – Vout (ii) Blue – Load Current (iii) Black - Control Signal, Cyan – Ramp Signal

5.4 Load support

Architecturally, the PWM loop can support any load; but the higher conduction losses and current handling restrictions of the metal routing and inductance limit the maximum load current where good performance is guaranteed. Depending on the switching frequency obtained, the max load above which the converter would operate in very low ripple constant frequency PWM mode (CCM) could be derived from the CCM-DCM boundary current equation (Eq 2.7). For 3MHz operation, this translates to PWM operation above 80mA.

To have enough hysteresis in the mode transition, the PFM load support should be maintained higher than 80mA. Using 100mA as the min. load support in PFM mode, and assuming $T_{dcomp} << T_{ON}$, the minimum On-time required can be calculated (from Eq 3.15) as shown in Eq 5.5. The value came out to be 220ns. For higher T_{dcomp}, we should increase $T_{ON,min}$ accordingly. From Eq 5.5 and 5.2, and from detailed simulations, a default T_{ON} value of **300ns** was used for 1.8V/0.9V.

$$T_{ON\ ,min} \sim \frac{2I_{LOAD_{PFM}}L}{(V_{IN} - V_{OUT})} \qquad [Eq.\ 5.5]$$

To support the maximum current of 500mA in PWM mode, the Power switch transistors and routing were sized according to EM and efficiency specifications.

5.5 Efficiency - power switch sizing

Power Switch sizing is one of the major steps involved in optimizing the efficiency of the converter. As mentioned earlier, the major contributor to loss at high load currents is the conduction loss across the resistive elements in the energy flow path. Hence the efficiency requirement at max load puts restriction on the minimum switch size. The only way to decrease the switch resistance is by making the switch bigger (larger W/L) which results in higher gate capacitance and thus reduced efficiency at low load currents. 85% efficiency at 500mA translates to a loss of approximately 75mW and hence a maximum resistance of 240mΩ (assuming 80% of this loss is due to conduction). This resistance includes the inductor ESR and all the board and die routing parasitics.

To optimize efficiency, we have to optimize switch size at an intermediate load current value to have equal switching and conduction losses. Here we have chosen the load current to be 200mA.

5.6 Feedback programming

The design incorporated two output voltage settings (0.9V and 1.2V). The Reference voltage was chosen to be 600mV as these references ICs were readily available in market. The sum of Rs and Rin as derived from the earlier section totaled to 75KΩ. For an output of 900mV,

$$\mathrm{I_{FB}} * (\mathrm{R_S} + \mathrm{R_{IN}}) = 0.9 - 0.6 = 0.3\mathrm{V} \rightarrow \quad \mathrm{I_{FB}} = \frac{0.3}{75K} = 4uA$$

To program the output to 1.2V, we would require an additional drop of 300mV across the resistor. This was done by adding one more branch of 4uA. The current sources were implemented using cascode current mirrors as shown in Figure 28. The slow ramp-up/down was achieved by ramping up/down the $NCAS_i$ voltage through a controlled current. This smooth output transition is achieved at the expense of silicon area in the form of additional NCAS generators and capacitors.

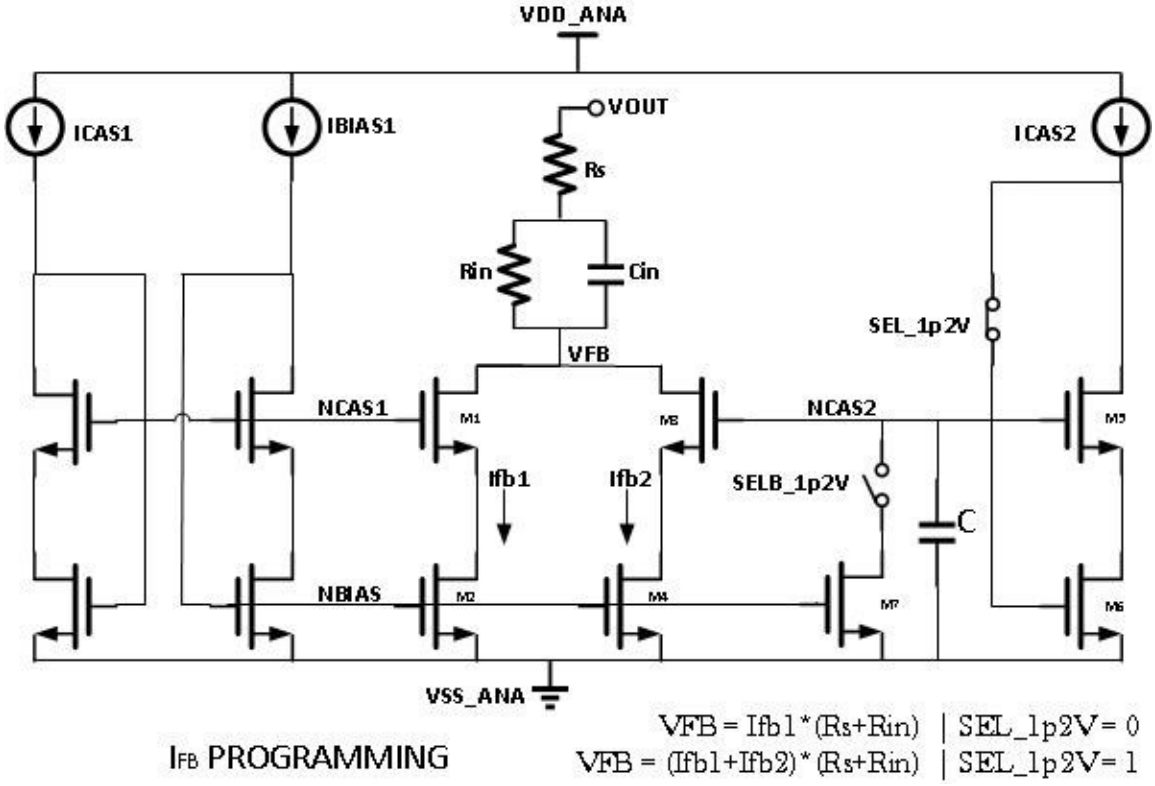


Figure 28. Feedback programming implementation.

5.7 Error amplifier implementation

Figure 29 shows a simple circuit implementation for the clamped Error Amplifier. It is a two stage amplifier. First stage contributes all of the gain. The error voltage has a maximum voltage of min. (V_{T2}, I_2*(Rout+Rped)) when V_{OUT} drops drastically below the set value; and is clamped at I_2*Rped when V_{OUT} overshoots. The CM node is also the pedestal for the supply dependent ramp generator to ensure that the error voltage doesn't go below the ramp signal at any circumstances.

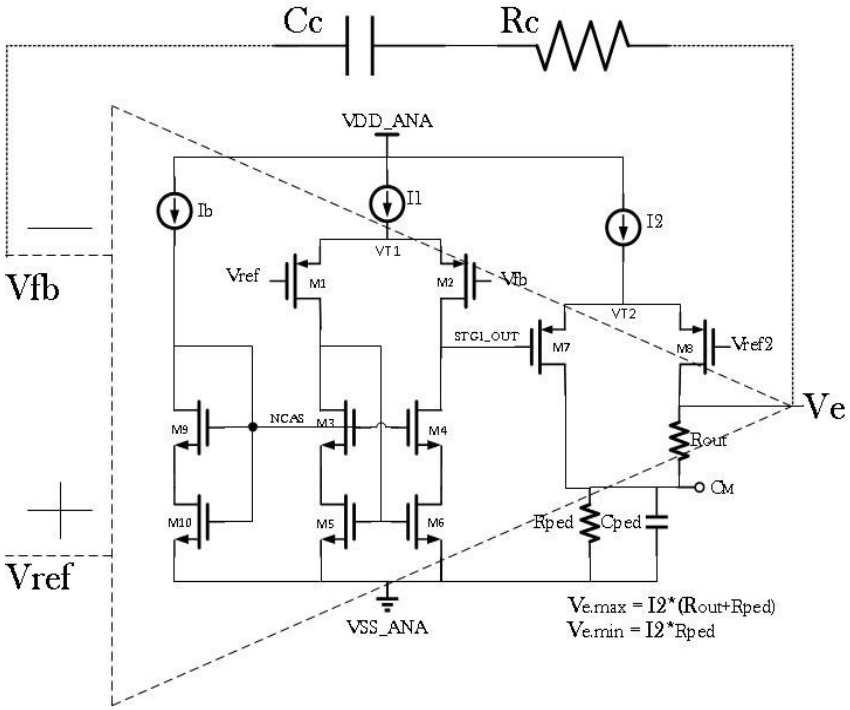


Figure 29. Proposed error amplifier schematic with compensation.

Overall Gain, $A_O = (gm_2/gds_2)*gm_8*Rout$. To ensure a constant voltage at CM even during transients, $I_2 >> (V_{FB}-V_E)/Rc$.

5.8 Supply dependent ramp generator

Figure 30 shows the ramp generator implementation. AMP1 generates a current 'I' proportional to the supply which is then used to determine the ramp peak voltage. The Ramp pedestal is fixed by the error amplifier at CM node. During the start of every cycle, C_{RAMP} gets charged through the supply dependent current 'yI' and V_{RAMP} rises. Once V_{RAMP} reaches V_{PEAK}, the capacitor is reset and V_{RAMP} drops to the V_{CM} value. By using a supply dependent current to charge the capacitor, switching frequency is maintained constant even with varying V_{IN} and V_{RAMP}.

$$\text{Fsw} = \frac{\text{y}}{\text{xCR}_{\text{PEAK}}} \qquad [Eq.5.6]$$

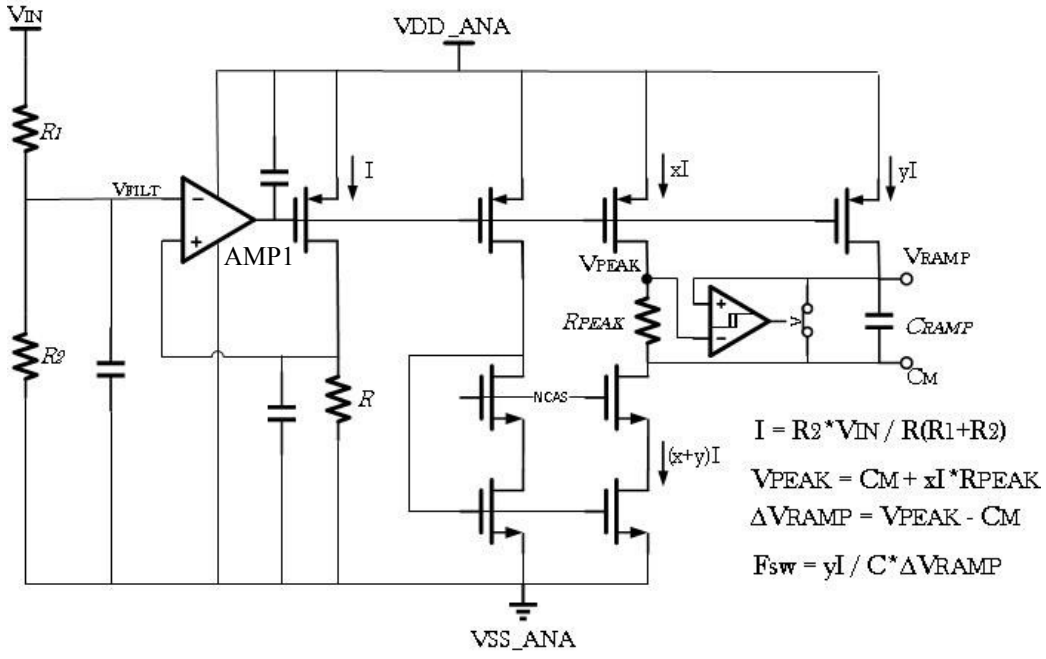


Figure 30. Supply dependent ramp voltage generator.

5.9 Comparators

A differential stage followed by a common source stage was used to compare signals as shown in Figure 31. A total of 40uA current was used for the fast PWM comparator, while the low power PFM comparator operated at 4uA. The delay programmability during transients was implemented by adding/removing MPX into the circuit using STANDBY_PFM signal as shown in Figure 31. The configuration shown is for the low power PFM mode. When faster comparison is required (as is the case during a load transition), the switches toggle and turn OFF MPX. Since MPY has to source all the current (Ib), node VB goes lower, pushing more current through MPT and MP3 reducing the delay.

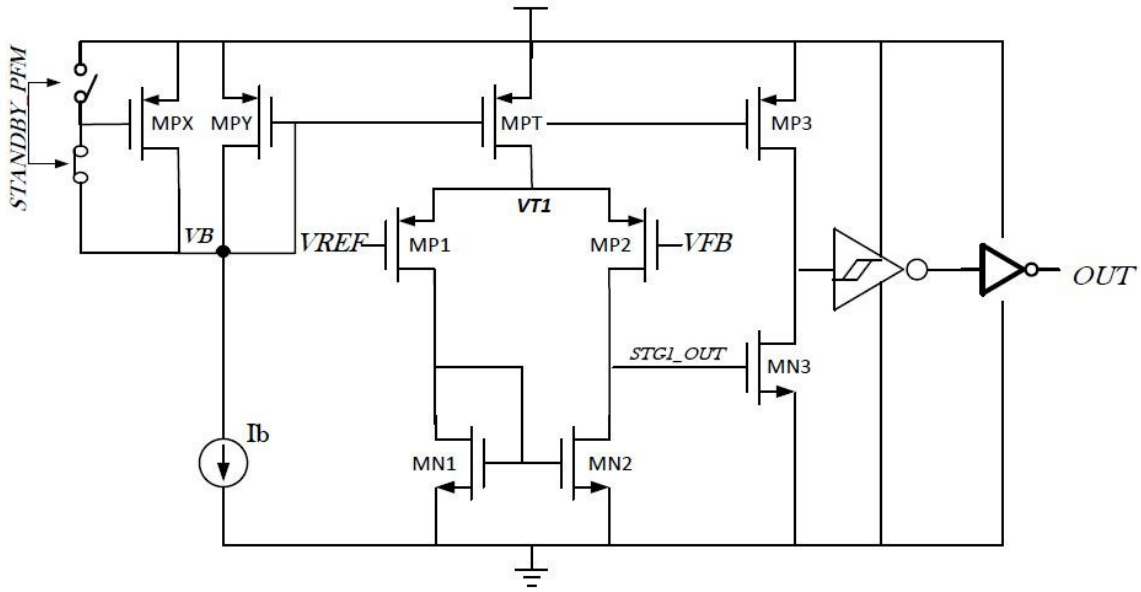


Figure 31. Comparator architecture.

5.10 On-time generator

The schematic implementation of the On-Time generator can be found in Figure 32. Transistor MP1 was sized to generate a voltage $V_G = V_{OUT} - Vtp$. Transistor MP2 was matched to MP1 but with higher current capacity (using more multipliers) depending on the default I_{ON} requirement. This ensures $V_S \sim V_{OUT}$. Thus we have a current, $I_{ON} = (V_{IN} - V_{OUT})/R_{PROG}$ flowing through MP2. When the PFM_COMPOUT signal goes low, this current is steered into the capacitor C_{ON}. When the Voltage V_{ON} rises till V_R, the comparator toggles and resets the Flip-Flop. The Comparator could be replaced by simple Common source stage or an inverter at the expense of On-time variation.

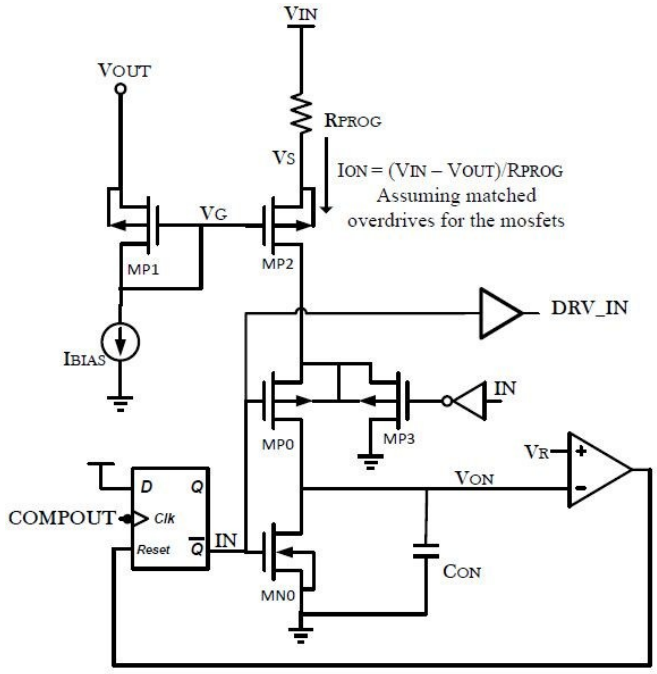


Figure 32. Tracking On-Time implementation.

5.11 Zero current detector

Zero Current Detector (ZCD) is used to switch OFF the N_{SW} when the inductor current reverses. This prevents unnecessary wastage of power and forces the converter into DCM.

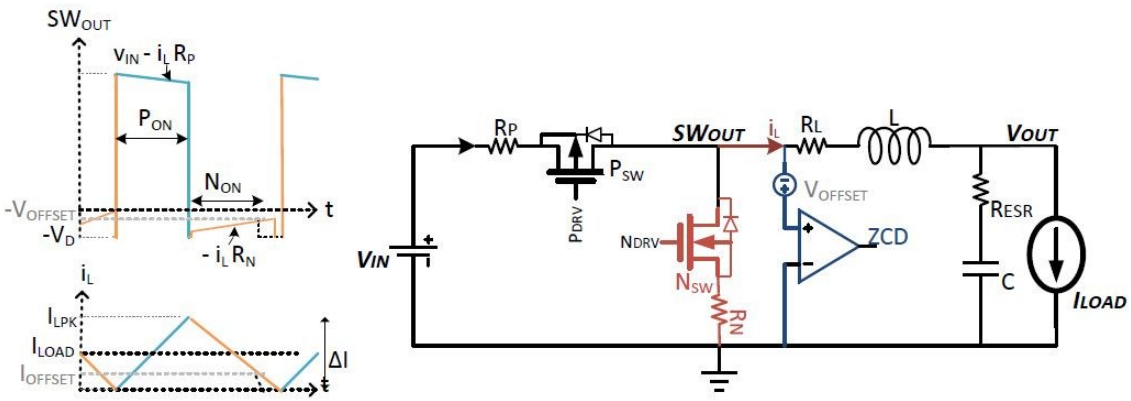


Figure 33. Zero current detector principle and waveform.

During the N_{SW} ON time, $V_{SWOUT} = -i_L * R_N + V_{SS}$, where R_N includes the N_{SW} ON resistance and the layout metal routing resistance and V_{SS} denotes the ground potential within the chip. Hence to detect a zero inductor current, we just need to look for V_{SWOUT} increasing above V_{SS}. Usually an intentional offset in put in the comparator as shown in Figure 33 so as to prevent the delay in comparator and control chain from causing a negative inductor current. The two inputs to the comparator are routed directly from the pads to have an accurate comparison.

Because of the common mode constraints (negative values of V_{SWOUT}), many works suggest DC shifting the signal and comparing [55]. In the present architecture, we use a common gate differential stage to sense and compare the signals. The comparator is initialized when P_{SW} is ON. 'Rinitial' generates an offset in the comparator and keeps the output low during initialization. To prevent the comparator first stage from seeing sudden transients in SWOUT, it is isolated till N_{SW} turns ON as shown in Figure 34.

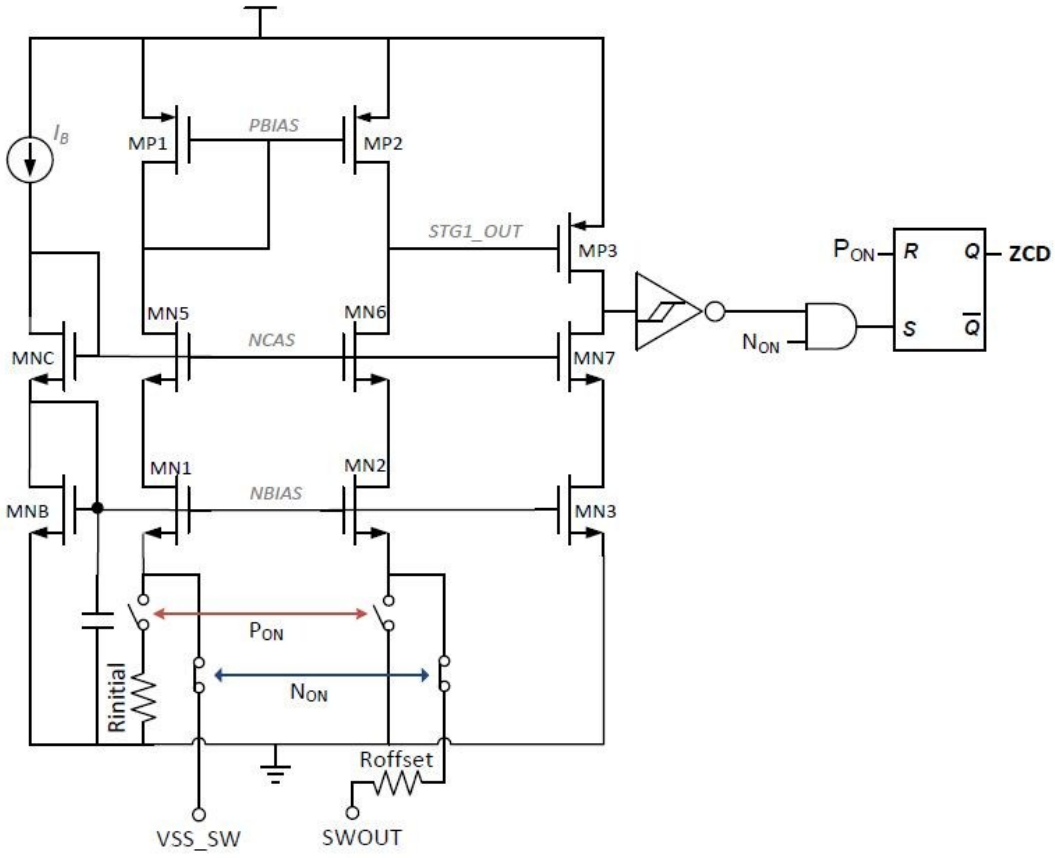


Figure 34. Zero current detector schematic

The intentional dc offset is provided using 'Roffset'. The equilibrium point is when,

$$V_{NBIAS} - VSS_{SW} = V_{NBIAS} - kI_B * R_{offset} - V_{SWOUT}$$

$$V_{SWOUT} - VSS_{SW} = -kI_B * R_{offset}$$

$$i_{L_{tripDC}} = kI_B * \frac{R_{offset}}{R_N} \qquad [Eq. 5.7]$$

By using NMOS switches as in N_{SW} to generate Roffset, we can maintain a fairly constant DC trip point across PVT. Since R_N also includes large metal routing resistance, exact tracking would be impossible. 'k' represents the ratio of W/L between MNB and MN1/MN2. Since the ramp down rate of inductor current depends on the output voltage, $I_{LtripDC}$ should be varied using Roffset with Output voltage programming.

The first stage output is fed to a common source second stage with current source load for additional gain. Its Output is fed to the Schmitt trigger to give better noise immunity. To prevent N_{SW} from turning ON till next P_{SW} ON, the output of the Schmitt trigger is latched and fed to NDRV generator. Once the decision is made, the first stage current is cut-off to save power, especially during the PFM mode of operation. The PON time is generally sufficient to wake up the comparator and be initialized to perform correct comparison.

5.12 Softstart

To prevent sudden inrush current during startup, the Gate of the P_{SW} is tri-stated and connected to a bias voltage. This high bias voltage limits the current in the power switch. By generating the bias voltage using a current source and identical diode connected PMOS transistor, the startup current could be controlled as shown in Figure 35. Once the output is charged to the required value, the SFST signal is deactivated using the PFM comparator output in the MODE_SEL_LOGIC block. This mechanism can charge the output to the required value smoothly as long as the load is lower than the softstart current ($K*I_B$).

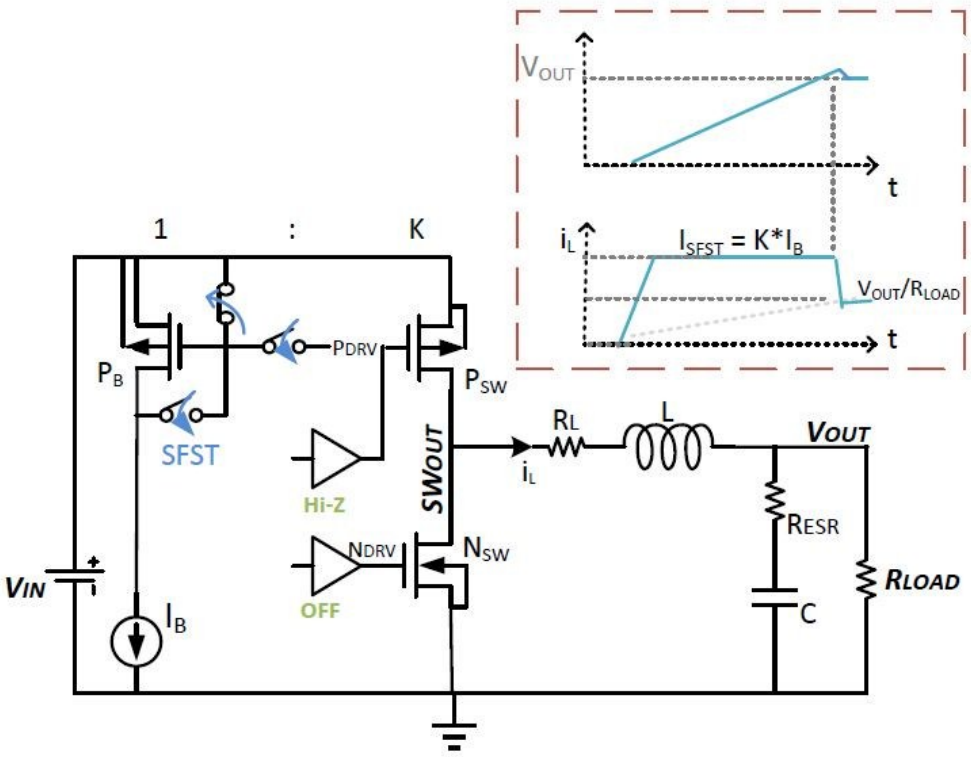


Figure 35. Soft-Start implementation.

CHAPTER VI

MEASUREMENT RESULTS

A buck converter was implemented using the above control mechanism in IBM180nm process. It was packaged in a 36 pin QFN as shown in Figure 36. Multiple bondpads were used for the switching supply and ground connections to reduce the parasitic inductance and resistance so as to minimize the supply/ground bounce during switching. The switching and quite part of the chip were placed and routed far apart to reduce coupling. Figure 37 show the major connection required on the board.

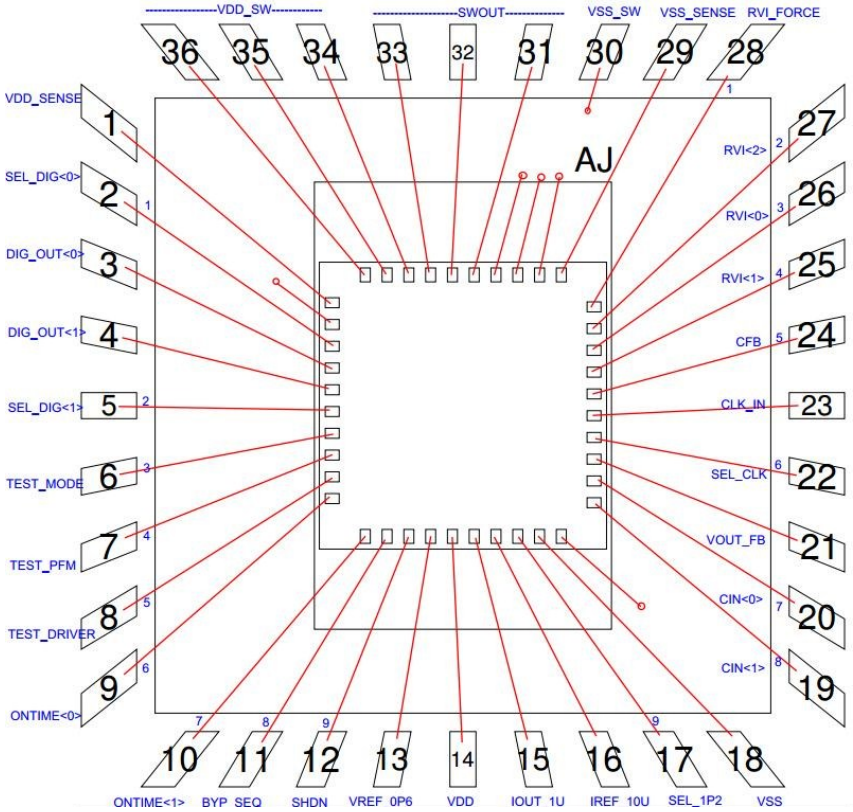


Figure 36. Bonding diagram for 36 pin QFN**.**

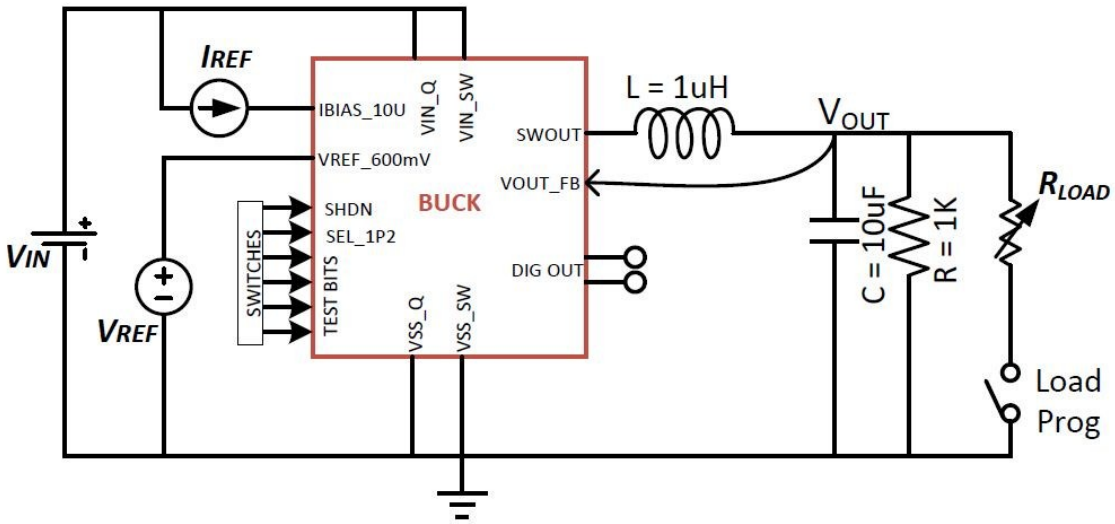


Figure 37. Required test setup to verify the functionality.

External components were purchased and a PCB was designed and manufactured for testing the chip. There were options provided in the PCB for debug through test switches. Figure 38 shows the design of the PCB following the guidelines in [56-58]. Two LDOs were soldered on-board to provide the switching and quite supply for the buck converter incase the DC voltage source was very noisy. Options exist to bypass the LDO and provide supply directly from the DC source. The bias current and reference voltage was provided using external IC on board to lower the offset. A series of switches powered by the quite supply was used to program the digital test options on the chip. Load transient test were conducted by connecting a programmable resistance at the output and switching it using external trigger. There was also an option to test the load transients using a current mirror load.

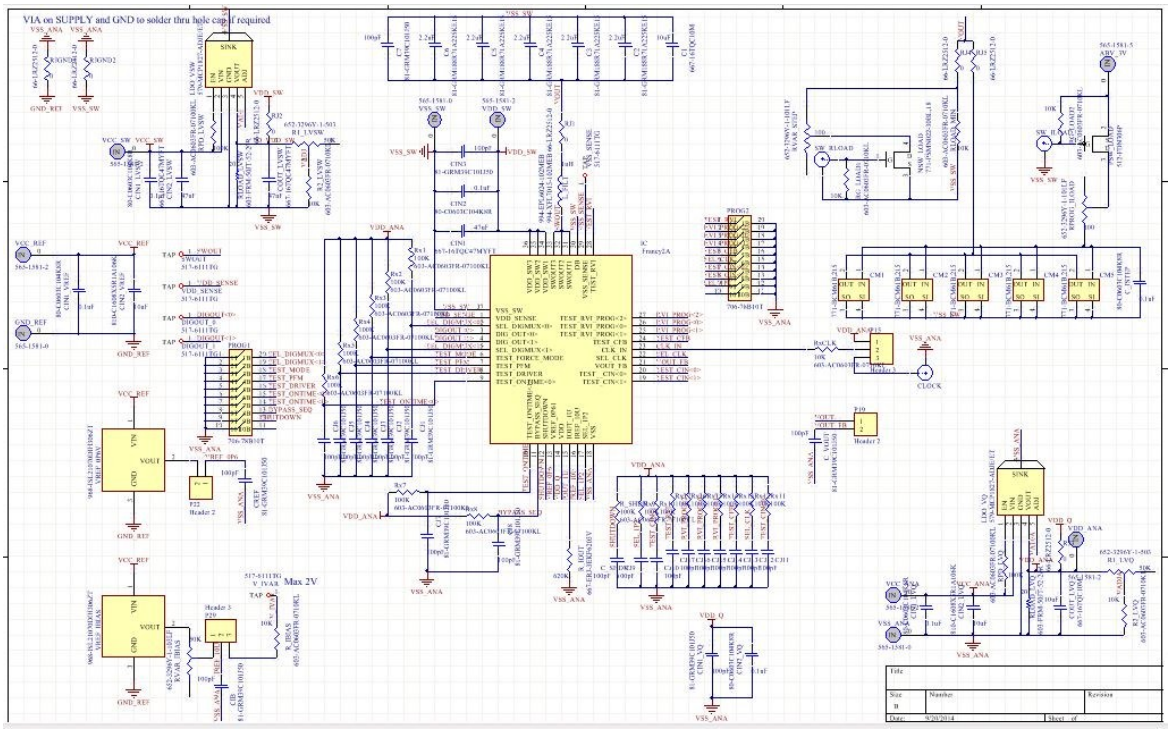
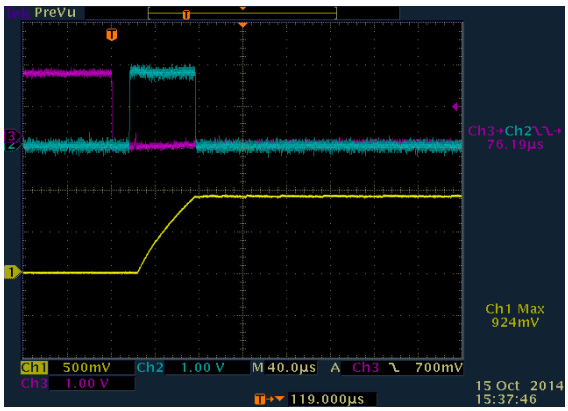
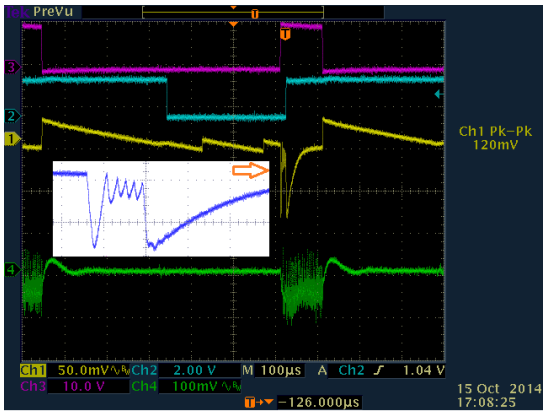


Figure 38. Complete PCB schematic.

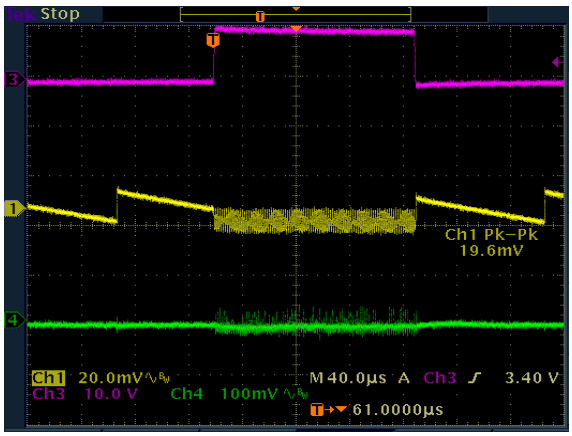
Figure 39 shows the test results for the first (Jun 2014) tape-out. Problems in regulation were seen at higher load currents (above 400mA) and efficiency was much lower. This was debugged to be because of the huge parasitic resistance in the layout due to fewer contacts. By taking the reading from the sense pins and correcting for the package and PCB parasitics, the results could be improved further. The chip however adheres to the trend in the efficiency curve as predicted in the thesis. The efficiency is improved during light load condition.



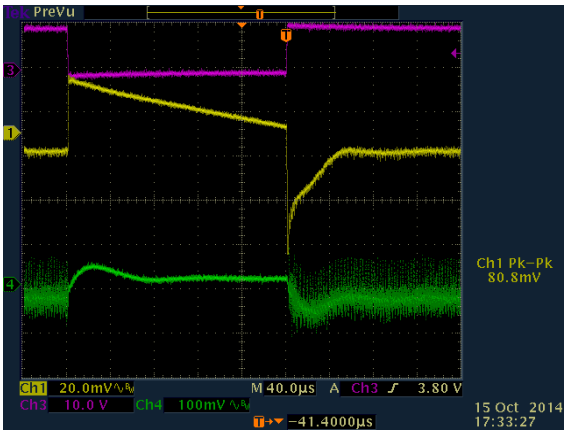
(a) Softstart Powerup



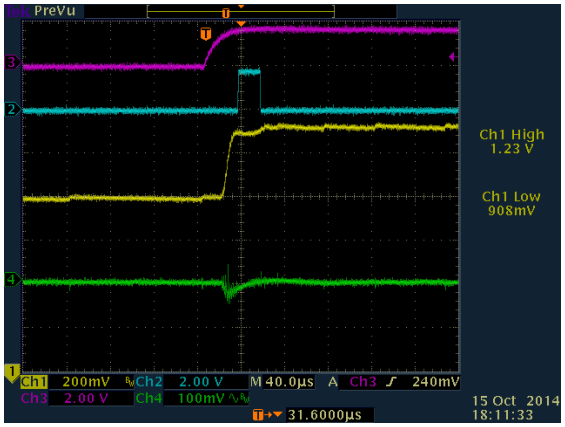
(b) Load Transient 1mA to 400mA – Auto



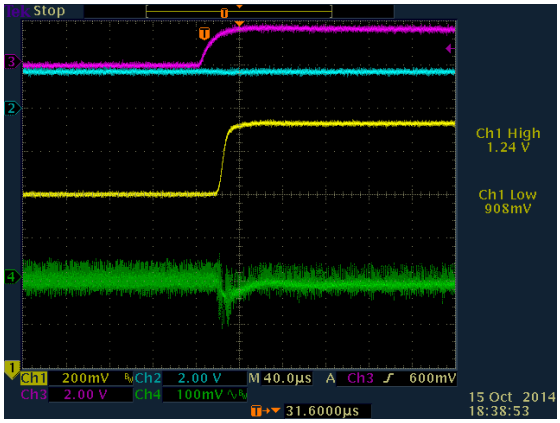
(c) 1mA to 50mA – PFM



(d) 1mA to 400mA – PWM Forced

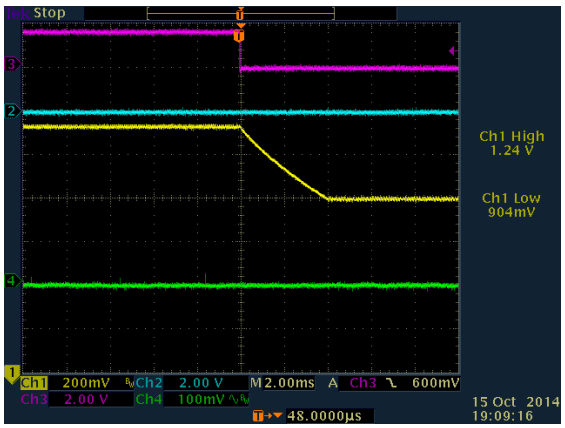


(e) 1mA – 0.9V to 1.2V programming

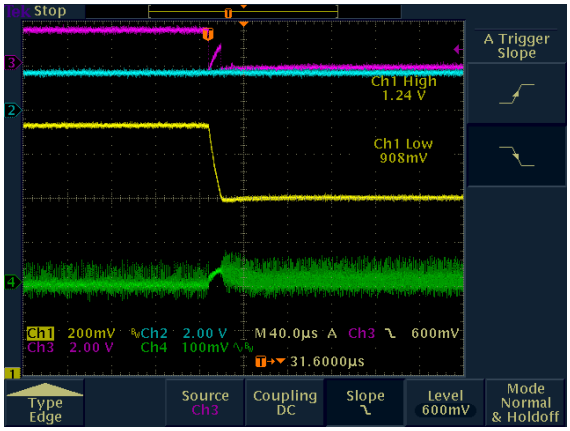


(f) 200mA – 0.9V to 1.2V programming

Figure 39. Measurement plots from the oscilloscope.



(g) 1mA – 1.2V to 0.9V programming



(h) 200mA – 1.2V to 0.9V programming

Figure 39. Continued

In Figure 39(a) the pink curve denotes the SHDN signal and the blue curve represents the converter in soft-start mode. The output can be seen ramping up to the desired value in the yellow curve. Figure 39(b) shows the load transient curve obtained by switching the resistive load. The pink curve denotes the transient trigger, the blue represents the converter's mode of operation (SEL_PWM) and the green curve represents the supply voltage inside the chip. The output (yellow) drops during a low to high load transient and the fast control mechanism switch the current in the PFM comparator and regulate the output till the PWM blocks kick in (as shown in the magnified box) and the converter moves into PWM. During a high to low load transient, the output overshoots and once it is in regulation, the converter switches from PWM to the PFM mode. Figure 39(c) and (d) shows the transient response with the mode forced externally.

Figure 39 (e) – (h) shows the Dynamic voltage scaling at different loads. At light loads, an increase in output was seen to cause an intermediate mode change; but the output ramp-up was smooth. The ramp-down of output voltage was depended on the load current as no additional current sink was incorporated. At 1mA (g) the output programming from 1.2V to 0.9V took 4ms; while the output settled in less than 20us at 200mA load.

Table 2 summarizes the test results. As can be seen, the transient and efficiency value are out of specifications. Modifications done in the schematic would be reflected in the Dec tape-out. The switch layout was optimized for improving the efficiency at high loads and proper sequencing was done to take care of the transient dip and overshoot. To measure the quiescent current, the load was disconnected and the supply was directly fed through the DC voltage source with an ammeter connected in series. Sufficient decoupling capacitors need to be connected at the input for this test.

Table 4. Test Summary (Jun Tape-out)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Voltage	V_{IN}		1.5	1.8	2	V
Output Voltage	V_{OUT}			0.9/1.2		V
Output Ripple	V_{RIPPLE}				15	mV
Transient Regulation		I_{OUT}=1mA to 400mA and back in 1us	-8(4)		4(4)	%
Load current	I_{OUT}	PWM mode PFM mode			400(500) 60(100)	mA mA
Inductor ESR	L_{ESR}	L= 1µH		0.02		Ω
Capacitor ESR	C_{ESR}	C= 10µF		< 1		mΩ
Switching Frequency	f_S			3		MHz
Efficiency	η	V_{OUT}=0.9V V_{IN}=1.8V,I_{OUT}=400mA (PWM mode) V_{IN}=1.8V,I_{OUT}=100mA (PWM mode) V_{IN}=1.8V,IOUT=1mA (PFM mode)	 60 (86) 75 (94) 80 (88)			%
Startup Current[3]	I_{ST}	V_{IN}=1.8V			150	mA
Quiscent Current	Iq	V_{IN}=1.8V,I_{OUT}= 0mA (PFM mode)		18		uA

( ) schematic simulation results

CHAPTER VII

CONCLUSION AND FUTURE WORK

A simple and effective strategy was proposed to maintain high efficiency at very light loads with a small voltage ripple and fast load transient. The technique was shown to be successful for a range of input and output voltages. The Input was varied from 1.3V to 2.0V and the output was made programmable between 0.9V and 1.2V. The faster detection and PWM loop initialization helps in reducing the voltage dip/overshoot. The load transient was seen to be +/- 40mV in the schematic simulations .The output ramp-up/down with programmability was made smooth with a new architecture. This new implementation could also remove the need for compensation change that would have been required with output programmability in a resister ladder feedback when used with an open loop error amplifier. Table 5 shows the comparison of the proposed converter with that reported in litreture.

All of them uses various modifications of the basic PFM and PWM scheme to improve the efficiency throughout the load range. We were able to meet the maximum efficiency at a current as low as 1mA in simulations. The Chip fabricated in the December with the corrections made in the schematic is expected to meet the specifications as reported.

Table 5. Comparison with reported literature

	This Work	[48]	[49]	[54]	[43]
Technology	IBM 0.18um	TSMC 0.25um	TSMC 0.35um	0.25um	TSMC 0.35um
VIN VOUT	1.4-2.0 0.9-1.2	3.0-4.5 1.8	3.0-5.0 1.8	2.8-5.5 1.0-1.8	3.3 1.65
L/C	1uH/10uF	1uH/4.7uF	10uH/10uF	10uH/47uF	4.7uH/4.7uF
Fsw	3MHz	5MHz	1MHz	1.5MHz	1MHz
Vripple	15mV	50mV	35mV	25mV	35mV
Control	PWM/PFM	Dual-Freq Hop	PWM/PFM	PWM/PFM (Ext. Mod sel)	PWM/DSM/PFM
Efficiency	86% @ 1mA	55% @ 5mA	82% @ 1mA	80% @ 1mA	90% @ 1mA
Transient	-/+40 mV 1 to 400mA	+/- 60mV 1 to 500 mA	N/A	25mV 0.1 to 100mA	66mV 30 to 120mA
IQ	18uA	N/A	122uA	4uA	N/A
Area	1.5mm^2	1.38 mm^2	3.57mm^2	2mm^2 (active)	3.2mm^2

REFERENCES

[1] H. Peng, D. Anderson, and M. Hella, "A 100 MHz Two-Phase Four-Segment DC-DC Converter With Light Load Efficiency Enhancement in 0.18μm CMOS," *Circuits and Systems I: Regular Papers, IEEE Transactions on* , vol.60, no.8, pp.2213,2224, Aug. 2013

[2] P.-L. Wong, F. Lee, X. Zhou, and D. Chen, "VRM transient study and output filter design for future processors," *Industrial Electronics Society, 1998. IECON '98. Proceedings of the 24th Annual Conference of the IEEE*, vol.1, no., pp.410, 415 vol.1, 31 Aug-4 Sep 1998

[3] M. Zhang, M. Jovanovic, and F. Lee, "Design considerations for low-voltage on-board DC/DC modules for next generations of data processing circuits," *Power Electronics, IEEE Transactions on* , vol.11, no.2, pp.328,337, Mar 1996

[4] P. Wu and P. Mok, "A Monolithic Buck Converter With Near-Optimum Reference Tracking Response Using Adaptive-Output-Feedback," *Solid-State Circuits, IEEE Journal of* , vol.42, no.11, pp.2441,2450, Nov. 2007

[5] R. Erickson and D. Maksimovic, “Fundamentals of Power Electronics”, 2nd ed. Kluwer Academic Publishers, 2001.

[6] B. Lee, "Understanding the terms and definitions of LDO voltage regulators." *Texas Instruments Application Report- slva079* (1999).

[7] S. Ben-Yaakov and V. Vorperian, "Modeling the switch of PWM convertors (comments, with reply, on `Simplified analysis of PWM converters using models of PWM switch' by V. Vorperian)," *Aerospace and Electronic Systems, IEEE Transactions on* , vol.28, no.3, pp.921,925, Jul 1992

[8] V. Vorperian, "Simplified analysis of PWM converters using model of PWM switch. II. Discontinuous conduction mode," *Aerospace and Electronic Systems, IEEE Transactions on* , vol.26, no.3, pp.497,505, May 1990

[9] C. Basso, "The PWM Switch concept included in mode transitioning SPICE models", *Power Conversion Intelligent Motion (PCIM).* 2005

[10] A. Brown and R. Middlebrook, "Sampled-data modeling of switching regulators." *PESC'81; Power Electronics Specialists Conference*. Vol. 1. 1981.

[11] Maxim, "An Efficiency Primer for Switch-Mode, DC-DC Converter Power Supplies" *APPLICATION NOTE 4266* (2008)

[12] J. Chen, "Determine Buck Converter Efficiency in PFM Mode-By analyzing the light-load efficiency of a synchronous buck operating under pulse frequency modulation control, designers can predict efficiency." *Power Electronics Technology* 33.9 (2007): 28-33.

[13] S. Kim and G. Rincon-Mora, "Achieving high efficiency under micro-watt loads with switching buck DC–DC converters." *Journal of Low Power Electronics* 5.2 (2009): 229-240.

[14] D. Jauregui, B. Wang, and R. Chen, "Power loss calculation with common source inductance consideration for synchronous buck converters."*Texas Instruments, SLPA009A, June* (2011).

[15] D. Solley, "Theory of Operation of V2 Controllers." *O.N. Semiconductor, Application note AND8276.* May. 2009

[16] R. Mammano, "Switching power supply topology voltage mode vs. current mode." *Elektron Journal-South African Institute of Electrical Engineers* 18.6 (2001): 25-27.

[17] W. Lei and T. Man, "A general approach for optimizing dynamic response for buck converter." *Proc. Application notes Onsemi Conductors*(2004).

[18] X. Zhang and D. Maksimovic, "Multimode Digital Controller for Synchronous Buck Converters Operating Over Wide Ranges of Input Voltages and Load Currents," *Power Electronics, IEEE Transactions on*, vol.25, no.8, pp.1958,1965, Aug. 2010

[19] K. Yao, Y. Ren, and F. Lee, "Critical bandwidth for the load transient response of voltage regulator modules," *Power Electronics, IEEE Transactions on*, vol.19, no.6, pp.1454,1461, Nov. 2004

[20] J. Betten and R. Kollman, "Easy calculation yields load transient response." *Power Electronics* (2005): 40-48.

[21] R. Miftakhutdinov, "Analysis and optimization of synchronous buck converter at high slew-rate load current transients," *Power Electronics Specialists Conference, 2000. PESC 00. 2000 IEEE 31st Annual*, vol.2, no., pp.714, 720 vol.2, 2000

[22] K. Yao, M. Xu, Y. Meng, and F. Lee, "Design considerations for VRM transient response based on the output impedance," *Power Electronics, IEEE Transactions on* , vol.18, no.6, pp.1270,1277, Nov. 2003

[23] R. Ridley, "Loop gain crossover frequency." *Switching Power Magazine January* (2001).

[24] R. Redl, B. Erisman, and Z. Zansky, "Optimizing the load transient response of the buck converter," *Applied Power Electronics Conference and Exposition, 1998. APEC '98. Conference Proceedings 1998, Thirteenth Annual* , vol.1, no., pp.170,176 vol.1, 15-19 Feb 1998

[25] B. Arbetter and D. Maksimovic, "DC-DC converter with fast transient response and high efficiency for low-voltage microprocessor loads," *Applied Power Electronics Conference and Exposition, 1998. APEC '98. Conference Proceedings 1998., Thirteenth Annual* , vol.1, no., pp.156,162 vol.1, 15-19 Feb 1998

[26] P.-J. Liu, W.-S. Ye, J.-N. Tai, H.-S. Chen, J.-H. Chen, and Y.-J. Chen, "A High-Efficiency CMOS DC-DC Converter With 9μ s Transient Recovery Time," *Circuits and Systems I: Regular Papers; IEEE Transactions on*; vol.59, no.3, pp.575,583, Mar. 2012

[27] J. Roh, "High-performance error amplifier for fast transient DC-DC converters," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol.52, no.9, pp.591,595, Sept. 2005

[28] M. Song and D. Ma, "A fast-transient over-sampled delta-sigma adaptive DC-DC converter for power-efficient noise-sensitive devices," *Low Power Electronics and Design (ISLPED), 2007 ACM/IEEE International Symposium on* , vol., no., pp.286,291, 27-29 Aug. 2007

[29] C.-L. Chen, W.-J. Lai, T.-H. Liu, and K.-H. Chen, "Zero current detection technique for fast transient response in buck DC-DC converters," *Circuits and Systems, 2008. ISCAS 2008. IEEE International Symposium on*, vol., no., pp.2214, 2217, 18-21 May 2008

[30] S. Jing, W. Xiaobo, Y. Dongqin, and C. Mingyang, "A Capacitor Current Based Adaptive Hysteresis Controlled Fast Transient Response DC-DC Converter," *Power and Energy Engineering Conference (APPEEC), 2010 Asia-Pacific* , vol., no., pp.1,4, 28-31 March 2010

[31] A. Emira, H. Elwan, and S. Abdelaziz, "DC-DC converter with ON-time control in pulse-skipping modulation," *Circuits and Systems (ISCAS), Proceedings of 2010 IEEE International Symposium on* , vol., no., pp.2746,2749, May 30 2010

[32] J. Sun, M. Xu, Y. Ren, and F. Lee, "Light-Load Efficiency Improvement for Buck Voltage Regulators," *Power Electronics, IEEE Transactions on*, vol.24, no.3, pp.742, 751, March 2009

[33] S. Maity and Y. Suraj, "A fixed frequency dual-mode DC-DC buck converter with fast-transient response and high efficiency over a wide load range," *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE* , vol., no., pp.415,420, 17-21 March 2013

[34] L.-F. Shi and L.-Y. Xu, "Frequency compensation circuit for adaptive on-time control buck regulator," *Power Electronics, IET* , vol.7, no.7, pp.1805,1809, July 2014

[35] C.-H. Teng and C.-H. Tsai, "A digital dc-dc buck converter with adaptive on-time PWM/PFM control," *Solid-State and Integrated Circuit Technology (ICSICT), 2014 12th IEEE International Conference on* , vol., no., pp.1,3, 28-31 Oct. 2014

[36] B. Sahu and G. Rincon-Mora, "An Accurate, Low-Voltage, CMOS Switching Power Supply With Adaptive On-Time Pulse-Frequency Modulation (PFM) Control," *Circuits and Systems I: Regular Papers, IEEE Transactions on* , vol.54, no.2, pp.312,321, Feb. 2007

[37] S. Kudva and R. Harjani, "Fully integrated on-chip DC-DC converter with a 450x output range," *Custom Integrated Circuits Conference (CICC), 2010 IEEE* , vol., no., pp.1,4, 19-22 Sept. 2010

[38] O. Trescases, J. Ng, H. Nishio, M. Edo, and T. Kawashima, "A Digitally Controlled DC-DC Converter Module with a Segmented Output Stage for Optimized Efficiency," *Power Semiconductor Devices and IC's, 2006. ISPSD 2006. IEEE International Symposium on*, vol., no., pp.1,4, 4-8 June 2006

[39] M. Mulligan, B. Broach, and T. Lee, "A constant-frequency method for improving light-load efficiency in synchronous buck converters," *Power Electronics Letters, IEEE* , vol.3, no.1, pp.24,29, March 2005

[40] A. Bentolila, "Step-down Switching Regulator Light-load Efficiency Improvement Using Recycled Parasitic Energy, and Gate Voltage Clamping." PhD diss., University of Florida, 2002.

[41] T. Man, P. Mok, and M. Chan, "An Auto-Selectable-Frequency Pulse-Width Modulator for Buck Converters with Improved Light-Load Efficiency," *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, vol., no., pp.440, 626, 3-7 Feb. 2008

[42] V. Yousefzadeh and D. Maksimovic, "Sensorless optimization of dead times in DC-DC converters with synchronous rectifiers," *Power Electronics, IEEE Transactions on*, vol.21, no.4, pp.994, 1002, July 2006

[43] H.-W. Huang, K.-H. Chen, and S.-Y. Kuo, "Dithering Skip Modulation, Width and Dead Time Controllers in Highly Efficient DC-DC Converters for System-On-Chip Applications," *Solid-State Circuits, IEEE Journal of* , vol.42, no.11, pp.2451,2465, Nov. 2007

[44] C.-H. Chia, P.-S. Lei, and R.-H. Chang, "A high-efficiency PWM DC-DC buck converter with a novel DCM control under light-load," *Circuits and Systems (ISCAS), 2011 IEEE International Symposium on* , vol., no., pp.237,240, 15-18 May 2011

[45] X. Zhou, M. Donati, L. Amoroso, and F. Lee, "Improve light load efficiency for synchronous rectifier buck converter," *Applied Power Electronics Conference and Exposition, 1999. APEC '99. Fourteenth Annual*, vol.1, no., pp.295, 302 vol.1, 14-18 Mar 1999

[46] S. Shin, D. Heo, H. Ko, and B. Park, "High efficiency DC-DC converter with auto-mode transition for mobile SOC applications," *SoC Design Conference (ISOCC), 2010 International* , vol., no., pp.345,348, 22-23 Nov. 2010

[47] C.-L. Chen, W.-L. Hsieh, W.-J. Lai, K.-H. Chen, and C.-S. Wang, "A new PWM/PFM control technique for improving efficiency over wide load range," *Electronics, Circuits and Systems, 2008. ICECS 2008. 15th IEEE International Conference on*, vol., no., pp.962, 965, Aug. 31 2008-Sept. 3 2008

[48] J.-C. Tsai, T.-Y. Huang, W.-W. Lai, and K.-H. Chen, "Dual modulation technique for high efficiency in high switching buck converters over a wide load range," *Circuits and Systems (ISCAS), Proceedings of 2010 IEEE International Symposium on* , vol., no., pp.3709,3712, May 30 2010

[49] W.-R. Liou, M.-L. Yeh, and Y. Kuo, "A High Efficiency Dual-Mode Buck Converter IC For Portable Applications," *Power Electronics, IEEE Transactions on* , vol.23, no.2, pp.667,677, March 2008

[50] H. Forghani-zadeh and G. Rincon-Mora, "An Accurate, Continuous, and Lossless Self-Learning CMOS Current-Sensing Scheme for Inductor-Based DC-DC Converters," *Solid-State Circuits, IEEE Journal of*, vol.42, no.3, pp.665,679, March 2007

[51] A. Esmaili and Y. Shirazi, "Combined current sensing in power electronic applications for increasing SNR ratio." *International Research Journal of Applied and Basic Sciences* 5.9 (2013): 1155-1163.

[52] B. Mammano, "Current sensing solutions for power supply designers."*Unitrode Seminar Notes SEM1200*. 1999.

[53] T. Man, P. Mok, and M. Chan, "Design of Fast-Response On-Chip Current Sensor for Current-Mode Controlled Buck Converters with MHz Switching Frequency," *Electron Devices and Solid-State Circuits, 2007. EDSSC 2007. IEEE Conference on* , vol., no., pp.389,392, 20-22 Dec. 2007

[54] J. Xiao, A. Peterchev, J. Zhang, and S. Sanders, "A 4-μa quiescent-current dual-mode digitally controlled buck converter IC for cellular phone applications," *Solid-State Circuits, IEEE Journal of*, vol.39, no.12, pp.2342,2348, Dec. 2004

[55] V. Michal, "Inductor Current Zero-Crossing Detector and CCM/DCM Boundary Detector for Integrated High-Current Switched-Mode DC–DC Converters," *Power Electronics, IEEE Transactions on* , vol.29, no.10, pp.5384,5391, Oct. 2014

[56] G. Rincon-Mora and H. Forghani-zadeh, "Using a circuit-driven approach to teach printed-circuit board (pcb) layout techniques for switching power supply circuits." (2010).

[57] Maxim, “Line and Load Transient Testing for Power Supplies.” *APPLICATION NOTE 3443* (2005)

[58] J. Barrow, “Understand and reduce DC/DC switching converter ground noise.” *EETimes*, Nov. 2011