Effect of Boron Incorporation on Slow Interface Traps in Si02/4H-SiC Structures

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Effect of Boron Incorporation on Slow Interface Traps in SiO_2/4H-SiC Structures

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Abstract The reason for the effective removal of interface traps in SiO_2/4H-SiC (0001) structures by boron (B) incorporation was investigated by employing low-temperature electrical measurements. Low-temperature capacitance–voltage and thermal dielectric relaxation current measurements revealed that the density of electrons captured in slow interface traps in B-incorporated oxide is lower than that in dry and NO-annealed oxides. These results suggest that near-interface traps can be removed by B incorporation, which is considered to be an important reason for the increase in the field-effect mobility of 4H-SiC metal–oxide–semiconductor devices. A model for the passivation mechanism is proposed that takes account of stress relaxation during thermal oxidation.

Keywords SiC · MOS interface · Near interface traps · Boron diffusion · Thermal dielectric relaxation current

1 Introduction

Silicon carbide (SiC) has attracted considerable attention over the last decade as a promising candidate for use in next-generation power devices for high-voltage and high-temperature applications. SiC power metal–oxide–semiconductor field-effect transistors (MOSFETs) have been commercialized and gradually put into practical use since the early 2010s. However, the channel resistance in the latest 4H-SiC power MOSFETs still accounts for about half the total conduction loss. Despite many years of process development on 4H-SiC MOS devices, the interface state density (D_{it}) remains high, resulting in low field-effect mobility. In particular, 4H-SiC MOSFETs fabricated by dry oxidation on a (0001) Si-face exhibit a field-effect mobility below 10 $cm^2V^{-1}s^{-1}$ [1], which hinders the development of planar-type SiC MOS devices. If we are to develop future-generation SiC power MOSFETs while achieving a low conduction loss, we must elucidate both the cause of the high interface state density and its passivation mechanisms.

Several annealing methods have been proposed for reducing D_{it} and enhancing the field-effect mobility of 4H-SiC MOSFETs. One of the best ways to reduce D_{it} is the nitridation of the interface with NO or N_2O gases [2–4]. Field-effective mobilities of 20–50 $cm^2V^{-1}s^{-1}$ and good oxide reliability can be obtained by the nitridation of the (0001) Si-face of 4H-SiC [3,4] and this process currently constitutes the industrial standard. Further mobility enhancement up to around 170 $cm^2V^{-1}s^{-1}$ has been achieved by sodium-enhanced oxidation on the (0001) Si-face of 4H-SiC [5]. In addition, we have reported that the incorporation of phosphorus (P) into a SiO_2/4H-SiC interface results in a low D_{it} and a high field-effect mobility of up to 89 $cm^2V^{-1}s^{-1}$ on the (0001) Si-face of 4H-SiC [6].

More recently, we have reported that the incorporation of boron (B) into a SiO_2/4H-SiC(0001) interface reduces D_{it} close to the conduction band edge of 4H-SiC [7]. A boron nitride (BN) planar diffusion source was used as the B source, and the fabricated MOSFETs exhibited a field-effect mobility of 102 $cm^2V^{-1}s^{-1}$ [7].

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In addition, Soler *et al.* reported the 4.5 kV 4H-SiC power MOSFETs with the B-doped gate oxide combined with a deposited SiO_2, demonstrating both the low on-resistance and relatively stable threshold voltage [8]. Therefore, the B diffusion is one promising process for the next-generation SiC power devices. This technique is unique in terms of utilizing a group III element. The fact that D_{it} can be reduced by B is in clear contrast to the many conventional passivation methods which are based on group V elements that act as donors in a 4H-SiC substrate [9,10]. The mechanism behind the improved field-effect mobility by the B incorporation remains unclear, and detailed investigations are required.

Here, we would like to discuss possible origins of interface traps at the SiO_2/4H-SiC interface. Afanas'ev *et al.* suggested three possible origins for the interface states at the SiO_2/4H-SiC interface: (i) Si or C dangling bonds, (ii) C clusters, and (iii) near-interface traps (NITs) [11,12]. Of these, NITs may play a dominant role because they are considered to create trap levels close to the conduction band edge of 4H-SiC at a high density [11–14]. It has been reported that NITs can be effectively removed by the incorporation of N [15], Na [16], K [17], and P [18] as revealed either by using low-temperature capacitance–voltage (C–V) [15,18] or thermal dielectric relaxation current (TDRC) [16–18] measurements. It is interesting to note that improved field-effect mobilities can be obtained by utilizing oxides incorporating N [3,4], Na [5], and P [6], and thus we can assume that the NIT density is closely related to the field-effect mobility. This makes it also important to investigate the nature of NITs in B-incorporated MOS structures for a comprehensive understanding of the origin of interface states and the passivation mechanisms in the SiO_2/4H-SiC interface structures.

In this study, we investigated the density of the trapped electrons in the NITs in the B-incorporated gate oxides in comparison with that in conventional dry and NO-annealed oxides. We employed C–V measurements at a low temperature [14] and TDRC measurements [19] to analyze the density of NITs. We discuss a possible mechanism for the improved field-effect mobility based on the excess Si atoms near the interface and interface stress during oxidation, and propose a model of the passivation mechanism. Some researchers have pointed out that near-interface oxide traps are also located close to the 4H-SiC valence band edge [20–22]. However, in this study, we focus on the NITs located close to the conduction band edge of 4H-SiC, which are strongly related to the channel mobility of 4H-SiC MOSFETs. Thus, we evaluated n-type MOS capacitors to investigate the NITs close to the conduction band edge of 4H-SiC.

2 Experimental details

N-type MOS capacitors were fabricated on n-type 4°-off 4H-SiC (0001) Si-face epitaxial layers with a net donor concentration of 1×10^{16} cm^{-3}. MOS capacitors with three different gate oxides were fabricated: (i) dry, (ii) NO-annealed, and (iii) B-incorporated oxides. After standard RCA cleaning, oxides approximately 47 nm thick were formed by dry oxidation at 1200 °C for 170 min. For the dry + NO samples, post oxidation annealing was performed in 20%-diluted NO (NO/Ar = 1.0/4.0 slm) at around 1350 °C for 3 min using a cold-wall furnace [23]. For the dry + B-diffusion samples, the dry-oxidized substrate was put into a three-zone hot-wall oxidation furnace and placed about 1 mm from a planar diffusion source (Saint-Gobain, BN-975) composed of BN and 3.5–6.5% boric oxide (B_2O_3). The sample was then annealed at 950 °C for 10 min in an O_2 (0.2 slm) and Ar (1.8 slm) gas mixture. The sample was subsequently annealed in Ar at 950 °C for 120 min without the BN plate. Al was evaporated to form gate and backside electrodes. The diameter of the gate electrodes was 400 μm. High-frequency C–V measurements (100 kHz or 1 MHz) were implemented using an Agilent 4294A impedance analyzer. Low-frequency (1 Hz) C–V measurements were performed using an Agilent ultra-low-frequency C–V system, which consisted of an Agilent B1500A and an Agilent 33210A function generator. TDRC measurements were carried out at temperatures between 40 and 300 K with a constant heating rate of 0.333 K/s (20 K/min) using a Keithley 4200 semiconductor characterization system equipped with preamps. The TDRC measurement is described in detail in Ref. [19].

3 Results

First, the D_{it} distributions were estimated by employing the hi-lo C–V method using 1 Hz and 1 MHz curves. Figure 1 shows the D_{it} distribution against the trap energy (E) from the conduction band edge (E_c) of 4H-SiC for dry, NO-annealed, and B-incorporated oxides as basic information about the fabricated samples. Note that the estimated D_{it} values only reflect the interface traps that can respond to the 1 Hz to 1 MHz frequency range due to the limitation of the Hi-Lo method [24, 25], and faster and shallower interface traps were not fully evaluated. Nevertheless, it is clear that B incorporation can reduce D_{it} by more than an order of magnitude. The peak field-effect mobility values for the 4H-SiC MOSFETs fabricated on the (0001) Si-face were 4, 17, and 102 cm^{2}V^{-1}s^{-1} for dry, NO-annealed, and B-incorporated oxides, respectively (not discussed in this

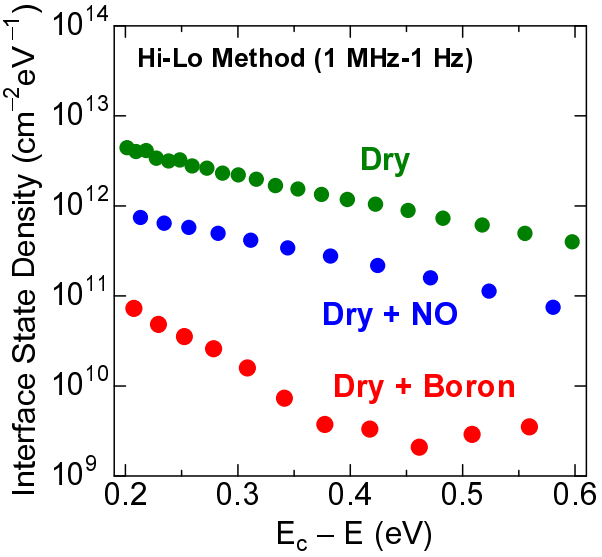

Fig. 1 Distributions of interface state density close to the conduction band edge of 4H-SiC for dry, NO-annealed, and B-incorporated oxides.

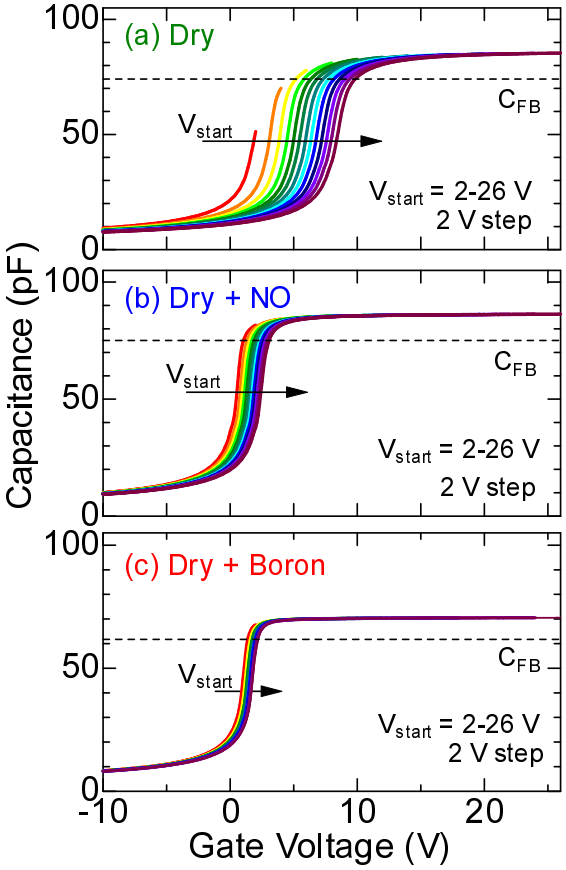

Fig. 2 Start-voltage dependence of high-frequency (100 kHz) C–V curves measured at 80 K for (a) dry, (b) NO-annealed, and (c) B-incorporated oxides. The gate voltage was swept from accumulation to depletion. The start voltage was increased from 2 to 26 V in 2-V steps. The dashed lines denote flat-band capacitance (C_{FB}) at 80 K.

paper). The characteristics of B-diffused MOSFETs are described in Ref. [7].

One of the most convenient ways to investigate the slow interface traps at the SiO_2/4H-SiC interface is to measure the start-voltage dependence of C–V curves at a sufficiently low temperature, as originally proposed by Afanas'ev *et al.* [14]. Figure 2 shows the start-voltage dependence of high-frequency (100 kHz) C–V curves measured at 80 K for the (a) dry, (b) NO-annealed, and (c) B-incorporated oxides. The gate voltage was swept from accumulation to depletion, and the C–V measurements were iterated while the start voltage was increased from 2 to 26 V in 2-V steps. The sweep rate was approximately 0.5 V/s. We used 100 kHz as the measurement frequency to avoid the decrease in accumulation capacitance due to series resistance. Parallel shifts in the C–V curves in the positive direction were observed for the dry and NO-annealed oxides that depended on the start voltage, suggesting that the electrons were captured in the traps located on the oxide side of the interface [14,15]. The electrons are thought to be captured by the NITs whose energy position is aligned close to the conduction band edge of 4H-SiC [11–14] because the Fermi level is very close to the conduction band edge in strong accumulation conditions. The time constant of the NITs is long because of the separation from the interface [11–13]. The electrons trapped in the NITs act like negative fixed charges in the oxide at 80 K, and, as a result, a parallel shift of the C–V curves in the positive direction was observed. The start voltage dependence effectively decreased for the B-incorporated oxide. This result indicates that the density of the NITs decreased more significantly in the B-incorporated samples than in the NO-annealed samples. The slight shift in the low-temperature C–V curves in the B-incorporated sample may be due to the imperfect passivation of the slow traps. Even though there is a slight shift in the C–V curves for the B sample, the shift is always smaller than for the NO samples at 80 K.

TDRC measurements were carried out to estimate the slow interface trap density. The heating rate (β) was 0.333 K/s and the discharging voltage (V_{dis}) was −5 V. The discharging voltage is not so important because we have confirmed that almost the same TDRC curves can be obtained at $V_{dis} = -10$ V. Figure 3 shows the TDRC curves at which the oxide electric field $E_{ox} = 3.0 \pm 0.1$ MV/cm. It is generally difficult to determine the oxide electric field precisely, but the charges in the oxide

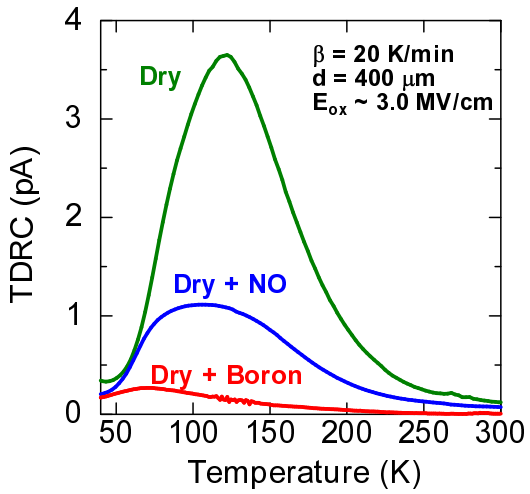

Fig. 3 TDRC spectra for dry, NO-annealed, and B-incorporated oxides. The oxide electric field during charging was approximately 3.0 ± 0.1 MV/cm. The heating rate (β) was 0.333 K/s. The discharging voltage ($V_{\rm dis}$) was -5 V.

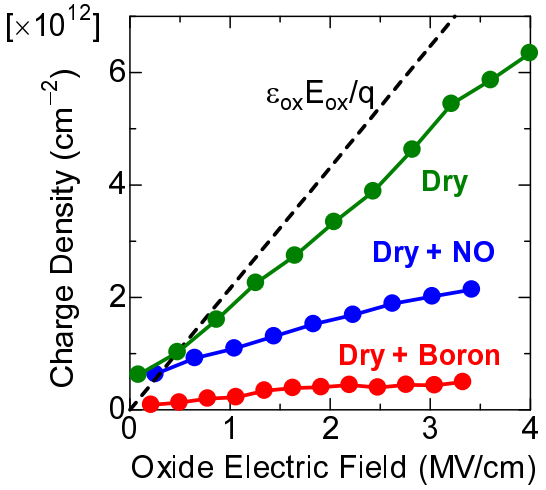

Fig. 4 Density of emitted electrons from NITs as a function of the estimated electric field across the oxide during charging. The dashed line denotes the total accumulated charge at the SiO_2/4H-SiC interface during charging.

seem to affect the $E_{\rm ox}$ value. Thus, in this study, we assumed that $E_{\rm ox} \approx (V_{\rm G} - V_{\rm FB,RT})/t_{\rm ox}$, where $V_{\rm G}$ is the gate voltage and $V_{\rm FB,RT}$ is the flat-band voltage measured at 1 MHz at room temperature, and $t_{\rm ox}$ is the oxide thickness determined by the accumulation capacitance assuming the dielectric constant to be 3.9. A large TDRC spectrum can be found in the dry sample due to the negative charges emitted from the slow interface traps. Rudenko *et al.* suggested that the TDRC spectrum observed in the 50–250 K temperature range is a signal caused by the electrons emitted from the NITs spatially located in the SiO_2 near the SiO_2/4H-SiC interface, rather than fast interface states that reside exactly at the interface [19]. The parallel shift observed in the C–V measurements at a low temperature also supports the detection of NITs [19]. The TDRC spectrum was reduced by NO annealing, but its effect was insufficient to passivate the active NITs. On the other hand, a much smaller TDRC spectrum was observed for the B-incorporated oxide, indicating that the NITs were effectively passivated. The TDRC curve for the B-incorporated sample is similar to those of the Na-incorporated [16] and P-incorporated samples [18], implying that their passivation mechanisms are similar.

By integrating a TDRC curve, we can estimate the density of the thermally stimulated electrons from the NITs [19]. The emitted charge density $N_{\rm em}$ is described as

$$N_{\rm em} = \frac{1}{\beta} \int_{T_{\rm low}}^{T_{\rm high}} |J_{\rm TDRC}(T)| dT \qquad (1)$$

where, $T_{\rm high}$ is the upper limit of the evaluable temperature, $T_{\rm low}$ is the lower limit of the evaluable temperature, $J_{\rm TDRC}$ is the thermally-stimulated current density (A/cm^2), and β is the ramp rate during heating (K/sec) [19]. The TDRC spectra were integrated in the 40 to 300 K temperature range because the constant heating rate is realized only at temperatures above 40 K in our measurement setup.

Figure 4 shows the $E_{\rm ox}$ dependence of the thermally stimulated charge density calculated with Eq. (1). As $E_{\rm ox}$ increases, the emitted charge density increases, particularly for the dry oxide. As the charging voltage increases, the electron density in the accumulation layer of an n-type MOS capacitor increases, and then the vast majority of the accumulated electrons are captured by the NITs for the dry oxide. The electron density in the accumulation layer was roughly estimated with $\epsilon_{\rm ox}E_{\rm ox}/q$ and is indicated in Fig. 4 with a broken line, where $\epsilon_{\rm ox}$ is the permittivity of the oxide and q is the elementary charge. Most of the accumulated electrons were captured by the slow traps for the dry oxide, whereas it is clear that the trapped charge density was reduced substantially by the B incorporation. For dry oxide, the thermally stimulated electron density does not reach the saturation value in the measured bias range, and the NIT density is at least 6×10^{12} cm^{-2} and may exceed 1×10^{13} cm^{-2}. The NIT density of the NO-annealed oxide decreased by more than a factor of two. The NIT density was further reduced by the B-incorporated oxide. The reduction in the TDRC spectra is in good agreement with the early results ob-

tained with Na and P incorporation [16,18], suggesting that the NIT density is strongly related to the field effect mobility.

4 Discussion

The two experiments described above revealed that the acceptor-type slow electron traps reside close to the conduction band edge of 4H-SiC particularly for the dry oxide, which agrees with the findings of early studies [14–19]. These slow traps can be effectively passivated by B incorporation. The observed slow interface traps cannot be explained solely by the fast interface states that reside exactly at the interface, and it is necessary to take the existence of NITs into account [14,19]. It has also been shown that the electron capture cross-section of the interface traps varies by several orders of magnitude and the value is small near the conduction band edge [26,27]. This implies that the traps are located in the oxide near the interface, and the capture cross-section is small because of the distance from the interface. If the electrons are captured by the NITs, the channel electron density is reduced and the estimated field-effect mobility decreases. Although the NITs are believed to be located in the oxide within a few nanometers of the interface [11,13], some of them may also impede the channel electron transport due to remote Coulomb scattering.

Afanas'ev *et al.* suggested that the NITs are inherent defects in SiO_2 located near the interface, and their energy position is 2.8 eV below the conduction band edge of SiO_2 [11,13]. Schöner *et al.* also suggested that the defect levels close to the conduction band edge of SiC are identical for 4H-, 6H-, and 15R-SiC, and they are energetically pinned at around 2.9 eV above the valence band edge of all the SiC polytypes [28]. The microscopic nature of NITs is still unknown, but excess Si atoms in SiO_2 [11–14], C=C dimers [29], and Si_2-C-O defects [30] have been proposed as possible candidates. However, the experimentally determined fact that the energy position of NITs is identical for both Si and SiC substrates [11,13] cannot be explained by the C-related defect structures. Thus, it may be reasonable to assume that the origin of NITs is Si-related defects as suggested by Afanas'ev *et al.* [11–14].

Although there is still a lack of convincing evidence for the physical origin of the NITs, their creation may be related to interface stress [15,18]. We consider that one possible origin for the NITs is excess Si atoms accumulated near the interface during thermal oxidation caused by interface stress. Si atoms are believed to be released from the interface during thermal oxidation both for the Si and SiC substrates to release the interface stress caused by volume expansion [31–33]. During the thermal annealing used for incorporating B atoms, the oxide thickness increased from 47 to 65 nm [7], meaning that there was additional thermal oxidation of the 4H-SiC substrate. A new interface is formed during this additional thermal oxidation, and B atoms are incorporated into the interface. B_2O_3 is known as a network former that reduces the connectivity of SiO_2 network [34], which is similar to the case of P_2O_5 incorporation [35]. Thus, the interface stress that occurs during thermal oxidation as a result of the volume expansion may be easily released because of the flexible oxide network realized by B incorporation [34]. This may lead to reduced NIT density and consequently high field-effect mobility in 4H-SiC MOSFETs. This interpretation is very similar to the case of P incorporation [18]. However, this result is very important because both the elements have similar effect for reducing the slow traps. P is in group V in the periodic table, whereas B is in group III. Therefore, the passivation of the slow interface traps is not related to the group number in the periodic table, but it may be related to the interface stress. Although the model discussed in this paper is currently speculative, this result will facilitate future investigations from a new perspective designed to improve the SiO_2/4H-SiC interface quality. In light of the interface stress, further experimental and theoretical investigations are needed to verify the proposed model and identify the passivation mechanisms that account for the high field-effect mobility obtained by B incorporation.

5 Conclusions

In this study, low-temperature C–V and TDRC measurements were employed to investigate the change in NIT density caused by B incorporation. The most important result we obtained is that the NITs were significantly reduced by B incorporation, which is similar to the case of P and Na incorporation by which high field-effect mobilities can be obtained. We discussed a model in which the possible origin of the NITs is accumulated Si atoms resulting from interface stress caused by volume expansion during thermal oxidation. We consider that B incorporation reduces the interface stress during thermal oxidation, thus lowering the NIT density. Therefore, we suggest that it is important to find a technology that minimizes interface stress during thermal oxidation to improve the field-effect mobility of 4H-SiC MOSFETs.

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