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The direct synthesis of multilayer graphene (MLG) on arbitrary substrates is essential for incorporating carbon wirings and heat spreaders into electronic devices. Here, we applied the metal-induced layer exchange (MILE) technique, developed for group-IV semiconductors, to a sputtered a-C thin film using Co as a catalyst. MLG was formed on a SiO_2 substrate at 800 °C for 10 min; however, it disappeared during wet etching for removing Co. This behavior was attributed to the small contact area between MLG and SiO_2 caused by the deformation of the Co layer during annealing. By preparing the Co layer at 200 °C, its thermal stability was improved, resulting in the synthesis of MLG on the substrate through MILE. Raman measurements indicated good crystal quality of the MLG compared with that obtained by conventional metal-induced solid-phase crystallization. MILE was thus proven to be useful not only for group-IV semiconductors but also for carbon materials on insulators.

1. Introduction

Graphene has garnered enormous interest because of its excellent transport properties leading to various advanced devices.[1] For applications handling large current or heat, thick multilayer graphene (MLG) is more favorable than few-layer graphene.[2–4] For example, a low-resistance wiring requires a thickness of several tens of nanometers to replace a Cu wiring in large-scale integrated circuits; a heat spreader requires a thickness of more than several micrometers depending on the kind of device. MLG on arbitrary substrates therefore opens up possibilities for fabricating advanced electronic devices. Since graphene has a unique two-dimensional structure, its characteristics are anisotropic and deteriorated by grain boundaries.[5,6] In line with this, large-grained, highly oriented MLG on insulators has been desired.

Mechanical transfer has allowed for the synthesis graphene on arbitrary substrates.[1] However, because the transfer causes damage to graphene including wrinkles, a transfer-free process is required for practical device applications. The low-temperature synthesis of graphene on insulators has been achieved by chemical vapor deposition (CVD) [7–10] and plasma-assisted vapor deposition [11,12] with metal catalysts (e.g., Cu, Ni, Fe, and Co). These techniques are useful for directly forming few-layer graphene on insulators but not stable for forming thick MLG, which is necessary for carrying large current or heat. In recent years, the metal-induced solid-phase crystallization of amorphous carbon (a-C) or polymers has attracted increasing attention for the direct synthesis of MLG on insulators at relatively low temperatures (< 900 °C).[13–24] Some of the techniques have allowed for the synthesis of thick (> 5 nm) MLG by controlling the initial thickness of a-C.[18–24] However, there are still more investigations necessary to achieve uniform MLG of high quality on insulators.

The metal-induced layer exchange (MILE) technique has been developed in the field of group-IV semiconductors including Si,[25–30] Ge,[31–36] and SiGe.[37–39] MILE has induced the growth of large-grained (> 50 μm), highly-oriented thin films on insulators at relatively low temperatures.[26,32] In MILE, an amorphous semiconductor layer crystallizes through "layer exchange" between the amorphous layer and a catalyst metal layer. To induce layer exchange, it is important to choose an appropriate metal where semiconductor atoms can dissolve without making compounds.[27,28] From binary phase diagrams, we found that Co would work as a catalyst metal for the layer exchange crystallization of a-C. In this study, we applied

MILE to a-C to synthesize a thick MLG layer on an insulator. The high-quality MLG layer was formed at 800 °C by layer exchange, which is a relatively low temperature among the fabrication techniques for MLG.

2. Experimental methods

The concept of this study is shown in Fig. 1(a). We aimed at the layer exchange between a-C and Co layers. Co and a-C thin films (50 nm thickness each) were sequentially prepared on a quartz glass (SiO_2) substrate at room temperature (RT) by radio-frequency (RF) magnetron sputtering (base pressure: 3.0×10^{-4} Pa) using Ar plasma. The RF power was set to 50 W for Co and 100 W for a-C. The sample was annealed at 800 °C for 10 min in Ar ambient to form MLG on the substrate via layer exchange. After annealing, the sample was evaluated by Nomarski optical microscopy, scanning electron microscopy (SEM), energy-dispersive X-ray (EDX) analysis (acceleration voltage: 10 kV, detection depth: approximately 1 μm), and Raman spectroscopy (spot diameter: 5 μm, wavelength: 532 nm). HNO_3 solution (HNO_3: 15%) was used to etch away Co after annealing.

3. Results and discussion

Figure 1(b) shows Raman spectra obtained from the front and back sides of the sample before annealing. For the front side, a broad peak is observed at around 1500 cm^{-1}, corresponding to a-C.[19] In contrast, for the back side, there is no peak related to C. We note that small peaks at around 1100 cm^{-1} originate from the substrate. These results ensure that an a-C layer is stacked on a Co layer without mixing before annealing.

The sample was annealed at 800 °C for 10 min. The results are shown in Fig. 2. Figure 2(a) shows the SEM image of the sample surface, indicating two contrasts: black and gray areas. The EDX maps shown in Figs. 2(b) and 2(c) indicate that the black area in Fig. 2(a) corresponds to C, while the gray area corresponds to Co. Figure 2(d) shows the Raman spectra obtained from the front and back sides of the sample. For both sides, sharp peaks are observed at around 1350, 1580, and 2700 cm^{-1}, corresponding to D (disordered mode), G (graphitic mode), and 2D (D mode overtone) peaks in the graphitic structure, respectively.[19]

The intensity of the G peaks is more than double that of the 2D peaks, indicating the synthesis of "multilayer" graphene.[18,19,22] We note that the peaks of the back side are weaker than those of the front side because the Raman laser decays in the SiO_2 substrate. From these results, the sample structure is estimated as shown in Fig. 2(e). MLG does not cover the whole surface of the substrate. In MILE, the configuration of the resulting semiconductor layer reflects that of the metal layer.[30,32] Therefore, the present morphology of MLG arises from the deformation of the Co layer during annealing. We attempted to remove Co to obtain only MLG on the substrate; however, MLG disappeared together with Co during wet etching. This is attributed to the insufficient coverage of MLG on the substrate, i.e., the small contact area between MLG and SiO_2. To synthesize a uniform MLG layer on the substrate, we focused on the thermal stability of the Co layer.

To suppress the deformation of a Co layer during annealing, we sputtered the Co layer at 200 °C. The Co layers formed on SiO_2 substrates at RT or 200 °C were annealed at 600 °C for 30 min to examine the thermal stability. As shown in Fig. 3, the Co layers have black areas on the surfaces in both cases, corresponding to holes caused by agglomeration during annealing. The comparison between Figs. 3(a) and 3(b) clearly shows that the density of holes in the Co layer is significantly lowered by preparing the layer at 200 °C. We therefore employed the Co layer prepared at 200 °C for the layer exchange growth of a-C.

An a-C layer was sputtered at RT on the Co layer sputtered at 200 °C, and then annealed at 800 °C for 10 min. The results are shown in Fig. 4. Figure 4(a) shows the SEM image of the sample surface, indicating three contrasts: black, white, and gray areas. The EDX maps shown in Figs. 4(b) and 4(c) indicate that the black area in Fig. 4(a) corresponds to C, the white area corresponds to Co, and the gray area corresponds to both Co and C. Figure 4(d) shows the Raman spectra obtained from the front and back sides of the sample. For both sides, peaks corresponding to MLG are present. We note that the intensity of the G peak of the back side is much higher than that of the front side. Considering that the Raman signals obtained from the back side decay in the SiO_2 substrate, MLG dominantly forms on the back side. From the results in Figs. 4(a)-4(d), the sample structure is estimated as shown in Fig. 4(e). Thus, the layer exchange between Co and C occurred in almost the entire sample surface. This result originates from the thermal stability of the Co layer improved by preparing the layer at 200 °C. This means that the coverage of MLG on the substrate

improved.

We dipped the sample in HNO$_3$ solution for 2 min to remove Co. As a result, a thin film survived on the substrate as shown in the photograph inserted in Fig. 5(a). The SEM images in Figs. 5(a) and 5(b) show the two-step structure, which is consistent with the C structure illustrated in Fig. 4(e). To identify the element of the thin film, we performed EDX analysis. The result in Fig. 5(c) suggests that the thin film consists of C. The peaks corresponding to Si and O originate from the SiO$_2$ substrate because the detection depth is more than the thickness of the C layer (50 nm). We note that the Co concentration in the C layer was below the detection limit of EDX (~1%). This is a typical feature in the semiconductor layers on insulators obtained via MILE.[32,38] The Raman spectrum of the resulting sample is shown in Fig. 5(d), indicating the synthesis of MLG. The intensity ratio of G to D peaks corresponds to the crystal quality of MLG.[10.13] The value of the back side (1.86) is larger than that of the front side (1.58) of the sample. These results indicate that the crystal quality of the MLG layer is different between the front and back sides: the back side has a higher crystal quality than the front side. This behavior is likely attributed to the formation of small-grained MLG islands, which is a typical feature in MILE.[25,36] The values of the G/D ratio indicate the high quality of the resulting MLG compared with the MLG directly synthesized by metal-induced solid-phase crystallization at around 800 °C.[19,22,24] Since MILE has many growth parameters such as the thickness, growth temperature, and interface conditions,[26,32,34,35] further investigations will enable us to further improve the uniformity and crystal quality of the MLG on an insulating substrate.

4. Conclusions

To directly synthesize multilayer graphene (MLG) on an insulating substrate, the MILE technique was applied to a sputtered a-C thin film using Co as a catalyst. MLG was formed on a SiO$_2$ substrate by postannealing in Ar at 800 °C for 10 min; however, it disappeared together with Co during wet etching. This behavior was attributed to the small contact area between MLG and SiO$_2$ caused by the deformation of the Co layer during annealing. By preparing the Co layer at 200 °C, its thermal stability was improved, resulting in the synthesis of MLG on the substrate through layer exchange between Co and a-C. Raman measurements

indicated good crystal quality of the MLG compared with the MLG formed by conventional techniques. Thus, we demonstrated that the MILE technique, developed for semiconductors on insulators, is also useful for carbon materials on insulators. Further investigation will open up possibilities for incorporating MLG into advanced electronic devices.

Acknowledgments

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Figure Captions

Fig. 1. (Color online) (a) Concept of this study: layer exchange between Co and a-C layers for the direct synthesis of MLG on an insulating substrate. (b) Raman spectra obtained from the front and back sides of the sample before annealing.

Fig. 2. (Color online) Characterization of the sample after annealing at 800 °C for 10 min, where the Co layer was prepared at RT. (a) SEM image and EDX elemental maps of (b) C and (c) Co. (d) Raman spectra obtained from the front and back sides of the sample. (e) Schematic of the sample estimated from the results in (a)-(d).

Fig. 3. (Color online) Characterization of the thermal stability of the Co layer. (a),(b) Nomarski optical micrographs of the Co layers after annealing at 600 °C for 30 min, where the Co layers were prepared on SiO_2 substrates at (a) RT and (b) 200 °C. The black areas correspond to holes formed by deformation during annealing.

Fig. 4. (Color online) Characterization of the sample after annealing at 800 °C for 10 min, where the Co layer was prepared at 200 °C. (a) SEM image and EDX elemental maps of (b) C and (c) Co. (d) Raman spectra obtained from the front and back sides of the sample. (e) Schematic of the sample estimated from the results in (a)-(d).

Fig. 5. (Color online) Characterization of the annealed sample after removing Co, where the Co layer was prepared at 200 °C. (a, b) SEM images with (a) low and (b) high magnifications. The photograph inserted in (a) shows the sample. (c) EDX spectrum where the peak positions of C and Co are indicated by dotted lines. (d) Raman spectrum obtained from the front side of the sample.
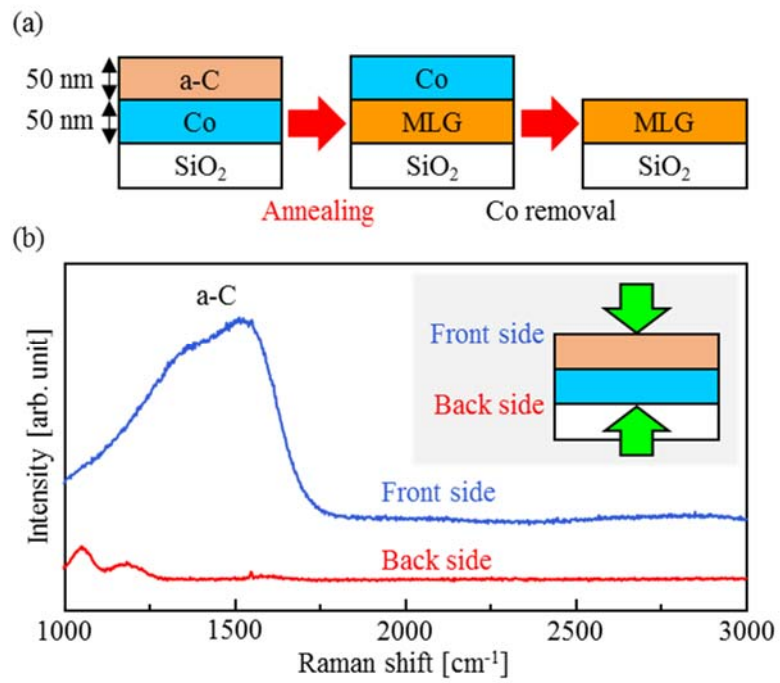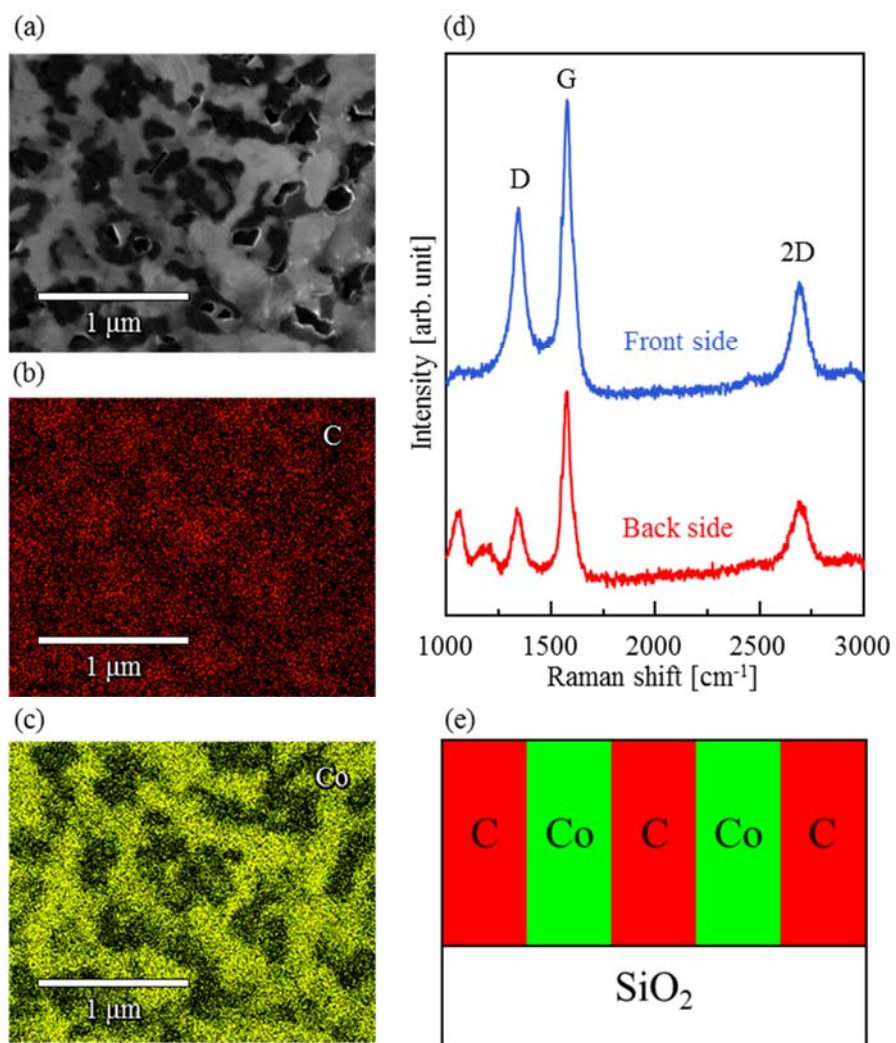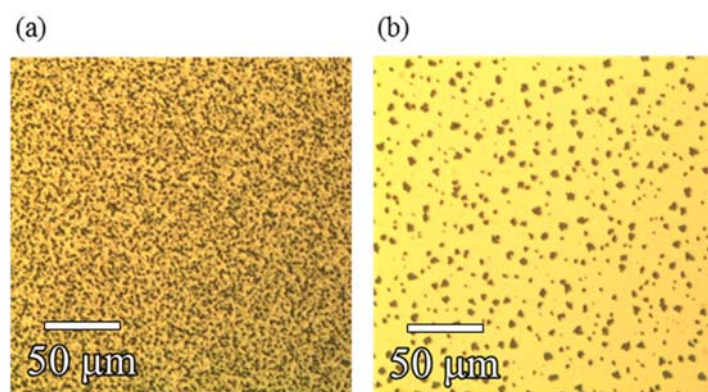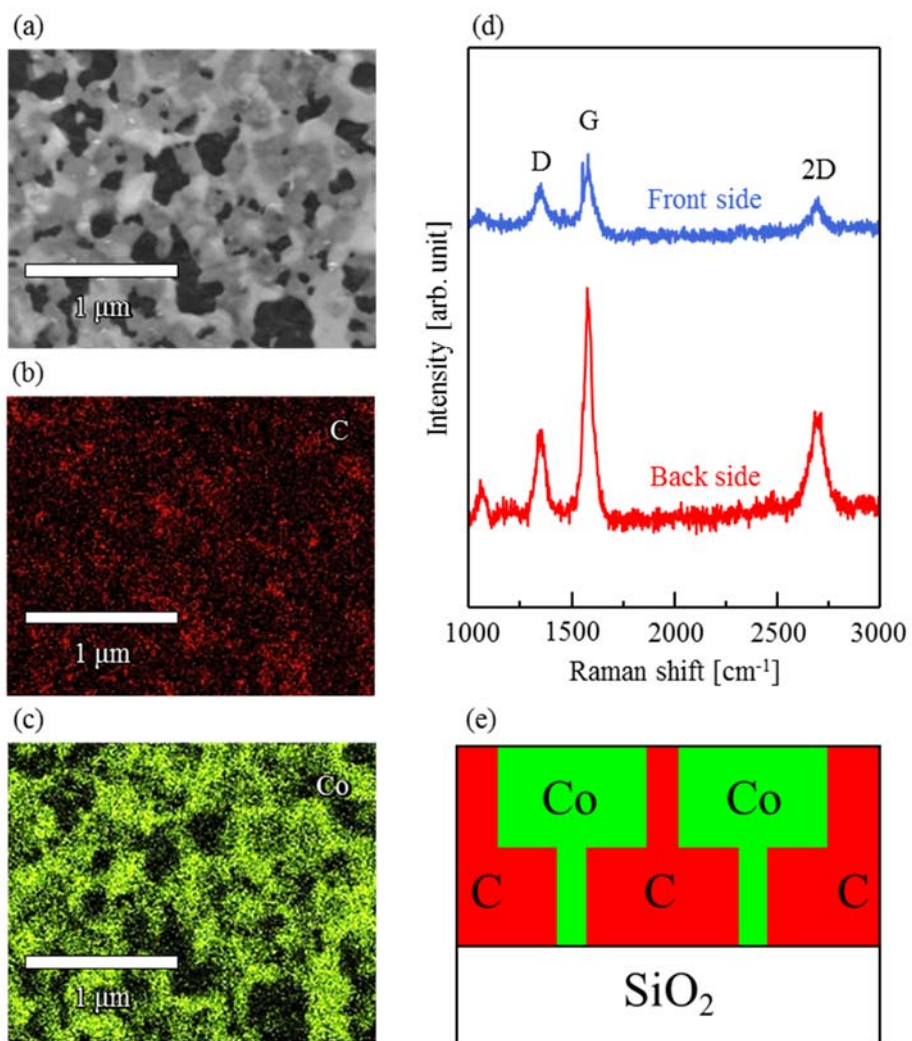
Fig.1.　(Color Online)

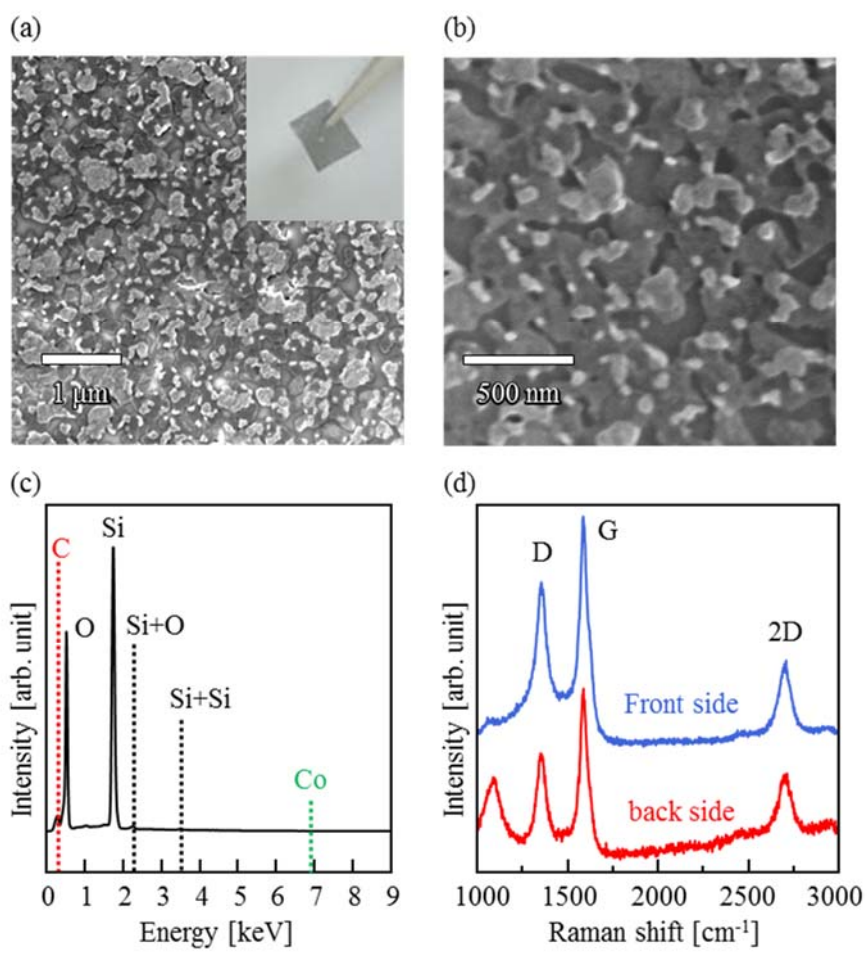Fig.2. (Color Online)

Fig.3. (Color Online)

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