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TIME-OF-FLIGHT SENSORS IN STANDARD CMOS TECHNOLOGIES

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HACEN CONSTAR:

Que la memoria titulada **TIME-OF-FLIGHT SENSORS IN STANDARD CMOS TECHNOLOGIES** ha sido realizada por **D. Julio Illade Quinteiro** bajo nuestra dirección en el Centro Singular de Investigación en Tecnoloxías da Información de la Universidad de Santiago de Compostela, y constituye la Tesis que presenta para optar al título de Doctor.

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A mi familia

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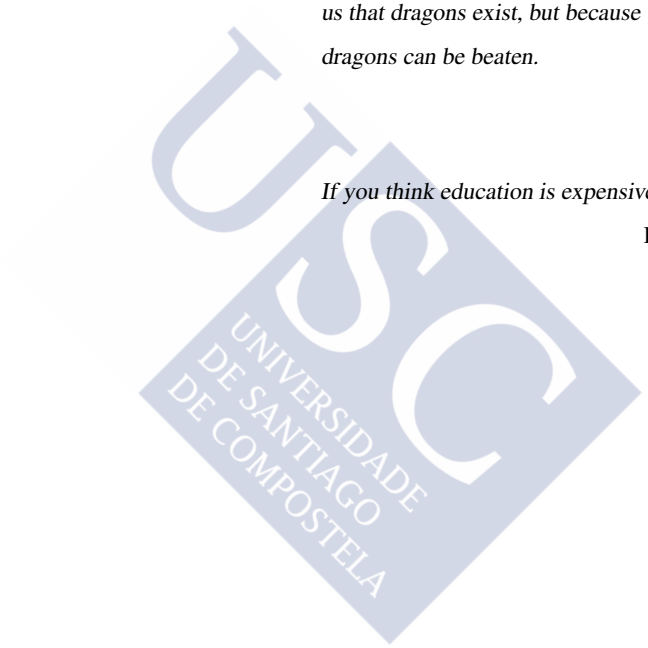
Fairy tales are more than true: not because they tell us that dragons exist, but because they tell us that dragons can be beaten.

Neil Gaiman

If you think education is expensive, try ignorance.

Derek Curtis Bok



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Contents

Resumen de la tesis

Siguiendo el reglamento de los estudios de tercer ciclo de la Universidad de Santiago de Compostela, aprobado en la Junta de Gobierno del día 7 de abril de 2000 (DOG de 6 de marzo de 2001) y modificado por la junta de Gobierno de 14 de noviembrede 2000, el Consejo de Gobierno de 22 de noviembre de 2003, de 18 de julio de 2005 (artículos 30 a 45), de 11 de noviembre de 2008, de 14 de mao de 2009; y, concretamente, cumpliendo con las especificaciones indicadas en el capítulo 4, artículo 30, apartado 3 de dicho reglamento, se muestra a continuación el resumen de la tesis.

Desde principios de los años 70 la industria de los semiconductores ha seguido el camino marcado por la "ley de Moore" y el número de transistores por procesador se ha ido duplicando de forma continua aproximadamente cada dos años. Esto ha permitido la aparición de dispositivos electrónicos con mayores velocidades de operación, mayor capacidad de procesado y menor coste de fabricación. Sin embargo en los últimos años ha aumentado la importancia de los sistemas que además de procesar información también son capaces de captarla y transmitirla, en lo que se conoce como "More-than-Moore".

Estos avances permiten vislubrar un futuro en el que el llamado internet-de-las-cosas tiene cada vez más importancia. Este concepto define la interconexión a través de internet de dispositivos electrónicos integrados en objetos de uso diario. Estos dispositivos tendrían la capacidad de captar indormación de su entorno, procesarla y comunicarse entre ellos para,

así mejorar su funcionamiento.

Además de esto, dos de los sectores relacionados con la electrónica con mayor potencial de crecimiento que existen ahora mismo son el de los sistemas avanzados de asistencia a la conducción (ADAS por sus siglas en inglés) y el de la realidad virtual/realidad aumentada. Para el primero de ellos se estima que alcanzará los 10 mil millones de dolares de beneficios en todo el mundo para 2020 y para el segundo esta estimación supera los 100 mil millones. A esto hay que añadir el gran interés que están despertando en la actualidad los vehículos aéreos no tripulados (UAVs por sus siglas en inglés), también llamados drones. En todos los casos citados hasta ahora la capatación de información, en particular inforamcion 3D, sobre el entorno en el que se encuentran es fundamental.

Para captar la información 3D del entorno existen diferentes tecnologías todas ellas basadas en el uso de ondas, ya sea luz, microondas o ultrasonidos. De todas estas opciones las ópticas son las que tienen mayor potencial para obtener esta información de manera precisa, rápida y en dispositivos de tamaño compacto.

En general se pueden usar dos técnicas distintas para el obtener la información 3D de un entorno con métodos ópticos: por triangulación o por Tiempo de Vuelo (ToF por sus siglas en inglés). El primero usa dos o mas perspectivas para determinar las distancias del sensor a los objetos de su entorno. Los sensores ToF miden el tiempo que tarda una señal luminosa en ir y volver para calcular estas distancias.

En el caso de sistemas que usan triangulación existen dos técnicas diferentes para hacerlo. La primera usa al menos dos cámaras en dos posiciones diferentes para captar la escena desde distintas perspectivas. Después, cada píxel de una de las cámaras se relaciona con el píxel de la otra cámara que está captando el mismo punto de la escena y la distancia hasta ese punto es calculada en base a la posición relativa de estos píxeles. El problema de esta técnica es que muy exigente en términos de potencia de computación porque para cada píxel de una cámara es necesario encontrar el equivalente en la otra. Además, el proceso puede fallar si la escena tiene poca información visual o si ésta es muy ambigua. La otra técnica que se puede utilizar

para calcular la información 3D de una escena mediante triangulación se basa en sustituir una de las cámaras por un sistema de iluminación. Si este sistema proyecta un patrón de luz conocido la técnica se denomina "de luz estructurada". Esta técnica tiene la ventaja de que se evita el proceso de correlación entre píxeles pero, en general, consigue poca resolución. Otra forma es utilizar como sistema de iluminación un láser e ir moviéndolo por la escena para escanearla. Sin embargo, las partes mecánicas extra que esto conlleva complican el sistema e incrementan su precio.

En contraste con esto, los sensores de tiempo de vuelo tienen el potencial para obtener la información 3D de la escena completa de forma rápida y sin necesidad de partes móviles o una gran potencia de computación. La luz que usan estos sensores es infrarroja de forma que no moleste a las personas moviéndose por dicho entorno y, normalmente, se utilizan láseres o diodos LED para generarla. El sistema emite señales luminosas que son reflejadas por los objetos de la escena y enfocadas en el sensor de tiempo de vuelo por un sistema de lentes. Cada píxel del sensor mide el tiempo que tardan dichas señales en llegar y, como la velocidad de la luz es una constante conocida, calculan la distancia desde la que se reflejan.

Sin embargo, los sensores de tiempo de vuelo tienen sus propias desventajas. Las más importantes están relacionadas los requisitos que tienen en términos de velocidad, ruido y bajos niveles de señal que tienen que medir. La razón de esto es que la potencia luminosa máxima que pueden emitir está restringida para evitar lesiones oculares. Por esta razón todos los sensores de tiempo de vuelo accumulan un gran número de medidas sobre las señal emitida para calcular la información de la distancia. Otro problema típico de estos sensores es que captan no sólo la luz que ellos mismos emiten sino también toda la demás luz que hay en el entorno, denominada luz de fondo. Esta luz de fondo degrada la calidad de las medidas de los sensores de tiempo de vuelo hasta el punto de que, si es muy alta como, por ejemplo en exteriores, puede que las medidas no sean posibles.

Las técnicas usadas por los sensores de tiempo de vuelo puede clasificarse en directas e indirectas. Las primeras miden el tiempo que tardan las señales, que generalmente son pul-

sos de luz, en ir y volver directamente. Los píxeles de estos sensores tienen relojes de alta precisión que se inician con la emisión de la señal y se paran cuando la señal es captada. Como necesitan mucha precisión en la medida del tiempo de llegada de la señal suelen usar como sensores pfotodiodos de efecto avalancha (SPAD por sus siglas en inglés). Los sensores que usan técnicas de tiempo de vuelo indirectas extrapolan la información de tiempo de vuelo de otras medidas. Estas medidas, generalmente, son integraciones de la luz captada sincronizadas con la emisión de la señal. El trabajo de esta tesis está centrado en técnicas de tiempo de vuelo indirectas.

El capítulo 1 da una idea general sobre los sensores de tiempo de vuelo resume el estado del arte actual respecto a ellos. La publicaciones de tiempo de vuelo que se detallan en este capítulo se clasifican en dos tipos diferentes dependiendo de la forma en la que solucionan la necesidad de realizar medidas a muy alta velocidad. Algunas de ellas utilizan tecnologías CMOS no estándar o modifican alguno de las etapas de fabricación en dichas tecnologías. Otras, las que ulizan tecnologías CMOS de fabricación estándar, necesitan circuitería extra dentro del pixel para conseguir la suficiente velocidad de respuesta. Las primersa tienen la ventaja de un menor tamaño de píxel, lo que les permite obtener una mayor resolución. Las segundas se benefician del hecho de que las tecnologías estandar son mucho más baratas.

En el capítulo 2 se describen las distintas técnicas indirectas de tiempo de vuelo. Éstas se pueden dividir en moduladas o pulsadas. Las primeras utilizan señales luminosas periodicas, generalmente de tipo sinusoidal. Las segundas utilizan luz pulsada com señal luminosa. Dentro de las técnicas de tiempo de vuelo de luz pulsada existen diversos métodos para obtener la información de la distancia. Estos métodos se diferencian, fundamentalmente, la sincronización entre la emisión de los pulsos de luz y las integración de la luz recibida que realizan.

En este capítulo, además, se comparan entre sí las técnicas presentadas. Esta comparación se hace en términos del efecto del ruido en la medida de la distancia. En particular, el ruido de disparo (shot noise en inglés) y el ruido térmico en los condensadores de almacenamiento. El

primero de ellos surge de la naturaleza discreta de los fotones, que hace que el flujo de ellos, la intensidad luminosa, no sea constante sino que varíe de un instante a otro. Dado que este ruido es intrínseco a la señal luminosa y la luz de fondo está presente en todos los sensores de tiempo de vuelo, independientemente de la topología usada para implementarlos. Esta es la razón por la que la comparación de técnicas de tiempo de vuelo indirectas se haga en términos de su efecto sobre la medida de la distancia. El ruido térmico en las capacidades de almacenamiento va a limitar el tamaño maximo de dichas capacidades. Como se demuestra en este capítulo, aumentar la capacidad de almacenamiento aumenta también el efecto de este ruido en la medida. Sin embargo, reducir mucho su valor puede crear situaciones en las que el píxel se satura por exceso de carga integrada y la información de la distancia se pierde. Un forma de conciliar estos dos efectos es utilizar topologías que, primero, eliminen el efecto de la luz de fondo antes de integrar la señal luminosa. Y segundo, implementen la técnica del número adaptativo de accumulaciones. En esta técnica, el número de veces que la señal luminosa es integrada es controlado de manera individual para cada píxel. De esta forma si un píxel está próximo a saturar deja de integrar la señal, mientras que el resto de ellos pueden continuar haciéndolo. El capítulo finaliza con una comparación numérica entre las distintas técnicas de tiempo de vuelo, para seleccionar la optima para nuestro diseño.

En el capítulo 3 se estudia la posibilidad de fabricar un sensor de tiempo de vuelo en tecnología CMOS estándar que realice la integraciones a nivel de dispositivo. Como ya se ha mecionado, estas tecnologías no disponen de foto-sensores con esta capacidad. Para su implementación sería necesario violar algunas reglas de diseño. Dados los riesgos que esto implica se realizó un estudio a nivel de dispositivo con el software comercial ATLAS de Silvaco. En particular el foto-sensor estudiado fue el "pinned" con puertas de transmisión para controlar las integraciones y difusiones flotantes para el almacenamiento de la carga. Este estudio se centró en tres parámetros distintos: la corriente oscura del dispositivo, el effecto del transistor de reset en la medida y la velocidad de transmisión de cargas. Las reglas de diseño que ignoran para la febricación de este dispositivo son geométricas, ya que los per-

files de dopado no se pueden modificar por usuarios externos a la fábrica. Las partes del mismo que se ven afectadas por estas reglas geométricas están en zona de alta generación de corriente oscura, con lo que se ha estudiado el comportamiento de dicha corriente con respecto a las modificaciones el el dispositivo propuestas. El transistor de reset afecta a la medida introduciendo ruido en las difusiones flotantes y reduciendo el rango dinámico de las mismas. El alcance de estos efectos también se estudió en este captítulo. Por último, el tercer parámetro estudiado, es la velocidad de transmisión de cargas del dispositivo. Estas simulaciones muestran que, sin un control sobre los perfiles de dopado, el dispositivo fabricado no sería lo suficientemente rápido en esta transmisión como para trabajar a la velocidad exigida por los sensores de tiempo de vuelo.

Descartada la opción de realizar un sensor de tiempo de vuelo que realice las integraciones a nivel de dispositivo se optó por diseñar un píxel con circuitería extra para aumentar su velocidad. El diseño de dicho píxel, en tecnología CMOS estandar de 0.18 μm, está recogido en el capítulo 4. El foto-diodo utilizado en este píxel es propio de la tecnología utilizada y está formado por un pozo N sobre sustrato P. Además, la técnica de tiempo de vuelo que selecionada utiliza pulsos de luz como señal luminosa. Aunque la anchura de dichos pulsos puede modificarse de manera externa, en el diseño de nuestro píxel siempre se asumieron pulsos de luz de 50 ns. Para aumentar la potencia luminosa de dichos pulsos sin aumentar la potencia media de luz emitida, y por lo tanto cumplir con las regulaciones sobre seguridad ocular, estos pulsos se emiten cada 50 μs.

El píxel amplifica la corriente generada por la señal luminosa antes de integrarla en las capacidades de almacenamiento. Debido a la baja potencia de dicha señal y las altas velocidades a las que se deben realizar las integraciones, la amplificación de la señal no es posible en modo corriente. Por esta razón, la señal es, primero convertida a voltaje por un amplificador a transimpedacia, es amplificada, y, después, convertida otra vez en corriente para su integración. En la etapa en la que la señal de voltaje es amplificada su valor de corriente continua es fijado a un valor concreto seleccionable desde el exterior del píxel. Dado que la

corriente continua de esta señal viene determinada por la luz de fondo captada por el sensor esto es equivalente a eliminar dicha luz de fondo de la señal que se va a integrar. Las simulaciones muestran que esto permite a nuestro píxel trabajar bajo niveles luminosos de hasta 20 kluxes. Despues de la integración de cada pulso de luz el píxel compara la señal acumulada con una tensión externa, para saber si las capacidades de almacenamiento están cerca de saturar. Si ese es el caso el píxel deja de integrar pulsos evitando así la pérdida de la información de la distancia. El píxel diseñado ucupa un área de 62×62 μm^2 con un foto-sensor de 50×50 μm^2.

Un array de 52×63 de dichos píxeles fue fabricado. Además de este array el chip incluye toda la circuitería extra necesaria para su funcionamiento. En primer lugar un banco de memorias digitales para almacenar la información digitalizada de cada pixel antes de que ésta pueda ser extraída fuera del chip. Además de esto también incluye un selector de filas y un selector de columnas para controlar el proceso de digitalización y extracción de la información del chip. Otro circuito implementado en el chip es un contador digital utilizado como parte del proceso de digitalización. Finalmente, también se diseño dentro del chip un bloque de control que se ocupa del funcionamiento completo del array. En el capítulo 5 se describen con detalle estos circuitos.

El capítulo también muestra el montaje experimental utilizado para testear el chip. Este montaje incluye, en primer lugar, la placa de cirucito impreso (PCB por sus siglas en inglés) en donde va montado el chip. Esta place tiene, además toda la circuitería necesaria para generar las tensiones de alimentación y de referencia del chip. También, dentro del montaje experimental, fue necesario el diseño de otra PCB con el módulo de iluminación, esto es, el sistema que genera las señales luminosas que serán después recibidas por el chip. Esta placa contiene tres láseres infrarrojos con la circuitería necesaria para su control y alimentados por un regulador de voltaje. Controlando la tensión de alimentación se puede controlar la potencia luminosa emitida. Otros componentes necesarios para el testeo del chip fueron la lente y su marco para enfocala sobre el chip. Éste último fue diseñado e impreso en 3D. Finalmente

el control sobre todos los componentes se ejecute utilizando una FPGA que, además lee los datos obtenidos y calcula a partir de ellos la información tridimensional de la escena.

Este capítulo también incluye las medidas experimentales realizadas sobre el chip. En primer lugar muestra un error en el diseño del chip con respecto al reseteo de las capacidades de almacenamiento. Dicho error evita que todas las capacidades se reseteen a un valor conocido y, en lugar de ello, hace que cada una se tenga su propio valor, cambiando éste de fotograma a fotograma y de píxel a píxel. Para corregir este error se propone digitalizar el valor de reset de cada píxel antes de iniciar las integraciones de los pulsos de luz. El efecto que esto tendría sobre la medida sería el de reducir el número de fotogramas por segundo del sistema. A mayores de esto el funcionamiento del chip no concuerda con el mostrado por simulaciones. El valor de tensión final en las capacidades de almacenamiento de cada píxel tiende a converger a un valor fijo, independiente de el número de acumulaciones realizado, de la potencia luminosa de los pulsos de luz o, incluso, de la logitud de dichos pulsos. Después de exahustivas medidas para descartar cualquier otro fenómeno se ha concluído que la razón de este fallo está en el solapamiento de cuatro señales de control durante la integración de los pulsos. Dichas señales son críticas para el funcionamiento de nuestro sensor de tiempo de vuelo y, en caso de solaparse, se produciría pérdida de carga en las capacidades de almacenamiento llegando a un estado estable en pocos pulsos.

El capítulo final de este trabajo resume todas las conclusiones extraídas de la investigación realizada y comenta la dirección que se tomará en el futuro para continuar con ella.

Introduction

Several methods exist to capture the 3D information of an entire scene. The greatest potential to achieve good distance resolution without expensive set-ups is achived by the ones that use optical based techniques and, among them, Time-of-Flight sensors provide good accuracy, fast response and a compact measuring system simultaneously. These sensors extract the distance information by measuring the time a light signal needs to travel back and forth the target. This work introduces a Time-of-Flight pixel design in standard CMOS technology with improved robustness to the background light.

Contributions

The primary contributions of this dissertation are:

- A study of the performance of the different indirect Time-of-Flight techniques in terms of the effect of the shot and thermal noise in the distance calculation.

  This contribution can be found in the following publication:

  – **Distance Measurement Error in Time-of-Flight Sensors Due to Shot Noise.** Julio Illade-Quinteiro, Víctor Manuel Brea, Paula López, Diego Cabello and Ginés Doménech-Asensi in *Sensors Journal*.

- A study of the possibility of performing the demodulation of the Time-of-Flight signal at device level in standard CMOS technologies.

The publications where this contribution can be found are listed below.

– **Comparison of Photosensing Structures in CMOS Standard Technology for Time-of-Flight Sensors.** Julio Illade-Quinteiro, Víctor Manuel Brea, Paula López, Diego Cabello and Ginés Doménech-Asensi in *28th Intenational Conference on the Design of Circuits and Integrated Systems (DCIS 2013)*.

– **Dark current in standard CMOS pinned photodiodes for Time-of-Flight sensors** Julio Illade-Quinteiro, Víctor Manuel Brea, Paula López, Bea Blanco-Filguiera, Diego Cabello and Ginés Doménech-Asensi in *2014 IEEE Workshop On Microelectronics And Electron Devices (WMED 2014)*.

– **Custom design of pinned photodiodes in standard CMOS technologies for Time-of-Flight sensors** Julio Illade-Quinteiro, Víctor Manuel Brea, Paula López, Diego Cabello and Ginés Doménech-Asensi in *14th International Workshop on Cellular Nanoscale Networks and their Applications (CNNA 2014)*.

– **Dark Current Optimization of 4-Transistor Pixel Topologies in Standard CMOS Technologies for Time-of-Flight Sensors** Julio Illade-Quinteiro, Víctor Manuel Brea, Paula López and Diego Cabello in *IEEE International Symposium on Circuits and Systems (ISCAS 2015)*.

– **Four-Transistor Pinned Photodiodes in Standard CMOS Technologies for Time-of-Flight Sensors** Julio Illade-Quinteiro, Víctor Manuel Brea, Paula López, Diego Cabello and Ginés Doménech-Asensi in *Semiconductor Science and Technology*.

- A ToF pixel in standard CMOS technology design with in-pixel background suppression and adaptive number of accumulations.

This contribution can be found in the following publication:

– **Time-of-flight chip in standard CMOS technology with in-pixel adaptive number of accumulations.** Julio Illade-Quinteiro, Víctor Manuel Brea, Paula López and Diego Cabello in *IEEE International Symposium on Circuits and Systems (ISCAS 2016)*.

Outline

This thesis is divided in five chapters. Chapter 1 gives a context of the state-of-the-art in indirect ToF sensors. Chapter 2 explains in detail the Time-of-Flight techniques used by these sensors. A comparison between them in terms of the error in the distance measurement introduced by the shot and thermal noise is also made in this chapter. The possibility of a device level demodulation pixel in standard CMOS technologies is explored in Chapter 3. In Chapter 4 a detailed description of the designed pixel together with circuit level simulations to check its viability is presented. Finally, the experimental results of the fabricated device, together with the set-up implemented to obtain them are presented in Chapter 5.

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Chapter 1

Background and Related Work

Contactless range measurement sensors are of great interest in areas such as safety, robotics, virtual reality or automotive. Among all the methods available optical based are the ones with greater potential to provide good accuracy, fast response and a compact measuring set-up simultaneously. Two different techniques are usually employed in these sensors: triangulation and Time-of-Flight (ToF). The first one uses multiple points of view to determine the distance to a target. ToF extracts the distance information by measuring the time a light signal needs to travel back and forth the target.

The acquisition of the distance information for an entire frame can be done in two different ways for a triangulation-based system. The first one is to use two or more cameras in two different positions to capture the scene from different points of view. After that, each pixel of one of the cameras is correlated with the pixel of the other camera acquiring the same point of the scene and the distance to that point is calculated based on the relative position of these pixels. This process is computationally very expensive because, for each pixel of one of the cameras the corresponding one from the other camera must be found. In addition to this, if the scene has low level or ambiguous features, the distance calculation can fail. The

second way to proceed in a triangulation-based system is by substituting one of the cameras with a light emitter. In this case, if the light emitter is a projector illuminating the scene with a known light pattern it is called structured light technique. This technique has the advantage of avoiding the pixel correlation problem but in general the spatial resolution achieved is low. Another way is to use a laser and move it through the entire scene to scan it, but the mechanical parts involved increase the complexity and cost of the system.

In contrast to this, ToF sensors have the potential of providing the distance information of an entire scene at a fast frame rate without the need of neither moving parts nor image matching algorithms [1]. However, ToF sensors have disadvantages of their own. The most problematic are the ones concerning their design demands as they have severe requirements in terms of speed, noise and minimum measurable levels for the pixels used in the sensor [2]. The reason for this comes from the fact that the power of the emitted light signal is limited by eye safety regulations [3]. In addition to this, the light not related to the emitted signal present in the scene, called background light, is also acquired by the ToF sensors and it degrades the distance measurement. If this background light is too high, for example in outdoor scenarios, the deterioration of the measurement can be so bad that the distance determination is not possible at all.

It is worth mentioning that the frequency of the light signal used is going to affect the accuracy of the ToF measurement and the maximum measurable distance by the sensor. Increasing this frequency improves the accuracy but reduces the measurable range. In [4] and [5] methods to improve the ToF measurement accuracy by increasing the frequency of the light signal used without diminishing the maximum distance range are presented.

ToF systems use a light source, usually a laser or LED, to illuminate the scene with infrared light, so the operation is unobtrusive to the people around it. This light signal is reflected by the objects on the scene and a set of lenses focus it in an array of ToF pixels. Each pixel measures the time difference between the emission and the reception of the signal, called Time-of-Flight, T_{oF}. Since the speed of light is a known constant, the distance to the

target can be easily calculated from this.

ToF methods can be divided between direct and indirect. The first ones measure the T_{oF} directly and the light signal they use are square pulses. Their pixels have a highly accurate counter that is started synchronized with the emission of the pulse and stops with its arrival. Because of their need of high time-of-arrival resolution almost all the ToF pixels employ single-photon avalanche diodes (SPAD) as sensors [2]. On the other hand, indirect ToF methods extrapolate the T_{oF} parameter from other measurements. These measurements are usually integrations of the light being received synchronized with the signal emission. This work is centered on indirect ToF methods and an extensive explanation of how they work will be given in Chapter 2.

According to the type of the light signal, indirect ToF methods can be classified in modulated or pulsed ToF. The first ones use continuous wave signals, usually sinusoidal ones, while the second ones use light pulses. Different ToF sensors have been reported in the literature both using modulated and pulsed techniques.

Regardless of the ToF technique, all the sensors must address the need of fast integration measurements. This can be achieved by two different means, either these integrations are performed at device level, or extra circuitry is added to the pixels. In the first case standard CMOS technologies can not be used or expensive modifications to them must be done. However, in the second case the extra circuitry increases the pixel size and reduces its fill-factor.

The first examples of ToF pixels designed in non-standard technologies can be found in [6], [7] and [8]. The sensors here presented were fabricated in mixed CCD/CMOS technology. The signal is sensed by a photogate and several transmission gates attached to it in a CCD style will drive the generated current to different regions for their integration. In [9] extra circuitry to subtract the component of the background light from the integrated signal is proposed for these pixels.

In [10] the sensor is also a photogate and two transmission gates are added to drive the generated current to the integration nodes. However, in this case the fabrication technology

is a 0.35 μm standard CMOS one. Since the sensors fabricated in this technology are not fast enough an extra buried N-layer was added to the process.

Other means of improving the speed of the sensor were presented in the literature. For example, in [11] the doping profile of the sensor is modified to create a lateral electric field inside. In other implementations the lateral electric field is achieved by adjusting the voltage in several points around the photo sensor. Such is the case of [12], [13] and [14] were one, two and six transmission gates, respectively, are situated around a pinned photodiode. By modifying the voltage in these gates the generated charges are driven to the current nodes to be integrated. Other example can be seen in [15] where also a pinned photodiode is used as photosensor, but instead of transmission gates polysilicon extended gates are used to direct the photocurrent.

In [4] extra fabrication layers are also added. In this case two photogates are used as photosensors, so one of them can be read while the other is integrating the signal and, thus, the speed is improved. Although the device is fabricated in 0.13 μm standard CMOS technology the p^+ layer between the photogates was modified to increase the isolation between them. In this pixel extra circuitry is added to subtract the background light component from the integrated signal and thus, improving the pixels robustness in high background ambients.

The most straightforward approach to increase the sensor performance is to design the ToF pixel in CIS technology and use a pinned photodiode with several transmission gates as photosensor. This is done in [16], [17], [18] and [19]. The pixels shown in these articles have the extra advantage of also performing conventional image acquisition on the same chip. The first three ones have photosensors that can alternate between the conventional and the ToF measurement while the last one mixes ToF pixels and conventional ones in the same array. The topology proposed in these articles is improved in [20], [21] and [22] by adding extra circuitry to deal with the background light component of the signal.

As explained before, if standard CMOS technology is used, extra circuitry must be added to improve the response of the photosensors. Further explanations of this can be found in [23].

One way to do this is to duplicate the photosensor and the acquisition circuitry so one of them can integrate the signal while the information of the other is being processed. This happens in [24], [25], [26] for a pixel topology very similar to the 3-transistors configuration and in [27] for another similar to the 4-transistors one. Another example of ToF pixel fabricated in standard CMOS technology can be found in [28].

The pixels fabricated in standard CMOS technology until now rely on intermediate storage capacitances to integrate the signal while is being received and then transfer it to a final storage node to accumulate it. The pixel presented in [29] uses a series of switches to drive the photocurrent generated by the light signal to the final storage capacitance directly, without intermediate storage nodes. This idea is improved in [30], [31] and [32] where current mirrors are added to eliminate the background component before the storage.

The objective of this work is to design a pixel in standard CMOS technology with improved robustness to the background light. To fulfill this, techniques like in-pixel background suppression and adaptive number of accumulations are used. Chapter 2 provides a review of the existing indirect ToF techniques and analyze them in terms of noise impact in the measurement. In Chapter 3 the possibility of performing the demodulation of the signal at device level in standard CMOS technologies is explored through simulations. Chapter 4 gives a detailed description of the designed ToF pixel. Finally, Chapter 5 shows the experimental set-up to measure the sensor fabricated and summarizes the experimentally obtained results.

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Chapter 2

Fundamentals of Time-of-Flight Sensors

Optical ToF methods can be classified in direct and indirect [2]. The first ones measure directly the time delay between the emitted and the received light signals. In the indirect ones the time is extrapolated from other measurements. This work is centered on indirect ToF methods. In this chapter the different techniques used to perform indirect ToF are described.

According to the light signal, indirect ToF methods can be divided in modulated, if the signal is a continuous wave, or pulsed ToF, if light pulses are used. Fig. 2.1 and Fig. 2.2 show the operation modes for modulated and pulsed ToF sensors, respectively. As it can be seen, besides the phase, ϕ, or time delay, T_{oF}, two more parameters are unknown in the incoming signal, namely, its amplitude, A, and the background light of the scene, B. This is the reason why at least three measurements in a cycle or pulse are needed to calculate a distance. In indirect ToF sensors, these measurements are integrations of the photocharges generated by the sensor in response to the incident light for different time intervals.

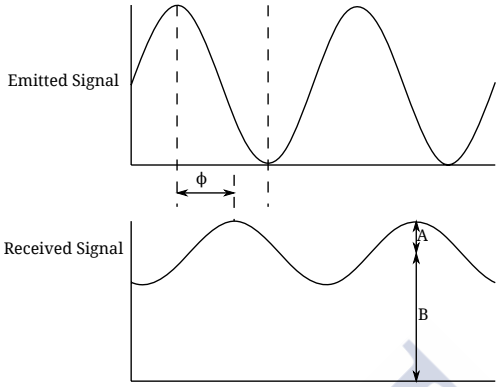

Figure 2.1: Light emission in modulated ToF sensors.

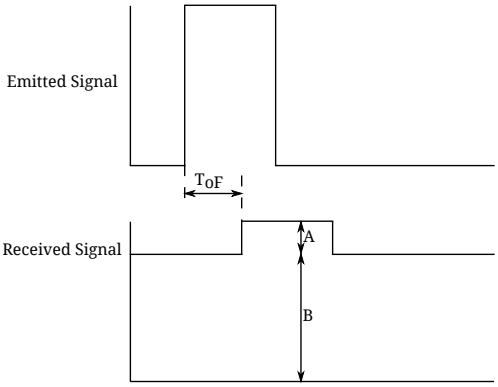

Figure 2.2: Light emission in pulsed ToF sensors.

In Section 2.1 the working principle of each ToF technique will be explained. Regardless of the technique, ToF measurements are severrily affected by from noise effects, with shot and thermal noise as the most relevant ones. The effect of this noise in the distance calculation is described in Section 2.2. The selection of the ToF technique to be implemented in this work will be based on the effect of noise. Section 2.3 provides the theoretical background needed to calculate realistic values for the parameters used in the noise equations. In Section 2.4 a comparison of different techniques is performed and, finally, in Section 2.5 the selected topology is detailed. Part of the material presented in this chapter was published in [33].

2.1 Indirect ToF Techniques

2.1.1 Modulated Time-of-Flight

In the modulated ToF operation the emitted signal is a continuous-wave signal modulated in time, usually a sinusoid. The phase difference between the emitted and the received light signals, ϕ, depends on the distance traveled by the light, from the sensor to the object and

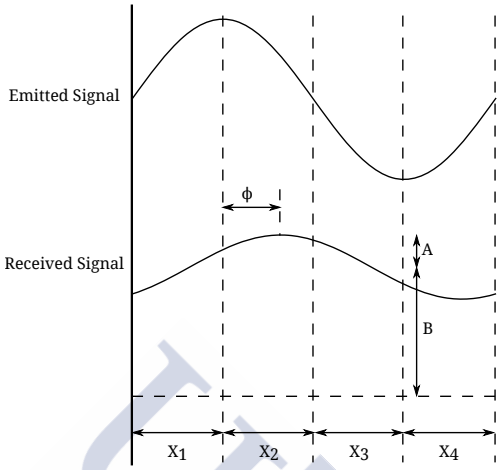

Figure 2.3: Measurements to perform indirect ToF with modulated light signal.

back again. The separation between the sensor and the object can then be calculated as:

$$L = \frac{c}{2}\frac{\phi}{\omega} = \frac{c}{2}\frac{\phi\tilde{T}}{2\pi} \tag{2.1}$$

where c is the speed of light, ω the angular frequency and $\tilde{T}$ the period of the signal. Fig. 2.3 shows the technique to measure the phase difference. In this figure A is the amplitude in number of photons per second reaching the photosensor due to the signal, and B the photons per second reaching the photosensor because of the background. Each x_i measurement is the integration of these photons in the time interval X_i. Four measurements are performed, instead of the minimum three, to simplify the calculation. After repeating these integrations N_{acc} times, the number of photons integrated in each x_i measurement is:

$$x_1 = \frac{N_{acc}B\tilde{T}}{4} + \frac{\sqrt{2}A\tilde{T}N_{acc}}{2\pi}sin(\phi) \tag{2.2a}$$

$$x_2 = \frac{N_{acc}B\tilde{T}}{4} + \frac{\sqrt{2}A\tilde{T}N_{acc}}{2\pi}cos(\phi) \tag{2.2b}$$

$$x_3 = \frac{N_{acc}B\tilde{T}}{4} - \frac{\sqrt{2}A\tilde{T}N_{acc}}{2\pi}sin(\phi) \tag{2.2c}$$

$$x_4 = \frac{N_{acc}B\tilde{T}}{4} - \frac{\sqrt{2}A\tilde{T}N_{acc}}{2\pi}cos(\phi) \tag{2.2d}$$

$$\tag{2.2e}$$

from which, the distance can be obtained as:

$$L_{Mod} = \frac{c}{2}\frac{\tilde{T}}{2\pi}\text{atan}\frac{x_3 - x_1}{x_4 - x_2} \tag{2.3}$$

2.1.2 Pulsed Time-of-Flight

Pulsed ToF employs square wave signals. The time delay between the emitted and received light pulses, T_{oF}, depends on the distance traveled by the light, that can be calculated as:

$$L = \frac{c}{2}T_{oF} \tag{2.4}$$

Two measurement techniques exist for the determination of the distance using pulsed ToF, Phase Shift Determination (PSD), and Multiple Double Short Time Integration (MDSI). As in the case of modulated ToF, A and B are the number of photons per second hitting the photosensor because of the signal and the background, respectively.

Phase Shift Determination

In the PSD case all the measurements have a duration equal to that of the emitted pulse, T_p. From Fig. 2.4 and Fig. 2.5, it can be seen that the PSD technique can be realized in two different ways, with either three, Fig. 2.4, or four measurements, Fig. 2.5. In both cases, the first measurement interval, X_1, is synchronized with the emitted pulse, while the second, X_2,

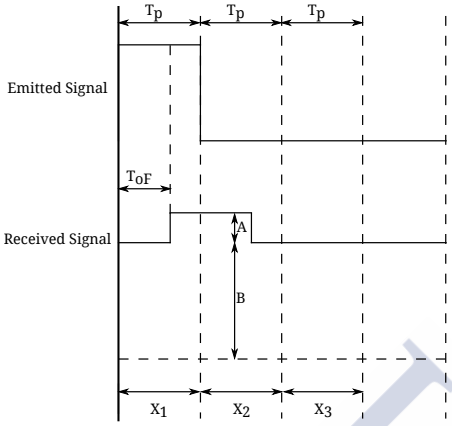

Figure 2.4: Measurements for pulsed PSD-1B ToF.

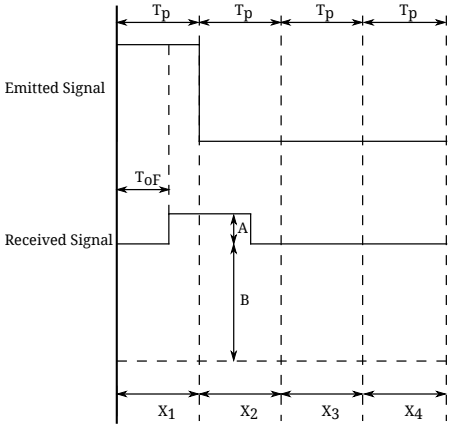

Figure 2.5: Measurements for pulsed PSD-2B ToF.

comes right after it. The third and fourth measurements are carried out without light signal in order to sense the background light. We will refer to the technique depicted in Fig. 2.4 as PSD with one background measurement (PSD-1B) and to the one on Fig. 2.5 as PSD with two background measurements (PSD-2B). For PSD-1B it is easy to show that the number of photons in each measurement interval, after N_{acc} accumulations, is:

$$x_1 = N_{acc}BT_p + N_{acc}A(T_p - T_{oF}) \tag{2.5a}$$

$$x_2 = N_{acc}BT_p + N_{acc}AT_{oF} \tag{2.5b}$$

$$x_3 = N_{acc}BT_p \tag{2.5c}$$

From (2.5), T_{oF} can be calculated and the distance will be:

$$L_{PSD-1B} = \frac{c}{2}T_p \frac{x_2 - x_3}{(x_1 - x_3) + (x_2 - x_3)} \tag{2.6}$$

For the PSD-2B case (2.5a-2.5c) are modified to:

$$x_1 = N_{acc}BT_p + N_{acc}A(T_p - T_{oF}) \tag{2.7a}$$

$$x_2 = N_{acc}BT_p + N_{acc}AT_{oF} \tag{2.7b}$$

$$x_3 = N_{acc}BT_p \tag{2.7c}$$

$$x_4 = N_{acc}BT_p \tag{2.7d}$$

and the distance calculation changes to,

$$L_{PSD-2B} = \frac{c}{2}T_p \frac{x_2 - x_4}{(x_1 - x_3) + (x_2 - x_4)} \tag{2.8}$$

Multiple Double Short Time Integration

In the MDSI technique [34], the first measurement is also synchronized with the emitted pulse and has the same duration, while for the second its duration is doubled in order to ensure that the entire received pulse is measured during X_2. As in PSD, the third and fourth measurements are performed without light signal to sense the background. The time diagram for these measurements are shown in Fig. 2.6 for MDSI-1B, and in Fig. 2.7 for MDSI-2B.

For MDSI-1B the number of photons at the photosensor, x_i, in each measurement interval X_i, when they are repeated N_{acc} times, can be inferred from Fig. 2.6 as:

$$x_1 = N_{acc}BT_p + N_{acc}A(T_p - T_{oF}) \tag{2.9a}$$

$$x_2 = 2N_{acc}BT_p + N_{acc}AT_p \tag{2.9b}$$

$$x_3 = N_{acc}BT_p \tag{2.9c}$$

Using (2.9a-2.9c) and (2.4), the distance can be calculated as:

$$L_{MDSI-1B} = \frac{c}{2}T_p \frac{x_2 - x_1 - x_3}{x_2 - 2x_3} \tag{2.10}$$

For the MDSI-2B technique (2.9a)-(2.9c) are modified to take into account the extra background measurement:

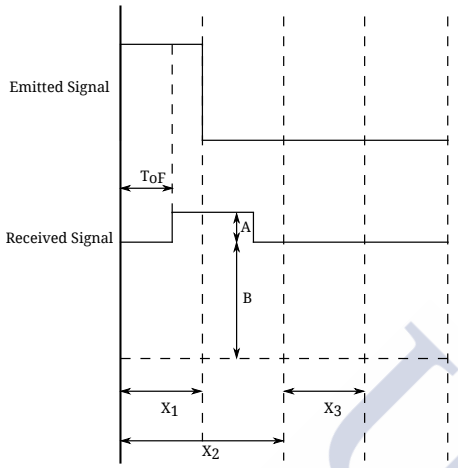

Figure 2.6: Measurements for pulsed MDSI-1B ToF.

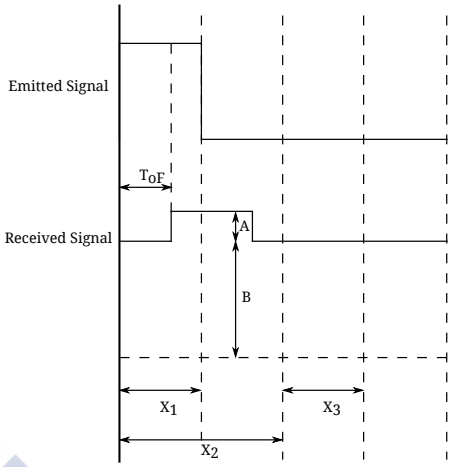

Figure 2.7: Measurements for pulsed MDSI-2B ToF.

$$x_1 = N_{acc}BT_p + N_{acc}A(T_p - T_{oF}) \tag{2.11a}$$

$$x_2 = 2N_{acc}BT_p + N_{acc}AT_p \tag{2.11b}$$

$$x_3 = N_{acc}BT_p \tag{2.11c}$$

$$x_4 = 2N_{acc}BT_p \tag{2.11d}$$

In this case, the distance becomes:

$$L_{MDSI-2B} = \frac{c}{2}T_p\frac{(x_2 - x_4) - (x_1 - x_3)}{x_2 - x_4} \tag{2.12}$$

2.2 Noise Related Distance Error

In the last section, the different indirect ToF techniques were shown. Each one of these techniques needs the integration of the photons reaching the sensor in three or four X_i time windows. These integrations will suffer from noise, being the most relevant ones the shot

and the thermal noise. This section models these noises in the sensor and their effect on the distance calculation.

2.2.1 Shot Noise

Because of the discrete nature of photons, the measurements x_i previously described suffer from shot noise [35]. In this case, each one of the measurements comes from the integration of the flow of photons reaching the sensor. These integrations follow a Poisson probability distribution, so its variance is:

$$(\delta x_i)^2 = x_i \tag{2.13}$$

To understand how this noise affects the distance measurement, error propagation can be applied as:

$$\Delta L = \sqrt{\sum_i \left(\frac{\partial L}{\partial x_i}\right)^2 (\delta x_i)^2} \tag{2.14}$$

In the modulated ToF case, applying (2.14) to (2.3) yields [8]:

$$\Delta L_{mod}^{SN} = \frac{c}{2} \frac{\sqrt{TB}}{2\sqrt{8}A\sqrt{N_{acc}}} \tag{2.15}$$

For PSD techniques, using (2.6) and (2.8) gives:

$$\Delta L_{PSD-1B}^{SN} = \frac{c}{2} \frac{\sqrt{2BT_p^2 - (6B-A)T_{oF}(T_p - T_{oF})}}{A\sqrt{N_{acc}}\sqrt{T_p}} \tag{2.16}$$

$$\Delta L_{PSD-2B}^{SN} = \frac{c}{2} \frac{\sqrt{2BT_p^2 - (4B-A)T_{oF}(T_p - T_{oF})}}{A\sqrt{N_{acc}}\sqrt{T_p}} \tag{2.17}$$

as the uncertainties in the distance measurements. Similarly, for MDSI techniques, their distance error caused by the shot noise are derived from (2.10) and (2.12) as:

$$\Delta L_{MDSI-1B}^{SN} = \frac{c}{2} \frac{\sqrt{(4B+2A)T_p^2 + (6B+A)T_{oF}^2 - (8B+3A)T_pT_{oF}}}{A\sqrt{N_{acc}}\sqrt{T_p}} \tag{2.18}$$

Table 2.1: Distance and its shot noise related error equations for different indirect ToF techniques.

	Distance	Distance error due to shot noise
Modulated	$\frac{c}{2}\frac{T}{2\pi}\text{atan}\frac{x_3-x_1}{x_4-x_2}$	$\frac{c}{2}\frac{\sqrt{TB}}{2\sqrt{8A}\sqrt{N_{acc}}}$
PSD-1B	$\frac{c}{2}T_p\frac{x_2-x_3}{(x_1-x_3)+(x_2-x_3)}$	$\frac{c}{2}\frac{\sqrt{2BT_p^2-(6B-A)T_{oF}(T_p-T_{oF})}}{A\sqrt{N_{acc}}\sqrt{T_p}}$
PSD-2B	$\frac{c}{2}T_p\frac{x_2-x_4}{(x_1-x_3)+(x_2-x_4)}$	$\frac{c}{2}\frac{\sqrt{2BT_p^2-(4B-A)T_{oF}(T_p-T_{oF})}}{A\sqrt{N_{acc}}\sqrt{T_p}}$
MDSI-1B	$\frac{c}{2}T_p\frac{x_2-x_1-x_3}{x_2-2x_3}$	$\frac{c}{2}\frac{\sqrt{(4B+2A)T_p^2+(6B+A)T_{oF}^2-(8B+3A)T_pT_{oF}}}{A\sqrt{N_{acc}}\sqrt{T_p}}$
MDSI-2B	$\frac{c}{2}T_p\frac{(x_2-x_4)-(x_1-x_3)}{x_2-x_4}$	$\frac{c}{2}\frac{\sqrt{(6B+2A)T_p^2+(4B+A)T_{oF}^2-(8B+3A)T_pT_{oF}}}{A\sqrt{N_{acc}}\sqrt{T_p}}$

$$\Delta L_{MDSI-2B}^{SN}=\frac{c}{2}\frac{\sqrt{(6B+2A)T_p^2+(4B+A)T_{oF}^2-(8B+3A)T_pT_{oF}}}{A\sqrt{N_{acc}}\sqrt{T_p}} \tag{2.19}$$

Table 2.1 gathers the distance equations and their shot noise related error for all the ToF techniques studied in this work. As it can be seen, this error is, in all cases, inversely proportional to the square root of N_{acc}. This means that the distance accuracy will improve if more accumulations are performed. Also, the shot noise related error is proportional to B, which means that higher values of background light will worsen the distance calculation.

2.2.2 Thermal Noise

To perform the ToF techniques, the light signal reaching the sensor must be transformed in an electrical one. One or more photosensors inside the pixel convert the received photons in charges, so the flux of photons reaching the sensor is converted in a current. This current is usually accumulated in storage capacitances. Because of their thermal energy, the electrons stored in these capacitances can flow in and out of them. This movement is random and generates a noise in the capacitor called thermal noise [36]. In this section the effect that this thermal noise has on the distance calculation is described.

Since the thermal noise affects the voltage signal accumulated in the storage capacitances, the distance calculation equations of Section 2.1 have to be modified to use these voltages instead of the photons integrated during the corresponding X_i measurement window. After that, the effect of the thermal noise in the distance calculation can be determined.

As it has been said, the photosensor converts the incoming flux of photons in a current. The relation between the number of photons per second, N, and the generated current, I_{ph}, is [37]:

$$I_{ph} = q\ QE\ N \tag{2.20}$$

where q is the electron charge and QE the quantum efficiency of the photosensor. This current integrated during an interval of time T_{integ} generates a voltage difference in the storage capacitor, $C_{storage}$, of:

$$V_{swing} = \frac{I_{ph}\ T_{integ}}{C_{storage}} \tag{2.21}$$

Using this equation the voltage swing generated in each x_i measurement can be calculated as:

$$V_{xi} = \frac{q\ QE}{C_{storage}} x_i \tag{2.22}$$

As it can be seen, V_{xi} is proportional to x_i, which means that, to calculate the distance with any of the ToF techniques described in Section 2.1, V_{xi} can be used instead of x_i. The second column of Table 2.2 shows the distance calculation equation for each technique using V_{xi} instead of x_i.

Any time the signal is updated in the storage capacitances thermal noise is added. The variance of this noise, δV_{xi}, depends on the capacitance value, $C_{storage}$, the temperature, T_{emp} and N_{acc}:

$$(\delta V_{xi})^2 = \frac{N_{acc}\ k\ T_{emp}}{C_{storage}} \tag{2.23}$$

Table 2.2: Distance and its thermal noise related error equations for different indirect ToF techniques.

	Distance	Distance error due to thermal noise
Modulated	$\frac{c}{2}\frac{T}{2\pi}\text{atan}\frac{V_{x3}-V_{x1}}{V_{x4}-V_{x2}}$	$\frac{c}{2}\frac{1}{2q\ QE\ A}\sqrt{\frac{C_{storage}kT_{emp}}{N_{acc}}}$
PSD-1B	$\frac{c}{2}T_p\frac{V_{x2}-V_{x3}}{(V_{x1}-V_{x3})+(V_{x2}-V_{x3})}$	$\frac{c}{2}\frac{\sqrt{T_{oF}^2+\left(T_p-T_{oF}\right)^2+\left(T_p-2T_{oF}\right)^2}}{q\ QE\ A\ T_p}\sqrt{\frac{C_{storage}kT_{emp}}{N_{acc}}}$
PSD-2B	$\frac{c}{2}T_p\frac{V_{x2}-V_{x4}}{(V_{x1}-V_{x3})+(V_{x2}-V_{x4})}$	$\frac{c}{2}\frac{\sqrt{T_{oF}^2+\left(T_p-T_{oF}\right)^2}}{q\ QE\ A\ T_p}\sqrt{\frac{C_{storage}kT_{emp}}{N_{acc}}}$
MDSI-1B	$\frac{c}{2}T_p\frac{V_{x2}-V_{x1}-V_{x3}}{V_{x2}-2V_{x3}}$	$\frac{c}{2}\frac{\sqrt{T_p^2+\left(T_p-T_{oF}\right)^2+\left(T_p-2T_{oF}\right)^2}}{q\ QE\ A\ T_p}\sqrt{\frac{C_{storage}kT_{emp}}{N_{acc}}}$
MDSI-2B	$\frac{c}{2}T_p\frac{(V_{x2}-V_{x4})-(V_{x1}-V_{x3})}{V_{x2}-V_{x4}}$	$\frac{c}{2}\frac{\sqrt{T_p^2+\left(T_p-T_{oF}\right)^2}}{q\ QE\ A\ T_p}\sqrt{\frac{C_{storage}kT_{emp}}{N_{acc}}}$

where k is the Boltzmann constant. Applying error propagation to the distance equations of Table 2.2 the effect of this noise can be calculated. These calculations are shown in Appendix A and the obtained results are shown in the third column of Table 2.2. As it can be seen, the thermal noise related distance error is inversely proportional to A and the square root of N_{acc}. This means that higher power light signals or more cycles or pulses of signal accumulated over time will reduce the thermal noise effect. Also, this distance error is proportional to the square root of $C_{storage}$, so larger storage capacitances increases the error in the distance calculation.

From the results collected in Table 2.2 it may seem that using small storage capacitances will benefit the pixel performance, but there is a maximum value of charge that a capacitance can store, so using small capacitances will increase the risk of saturation. If this happens the distance information is lost for that pixel.

The minimum value of capacitance that ensures that the voltage at $C_{storage}$ will not reach saturation depends on the maximum amount of charge that is accumulated in the x_i integration window, as it can be seen from (2.21). The charge generated during each x_i measurement, Q_{xi}, can be calculated as:

$$Q_{xi} = q\ QE\ x_i \tag{2.24}$$

Table 2.3: Maximum charge accumulated in the storage capacitances for the different ToF techniques.

Measurement Technique	Maximum charge integration
Modulated ToF	$Q_{max}^{Mod} = \frac{q\ QE\ N_{acc} A^{max} \tilde{T}}{\pi}$
PSD-1B	$Q_{max}^{PSD-1B} = q\ QE\ N_{acc}\,(B^{max} + A^{max})\,T_p$
PSD-2B	$Q_{max}^{PSD-2B} = q\ QE\ N_{acc} A^{max} T_p$
MDSI-1B	$Q_{max}^{MDSI-1B} = q\ QE\ N_{acc}\,(2B^{max} + A^{max})\,T_p$
MDSI-2B	$Q_{max}^{MDSI-2B} = q\ QE\ N_{acc} A^{max} T_p$

The expressions for the charges stored after N_{acc} accumulations for each indirect ToF technique are formulated in Appendix B. With these equations the maximum charge that the storage capacitances can accumulate can be calculated. Table 2.3 shows this result for each technique. The calculated value will depend, in addition to the selected technique, on the maximum number of photons per second of the ToF signal, A^{max}, and of the background, B^{max}, and on the selected number of accumulations N_{acc}. Using these equations together with (2.21) the minimum storage capacitance needed in a ToF pixel can be calculated. In Section 2.4 numerical examples will be provided using realistic values for A^{max}, B^{max} and N_{acc}. Table 2.3 shows that for the pulsed ToF techniques with two background measurements (PSD-2B and MDSI-2B) and for the modulated ToF technique the maximum charge integrated during an x_i measurement does not depend on the background light. The reason for this is that, for these techniques, the charges from the x_3 and x_4 measurements are subtracted from the charges from x_1 and x_2, respectively, before the storage, so ideally the charges saved are $x_1 - x_3$ and $x_2 - x_4$ and no background is accumulated. This has the added benefit of using only two storage capacitances, while in the pulsed ToF techniques with one background measurement (PSD-1B and MDSI-1B) three capacitors are needed, one for every x_i integration window.

One important thing to take into account is that the thermal noise is not present in ToF sensors where the demodulation is performed at sensor level using pinned photodiodes, like, for example, in [16, 18]. The reason for this is the voltage drop between the photodiode and the floating diffusions that act as storage capacitances, which does not allow electrons to flow between both structures just by their thermal energy. In Chapter 3 the viability of this type of structures in standard CMOS technology will be studied.

Summarizing, the thermal noise related distance error improves if N_{acc} or A are increased and worsens if $C_{storage}$ is made larger, as it can be seen from the equations gathered in Table 2.2. On the other hand, there is a minimum $C_{storage}$ value that ensures that these capacitances do not saturate and loose distance information. A solution to this trade-off is the adaptive number of accumulations [27]. This technique will be explained in Section 2.4.2 along with some numerical examples of the effect of the thermal noise in the distance calculation.

In this section, the effect of the shot and thermal noise in the distance calculation in ToF sensors was presented. To provide quantitative estimations of these effects from the equations of Table 2.1 and Table 2.2, realistic values A, B and N_{acc} must be provided. In the next section, equations for the estimation of these parameters are presented.

2.3 Signal and Background Estimations

2.3.1 Light Power Considerations

In ToF operation the light signal emitted by the source will reach the sensor after being reflected by the target. In order to calculate the distance error, ΔL, for the different ToF techniques, it is necessary to determine the amplitude in number of photons reaching the photosensor due to the reflected signal, A, and the number of photons due to the background light, B, in terms of the emitted light power source and the ambient illuminance, respectively.

The maximum light power that reaches the target is determined by eye safety regulations [3]. After hitting the target, the light power density reflected by the target can be calculated as,

$$p_d(L) = \frac{\rho\, P_{light}}{4Ltan(\theta_{||}/2)tan(\theta_{\perp}/2)} \tag{2.25}$$

where ρ is the target reflectivity, P_{light} the light source power, L the distance between the source and the target and $\theta_{||}$ and $\theta_{\perp}$ the emitter beam divergences parallel and perpendicular to the ground, respectively. After being reflected by the target this light signal hits the sensor, and the light power at the pixel, $P_{pix}(L)$, can be calculated as [15],

$$P_{pix}(L) = \frac{\tau_{opt} A_{PS} p_d(L)}{4F\#^2} \tag{2.26}$$

where τ_{opt} is the optics transmission efficiency, A_{PS} the area of the photosensor and $F\#$ the F-number of the lenses. After obtaining the light power density at the sensor site from a specific distance, it can be extended to any distance as,

$$P_{pix}(L_2) = P_{pix}(L_1)\left(\frac{L_1}{L_2}\right)^2 \tag{2.27}$$

With (2.26) the value of A can be calculated as:

$$A = \frac{\lambda}{hc} P_{pix}(L) \tag{2.28}$$

where λ is the wavelength of the incident light and h the Planck's constant. Finally, B can be calculated using the light power from typical values of luminance and conversion factors, P_B, see, for example, [37]. Thus,

$$B = \frac{\lambda}{hc} P_B \tag{2.29}$$

2.3.2 Signal Accumulation

As explained, regardless of the ToF technique, signal averaging by means of several accumulations is needed in order to reduce the shot noise of a single distance measurement and,

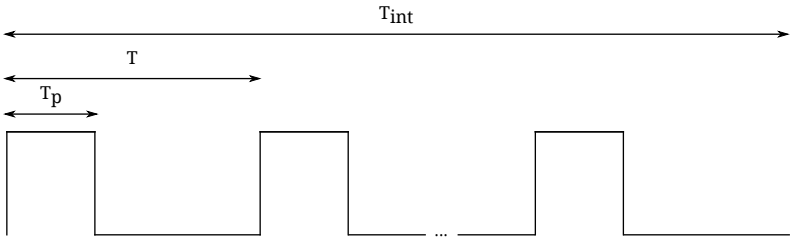

Figure 2.8: Time diagram showing T_p, T and T_{int} for pulsed ToF techniques.

consequently the uncertainty in the distance measurement, ΔL. In this section we will calculate the value of N_{acc} for each ToF technique in a given integration time, T_{int}, defined as the period of time during which the samples x_i are accumulated. To do so, it is necessary to take into account whether or not the studied design needs to reset part of the pixel nodes between x_i measurements. Examples of designs that need this are [27] or [38]. On the other hand, pixels like the ones presented in [39] and [16] can perform all the samples x_i one after the other, without the need of a reset.

To calculate N_{acc} we first define T as the time between two successive light pulses in pulsed ToF techniques. We also define the duty cycle in the pulsed-ToF case as the ratio of the pulse width, T_p, to T. Fig. 2.8 shows the relation between T_p, T and T_{int}. If the reset is necessary, at least two cycles or pulses need to be used to obtain all the x_i measurements. This means that the time for the distance calculation is doubled or N_{acc} reduced to a half. The same problem appears in the MDSI techniques, since x_1 and x_2 are performed simultaneously (see Fig. 2.6 and Fig. 2.7). Table 2.4 summarizes the number of accumulations for every technique. As seen, increasing the integration time can to reduce the shot noise as it increases the number of signal accumulations for a given ToF technique and frequency of the emitted signal.

Table 2.4: Number of accumulations for different ToF techniques.

	Number of accumulations, N_{acc}	
Measurement Technique	No need of reset	Need of reset
Modulated ToF	$\frac{T_{int}}{T}$	$\frac{T_{int}}{2T}$
PSD	$\frac{T_{int}}{T}$	$\frac{T_{int}}{2T}$
MDSI	$\frac{T_{int}}{2T}$	$\frac{T_{int}}{2T}$

2.4 Numerical Examples

In this section numerical examples comparing the different indirect ToF modes of operation are presented. These examples are intended to be as general as possible, but some values must be set. In particular, the wavelength of the light signal is set to $\lambda = 850$ nm. Also, in all cases we used $\tilde{T} = 50$ ns and $T_p = 50$ ns in modulated and pulsed ToF, respectively, which means that the maximum distance measurable by the sensor is 7.5 m ((2.1) and (2.4)). The integration time was set to $T_{int} = 20$ ms, during which the accumulations of x_i are stored in the pixel. This leaves more than 10 ms for A/D conversion and read-out to comply with the time constraint of video rate: 33 frames per second. In addition to this, assuming an NWell over Psubstrate photodiode in standard 0.18 μm CMOS technology, the quantum efficiency of the photosensor was calculated from the experimental data provided in [40]. The area of the photosensor is set to 50×50 μm^2. These assumptions affect the final values, but not the comparison between the different ToF techniques.

Three different ambient light illuminations were studied: a poorly illuminated indoor scenario, with a background light power density of $p_{BIndoorMin} = 6.25 \times 10^{-4}$ W/cm^2, a well illuminated indoor scenario with $p_{BIndoorMax} = 6.25 \times 10^{-2}$ W/cm^2 and outdoor illumination in midsummer with $p_{BMax} = 0.167\times$ W/cm^2. This background comprises light of different

Table 2.5: Maximum emitted power to comply with eye safety regulations for a distance of 25 cm or more.

	Duty Cycle	Light Power (W)
Pulsed	0.1	33
Pulsed	1	9
Pulsed	10	0.87
Modulated	-	0.09

wavelengths but for the calculation of B using (2.29) $\lambda = 630$ nm was used since around this wavelength the silicon has higher sensitivity. The obtained values are: $B_{IndoorMin} = 4.46 \times 10^9$, $B_{IndoorMax} = 4.46 \times 10^{11}$ and $B_{Max} = 1.19 \times 10^{12}$ photons per second.

The maximum light power that can reach the eye without safety glasses depends on several factors [3] such as the width of the emitted pulse, its wavelength or the frequency of the signal. In general, for infrared radiation with the signal frequency that ToF sensors operate, the light power limit is defined by the average power that can reach an unprotected eye. This means that bursts of pulses with low duty cycle will allow to operate at higher instant light power without violating the maximum average light power set by eye safety regulations. Table 2.5 shows the maximum light power allowed for the different situations studied in this chapter. These values were calculated assuming that safety regulations are satisfied for every distance to the sensor greater than 25 cm and setting $\rho = 0.5$, $\theta_{||} = 9°$, $\theta_{\perp} = 25°$, $\tau_{opt} = 1$ and $F\# = 1.7$. The values of these parameters were selected based on the experimental setup designed to test the sensor, that will be described in Chapter 5.

From this, and using (2.25), (2.26) and (2.28), the maximum value of A as a function of the distance between the sensor and the target can be calculated, as seen in Fig. 2.9. This figure shows that in modulated ToF techniques A is severely reduced for longer distances,

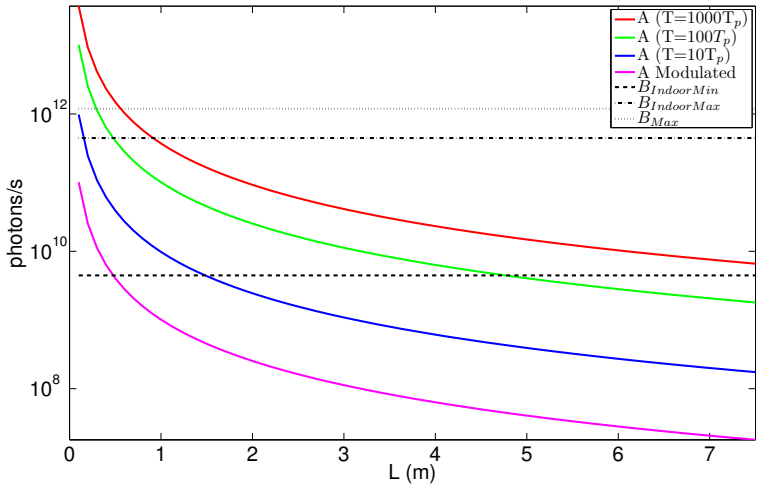

Figure 2.9: *A* value as a function of the distance between the target and the sensor. In the pulsed ToF case, values are shown for three different duty cycles.

which in turn results in higher shot noise. On the other hand, in pulsed ToF the value of *A* depends on the duty cycle selected. Lower duty cycles result in higher *A* due to the fact that by decreasing the duty cycle it is possible to increase the light power of the pulse without increasing the average light power. It should also be noted that in modulated ToF the number of photons reaching the sensor because of the background is bigger than those from the signal in all the cases except for the lowest background situations and, even in that case, only at distances smaller than 0.5 m. In pulsed ToF, the signal power exceeds every background one, only for small duty cycles and distances to the target smaller than 1 m.

2.4.1 Shot Noise Results

Having calculated realistic values for *A* and *B*, the distance error due to shot noise can be obtained. Fig. 2.10 and Fig. 2.11 show this error for all the different ToF techniques for

$B_{IndoorMin}$. Duty cycles of 10% and 0.1% were used for the pulsed ToF techniques, respectively, whereas the period for the modulated ToF was set to $\tilde{T} = 50$ ns. By comparing both figures, the fact that the shot noise in pulsed ToF is reduced with smaller duty cycles is apparent, despite the fact that the number of accumulations is reduced. The reason for this, as explained before, is that, by reducing the duty cycle, higher light power can be used in each pulse, without increasing the average light power and, thus, complying with eye safety regulations. It can also be seen that, because of the reduction of A for greater distances, the shot noise, and thus the accuracy, worsens with the distance. In addition, a comparison between ToF techniques can be performed. First of all, for the same ToF technique, those topologies that do not need to perform a reset operation between consecutive x_i integrations, always present less error due to shot noise than the ones that need it. The reason for this can be inferred from Table 2.4. The number of accumulations in both modulated and PSD ToF for a given integration time, when the reset between x_i is no needed, is twice the number of those used when the reset is required because, in this case, two light pulses per measurement are needed. The MDSI technique always needs two light pulses per measurement. Finally, for the same technique, 1B measurements present lower shot noise than 2B measurements.

There exist four ways of reducing shot noise related distance errors. The first one is to increase the light power of the pulse, however, this will make the sensor violate eye safety regulations for longer distances. The second option is to use larger photosensors, as increasing the photosensors area by a factor of four reduces the shot noise uncertainty by two, but larger photosensors have slower responses and the photosensor area used in these calculations was of 50×50 μm^2, which is already large. The third option is to increase the integration time of the sensor (T_{int}), which increases N_{acc} and hence reduces ΔL by a factor $1/\sqrt{N_{acc}}$. Alternatively, for pulsed ToF, decreasing the duty cycle, and thus increasing A, reduces the distance uncertainty as $\Delta L \propto \sqrt{A}/A$. Finally, the last option is to minimize the background light reaching the pixel, which in practice is usually accomplished placing optical filters in front of the sensor that restrict the incident light to the wavelength of the light source.

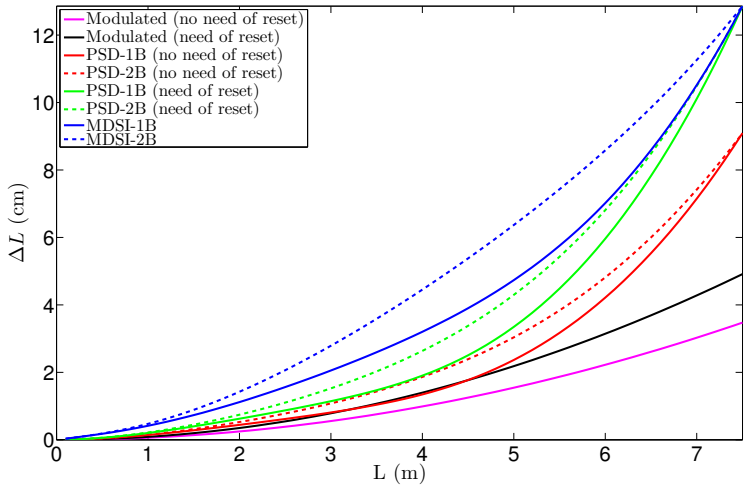

Figure 2.10: Distance error due to shot noise for the different ToF techniques. In pulsed ToF, duty cycle was set to 10%.

The same situation as in Fig. 2.11, but without background light ($B = 0$) is shown in Fig. 2.12. This represents the minimum achievable error of the ToF sensor. In the ideal situation of no background light there is no difference between 1B and 2B measurement techniques. Also, as it can be seen, for most distances, with no background noise, the ToF technique that achieves better distance resolution is the modulated one.

2.4.2 Thermal Noise Results

As explained in Section 2.2.2 there is a trade-off when selecting the storage capacitances value. If a small value is used, there is a risk of voltage saturation at the capacitors when high light power reaches the pixel. If large capacitances are used, the distance error because of the thermal noise will increase. Using the equations from Table 2.3 the minimum capacitances to avoid saturation can be calculated. Assuming that the maximum light power for the back-

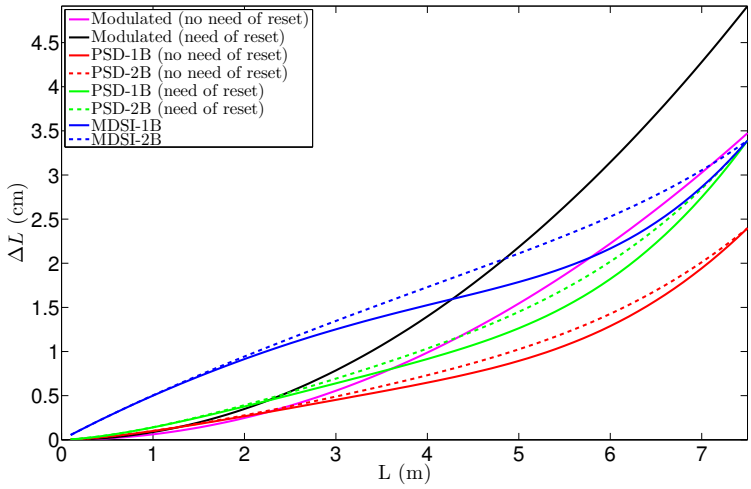

Figure 2.11: Distance error due to shot noise for the different ToF techniques. In pulsed ToF, duty cycle was set to 0.1%.

ground is $\bar{p}_{BIndoorMin}$ and that the minimum distance from which the light signal is reflected is 0.5 m these values were calculated as:

- For the modulated ToF: $C_{mod} = 400$ fF
- For the PSD ToF: $C_{PSD} = 450$ fF
- For the MDSI ToF: $C_{MDSI} = 230$ fF

For the pulsed ToF techniques a duty cycle of 0.1% was selected. Fig. 2.13 shows the thermal noise related distance error for the all the studied techniques. Even with these light power values it can be seen that the thermal error generated is unacceptable for almost any application. As said before, one way to avoid this is to use an adaptive number of accumulations, where T_{int} and, thus, N_{acc} for each pixel is not fixed. Instead, a pixel continues to accumulate measurements until a certain voltage in the storage capacitors is reached. If

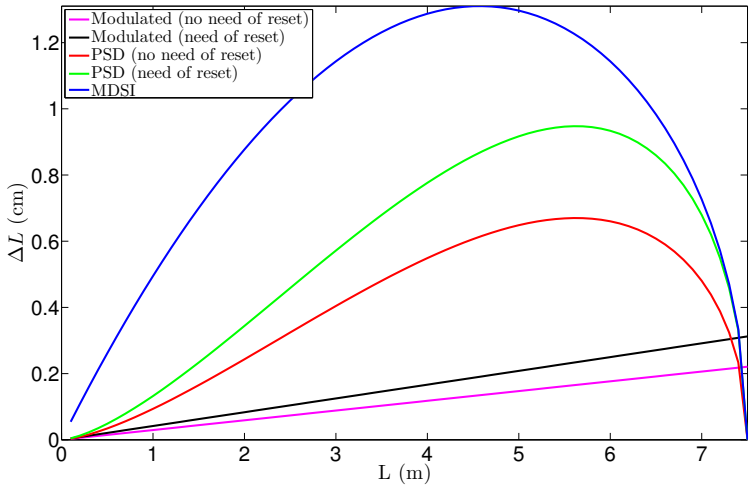

Figure 2.12: Distance error due to shot noise for the different ToF techniques with no background light. In pulsed ToF, duty cycle was set to 0.1%.

this condition is met, then the pixel stops the integration process, but the rest of the pixels can continue accumulating. To perform this, a comparison between the voltages stored in the capacitances and a saturation voltage must be performed every certain number of cycles, N_{comp}.

Thanks to this, the storage capacitances can be of any size as long as they do not lead to pixel saturation in N_{comp} cycles, avoiding loss of distance information. Fig. 2.14 shows the thermal noise using capacitances of 10 fF. This value will assure in all cases that at least 10 accumulations can be performed. As it can be seen, with this technique, the distance error because of thermal noise in the storage capacitors decreases significantly.

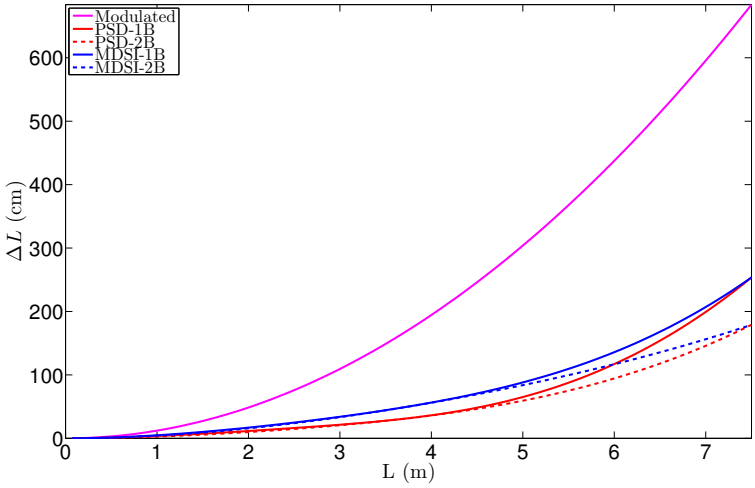

Figure 2.13: Distance error due to thermal noise for the different ToF techniques with big storage capacitances.

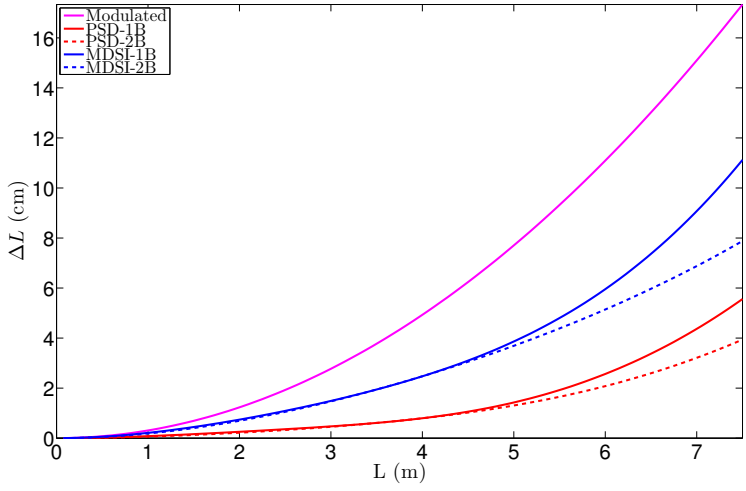

Figure 2.14: Distance error due to thermal noise for the different ToF techniques with $C = 10$ fF.

2.5 Selected Topology

Results from Section 2.4 show that in scenes with moderate or high background ambient light, pulsed ToF with low duty cycles (0.1%) perform better than modulated ones in relation to the shot and the thermal noise effect in the distance calculation. Among the pulsed techniques, from Fig. 2.11 it can be seen that the PSD techniques have lower shot noise than the MDSI ones. In addition to this, techniques without reset between x_i measurements present lower shot noise related errors. Finally, the choice between one or two background techniques depends on the amount of background light under which the sensor works. In high levels of ambient light, the two background measurements technique reduces the risk of pixel saturation. On the other hand, one background measurement techniques are less affected by shot noise. Next two chapters give an in-depth analysis at device (semiconductor) and circuit level of the different techniques addressed in this chapter.

Chapter 3

Study of Light Sensing Devices for ToF Sensors in Standard CMOS Technologies

One of the problems in ToF sensors design is the fast response required from the photosensor. One of the most used structures to deal with this problem are photosensing devices with transmission gates (TG) and floating diffusions (FD). Examples of this type of solutions can be found in [38, 11, 10, 16, 18]. In [38, 11, 10] the photosensors used are photogates, with four transmission gates drawing the flow of photogenerated charges to floating diffusions, where the x_i integrations are performed. The first two are fabricated in two-polygate technologies, and the third one adds an extra step in the standard fabrication process. In [16, 18] TG and FD are also used, but the sensors are implemented by pinned photodiodes (PPD). This makes them an interesting solution for sensors with imaging and ToF capabilities within the same pixel. Unfortunately, PPD technology requires a costly and dedicated fabrication process.

The objective of this chapter is to study the feasibility of fabricating structures with TG for ToF in standard CMOS technologies, in particular PPD-like topologies. Although the doping profiles of the foundries cannot be modified by external users, it is still possible to break some of the layout rules without compromising the integrity of the chip. Because of these design rules violations, an exhaustive analysis of the devices by means of software simulations was performed. To simulate these structures values for the doping profiles and the separation between pixel components are necessary. These values will be discussed in the next section. The feasibility of the pixels was studied in terms of the dark current (DC), the noise introduced by the reset transistor and the transmission velocity of the photocharges from the photosensor to the FD. This study was done using ATLAS simulation software tool [41].

In Section 3.1 the proposed structures are described. Section 3.2 presents the effects in terms of DC of adjusting several geometrical parameters in these devices. The effect of the reset transistor in the measurement error is analyzed in Section 3.3 and in Section 3.4 the transmission speed of the photocharges between the PD and the FD is evaluated. Section 3.5 summarizes the results obtained in this chapter. Part of the material presented in this chapter can be found in [42, 43, 44, 45].

3.1 Studied Structures

The PPD is a photosensing element consisting of two PN junctions: one between a superficial P^+ layer over an N layer and the other, deeper in the bulk, between the same N layer and the Psubstrate. The PPD is usually included within a 4-transistor configuration and constitutes the most common pixel in image sensors. In this imaging mode the photogenerated charges are accumulated in the PD and, at the end of the integration period, transferred to the FD, setting the TG ON for a small period of time, as shown in Fig 3.1. The initial voltage at which the FD is reset is measured before the transmission of the charges and this value is

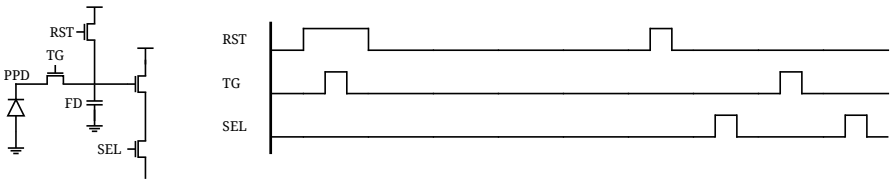

Figure 3.1: 4-Transistor pixel configuration and its associated time diagram for conventional image acquisition mode.

subtracted from the final voltage of the FD in an operation called correlated-double sampling (CDS). This operation removes the DC generated in the FD and the noise generated by the reset transistor. Also, since the time the TG is ON is smaller than the integration time, the effects of the TG can be neglected. Unfortunately, this operation cannot be performed in ToF mode and the impact of the DC and the reset noise has to be clearly investigated.

Without loss of generality, the ToF technique selected to study the pinned photodiode is the pulsed PSD-1B ToF. Fig 3.2 shows a structure with two TG in ToF mode with its companion timing diagram. The integration time must be controlled so that the first measurement is synchronized with the light pulse emission and the second one comes immediately after it (see also Fig 2.4 of Chapter 2). For this reason, the charges are not accumulated in the PD, but in the FD. By controlling the TG ON and OFF states as shown in Fig 3.2 the generated charges are transferred to the FD, so in one FD x_1 integration is performed while in the other FD the charges of x_2 are integrated. The process is repeated for a given number of pulses. Afterwards a third measurement is performed without light emission to obtain the background contribution from x_3 photons. This operation mode presents some problems that do not appear in the normal image operation mode. In particular, no CDS operation can be performed and the time the TG must be ON equals the integration time. This means that the DC of the FD and the reset transistor noise are not removed, and the DC generated under the TG cannot be neglected. These effects will be studied in Section 3.2 and Section 3.3. For this study a structure with only one TG is necessary because simulations show that extra TG do

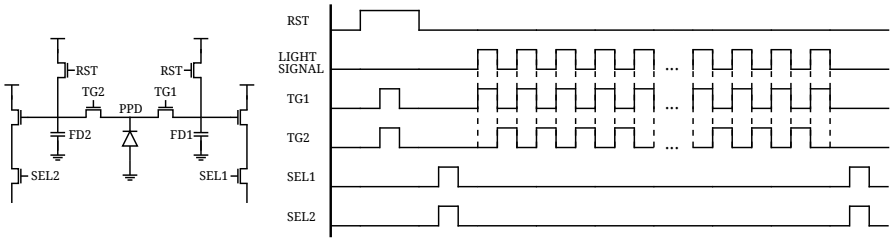

Figure 3.2: 2-tap pixel configuration and its associated timing diagram for ToF acquisition mode.

not affect the results presented in this chapter. For this reason the simulated structures will only have one TG, although ToF sensors in dedicated technologies usually have two or more.

The simplest structure of a photosensor with a TG is shown in Fig. 3.3. Here an Nwell layer over Psubstrate acts as the photodiode and it is connected to the FD through a transmission gate. In this figure, Y_{FD}, Y_{TG} and Y_{FD} are the horizontal length of the photodiode, transmission gate and floating diffusion, respectively. To keep the Psubstrate properly grounded two anodes are added to the device, with *CON* being their horizontal lengths. To separate these anodes from the rest of the device Shallow Trench Isolation (STI) structures with horizontal width $S1$ are added [46]. The vertical lengths of the Nwell layer and the N^+ and P^+ layers are marked in the figure as Y_j and Y_{Pj}, respectively. Commercial image sensor structures with TG are usually implemented using PPD. This structure reduces the DC and noise of the device and increases the quantum efficiency (QE) [47]. In the design and fabrication of commercial PPD a careful study of the doping profiles is needed to ensure the correct operation of the device [47, 48]. In standard CMOS technologies, this control is not possible, but the structure can be emulated using an Nwell over Psubstrate with a P^+ layer over it. Fig 3.4 and Fig 3.5 show the devices used to study this. As it can be seen, in none of them the Nwell layer and the P^+ are aligned with the TG at the same time. The reason for this is because a path between the PD and the TG for the photogenerated electrons must exist. The first device will be referred to as Nwell-aligned PPD, creating this path by aligning the Nwell layer with

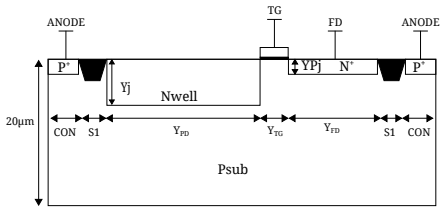

Figure 3.3: Cross-section of the simulated Nwell PD structure.

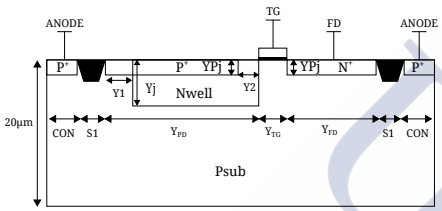

Figure 3.4: Cross-section of the simulated Nwell-aligned PPD structure.

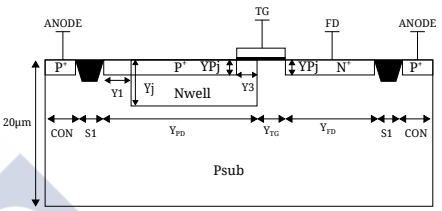

Figure 3.5: Cross-section of the simulated P^+-aligned PPD structure.

the TG and separating the P^+ layer. The second, named P^+-aligned, introduces the Nwell under the TG. These devices have three more parameters in addition to the ones present in Fig. 3.3: $Y1$, $Y2$ and $Y3$.

All the simulations shown in this paper are based on a 180 nm CMOS standard technology. All the parameters shown in Fig. 3.3, Fig 3.4 and Fig 3.5 must be correctly estimated to perform reliable simulations. For the doping concentrations, Gaussian profiles that emulate the actual doping profiles of the target technology were used. The vertical dimensions were estimated using values from the BSIM model for transistors and diodes provided by the manufacturer. Regarding the horizontal parameters, the minimum values allowed by the technology were chosen, except for Y_{PD}, Y_{TG} and Y_{FD}, that were set to 8 μm, 0.36 μm and 2 μm respectively and for $Y1$, $Y2$ and $Y3$ that are in regions of the device where layout rules are broken. For this reason and because these values strongly affect the dark current, a study of the effects of these parameters is performed in the next section.

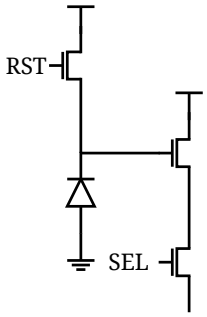

Figure 3.6: 3-Transistor pixel configuration.

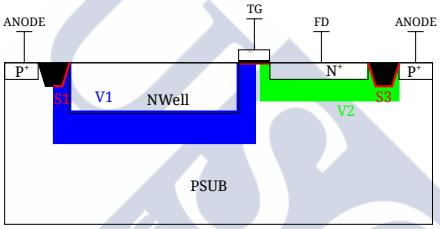

Figure 3.7: Cross-section of the Nwell PD where the dark current generation zones are marked.

To verify the reliability of the process parameters used for the simulation, experimental results from the same target technology presented in [49] were compared to simulations of the same devices performed with the ATLAS tool. These results are dark voltage (DV) measurements in a 3-Transistor (3T) pixel structure, like the one shown in Fig. 3.6. The dark voltage is defined as the voltage difference obtained due to the integration of the DC in the photodiode node. Table 3.1 conveys such DV values for two different devices and several PD sizes. In all cases, 2D simulations were performed and then generalized to the 3D case. In our simulation results, two fitting parameters were included to take into account the effects of the reset transistor and the gain of the source follower transistor, since they were not included in the simulations. As it can be seen, the simulated results differ less than 15 mV/s from the measured ones, demonstrating the accuracy of the simulation setup.

Device	Size (μm^2)	DV (mV/s) from [49]	Simulated DV (mV/s)
Nwell/Psub	5 × 5	149.5	159.4
	10 × 10	101.3	115.1
	20 × 20	64.0	72.8
	40 × 40	54.8	39.3
P+/Nwell/ Psub	5 × 5	74.0	69.9
	10 × 10	34.0	41.0
	20 × 20	23.2	21.9
	40 × 40	12.3	10.9

Table 3.1: Comparison between the dark voltage measured in [49] and the same devices simulated with ATLAS.

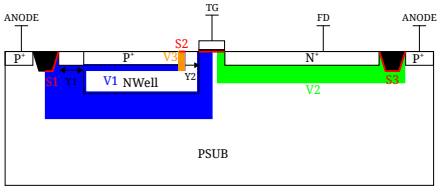

Figure 3.8: Cross-section of the Nwell-aligned PPD where the dark current generation zones are marked.

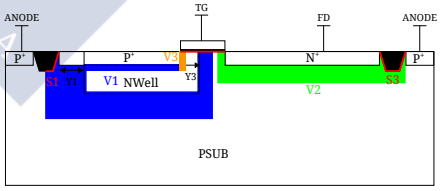

Figure 3.9: Cross-section of the P^+-aligned PPD where the dark current generation zones are marked.

3.2 Layout Optimization in terms of DC

The advantage that the P^+ layer offers in commercial pinned photodiodes is, mainly, the reduction of the generated surface DC. This section explores the effect of this layer in the Nwell-aligned and P^+-aligned PPD devices in terms of DC. Since the values selected for $Y1$, $Y2$ and $Y3$ influence this, our study takes into account these three parameters. The three main DC sources in the displayed devices are:

i. Thermal DC in the depletion regions.

ii. Surface DC in the silicon oxide interfaces.

iii. Band-to-band tunneling dark current (BTB-DC) in the heavily doped PN junctions.

Other effects such as carrier diffusion from neutral regions, impact ionization or Auger recombination were also simulated, but they cause currents at least two orders of magnitude lower, so they were neglected. In the next three sections the main DC sources are summarized. Then in Section 3.2.4 values for $Y1$, $Y2$ and $Y3$ that minimize the DC are selected and a discussion of the effect of the P^+ layer in the DC of the Nwell-aligned and P^+-aligned PPD devices is presented.

3.2.1 Thermal DC

The defects present in the silicon lattice generate and recombine electron-hole pairs. In the depletion regions the generated pairs are separated by the electric field but, in equilibrium, the number of generated pairs equals, on average, the number of recombined ones. Since the PD is biased in inversion mode, the number of minority carriers is smaller than in equilibrium and the system tends to recover by making the number of generated pairs higher than the number of recombined ones. This leads to thermal dark current in the depletion regions. This type of DC is generated in the volumes marked as $V1$, $V2$ and $V3$ in Fig 3.7, Fig 3.8 and Fig 3.9.

From these generation volumes it makes sense to assume that this DC source is proportional to the area of the PD and the FD.

3.2.2 Surface DC

The number of defects present in the silicon-oxide interface is much higher (several orders of magnitude) than those in the silicon lattice. For this reason, when a depletion region is in contact with an interface the number of electron-hole pairs generated increases. This current is called surface dark current, and appears in the surfaces marked as S1, S2 and S3 in Fig 3.7, Fig 3.8 and Fig 3.9. Since this DC term is generated in the surfaces around the PD and FD, it is proportional to the perimeter of these regions.

3.2.3 Band-to-Band Tunneling DC

The BTB-DC is generated when the PN junctions of a depletion region are heavily doped. In this case, the carriers can flow from the valence to the conduction band by means of direct tunneling. The more heavily doped are both sides of the junction, the more BTB-DC will be generated. This process is also enhanced by defects in the silicon structure, since these defects place available energy states inside the band gap. In the studied devices the BTB-DC is significant in the $V3$ volumes of Fig 3.8 and Fig 3.9. As it can be seen in these figures, the V3 volume and, hence, the BTB-DC is proportional to the width of the PD.

3.2.4 Layout Parameters Optimization

The P^+ layer of the devices in Fig 3.8 and Fig 3.9 is used to reduce the surface DC from the surfaces marked as S1 by separating the lateral depletion region of the Nwell/Psub junction from the silicon-oxide interface of the STI. $Y1$ is the distance between the Nwell and the STI oxide in the structures from Fig 3.4 and Fig 3.5. As it can be seen in the inlet of Fig 3.10, if this parameter is small a better fill-factor is achieved, but the lateral depletion region of the

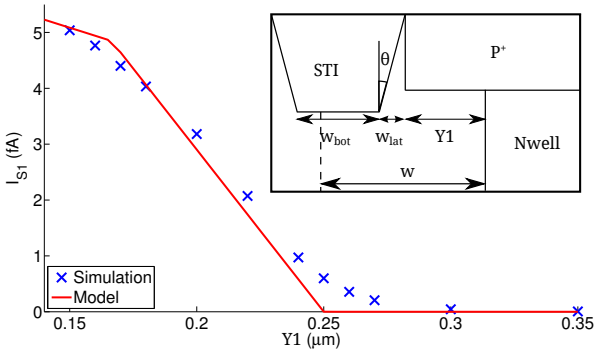

Figure 3.10: Simulations and theoretical calculation of the surface DC generated in the STI oxide for different $Y1$ values.

Nwell/Psub junction would reach the silicon-oxide interface of the STI and surface DC will be generated. This surface DC can be calculated as [50]:

$$I_{surf} = \frac{qn_iS_0}{2}PW \tag{3.1}$$

where q is the charge of the electron, n_i the intrinsic concentration of the silicon, S_0 the surface generation velocity and P the perimeter of the PN junction. This interface has two zones, the horizontal part at the bottom of the STI and the tilted interface of the walls. The surface DC in S1 can be calculated through the model introduced in [42] as:

$$I_{S1} = \begin{cases} \frac{qn_iS_0}{2}P\left[w-\left(w_{lat}+Y1\right)+\frac{w_{lat}}{sin(\theta)}\right], & \text{if } I \\ \frac{qn_iS_0}{2}P\frac{w-Y1}{sin(\theta)}, & \text{if } II \\ 0, & \text{if } III \end{cases} \tag{3.2}$$

where w_{lat} the horizontal length of the tilted wall and θ the angle that the wall forms with the vertical. Situation I occurs when $Y1 \leq w - w_{lat}$, II if $w - w_{lat} < X1 \leq w$, and III if $Y1 \geq w$.

Simulations for different $Y1$ values were performed using ATLAS. Fig 3.10 shows a comparison between the DC obtained in these simulations and the one calculated with (3.2). As it can be seen, for $Y1 > 0.3$ μm the surface DC generated in this region is negligible, so that $Y1 = 0.3$ μm was selected. In the inlet of this figure, w_{bot} is the bottom length of the STI.

As said, the P^+ and the Nwell layers cannot be simultaneously aligned with the TG. If that was the case no path would exist for the photocharges to reach the FD. To guarantee the generation of this path, in the Nwell-aligned structure, the P^+ layer must be moved away a distance $Y2$. The minimum value of $Y2$ that ensures the formation of this path is 0.1 μm, as it can be seen in Fig. 3.11 and Fig. 3.12, where the potential of the device around the channel is shown for two different $Y2$ values. In the first one $Y2$ has a value of 0.07 μm and it can be seen that there is no path for the electrons to flow from the Nwell to the TG's channel. In Fig. 3.12, $Y2$ value is 0.1 μm and the path is formed so the electrons can flow. This, in turn, results in the formation of the surface S2 in Fig 3.8, which results in BTB-DC generation as explained in Section 3.2.3. Fig 3.13 shows the relation between this BTB-DC and $Y2$. This figure also shows the total DC of the structure, revealing that most of the DC of the device is due to the BTB-DC produced at this surface. Shorter $Y2$ distances bring the P^+/Nwell junction closer to the Nwell region, enhancing the band curvature, and thus increasing BTB-DC. From Fig 3.13, $Y2$=1.2 μm was chosen as the optimum value.

In the P^+-aligned PPD the path for the photocharges is set by shifting the Nwell a distance $Y3$ under the TG. A minimum value $Y3 = 0.11$ μm is necessary for the correct transmission of charges, as it can be seen in Fig. 3.14. Shorter distances cause a potential barrier along the electrons path, as seen in Fig. 3.15, while longer ones create pockets, [51]. Both effects could generate image lag in conventional 2D imagining, and inaccuracies in the distance measured by the ToF sensor. This problem was presented in [51], and a surface P-layer under the TG was proposed as a solution. As apparent, this approach cannot be adopted with standard CMOS technologies. Another drawback of the Nwell under the TG is the curvature introduced by the gate potential in this region. Since this potential is positive, the Nwell

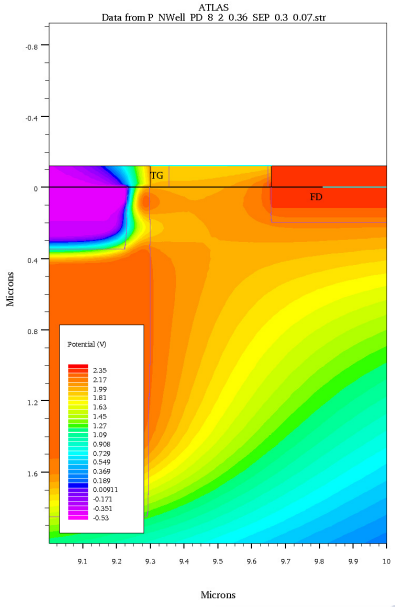

Figure 3.11: Nwell-aligned PPD TG region with $Y2 = 0.07\ \mu$m.

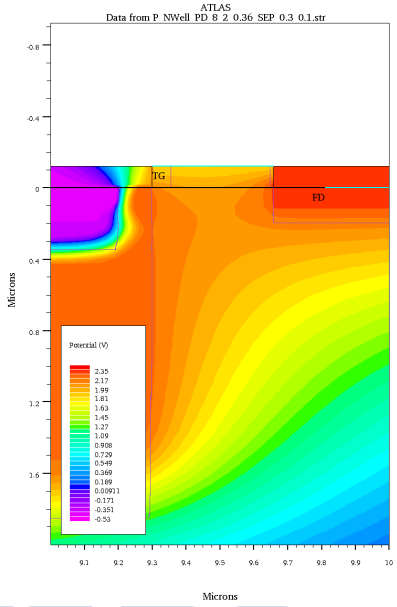

Figure 3.12: Nwell-aligned PPD TG region with $Y2 = 0.1\ \mu$m.

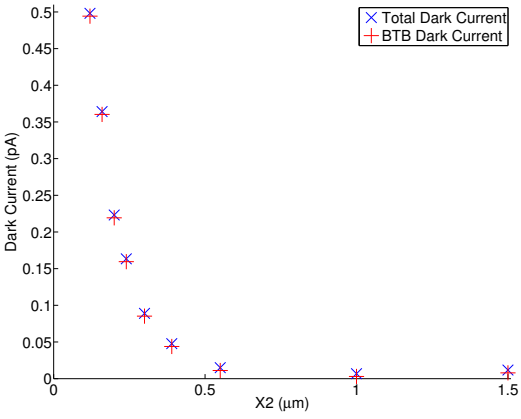

Figure 3.13: Relation between *X2* and BTB-DC and total DC in the Nwell-aligned PPD.

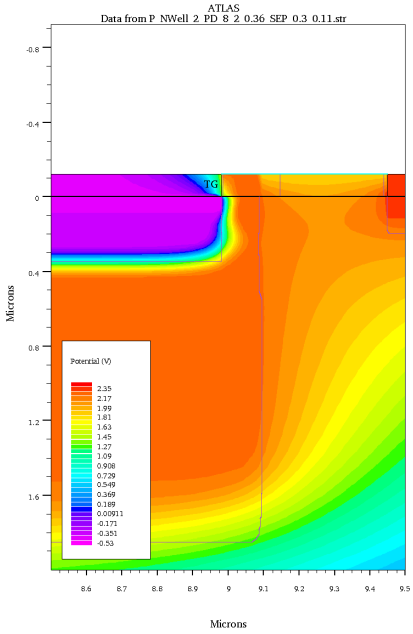

Figure 3.14: P^+-aligned PPD TG region with $Y2 = 0.11\ \mu$m.

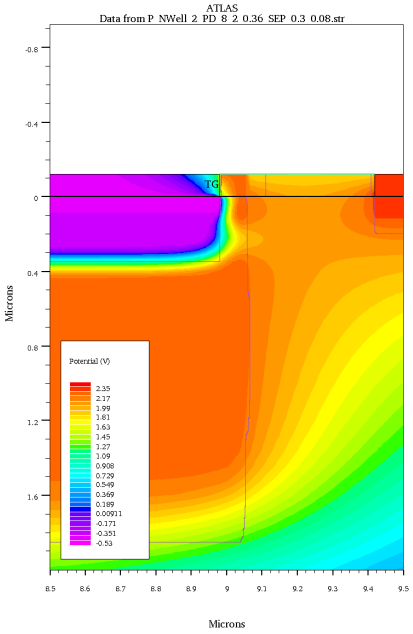

Figure 3.15: P^+-aligned PPD TG region with $Y2 = 0.08\ \mu$m.

under it is in accumulation mode and operates as if having higher doping concentrations. Hence, the BTB-DC generated at the S2 surface is greatly increased, becoming 8 orders of magnitude higher than in the Nwell-aligned PPD. Nevertheless, this structure is widely used in commercial PPDs for conventional 2D imaging [47]. The reason is that the DC is kept low using *ad hoc* doping concentrations in the Nwell and a P-layer under the TG, [51]. Also, in conventional image acquisition mode, TG is ON for only a small fraction of the whole integration time, yielding a negligible contribution to the total DC.

Once the optimum $Y1$, $Y2$ and $Y3$ values have been selected, a comparison between the three devices can be made. Table 3.2 summarizes the DC of these structures, classifying it as function of the part of the device where it is generated. The simulations were performed in 2D

Device		Dark current (fA)			
		Thermal	Surface	BTB-DC	Total
Nwell-align PPD	PD	1.582	0.442	2.986	5.010
	TG	0.005	0.001	0.000	0.006
	FD	0.025	1.480	0.000	1.505
P^+-align PPD	PD	-500.745	-11,257	0.000	-512.002
	TG	-3742.272	1409.760	2.67×10^8	2.67×10^8
	FD	0.023	0.899	0.000	0.923
Nwell PD	PD	0.121	2.530	0.000	2.651
	TG	0.005	0.001	0.000	0.006
	FD	0.025	0.899	0.000	0.924

Table 3.2: Comparison between the simulated dark current of the three studied structures.

and the results extrapolated to 3D structures. The Nwell PD values show that approximately 75% of the DC of the device comes from the PD and, of this, nearly 95% of it is surface DC. The other two structures have the P^+ layer with the purpose of reducing this DC. It can be seen from Table 3.2 that this objective is achieved since they have at least one order of magnitude less of surface DC in the PD. Unfortunately, this P^+ layer generates larger BTB-DC. It can also be seen that the P^+-aligned has a DC 8 orders of magnitude higher than the other two. As explained, this is because of the BTB-DC generated under the TG is so high that instead of generating electron-hole pairs the depletion regions of the PD and the TG it recombines them, being the reason of the negative values in the thermal and surface DC. Summarizing, simulations show that in standard CMOS technology, because of the lack of control over the doping profiles, the P^+ layer of the PPD does not achieve a reduction of the generated DC.

3.3 Reset Transistor

The three studied structures need a transistor for the reset operation (see Fig. 3.2). This transistor introduces extra effects that degrade the performance of the pixel, being the most important ones:

- Thermal noise.
- Clock feedthrough.
- Dependence of the reset voltage with the illumination.
- Leakage currents.

For the study of these effects an NMOS reset transistor at circuit level was added to the devices of Fig. 3.4, Fig. 3.5 and Fig. 3.3 in ATLAS simulations. The simulations show that this transistor affects in the same way the three structures. The reason for this is that the only dependence of the studied effects with the structures comes from the FD capacitance, which is the same in all the devices under study.

The thermal noise is a random effect, different for every FD and reset operation, generating an error in the distance measured by the sensor. The other three studied phenomena cause a systematic reduction of the FD voltage. While these effects can be countered with proper calibration, they reduce the dynamic range of the FD and, in consequence, the achievable SNR of the voltages stored there.

Before the beginning of the measurement the reset transistor sets the voltage of the FD to a fixed reset value, usually the power supply voltage, V_{DD}. During the measurement cycle the TG is used to direct the generated photocurrent to the FD according to the time diagram of Fig 3.2, decreasing the FD voltage. The minimum value of the FD will be reached when the Nwell and the FD reach the same potential, because then the transmission of the photocharges will stop. Fig. 3.16 shows the electrostatic potential for the Nwell PD structure

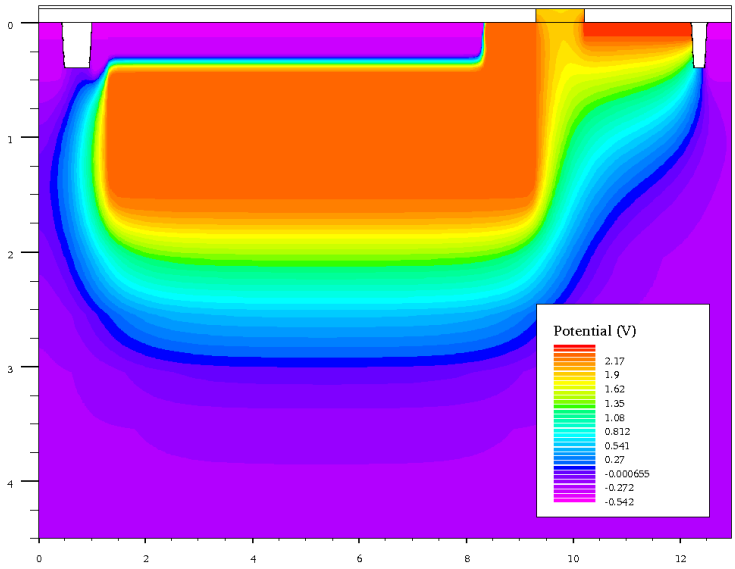

Figure 3.16: Electrostatic potential of the Nwell-aligned PPD structure.

when the FD is biased to the supply voltage, $V_{DD} = 1.8$ V. Based on this figure the difference between the Nwell and FD potential, this is, the maximum voltage variation of the FD is $\Delta V_{FDmax} = 150$ mV.

We will define the voltage variation generated by the photocharges being integrated in the FD as V_{Xi}, being $i = 1$, 2 or 3 depending on which X_i measurement is being integrated in the FD. If the systematic errors of the reset transistor were not present, the maximum value achievable by V_{Xi}, V_{Xmax}, will be ΔV_{FDmax}. If these effects are taken into account V_{Xmax} is modified as

$$V_{Xmax} = \Delta V_{FDmax} - \Delta V_{syst,total} \tag{3.3}$$

Being $\Delta V_{syst,total}$ the total systematic reduction of the FD voltage introduced by the reset transistor effects, calculated as the sum of the clock feedthrough, $\Delta V_{syst,clk}$, illumination, $\Delta V_{syst,light}$, and leakage, $\Delta V_{syst,leak}$, effects,

$$\Delta V_{syst,total} = \Delta V_{syst,clk} + \Delta V_{syst,light} + \Delta V_{syst,leak} \tag{3.4}$$

In other words, even if the only significant source of noise introduced by the reset transistor is the thermal noise, the other effects studied in this section reduce the maximum voltage value that the FD can accumulate and, thus, the maximum accuracy achievable by the sensor. In the rest of this section the effect of each of these phenomena in the distance accuracy will be discussed.

The thermal noise will generate an error in each V_{Xi} measurement of $\delta V_{thermal}$. Applying error propagation to (2.6) the effect of this noise in the distance measurement can be calculated:

$$\delta L = L_{max} \frac{\sqrt{V_{X1-X3}^2 + V_{X2-X3}^2 + V_{X2-X1}^2}}{\left(V_{X1-X3} + V_{X2-X3}\right)^2} \delta V_{thermal} \tag{3.5}$$

where:

$$V_{X1-X3} = V_{X1} - V_{X3} \tag{3.6}$$

$$V_{X2-X3} = V_{X2} - V_{X3} \tag{3.7}$$

$$V_{X2-X1} = V_{X2} - V_{X1} \tag{3.8}$$

V_{Xi} depends upon multiple factors like the power of the light signal, the capacitance of the FD, the quantum efficiency of the PD or the T_{oF} value. To illustrate the influence of the systematic effects introduced by the reset transistor the best case scenario for the ToF measurement will be studied. This means that we will assume, first, that V_{X1} and V_{X2} are equal to V_{Xmax} and, secondly, that V_{X3} is 0. The first assumption implies that the measured

distance is at mid-range, $L_{max}/2$, and the light signal is the strongest one measurable by the sensor. The second implies that there is not background light present. Since this is the best case scenario, in general, the distance error will be worse than the calculated in the following study. With these assumptions (3.5) becomes,

$$\delta L = \frac{L_{max}}{2\sqrt{2}} \frac{\delta V_{thermal}}{V_{Xmax}} \tag{3.9}$$

In the rest of this section (3.9) is used to evaluate the influence of each reset transistor effect in the distance measurement. In all cases $L_{max} = 7.5$ m is supposed, so the distance at which this error is estimated is 3.75 m.

3.3.1 Thermal noise

The thermal noise is generated at the end of the reset operation, when the transistor is set OFF. Because of the thermal energy of the electrons in the FD capacitance they can move in and out of it through the reset transistor. This introduces an error in the voltage value of the FD,

$$\delta V_{thermal} = \sqrt{\frac{kT_{emp}}{C_{FD}}} \tag{3.10}$$

where k is the Boltzmann constant and T_{emp} the absolute temperature. In the devices studied the thermal noise introduced by the reset transistor is around $\delta V_{thermal} = 4$ mV at room temperature. Applying $\Delta V_{syst,total} = 0$ V to (3.3) and (3.9) this noise is translated in a distance uncertainty of 7.07 cm.

3.3.2 Clock feedthrough

When the reset transistor is cut off a capacitive coupling between the reset gate and the FD node causes a reduction in the voltage at the FD, due to clock feedthrough. This effect

W (μm)	Y_{FD} (μm)	$\Delta V_{syst,clk}$ (mV)	ΔL (cm)
1	1	133.1	62.76
1	2	121.5	37.22
1	4	103.4	22.76
0.5	2	69.6	13.19
0.25	2	36.15	9.32

Table 3.3: $\Delta V_{syst,clk}$ due to the clock feedthrough effect for different W and Y_{FD}.

depends on the voltage swing of the signal at the reset gate, ΔV_g, the FD capacitance, C_{FD}, and the C_{gs} value of the reset transistor,

$$\Delta V_{syst,clk} = \Delta V_g \frac{C_{gs}}{C_{gs} + C_{FD}} \tag{3.11}$$

As C_{gs} depends on the width of the transistor, W, simulations were performed for different widths. Also, C_{FD} varies with Y_{FD}, so this parameter was also varied. These simulations show great agreement with the results obtained using (3.11), showing a difference less than 10 % between them. The results from (3.11) are shown in Table 3.3. Using $\delta V_{thermal}$ calculated in the last subsection, this table also includes the distance error generated when only $\Delta V_{syst,clk}$ as a source of systematic voltage reduction is taken into account. Even in the best case of Table 3.3, ΔL increases to a value near 10 cm.

3.3.3 Dependence of the reset voltage with the illumination

When the reset transistor is activated the voltage of the FD is set to the initial voltage, ideally, V_{DD}, but the actual reset voltage is achieved when the current from the PD, I_{ph}, equals the sub-threshold current from the reset transistor, I_{RST}. For this reason, the reset voltage depends on the illumination reaching the pixel which is being reset. As long as the resetting of the FD for the three measurement intervals is done under the same illumination levels this error will be

I_{ph} (pA)	$\Delta V_{syst,light}$ (mV)	ΔL (cm)
200	0.5	7.09
500	1.4	7.14
2000	5.1	7.32
5000	11.2	7.64

Table 3.4: $\Delta V_{syst,light}$ due to different illumination levels during the reset operation.

a systematic one that will generate a reduction in the available voltage swing, $\Delta V_{syst,light}$. The subthreshold current from the reset transistor can be calculated using equations from [52]. Matching this current with I_{ph} the FD reset voltage as a function of the photocurrent can be calculated, and thus $\Delta V_{syst,light}$. Table 3.4 gathers the calculated $\Delta V_{syst,light}$ for different photogenerated currents, that match with less than a 1 % of difference with the values obtained through simulation. This table also includes the distance error calculated when $\delta V_{thermal}$ estimated in subsection 3.3.1 is used and the only systematic voltage reduction considered is $\Delta V_{syst,light}$.

3.3.4 Leakage current

Although the reset transistor is cut off during the measurement operation a small subthreshold current still flows through it. The reduction of the FD voltage because of this current is of approximately, $\Delta V_{syst,leakage} = 10$ mV at room temperature. When only this systematic voltage reduction is considered, ΔL is 7.57 cm.

When all the effects of the reset transistor are taken into account, the error introduced by them in the distance measurement is, in the best case scenario, around 10 cm. In the case of conventional imagers this error can be removed using CDS operation but, as it was said at the beginning of the chapter, this operation cannot be performed in ToF mode so, this error will always be present.

3.4 Transient Analysis

Indirect pulsed ToF techniques assume square light pulses reaching the devices. The fact that the electrons generated by this light need a finite time to be transmitted from the PD through the TG causes some distortion in the photocurrent pulses reaching the FD. In this section, the transmission speed of the device is analyzed discussing its dependence with the PD and TG lengths. In addition to this, the effect that the pulse distortion has on the distance measurement is quantified.

To study the transmission velocity, simulations varying the PD and TG length were performed for the devices in Fig. 3.3 and Fig. 3.4. The device in Fig. 3.5 was not investigated because the high value of its dark current masks the photocharges reaching the FD. Transient simulations were performed where the current reaching the FD of the device is measured when a light pulse of $T_p = 50$ ns is used to illuminate the PD. This pulse is emitted 50 ns after the beginning of the simulation. Fig. 3.17 shows the result of these simulations for the Nwell PD structure with Y_{PD} =4 μm and TG lengths of 0.35, 0.54, 0.72 and 0.9 μm. It is clear from this figure that the signal being accumulated in the FD does not present a square pulse profile.

To study the charge transfer capabilities of the structures, the concept of dynamic charge transfer efficiency (DCTE) is introduced. We define the DCTE as the result of the integration of the charges reaching the FD, during the light pulse, divided between the integration of all the generated charges in the PD during the same time interval. Table 3.5 shows this parameter for the Nwell PD and the Nwell-aligned PPD structures. This value has been calculated for different Y_{PD} and Y_{TG} values. In both devices, when the TG length is maintained constant, the variation of the charge transfer is around 10% for a 4$\times$ increase in Y_{PD}. This shows that the size of the PD has only a moderate effect on the charge transfer capabilities of these structures. On the other hand, this feature presents a great dependence with Y_{TG}. Varying this parameter from 0.36 μm to 0.9 μm generates a decrease in the charge transfer of about 55% for both devices and PD length values. Also, for the same geometry sizes, the Nwell

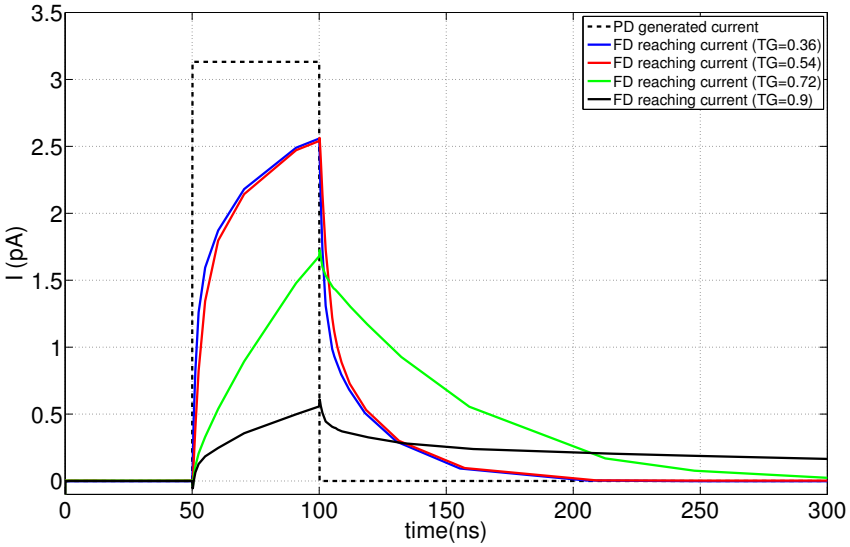

Figure 3.17: Current reaching the FD of the device after illuminating it with $T_p = 50$ ns for the nwell PD with Y_{PD} =4 μm.

PD structure presents better DCTE. This is the contrary of what happens in commercial PPD devices where the P^+ layer is adjusted to help collect and transfer the photocharges from the PD to the TG. Finally, this table also shows that the problems of slow transmission of the photocharges still appear even with TG lengths as low as 0.36 μm.

From these results two conclusions can be inferred. First, as in the case of the DC study, the simulations show that the addition of the P^+ layer into the PD in standard CMOS technologies does not improve its behavior, on the contrary, it worsens it. And secondly, the transient response is too slow to transmit the signal used in pulsed indirect ToF techniques.

To calculate the deviation in the distance measurement due to the finite transmission time of the device, the photocurrents represented in Fig. 3.17 can be modeled as exponential func-

Y_{PD} (μm)	Y_{TG} (μm)	Nwell-align PPD DCTE (%)	Nwell PD DCTE (%)
2	0.36	71.53	83.92
	0.54	68.38	82.42
	0.72	31.88	51.82
	0.90	15.55	31.57
4	0.36	66.53	76.80
	0.54	63.72	74.51
	0.72	24.85	40.89
	0.90	9.97	21.41
8	0.36	65.59	72.66
	0.54	62.14	69.67
	0.72	19.70	32.03
	0.90	6.93	14.77

Table 3.5: Comparison between the DCTE of the Nwell-aligned PPD and the Nwell PD for different Y_{PD} and Y_{TG}. In all cases Y_{FD} =2 μm.

tions with time constant τ:

$$I_{signal} = \begin{cases} I_m \left[1 - e^{-\frac{t}{\tau}}\right], & \text{if } 0 < t < T_p \\ I_m e^{-\frac{t}{\tau}}, & \text{if } t > T_p \\ 0, & \text{if else} \end{cases} \tag{3.12}$$

where I_m is the maximum I_{signal} value during the pulse transmission. Under ideal circumstances the charges accumulated during each measurement will be proportional to the number of photons reaching the device, so in (2.6) these charges can be used instead of the number of photons. However, due to the non-ideal situation of finite transmission time of the electrons, the charges accumulated during each measurement, will be:

$$x_1 = I_B T_p + I_m \left[(T_p - T_{oF}) - \tau \left(1 - e^{-\frac{T_p - T_{oF}}{\tau}}\right)\right] \tag{3.13a}$$

$$x_2 = I_B T_p + I_m \left[T_{oF} + \tau \left(1 - 2e^{-\frac{T_p - T_{oF}}{\tau}} + e^{-\frac{T_p}{\tau}}\right)\right] \tag{3.13b}$$

$$x_3 = I_B T_p \tag{3.13c}$$

where I_B is the photocurrent generated due to the background light reaching the FD. Using (3.13) in (2.6) allows to obtain the difference between the real distance, L, and the calculated one, L_{meas}:

$$L_{meas} = \frac{L + L_{max} f(T_{oF})}{g(T_{oF})} \tag{3.14}$$

where:

$$f(T_{oF}) = \frac{1 + e^{-n}\left[1 - 2e^{n\frac{T_{oF}}{T_p}}\right]}{n} \tag{3.15}$$

$$g(T_{oF}) = 1 + e^{-n}\frac{1 - e^{n\frac{T_{oF}}{T_p}}}{n} \tag{3.16}$$

$$n = \frac{T_p}{\tau} \tag{3.17}$$

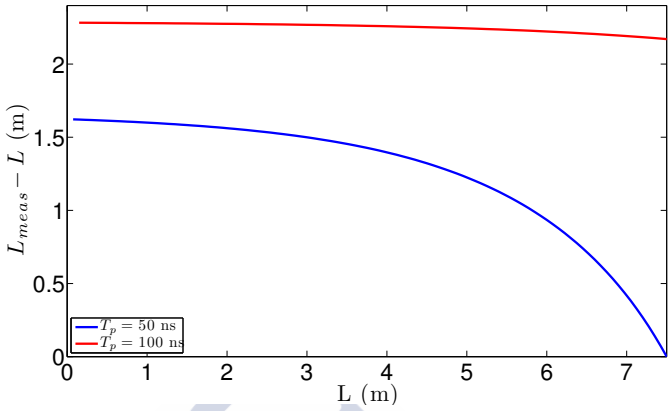

Figure 3.18: Difference because of the finite time response of the TG between the real distance and the measured one for the nwell-aligned PPD with TG length of 0.54 μm and $Y_{PD} = 8$ μm for $T_p = 50$ ns and $T_p = 100$ ns.

From (3.14) to (3.17) it can be seen that the generated error only depends on the pulse width T_p, the time constant τ and the T_{oF}. The first two parameters are constant for every ToF sensor and, thus, this error can be corrected by proper calibration of the device for the different T_{oF}. Fig. 3.18 shows the difference between L_{meas} and L for the Nwell PD device with $Y_{TG} = 0.54$ μm and $Y_{PD} = 8$ μm. This difference is presented for two T_p values, 50 ns and 100 ns. In the first case the error generated is around 1.5 m for most of the measurement interval except at the end of it. In the second one it is more uniform during the whole interval, but its value exceeds 2 m. It is important to note that with $T_p = 100$ ns the maximum measurable distance is 15 m, not 7.5 m, being this the reason why the error remains almost constant in Fig. 3.18.

3.5 Conclusions

The simulations presented in this chapter and the analysis developed from them show that PD structures with TG fabricated in standard CMOS technologies are not suited for the implementation of indirect ToF sensors. Either the devices are fabricated in alternative technologies, like CIS, or simple PD are used as photosensing devices and extra circuitry is added to perform the demodulation of the light signal. Since this work's objective is to design a ToF sensor in standard CMOS technologies, the latter approach is taken. In the next chapter the ToF pixel designed in this technology will be described. The chosen photosensor is the Nwell over Psubstrate, since in [40] experimental data is provided that shows that this photodiode is the one with better quantum efficiency and fastest response from all the possible ones in the selected 0.18 μm CMOS technology.

Chapter 4

Time-of-Flight Pixel

Chapter 2 shows that the pulsed PSD technique was the least affected by shot noise, so it was selected for the design of our ToF pixel. In addition, the adaptive number of accumulations technique permits to increase the signal level without pixel saturation. Also, Chapter 3 has shown that neither PPD nor TG structures are possible in standard CMOS technology, concluding that the Nwell over Psubstrate is our choice as photosensing device. In this chapter an alternative solution will be proposed and the selected topology for the ToF pixel will be described. Section 4.1 describes the operation of the pixel. In Section 4.2 each part of the pixel is explained. Finally, in Section 4.3 a detailed operation timing diagram of the pixel is presented. Part of the material presented in this chapter was previously published in [53]

For the sake of clarity, in the following sections the next notation is used for currents and voltages. Any DC signal or constant offset will be written in upper case with the subindex also in upper case, eg. V_{DC}. Small signal voltages or currents will be represented with the magnitude and subindex in lower case, for example v_s. Finally, the total value, this is DC plus small signal, will be written with the magnitude in lower case and the subindex in upper case, v_T.

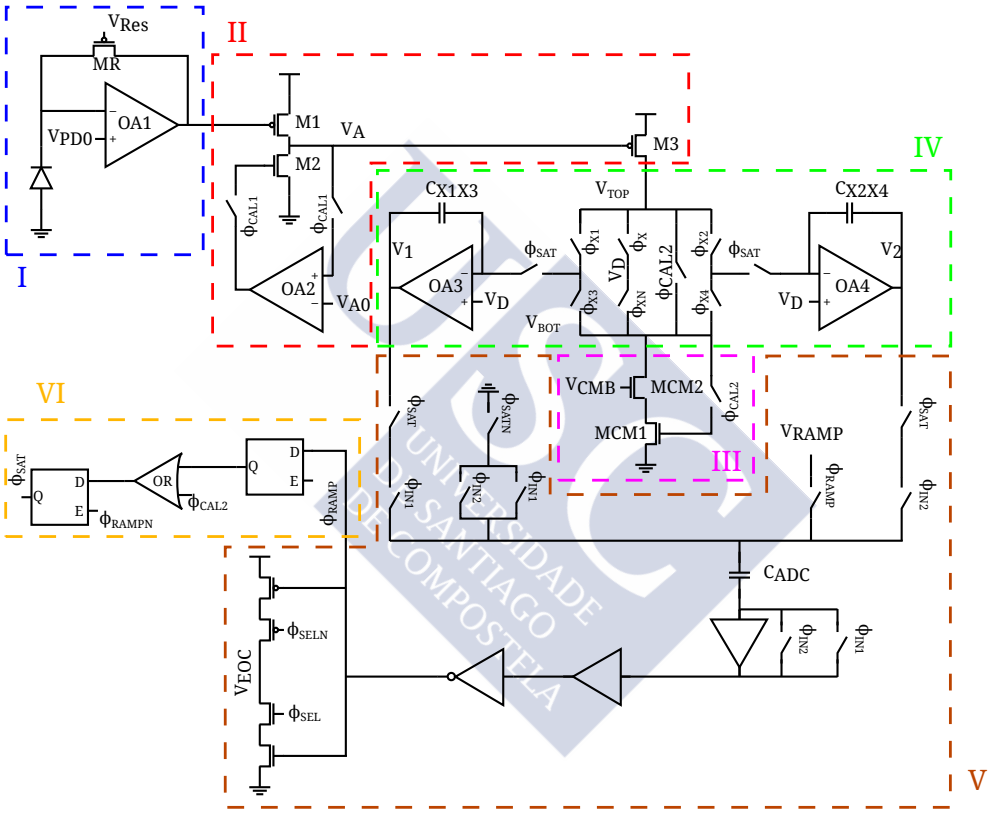

Figure 4.1: Complete schematic of the pixel for indirect ToF.

4.1 Pixel Operation

In this section an overall description of the pixel operation is provided. The pixel designed has an area of 65×65 μm^2 with an Nwell over Psubstrate photodiode of 50×50 μm^2. The width and duty cycle of the emitted pulses can be controlled externally but the design was made assuming a $T_p = 50$ ns as pulse width and a 0.1% duty cycle, this is, the pulses are repeated every 50 μs.

Fig. 4.1 shows the schematic of the pixel. This circuit is composed of six subcircuits, highlighted with dashed lines in the figure, each one with a different function:

Subcircuit I. Transimpedance Amplifier: the photodiode converts the background and signal lights into currents, which are subsequently converted to voltage before being amplified. This is done by the transimpedance amplifier subcircuit, highlighted in blue in Fig. 4.1.

Subcircuit II. Calibration Subcircuit: this subcircuit is highlighted in red in Fig. 4.1. The voltage signal is amplified by transistor M1 in common source mode. Transistor M3 then converts the voltage signal back to a current one. Amplifier OA2 is used before the arrival of the pulse to set V_A to a known value. This fixes the voltage generated by the background light and, consequently, the DC component of M3 transistor's current is fixed to a known value.

Subcircuit III. Background Suppression Subcircuit: even if the DC current of M3 is set to a low value, it is still necessary to subtract it from the pulse signal. For this reason our pixel includes the subcircuit highlighted in pink in Fig. 4.1. This is a current memory that senses the current generated at transistor M3 before the arrival of the pulse and then subtracts it after its arrival.

Subcircuit IV. Integrator Subcircuit: this subcircuit includes the storage integrator and the switches used to draw the current from transistor M3 and from the background suppression subcircuit to the integrators. It is highlighted in green in Fig. 4.1.

Subcircuit V. ADC subcircuit: the digitization in this topology is done with a single ramp ADC. Each pixel includes the comparator of the ADC, which also implements the adaptive

number of accumulations operation. This subcircuit is highlighted in orange in Fig. 4.1.

Subcircuit VI. Adaptive Number of Accumulations Subcircuit: this subcircuit stops the accumulations of the pixel before reaching saturation. It is highlighted in yellow in Fig. 4.1.

To obtain the distance information using the PSD method, the photocurrent must be integrated as defined by (2.7). In our pixel the photocurrent is amplified before being integrated. Because of speed constraints and the low levels of the photogenerated current this cannot be done in a single step. Subcircuit marked as I in Fig. 4.1 converts the photogenerated current in a voltage signal. After that, transistors M1 and M2 of subcircuit II amplify the signal and transistor M3 converts it back into a current. This current is the one integrated to calculate (2.8), repeated here for convenience:

$$L_{PSD-2B} = \frac{c}{2} T_p \frac{x_2 - x_4}{(x_1 - x_3) + (x_2 - x_4)} \tag{4.1}$$

Its DC part, I_{OUT}^{M3}, is equivalent to parameter B, the background light, in (2.7) and its small signal response, i_{out}^{M3}, to A, the light signal. To reduce the effect of the background light, operational amplifier OA2 is connected through the switches controlled by ϕ_{CAL1} before the emission of the pulse. By doing this, M2 gate voltage is adjusted to the incoming background light and the DC component of V_A and, consequently, I_{OUT}^{M3} is set to a known and externally selectable value, independent of the background light. This I_{OUT}^{M3} is sampled by the current memory subcircuit, III, for subsequent use. The x_i integrations of (2.8) are then performed by the subcircuit IV, by using the switches to lead the current from transistor M3 and from subcircuit III to the integrators in subcircuit IV. x_1 and x_2 are performed by integrating the current from the M3 transistor, while x_3 and x_4 use the current from subcircuit IV. After each pulse integration subcircuits V and VI perform the adaptive number of accumulations comparison.

For every frame the complete operation of the pixel is presented in Fig. 4.2, where the duration of each phase depicted here was verified by Montecarlo simulations. In this figure, 400 pulses are considered, although this number is externally selectable. As it can be seen

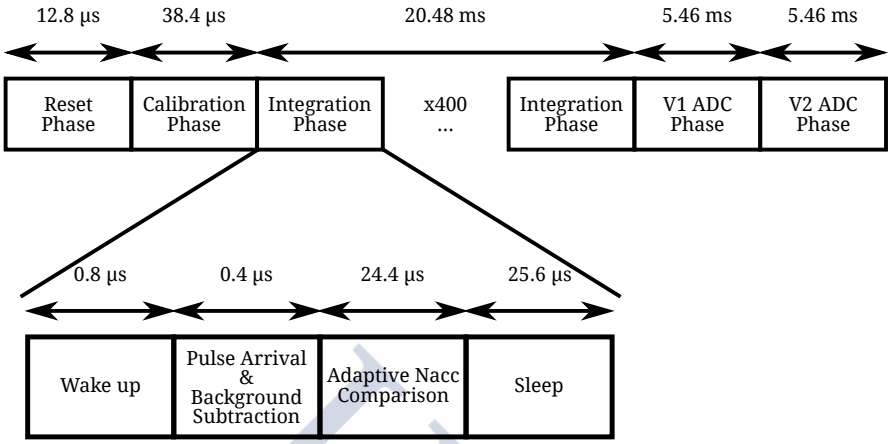

Figure 4.2: Time diagram of an entire frame in our ToF pixel.

every frame takes around 31.5 ms to finish, which gives a frame rate of 31 fps. Such values were extracted by simulation. An explanation of each phase of the figure is presented below:

i. Reset phase: during this step the storage integrators inside subcircuit *IV* are reset, so nodes V_1 and V_2 in Fig. 4.1 are set to a known and externally selectable value.

ii. Calibration phase: in this step signals ϕ_{CAL1} and ϕ_{CAL2} are activated. This has two consequences. First, V_A node is set to a known value, V_{A0}, which fixes the DC current flowing through M3, I_{OUT}^{M3}. This current is equivalent to parameter B in (2.7) and (2.8). Also, this current is sampled by subcircuit *III*.

iii. Signal integration phase: this phase is repeated multiple times and it is composed of four parts, as it can be seen in Fig. 4.2:

   (a) Wake up: since the duty cycle of the pulse is 0.1%, the operational amplifier OA1 is turned OFF most of the time to reduce power consumption. During wake up OA1 is turned back ON. Also, the voltage at M2's gate tends to fall because of leakage currents, so signal ϕ_{CAL1} is activated to restore it to the correct value.

(b) Pulse arrival and background subtraction: in this step the pulse is emitted and the integrations defined by (2.7) are performed. As explained before, these integrations are not performed over the photogenerated current but over an amplified version of it. Specifically over M3 transistor's current. This is done by using the switches present in subcircuit *IV* to drive this current to the integrators.

(c) Adaptive number of accumulations comparison: after each pulse integration the values stored as voltages V_1 and V_2 are compared to an external voltage in order to avoid saturation. If either voltage V_1 or V_2 reaches saturation, signal ϕ_{SAT} in Fig. 4.1 is turned OFF and the integration of pulses for that particular pixel stops for the rest of the frame.

(d) Sleep: until the arrival of the next pulse OA1 is turned OFF to decrease power consumption.

iv. Analog to digital conversion phase: at the end of the frame, V_1 and V_2 values for each pixel are digitized and stored in a memory. As said before, the ADC used is a single slope one. The digitization is done in a row-by-row manner, taking 104 µs per row. As it will be seen in the next chapter, our ToF chip comprises M×N pixels, thus it has 52 rows, leading to 10.92 ms for A/D conversion (5.46 ms for V_1 and the same amount of time for V_2).

4.2 Circuit Description

4.2.1 Transimpedance Converter

The transimpedance circuit of the ToF pixel, marked as *I* in Fig. 4.1 and shown in detail in Fig. 4.3, converts the current generated in the photodiode into a voltage. Transistor MR operates in the triode region acting as a resistance and, thus, converting the current signal

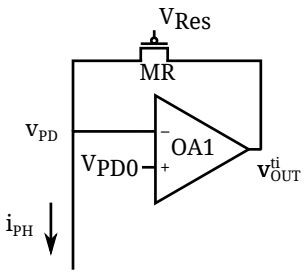

Figure 4.3: Schematic of the transimpedance subcircuit.

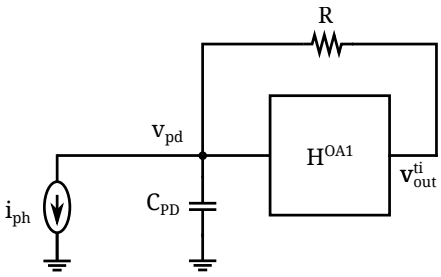

Figure 4.4: Equivalent version of the transimpedance subcircuit of the ToF pixel.

generated in the photodiode in a voltage one. As seen in Fig. 4.3 the resistance of MR can be externally tuned with voltage V_{Res}. The use of a differential amplifier for OA1 ensures a constant voltage in the photodiode biasing node that can be controlled through V_{PD0}. The higher this voltage, the better the quantum efficiency of the photodiode. However, very high values would complicate the design of operational amplifier OA1, since they would pull its common mode input voltage near the supply voltage. $V_{PD0} = 1.5$ V was finally selected as a trade-off design value. Fig. 4.5 shows the schematic of OA1. The geometries of the transistors of this circuit are summarized in Table 4.1 and the biasing voltage is set to $V_{BN} = 0.3$ V. These values were selected to ensure a cut-off frequency sufficiently high to transmit a square pulse of 50 ns generated by the light signal. Fig. 4.7 shows a simulation to illustrate the deformation of the pulse at the output of this subcircuit. Even if the deformation appears significative, it remains approximately constant, so it could be corrected for almost the entire measurement range with just an offset calibration.

Fig. 4.6 shows the Bode plot of OA1. As it can be seen, this circuit has a DC gain $G_0^{OA1} = 23$ dB and a cut-off frequency $f_0^{OA1} = 44$ MHz. The power consumption is around 20 μA. From this figure it is inferred that the response of OA1 can be modeled as a first order low-pass filter, with a transfer function:

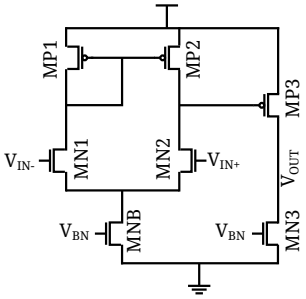

Figure 4.5: Schematic of operational amplifier OA1 of the ToF pixel.

Table 4.1: Transistor dimensions, in µm, for OA1.

	W	L		W	L
MN1	5	0.24	MP1	5	0.24
MN2	5	0.24	MP2	5	0.24
MN3	1.5	0.24	MP3	5	0.24
MNB	0.34	0.24			

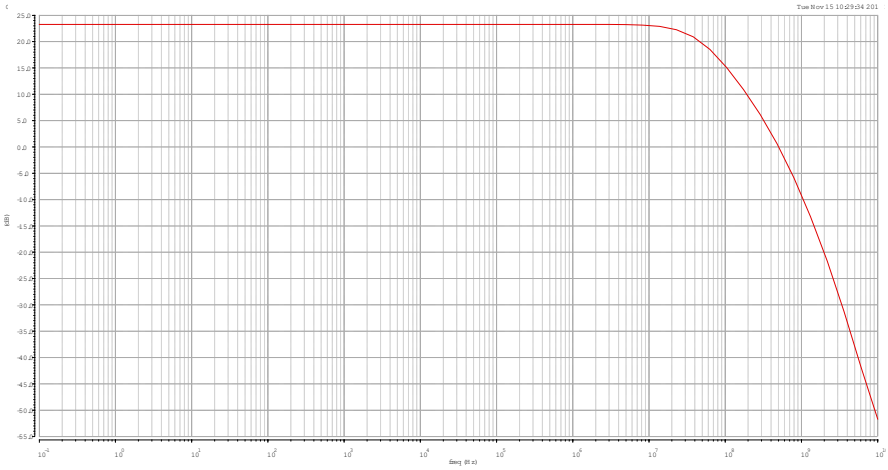

Figure 4.6: Bode plot of the operational amplifier OA1.

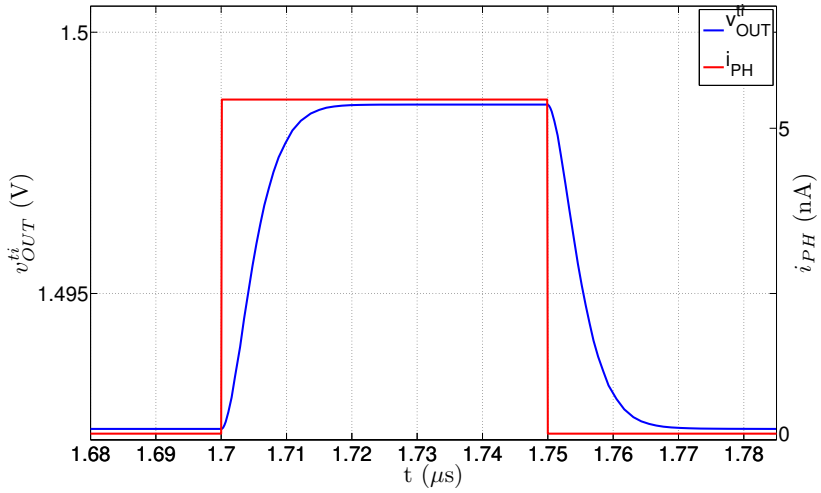

Figure 4.7: Deformation of the signal pulse at the output of subcircuit I of the ToF pixel.

$$H_{OA1}(s) = \frac{G_0^{OA1}}{\frac{s}{\omega_0^{OA1}} + 1} \tag{4.2}$$

Since operational amplifier OA1 has a high current consumption, it is only ON during the integration of the signal. The rest of the time V_{BN} is set to 0 V, so its power consumption is negligible.

Fig. 4.4 shows a simplified schematic of the transimpedance converter. Here i_{ph} is the current generated in the photodiode, C_{PD} its intrinsic capacitance and R the equivalent resistance of transistor MR:

$$R = \frac{1}{\mu_p C_{ox} \frac{W}{L} [V_{Res} - V_{PD} - V_{THP}]} \tag{4.3}$$

where V_{Res} is an externally adjustable voltage that controls the gate voltage of transistor MR. Applying Kirchhoff laws it can be demonstrated that the transfer function of the

transimpedance output node, v_{out}^{ti}, with respect to the photodiode current i_{ph} is:

$$H_{TI}(s) = \frac{v_{out}^{ti}}{i_{ph}} = \frac{\frac{G_0^{OA1}\omega_0^{OA1}}{C_{PD}}}{s^2 + s\frac{C_{PD}R\omega_0^{OA1}}{C_{PD}R} + \frac{\omega_0^{OA1}\left(G_0^{OA1}-1\right)}{C_{PD}R}} \tag{4.4}$$

This equation has the form of a second order low-pass filter and, assuming $G_0^{OA1} >> 1$, the DC gain of the entire subcircuit, G_0^I, and cut-off frequency, ω_0^I, become:

$$G_0^I = R \tag{4.5}$$

$$\omega_0^I = \sqrt{\frac{\omega_0^{OA1} G_0^{OA1}}{C_{PD}R}} \tag{4.6}$$

These two equations define the trade-off for the optimum value of R and, thus, the geometry of MR. Equation (4.5) shows that the current generated by the light signal in the photodiode is amplified by R, so, under this point of view, R should be as large as possible. On the other hand, from (4.6) it can be seen that the cut-off frequency of the entire subcircuit is proportional to the inverse of the square root of R, so larger values move the dominant pole of the circuit to the left in the s-plane, which could force the light signal out of the high gain region. The selected value was $R = 1.2$ MΩ. This puts the cut-off frequency of the transimpedance subcircuit at $f_0^I = 38$ MHz and the DC gain at $G_o^I = 120$ dB. This resistance is achieved by using $W = 0.24$ µm, $L = 8$ µm and $V_{Res} = 0.45$ V for MR, although as explained, this voltage is externally adjustable.

The current generated by the photodiode can be divided in two contributions: the one generated by the background light, I_{PHB}, and the one generated by the light signal i_{phs}. As it has been mentioned before, these currents are amplified by R. From Fig. 4.3 it can be seen that, in the absence of any photocurrent, the output voltage will be V_{PD0}, so the output voltage of this subcircuit can be calculated as

$$v_{OUT}^I = V_{PD0} - I_{PHB}R + i_{phs}R \tag{4.7}$$

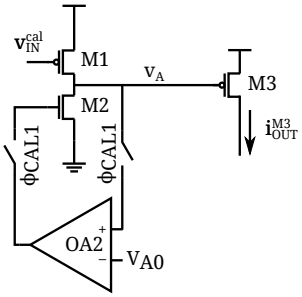

Figure 4.8: Schematic of the calibration subcircuit of our ToF pixel.

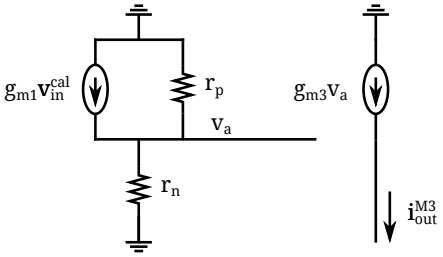

Figure 4.9: Equivalent circuit of the calibration subcircuit of the ToF pixel.

where only the third addend carries information from the light pulse. In other words, the response of this part of the circuit depends not only on the light signal reaching the pixel but also on the background light and the value selected for V_{PD0}. The next part of the circuit will amplify the response of the pixel to the light signal, while making it independent of the background light and V_{PD0}.

4.2.2 Calibration Subcircuit

The calibration subcircuit of the ToF pixel is marked as *II* in Fig. 4.1 and shown in detail in Fig. 4.8. This part of the pixel amplifies the voltage signal generated in the transimpedance subcircuit by the light signal reaching the photodiode, while ignoring the effect of the background light. After that, transistor M3 converts this signal back from voltage to current. The amplification is done by means of transistor M1 in common source configuration with the bias current provided by M2. The input to this part of the subcircuit, v_{IN}^{II}, is the output of the previous subcircuit, detailed in (4.7):

$$v_{IN}^{II} = (V_{PD0} - I_{PHB}R) + i_{phs}R = V_{IN}^{II} + v_{in}^{II} \tag{4.8}$$

where the input signal is separated in two parts, one that is considered constant over all

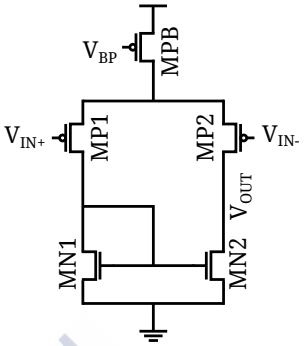

Figure 4.10: Schematic of operational amplifier OA2 of the ToF pixel.

Table 4.2: Transistor dimensions, in µm, for OA2.

	W	L		W	L
MP1	0.6	0.3	MN1	0.8	0.3
MP2	0.6	0.3	MN2	0.8	0.3
MPB	0.3	1.5			

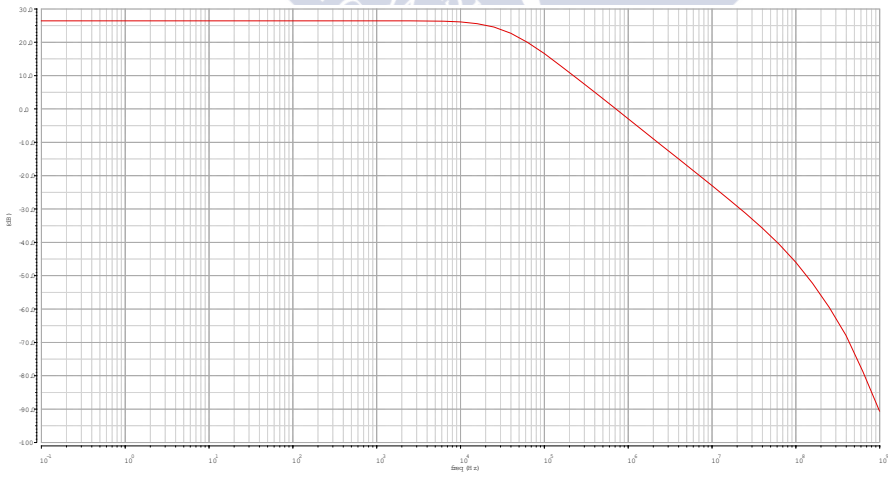

Figure 4.11: Bode plot of operational amplifier OA2.

the measurement period, V_{IN}^{II}, and one that carries the received light signal information, v_{in}^{II}. To make the pixel response independent of the background light the switches controlled by ϕ_{CAL1} are turned ON before the emission of the light signal. When this happens, the input to this subcircuit is only composed of V_{IN}^{II} and the feedback provided by operational amplifier OA2 adjusts the bias current generated by transistor M2, so M1 continue to work in the linear gain region and V_A equals V_{A0}, being V_{A0} an externally selectable voltage. The calibration signal ϕ_{CAL1} is turned OFF before the emission of the light signal but, now, V_A has a fixed and known value that does not depend on the background light. Also, this calibration step increases the robustness of the circuit against deviations from design nominal values in M1 and M2.

Since operational amplifier OA2 is not connected to the rest of the pixel when the light signal is arriving, it does not have the same requirements in terms of speed as the rest of the circuit. But, when connected, being in a feedback loop configuration means that stability concerns arise. To address this, OA2 was designed with a dominant pole at its output node. Fig. 4.10 and table 4.2 show the schematics and OA2 geometry values. The dominant pole is located at $f_0^{OA2} = 40$ KHz, its DC gain is $G_0^{OA2} = 26$ dB, as it can be seen in the Bode plot for this amplifier shown in Fig. 4.11, while its current consumption is 90 nA.

As it was said before, the DC part of v_A node is set to V_{A0} in the calibration phase. The small signal response of this node, v_a, is calculated applying Kirchhoff laws to the equivalent schematic of this subcircuit, depicted in Fig. 4.9:

$$v_a = -\frac{g_{m1} r_p r_n}{r_p + r_n} v_{in}^{cal} \tag{4.9}$$

where g_{m1} is the transimpedance of transistor M1, and r_p and r_n the resistances of M1 and M2, respectively. These parameters depend on the biasing current flowing through M1 and M2. Grouping them together, (4.9) can be rewritten as:

$$v_a = -G_{M1} v_{in}^{cal} \tag{4.10}$$

Selected geometries for M1 and M2 are $W = 2.72$ µm and $L = 0.24$ µm, and $W = 0.25$ µm and $L = 1.13$ µm, respectively. With these values the nominal gain for M1 is $G_{M1} = 30$ dB and the bias current $I_{bias}^{M1} = 8$ µA. After calibration G_{M1} depends on the background light. Contrary to conventional image sensors, in ToF sensors the information we are interested on is contained in the phase or delay of the signal, not on its amplitude, so even if the background light generates non-uniform gain for the pixels of the array, this does not degrade the resultant images.

As it was said before, the photodiode used in this pixel is an Nwell over Psubstrate with an area of 50×50 µm^2. The selection of the photodiode size was done at this stage of the design. Fig. 4.12 shows the SNR at node v_A for different photodiode sizes. As it can be seen, at approximately 50×50 µm^2 the SNR stops increasing with the photodiode size. The reason for this can be inferred from (4.6). As the size of the photosensor increases, so does its capacitance and the cut-off frequency of the transimpedance subcircuit decreases. For photodiode sizes larger than 50×50 µm^2 this frequency gets below the frequency of the light signal, so it is not correctly amplified, and this is reflected in the SNR.

Since transistor M3 is going to work in saturation, after the calibration its DC current can be expressed as:

$$I_{OUT}^{M3} = \mu_p C_{ox} \left(\frac{W}{L}\right)_3 (V_{DD} - V_{A0} - |V_{THP}|)^2 \tag{4.11}$$

where μ_p, C_{ox} and V_{THP} are the mobility, intrinsic capacitance and threshold voltage of M3, W and L its width and length and $V_{DD} = 1.8$ V the supply voltage. Since V_{A0} is known, externally selectable and independent from the background, the DC current at the output of this circuit is always constant and can be programmed. On the other hand, the small signal response of the transistor can be calculated from Fig. 4.9 as:

$$i_{out}^{M3} = -g_{m3} v_a \tag{4.12}$$

with g_{m3} being the transimpedance of transistor M3. Selected geometries for M3 transis-

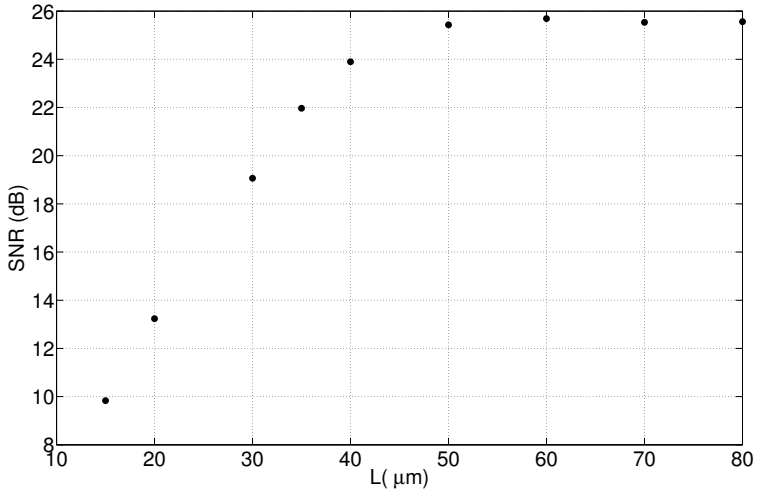

Figure 4.12: SNR at the v_A node for different photodiode sizes, assuming the photodiode is a square of side L and the light signal is reflected from a 1 m distance.

tor are $W = 0.3$ μm and $L = 2$ μm and $V_{A0} = 1.1$ V. With these values the DC component of the output current for this subcircuit is $I_{OUT}^{M3} = 105$ nA. From (4.10) and (4.12) the relation between the small signal input voltage and the output current for this subcircuit is:

$$i_{out}^{M3} = -g_{m3} G_{M1} v_{in}^{II} = G_0^{II} v_{in}^{II} \tag{4.13}$$

As stated before, G_0^{II} will vary depending on the background light, because of the calibration step, but for the background light conditions considered in this work its value will be between 90 μA/V and 110 μA/V. Putting together (4.7) and (4.13) gives an equation that links the photodiode's current generated by the light signal, i_{phs}, with i_{out}^{M3}:

$$i_{out}^{M3} = G_0^{II}\, R i_{phs} \tag{4.14}$$

So, the total current at the output of this subcircuit is:

$$i_{OUT}^{M3} = I_{OUT}^{M3} + G_0^{II}\, R\, i_{phs} \tag{4.15}$$

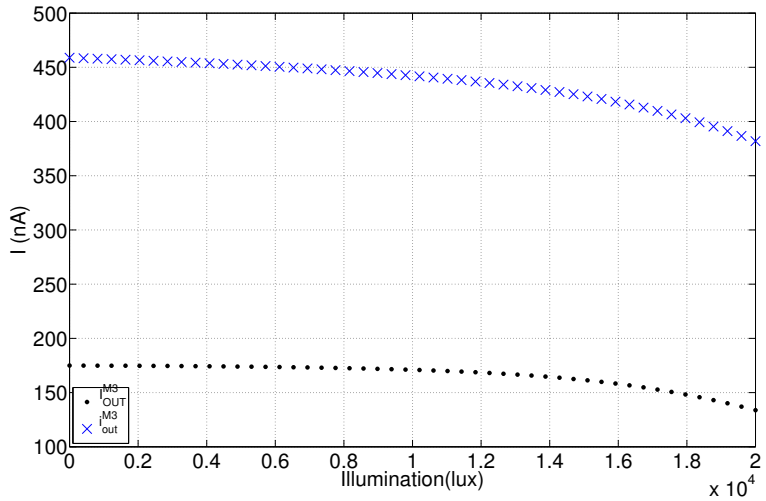

Figure 4.13: I_{OUT}^{M3} and i_{out}^{M3} as a function of the background light illuminance assuming the light signal is reflected from 1 m distance.

Fig. 4.13 shows simulations of how I_{OUT}^{M3} and i_{out}^{M3} change for different background values. The light signal is assumed to be reflected from a 1 m distance, and both the photocurrent generated by the light signal and by the background light are calculated using the data presented in Section 2.4 within Chapter 2. As it can be seen, there is a 20% decrease in I_{OUT}^{M3} and i_{out}^{M3} when 20 klux background light is present. To check the robustness of the design against mismatch, Montecarlo simulations were run. The results for two different situations: no background light and background light of 20 klux are shown in Fig. 4.14 and Fig. 4.15, respectively. In both cases it is assumed that the light signal is reflected from a distance of 1 m. Fig. 4.15 shows that, with a 20 klux background, some Montecarlo simulations show $i_{out}^{M3} = 0$ A. This is because the calibration circuitry is not able to compensate for the background light and mismatches between M1 and M2, so V_A saturates to the supply voltage. This is the reason why a background light of 20 klux is considered as the upper operational limit

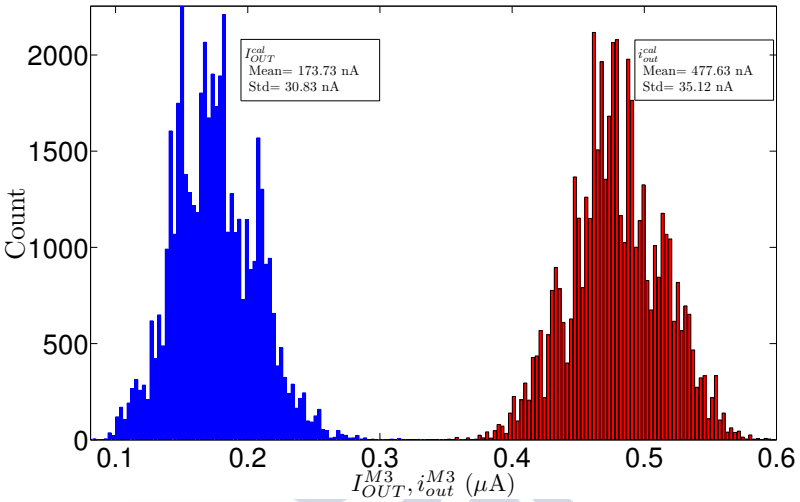

Figure 4.14: Montecarlo analysis for I_{OUT}^{M3} and i_{out}^{M3} with no background noise in our ToF pixel.

for our ToF sensor.

As it was said before, it is not the photocurrent, but i_{OUT}^{M3} the one to be integrated to calculate x_1,...,x_4 values from (2.8) in Chapter 2. This is possible because i_{out}^{M3} is proportional to i_{phs} and I_{OUT}^{M3} is constant, as it also happens with the photocurrent generated by the background light. This is what subcircuit *IV* does. As we are only interested in integrating i_{out}^{M3}, I_{OUT}^{M3} must be subtracted and, for this, a current memory that copies this current and reverses its direction is implemented. This circuit is explained in the next section.

4.2.3 Background Suppression Subcircuit

Fig. 4.16 shows the background suppression subcircuit in detail, which is marked as *III* in the circuit of the ToF pixel displayed on Fig. 4.1. This is an SI current memory formed by transistors MCM1 and MCM2 and two switches. The signal controlling these switches is ϕ_{CAL2}. As explained in the last section, a calibration step takes place before the emission of

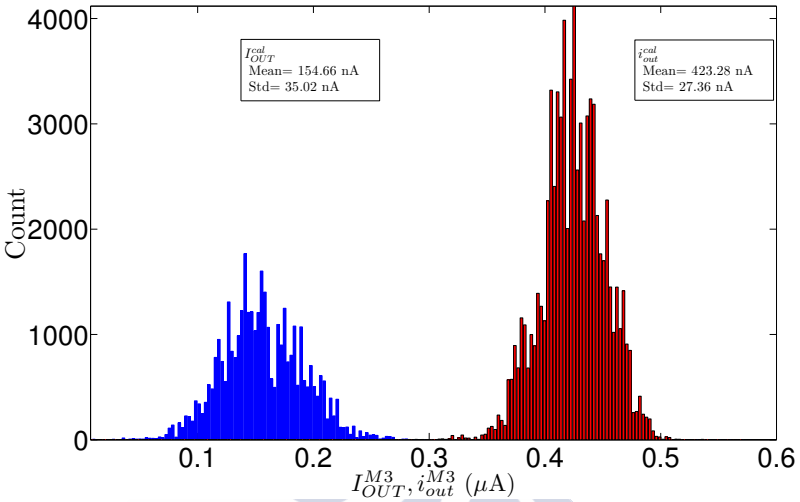

Figure 4.15: Montecarlo analysis for I_{OUT}^{M3} and i_{out}^{M3} with 20 klux background noise in our ToF pixel.

the light signal. During this step, voltage v_A is set to V_{A0}, which, in turn, sets the current from M3 to I_{OUT}^{M3}. ϕ_{CAL2} is turned ON after this calibration step, but before of the emission of the light signal. With both switches of the background suppression subcircuit of Fig. 4.16 ON, the current flowing through MCM1 equals I_{OUT}^{M3}. When these switches are turned OFF, capacitance C_{CM} holds the gate voltage of MCM1, so the current flowing through it remains constant except for non-idealities. A second transistor MCM2 is added to make a cascode configuration and, thus, to add robustness to the current of MCM1 against V_{BOT} variations. Width and length geometries of MCM1 are $W_{CM1} = 0.4$ µm and $L_{CM1} = 18.5$ µm and, for MCM2, $W_{CM2} = 0.5$ µm and $L_{CM2} = 0.5$ µm. C_{CM} has a capacitance around 200 fF implemented as an Ncap capacitor with $V_{CMB} = 0.8$ V.

Fig. 4.17 shows the result of a Montecarlo simulations in this circuit. It plots the difference between the current flowing through M3 transistor, I_{OUT}^{M3}, and the current memory after the calibration process. As it can be seen, there is an average difference of 17 nA between

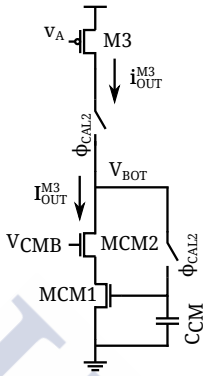

Figure 4.16: Background suppression subcircuit of our ToF pixel.

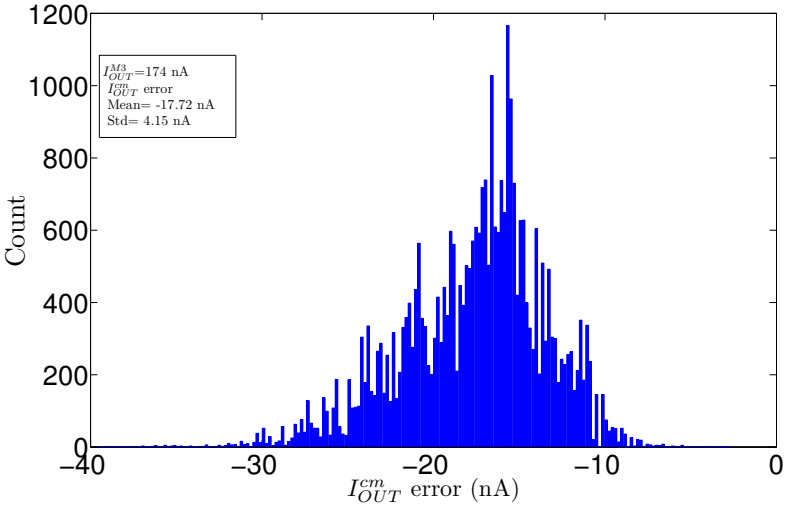

Figure 4.17: Montecarlo runs of the difference between I_{OUT}^{M3} and the current memory output after calibration.

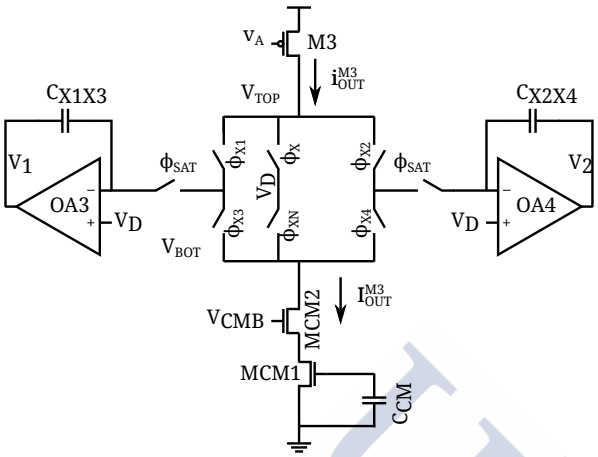

Figure 4.18: Detailed schematic of the integrator subcircuit of our ToF pixel.

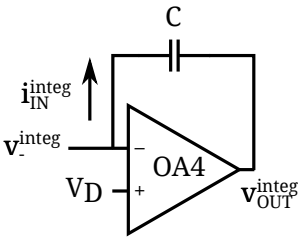

Figure 4.19: Equivalent circuit of the integrator circuit of our ToF pixel.

them. This is around a 10% of the nominal I_{OUT}^{M3} value. Nevertheless, this difference does not show a large variance between different seeds of Montecarlo, so it could be treated as a systematic error and be corrected in later steps.

4.2.4 Integrator Subcircuit

The integrator subcircuit of the ToF pixel is marked as *IV* in Fig. 4.1 and shown in detail in Fig. 4.18. It is composed of two integrators and six switches. The switches, controlled by signals ϕ_{X1} and ϕ_{X2}, drive the current from transistor M3 to the two integrators. This operation is synchronized with the emission of the light signal and right after, respectively, while the switches controlled by ϕ_{X3} and ϕ_{X4} drive the current of the current memory to the same integrators to subtract the background current. The switches controlled by ϕ_X and ϕ_{XN} provide a path to the currents of M3 and the current memory when they are not connected to the integrators.

Fig. 4.19 shows a simplified schematic of one of the integrators. Each of the two inte-

grators is composed of an operational amplifier, OA3 and OA4, and a capacitor, C_{X1X3} and C_{X2X4}, in a feedback loop configuration. Assuming that the current flowing in the integrator is i_{IN}^{integ} and the integration process lasts for a period of time T, the charge stored in the capacitor will be:

$$C = \frac{\Delta Q}{\Delta V} = \frac{\int_0^T i_{IN}^{integ} dt}{\left(v_-^{integ}(T) - v_-^{integ}(0)\right) - \left(v_{OUT}^{integ}(T) - v_{OUT}^{integ}(0)\right)} \tag{4.16}$$

where $v_-^{integ}(0)$ and $v_-^{integ}(T)$ are the values of the v_- node at the beginning and at the end of the integration period, respectively. Similarly, $v_{OUT}^{integ}(0)$ and $v_{OUT}^{integ}(T)$ are the values of v_{OUT} node at the beginning and the end of this period. These values are related with each other through the amplifier gain, A:

$$v_{OUT} = A\,(V_D - v_-) \tag{4.17}$$

Replacing (4.17) in (4.16), v_{OUT}^{integ} as a function of the incoming current can be calculated:

$$v_{OUT}^{integ}(T) = V_{OUT}^{integ}(0) - \frac{A}{A+1}\frac{\int_0^T i_{IN}^{integ} dt}{C} \tag{4.18}$$

If $A >> 1$ then:

$$v_{OUT}^{integ}(T) = V_{OUT}^{integ}(0) - \frac{1}{C}\int_0^T i_{IN}^{integ} dt \tag{4.19}$$

Fig. 4.21 shows the schematic of amplifiers OA3 and OA4 with the geometries of their transistors shown in Table 4.3. Also, the bias voltages are $V_{BN} = 0.5$ V, $V_{CN} = 0.8$ V and $V_{CP} = 0.5$ V. With these values the DC gain of these operational amplifiers is $G_0^{OA3} = G_0^{OA4} =$ 43 dB, their cut-off frequency $f_0^{OA3} = 1.75$ MHz and they consume 5.5 µA each. These values can be extracted from their Bode plot, that is shown in Fig. 4.20. Capacitance values for C_{X1X3} and C_{X2X4} are sized according to the dynamic range, and thus to the operating distance of the ToF sensor. V_1 and V_2 are reset to 1.4 V at the beginning of each frame. As it will be explained in the next sections, the adaptive number of accumulations subcircuit will

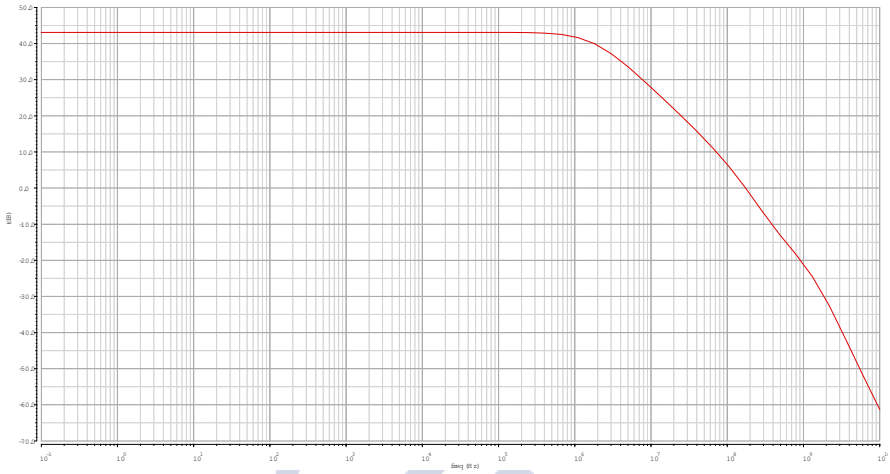

Figure 4.20: Bode plot of the operational amplifier 3 and 4.

stop the accumulation of charge for a given pixel when V_1 or V_2 reach an externally selectable value, that here is assumed to be set at 0.3 V. This means that the dynamic range of these two voltages is 1.1 V. On the other hand, the minimum distance for our ToF sensor was set to 1 m. Fig. 4.13 shows that the nominal value for i_{out}^{cal} at that distance is around 450 nA. Since the pulse width of the light signal is $T_{pulse} = 50$ ns, to ensure a minimum number of accumulations of $n_{acc} = 10$ pulses, we need capacitance values for C_{X1X3} and C_{X2X4} of:

$$C_{X1X3} = C_{X2X4} = \frac{n_{acc} i_{out}^{cal} T_{pulse}}{\Delta V} = \frac{10 \times 450 \times 10^{-9} \times 50 \times 10^{-9}}{1.1} \approx 204 \text{ fF} \qquad (4.20)$$

which is the value selected. To implement them, MIM capacitors with geometries $W =$ 20 µm and $L = 10$ µm were used.

4.2.5 ADC Subcircuit

Fig. 4.22 shows a detailed view of the ADC subcircuit of our ToF pixel to perform the analog-to-digital conversion of V_1 and V_2. This subcircuit is marked as V in Fig. 4.1. The selected

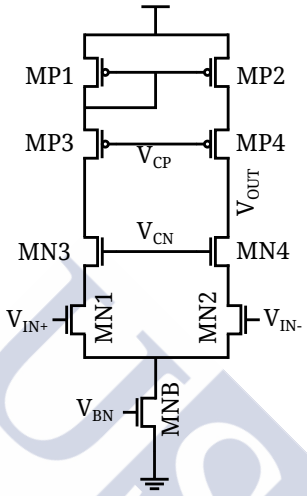

Figure 4.21: Schematic of operational amplifiers OA3 and OA4.

Table 4.3: Transistor dimensions, in µm, for OA3 and OA4.

	W	L		W	L
MN1	3	0.3	MP1	4.8	0.3
MN2	3	0.3	MP2	4.8	0.3
MN3	1.85	0.3	MP3	4.8	0.3
MN4	1.85	0.3	MP3	4.8	0.3
MPB	3.7	0.3			

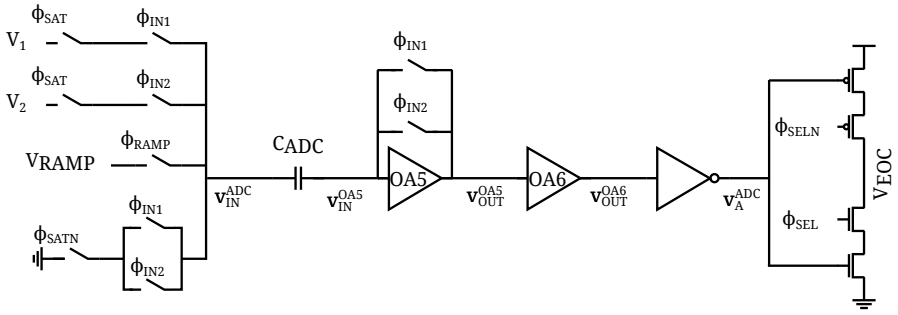

Figure 4.22: Detailed schematic of the ADC subcircuit.

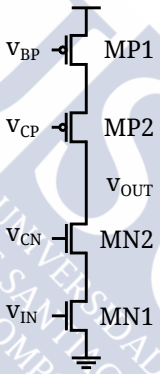

Figure 4.23: Schematic of operational amplifiers OA5 and OA6.

topology is a single slope ADC, with the ramp externally provided. The comparator of the ADC is included as part of the pixel circuitry. The control is implemented with a counter outside of the ToF array, while the frame buffer is a memory array. The comparator also performs the adaptive number of accumulations operation, as it will be shown in the next section.

The topology of operational amplifiers OA5 and OA6 is shown in Fig. 4.23, with their geometry values in Table 4.4. The bias voltages are: $V_{BP} = 1.2$ V, $V_{CP} = 0.8$ V and $V_{CN} =$

Table 4.4: Transistor dimensions, in μm, for OA5 and OA6.

	W	L
MN1	0.4	0.6
MN2	0.4	2
MP1	1	0.6
MP2	1.2	1.5

Figure 4.24: Bode plot of operational amplifiers OA5 and OA6.

0.6 V. The relation between the input and the output of OA5 is [54]:

$$v_{OUT}^{OA5} = v_Q^{OA5} - K^{OA5}\left(v_{IN}^{OA5} - v_Q^{OA5}\right) \tag{4.21}$$

where V_Q^{OA5} is the voltage at the output when the input and output nodes are short circuited and K^{OA5} its gain. From its Bode plot, shown in Fig. 4.24 it can be seen that their gain is $K^{OA5} = K^{OA6} = 53$ dB, its cut-off frequency $f_0^{OA5} = f_0^{OA6} = 200$ KHz and they consume 500 nA. Also, its nominal v_Q^{OA5} value is 500 mV.

This topology with a single input amplifier was selected for offset cancellation. The operation of this comparator is as follows. While OA5 input and output are short circuited, the first value to compare (V_1 or V_2) is connected to v_{IN}^{ADC}. Lets assume, for this explanation, that the connected voltage is V_1. The charge stored in C_{ADC} is:

$$Q_0^{ADC} = C_{ADC}\left(V_1 - v_Q^{ADC}\right) \tag{4.22}$$

with v_Q^{ADC} being the operating point of OA5. Next, the short circuit of OA5 is opened and the second value to compare, v_{RAMP}, is connected to v_{IN}^{ADC}. Now the charge stored in C_{ADC} will be:

$$Q_F^{ADC} = C_{ADC}\left(v_{RAMP} - v_{IN}^{OA5}\right) \tag{4.23}$$

Since the right node of C_{ADC} is isolated, both charges, Q_0^{ADC} and Q_F^{ADC} must be equal, so, from (4.22) and (4.23):

$$v_{IN}^{OA5} = v_{RAMP} - v_1 + v_Q^{OA5} \tag{4.24}$$

and using (4.21) the output voltage of OA5 will be:

$$v_{OUT}^{OA5} = V_Q^{OA5} - K^{OA5}\left(v_{RAMP} - v_1\right) \tag{4.25}$$

The gain of OA5, K^{OA5} should be high enough to make v_{OUT}^{OA5} saturate to 0 V (LOW logical value) or the supply voltage (HIGH logical value). The next blocks of the subcircuit,

operational amplifier OA6 and two inverters, increase the static and dynamic resolutions of the circuit. Since the gain of these steps is negative it means that

- $v_{RAMP} > v_1 \rightarrow V_A^{ADC}$ saturates to LOW and V_{EOC} to HIGH
- $v_{RAMP} < v_1 \rightarrow V_A^{ADC}$ saturates to HIGH and V_{EOC} to LOW

Another aspect to take into account is that the switches around C_{ADC} introduce charge noise in this capacitor, because of charge injection and clock feedthrough effects. Larger values of C_{ADC} reduce the effect of these charges, at the cost of increasing the area of the pixel. $C_{ADC} = 100$ fF was finally selected based on simulation results of Fig. 4.25 and Fig. 4.26. Fig. 4.25 shows the static resolution of the comparator for the whole input range of V_1. Fig. 4.26 shows Montecarlo simulations of this same difference for $V_1 = 0.7$ V. Assuming that the ADC input range is 1.8 V and the wanted precision is 8 bits, the least significant bit voltage is $V_{LSB} \approx 7$ mV. As it can be seen in Fig. 4.25, in the nominal case the comparator error is always smaller than V_{LSB}. Montecarlo simulations of Fig. 4.26 reveal that less than 1% of the runs exceed V_{LSB}. C_{ADC} was implemented using MIM technology.

4.2.6 Adaptive Number of Accumulations Subcircuit

Fig. 4.27 shows the adaptive number of accumulations subcircuit, also highlighted in yellow in Fig. 4.1. It includes two D flip flops and an OR logic gate. The flip flops are composed of four NAND gates, as it can be seen in Fig. 4.28. The output Q does not change if input E is in the LOW state. If E is in the HIGH state, Q will acquire the same state as the D input. The objective of this subcircuit is to generate the internal control signal, ϕ_{SAT}, that stops the accumulation of pulses when either V_1 or V_2 reach a certain level. Its precise operation will be explained in the next sections.

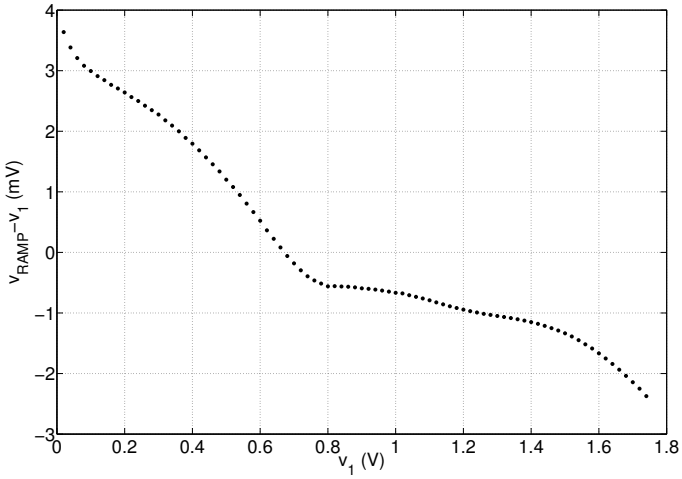

Figure 4.25: Static voltage resolution of the comparator with V_1 as common mode signal.

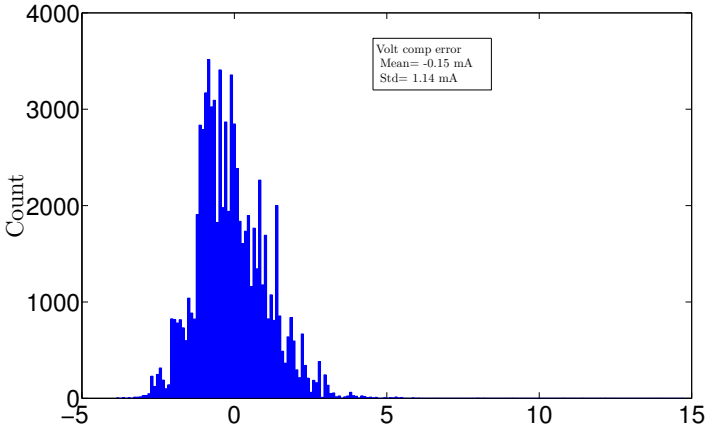

Figure 4.26: Montecarlo simulations of the comparator error for $V_1 = 0.7$ V.

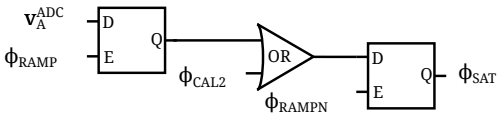

Figure 4.27: Schematic of the adaptive number of accumulations subcircuit.

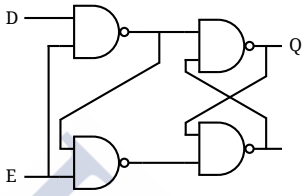

Figure 4.28: Schematic of the D flip-flop used as part of the subcircuit of our ToF pixel that implements the adaptive number of accumulations.

4.3 Measurement Steps

Twelve control signals are used to operate the pixel. The next sections explain how the circuits previously described are used to perform the ToF operation. In each frame, four different phases are needed. The first two, the reset and calibration phases, occur only once at the beginning of the frame. Then, several signal integration phases are performed and, finally, the analog-to-digital conversion phase is carried out.

4.3.1 Reset and Calibration Phases

These two phases take place at the beginning of the frame acquisition and the associated timing diagram of the control signals is shown in Fig. 4.29. As it can be seen, it takes 51.2 µs to complete both, 12.8 µs for the reset phase and 38.4 µs for the calibration one. In the first one, the storage capacitors, C_{X1X3} and C_{X2X4}, are reset. In the calibration phase, node V_A is set to V_{A0} and the memory current is set to I_{OUT}^{M3}, as explained in Section 4.2.2 and 4.2.3, respectively. In addition to this, during this step, the internal signal ϕ_{SAT} is set to HIGH. In

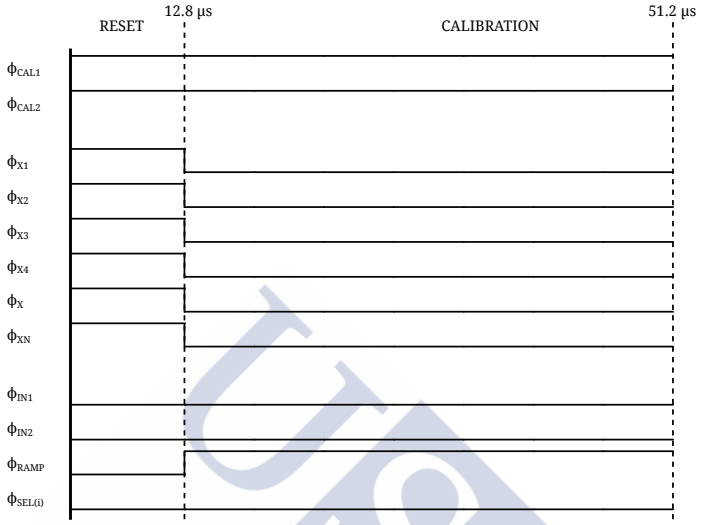

Figure 4.29: Timing diagram of the control signals during the reset and calibration phase.

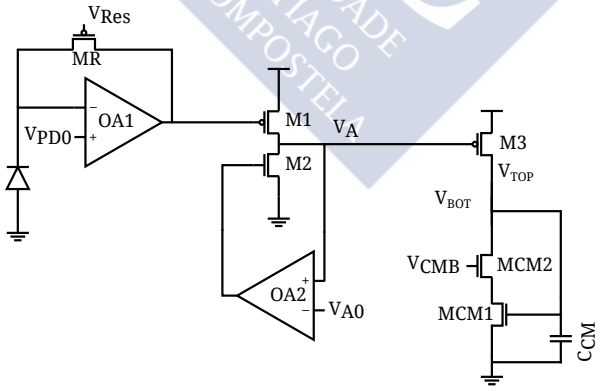

Figure 4.30: Circuit of the ToF pixel in the calibration step.

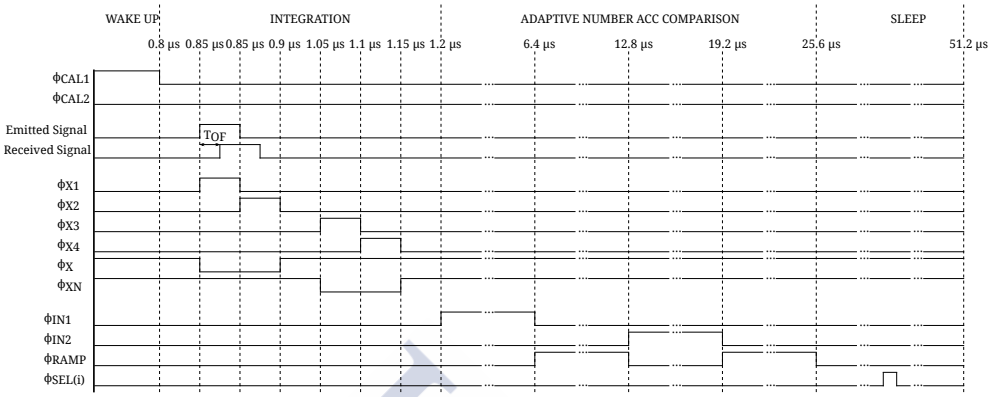

Figure 4.31: Timing diagram of the control signals during the signal integration phase.

Fig. 4.29 it can be seen that, in the calibration phase, ϕ_{CAL2} signal is HIGH, while ϕ_{RAMP} is LOW, so ϕ_{SAT} generation circuit, shown in Fig. 4.27, sets this signal to HIGH. Fig. 4.30 shows a simplified schematic of the relevant parts of the pixel in the calibration phase.

4.3.2 Signal Integration

The signal integration phases are performed after reset and calibration. During these phases the light pulses are emitted and the integrations to calculate the time-of-flight are performed. The signal integration phase is composed of four steps. The first one is the wake up step, where amplifier OA1 is turned ON. As it was explained in section 4.2.1, OA1 is turned OFF when it is not used, since its current consumption is high. In the next step, the four integrations necessary to obtain V_1 and V_2 and, thus, T_{OF} are performed. After that, V_1 and V_2 are compared to an externally selected voltage. If any of the two is smaller than this voltage, this pixel will not integrate more charge during this frame. At the end of this step, signal ϕ_{SEL} for each row is activated to store the number of pulses accumulated by each pixel. A timing diagram showing the control signals behavior at this phase can be seen in Fig. 4.31.

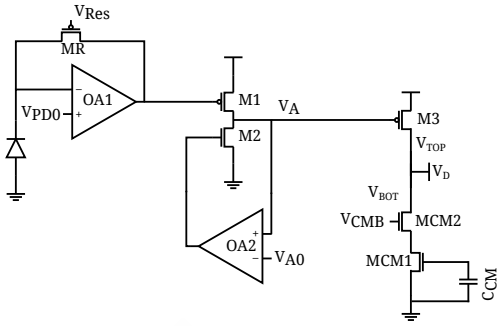

Figure 4.32: Schematic of the pixel in the wake up step.

Wake Up

During this step, amplifier OA1 is turned ON again and the node V_A is set to V_{A0}. This is done because, while amplifier OA1 is OFF, some charge at the gate of transistor M2 is lost so, before the arrival of the pulse, V_A node is reset to the correct voltage. Fig. 4.32 shows a simplified schematic of the relevant parts of the pixel for this step. This step starts at the beginning of the integration phase and lasts 0.8 µs.

Pulse Integration and Background Suppression

In this step the light pulse is emitted and all the information needed for the ToF calculation is collected. This is obtained with the four integrations of currents in the integrators of subcircuit *IV*. The integrated currents are either the one generated in M3 or the one generated in the current memory. Through all phases of the pixel, the currents that are not being integrated are being absorbed by V_D in order to avoid saturating V_{TOP} or V_{BOT} nodes. These integrations are run by the switches controlled by the signals ϕ_{X1} to ϕ_{X4} and the light pulse is emitted synchronized with the integration X_1. Figures 4.33 through 4.36 show the configuration of the pixel during these integrations. At the end of this step amplifier OA1 is turned OFF to save current. This step lasts 0.4 µs.

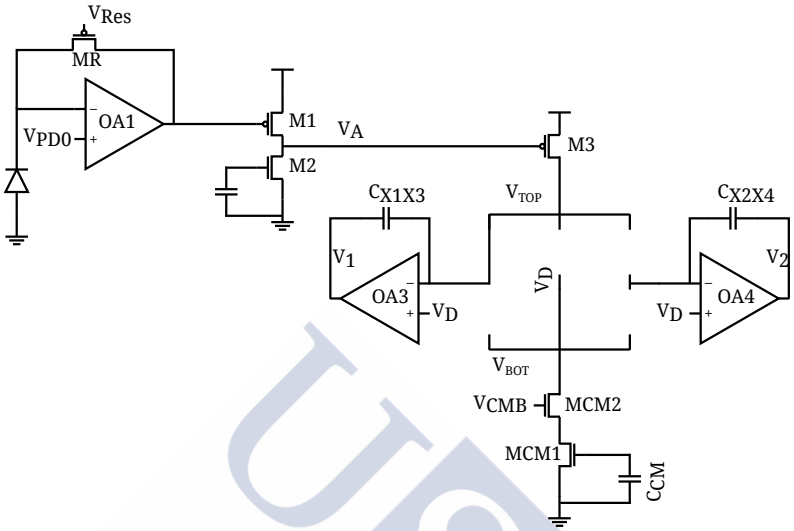

Figure 4.33: Simplified schematic of the pixel in the X1 integration step.

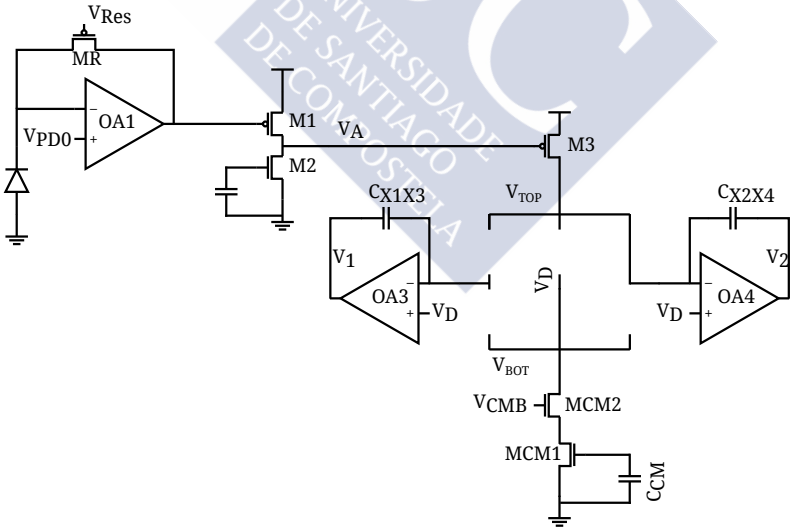

Figure 4.34: Simplified schematic of the pixel in the X2 integration step.

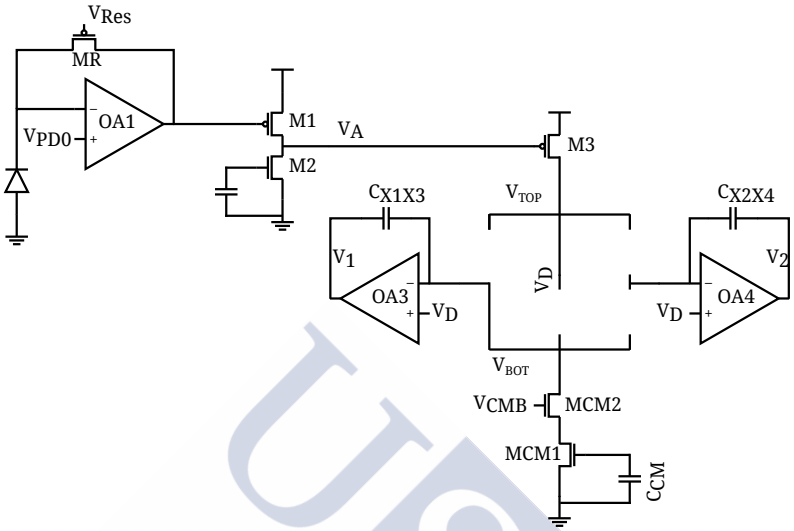

Figure 4.35: Simplified schematic of the pixel in the X3 integration step.

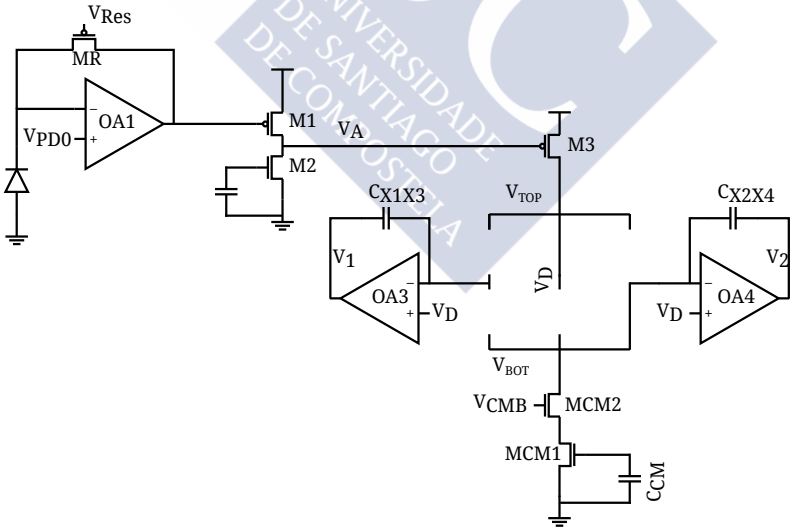

Figure 4.36: Simplified schematic of the pixel in the X4 integration step.

Adaptive Comparison

After the integrations of the incoming photons, the voltages accumulated as V_1 and V_2 in the ToF pixel of Fig. 4.1 are compared with an externally selected voltage using the comparator explained in Section 4.2.5. If either of them is smaller than this external voltage, the integration of pulses is stopped until the end of the frame. This is accomplished by turning off ϕ_{SAT}. We illustrate this with signal V_1 comparison. First, V_1 voltage is applied to C_{ADC}, by turning ON signal ϕ_{IN1}, as it can be seen in Fig. 4.38. Next, the externally controlled voltage is applied to this capacitor. This voltage is introduced in the pixel through input V_{RAMP}. The configuration of the comparator in this step can be seen in Fig. 4.39. If V_{RAMP} is bigger than V_1 then V_A^{ADC} saturates to LOW, which means that the output of the first flip flop will also turn to LOW. When the signal ϕ_{RAMP} is turned OFF, the output of the second flip flop, ϕ_{SAT}, will also turn OFF. ϕ_{SAT} will be restored in the next reset and calibration phase. Fig. 4.40 shows the pixel schematic while ϕ_{SAT} is OFF. As it can be seen, two things happen. First, the pixel integrators will be isolated from the currents of transistor M3 and the current memory, avoiding the accumulation of more pulses. Secondly, since ϕ_{SAT} is OFF and ϕ_{SATN} is ON, in the next signal integration phases, during this step, the external voltage is not compared with V_1 or V_2, but with ground voltage. Since $V_{RAMP} > 0$, this ensures that ϕ_{SAT} will continue OFF until the digitization phase. Fig. 4.37 shows a simulation of the transient response of V_1 and V_2 when the integration of pulses stops. As it can be seen in this example, after 16 pulse integrations, the voltage of V_1 falls under the externally selectable voltage applied to V_{RAMP}. When this happens, the pixel stops the accumulation of pulses in the integrators and V_1 and V_2 voltages remain constant until digitization. The adaptive comparison step lasts until 25.6 µs after the phase started. For the rest of the time, the row selection signal ϕ_{SEL} of each row is sequentially turned ON, so it can be known if the pixel stopped integrating pulses, because in that case, V_{EOC} of that pixel will be low. The entire signal integration phase lasts 51.2 µs.

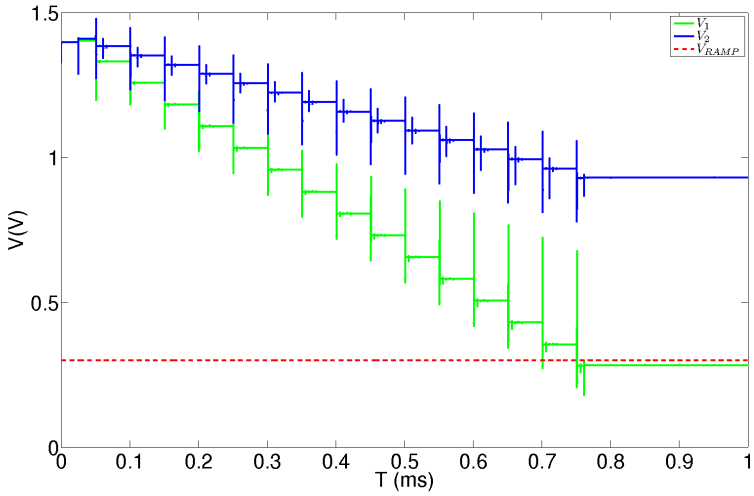

Figure 4.37: Transient simulation of several signal integration phases to show the action of the adaptive comparison avoiding the saturation of V_1 or V_2

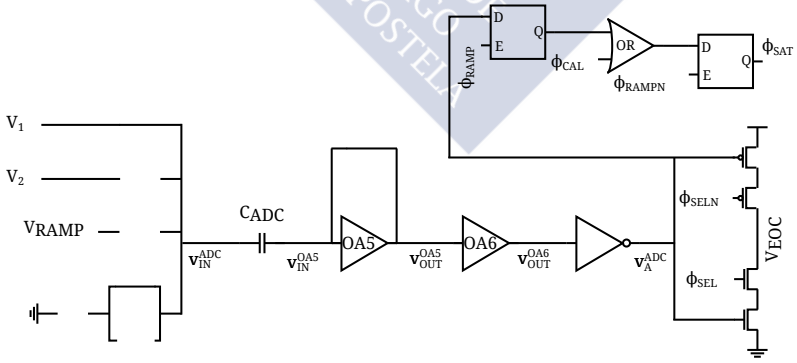

Figure 4.38: Schematic of the ToF pixel in the V_1 comparison step.

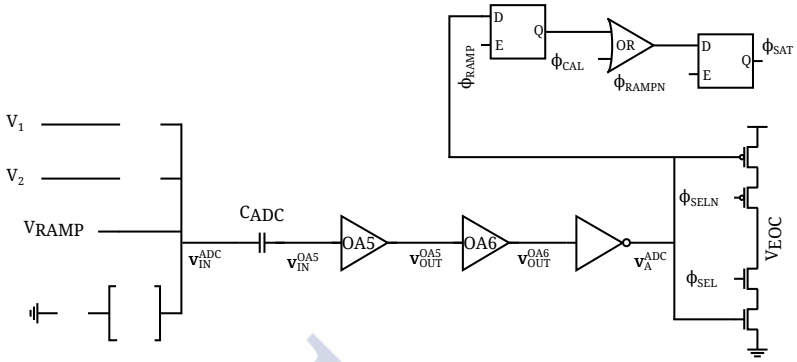

Figure 4.39: Schematic of the ToF pixel in the V_{RAMP} comparison step.

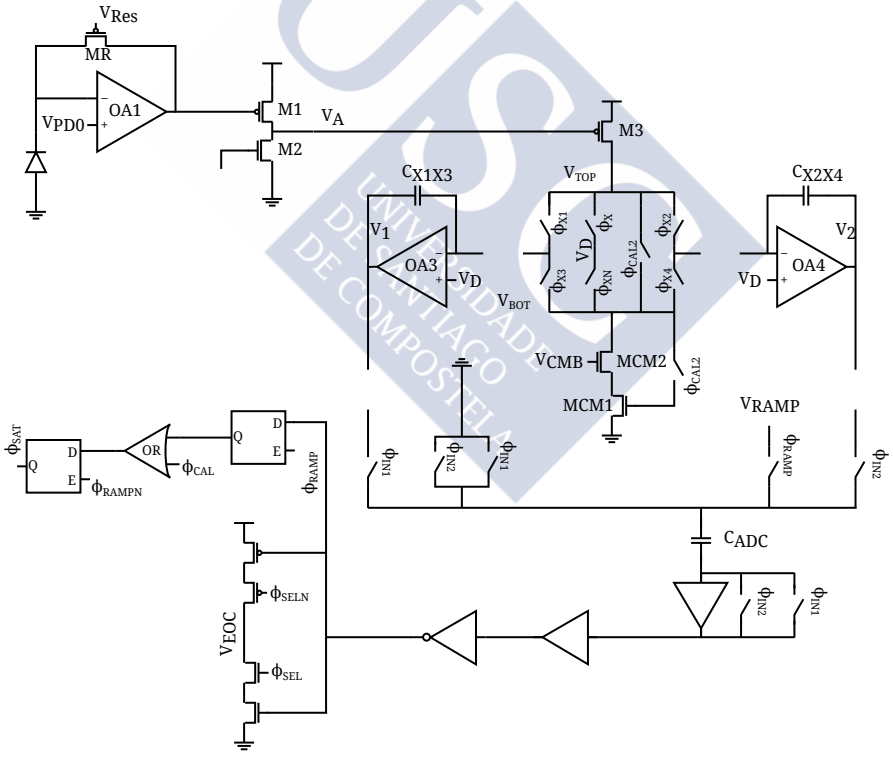

Figure 4.40: Schematic of the ToF pixel when ϕ_{SAT} is OFF.

4.3.3 Analog to Digital Conversion

After the signal integration phases, the digitization of V_1 and V_2 takes place for each pixel. As it was said before, the A/D conversion of these values uses the single slope ADC technique. This needs extra circuitry outside the pixel. Specifically, a memory cell for each voltage to be digitized (two per pixel), a row decoder, a counter, and a Digital-to-Analog-Converter (DAC) to generate the ramp synchronized with the counter. Everything except the DAC was implemented inside the chip. A simplified schematic of the ADC circuit can be seen in Fig. 4.44 and its timing diagrams in Fig. 4.42 and Fig. 4.43. As it can be seen, the DAC controls the values applied to V_{RAMP}, the output of the counter is written to the memory cells and the write enable port of this cell is controlled by V_{EOC} and ϕ_{SEL} for each row.

Typical flow for the A/D conversion of V_1 or V_2 goes as follows. Lets assume that the voltage being converted is V_1. First, the row select signal ϕ_{SEL} for the selected row is activated. Then, V_1 is sampled in C_{ADC}. After that, V_{RAMP} is externally set to 1.8 V and sampled to C_{ADC}. Since at this point $V_1 < V_{RAMP}$, V_{EOC} will saturate to HIGH. The counter then starts to write values in the memory cell, synchronized to the linear variation of V_{RAMP} from 1.8 V to 0 V. At some point V_{RAMP} will be smaller than V_1 and V_{EOC} will turn from HIGH to LOW. Since this signal controls the write enable port of the memory cell, writing in that cell will stop and the digital value for V_1 will be stored. Fig. 4.41 shows a transient simulation where $V_1 = 0.5$ V. As it can be seen, when the voltage of V_{RAMP} falls under this voltage, V_{EOC} goes LOW. This process is done for all the pixels of the row at the same time, but it has to be repeated to make the A/D conversion of V_2, so in total, it has to be performed two times for each row of the pixel array.

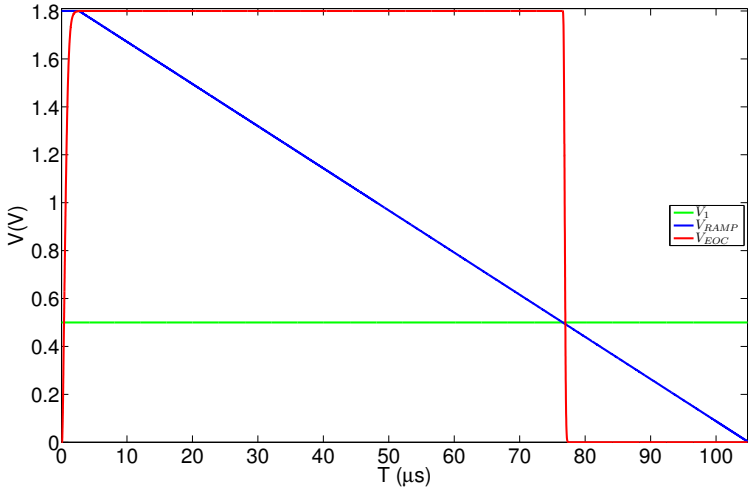

Figure 4.41: Transient simulation showing the single slope ADC process when the voltage to be digitized equals 0.5 V

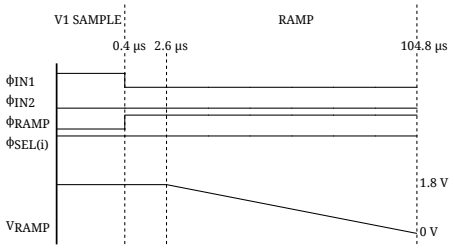

Figure 4.42: Time diagram of V_1 ADC.

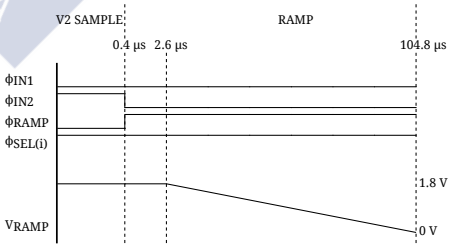

Figure 4.43: Time diagram of V_2 ADC.

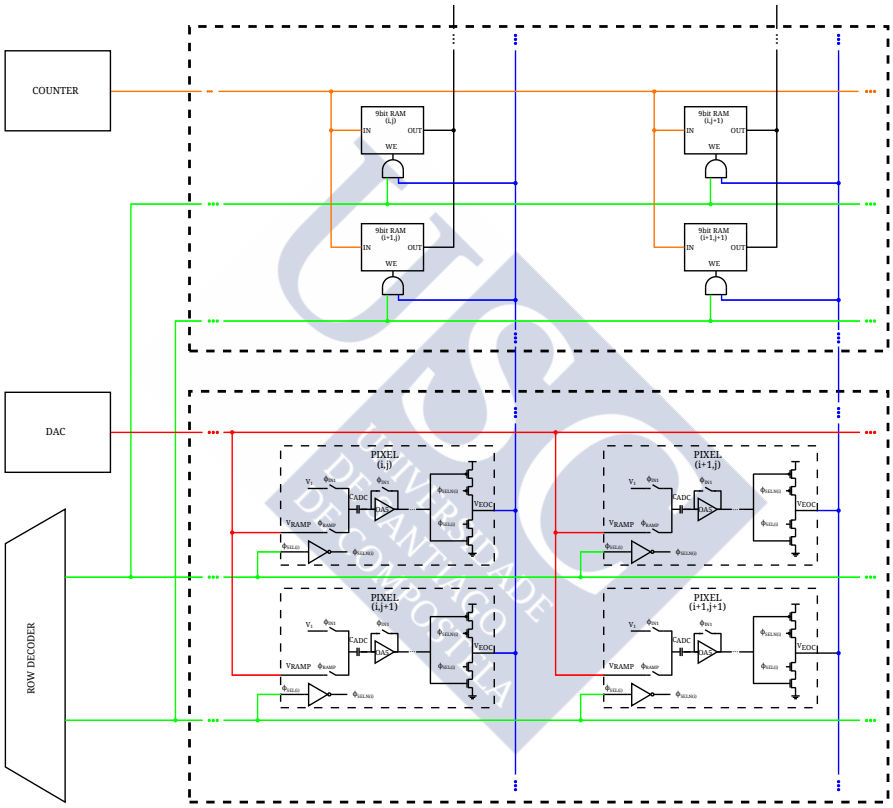

Figure 4.44: Simplified schematic of the single slope ADC.

4.4 Conclusions

This chapter gives a detailed description of the ToF pixel designed. It uses the pulsed PSD-2B technique to perform the distance calculation and includes a circuit to check out the threshold condition in the operation of adaptive number of accumulations. An array of 52×63 of these pixels was fabricated in 0.18 μm standard CMOS technology. The next chapter shows the extra circuitry, outside of the pixel array, included in the chip, the experimental setup used to measure the chip response and the obtained results.

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Chapter 5

Chip Test

An array of 52×63 pixels with the ToF pixel topology presented in Chapter 4 was fabricated in a 0.18 μm Standard CMOS technology. In addition to this array the chip includes a digital frame buffer, row and column decoders, as well as supporting circuitry for the ADC and different control signals in the ToF pixel. To measure the operation of the sensor an experimental setup was designed. This setup includes the Printed Circuit Board (PCB) where the chip is going to be allocated, a laser module to generate the light signals, the lenses to focus the reflected light on the chip and an FPGA to control the process and extract the data from the chip.

The extra circuitry inside the chip is described in Section 5.1 of this chapter. Section 5.2 summarizes the experimental setup used and Section 5.3 shows the obtained experimental results.

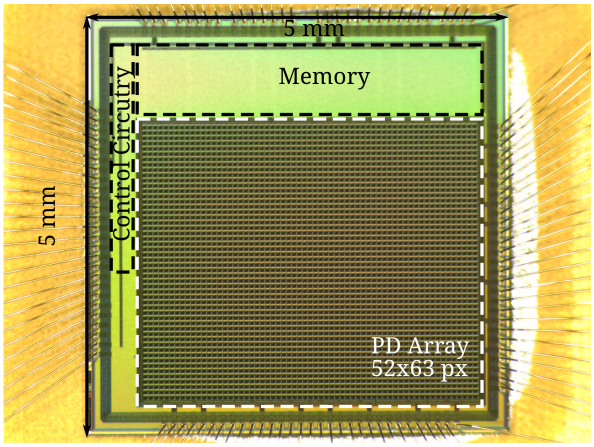

Figure 5.1: ToF chip microphotograph.

5.1 Chip Floorplan

Fig. 5.1 shows the fabricated chip. It has an area of 5 mm^2 where 3.5 mm^2 are occupied by the pixel array. In Fig. 5.2 a schematic with the relation between the different circuit blocks of the chip is shown. The function of each of these blocks is summarized below and, in the rest of this section, these extra circuitry is described in detail.

- Control signal generator: this block handles the correct flow of the measurement steps described in Section 4.3 of Chapter 4. This is achieved with five input signals coming from outside of the chip. In our setup these signals are generated by the FPGA.

- Frame Buffer: an array of digital memories where the values of V_1 and V_2 of each ToF pixel are stored before being sent out of the chip.

- ADC counter: this counter operates synchronized with the voltage ramp used as part of the ADC operation. It is the input to the digital memories of the frame buffer. The clock and reset signal are provided by the FPGA.

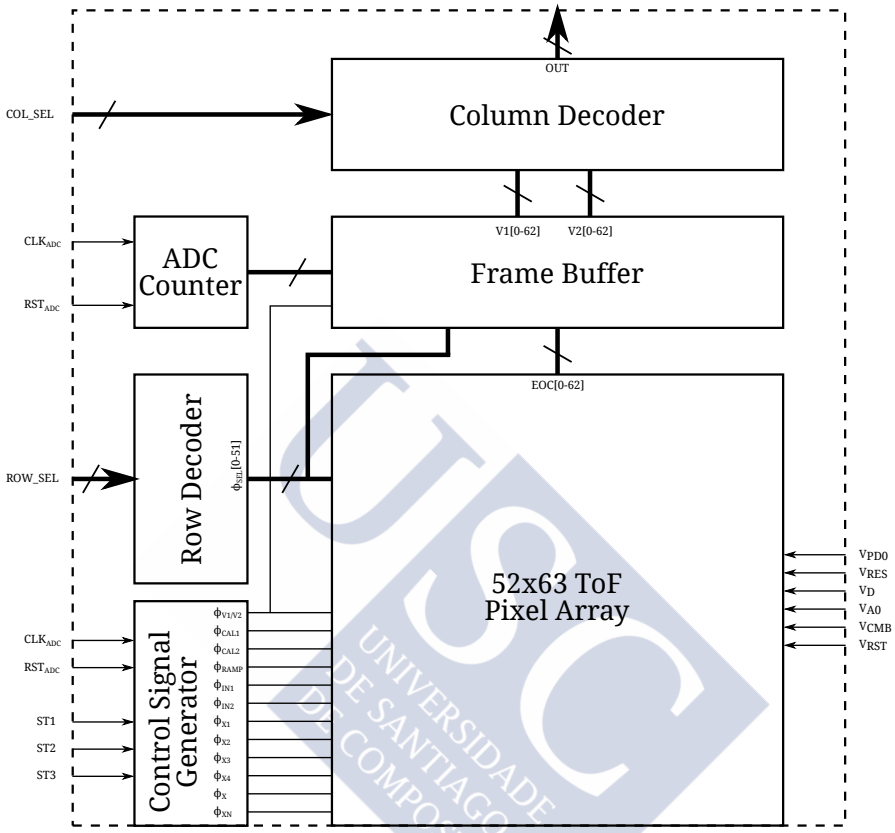

Figure 5.2: ToF chip floorplan.

– Row decoder: this block controls which row is being digitized and read outside of the pixel. The row being selected is controlled by the 6-bit ROW_SEL signal generated by the FPGA.

– Column decoder: this block receives V_1 and V_2 values of an entire row and selects which one is sent outside the chip. As with the row decoder, a 6-bit signal, COL_SEL, coming from the FPGA controls this block.

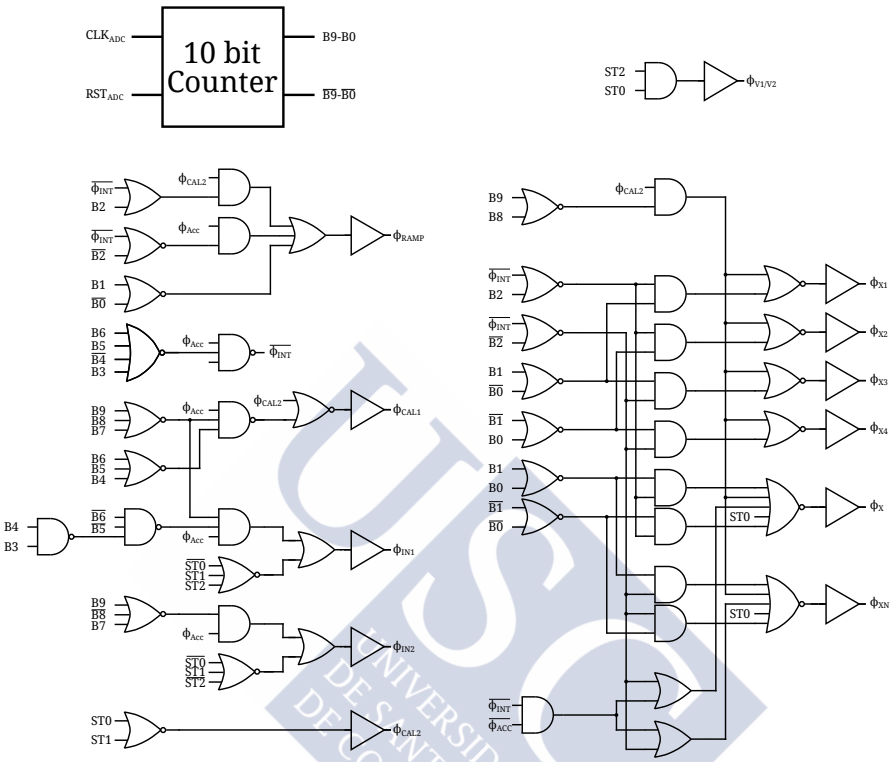

Figure 5.3: Schematic of the control signal generator block.

5.1.1 Control Signal Generator

Fig. 5.3 shows a schematic of the control signal generator. As it can be seen it is composed of a 10-bit counter and combinational logic to generate the control signals for the ToF pixel array. Additional buffers are required due to the large fan-out from the ToF array. The operation described in Section 4.3 is divided in six different states. The selection of the state under execution is externally controlled through 3 signals: ST1, ST2, ST3. Clock and reset signals, RST_{CTRL} and CLK_{CTRL}, are also needed. Both signals are applied to the counter, the first one is an active at LOW synchronous reset, the second is the clock signal.

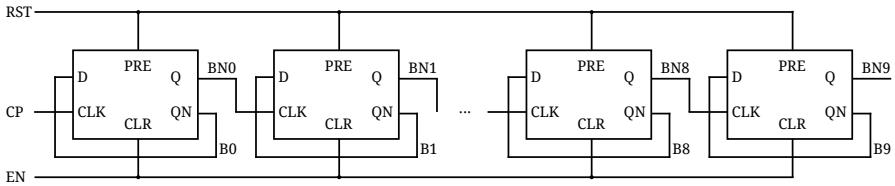

Figure 5.4: Schematic of the 10-bit counter for the control signal generator block.

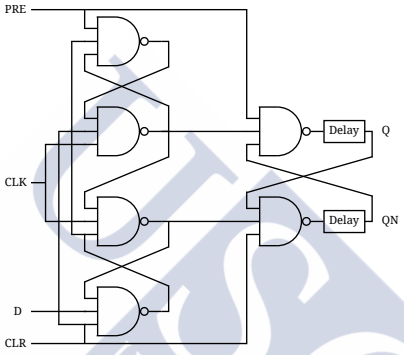

Figure 5.5: Schematic of the latches with delay for the control signal generator block.

For the correct operation of the pixels the control signals ϕ_{X1}, ϕ_{X2}, ϕ_{X3}, ϕ_{X4}, ϕ_X and ϕ_{XN} cannot overlap. To ensure this, the counter is designed to generate non-overlapping signals. The schematic of the counter can be seen in Fig. 5.4. Its latches can be seen in Fig. 5.5. In this figure it can be seen that they include delay circuitry. This ensures that none of the bits from the counter will change before the preceding one finishes its transition.

The six states under which the block operates are described in Table 5.1, together with the measurement phases that are performed in each state and the period of the control clock, T_{CTRL} needed in each state. For example, to perform the reset and calibration phases ST2, ST1 and ST0 must be set to 0 and a period of 50 ns must be used for the clock signal, $\mathrm{CLK_{CTRL}}$. Another important point is that the system is designed so the values of V_2 stored in the frame buffer can be read from outside of the chip while the values of V_1 are being digitized, and

ST2 ST1 ST0	Measurement phases	T_{CTRL}	Total Count Time
000	Reset and calibration	50 ns	51.2 µs
110	Signal integration	50 ns	51.2 µs
001	ADC V_1 sample	-	-
011	ADC V_1 digitization and V_2 output	100 ns	102.4 µs
101	ADC V_2 sample	-	-
111	ADC V_2 digitization and V_1 output	100 ns	102.4 µs

Table 5.1: ST2, ST1 and ST0 code and the measurement step that they perform.

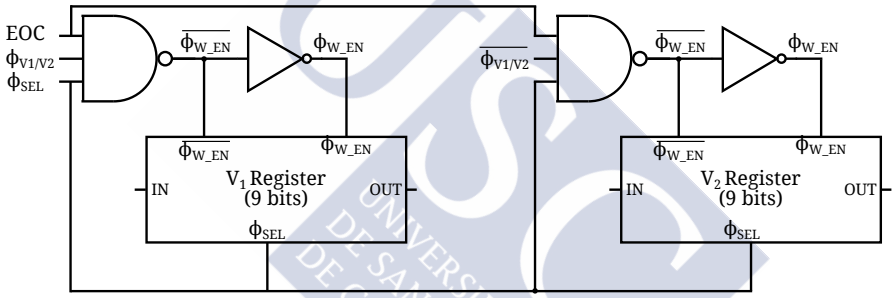

Figure 5.6: Memory element from which the frame buffer is composed.

vice versa. This happens in the control states 011 and 111 respectively.

5.1.2 Frame Buffer

For the distance calculation two values, V_1 and V_2, from each pixel must be digitized. These values are stored in the frame buffer before being sent outside of the chip. This means that the frame buffer is composed of 52×63 elements. Each element is composed of two 9 bits registers and some extra circuitry that controls the writing in the registers, as it can be seen in Fig. 5.6.

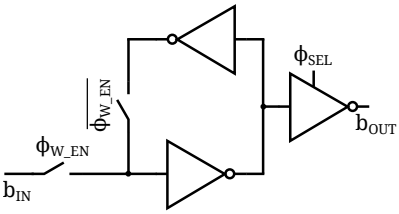

Figure 5.7: Schematic of one bit register.

One bit register is shown in Fig. 5.7. It is controlled with a write enable signal, ϕ_{W_EN}, and a row selection signal, ϕ_{SEL}. This second signal controls a tristate buffer, so only the results from the selected row are outputted to the column decoder.

Extra circuitry is included to generate signal ϕ_{W_EN} of each register. As seen in Fig. 5.6 the write operation in these registers is programmed through signals EOC, which is different for each column of the array, ϕ_{SEL} which is different for each row of the array, and $\phi_{V1/V2}$ that controls if the register which is being written to is a V_1 register or a V_2 register.

5.1.3 ADC Counter

The ADC counter generates the values being written in the digital memories during the ADC phase, as explained in Section 4.3.3. This counter is equal to the one inside the control signal generator, except that it has 9 bits instead of 10 and its latches do not have delay circuits inside, as it is shown in Fig. 5.8. Two external signals, $\mathrm{RST_{ADC}}$ and $\mathrm{CLK_{ADC}}$, control this circuit. The first one is an active at LOW synchronous reset and the second one is the counter's clock.

5.1.4 Row decoder

The digitization of V_1 and V_2 is done row-by-row. A 64-bit row decoder selects one row out of the 53 of the ToF array through signals $\phi_{SEL}(i)$. As it can be seen in Fig. 5.9 this block

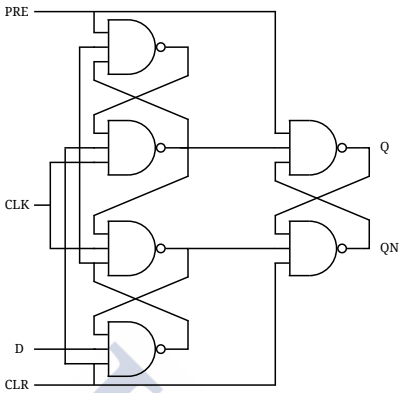

Figure 5.8: Schematic of the latches without delay for the ADC counter.

is implemented as an NOR MOS with pull-up. With this configuration only one row can be selected at a time. A six bit signal, ROW_SEL, makes this selection.

5.1.5 Column decoder

Fig. 5.10 shows the schematic of the column decoder. This block receives the V_1 and V_2 values of an entire row from the frame buffer, represented as $V1_{IN}$ and $V2_{IN}$ in the figure respectively, and selects which one is sent outside the chip using tristate buffers. As it can be seen, it is controlled through a six bit external signal and the control signal $\phi_{V1/V2}$. The first one selects the column of the pixel whose information is going to be sent out of the chip and the second one selects if that information is V_1 or V_2.

5.2 Experimental Set-up

The entire experimental setup for the sensor test can be seen in Fig. 5.11. It is composed of two PCBs, one accommodating the chip and the other the lasers that generate the light signal, the lenses to focus the image on the chip and an FPGA that provides control signal,

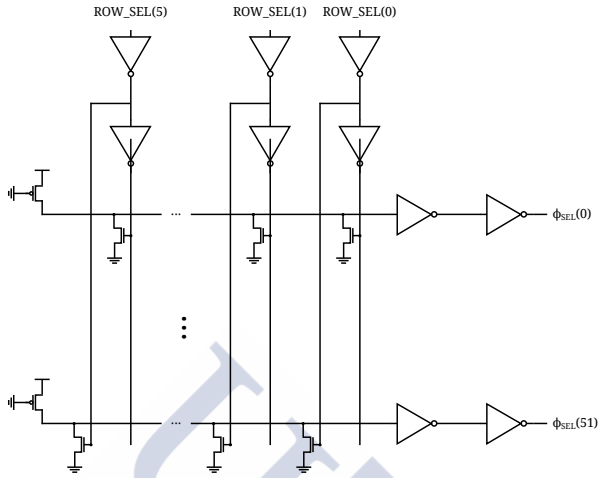

Figure 5.9: Schematic of the row decoder.

read V_1 and V_2 out of the chip to compute the distance measurement. The complete set-up is described below.

5.2.1 Chip PCB

The PCB where the chip is situated is shown in Fig. 5.12. In addition to the chip, it includes all the circuitry to generate the supply and reference voltages for the ToF pixels and a digital-to-analog conversor, DAC, that generates V_{ramp} from a signal sent by the FPGA. This PCB also includes a 40-pins connector to communicate with the FPGA.

5.2.2 Illumination PCB

The light signals are generated by three OSRAM SPL PL90_3 IR lasers. Each one has beam divergences of $\theta_{||} = 9^\circ$ and $\theta_{\perp} = 25^\circ$ and are orientated to avoid overlap between them. In addition to the lasers and their driving circuitry, the PCB where they are mounted includes a voltage regulator that controls the voltage being applied to the lasers and, thus, the light

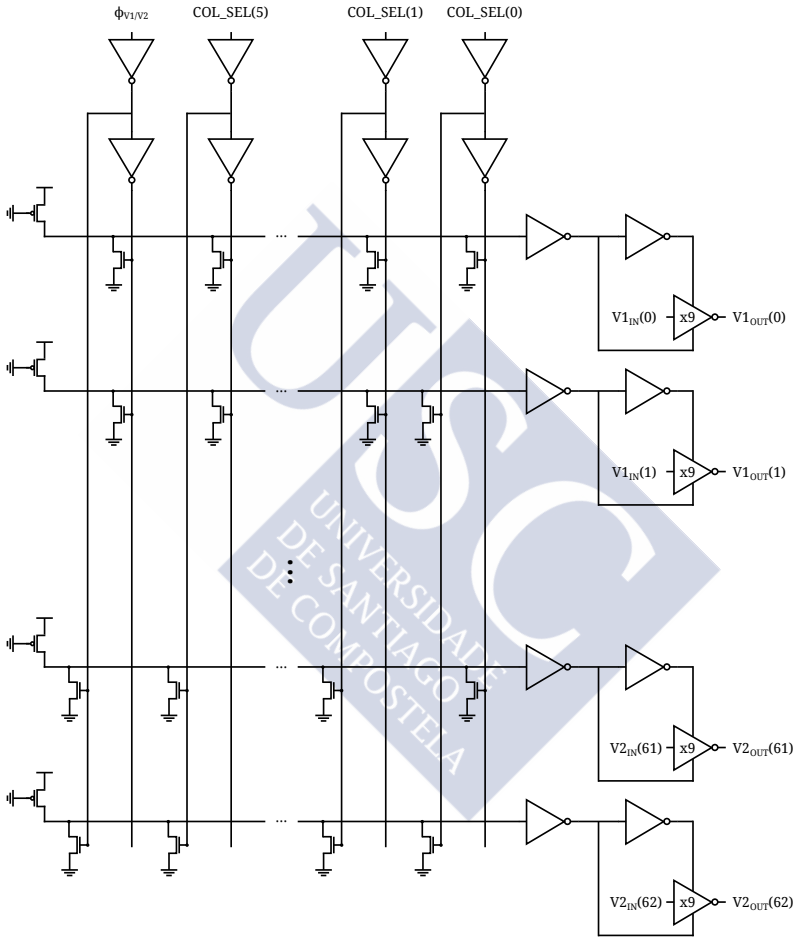

Figure 5.10: Schematic of the column decoder.

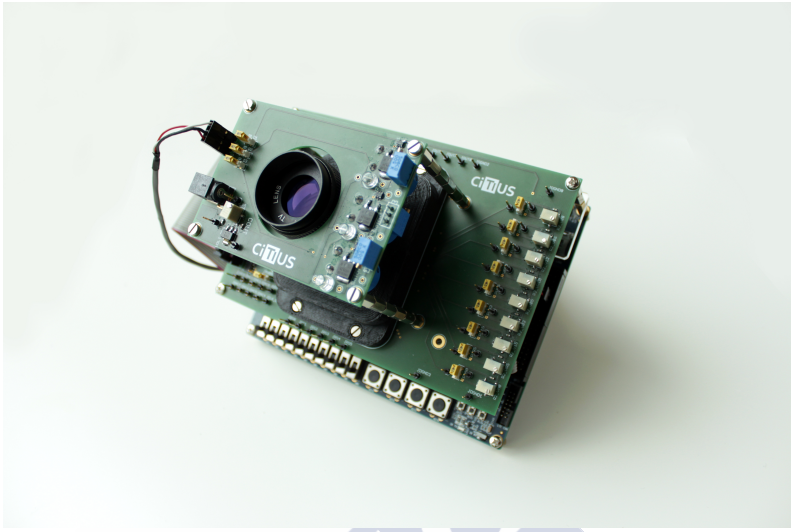

Figure 5.11: Complete experimental setup to test the ToF sensor.

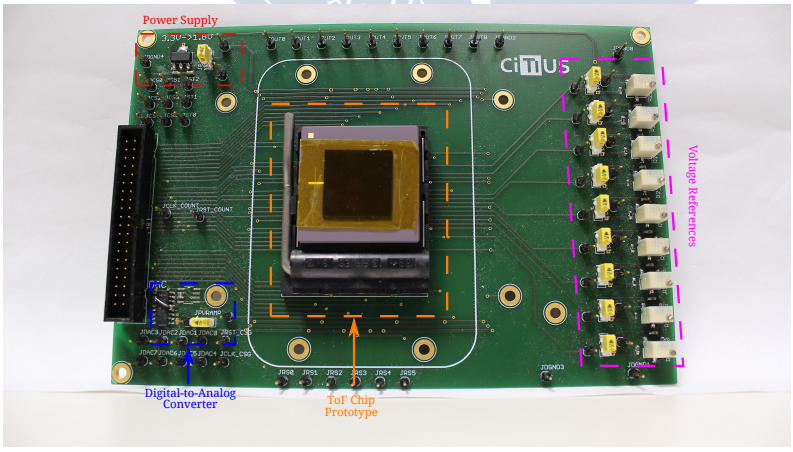

Figure 5.12: Photograph of the chip PCB.

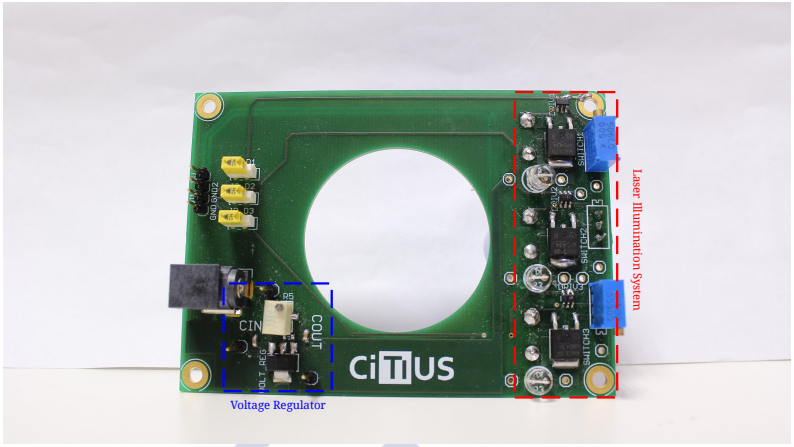

Figure 5.13: Photograph of the Illumination PCB.

power emitted. The complete PCB can be seen in Fig. 5.13.

5.2.3 Lens and Case

The system uses and 35 mm lens system with an F number of 1.7. To support this lens and align it with the sensor a custom 3D printed case was designed. Fig. 5.14 shows both components.

5.2.4 FPGA

The DE1-SoC FPGA development board is used to control the chip, receive V_1 and V_2 values and compute the distance information. The FPGA included in this board is the ALTERA Cyclone V. This device handles all the signals that control the chip, described in Section 5.1, in addition to the data to generate V_{ramp} by the DAC for the ADC conversion of V_1 and V_2. The FPGA also provides the control for the emission of the light signals by the laser module. The development board includes a VGA connector so the distance information can be directly

Figure 5.14: Photograph of the 3D printed case and lenses system.

displayed in a monitor. In this section, the experimental setup used to test the chip has been presented. In the next section, the experimental results will be presented.

5.3 Experimental Results

This section presents the experimental results from the chip test. As these results do not match the expected behavior predicted by the simulations in Chapter 4 an exhaustive validation has been performed in order to identify the possible causes of this misbehavior. Section 5.3.1 describes a design error regarding the reset of the pixel integrators identified during the chip measurement. This error can be fixed with extra measurement steps. In addition to this, the pixel response to background and light pulses is not the correct one, but experiments were performed to locate where the error is in the chip. Section 5.3.2 shows the measured results of the response of the ToF pixel with the background light. Section 5.3.3 does the same for

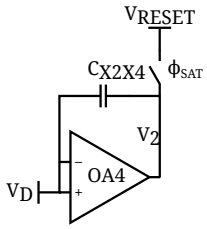

Figure 5.15: Schematic of the reset circuitry for the storage integrators.

the light signal pulses. The results presented in this section are summarized in Section 5.4.

In the normal operation of the ToF sensor the light pulses reaching it are first reflected from the target. To avoid the dependence of the pulse's light power with the reflectivity of the target and its distance to the sensor, in all the results presented in this section these pulses are aimed directly at the sensor. Unless stated otherwise, the measurements presented were recorded with a background light power typical of indoor scenarios.

5.3.1 Reset Topology

Our sensor calculates the distance to the target using the indirect PSD-2B technique with the equation presented in Table 2.2 and repeated here for convenience:

$$L = \frac{c}{2} T_p \frac{V_{x2} - V_{x4}}{(V_{x1} - V_{x3}) + (V_{x2} - V_{x4})} \tag{5.1}$$

In our pixel, voltages $V_{x1} - V_{x3}$ and $V_{x2} - V_{x4}$ are stored in the integrators nodes V_1 and V_2, respectively, as explained in Section 4.2.4. For each frame, before the integration of pulses begins, the integrators must be reset. Fig. 5.15 shows the circuit used to reset the V_2 storage integrator. The circuit for the V_1 integrator is identical. As it can be seen, it uses a switch to fix V_1 and V_2 to an external selectable value. The operation of this circuit is incorrect, because it attacks the output of amplifiers OA3 and OA4 without shunting both nodes of the storage capacitances, so the integrators are not correctly reset.

Because of this error, the result of the reset operation is different for every pixel. To study how this error affects the pixel performance, the reset voltage of the ToF pixel array was measured for 50 frames and an average and standard deviation for each pixel was calculated. Fig. 5.16 shows the obtained results for an entire row. Since these data do not show variation from one row to another, the results presented in Fig. 5.16 can be considered as the typical for the entire array. As it can be seen, the reset average values vary from 1.2 V to 1.7 V and have a standard deviation below to 200 mV. From these data it can be concluded that the inconsistency of reset value from pixel to pixel and frame to frame is too large to be treated as a systematic error and it has to be taken into account. A proposed solution is to digitize the reset value of V_1 and V_2 before the beginning of the integration of the pulses. This extra operation would reduce the frame rate of the system, since two extra digitizations per pixel must to be performed. It can also reduce the dynamic range of V_1 and V_2, and thus their SNR, since originally these voltage were designed to be reset to 1.4 V and in practice some of them reset to lower values. However, the distance measurement should not be affected by this error besides these two consequences.

5.3.2 Sensor response to background light

From the simulations shown in Chapter 4 the pixel response should be immune to the background up to 20 klux. This is, V_1 and V_2 should not change from the reset value if no light pulses are emitted. To evaluate this, 50 frames were recorded without the emission of light pulses. Fig. 5.17 shows these data for one pixel together with the reset values for comparison. These measurements were taken with a maximum number of accumulations of N_{acc}^{Max} =150. As it can be seen the final voltages clearly differ from the reset ones.

One important thing about this result is that the standard deviations of the final V_1 and V_2 values are significantly lower than in the reset voltages. For the pixel data shown in Fig. 5.17, the standard deviation after the 150 accumulations is around 25 mV while for the reset is

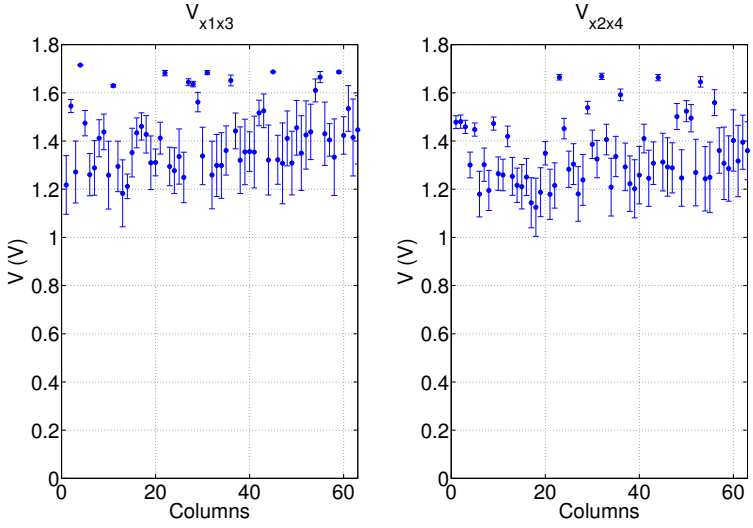

Figure 5.16: Experimental results for the reset operation for the pixels of an entire row after averaging 50 frames.

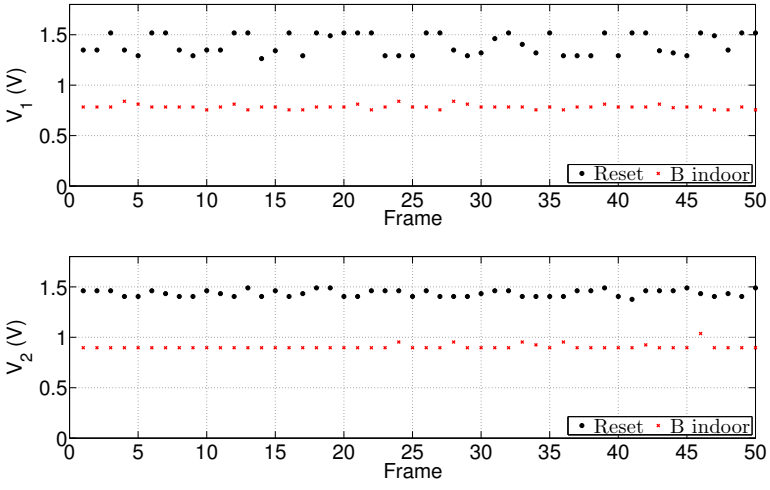

Figure 5.17: Experimental results of the reset and final voltages without light signal emission.

around 100 mV. This suggests a systematic effect affecting the measurement and not some random noise.

To check if the difference between the reset and final values is influenced by the background light levels or the maximum number of accumulations two other measurements were performed. In the first case N_{acc}^{Max} was not modified and the measurement was done in total darkness conditions while in the second case the same level of illumination as in Fig. 5.17 but with a maximum number of accumulations of N_{acc}^{Max} =500 was used. The results obtained for one pixel are shown in Fig. 5.18. These results suggest that the V_1 and V_2 values at which the pixel converges do not depend on the background light level or the number of accumulations performed and is, instead, intrinsic for each pixel. The fact that the the final values of V_1 and V_2 do not show a dependence with the number of accumulations dismisses the option that effects like charge injection or clock feedthrough in the storage capacitances are the ones affecting the measurement.

The results presents in Fig. 5.17 and Fig. 5.18 were for one particular pixel, but a comparison with the results of the rest of the array shows that all of them behave in the same way, except for the fact that the final V_1 and V_2 vary from one pixel to another in what it seems a random way.

5.3.3 Sensor response to light pulses

The same experiments performed to evaluate the effect of the background on the ToF pixels were performed to understand how they are affected by the light signals. To discard any effect produced by the lenses system the experiment was executed with and without lenses. As in the experiments presented in the previous section, the results for 50 frames were recorded. Fig. 5.19 shows the results for one pixel. In this figure it can be seen that the response of the pixel when the light pulses are emitted is clearly different from the situation of only the background light illuminating the pixel. It can also be seen that when the lenses are used, the

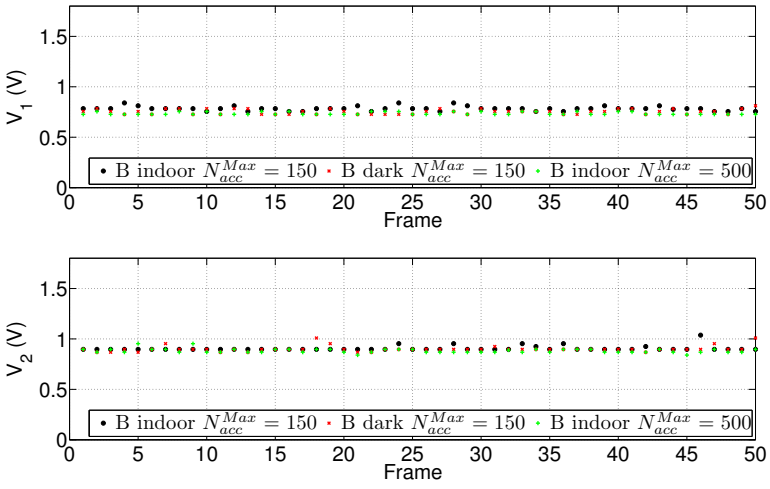

Figure 5.18: Experimental results of the final voltages without light signal emission for different background light and N_{acc} situations.

pixel response to the light signals is reduced. The reason for this is, first, that since no image is being obtained, the correct focus of the lenses in the array is not feasible and, secondly, because the lenses are partially opaque to the infrared light.

The simulations from Chapter 4 show that, with respect to the light pulses, V_1 and V_2 values should be proportional to the number of accumulations and the light power of these pulses. As before, new experiments were performed to verify this. These experiments were performed without lenses and the results of one representative pixel can be seen in Fig. 5.20. The data measured show that final values for V_1 and V_2 do not depend on the number of accumulations performed. With respect to the dependence of these values with the light power, V_2 shows no dependence at all while V_1 does depend on it.

Another possible parameter that should affect the pixel response is the width of the light pulses, T_p. Simulations show that V_1 and V_2 should be proportional to this parame-

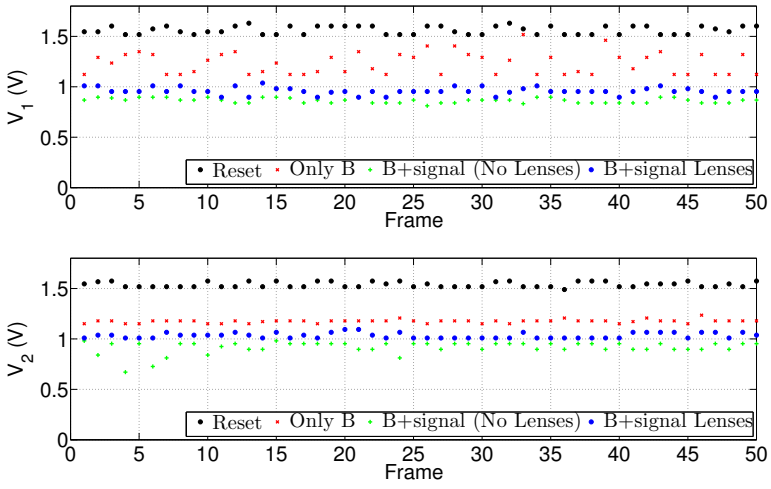

Figure 5.19: Experimental results of the final voltages with light signal emission with and without lenses.

ter. Fig. 5.21 show the measurement of 50 frames for one pixel comparing V_1 and V_2 final results for different values of T_p. This measurements were performed with a maximum number of accumulations of $N_{acc}^{Max} = 150$. As it can be seen the experimental results differ from the simulated ones also in this case, since V_1 and V_2 show no variation even if T_p is doubled.

The experiments presented in the last section show that, without light pulses, V_1 and V_2 tend to converge to a voltage, independent of the background light or the number of accumulations and different for each pixel, but always constant for any given pixel. However, if light pulses are emitted this is not the case for all the pixels of the array. Fig. 5.22 shows the same results as Fig. 5.19 but for another pixel. As it can be seen, for this pixel, when the lenses are attached to the system, a lot of values of V_1 and V_2 saturate to a voltage near 1.8 V. The pixels for which this happens are not randomly distributed, as it can be seen accumulating in one plot the pixel response to the light pulses for all the array. Fig. 5.23 shows these data for V_1 and 50 frames. The pixels for which the saturation occurs draw a circumference around the

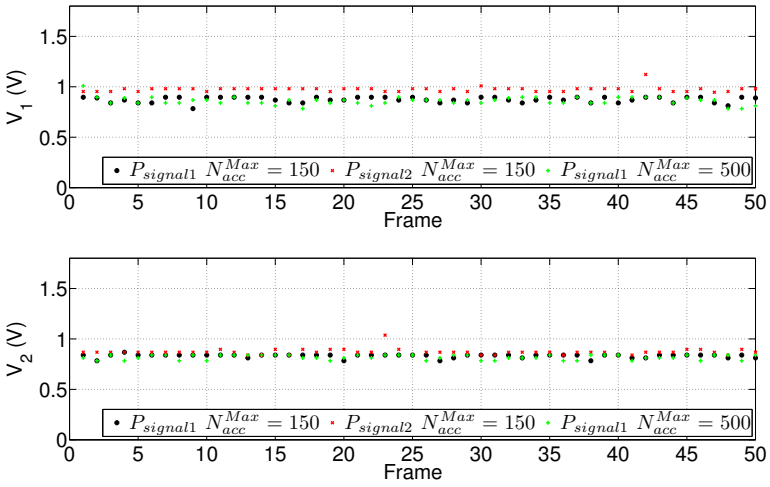

Figure 5.20: Experimental results of the final voltages with light signal emission for different background light and N_{acc} situations.

ones for which it do not. Moving the lenses a little changes the position of this circle, which suggest that the problem is due to some focusing effect of the lenses.

Experimental measurements with the laser module situated at different distances from the sensor were performed to test if, despite the problems described in this chapter, the ToF array is able to calculate the T_{oF} and thus, the distance. Unfortunately, the effect of these problems is too big and the system is not capable of calculating the distance to the target.

5.4 Experimental Results Conclusion

Section 5.3.1 shows that an error was made in the design of the reset circuit for the integrators. This error prevents the pixels of the array to reset to an externally selectable value and, instead, they all reset to different values. The effect of this error can be minimized by

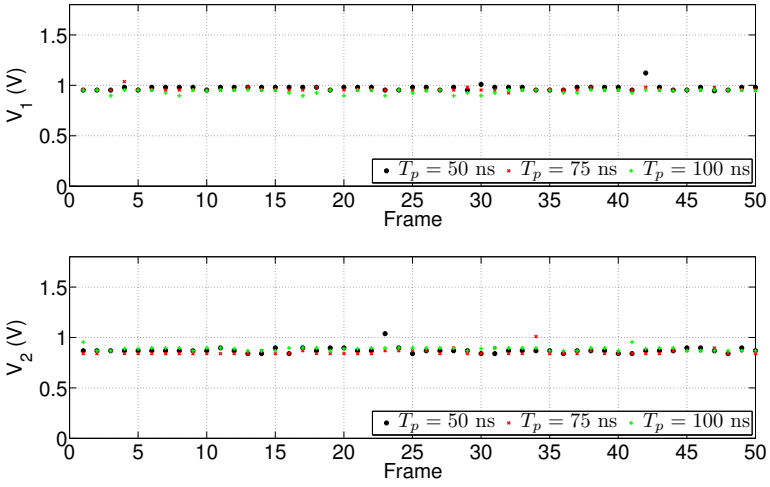

Figure 5.21: Experimental results showing the typical response of V_1 and V_2 for one pixel for T_p =50 ns, 75 ns and 100 ns.

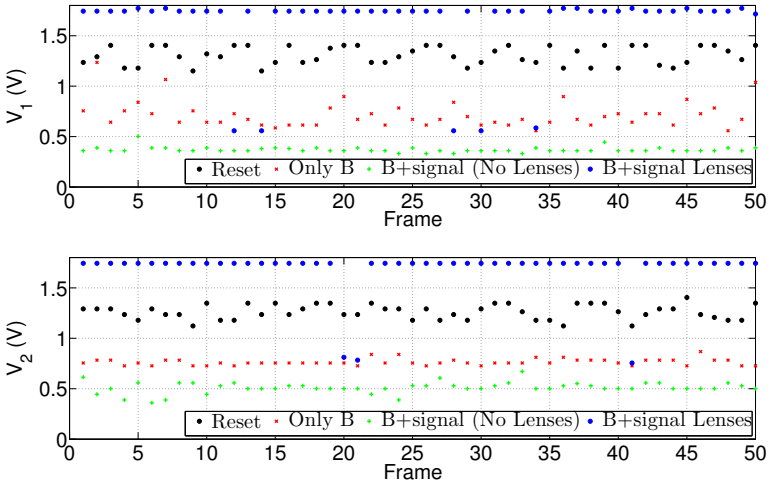

Figure 5.22: Experimental results of the final voltages with light signal emission with and without lenses.

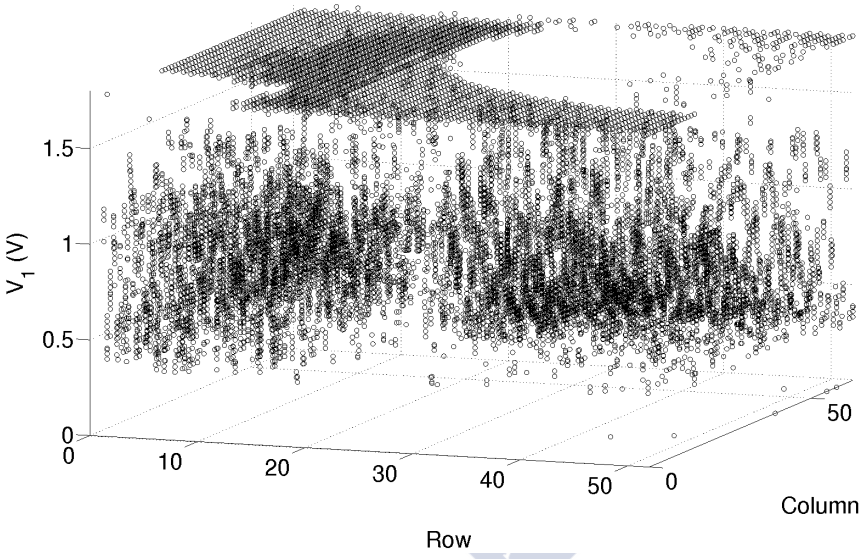

Figure 5.23: Experimental results of V_1 voltages of the entire array for the system with lenses.

digitizing the reset values before starting the integration of pulses.

Simulations from Chapter 4 show that V_1 and V_2 should not change if light pulses are not emitted and their final values should be proportional to the number of accumulations performed and the power and width of the light signals. Despite this, the experimental results presented in Section 5.3.2 and Section 5.3.3 show that V_1 and V_2 voltages in fact change without the emission of light pulses and their final value is not proportional to the number of accumulations performed, the width of the emitted light pulses or even, in the case of V_2, to their light power.

The most likely reason for this is an overlap between some of the control signals ϕ_{X1}, ϕ_{X2}, ϕ_{X3}, ϕ_{X4}, ϕ_X and ϕ_{XN}. If ϕ_{X1} and ϕ_{X2} or ϕ_{X3} and ϕ_{X4} overlap, charge sharing between the storage capacitances will happen every time a pulse is integrated. Also, if ϕ_X or ϕ_{XN} overlap with any of the other four signals mentioned charge will be lost every time a pulse is integrated. If this happens V_1 and V_2 will converge to a given value after a certain number of pulses. This problem could be produced by an incorrect design of the digital buffers of the control signal generator block, explained in Section 5.1.1 of this chapter. This problem is similar to the one presented in [55] where the charge sharing with the parasitic capacitances made the output voltage of the ToF sensor converge to a certain value.

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Conclusions

In this work a novel Time-of-Flight pixel topology designed in standard CMOS technology has been presented. This pixel includes circuitry to deal with the background light before the storage of the light signal and performs the adaptive number of accumulations technique to avoid its saturation, making it very suitable to work under large background light conditions.

First, different techniques to perform the ToF operation to measure distances were introduced. The study presented in this work is limited to indirect ToF approaches. These techniques were then compared in terms of the effect of shot and thermal noise. For this comparison realistic parameters for the power of the signal and background light and for the number of accumulations performed in each frame were calculated. Regarding this last parameter, the adaptive number of accumulations technique was presented. This technique allows to use the optimal number of accumulations for each pixel of an array by controlling this number individually for each pixel. This way the risk of pixel saturation is minimized, maximizing SNR. The comparison between techniques allowed us to select the best ToF technique to be used. This technique was the phase shift determination with two background subtractions (PSD-2B).

With the selected technique, the most straightforward way to implement the ToF operation is to use a pinned photodiode with several transmission gates and perform the demodulation at device level. In standard CMOS technology this topology cannot be performed without

violating some layout rules. The next step of this work was to study the feasibility of fabricating this device in standard CMOS technologies, even at the cost of violating this rules. The study was performed at device level through simulations with the ATLAS software from Silvaco. The parameters studied to evaluate the performance of the structure were the dark current, the noise introduced by the reset transistor and the transmission velocity of the photocharges. The simulations obtained and the analysis developed from them show that this structure fabricated in standard CMOS technologies is not suited for the implementation of indirect ToF sensors. Either the device is fabricated in alternative technologies, like CIS, or simple photodiodes are used as photosensing devices and extra circuitry is added to perform the demodulation of the light signal.

Since the objective of this work was to develop the sensor in standard CMOS technologies the later approach was taken. A ToF pixel performing the PSD-2B technique was designed with a total size of 62×62 μm^2 and a fill-factor of 65%. The photocurrent generated by the background and light signals in the photodiode is amplified before integration. Because of speed constraints and the low levels of the photogenerated current this cannot be done in a single step. First the photocurrent is converted in a voltage signal and amplified. After that the signal is converted back into a current and the integrations needed for the ToF calculation are performed. During the amplifying state the DC component of the signal, which is generated by the background light, is removed. Thanks to this operation the pixel can work on ambients with up to 20 klux of background light. After each light pulse is integrated the pixel compares the voltages in the storage capacitances with an externally selectable one, to verify they are close to saturation. If this is the case the pixel will stop accumulating until the end of the frame. In this way the saturation of that particular pixel is avoided while the rest of the pixels can continue with the pulse accumulations.

An array of 52×63 of this designed pixels was fabricated in 0.18 μm CMOS standard technology. In addition to this array the chip includes control circuitry and the necessary electronics to perform the analog-to-digital conversion. An experimental setup to test the

chip was also designed. This setup includes the PCB where the chip is mounted and where all the needed reference voltages are generated, another PCB for the lasers that generate the light signal and an FPGA to provide control signals to the entire system.

With this experimental set-up measurements were taken to asses the performance of the chip. An error in the reset circuit of the storage capacitances was discovered. This error prevents the pixels to reset to the nominal values and, instead, the reset value of each pixel varies from frame to frame. This forces to carry out two extra digitization at the beginning of each frame to measure the real reset value of each pixel. In addition to this, the final voltages of each pixel tend to converge to a value that is not related with T_{oF}. Through experimental measurements it has been inferred that this voltage is independent of the background light reaching the pixel, the number of accumulations performed, the width of the light pulses employed and, even, their light power. The most probable explanation for this misbehavior is an overlapping of the control signals that direct the integration measurements for the ToF calculation.

Future Work

The experimental results presented in this work showed a series of failures in the fabricated chip. A second chip is going to be fabricated, correcting the reset of the storage capacitances problem and adding extra test circuitry to test if the differences between simulations and experimental results come from an overlap in the control signals. In addition to this, several modifications to improve the performance of the pixel will be addressed. In particular the front-end circuitry of the pixel where the photocurrent is converted to a voltage, amplified and converted back to a current can degrade the signal, so another topology based on a band pass filter to eliminate part of the shot noise will be used.

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Appendix A

Thermal Noise Related Distance Error Demonstration

To calculate the effect of the thermal noise in the distance measurement, first, the voltage generated during each x_i measurement, V_{xi}, must be calculated as:

$$V_{xi} = \frac{q\ QE}{C_{storage}} x_i \tag{A.1}$$

applying this equation to (2.2), (2.5), (2.7), (2.9) and (2.11). For the modulated ToF technique:

$$V_{x1} = \frac{q\ QE}{C_{storage}} x_1 = \frac{q\ QE}{C_{storage}} \left(\frac{N_{acc} B\tilde{T}}{4} + \frac{\sqrt{2} A\tilde{T} N_{acc}}{2\pi} sin(\phi) \right) \tag{A.2a}$$

$$V_{x2} = \frac{q\ QE}{C_{storage}} x_2 = \frac{q\ QE}{C_{storage}} \left(\frac{N_{acc} B\tilde{T}}{4} + \frac{\sqrt{2} A\tilde{T} N_{acc}}{2\pi} cos(\phi) \right) \tag{A.2b}$$

$$V_{x3} = \frac{q\ QE}{C_{storage}} x_3 = \frac{q\ QE}{C_{storage}} \left(\frac{N_{acc} B\tilde{T}}{4} - \frac{\sqrt{2} A\tilde{T} N_{acc}}{2\pi} sin(\phi) \right) \tag{A.2c}$$

$$V_{x4} = \frac{q\ QE}{C_{storage}} x_1 = \frac{q\ QE}{C_{storage}} \left(\frac{N_{acc} B\tilde{T}}{4} - \frac{\sqrt{2} A\tilde{T} N_{acc}}{2\pi} cos(\phi) \right) \tag{A.2d}$$

The same way, for the PSD-1B, the accumulated charged for each x_i is:

$$V_{x1} = \frac{q\ QE}{C_{storage}} x_1 = \frac{q\ QE\ N_{acc}}{C_{storage}} \left[BT_p + A\left(T_p - T_{oF}\right) \right] \tag{A.3a}$$

$$V_{x2} = \frac{q\ QE}{C_{storage}} x_2 = \frac{q\ QE\ N_{acc}}{C_{storage}} \left(BT_p + AT_{oF} \right) \tag{A.3b}$$

$$V_{x3} = \frac{q\ QE}{C_{storage}} x_3 = \frac{q\ QE\ N_{acc}}{C_{storage}} BT_p \tag{A.3c}$$

And for the PSD-2B technique:

$$V_{x1} = \frac{q\ QE}{C_{storage}} x_1 = \frac{q\ QE\ N_{acc}}{C_{storage}} \left[BT_p + A\left(T_p - T_{oF}\right) \right] \tag{A.4a}$$

$$V_{x2} = \frac{q\ QE}{C_{storage}} x_2 = \frac{q\ QE\ N_{acc}}{C_{storage}} \left(BT_p + AT_{oF} \right) \tag{A.4b}$$

$$V_{x3} = \frac{q\ QE}{C_{storage}} x_3 = \frac{q\ QE\ N_{acc}}{C_{storage}} BT_p \tag{A.4c}$$

$$V_{x4} = \frac{q\ QE}{C_{storage}} x_4 = \frac{q\ QE\ N_{acc}}{C_{storage}} BT_p \tag{A.4d}$$

Finally, for the MDSI-1B and MDSI-2B techniques, the integrated charges are summarized in (A.5) and (A.6), respectively:

$$V_{x1} = \frac{q\ QE}{C_{storage}} x_1 = \frac{q\ QE\ N_{acc}}{C_{storage}} \left[BT_p + A\left(T_p - T_{oF}\right)\right] \tag{A.5a}$$

$$V_{x2} = \frac{q\ QE}{C_{storage}} x_2 = \frac{q\ QE\ N_{acc}}{C_{storage}} \left(2BT_p + AT_p\right) \tag{A.5b}$$

$$V_{x3} = \frac{q\ QE}{C_{storage}} x_3 = \frac{q\ QE\ N_{acc}}{C_{storage}} BT_p \tag{A.5c}$$

$$V_{x1} = \frac{q\ QE}{C_{storage}} x_1 = \frac{q\ QE\ N_{acc}}{C_{storage}} \left[BT_p + A\left(T_p - T_{oF}\right)\right] \tag{A.6a}$$

$$V_{x2} = \frac{q\ QE}{C_{storage}} x_2 = \frac{q\ QE\ N_{acc}}{C_{storage}} \left(2BT_p + AT_p\right) \tag{A.6b}$$

$$V_{x3} = \frac{q\ QE}{C_{storage}} x_3 = \frac{q\ QE\ N_{acc}}{C_{storage}} BT_p \tag{A.6c}$$

$$V_{x4} = \frac{q\ QE}{C_{storage}} x_4 = \frac{q\ QE\ N_{acc}}{C_{storage}} 2BT_p \tag{A.6d}$$

Replacing x_i with V_{xi} for each ToF technique we obtain:

- Modulated: $L_{Mod} = \frac{c}{2}\frac{T}{2\pi}\text{atan}\frac{V_{x3}-V_{x1}}{V_{x4}-V_{x2}}$
- PSD-1B: $L_{PSD-1B} = \frac{c}{2}T_p\frac{V_{x2}-V_{x3}}{(V_{x1}-V_{x3})+(V_{x2}-V_{x3})}$
- PSD-2B: $L_{PSD-2B} = \frac{c}{2}T_p\frac{V_{x2}-V_{x4}}{(V_{x1}-V_{x3})+(V_{x2}-V_{x4})}$
- MDSI-1B: $L_{MDSI-1B} = \frac{c}{2}T_p\frac{V_{x2}-V_{x1}-V_{x3}}{V_{x2}-2V_{x3}}$
- MDSI-2B: $L_{MDSI-2B} = \frac{c}{2}T_p\frac{(V_{x2}-V_{x4})-(V_{x1}-V_{x3})}{V_{x2}-V_{x4}}$

Taking into account that the variance of the thermal noise for each V_{xi} value is:

$$(\delta V_{xi})^2 = \frac{N_{acc}kT_{emp}}{C_{storage}} \tag{A.7}$$

error propagation can be applied to the above equations to calculate the effect of the thermal noise in the distance measurement. For the modulated case, applying error propagation gives:

$$\Delta L_{Mod} = \sqrt{\left(\frac{\partial L_{Mod}}{\partial V_{x1}}\right)^2 \delta V_{x1}^2 + \left(\frac{\partial L_{Mod}}{\partial V_{x2}}\right)^2 \delta V_{x2}^2 + \left(\frac{\partial L_{Mod}}{\partial V_{x3}}\right)^2 \delta V_{x3}^2 + \left(\frac{\partial L_{Mod}}{\partial V_{x4}}\right)^2 \delta V_{x4}^2} \tag{A.8}$$

where each of the partial derivatives is:

$$\frac{\partial L_{Mod}}{\partial V_{x1}} = \frac{c}{2}\frac{T}{2\pi}\frac{-(V_{x4}-V_{x2})}{(V_{x3}-V_{x1})^2+(V_{x4}-V_{x2})^2} \tag{A.9a}$$

$$\frac{\partial L_{Mod}}{\partial V_{x2}} = \frac{c}{2}\frac{T}{2\pi}\frac{(V_{x3}-V_{x1})}{(V_{x3}-V_{x1})^2+(V_{x4}-V_{x2})^2} \tag{A.9b}$$

$$\frac{\partial L_{Mod}}{\partial V_{x3}} = \frac{c}{2}\frac{T}{2\pi}\frac{(V_{x4}-V_{x2})}{(V_{x3}-V_{x1})^2+(V_{x4}-V_{x2})^2} \tag{A.9c}$$

$$\frac{\partial L_{Mod}}{\partial V_{x4}} = \frac{c}{2}\frac{T}{2\pi}\frac{-(V_{x3}-V_{x1})}{(V_{x3}-V_{x1})^2+(V_{x4}-V_{x2})^2} \tag{A.9d}$$

Applying (A.2), (A.7) and (A.9) into (A.8) gives:

$$\Delta L_{Mod} = \frac{c}{2}\frac{T}{2\pi}\frac{\sqrt{2}}{\sqrt{\left(\frac{qQE}{C_{storage}\frac{\sqrt{2}A\hat{I}N_{acc}}{\pi}}\right)^2(sin^2\phi+cos^2\phi)}}\sqrt{\frac{N_{acc}kT_{emp}}{C_{storage}}} \tag{A.10}$$

Which, simplified gives:

$$\Delta L_{Mod} = \frac{c}{2}\frac{1}{2qQE\,A}\sqrt{\frac{C_{storage}kT_{emp}}{N_{acc}}} \tag{A.11}$$

For the rest of the ToF techniques this calculation can be repeated obtaining the results depicted in Table 2.2.

Appendix B

Maximum Charge Integration for Every ToF Technique Demonstration

The charge generated during each x_i measurement, Q_{xi}, can be calculated as:

$$Q_{xi} = q\ QE\ x_i \tag{B.1}$$

Applying this equation to (2.2), (2.5), (2.7), (2.9) and (2.11) the charge integrated every for every x_i measurement can be calculated. For the modulated ToF technique:

$$Q_{x1-x3} = q\ QE\,(x_1 - x_3) = qQEN_{acc}\frac{\sqrt{2}A\tilde{T}}{\pi}cos\,(\phi) \tag{B.2a}$$

$$Q_{x2-x4} = q\ QE\,(x_2 - x_4) = qQEN_{acc}\frac{\sqrt{2}A\tilde{T}}{\pi}sin\,(\phi) \tag{B.2b}$$

The same way, for the PSD-1B, the accumulated charged for each x_i is:

$$Q_{x1} = q\ QE\ x_1 = q\ QE\ N_{acc}\left[BT_p + A\left(T_p - T_{oF}\right)\right] \tag{B.3a}$$

$$Q_{x2} = q\ QE\ x_2 = q\ QE\ N_{acc}\left(BT_p + AT_{oF}\right) \tag{B.3b}$$

$$Q_{x3} = q\ QE\ x_3 = q\ QE\ N_{acc}BT_p \tag{B.3c}$$

And for the PSD-2B technique:

$$Q_{x1-x3} = q\ QE\left(x_1 - x_3\right) = q\ QE\ N_{acc}A\left(T_p - T_{oF}\right) \tag{B.4a}$$

$$Q_{x2-x4} = q\ QE\left(x_2 - x_4\right) = q\ QE\ N_{acc}AT_{oF} \tag{B.4b}$$

Finally, for the MDSI-1B and MDSI-2B techniques, the integrated charges are summarized in (B.5) and (B.6), respectively:

$$Q_{x1} = q\ QE\ x_1 = q\ QE\ N_{acc}\left[BT_p + A\left(T_p - T_{oF}\right)\right] \tag{B.5a}$$

$$Q_{x2} = q\ QE\ x_2 = q\ QE\ N_{acc}\left(2BT_p + AT_p\right) \tag{B.5b}$$

$$Q_{x3} = q\ QE\ x_3 = q\ QE\ N_{acc}BT_p \tag{B.5c}$$

$$Q_{x1-x3} = q\ QE\left(x_1 - x_3\right) = q\ QE\ N_{acc}A\left(T_p - T_{oF}\right) \tag{B.6a}$$

$$Q_{x2-x4} = q\ QE\left(x_2 - x_4\right) = q\ QE\ N_{acc}AT_p \tag{B.6b}$$

From these equations the maximum charge that the storage capacitances can accumulate can be calculated. Q_{x3} and Q_{x4} are just measurements of the background without the signal, so they are always smaller than Q_{x1} and Q_{x2}. Applying the first derivative with respect to ϕ or T_{oF} to Q_{x1}, Q_{x2}, Q_{x1-x3} and Q_{x2-x4} and matching the result to 0 the maximum values can be calculated. In the modulated case the maximum charge accumulation occurs at $\phi = 0$ or $\phi = \pi$ for Q_{x1-x3} and at $\phi = \phi/2$ or $\phi = 3\pi/2$ for Q_{x2-x4} and in both cases the maximum charge is:

$$Q_{max}^{Mod} = \frac{q\ QE\ N_{acc}A^{max}\tilde{T}}{\pi} \tag{B.7}$$

For the pulsed ToF techiques the maximum charge accumulations happens at $T_{oF} = 0$ ns for Q_{x1} or Q_{x1-x3} and at $T_{oF} = 50$ ns for Q_{x2} or Q_{x2-x4} and, in both cases is equal. For the PSD-1B technique this maximum charge is:

$$Q_{max}^{PSD-1B} = q\ QE\ N_{acc}\,(B^{max} + A^{max})\,T_p \tag{B.8}$$

And for the PSD-2B this calculation gives:

$$Q_{max}^{PSD-2B} = q\ QE\ N_{acc} A^{max} T_p \tag{B.9}$$

For the MDSI-1B and MDSI-2B the result is, respectively:

$$Q_{max}^{MDSI-1B} = q\ QE\ N_{acc}\,(2B^{max} + A^{max})\,T_p \tag{B.10}$$

$$Q_{max}^{MDSI-2B} = q\ QE\ N_{acc} A^{max} T_p \tag{B.11}$$

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