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Controlling the Carrier Density of SrTiO₃–based Heterostructures with Annealing

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Abstract:

The conducting interface between the insulating oxides LaAlO₃ (LAO) and SrTiO₃ (STO) displays numerous physical phenomena that can be tuned by varying the carrier density, which is generally achieved by electrostatic gating or adjustment of growth parameters. Here, we report how annealing in oxygen at low temperatures ($T < 300$ °C) can be used as a simple route to control the carrier density by several orders of magnitude. The pathway to control the carrier density relies on donor oxidation and is thus applicable to material systems where oxygen vacancies are the dominant source of conductivity. Using STO capped with epitaxial γ -Al₂O₃ (GAO) or amorphous LAO (a-LAO), we identify the pathways for changing the carrier density in the two STO-based cases where oxygen blocking (GAO) and oxygen permeable (a-LAO) films create interface conductivity from oxygen vacancies located in STO near the interface. For a-LAO/STO, the rate limiting step ($E_a = 0.25$ eV) for oxidizing oxygen vacancies is the transportation of oxygen from the atmosphere through the a-LAO film, whereas GAO/STO is limited by oxygen migration inside STO ($E_a = 0.5$ eV). Finally, we show how the control of the carrier density enables writing of conducting nanostructures in γ -Al₂O₃/STO by conducting atomic force microscopy (c-AFM).

Keywords: γ -Al₂O₃/SrTiO₃, LaAlO₃/SrTiO₃, Carrier Density, Oxide Electronics, c-AFM Nanowires

1. Introduction

Controlling the carrier density *in operando* or by means of device fabrication plays a key role in modern electronics. Varying the carrier density at the interface between the band insulator SrTiO₃ (STO) and a thin film of a second band insulator, LaAlO₃ (LAO), grown on top of STO has resulted in a particularly versatile control of many physical phenomena. The carrier density in this system is typically controlled either by varying the sample fabrication process or by electrostatic gating. In the former approach, the carrier density is controlled by the parameters of the LAO growth, where, for instance, increasing the LAO layer thickness above a critical thickness of 4 unit cells^[1] or lowering the oxygen growth pressure^[2] renders insulating interfaces conducting. In the latter approach, free carriers are induced by electrostatic gating of the conducting interface separated from the gate by a solid dielectric (typically STO or LAO)^[1], an electrolyte with mobile ions^[3] or a ferroelectric material.^[4] Using this approach, the gate-control of a large number of properties has been demonstrated including magnetism^[5], the anomalous Hall effect^[3], superconductivity^[6] and spin-orbit coupling.^[7]

The two different approaches each have their strengths and weaknesses. In the first approach, the effect of the carrier density on the sample properties is often studied by fabricating a series of samples with a discrete set of carrier densities. This allows for a change in carrier density exceeding 10^{14} cm⁻². The process does not allow for *in-situ* control of the carrier density, and the results may be strongly influenced by unwanted sample-to-sample variations related to variations the sample fabrication process or the STO substrate quality.

In the second approach, the carrier density can be controlled continuously within a single sample during the experiments. The range of the carrier density tuning using conventional back-gating is much smaller than the first approach. A typical induced carrier density when 100 V is applied at room temperature through a 0.5 mm thick STO substrate is less than 10^{12} cm⁻² [8], which is much lower than typical carrier densities ($n_s > 10^{13}$ cm⁻²) in as-grown LAO/STO.^[1] The use of top-gating or gating through electrolytes can reduce the gate potential while maintaining or increasing the possible range of carrier density tuning. The electrostatic gating has side effects beyond changing the carrier density by a shift in the Fermi energy level. The applied potential adds to the confinement potential of the electrons at the interface and effectively changes their depth distribution.^[9] At low temperatures, electrostatic gating has also previously been observed to predominantly alter the electron mobility rather than the carrier density^[9], change the tetragonal domain structure in STO^[10] and result in pronounced hysteresis of the electrical properties.^[11] At or above room temperature, electromigration of oxygen may occur in STO.^[8,12,13] In addition, obtaining a desired electron density through gating requires a continuous application of an electrostatic potential, which may be undesirable in combination with local gating or when designing functional electronic devices.

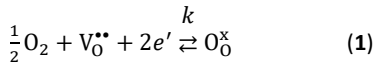
Understanding the origin of the conducting interface is crucial to predict how the growth parameters should be changed to obtain a desired carrier density. However, the origin of the conductivity in LAO/STO is still debated, with the predominant explanations relying on a potential build-up in the polar LAO^[14,15] or oxygen vacancies in STO.^[16] In the wake of the discovery of the LAO/STO heterostructure, several other conducting STO-based interfaces have been fabricated where the origin of the conductivity is less controversially assigned to oxygen vacancies such as STO capped with, e.g., γ -Al₂O₃ (GAO)^[17,18] or amorphous LAO (a-LAO).^[18,19] In these cases, the top film gathers oxygen from STO during growth which leads to oxygen vacancies and free electrons in the near-interface region of STO. Recent high temperature equilibrium conductance (HTEC) measurements in various oxygen pressures have been used to compare several STO-based heterostructures. The results show that the conductivity disappears in a-LAO/STO and GAO/STO in oxidizing conditions, whereas a conductivity component attributed to the potential build-up persists in epitaxial-LAO/STO.^[18] Besides testing if the interface conductivity survives oxidizing conditions, annealing at

elevated temperatures in oxygen atmospheres has frequently been used to minimize the effect of oxygen vacancies.

A hitherto largely overlooked possibility is to use a controlled annealing to regulate the free carrier density by refilling oxygen vacancies with oxygen from a reservoir such as an oxygen-containing atmosphere. Here, we report the control of the carrier density and conductivity in GAO/STO and a-LAO/STO using a low-temperature ($T < 300$ °C) annealing in a 1 bar oxygen environment. As an application of the carrier density control, we show how it can be used to tune GAO/STO into a regime where it is possible to write and erase nanostructures with the biased tip of a conducting atomic force microscope (c-AFM).

2. Results and discussion

The annihilation or creation of oxygen vacancies in oxidizing or reducing environment can be described by a chemical equation of the form



using the Kröger-Vink notation and a rate constant k . Here, the two electrons created by forming an oxygen vacancy can be delocalized and contribute to the conductivity or be localized e.g. by creating different oxygen vacancy charge states (V_O^* or V_O^{**}). The oxygen vacancies created in STO during the growth of a reducing top layer are thermodynamically unstable^[18], but refilling is kinetically hindered at room temperature leading to quasi-stable interfaces. We investigate this oxygen vacancy refilling by measuring the changes in the sheet conductance *in situ* in an atmosphere of 1 bar pure oxygen while the temperature is increased in steps from room temperature to 350 °C (see the Experimental Section for details). The refilling is highly accelerated by elevating the temperature, with the conductivity of the GAO/STO interface being significantly more stable than a-LAO/STO (see **Figure 1a** and **b**). Annealing can be used to carefully control the conductance with a time scale of hours at $T \leq 300$ °C, where the movement of the heavier cations (La, Sr and Ti) is generally frozen.^[20,21] We note, however, that the lighter aluminum may be mobile in GAO below 300 °C owing to the inherent Al vacancies present in GAO.^[22] The change in conductivity for 20 °C $< T < 300$ °C is mainly a result of varying the carrier density (See **Figure 1c**). The contribution of the carrier mobility change is typically $< 10\%$ of the total conductivity change, as the mobility at these temperatures is limited by optical phonon scattering with only a moderate dependence on the electron density.^[23] For a-LAO/STO the maximum carrier density is typically around 10^{14} cm⁻² at room temperature^[19], whereas for GAO/STO carrier densities up to 10^{15} cm⁻² have been reported.^[17] In both cases, the carrier density can easily be controlled without sample-to-sample variations in a large range from the maximum value to a level where the free carriers cannot be measured.

The temperature dependence can be analyzed quantitatively by investigating the thermal activation of the annealing process. We extract the rate of sheet conductance change at each temperature and present it in an Arrhenius plot (see **Figure 2**). While the rate of sheet conductance change is fastest for a-LAO/STO, the activation barrier is 0.5 eV for both a-LAO/STO and GAO/STO at low temperatures. Upon reaching higher temperatures of ≈ 125 °C during the incremental increase of the temperature, the rates deviate from the straight Arrhenius-type behavior observed at low temperatures. For a-LAO/STO, the activation energy of the thermally activated behavior changes from 0.5 eV at low temperatures (< 75 °C) to 0.24 eV at high temperatures (> 125 °C). For GAO/STO, the rate decreases dramatically by more than two orders of magnitude and subsequently reestablishes a regular thermal activation with an activation energy of 0.5 eV. This is consistently reproduced in four GAO/STO samples. Such behavior is typical for the

coexistence of two distinct processes where one process (process A) initially is dominant but eventually saturates, thus allowing the observation of a second process (process B). To test this hypothesis, we subject a new as-grown GAO/STO sample to a fixed temperature of 150 °C in 1 bar of oxygen while continuously measuring the sheet conductance (see inset of **Figure 2**). The initial rate of sheet conductance change ($8 \mu\text{S hour}^{-1}$) is decreased by more than two orders of magnitude to $0.014 \mu\text{S hour}^{-1}$ after 140 hours at 150 °C. Following this pre-annealing step at 150 °C, the sample is cooled to room temperature and then subjected to an identical stepwise increase in the temperature as previously employed to obtain the Arrhenius plot in **Figure 2**. Contrary to as-grown GAO/STO, this pre-annealed GAO/STO now shows a single thermal activation energy during the annealing with $E_a = 0.5$ eV without a drop in the rate (green circles in **Figure 2**), and the pre-annealing is consistent with a saturation of process A.

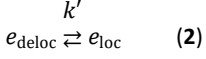
When GAO/STO heterostructures are subjected to the same step-wise annealing procedure in 1 bar nitrogen rather than 1 bar oxygen, the changes in the initial conductivity at low temperatures are similar (dark blue curve in **Figure 2**). After saturation, the conductivity change decreases in both annealing environments before it increases again at higher temperatures. The high-temperature annealing rate in nitrogen is, however, smaller than in oxygen by a factor 2-4. Based on this annealing in nitrogen, we conclude that process A and its saturation are independent of the environment.

We furthermore determine the thickness dependence of the conductance change rate ($|dG_s/dt|$) when GAO/STO and a-LAO/STO samples are stored for around two months at room temperature in a standard vacuum desiccator providing a slight vacuum of 0.8 bar. For GAO/STO the rate is largely independent of the top film thickness (see **Figure S1** in the Supporting Information). For a-LAO/STO the average rate increases almost one order of magnitude when the a-LAO layer is decreased from 5 to 1.5 nm, whereas varying the film thickness only produces a small change if merely the first 12 days are considered. Process A is therefore independent of the top layer thickness whereas process B is highly dependent on the top layer thickness, however, only for the case of a-LAO/STO.

We then attempt to explain the physical origin of the two processes. As the temperature is stabilized at each step, fast (electronic) changes have already occurred before the beginning of each measurement. This includes thermal activation of electrons to the conduction band. Slow ionic movements are therefore suggested to be responsible for the conductivity change reported here. Cation movement generally requires higher activation energy than what is observed here. The energy barriers for moving oxygen in STO^[24,25] and GAO^[26] are 0.5-0.6 eV and 1.3 eV, respectively; the energy barrier in a-LAO is to our knowledge unknown, but arguably smaller than the 0.6-0.7 eV for crystalline LAO.^[24] We therefore attribute the activation energies of 0.5 eV observed at low temperatures (process A), and, for GAO/STO, at high temperatures (process B) to oxygen movement in STO (black, dashed lines in **Figure 2**).

Process A is two orders of magnitude faster than process B, which suggests that the initial oxygen movement occurs over short distances. In addition, process A occurs for both a-LAO/STO and GAO/STO and is independent of top layer thickness and annealing atmosphere. It can therefore be attributed to an internal redistribution of oxygen vacancies within STO (see **Figure 3**). During deposition of oxygen deficient thin films, a non-equilibrium vacancy depth distribution is created in STO, which eventually equilibrates during process A leading to the observed saturation. The effect on the conductivity is likely due to a change in the charge localization when oxygen vacancies are redistributed. Localization of charges is often attributed to trapping sites in the vicinity of oxygen vacancies or a lack of a macroscopic percolation path. Using density functional theory, it was for instance deduced that oxygen

vacancies at the surface of STO traps electrons in contrast to bulk oxygen vacancies.^[27] Movement of oxygen vacancies from the bulk to the surface may thus lower the free carrier density. Electrons can therefore change their state between delocalized and localized with an associated rate constant k' :



This contribution gives $dn_s/dt|_{(\text{de})\text{loc}} \propto -k'$.

Process B, however, is different for a-LAO/STO and GAO/STO. In the former case, process B has a low activation energy and increases greatly when the a-LAO thickness is decreased. Consistent with a previous report^[28], we assign the oxygen vacancy refilling in a-LAO/STO preferentially to molecular oxygen dissociating and diffusing through the top film with a rate-limiting energy barrier of 0.24 eV (see Figure 3). For GAO/STO, this process is halted due to the high activation energy for oxygen movement in GAO, and the oxidation occurs through STO instead. Although the pathway is different for a-LAO/STO and GAO/STO, the net result of both oxidation reactions can be described by equation 1 with a rate constant k giving rise to a contribution $dn_s/dt|_{\text{redox}} \propto -k$.

Oxygen vacancies therefore affect the density of itinerant charge carriers by changing the donor density and by localizing charge carriers. The total rate of carrier density change by the two processes can be described by $\frac{dn_s}{dt} = \frac{1}{A} \frac{dN_{\text{total}}}{dt} = -\frac{1}{A} (f_{\text{deloc}}k + k')$. Here, f_{deloc} denotes the average number of delocalized electrons annihilated when an oxygen vacancy is refilled with oxygen, and the sheet carrier density $n_s = N_{\text{total}}/A$ is defined as the total amount of delocalized electrons (N_{total}) pr. sample area (A).

Since the change in sheet conductance (G_s) during the annealing at a constant temperature is predominantly caused by a change in the carrier density (n_s) rather than the electron mobility (μ), the measured rate of sheet conductance change at a fixed temperature can then be described by:

$$-\left. \frac{dG_s}{dt} \right|_T \approx -e\mu \frac{dn_s}{dt} = e\mu \frac{1}{A} (f_{\text{deloc}}k + k') = e\mu \frac{1}{A} \left[f_{\text{deloc}}k_0 \exp\left(-\frac{E_a}{k_B T}\right) + k'_0 \exp\left(-\frac{E'_a}{k_B T}\right) \right] \quad (3)$$

We assume that the rates can be described by the product of a prefactor (k_0 and k'_0) with an exponential term describing the thermal activation balancing the thermal energy ($k_B T$) with the activation energies (E_a and E'_a) of the rate-limiting step in reaction (1) and (2). Using $E_a^{\text{a-LAO}} = 0.24$ eV and $E_a^{\text{GAO}} = E_a^{\text{GAO}} = E_a^{\text{a-LAO}} = 0.5$ eV together with $k'_0 \rightarrow 0$ as the oxygen vacancy redistribution reaches a quasi-equilibrium, Equation 3 captures the essence of the annealing processes observed in Figure 2.

We note that extracting activation energies is a useful way to deduce the location of the donors. For GAO/STO it has been unclear whether oxygen vacancy donors are located in STO^[17,19] or on the GAO surface due to a possible polarity in GAO in analogy with the polar discontinuity model initially proposed for LAO/STO.^[15] The activation energy of 0.5 eV for oxidizing oxygen vacancies in GAO/STO, however, implies that oxygen vacancies are predominantly located in STO, consistent with interface redox reactions where the growth of an oxygen deficient film reduces STO.^[17,19]

The control of carrier density may be used to enable writing of conducting nanowires in GAO/STO using conducting atomic force microscopy (c-AFM), similar to the nanowire writing demonstrated in LAO/STO.^[29,30] Previously, LAO/STO samples for AFM sketching required a careful control of the deposition parameters including a precise LAO thickness of 3.3 unit cells^[30,31], which is just below the critical thickness

of ~ 4 unit cells for inducing metallic conductivity.^[1] Metallic conductivity can then be locally induced at the interface by moving a positively biased c-AFM tip across the surface of LAO, leaving behind conducting lines with widths down to a few nanometers (see the left schematic drawing in **Figure 4**). Preparing the sample in an ideal initial state is challenging due to the abrupt insulator-to-metal transition accompanied with a decrease in the sheet resistance by more than 5 orders of magnitude when increasing the LAO thickness with a single unit cell from 3 to 4 unit cells.^[1] Instead, the metal-to-insulator transition can be induced after the deposition using annealing, which may enable c-AFM writing of nanostructures. To simplify the fabrication process, we here use a crystalline GAO/STO sample with GAO deposited at room temperature and subsequently annealed on a standard laboratory hot plate in ambient environment.

Prior to the annealing, the GAO/STO interface is metallically conducting, and it is, as expected, not possible to measure a notable conductance change when attempting to write a nanowire between two gold electrodes (see Figure 4). Upon annealing the interface on a hot plate at 150 °C for 3 hours, the room temperature resistance of the sample increases by a factor of 30. In this state, nanowires can be efficiently written and erased at room temperature with positive and negative voltages applied to the c-AFM tip, respectively. When connecting the two gold electrodes with a nanowire written with +25 V applied on the tip, the 4-probe resistance between the electrodes decreases one order of magnitude. Subsequent cutting of the wire by applying a negative tip voltage and scanning across the wire returns the resistance to the original value. By correlating the cutting of the wire with the speed of the c-AFM tip, the width of a nanowire is determined to be approximately 50 nm. The nanowire is observed to be metallically conducting down to 50 mK, whereas the remaining sample is insulating, thus further increasing the difference in the local resistivity of the nanowire and the background. The low-temperature characterization of the c-AFM written nanostructures will be presented in a future publication. The mechanism underpinning the c-AFM writing has been attributed to dissociation of water on the surface, which effectively donates electrons to the nanowire located at interface.^[32] The role of the annealing is expected simply to be to raise the sample resistance to an insulating state where writing can be observed. The annealing strategy thus makes it possible to post-process of the interface of GAO/STO with the possibility to stop at a desired point rather than relying on an intricate control of deposition parameters that may depend on the specific sample, growth method and growth chamber.

We have shown that annealing can be used as a simple way to control the carrier density over many orders of magnitude with no sample-to-sample variation. The approach should be applicable to numerous materials, in particular oxides, where the conductivity either originates primarily from oxygen vacancies or where donor atoms or the material itself changes the electronic properties upon oxidation. Focusing on STO-based samples the approach can be applied on ion-bombarded^[33] or illuminated^[34] STO, STO capped with various metal films^[35] and STO capped with reducing oxides such as yttrium-stabilized zirconia (YSZ)^[19], amorphous STO^[19] or CaHfO₂.^[36] The carrier density in epitaxial LAO/STO can also be controlled to some extent by annealing, if a post-annealing step is not performed after the LAO growth.^[37] Differences are, however, expected depending on the capping of STO. Firstly, the route for refilling oxygen vacancies is determined by the kinetics of breaking molecular O₂ bonds on the surface and diffusing oxygen through the thin film. Oxygen blocking layers such as crystalline GAO grown at high temperatures provide a high stability of the interface conductivity whereas a freely exposed STO surface degrades rapidly. Secondly, the different atomic arrangement at the interface may result in atomic sites located at the interface where oxygen vacancies are stabilized or destabilized.

The carrier density control and dopant engineering using annealing have strengths and weaknesses compared to controlling the carriers by gating or growth. Similar to the growth-induced carrier density change, annealing allows for a large carrier density change, but the low-temperature oxidation minimizes sample-to-sample variations and unwanted side effects such as large changes in the crystallinity. An immediate weakness is that by annealing a sample, the initial state is lost with attempts to reverse the oxidation by reduction being likely to lead to a different state. This has profound implications for reproducing results without suffering from sample-to-sample variation by fabricating a new sample. Secondly, if oxygen blocking films such as GAO are used, the annealing process can result in some degree of inhomogeneity of the carrier density with the center of the sample being more resilient to annealing due to oxygen diffusion through the sides of STO. Lastly, whereas the carrier density tuning by annealing is usually easier than the growth approach, gating is often more convenient and allows for real-time tunability during a number of measurements. However, in certain cases leakage current or insufficient carrier density tunability render gating ineffective. This includes gating of highly conducting samples or gating through a leaking dielectric with free carriers stemming from e.g. some degree of bulk conductivity, defects or photoinduced carriers in measurements featuring irradiation with x-ray, UV or visible light.

Beyond studying effects of shifting the Fermi energy level, the simultaneous control of the oxygen vacancies and electrons can yield some advantages over gating. Donors constitute scattering sites for electrons, and by controlling the number and distribution of donors, we expect that annealing can enhance the mobility and help identifying the dominant scattering mechanism by comparing theoretical predictions with the dependence of the mobility on the carrier density. This includes classical cases of coexisting electrons and donors^[38], modulation doping^[39] and delta-doping in the low and high density regime.^[40] In addition, magnetism in STO and STO-based heterostructures is often suggested to originate in localized magnetic moments on oxygen vacancies^[41], which then could be controlled by careful annealing.

3. Conclusion

We have shown that in those oxides where the conductivity originates from oxygen vacancies, such as a range of STO-based heterostructures, annealing is a powerful procedure for controlling both the Fermi energy level and the donor concentration and distribution. For STO-based heterostructures, the annealing approach provides a hitherto largely overlooked alternative or supplement to traditional approaches to tune the carrier density such as gating and adjustment of growth parameters. We have shown that annealing can enable interface nanowire writing, but the approach may also be particularly interesting for tuning emergent magnetism, enhancing mobility and studying the metal-to-insulator transition.

4. Experimental Section

GAO/STO heterostructures were prepared using pulsed laser deposition from TiO₂-terminated STO at a temperature of 650 °C as described elsewhere.^[42] The same deposition conditions were used for making the a-LAO/STO heterostructures with the exception of depositing LAO on a STO substrate with a temperature of 25 °C instead of 650 °C. For GAO/STO the heating and cooling rate was set to 15 °C min⁻¹, and the samples were cooled immediately after the deposition. If not stated otherwise, the thickness of the GAO film is fixed to ~3.5 unit cells (2.8 nm), whereas thicker a-LAO films of 16 nm were used to clearly resolve the low-temperature annealing behavior. The heterostructures were

electrically connected using wedge wire bonding in van der Pauw geometry, and subjected to annealing at various temperatures in 1 bar oxygen or nitrogen. For the measurements presented in Figure 1a, 1b and 2, the temperature was increased in steps from room temperature to 350 °C. At each step, the temperature was stabilized and the sheet conductance was measured *in situ*. The Hall carrier density and sheet conductivity presented in Figure 1c were measured at room temperature after subjecting the heterostructures to annealing at ~200 °C in 1 bar oxygen for 2-8 hours. The Hall carrier density was deduced from the linear Hall coefficient in magnetic fields up to 15 T. For c-AFM writing, e-beam lithography was used to create resist patterns such that the sample surface was exposed only at areas intended for metal contacts. Argon ion milling was then used to remove 10 nm of GAO and STO, which produced trenches that were filled with titanium (2 nm) and gold (8 nm) to contact the buried electron gas at the GAO/STO interface. A positive voltage applied on the c-AFM tip was used to draw conducting lines from the gold contacts as sketched in Figure 4. To emphasize the simplicity of fabricating interfaces that enable nanowire writing, the GAO film (4 nm) was deposited at room temperature, and the nanowire writing was enabled by annealing on a standard laboratory hot plate in ambient environment.

Supporting Information

Supporting Information is available from the Wiley Online Library

Acknowledgements

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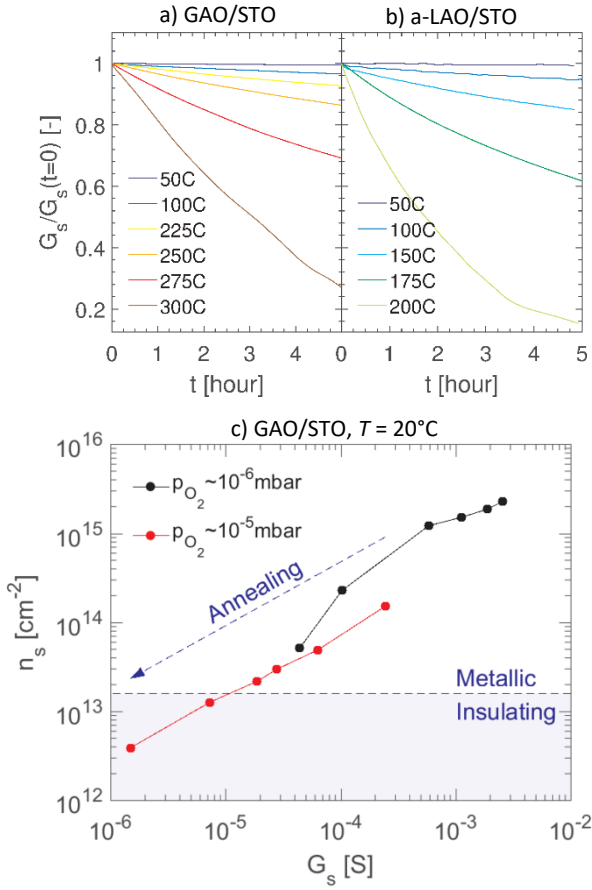


Figure 1: Normalized sheet conductance G_s for a) $\gamma\text{-Al}_2\text{O}_3/\text{SrTiO}_3$ (GAO/STO) and b) amorphous- $\text{LaAlO}_3/\text{SrTiO}_3$ (a-LAO/STO) measured as a function of time during annealing in 1 bar oxygen. Selected temperatures are chosen which produces comparable annealing traces for the two heterostructures while avoiding large non-linearities (see discussion in the main text). c) The Hall carrier density, n_s , as a function of the sheet conductance for two GAO/STO samples with different initial carrier densities obtained by varying the oxygen partial pressure (p_{O_2}) during growth. The carrier density and sheet conductance is measured at room temperature and in between two measurement points the sample is annealed at $\sim 200^\circ\text{C}$ in 1 bar oxygen to induce a carrier density change. The metallic region is defined as the region in carrier densities where $dG_s/dT > 0$ for any temperature T in the interval $2\text{ K} < T < 300\text{ K}$.

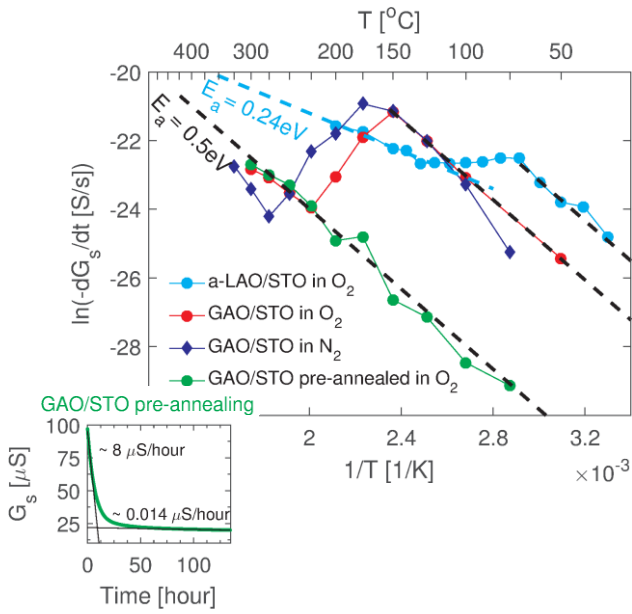


Figure 2: Arrhenius plot of the sheet conductance change (dG_s/dt) measured at various annealing temperatures (T) for GAO/STO and a-LAO/STO in 1 bar nitrogen or oxygen. The rate of conductance change was obtained by stabilizing each temperature for 12 hours while measuring the conductance, except for a-LAO/STO where each annealing step was limited to 7 hours to resolve the low-temperature behavior below 150 °C before saturation. The Arrhenius plot is shown for three as-grown samples and one pre-annealed GAO/STO heterostructure. The latter has been subjected to a 140 hours pre-annealing step at 150 °C in 1 bar oxygen prior to measuring the rate of conductance change for the Arrhenius plot. This pre-annealing saturates the initial degradation process responsible for the high initial conductance change at lower temperatures. The inset shows the sheet conductance as a function of time during this 140 hours pre-annealing; we note that this cannot be fitted satisfactorily by a single exponential function. The parallel black lines correspond to an activation barrier of 0.50 eV, whereas the light blue line represents an activation barrier of 0.24 eV.

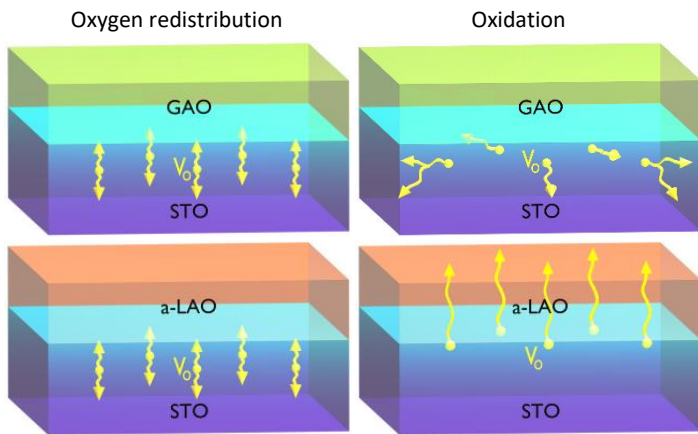


Figure 3: The proposed mechanism for conductance change upon annealing of a-LAO/STO and GAO/STO. Initially, the conductance change is governed by oxygen redistribution (left column), which effectively localizes the electrons. After the oxygen redistribution has reached saturation, oxygen from the atmosphere eliminates oxygen vacancies close to the interface (right column).

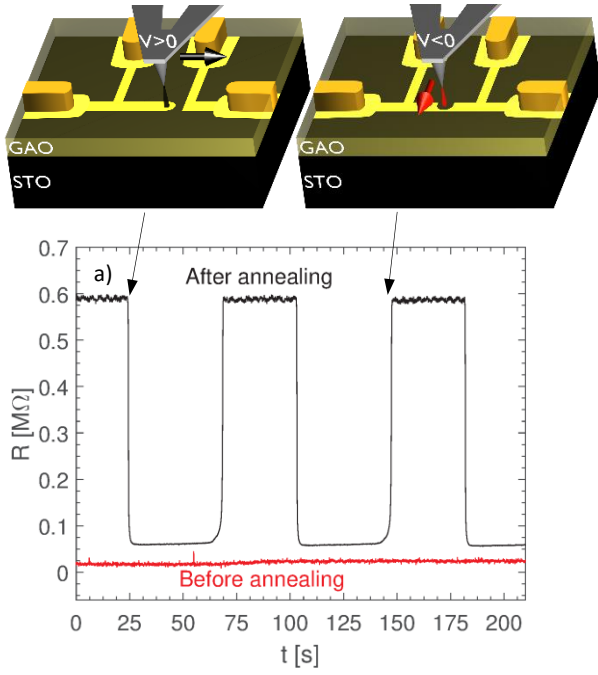


Figure 4: 4-probe resistance (R) measured at room temperature as a function of time (t) during writing and erasing of conducting nanowires before and after annealing on a hot plate at 150 °C for 3 hours in ambient conditions. The writing (erasing) is achieved by applying a positive (negative) voltage on a conducting atomic force microscopy tip, which is then moved across the surface of GAO/STO in order to write (cut) a conducting nanowire at the interface connecting four gold contacts as depicted in the schematic drawings.

Supporting Information

Controlling the Carrier Density of SrTiO₃-based Heterostructures with Annealing

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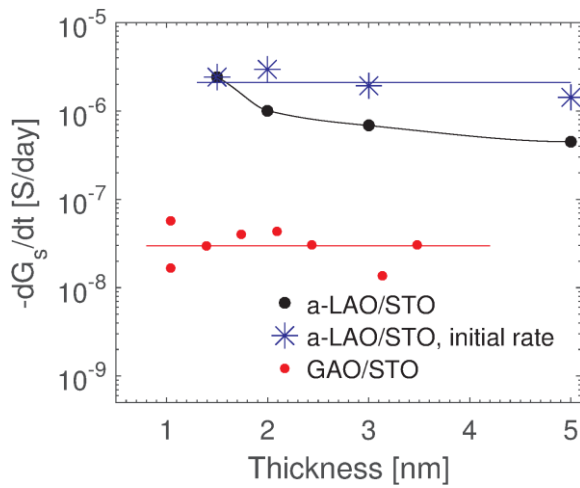


Figure S1: The conductance change (dG_s/dt) in GAO/STO and a-LAO/STO as a function of the thickness of the GAO and a-LAO films when stored for around 2 months in a vacuum desiccator providing a slight vacuum of 0.8 bar. For amorphous-LaAlO₃ the initial conductance change from the first 12 days is also shown.

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