CUBESAT DATA TRANSMISSION AND STORAGE THROUGHPUT OPTIMIZATION THROUGH THE USE OF A ZYNQ SOC BASED CUBESAT SCIENCE INSTRUMENT INTERFACE ELECTRONICS BOARD

A Thesis
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the Faculty of California Polytechnic State University,
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In Partial Fulfillment
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Master of Science in Electrical Engineering

by
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ABSTRACT

CubeSat Data Transmission and Storage Throughput Optimization Through The Use Of a Zynq SoC Based CubeSat Science Instrument Interface Electronics Board

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The CubeSat standard sprang from the desire to create a satellite standard that would open the doors for universities and other lower budget research institutions by making it more feasible to get their work into space. Since then, many other institutions and industries have been adopting variations on the standard for their own use. As more people are seeking out to use the CubeSat standard as their main bus, the standards and practices of the community have grown and expanded and with this growth, new challenges have been created. One such challenge is the bandwidth limitation in the RF-downlink. When carrying payloads requiring what might seem to be a relatively small (science data) bandwidth requirement (on the order of thousands of bps), the RF-link to ground is overloaded. Many approaches in the past have been put forth to help alleviate this issue, unfortunately, none have been fully adopted. This paper presents a solution that takes advantage of new technology yet to be fully exploited in space applications. The key to the solution lies in removing the bandwidth requirements by enabling onboard post-data processing and compression. In order to achieve the high computational needs, while minimizing power consumption, a Xilinx Zynq-7000 SoC is used, creating a highly-programmable, open integration device. This report outlines the design, fabrication and testing of this solution. The completion of the Zynq Processing System CubeSat Science Instrument Interface Electronics Board (or ZPS-Board), ultimately demonstrates the feasibility of this solution. Additionally, this research is funded by NASA's JPL, with secondary motives for the creating of a space application Zynq-7000 SoC based product. Upon successful completion of the ZPS-Board, the product creates a platform for JPL to perform environmental testing in order to study the effects and performance characteristics of the Zynq in space applications.

Keywords: CubeSat, JPL, ZPS-Board, Zynq, Zynq-7000, SoC, XC7Z010, ADP5052, ADS1255, CameraLink, DS90CR288, PolySat

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1. INTRODUCTION

This thesis report outlines the motivation, design, fabrication and testing of the Zynq Processing System CubeSat Science Instrument Interface Electronics Board which will henceforth be referred to as the ZPS-Board. The work performed was done as partial fulfillment of a master's degree from the California Polytechnic State University, San Luis Obispo (Cal Poly). The project was a collaborative effort between Cal Poly State University and NASA's Jet Propulsion Laboratory (JPL). The concept that became the ZPS-Board, was motivated by an interest of JPL in the viability of the Xilinx's Zynq-7000 SoC in space applications. The ZPS-Board is CubeSat electronics payload interface, whose design is based on a solution presented to elevate a growing problem in the field of CubeSats. In creating a space application product that used the Zynq as its primary component, the ZPS-Board provided JPL with a product that could be used to experiment with and gain understanding into the use of the Zynq SoC in a space environment.

This report begins with a general background into the field of CubeSats and then offers a brief overview of the crucial element of the project, Xilinx's Zynq-7000 SoC. The following chapters then step sequentially through the development of the ZPS-Board, beginning with Chapter 3, which presents the constraints of the design. Chapter's 4-5 discuss the development of the ZPS-design and fabrication, focusing on the key considerations and obstacles. The completed design is functionally tested and the resulting data is presented in Chapter 6. Chapter 7 concludes the report with analysis of the final design, offering suggestions concerning improvements and future work.

2. BACKGROUND AND MOTIVATION

Figure 1, demonstrates an example of CubeSat (From LibreCUBE CubeSat open source community). This Satellite follows the smallest and simplest CubeSat standard dimensions of 100x100x113.5mm, called a 1U (The CubeSat Program). Larger variations following the standard essentially scales the satellite up by stacking cubes, effectively increasing the satellite by a "unit" each time, thus called 2U, 3U, etc.… as shown in Figure 2.

Figure 1: Example of a 1U CubeSat -- LibreCUBE (Libre Cube)

The CubeSat standard, created in 1999, began as a joint effort between Dr. Jordi Puig-Suari at California Polytechnic State University, San Luis Obispo and Dr. Bob Twiggs at Stanford University. The objective was to create a picosatellite standard that would allow for the creation of simpler, lower cost satellites. The hope was that the standard would allow for academic and research based institutions to easily and affordably reach space. The CubeSat standard has since grown considerably and is now an internationally adopted standard with collaborations between over a hundred universities, schools and private intuitions.

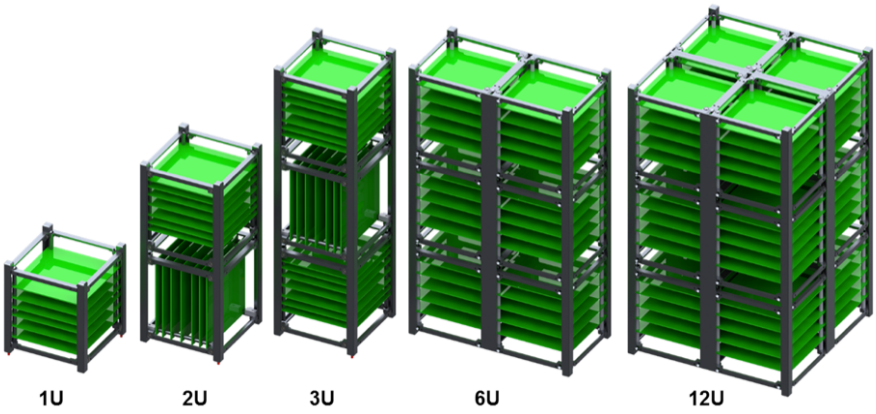

Figure 2: Example of Physical Variations on the CubeSat Design (NSR)

This growing CubeSat community and continued use of CubeSats has led to developments which include their use in more advanced science exploration, including inter-planetary science as well as more advanced payloads. For example, NASA's MarCO (2016) and University of Colorado Boulder's CSWEE CubeSat (2014), which carries a relativistic electron and proton telescope to study space weather (Palo, O'Connor and Devito). However, with these developments have come new obstacles in CubeSat designs. One of the current prevalent issues, is the CubeSat RF telemetry downlink. The payload, or commonly referred to as the "Science Instrument", is the focal point of a mission. The science instrument, once in space, electronically performs and measures a science experiment of interest to the mission and sends resulting data to earth to be studied. Unfortunately, sending the data to the ground is not always a simple task. If the science instrument measures data at too high a resolution and/or at too high a sample rate, the current downlink rates may not be capable of downloading it at a reasonable rate. To better quantify this, a traditional CubeSat has a communication window of about forty minutes a day with a rate of approximately 1200bps (Koritza and Bellardo). Many engineering solutions are being pursued in order to find ways around this bottlenecked design. For example, many are attempting to move into the use of higher frequency band transceivers for communication. Traditionally, CubeSats use UHF and S-Band transceivers

for their low cost and ease of access (being within the amateur radio band). However, recently many commercial companies are designing X-Band CubeSat transceivers as an off the shelf option to the community (Peragin, Diez and Darnon). Unfortunately, this approach still requires the increase costs of ground station access and still only increases the downlink rates during flyby and can still require large buffering capabilities for the science data. This paper presents a different solution to the common RF bottleneck problem. Through the use of a computationally-dense, low-power, on-board device, a CubeSat could perform real-time post-processing of the science data and/or data compression. This solution seeks to greatly diminish downlink bandwidth needs as well as buffering requirements. This paper presents the complete and verified design of the ZPS-Board. Through the use of Xilinx's powerful, highly programmable Zynq-7000 SoC, the ZPS-Board is more than capable of performing the task.

Table 1: Zynq-7000 All Programmable Device Options (Xilinx, PSG)

		Low-End Portfolio			Mid-Range Devices			
	Device Name	Z-7010	Z-7015	Z-7020	Z-7030	Z-7035	Z-7045	Z-7100
	Part Number	XC7Z010	XC7Z015	XC7Z020	XC7Z030	XC7Z035	XC7Z045	XC7Z100
Processing System	Processor Core	Dual ARM® Cortex™-A9 MPCore™ with CoreSight™						
	Processor Extensions	NEON™ & Single / Double Precision Floating Point for each processor						
	Maximum Frequency	866MHz			Up to 1GHz[1]			
	L1 Cache	32KB Instruction, 32KB Data per processor						
	L2 Cache	512KB						
	On-Chip Memory	256KB						
	External Memory Support[2]	DDR3, DDR3L, DDR2, LPDDR2						
	External Static Memory Support[2]	2x Quad-SPI, NAND, NOR						
	DMA Channels	8 (4 dedicated to Programmable Logic)						
	Peripherals	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO						
	Peripherals w/ built-in DMA[2]	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO						
	Security[3]	RSA Authentication of First Stage Boot Loader, AES and SHA 256b Decryption and Authentication for Secure Boot						
	Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	2x AXI 32b Master, 2x AXI 32b Slave 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts						
Programmable Logic	7 Series Programmable Logic Equivalent	Artix®-7 FPGA	Artix-7 FPGA	Artix-7 FPGA	Kintex®-7 FPGA	Kintex-7 FPGA	Kintex-7 FPGA	Kintex-7 FPGA
	Logic Cells (Approximate ASIC Gates[4])	28K (~430K)	74K (~1.1M)	85K (~1.3M)	125K (~1.9M)	275K (~4.1M)	350K (~5.2M)	444K (~6.6M)
	Look-Up Tables (LUTs)	17,600	46,200	53,200	78,600	171,900	218,600	277,400
	Flip-Flops	35,200	92,400	106,400	157,200	343,800	437,200	554,800
	Total Block RAM (# 36Kb Blocks)	2.1Mb (60)	3.3Mb (95)	4.9Mb (140)	9.3Mb (265)	17.6Mb (500)	19.1Mb (545)	26.5Mb (755)
	Programmable DSP Slices (18x25 MACCs)	80	160	220	400	900	900	2,020
	Peak DSP Performance (Symmetric FIR)	100 GMACs	200 GMACS	276 GMACs	593 GMACs	1,334 GMACs	1,334 GMACs	2,622 GMACs
	PCI Express® (Root Complex or Endpoint)	—	Gen2 x4	—	Gen2 x4	Gen2 x8	Gen2 x8	Gen2 x8
	Analog Mixed Signal (AMS) / XADC[2]	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs						
	Security[3]	AES and SHA 256b Decryption and Authentication for Secure Programmable Logic Configuration						

1. 1 GHz processor frequency is available only for -3 speed grades for devices in flip-chip packages. Please see the data sheet for more details.
2. Z-7010 in CLG225 has restrictions on PS peripherals, memory interfaces, and I/Os. Please refer to the Technical Reference Manual for more details.
3. Security block is shared by the Processing System and the Programmable Logic.
4. Equivalent ASIC gate count is dependent of the function implemented. The assumption is 1 Logic Cell = ~15 ASIC Gates.

Table 1 demonstrates the Zynq-7000 options list and some of their advantages. The Zynq-7000 SoC, released by Xilinx in 2011 is the ideal central component for the purposed application. The

Zynq-7000 SoC is a family of highly configurable embedded system ICs, which tightly integrates dual ARM Cortex-A9 processors, with an equivalent Xilinx 7 series FPGA.

Since the release of the Zynq-7000 SoC, many industries have begun to see its potential for use in many applications. The Zynq offers a highly programmable platform while at the same time minimizes time-to-market, by offering fully integrated hardware already familiar to industry. The duel ARM Cortex-A9 processors on the Zynq offer large potential for running complex software and operating systems, with its ARM NEON architecture and double precision floating-point engines. At the same time, the Zynq offers easy and rapid design/configuration of external hardware accelerators by use of the on-board FPGA. The two programmable platforms integrated onto one die offers space savings, but more importantly, it eliminates I/O bottlenecks and dramatically reduces power waste, by use of a high-speed interconnect. The duel ARM Cortex-A9 referred to as the "Processing System" (PS) and FPGA referred to as the "Programmable Logic" (PL), are connected using one of ARM's "Advanced Microcontroller Bus Architectures" (AMBA), called the "Advanced eXtensible Interface 4" (AXI4). The AXI4 programmable bus allows for rapid configuring of this highly adaptable interconnect and can achieve multi-gigabit data communication.

This computationally powerful, low power and small form factor SoC, offers a perfect solution for the design of a CubeSat science instrument with high bandwidth needs. However, the use of the Zynq on a CubeSat offers extended potential. As already mentioned, many industries are looking into the potential viability of the Zynq in areas such as machine vision, communication systems, automotive and in the case with the ZPS-Board, Space. NASA's JPL, has interest in the potential of using the Zynq in space applications and how it will perform in space's extreme temperature and radiation environment. The funding for this project came from JPL with the objective that the ZPS-Board will create a platform to begin testing the Zynq in space environments. With the completion of the ZPS-Board's design, JPL will then use it to perform simulated environmental testing. Further,

with its use in actual CubeSat missions by other institutions (for example, Cal Poly's PolySat program), the Zynq can be extensively environmentally tested.

3. DESIGN SPECIFICATIONS

3.1.Overall Design Concept

Figure 3, demonstrates the black box representation of the Zynq Processing System CubeSat Science Instrument Interface Electronics Board (ZPS-Board).

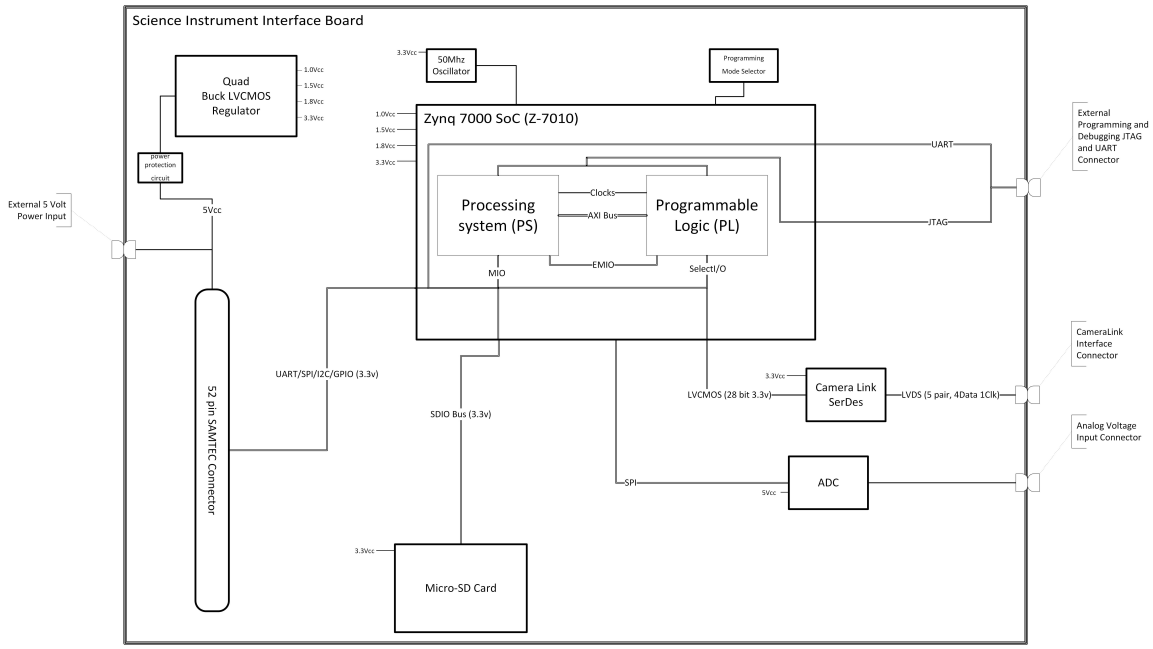

Figure 3: ZPS Electronics Board Overall System Black Box Diagram

The ZPS-Board was designed around Xilinx's Zynq Z-7010 SoC, which interfaces directly to all support and peripheral circuits on the ZPS-Board. There are three key peripheral circuits: the analog to digital interface (ADC), the Camera Link interface, and the inter-board signaling. There is also support circuitry, which is comprised of the power system, configuration circuitry and communications signaling. In what follows, each of these systems will be looked at in detail, exploring each subsystems design specifications and what factors led to them.

3.2.Overall System Constraints

The ZPS-Board has two key constraining factors. The first is that it must integrate into current CubeSat designs. This requires that it not only fit into commonly used CubeSat space-crafts (chassis), but must also integrate into the software, hardware and electrical interconnects. The second constraining factor is durability. The environment of space can be extremely hostile to electronic systems and so the ZPS-Board must account for all commonly encountered environmental factors.

3.2.1.Form Factor

One of the key constraints of the ZPS-board, is form factor. Though the overall mechanical structure of a CubeSat is well define by its standard (The CubeSat Program), the internals of the satellite are not. Fortunately, there is a good amount of common practice that is observed across CubeSats designs. One of these practices, is following the legacy of large scale satellites, which use discrete systems that make up what is commonly referred to as the “spacecraft bus”. The spacecraft bus is comprised of discrete systems: a command and data handling subsystem, electrical power subsystem, communications subsystem and attitude control subsystem. The spacecraft bus acts as the vehicle for which the whole purpose is to deliver and support the payload; which in general, is an instrument that performs some sort of measurement.

Figure 4 (pg.9) demonstrates a common example of a simple 1-U CubeSat stack up. The satellite shown in *Figure 4* is of the ESTCube-1 CubeSat built by the Estonian Student Satellite Program through the assistance of ESA (ESA). As one can see, there are what looks like small boards labeled as the aforementioned spacecraft bus subsystems. On large scale satellites, the common subsystem is laid out over a handful of dedicated enclosed “units”. On a CubeSat, due to size and weight

constraints, these subsystems are often confined to a single electronics board and connect/communicate over a stacked-through board connector, as shown below.

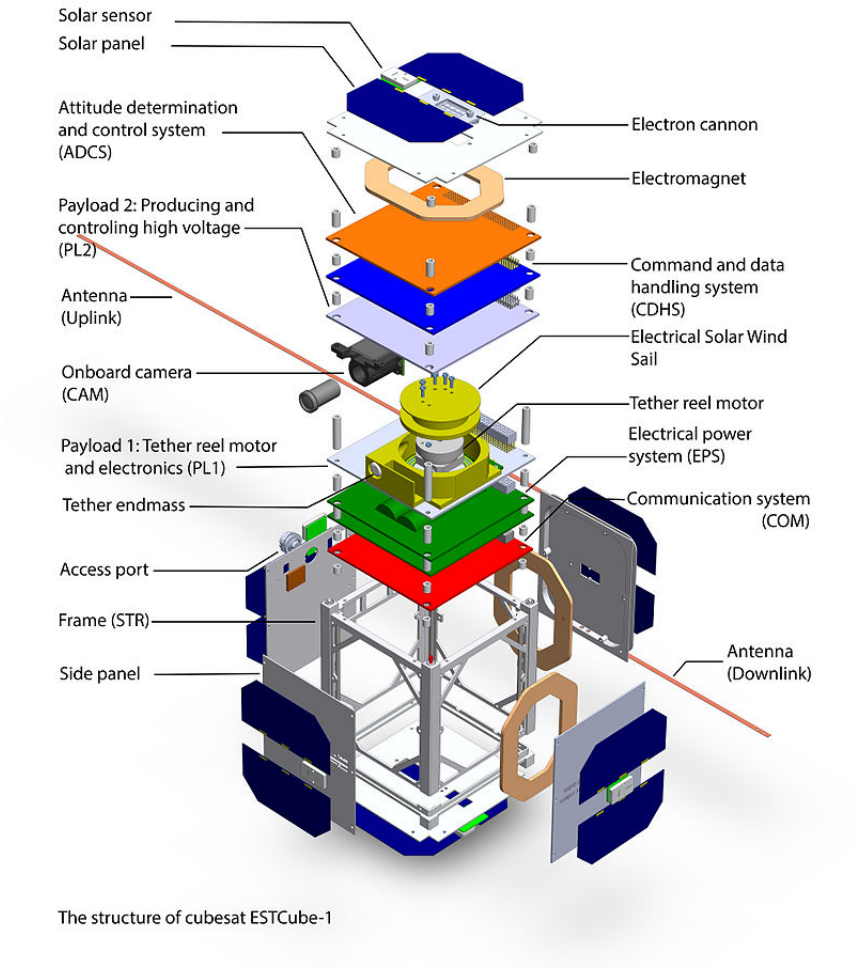

Figure 4: Example of a CubeSat Electronics Stack-Up (ESA)

Another common practice in the CubeSat community is the use of the PC/104 form factor as the standard for the subsystem electronics boards. The PC/104 physical constraints and dimensionality are shown in Figure 5.

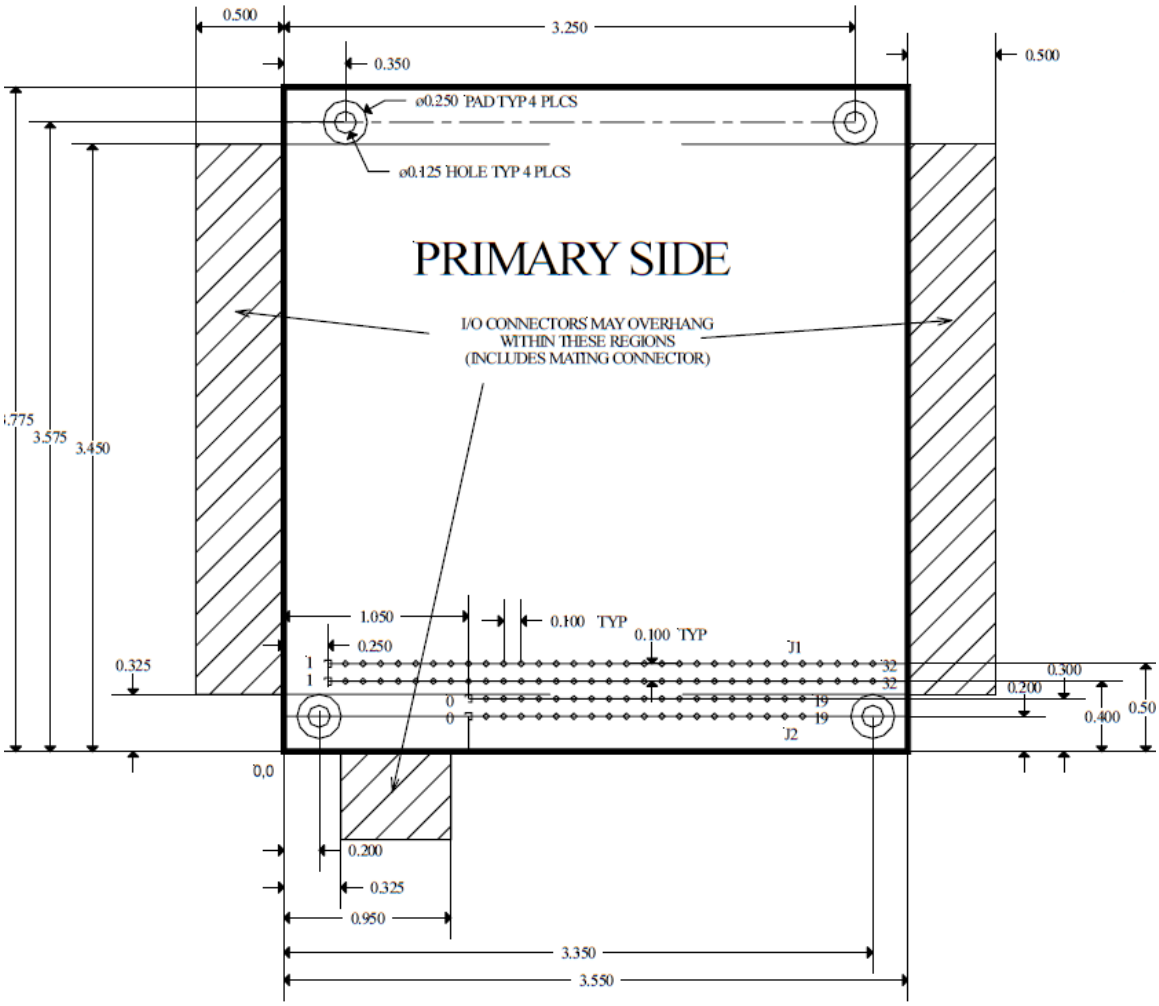

Figure 5: PC/104 Standard Form Factor Dimensions (PC/104 Embedded Consortium)

The PC/104 embedded system form factor was standardized in 1992 and is in wide use (PC/104 Embedded Consortium). The form factor fits well within the dimension of a CubeSat chassis and is stackable. Therefore, its use helps to insure compliance with the CubeSat standard, while at the same time, allowing for an already widely accepted standard to be easily adopted. This insures higher level of integration success when mixing different designer's subsystem electronics boards. This serves to further the ideal of CubeSats being a relatively inexpensive, generic, off-the-shelf,

satellite option. Thus, the ZPS-Board, is based around these CubeSat standard practices. The ZPS-Board acts as a standalone interface for a generic science instrument (payload) and follows the PC/104 form factor. The board connects to the spacecraft bus through the standard stack-through connector (a standard of the PC/104) and complies with the dimensional constraints of PC/104.

It is of note that one of the objectives of the ZPS-Board design is to allow for its use in Cal Poly's PolySat program and prospective missions. However, PolySat currently uses a non-PC/104 compliant form factor for their electronics boards. PolySat's designs are based off their main provider of off-the-shelf parts, Tyvak Nano-Satellite Systems Inc. Tyvak's board designs are maintained as proprietary and consequently cannot be by fully discussed within this document. What can be mentioned however, is that the Tyvak boards are slightly smaller than the PC/104 and use a center of the board stack-through connecters with different bus/pinouts then those followed by PC/104 based CubeSats. As previously mentioned, in order to keep with the ideal of the CubeSat community for generic off the shelf conformity, the ZPS-Board follows the PC/104 form factor. However, the layout of the board is done in such a way that it allows all components to fit within the smaller Tyvak board footprint and would require only a handful of minor adjustments to convert it to Tyvak compliant. In order to make the board Tyvak compliant, the PCB's board outline would have to be resized to the Tyvaks's and the PC/104 52-pin stack-through connector would need to be removed.

3.2.2.Environmental

The second key constraint of the ZPS-Board is durability. Space applications require extreme environmental considerations when being designed. Though a CubeSat is not commonly used in deep space applications (requiring much more extreme radiation and temperature considerations), they still see harsh temperature swings and damaging radiation (Heidt, Puig-Suari and Moore).

Currently, most CubeSat satellites are used for low earth orbit (LEO) applications and they tend to see reasonably predictable, wide temperature swings. Figure 6, demonstrates an expected thermal profile of a CubeSat in a LEO. The plot in Figure 6 was created using the data collected from California Polytechnic State University's CP3 satellite's external side sensor.

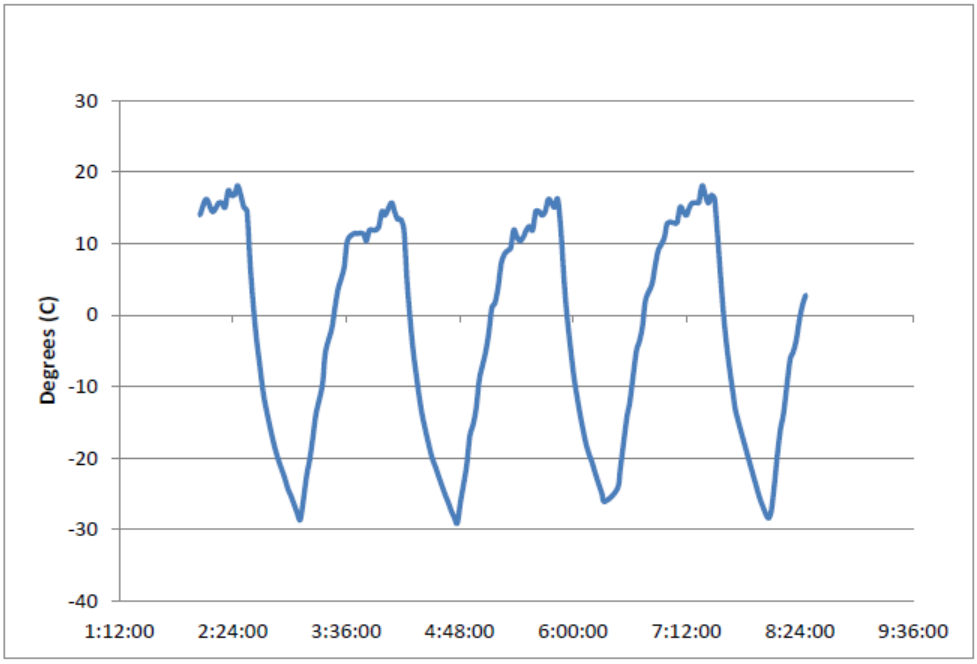

Figure 6: Measured Temperature Data Taken From the CP3 CubeSat Satellite External Sensor (Friedel and McKibbon)

As one will note, there is a reasonably well defined window for the temperature profile of a typical CubeSat. Further, there is a reasonably well-defined temperature gradient. All the elements that make up the ZPS-Board had to be constrained based on this information. All elements including all electrical and mechanical components are rated for operating temperatures of -30° to 20°C (except the DS90CR288A, see Section 7.3 for more information). Since the temperature variation over a given cycle is within a reasonable rate (~100[°C/hr]), this effect was ignored.

Radiation in a LEO (160km to 2,000km) is not relatively high due to geomagnetic shielding effects. Further, the current mean lifetime for a CubeSat mission means the overall total ionizing dose (TID)

levels are relatively low. For perspective, a common failure rate of a microprocessor is 10-20kRad(Si) (Sinclair and Dyer). When compared to NASA GSFC's research on total dose per year with respect to aluminum shielding for different orbits (Figure 7), one can see that within LEO and for a common one year mission life (assuming a reasonable 100mills shielding), the TID is below 10kRad and therefore negligible (Barth).

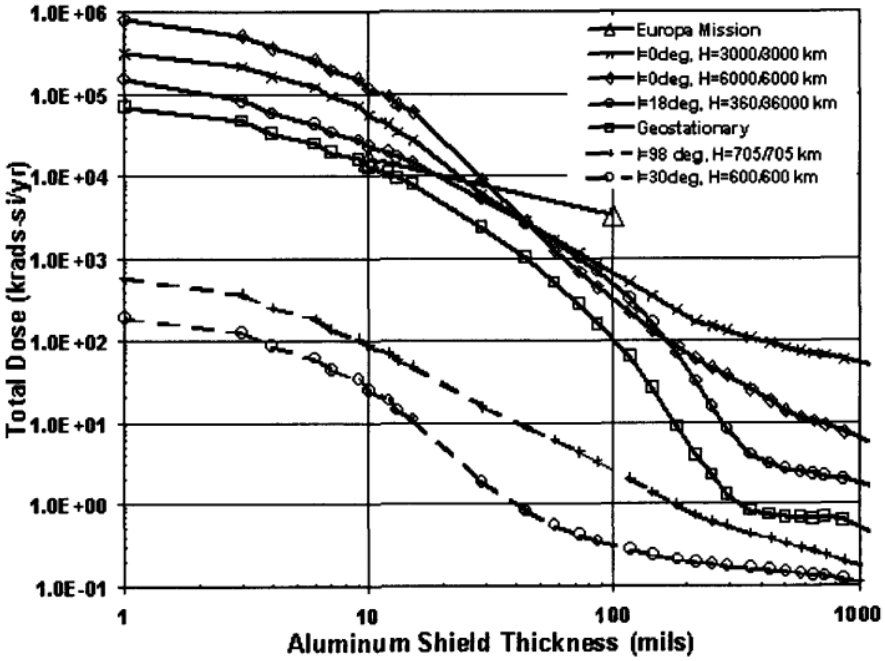

Figure 7: Spacecraft Electronics Total Dose per Year versus Aluminum Shielding for Different Orbits and Inclination (Barth)

Though the total radiation doses may be small enough to ignore, single event upsets (SEU) are still reasonably common due to cosmic rays, which contain heavy energetic ions. These high energy particles have the potential of causing a transistor latch up. It is assumed that for the sake of dramatically reducing the cost of the ZPS-Board, this environmental concern can reasonably be taken care of through the use of redundancies and error scrubbing in software.

In conclusion, since radiation is still a potential concern due to the fact that semiconductor devices can act wildly different in the presence of radiation, testing should be done to characterize how well the ZPS-Board will actually function. In fact, the Zynq's performance in a radiation environment is a major interest of JPL and testing is planned in the future work on the ZPS board. Please see Chapter 7. for further discussion.

3.2.3.Zynq

The Xilinx Zynq-7000 SoC comes in a series of different options. The major distinction between each of Zynq options, is the different FPGA technologies/capabilities as can be seen in Table 1 (pg.4). There are of course more distinctions between the offerings in the 7000 series. For example, when moving from the Z-7020 to the Z-7030, the max frequency of the ARM processors moves from 866MHz to 1GHz. (for speed grade -3) (Xilinx, DS187). Additionally, there are two other relevant differences in the options. The Z-7030 and above, offer Xilinx's Digitally Controller Impedance (DCI) technology. DCI, can greatly increase high speed signal integrity by having internal dynamic termination for I/O. Secondly, the packaging options of the 7000 series devices affect sizing and how many pins are available and consequently how many IOs are available. Table 2 (pg.15) demonstrates the option list, comparing the advantages and disadvantages of each.

Based on the required minimal sizing of the ZPS-Board, the Z-7010 was chosen. The Artix-7 with 17,600 look up tables is presumed reasonably sufficient and the DCI is not required due to the use of the external SERDES for high-speed interfacing. The CLG400 packaging was chosen since fifty-four PL I/O (SelectIO) lines available on the CLG225 packaging would greatly limit further expandability of the ZPS-Board (after the minimal required thirty-five SelectIO were used). The I-grade (industrial) temperature rating was selected with a range of -40°C to 100°C in order to meet

specifications. Lastly, the -2 (Mid) speed-grade was selected as a balance of speed vs. power. The final device selected is defined as XC7Z010-2CLG400I.

Table 2: Zynq-7000 All Programmable Packaging Options (Xilinx, PSG)

		Low-End Portfolio			Mid-Range Devices			
	Device Name	Z-7010	Z-7015	Z-7020	Z-7030	Z-7035	Z-7045	Z-7100
	Part Number	XC7Z010	XC7Z015	XC7Z020	XC7Z030	XC7Z035	XC7Z045	XC7Z100
Unique Footprint	PCB Footprint Dimensions (mm) [1]	HR I/O, PS I/O[2], GTP Transceivers			HR I/O, HP I/O, PS I/O[2], GTX Transceivers			
CLG225	13x13	54[3], 86, 0						
CLG400	17x17	100, 128, 0		128, 128, 0				
CLG484	19x19			200, 128, 0				
CLG485[4]	19x19		150, 128, 4					
SBG485 / SBV485[4]	19x19				50[3], 100, 128, 4			
FBG484 / FBV484	23x23				100, 63, 128, 4			
FBG676 / FBV676[1]	27x27				100, 150, 128, 4	100, 150, 128, 8	100, 150, 128, 8	
FFG676 / FFV676[1]	27x27				100, 150, 128, 4	100, 150, 128, 8	100, 150, 128, 8	
FFG900 / FFV900	31x31					212, 150, 128, 16	212, 150, 128, 16	212, 150, 128, 16
FFG1156 / FFV1156	35x35							250, 150, 128, 16

1. Devices in the same package are footprint compatible. FBG676 / FBV676 and FFG676 / FFV676 are also footprint compatible.
2. PS I/O count does not include dedicated DDR calibration pins.
3. Static memory interface combined with the usage of many peripherals could require more than 50 I/Os. In that case, the designer can use the Programmable Logic SelectIO interface.
4. CLG485 and SBG485 / SBV485 are pin-to-pin compatible. See product data sheets and user guides for more details.
   See DS190, *Zynq-7000 All Programmable SoC Overview* for package details.

3.3.Peripherals

Since the ZPS-Board is meant to be a generic, customizable, science instrument interface, the science instrument integration options had to be fairly wide-ranged. Assuming that the science instrument could be a fairly intelligent system, a digital interface would be needed. However, if the science instrument was more of a dumb-sensor, then an analog to digital interface might be required. Both scenarios must therefore be accounted for by adding both interfaces to the design.

3.3.1.Analog Interface

The analog to digital converter that was chosen is Texas Instrument's ADS1255, a very low noise 24-bit ADC. The device is a two channel 30kSPS, 4th order delta-sigma ultra-high precision ADC

with two single ended analog inputs (5v range) or a one differential (±5v range). The ADC uses a serial SPI interface for configuration and data reading. This device was selected since having a high precision, low noise ADC would increase the viability of it in many CubeSat designs, while not having overly adverse effect on cost.

3.3.2.Digital Interface

Camera-Link was the chosen standard for the high-speed digital interface option. The Camera Link standard is based on the Channel Link Standard and is widely used for high bandwidth digital camera interfacing. The base system (which was selected for this design) has a 7:1 serial interface running at 85MHz (strobe) over four LVDS lines, which allows for maximum of 2.38Gbps data rate. The selection of this interface is useful in rabidly integrating off the shelf image capturing science instruments and also capable of being easily adapted for other user designed high speed interfaces.

3.3.3.Storage

Since the ZPS-Board is meant to be more of a proof of concept then a final design, any extraneous options for the design were not added. It was decided that adding additional external RAM for the Zynq was not required since there was already a small amount contained within the Zynq. Therefore, since space was limited on the ZPS-Board and DDR memory added additional unrequired complexity to the design, it was not added.

External non-volatile storage however, was required for the ZPS-Board. In order to boot locally, the Zynq would require flash memory to store boot information for the Processing System and the

bit file for configuring the Programmable Logic. The four supported options were evaluated: NAND, NOR, QSPI and SD-Flash (Xilinx, TRM). It was decided based on size and expandability, as well as, its potential to use as extra storage for the Zynq, that SD-Flash should be used. Further, SD-Flash happens to be the most commonly used memory storage for off the shelf CubeSat electronics, so its proven use for this application reinforced this decision. The Micro SD Card form factor was chosen in order to minimize size and weight.

3.4.Major Support Circuitry

3.4.1.Power

The power support circuitry is based upon Analog Devices' ADP5052ACPZ-R7 5-channel (quad buck and one low power/LDO) power regulator. This IC was chosen based on the power requirements and its proven use in Digilent's Zybo board (a Zynq SoC breakout board). The ZPS-Board has a small number of different regulated voltage requirements, which are ultimately set by the Zynq SoC whose requirements are shown in Table 3.

Table 3: Voltage Supply Requirements List for the Zynq-7000 SoC (Xilinx, TRM)

Type	Pin Name	Nominal Voltage	Power Pin Description
PS Power	V_{CCPINT}	1.0V	Internal logic
	V_{CCPAUX}	1.8V	I/O buffer pre-driver
	V_{CCO_DDR}	1.2V to 1.8V	DDR memory interface
	V_{CCO_MIO0}	1.8V to 3.3V	MIO bank 0, pins 0:15
	V_{CCO_MIO1}	1.8V to 3.3V	MIO bank 1, pins 16:53
	V_{CCPLL}	1.8V	Three PLL clocks, analog
PL Power	V_{CCINT}	1.0V	Internal core logic
	V_{CCAUX}	1.8V	I/O buffer pre-driver
	$V_{CCO\_\#}$	1.8V to 3.3V	I/O buffers drivers (per bank)
	V_{CC_BATT}	1.5V	PL decryption key memory backup
	V_{CCBRAM}	1.0V	PL block RAM
	$V_{CCAUX\_IO\_G\#}$	1.8V to 2.0V	PL auxiliary I/O circuits
XADC	VCCADC, GNDADC	N/A	Analog power and ground.
Ground	GND	Ground	Digital and analog grounds

All other devices on the ZPS-Board require a regulated 3.3v supply voltage (aside from the ADC's 5.0v and reference 2.5v voltage -- see 4.2 for more information). As one will note from Table 3, there are three required voltages for the ZPS-Board, 3.3v, 1.0v and 1.8v. These supply voltages are all generated from the power supply circuit. It is also of note that the ADP5052 has four buck regulated supplies. The fourth, which was not needed, was configured to be 1.5v in order to create the option for adding DDR memory to the ZPS-Board. In addition, the linear power regulator on the ADP5052 was configured to supply a 1.8v reference for the Zynq's integrated ADC (since it offers a low output noise of 92μVrms (Analog Devices)). See Section 7.6 for more information on this.

The specifications that define the configuration and sizing of the power circuit elements are based on Table 4. Since the design is based upon an open ended application of the Zynq (the dominate load), the max load constraints are based on the Digilent and Analog Devices' Zybo Board specifications (Digilent), The Zynq's load requirements are effectively set by the programming and configuration of the device. Ultimately, these constraints of the design are nonspecific and can greatly affect how the board can be used. Therefore, when using the ZPS-Board for particular applications, the maximum load constraints should be noted by the end user. Load regulation and percent output ripple, are based on the minimum and maximum ratings for the devices attached to that supply.

Table 4: Power Circuit Design Specifications

SUPPLY VOLTAGE	MAX OUTPUT LOAD [A]	PERCENT OUTPUT VOLTAGE RIPPLE	LOAD REGULATION
3.3V	1.5	5%	5%
1.8V	0.6	5%	5%
1.0V	2.1	5%	5%
NOMINAL EXTERNAL SUPPLY VOLTAGE FOR THE ZPS-BOARD			**5V**

3.4.2.Debug, Communication and Configuration Signaling

In order to configure and communicate with the ZPS-Board, both within a CubeSat and during configuration and testing, the board required multiple serial interfaces. A JTAG interface is needed for configuring and testing the Zynq SoC and needs to be accessible while the board is fully integrated into a CubeSat. Further, an optional UART and I2C serial bus (chosen for minimal signal requirements and multiplexed on same pins of the Zynq) for basic debug and communication with the ZPS-Board during CubeSat integration would be required. Therefore, a right angle with minimal profile (to meet the PC/104) and eight contacts (four for JTAG, two for UART/I2C and two for external power/references) was selected to allow external connection to these signals.

The ZPS-Board also needed to be able to communicate through the stack-through interconnect to other subsystems within a standard CubeSat. In order to insure success, many serial and GPIO lines were connected from the Zynq to the 52-pin standard connector of the PC/104 form factor. Four multiplexed serial (UART, I2C, SPI and PS-GPIO) lines were connected the 52-pin stack-through connector. Additionally, six fully configurable lines from the Programmable Logic (called SelectIO) lines were brought out to the 52-pin connector.

4. DESIGN

4.1.Power

As stated in Section 3.4.1, the power circuit is based upon the ADP5052. This power controller IC is a quad buck regulator with a low current LDO linear regulator. The power circuit contains the controller IC (ADP5052) at its center and all other basic buck circuit components for each voltage supply rail including inductor, output capacitor, etc. (high side FETs are internal to IC).

4.1.1.Schematic

The circuit design and configuration of the ADP5052 is based on the circuit schematic for Digilent's Zybo board (Digilent) and cross-compared with the Analog Devices' "ADP505x Multi Channel Buck Designer" (release 1.122) and Analog Devices' ADP5052 datasheet (Analog Devices), to insure that the design would meet the required specifications (see Table 4). Figure 8 demonstrates the schematic of the ZPS-Board power circuit that was created.

The circuit is powered nominally with a 5v external supply as noted in Table 4: Power Circuit Design Specifications (pg.18). The voltage supply to the ZPS-Board was designed to be supplied by two sources and selected via a jumper connector J7 (see Appendix II – Circuit Schematics -- sheet 6, for more information on jumper wiring). When powered nominally inflight, the board will receive all power through the 52-pin stack-through connector and sourced from the CubeSat's EPS subsystem. However, during design and testing of the ZPS-Board, the board can be supplied through the alternate external barrel jack connector (J5). This additional external power source can prove useful if the board requires dedicated and/or isolated power during testing of the ZPS-Board when fully integrated into a CubeSat.

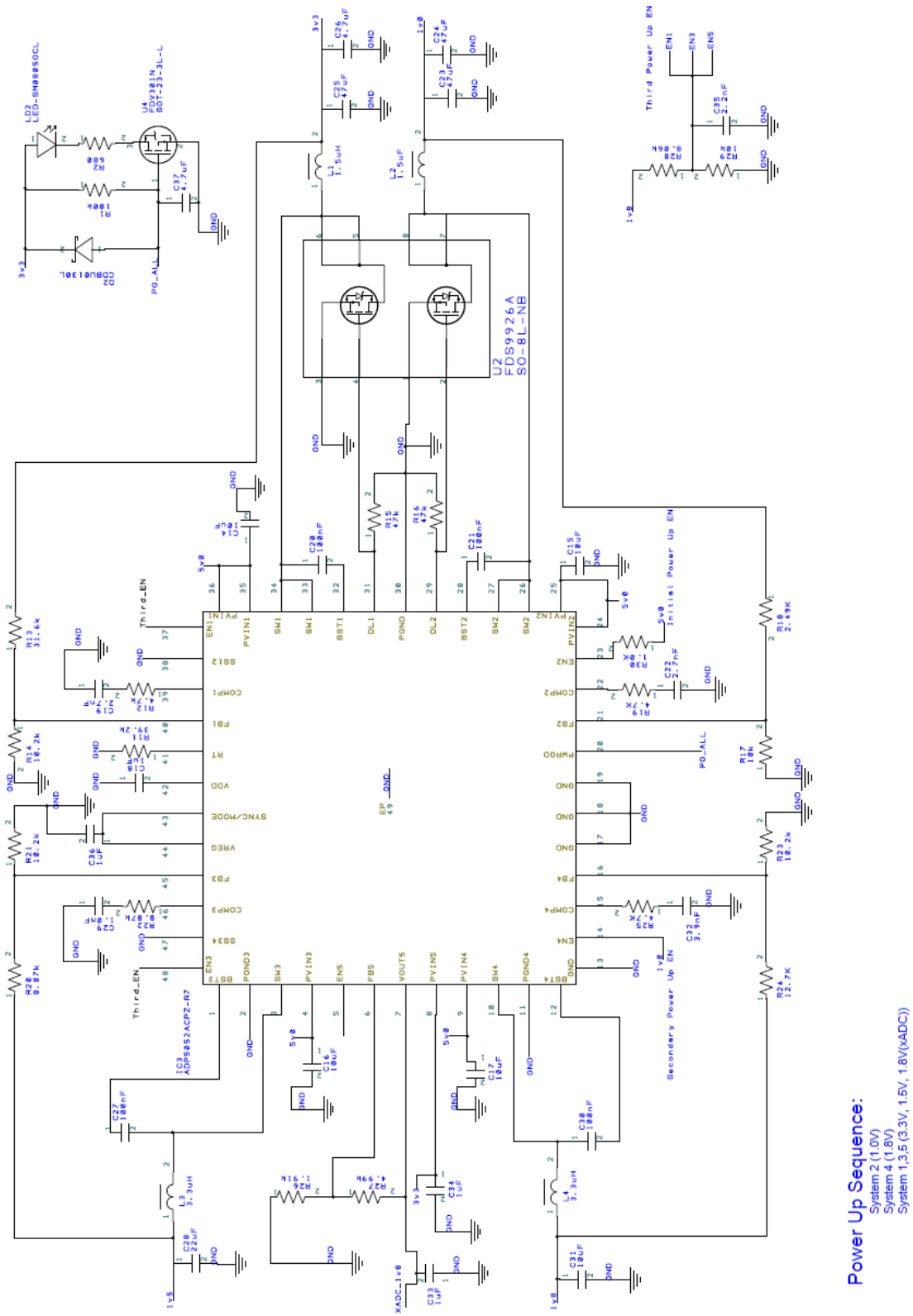

Figure 8: Power Circuit Schematic for ZPS-Board

Power up sequence of each supply voltage is shown in Figure 8, as 1.0v, 1.8v and then the remaining. This is achieved by cascading the output of each independent regulator to the enable pin of the next in the sequence. The 3.3V channel is the last supply to come up and the channel for which the regulator's "power good" signal is based on. This signal, drives an LED indicator as well as the enable pin "PS_POR_B" of the Zynq itself (all other devices on the ZPS-Board are enabled via the Zynq's I/O thereafter). The reason for this sequential power up constriction is due to the Zynq's requirement that its core voltages to be stabilized before bringing up the 3.3v supply and enabling the Zynq (Xilinx, DS187).

4.1.2.Layout

Layout and part selection for the power circuit was based on the recommendations of the ADP5052 datasheet (Analog Devices). The layout of the power circuit can be seen in Figure 9, which depicts the top layer of the board (where most of power circuit's traces lie). Based on the requirements that ZPS-Board would have to be fabricated by hand (due to cost constraints) the smallest components used were 0805 (imperial). This larger sizing when compared to the datasheets recommended 0402 or even 0603, created a highly cramped area for layout and proved very difficult to produce.

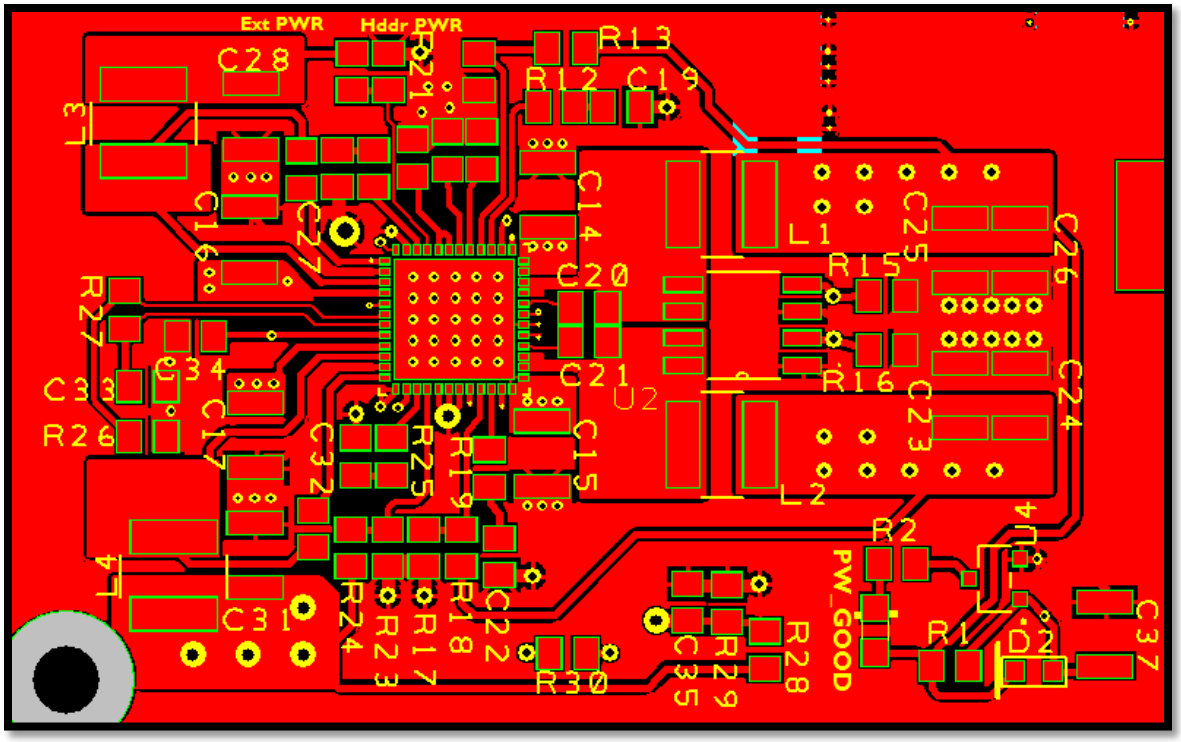

Figure 9: Power Circuit Top Layer Layout on ZPS-Board

Some key considerations that were applied while laying out this circuit were:

- Insuring feedback trace overlap with high current paths is minimized and feedback divider is close to the ADP5052 FBx pin
- Highest emphasis was placed on PVINx decoupling capacitors locality to input (minimize length/inductance to input)
- Used several vias on output supply planelets to expand area for return currents
- Maximized the ADP5052's ground-pad footprint with as many vias as possible to optimize thermal dissipation

4.2.Analog to Digital Circuit

As stated in 3.3.1, the analog to digital circuit is based on Texas Instrument's ADS1255 high precision, low noise, 24-bit ADC. This IC is mostly self-contained; however, it does require a small amount of support circuitry such as a highly stable reference voltage and an external oscillator.

4.2.1.Schematic

The complete ADC circuit is shown in Figure 10 (pg.25). The schematic demonstrates the ADS1255 as the main component of the circuit and the support circuitry. The required reference voltage for the ADC is generated by a Texas Instrument's REF6025IDGKT extremely low noise (total noise 5 μVrms and temperature drift of 5 ppm/°C (max) from –40°C to +125°C (Texas Instraments, SBOS708B)) voltage reference. A crystal oscillator was chosen to supply the master clock of the ADC (as opposed to clock generator) and the crystal was selected to be 7.68MHz. This frequency was selected because it was used for all test case data in the datasheet (Texas Instraments, SBAS288K).

There are some circuit elements that should also be highlighted with the ADC circuit (see Figure 10). For example, the addition of termination resistors placed on all serial inputs. The purpose of these resistors is to minimize the potential of error in the final design due to parasitic inductance caused by layout. This parasitic inductance, coupled with the input capacitance of these inputs, can cause potentially large amounts of ringing when subject to steep step changes. This effect is especially important for the serial SPI clock line, as too large of ringing will look like false edges to the slave devices, causing a corruption of data. Also, by recommendation of the ADS1255 datasheet (Texas Instraments, SBAS288K), an RC filter was created on the inputs of the ADC in order to limit the potential high-frequency noise near the delta-sigma modulation frequency.

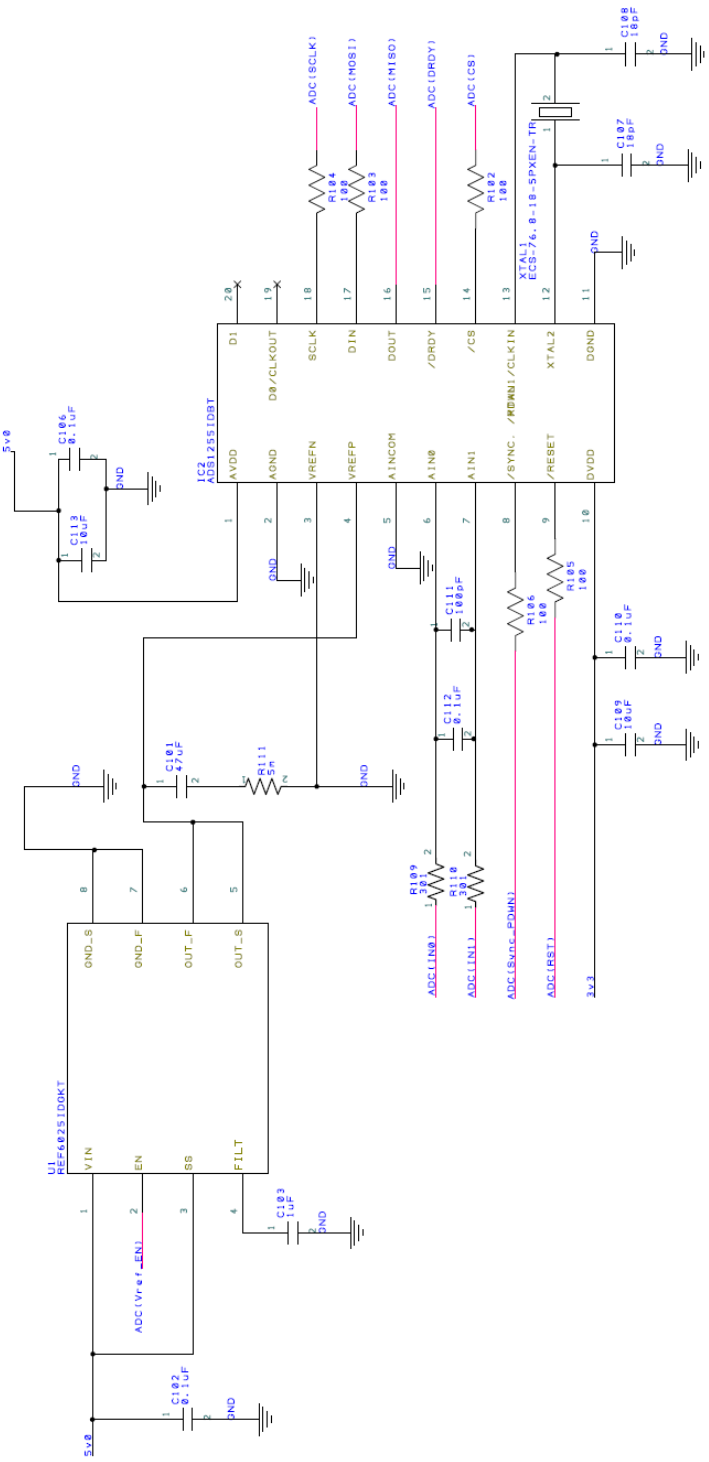

Figure 10: Analog to Digital Circuit Schematic for ZPS-Board

4.2.2.Layout

The layout of the analog to digital circuit is one of the simplest, but still contains some very important considerations. The ADS1255 is designed to be good at removing input referred noise, but if not isolated well, this can be severally degraded. Additionally, since the ADC is such high resolution (24-bits), the level of isolation required is extremely high. The greatest contributors of noise on the ZPS-Board are the Zynq SoC and the high current switching noise generated by the power circuits. Figure 11, demonstrates the layout of the ADC circuit as well as the high noise areas and components.

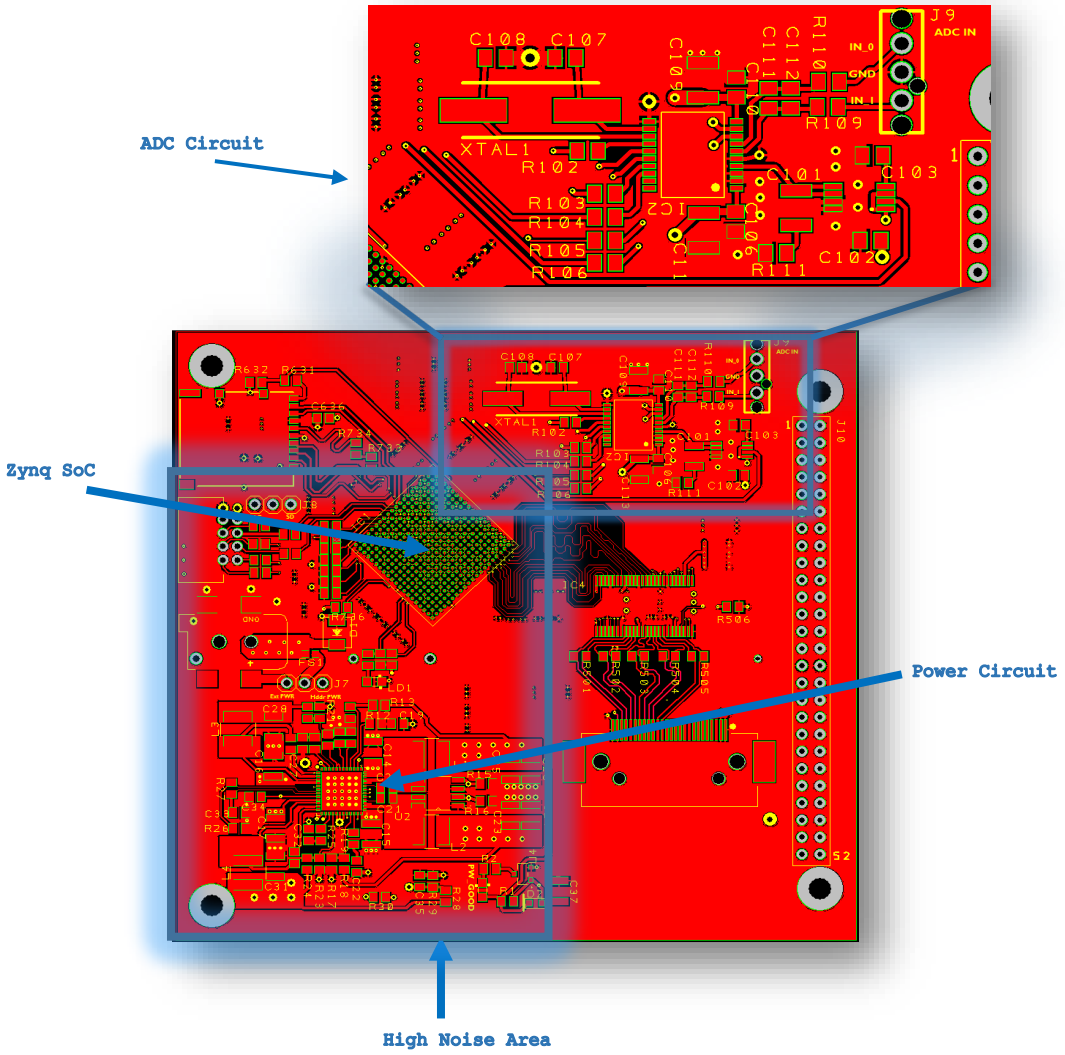

Figure 11: Analog to Digital Circuit Top Layer Layout on ZPS-Board

As one will note from Figure 11, the ADC circuit is the furthest it can be from the power circuit and lies outside the high return current paths. The circuit with the highest risk to injecting noise into the input of the ADC is the power circuit. This high potential for noise injection is due to the switching of the regulator, which will pull large amounts of current though the ground plane. Additionally, the Zynq will generate very large noise over a wide band of frequencies due to the nature of the device and therefore, the ADC is not only as far away from it as possible but is also far away from its return currents (with respect to the power circuit). Additionally, but not shown in Figure 11, there are banks of the bypass capacitors that lie between the Zynq and the ADC circuit (on the bottom layer of the board). These tanks of energy will offer localized bypassing of the rails which will help to block noise reaching the ADC via the ground plane. Lastly, the ADS1255 IC has two sides, an analog side, where the reference voltage and input signals are connected and the digital side, where the serial interface and external oscillator are connected. These two sides are laid out apposing each other in order to minimize the interference between the two. Additionally, the analog side of the ADS1255 is facing away from the sources of noise within the board.

4.2.3.Prefabrication Testing

Since the ADC circuit's ADS1255 IC had not been tested with the Zynq, there was no certainty that the two devices would integrate as expected. Therefore, before the design of the ZPS-Board was fabricated, the option of verifying this interface was investigated. Since no reasonably priced breakout board for the ADS1255 was available for purchase, the actually ZPS-Board ADC circuit was fabricated on a simple standalone board shown in Figure 12. The traces that would normally run through the ZPS-Board to the Zynq, as well as supply rails, were brought out to a test-point pins on the test-board.

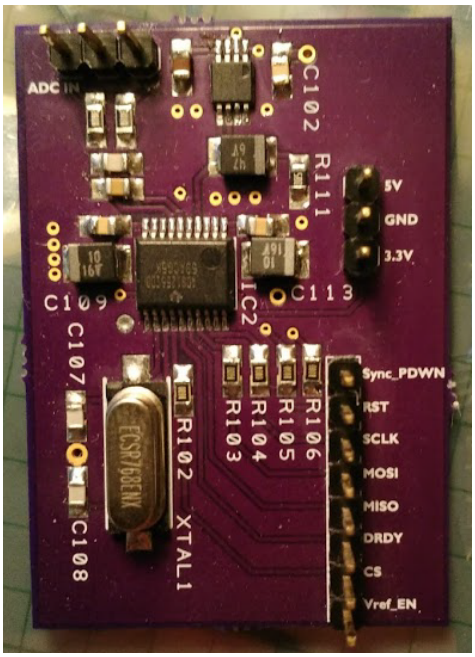

Figure 12: Analog to Digital Test Breakout Board

The ADC test breakout board was connected to a Zynq breakout board by Digilent called the Zybo. Test software was written to run on the Zynq's Processing System and allowed for testing of the Zynq's SPI hardware. The first basic test to be run was a simple register read from the slave device (ADS1255). In performing this test, an integration error was discovered. The slave device required multiple bytes to be transmitted for a single read/write command and required that the chip select (CS) line be asserted until the command was completed (Texas Instraments, SBAS288K). Unfortunately, it was discovered that the CS line would always de-assert after each transmission of a byte. It was also discovered, that this effect was not correctable through the Zynq's peripheral driver. Therefore a design change was made to the ZPS-Board to circumvent the incompatibility. The CS line was removed from the Zynq's dedicated SPI CS line and connected to a GPIO, thereby allowing the assertion of the slave line to be fully controllable within software.

Once this correction was made, the slave responded to the register read command and an example of a successful read of address 0x00 is shown in Figure 13. The first byte (sent by the master, not shown) is 0x10 (command: read register 0x00). Second byte (sent by master, not shown) is 0x00

(command: read only one successive register(s)). The last byte is the response from the slave, labeled in time waveform as “SDIO” and is 0x30, which is the expected response. The first nibble is the factory programmed ID and the last nibble are configuration registers that are default zero. Please refer to the ADS1255 datasheet for more information (Texas Instraments, SBAS288K).

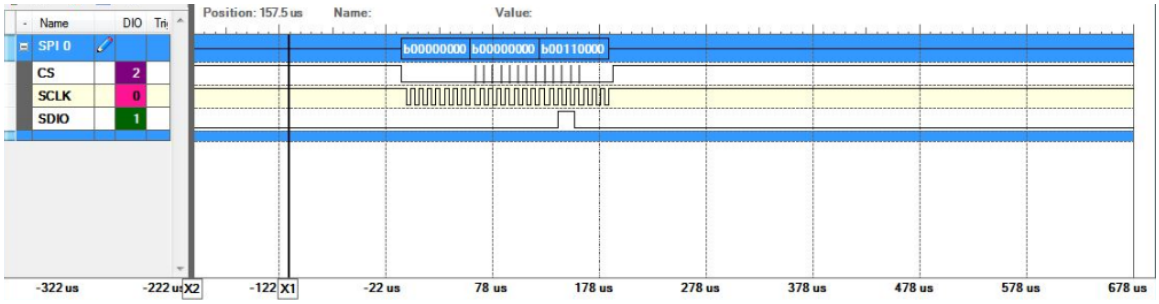

Figure 13: Analog to Digital Serial Interface Testing of Test Breakout Board

Once a basic register read command was successfully executed, a complete test of all the ADS1255’s commands were performed. Final test software, to be used during later testing with the ZPS-Board, was written during this ADC to Zynq compatibility testing. This test software which allowed for interfacing directly to the Zynq via a UART/user command-line, allowed for rapid configuration and testing of the final ADC circuit, once the ZPS-Board was fabricated (See 6.3.1 for more information).

4.3.Camera Link

The high speed digital interface for the science instrument is based on the Camera Link standard (see section 3.3.2, for more information). This key element of the circuit is a serial/deserializer (SERDES), which is used to take the high speed LVDS lines and convert them to a slower parallel data stream for the Zynq.

4.3.1.Schematic

Figure 14 demonstrates the constructed circuit for the Camera Link interface.

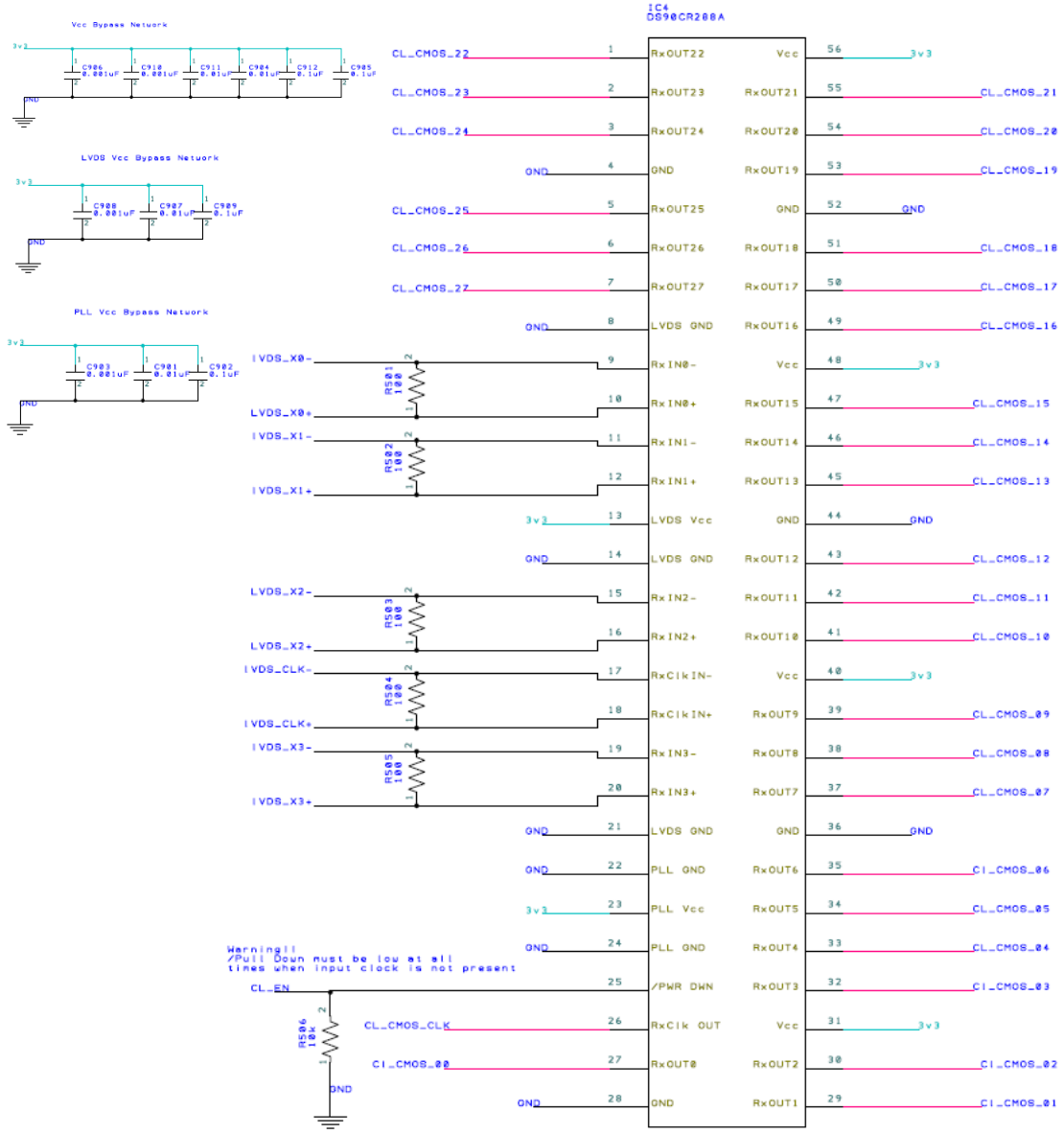

Figure 14: Camera Link Circuit Schematic for ZPS-Board

The physical layer of Camera Link is based off the Channel Link standard and is comprised of a driver receiver pair connected with five low voltage differential lines (LVDS – Standard:

ANSI/TIA/EIA-644) . The driver takes twenty eight single ended CMOS signals and serializes it 7:1 for four of the LVDS lines. The fifth line is a LVDS clock, which is nominally run at 85MHz. The Receiver takes the four data lines and deserializes them back to 28 CMOS lines clocked out at 85MHz. Figure 15 demonstrates a standard physical layer for a Cameral Link system.

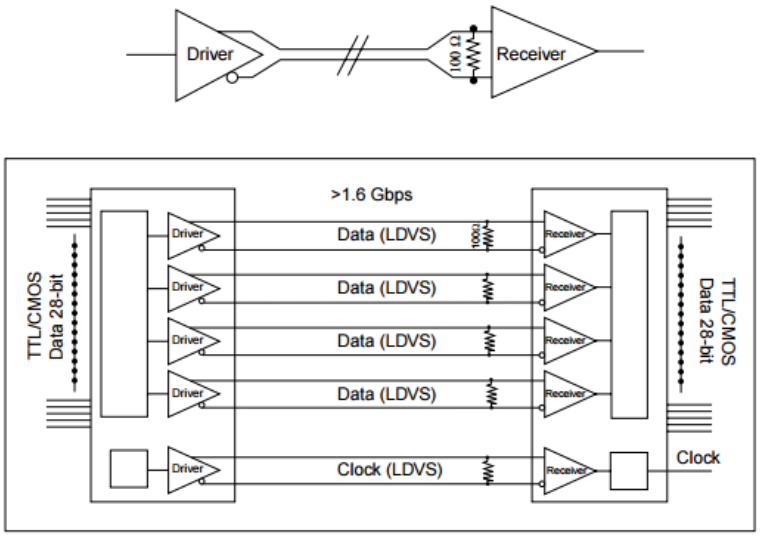

Figure 15: Camera Link Standard Physical Layer (National Semiconductor, PULNiX America, Inc and Basler)

The clock is a serial frame indicator and between each strobe of the clock, seven bits are transmitted for each LVDS line. For this setup (Base Camera Link), the physical layer is capable of transmitting (85MHz x 7bits x 4 lines) 2.38Gbps (National Semiconductor, PULNiX America, Inc and Basler).

The most complicated element of the Camera Link interface is the high speed aspect. Though high speed affected the layout the most, the schematic was also affected. The DS90CR288A IC receiver deserializer is the main component of the Camera Link circuit and due to its high switching, requires a large amount capacitor bypassing (Note the bypass capacitor banks in the Camera Link Schematic, Figure 14). In order to supply energy up to high frequencies, a spectrum of capacitors values were used in order to minimize inductive impedance, as advised by the DS90CR288A datasheet (Texas Instraments, SNLS056G).

4.3.2.Layout

Figure 16, shows the layout of the Camera link input side and DS90CR288A footprint for the ZPS-Board.

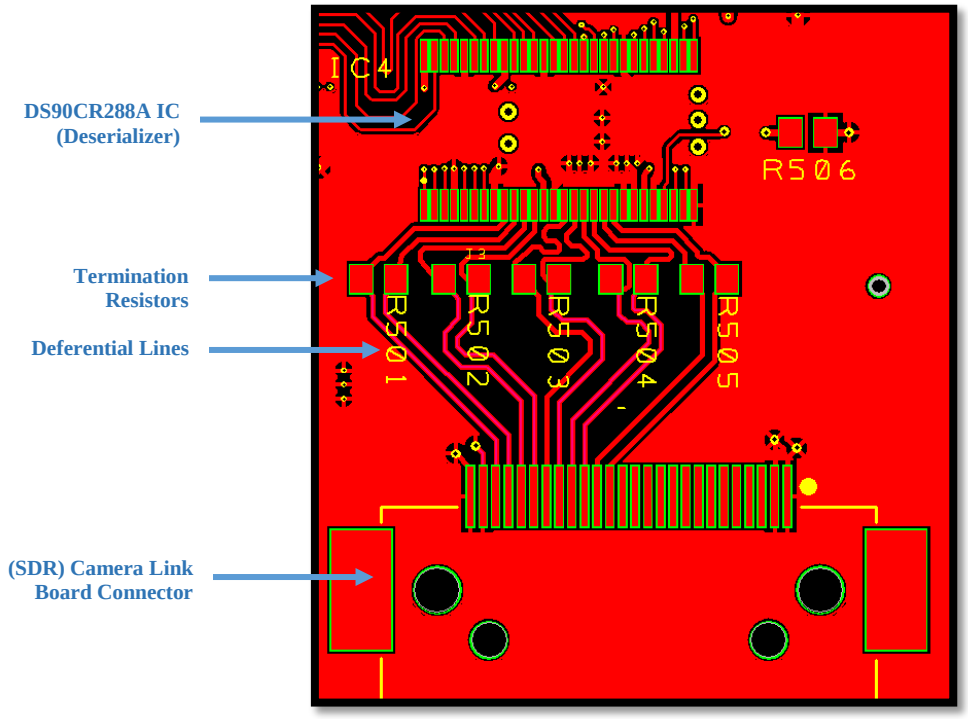

Figure 16: Camera Link Circuit Layout LVDS Traces for the ZPS-Board

The key elements of the layout to note, are for example, the five differential traces. Since the software used to perform this portion of the design did not offer automatic differential spacing for trace placement, each differently pair had to be laid-out by hand. In order to properly match the pairs to 100Ω differential impedance (set by LVDS standard), the manufacturers of the board stack up and sizing had to be acquired. Once a PCB fabricator was decided upon (See Chapter 5. Fabrication, for more information), the information needed to properly size the different traces were obtained from the manufacturer and shown in Figure 17. The trace sizing was calculated using Saturn PCB Design software, provided in Table 5.

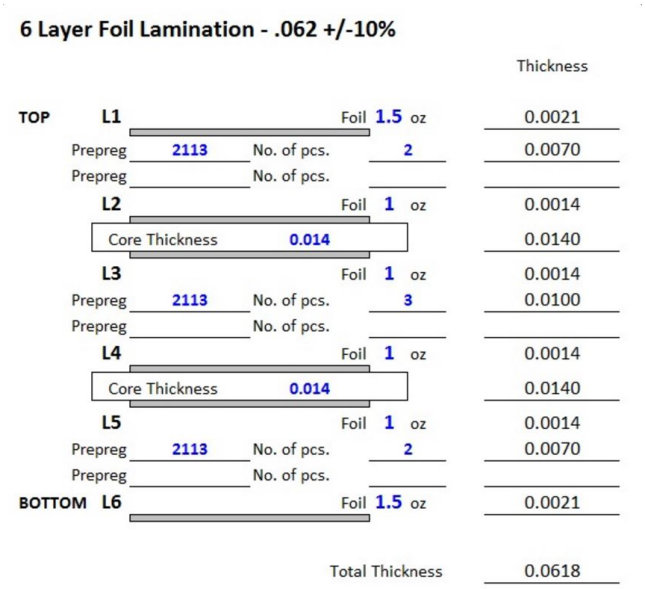

Figure 17: Manufacturers Board Specifications for 6 Layer Stack Up (Bay Area Circuits Inc.)

Table 5: Calculated Dimensions Required for Camera Link LVDS Traces on the ZPS-Board

GIVEN CONSTRAINTS		**CALCULATED CONSTRAINTS**	
Er	4.2	**Conductor Spacing**	0.4 mm
Conductor Height	0.1778 mm	**Conductor Width**	0.25 mm
Target Zdiff	100 Ω	**Actual Zdiff**	99.630 Ω

The differential traces were laid-out based on the spacing and trace size given in Table 5. While at the same time, length matching all five LVDS lines, in order to minimize skew. The LVDS traces were terminated using 100Ω termination resistors (placing them as close as possible to the DS90CR288A IC) in order to cancel reflections in the high-speed lines.

Figure 18 shows the layout of the twenty eight CMOS lines of the Camera Link circuit (output side of SERDES). These traces connect the DS90CR288A IC deserialized data and clocks lines to the Zynq SoC. Each trace is length matched to 33mm in order to minimize signal skew. As noted in

the figure, there is a ground plane in between the two planes that separate the traces. In addition, (which is not easy to see from the figure) all traces between each plane never run directly parallel with traces on the opposing plane. These two layout constraints were implemented in order to minimize the single-ended signal's crosstalk.

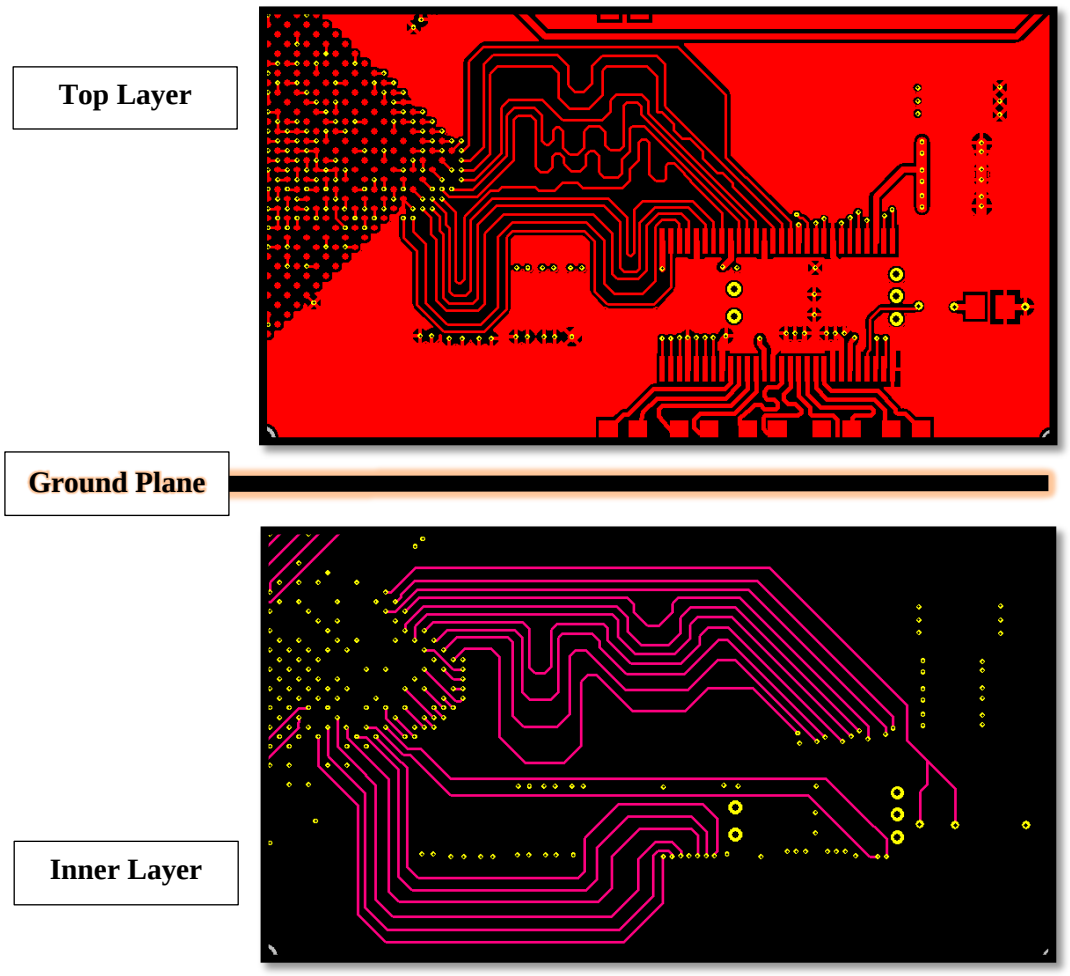

Figure 18: Camera Link Circuit Layout CMOS Traces for the ZPS-Board

4.3.3.Prefabrication Testing

Due to the high risk of failure in the high speed lines for the Camera link signal traces and a lack of experience in their potential electromagnetic interference (EMI), simulation testing was performed in order to increase the certainty of a successful design. Keysight's Advanced Design Systems (ADS) software (Ver. 2016.1), was used to perform the EMI simulations and analysis. Using ADS, Gerber files for the layer of interest (top layer) was imported into the EMI simulator. The EMI Simulator takes the layout dimension from the Gerber file and with the physical board parameters shown in Figure 17 (pg.33), generates an EMI Schematic Model, which can then be used within ADS Schematics. The created model for testing the LVDS traces is shown in Figure 19 (below) and demonstrates the test configuration in ADS "Schematics". In order to properly configure the driver model for the test, the rise and fall times as well as the data rate and voltage swing of the DS90CR288A IC were extracted from its datasheet (Texas Instraments, SNLS056G). The extracted information is given in Table 6.

Table 6: DS90CR288A IC LVDS Signal Characteristics Required for Simulation

Rise Time (Max)	**Fall Time (Max)**	**High Voltage**	**Low Voltage**	**Data Rate (Max)**
0.75ns	0.75ns	450mV	250mV	545Mbps

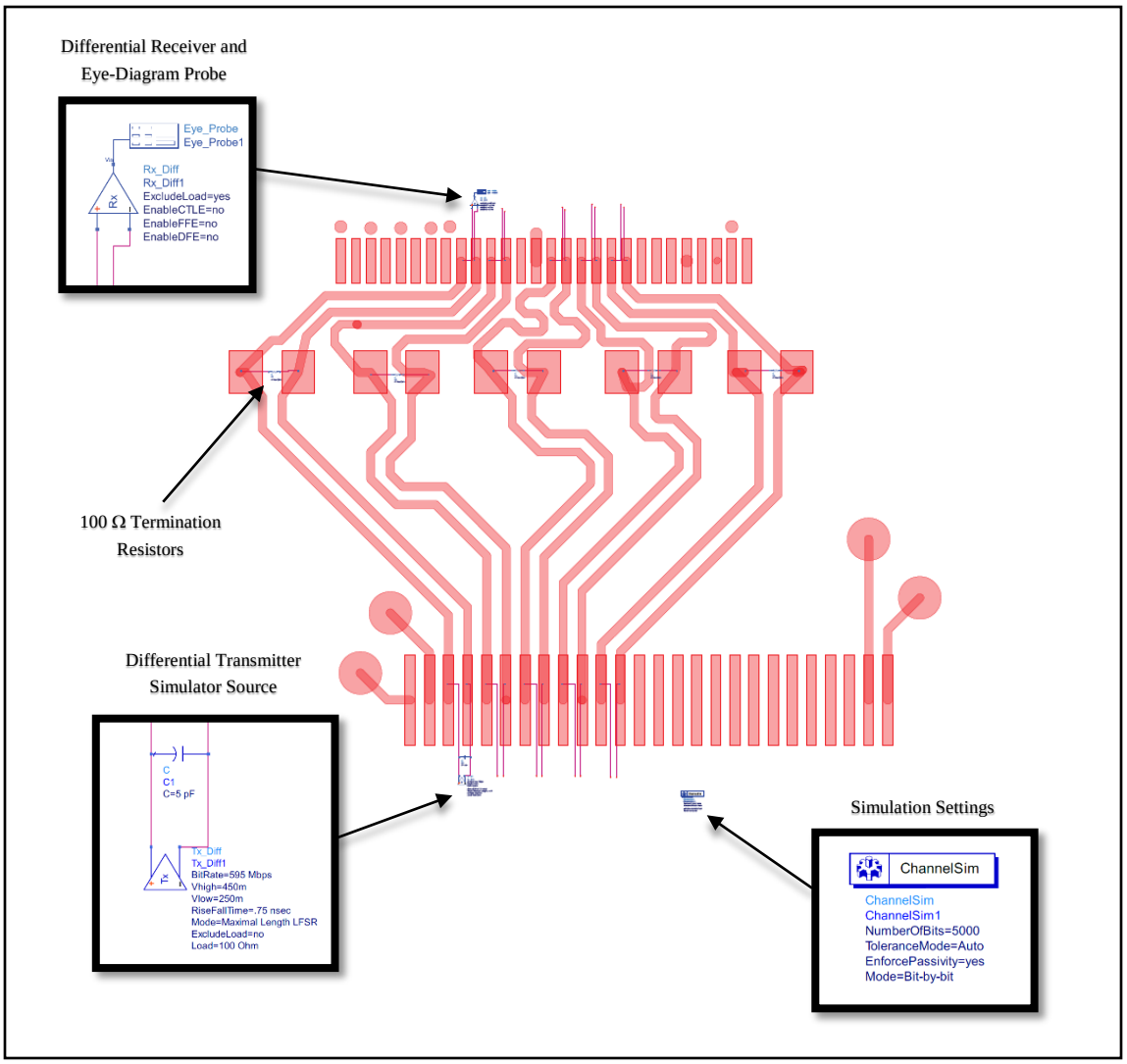

Figure 19: ADS Eye-Diagram Simulation Test Configuration for LVDS Board layout Traces

The result of the test demonstrated in Figure 19 is shown in Figure 20, where the eye of the persistent diagram looks quite “open” and therefore implies the design should work as expected. Further, one will note that the test shown is only one of the five LVDS lines. This is because ADS only allows one eye diagram simulation/test at a time. A test of each LVDS line was performed individually and demonstrated similar enough results that they were omitted due to not offering any reasonable value to this analysis/discussion.

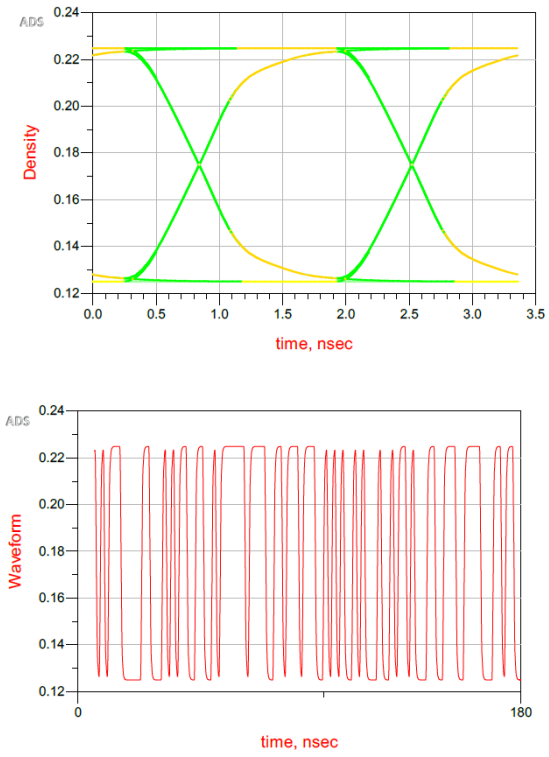

Figure 20: Simulation Eye Probe Diagrams for Camera Link Interface LVDS Trace Testing

Once the testing of the LVDS lines were completed, the twenty eight CMOS lines needed to be tested as well. This test, again used the EMI simulation capability of ADS software. However, this test now looked not at the reflection noise of an individual line but the crosstalk between adjacent traces (as these lines are single ended, not differential, and will therefore be notably more susceptible to this type of noise). This test follows the same procedure as the LVDS test (as discussed above), but used different transmitter/receiver test components in the ADS Schematic software. The test configuration is shown in Figure 21, where again, the information concerning the timing, voltage and loading parameters of the DS90CR288A were taken from its datasheet (Texas Instraments, SNLS056G). However, the input load information of the Zynq was not readily available in any documents that are freely distributed by Xilinx and so they were contacted to

request an IBIS model. The request was subsequently denied without reason and so the common CMOS input capacitance of 5pF was assumed, in order to complete the test.

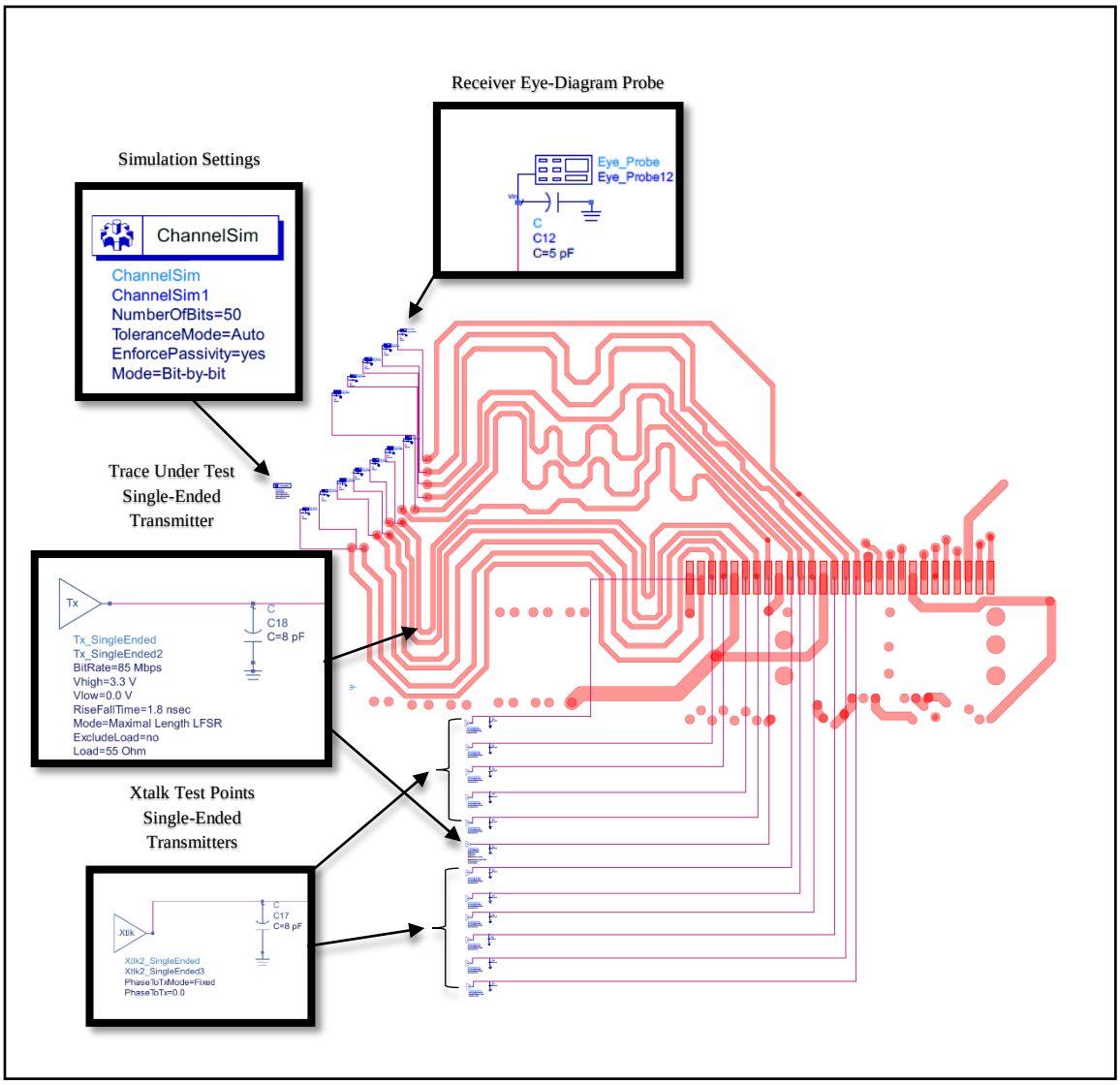

Figure 21: ADS Crosstalk Simulation Test Configuration for CMOS Board Layout Traces

As one will note from Figure 21, ADS simulates the EMI between a single trace of interest and coupled sources. The trace highlighted in the figure was selected (out of the twenty-eight others) to demonstrate this testing, since it is the worst-case trace (for crosstalk), due to its geometry and relation to other traces. The results of the test are demonstrated in Figure 22, where one will note,

that the trace under test (Channel 6) is causing interference noise on directly adjacent traces, which is to be expected. Further, the results of the worst trace example, demonstrate that the design is reasonably sound as the eye diagrams are wide (open).

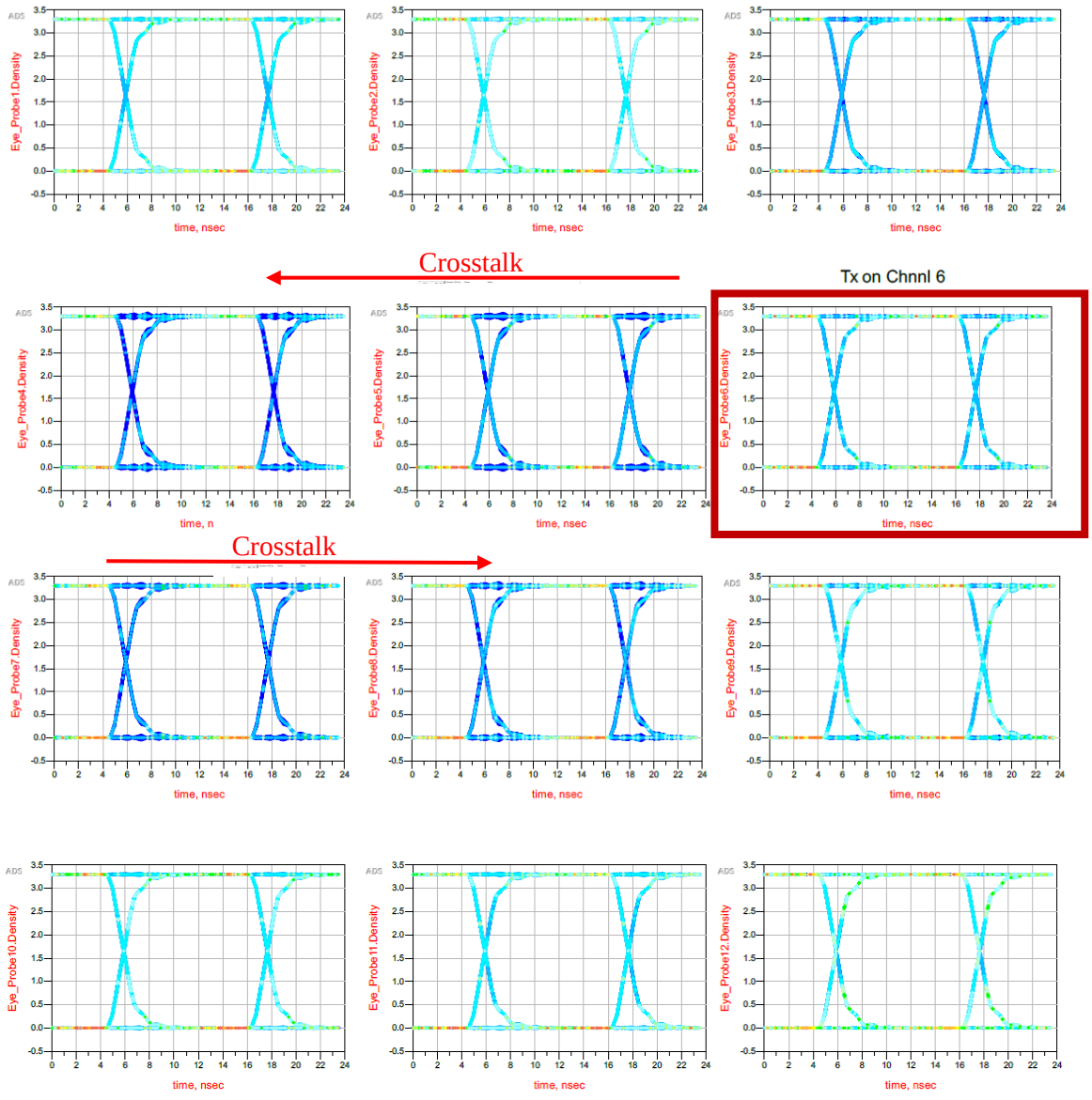

Figure 22: Simulation Eye Probe Diagrams for Camera Link Interface CMOS Trace Testing

4.4.SD Card & External Signals

4.4.1. SD-Card

As stated in Section 3.3.3, Micro SD flash was selected for the non-volatile external storage required for the ZPS-Board. This memory circuit (shown in Figure 23) is comprised of Micro-SD push-push connector, a series termination resistance (not shown) on the SD clock line and a resistor pull-up/pull-down network on the card detect pin.

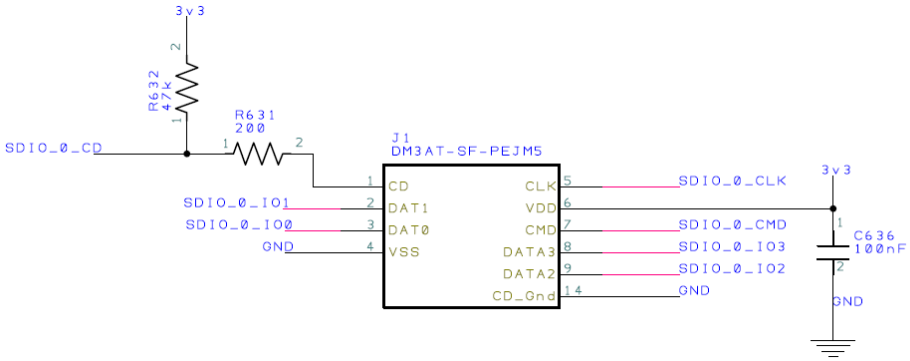

Figure 23: SD Card Connector Circuit Schematic for the ZPS-Board

The most complicated portion of this circuit is the layout of its traces. The traces needed to be length matched to less than 3mm (≈20ps) skew (Toradex), based on the Zynq's max SD frequency of 50MHz (Xilinx, TRM). See Figure 24 for the SD memory circuit layout.

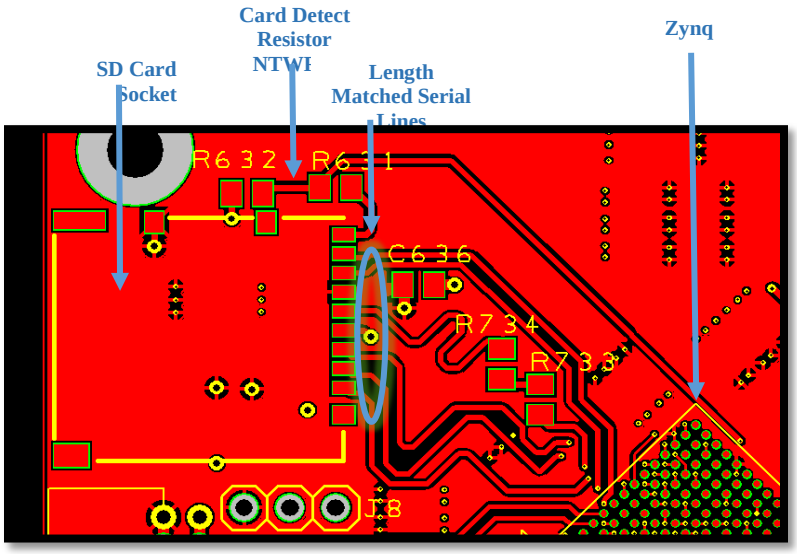

Figure 24: SD Card Connector Circuit Layout Top Layer of the ZPS-Board

4.4.2.Debug, Communication and Configuration signaling

It is worth briefly discussing the layout of the communication, debug and configuration signaling, previously defined in Section 3.4.2. These signals, are all relatively slow and are therefore simpler to layout then the aforementioned signaling. The signals run on three different layers and can run up to the full length of the ZPS-Board (Figure 25 offers a demonstration of some of this signaling). Due to this fact, providing a good idea of how these signals are laid out with simple figures would not be very useful. Therefore, please see Appendix III – Board Layout, for full-layer layouts, in order to get a better sense of how these traces were incorporated into the ZPS-Board layout.

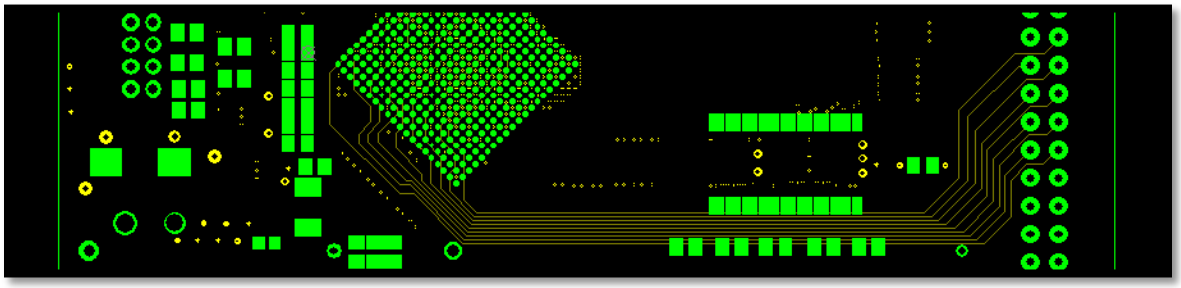

Figure 25: Inter-board Trace Signaling Example on the ZPS-Board

4.5.Zynq

Up to this point in the document, the Zynq SoC has been discussed considerably, but with respect to its relation to other devices. This section focuses instead on the Zynq SoC in regards to the properties that define it as a standalone element within the ZPS-Board. The Zynq SoC is a monolithic IC that had a significantly large amount of considerations that needed to be taken into account when designing its supporting circuity and layout.

4.5.1.Zynq Power/Bypassing

Figure 26 demonstrates the Zynq's power banks for each required voltage rail (please refer to Table 3 on page 17 for descriptions of each bank)

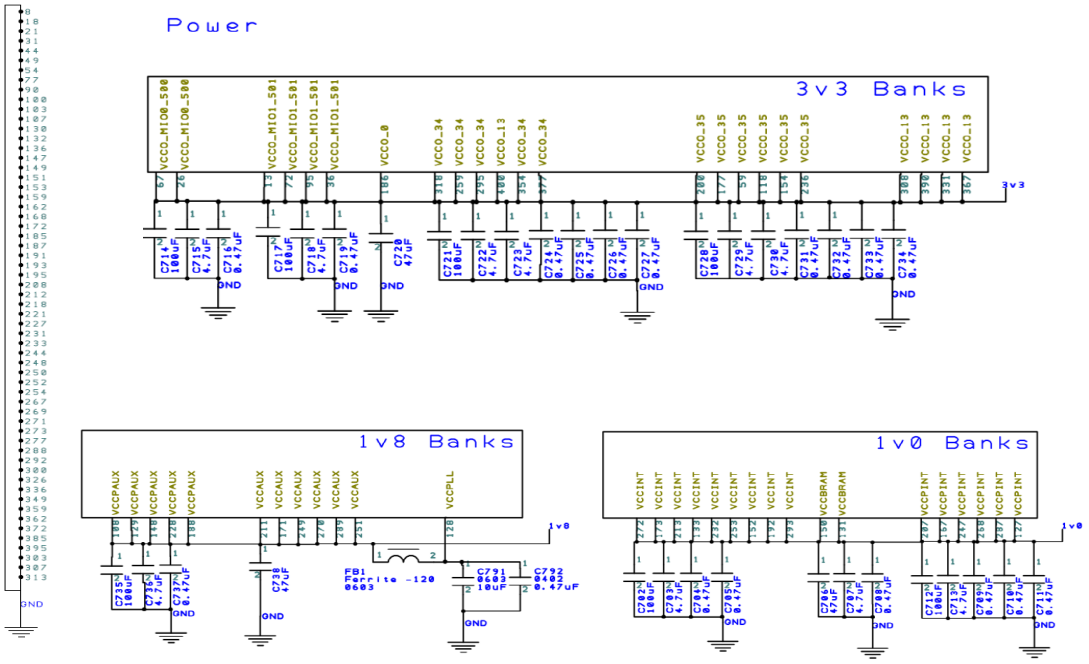

Figure 26: Zynq Power Banks Schematic for the ZPS-Board

As one will notice from Figure 26, there is a considerable amount of capacitor-bypassing required for the Zynq. The amount and sizing of the required bypass capacitors was determined from the Xilinx's ug933 document (Xilinx, UG933). The placement of these capacitors with respect to the Zynq is also described within the ug933. Bulk capacitors (C>4.7μF), are for low enough frequency that there location on the PCB with respect to the Zynq is relatively inconsequential. Mid-band frequency capacitor (4.7μF≥C>0.47μF) placement has some impact based on locality and needed to be within two inches of the Zynq's outer edge in order to be effective. Lastly, the high frequency capacitor (C ≤0.47μF) placement is critical and needed to be within half and an inch of the Zynq's outer edge.

In order to decrease the inductance in the path of the bypass capacitors to the Zynq, all the capacitors are connected on the bottom layer (layer 5) of the board. Figure 27 demonstrates the bypass capacitor layout placement on the ZPS-Board.

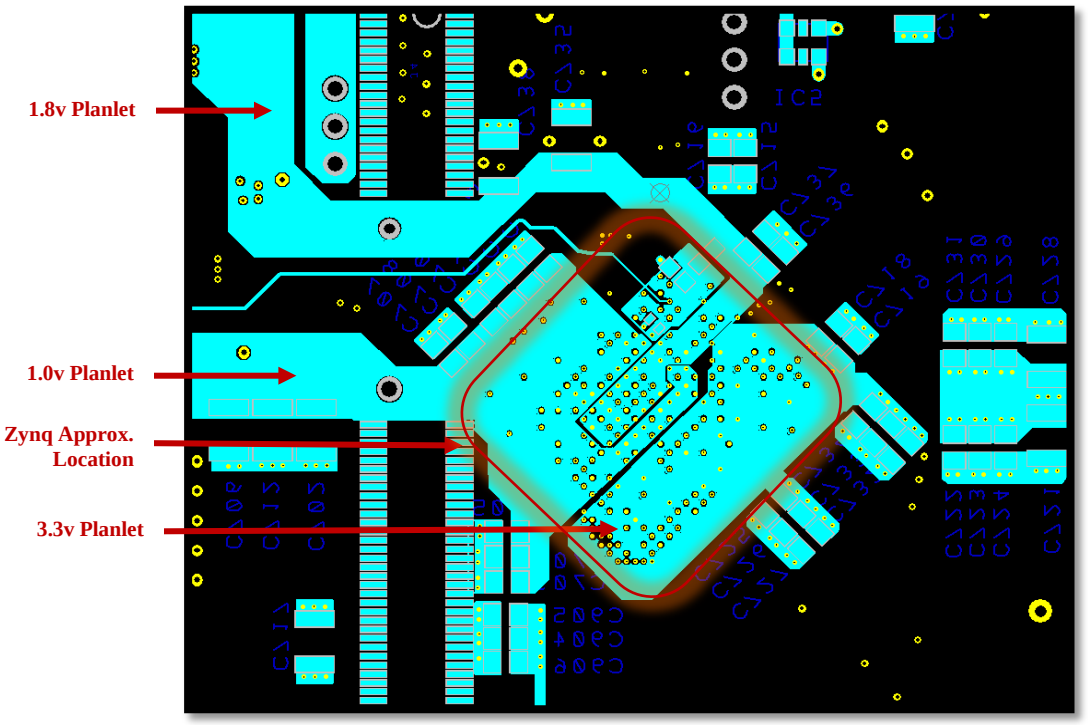

Figure 27: Zynq's Bypass Capacitor Layout Placement for the ZPS-Board

Due to the extreme sensitivity of the Zynq's phase locked loop's (PLL) to its supply voltage and that is shares the rail with V_{CCPAUX}, the input of the supply to the PLL had to be filtered. In order for the filter (Figure 28) to be most effective it had hard constraints given in Xilinx's ug933:

- Input connected to rail through120Ω at 100MHz ferrite bead
- 10µF bypass capacitor be an 0603 and the 0.47µF bypass capacitor 0402 or smaller
- Connection of the 10µF and the V_{CCPLL} pad is 2mm width min and less than 76mm long
- The 0.47µF has a minimum of 5.1mm trace length between the V_{CCPLL} and ground vias

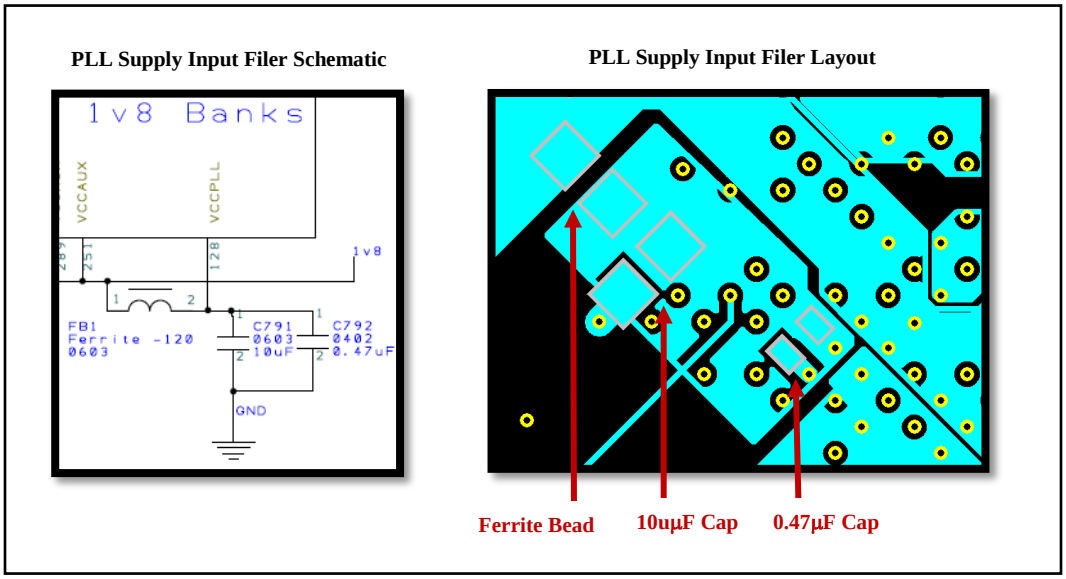

Figure 28: Zynq's PLL Input Supply Filter for the ZPS-Board

4.5.2.Zynq Configuration

There are several configuration pins on the Zynq that needed to be set in accordance with its intended use on the ZPS-Board. A schematic demonstrating how each pin is configured is shown

in Figure 29**.** A table defining what each pin means is given in Table 7 for quick reference. For more detailed information about each pin, please refer to Zynq's TRM (Xilinx, TRM).

Most configuration of the Zynq is all hard set into the ZPS-Board design and cannot be changed post fabrication. However, the boot-mode is one option that is reconfigurable by the end user. The boot-mode pins have a circuit attached to them, which allows for the selection of either JTAG or SD. These two modes are selectable via a jumper (J8) on the ZPS-Board, which effectively ties pull-up/pull-down resistors to achieve their setting. See Figure 29 and compare to the boot-mode selection matrix in Table 7 for more information.

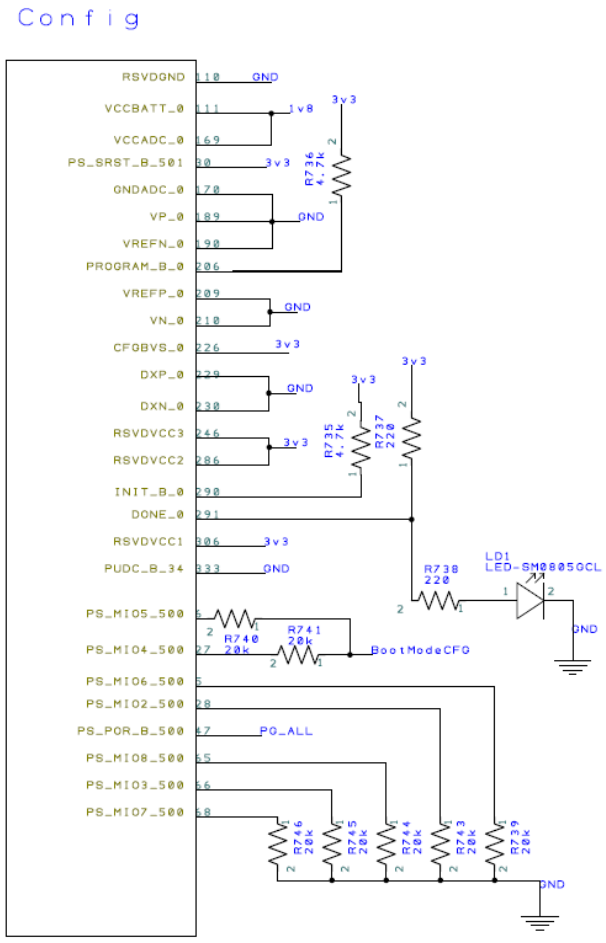

Figure 29: Zynq Configuration Schematic for the ZPS-Board

Table 7: Zynq Configuration Definition Table (Xilinx, TRM)

PUDC_B	DONE	PROGRAM_B	INIT_B
Pull-Up During Configuration (bar) Before and during configuration, PUDC_B is an active-low input that activates the internal pull-up resistors on the unconfigured SelectIO pins.	Done A High signal on the DONE pin indicates completion of the configuration sequence. The DONE output is an open-drain output by default.	Program (bar) Active-Low reset input to configuration logic. When PROGRAM_B is pulsed Low, the FPGA configuration is cleared and a new configuration sequence is initiated.	Configuration Banks Voltage Select CFGBVS determines the I/O voltage operating range - Connect CFGBVS=GND for VCCO_0 of 1.8V or 1.5V. - Connect CFGBVS=VCCO when VCCO_0 is 3.3V or 2.5V.

PS_POR_B	FGBVS	PS_SRST_B_501
Power on Reset See power on sequence under 4.1.1 for related info	Initialization (bar) Active-Low FPGA initialization pin or configuration error signal.	External System Reset Pulses to Perform a system Reset

Dedicated Pins:	**RSVDVCC#** **RSVDGND** **VCCBATT**	Tied to associated rail (Battery holds security keys)
Pins Required To Be Tied:	**VCCADC** **GND_ADC** **VP** **VN** **VREFP** **DXP** **DXN**	Internal ADC not used

Configure the MIO Bank Voltage Mode:	**PS_MIO7** **PS_MIO8**	High=2.5v,3.3v Low=1.8v	Bank 1 =MIO8 Bank 0 =MIO87
PLL Enable/Disable:	**PS_MIO6**	Active low	
JATG Chain Routing :	**PS_MIO2**	0: Cascade Mode 1: Independent Mode	

Configure/Select the Boot Device:	**PS_MIO3** **PS_MIO4** **PS_MIO5**		**MIO 3**	**MIO 4**	**MIO 5**
		JTAG	0	0	0
		NOR	0	0	1
		NAND	0	1	0
		Quad-SPI	1	0	0
		SD	1	1	0

4.5.3.Zynq External Oscillator

The Zynq requires a 3.3v CMOS based high frequency external oscillator/clock generator in the range of 30MHz to 60MHz. The DSC1121CL5 50MHz, microelectromechanical (MEMS), low jitter, external clock generator, was selected as the external clock source due to its high stability over the temperature range (±10ppm, -40 to 105°C) required for the ZPS-Board (see Section 3.2.2) (Micrel). In order to isolate the source clock signal from noise, the external clock was placed on the bottom layer of the board, away from signal noise on layers zero, two, and three. Additionally, the generator was placed as close to the Zynq clock input pin as possible (See "Appendix III – Board Layout" layer 5 for a more relative perspective of the external clock's (IC5) placement).

4.5.4.Zynq I/O Signaling

Prior to this point, the signaling on the ZPS-Board has been discussed more with respect to their use by the peripherals to the Zynq. To get a perspective of the I/O signaling usage of the Zynq, refer to Table 8.

Table 8: Zynq IO Signaling Usage Required for the ZPS-Board

	PL SELECTIO PINS	**PS MULTIPLEXED I/O**
I/O AVAILABLE ON THE ZYNQ XC7Z010-2CLG400I	100	128
I/O USED ON THE ZYNQ FOR THE ZPS-BOARD	35	32

4.6.Some Key Fabrication Considerations

4.6.1.Zynq BGA Breakout

Since the Zynq being used (XC7Z010-2CLG400I) is a four hundred pad, ball grid array (BGA) package, with 0.8mm pitch, fabrication of the ZPS-Board had relatively advanced needs (Xilinx, UG865). There are two common methods to break out the pins from a dense BGA area, “dog-bone” or “via-in-pad”. Via-in-pad is a BGA breakout method where a via is placed directly in the landing pad of the BGA. This approach requires that the PCB fabricator drill the via, plate it and then plug the top. Needless to say, since this is not a simple or common fabrication technique, it is quite costly. However, it is the most ideal method, since there is no space sharing under the package. Dog-Bone method (Shown in Figure 30), is where the BGA landing pad is connected to a via placed in the open space directly next to it. This method is less than ideal, since it uses more space underneath the package and creates space contention when attempting to layout traces. However, this method is relatively inexpensive, since it doesn’t require advanced fabrication techniques. Both methods unfortunately, still have an inherent issue due to the nature of high-density BGAs. In order to break out the pads of a BGA, the via landing diameter, in coordination with the trace width and/or air-gap (fabricator’s) minimums, must be sufficiently small enough to allow the traces to snake through the vias. Based on these fabrication consideration, the costs for the ZPS-Board was considerably higher than normal and the dog-bone method was used for pad breakout in order to minimize this cost.

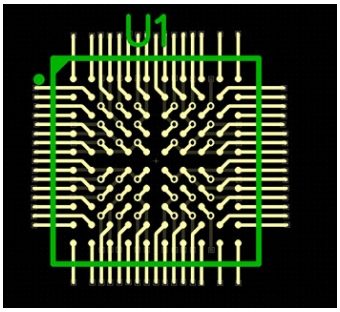

Figure 30: Dog-Bone Break out Method Example (Embeddded)

4.6.2.Camera Link Connector

Camera Link cabling connectors come in two types, Mini Delta Ribbon (MDR) and Shrunk Delta Ribbon (SDR – sometimes referred to as HDR, High Density Ribbon). Due to the size of the MDR's footprint (11.40x38.2mm) only the SDR connector ended up being reasonable for the ZPS-Board (at 10.7x28.2mm). Additionally, when the ZPS-Board is fully integrated into a CubeSat, the sides of the board will be butted up to the housing and therefore will not allow for edge of the board connectors to be matted to anything (assuming a vertical stack of the CubeSat). Due to this presumed use of the ZPS-Board, the most reasonable way to connect a science instrument to the Camera Link interface would be vertically. However, this vertical connection proved to create problems in the design when it was discovered that only one company (3M) manufactures these types of connectors. 3M, only offers one vertical facing connector and it is through-hole. Even more problematic, is that the connector has a 1.4mm pin-pitch. With a 1.4mm pin pitch and an advised pad diameter of 0.9mm, one is only left with 0.5mm air gap in which to breakout the pins. With the chosen manufactures design requirements of 5mil air gap and 5mil minimum trace (Bay Area Circuits Inc.), this made the layout almost impossible without breaking out the pins across multiple layers (which negatively affect impedance matching). Therefore, it was decided that a right angle surface-mount connector from 3M would have to be used. The board connector was backed off from the edge of the board such that a right angle cable connector could be connected with enough clearance to not overlap the potential CubeSat housing. A side profile depiction of how this connection would work is shown in Figure 31.

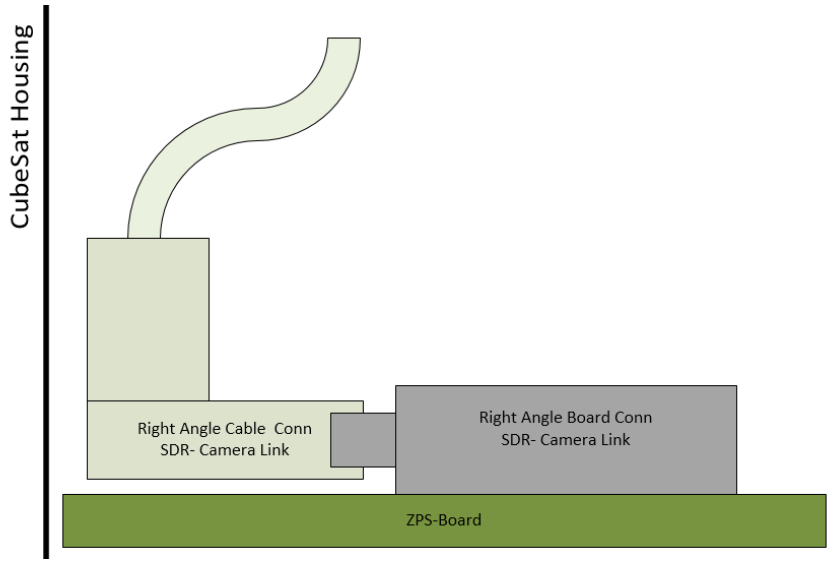

Figure 31: Example of Right Angle Connectors Used for the Camera Link Board Conn. on the ZPS-Board

4.6.3.Tyvak vs PC/104

As previously discussed in Section 3.2.1, the form factor followed in the design of the ZPS-Board was the PC/104. Also previously noted, the Tyvak board form factor was also taken into consideration, such that only minor changes to the layout would be needed in order to quickly refabricate a Tyvak version of the ZPS-Board. Since the Tyvak form factor is smaller than PC/104, this resulted in less useable space. This can be seen in Figure 32, where the board outline of the PC/104 based ZBS-Board is marked in green and the Tyvak is marked in yellow. One of the largest constraints that adhering to this additional form factor created, was due to its center of the board connectors (shown in Figure 32 as the long dense array of pads spanning the center of the board). Even though the Tyvak connectors were on the bottom of the board and not through-hole, they could not be over top of the Zynq, due to its considerable amount of vias. This resulted in having to move the Zynq from the ideal location, in the direct center of the board, to one side. This made

the layout considerably harder in attempting to keep the noise created by the Zynq away from the ADC circuit. Additionally, this created an even more cramped layout area around the Zynq.

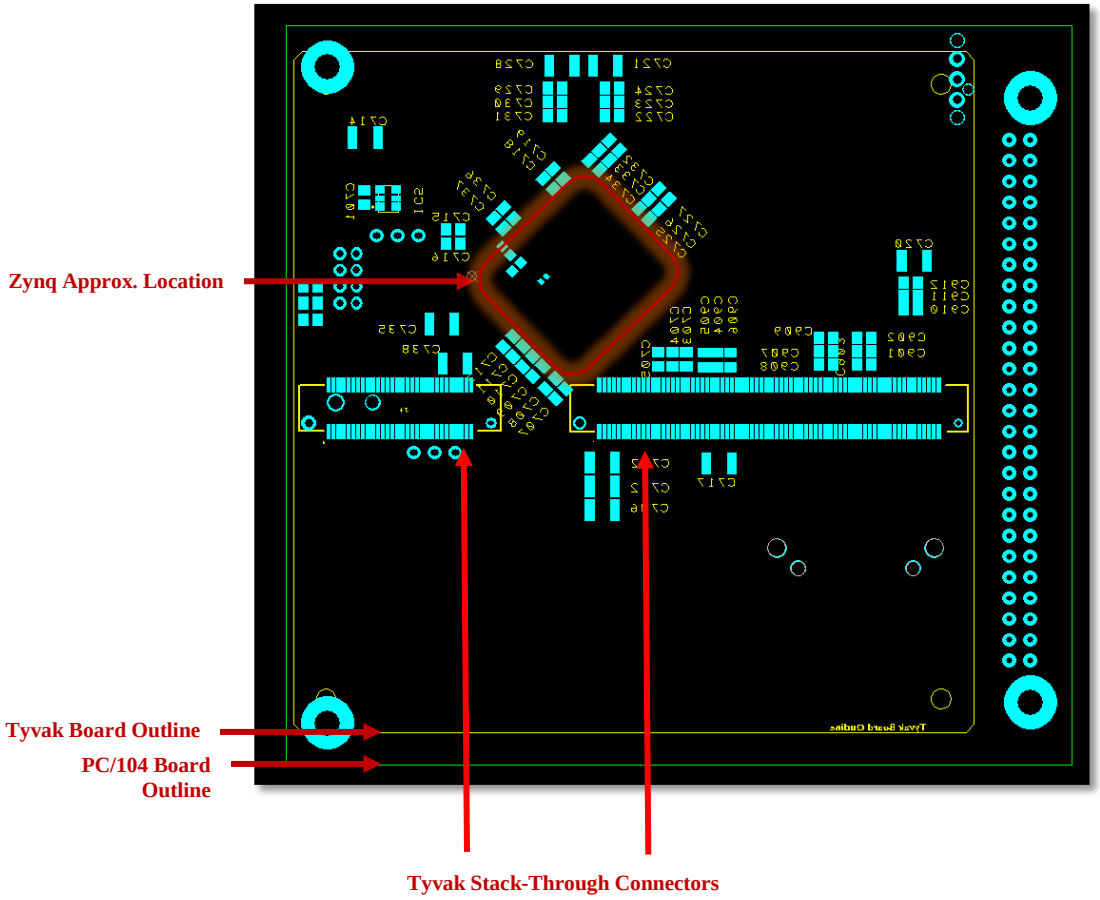

Figure 32: PC/104 Form Factor vs. Tyvak Footprint of the ZPS-Board (PC/104 Board Outline: Green Tyvak: Yellow)

5. FABRICATION

Due to the discovery that the small pin-pitch of the Zynq (0.8mm) drove up the cost of fabrication considerably (relative to the projects budget), a lot of searching ended up being required to find a fabricator that would be fiscally plausible. Ultimately, one was found at the price of $783.00 with design rules of 5mil trace, 5mil air gap, 6mil drill and 3mil annular ring which would allow for required breakout of the Zynq pads. The complete fabricated board is shown in Figure 33 (Bay Area Circuits Inc.).

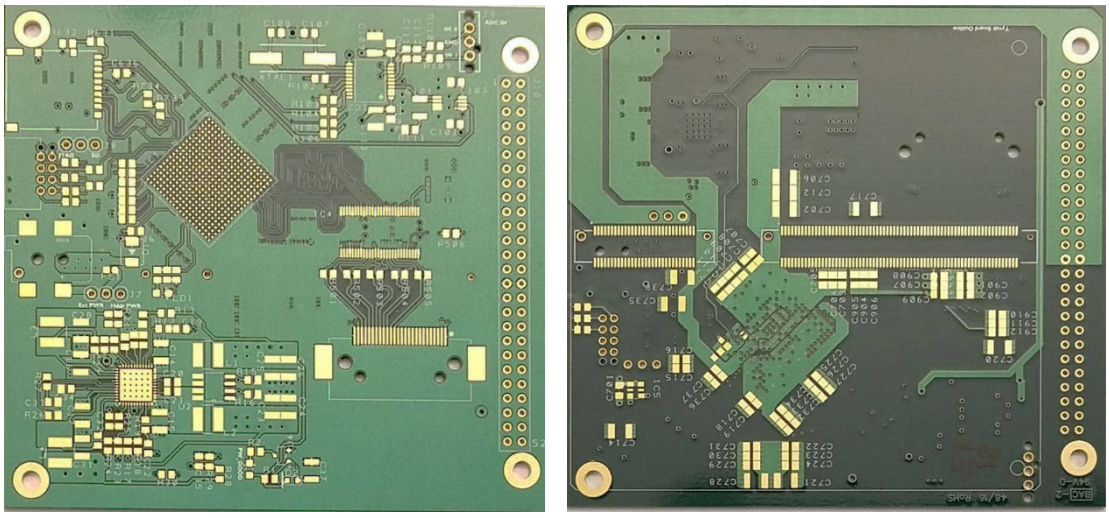

Figure 33: Example of the Fully Fabricated (Unpopulated) ZPS-Board

The board was populated by hand using a manual pick and place machine built using a syringe and a modified fish-tank air pump. The Zynq's board contact pads were tinned but not populated in order to perform initial testing of the power circuit without the added possibility of shorts that the Zynq packaging and layout complexity created. The populated board was then reflowed using a standard reflow oven. The results are shown in Figure 34 and Figure 35. Since the bottom of the board (Figure 34) was the simplest in terms of the components, it was the first populated and allowed for testing the process. The top side was then populated and reflowed (Figure 35).

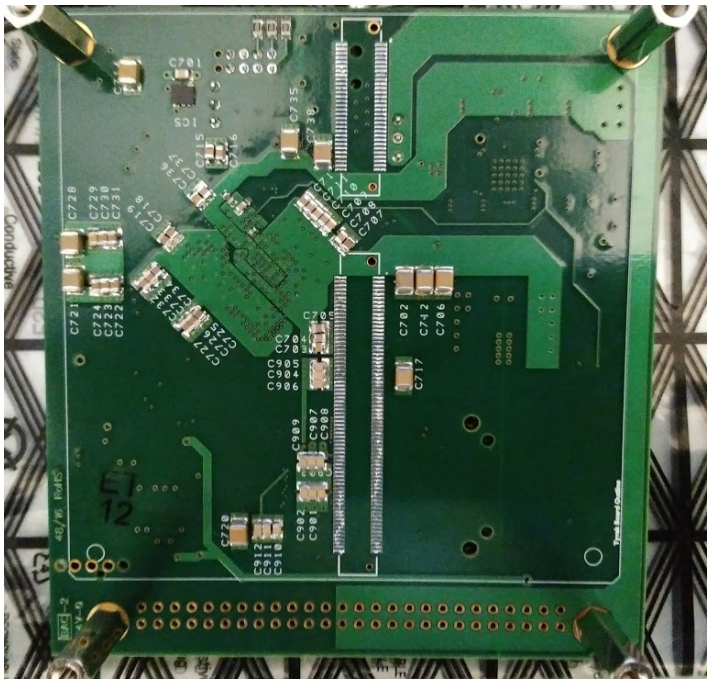

Figure 34: Population of the ZPS-Board -- Initial Population and Reflow Bottom Side

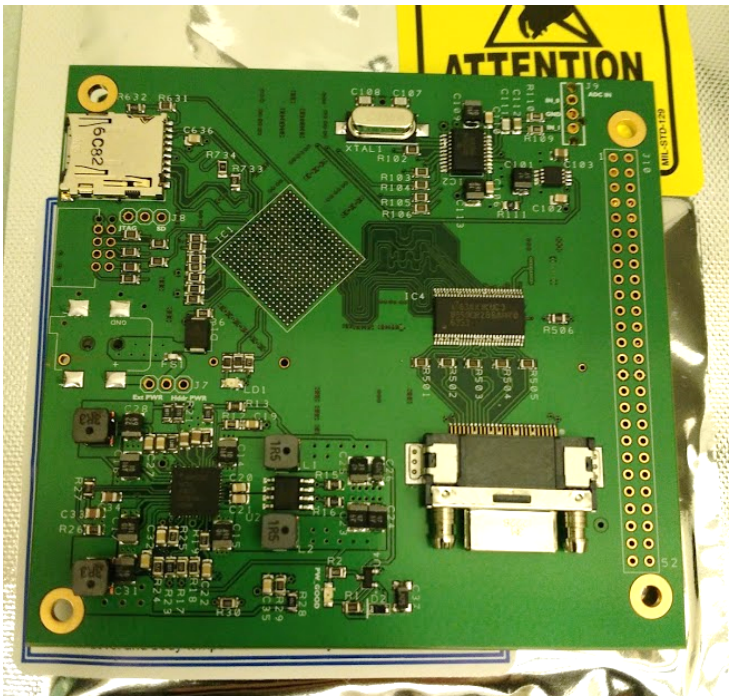

Figure 35: Population of the ZPS-Board -- Initial Population and Reflow Top Side

After completing the reflow process, the board was then worked by hand to correct any solder-shorts that were created during the reflow solder process and to add any through-hole components/connectors

Once the board was populated (aside from the Zynq), the power circuit needed to be tested to insure it was functioning as it should and was meeting specifications. Test inputs were attached to the ZPS-Board as shown in Figure 36, where the red is 5.0v and black is 0v (ref).

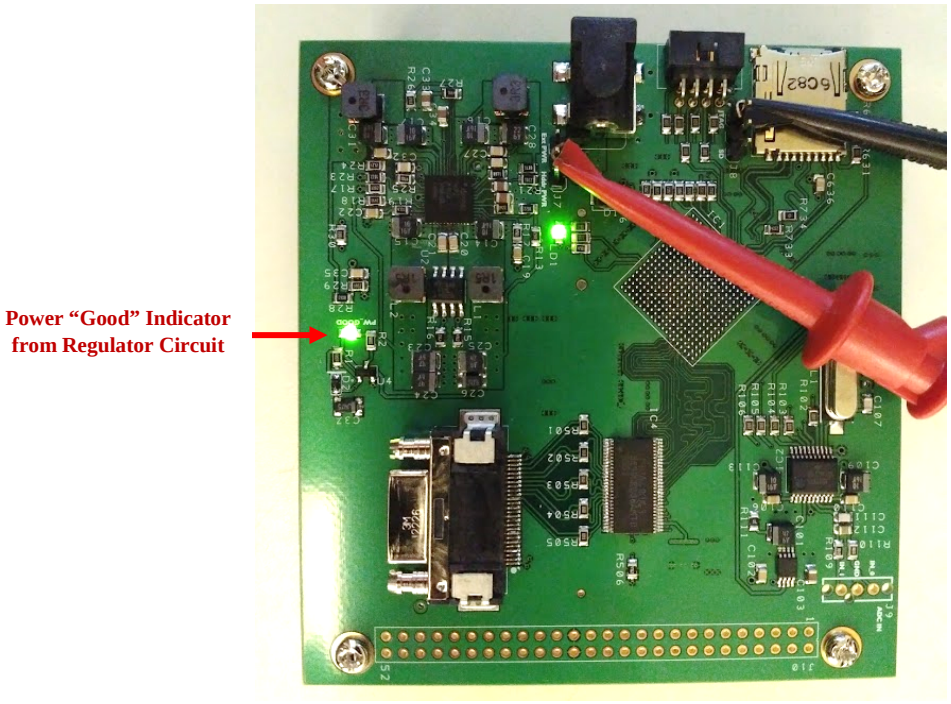

Figure 36: ZPS-Board Initial Testing of the Power Supply Circuit

Once powered up, the power-good illuminated as expected, indicating the regulator (ADP5052) was up and reading nominal output voltages. The supply voltages were then measured by probing the supply circuit's output capacitors and were found to be within their respective nominal ranges (unloaded) and are shown in Table 9.

Table 9: Measured Supply Voltages for Unloaded ZPS-Board

UNLOADED MEASURED SUPPLY VOLTAGES

NOMINAL	3.3v	1.8v	1.0v	1.5v
MEASURED	3.2905v	1.79900v	0.99697v	1.49060v

Once there was certainty in the power supply circuit, the Zynq was then attached to the board. The Zynq was manually attached to the board through the use of a heat gun. This was done by applying tacky flux to help insure the Zynq would stay relatively static, while applying the heated air (as well as perform its normal function of aiding the solders reflow). The heat gun was held approximately six inches away from the Zynq package and was moved in a circular pattern to insure heat was properly spread across the whole package. Proper setting of the Zynq's pads was insured by visually observing complete reflow of the Zynq's solder balls and previously tinned pads on the board. The fully populated board is shown in Figure 37.

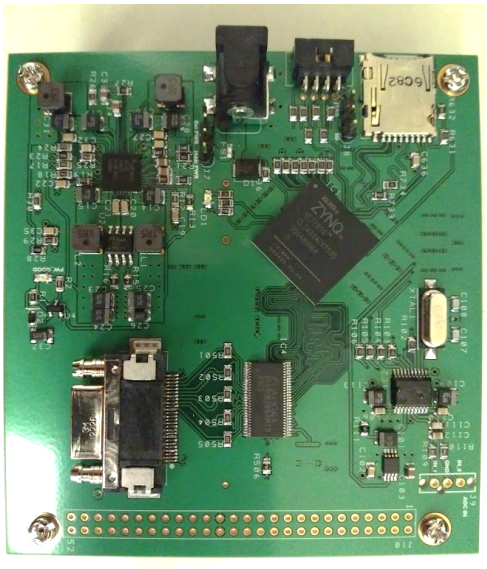

Figure 37: Population of the ZPS-Board – Completed (With Zynq) Top Side

6. DESIGN TESTING

6.1.Initial Power Up of the Full ZPS-Board

Upon initial power up of the ZPS-Board, the results looked good. The board was drawing 0.105W and the appeared stable. In order to insure that the Zynq was fully powered and functioning as expected, a JTAG interface was needed. A USB to JTAG device from Digilent called the HS2 (Rev. A) was used to perform this task and was connected to the ZPS-Board as shown in Figure 38.

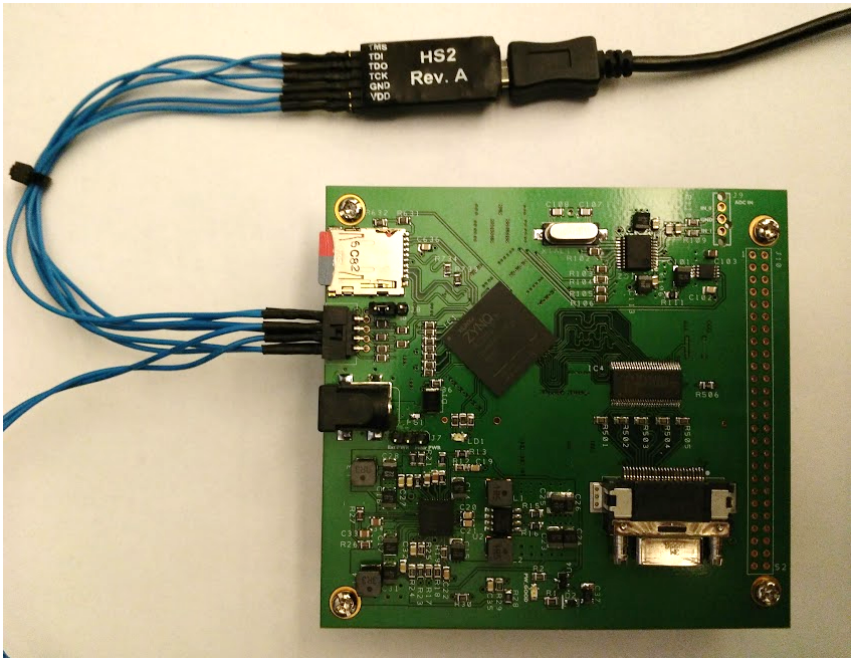

Figure 38: Example of Digilent's HS2 JTAG Interfacing for ZPS-Board

Upon connecting the JTAG interface and attempting to communicate with the Zynq, only the PL (FPGA) was visible on the JTAG chain. During this testing and attempting to determine why the ARM processors were not communicating over the JTAG, a new error arose. The power good signal from the power circuit shut off and the supply circuit on the board cutout power to the rest of the board.

Upon probing the supply outputs of the power circuit, a pulsating waveform was observed. This phenomenon was then referenced to the datasheet of the ADP5052 and it was discovered that it resembled an over-current protection state called “hiccup protection” (Analog Devices). Hiccup protection is entered into when the regulator detects an over-current event. Once entered, the regulator turns off the high and low side FETs for a period equal to seven soft start cycles and then attempts to bring the system back up. This repeats indefinitely until an over-current is no longer observed. The over-current protection is set via R_{15} and R_{16} for channel 1 & 2 respectively (see the schematic in Figure 8 (pg.21)). The resistors were set at 47kΩ to constrain the peak output current to 2.64A. Since output current ripple is very hard to observe in a closed system, it was not plausible to confirm that ripple larger than expected was causing a false over-current event. To test that large ripple was not causing the problem (but not considered a perfect verification), the over current resistor was replaced with a 22kΩ, which set the max current to 6.44A. Upon increasing the current limit, a test was performed to determine if the problem persisted. The device again failed and entered into its hiccup mode as before.

In continuing to investigate the cause of the system failure, there was one other behavioral clue observed. It was noticed, that the device did not always immediately enter this hiccupping state and exhibited an interesting characteristic. When the board was left off for twenty-four hours, the power circuit would come up nominal for approximately two minutes before going into the hiccupping state. Once the system went into the hiccupping state and then subsequently had its external power removed for a short time, the ADP5052 would enter the hiccupping state with less delay each time the board was reenergized (eventually entering the state almost immediately every time). This behavior seemed to imply that it may have been thermally related, but ADP5052 (regulator IC) was cool to the touch and has a thermal shutdown of 150°C (Analog Devices).

While performing a slew of simple guess-&-check tests to determine the root cause of the problem, an over-voltage incident on the ZPS-Board external supply occurred, which irrevocably damaged the ADP5052. This event led to the necessary removal of the ADP5052 IC from the ZPS-Board. While waiting on a replacement, testing was continued, but now with each power rail supplied by a bench-top power supply (something that was not acceptable when the ADP5052 was still on the board). This event and resulting tests were extremely revealing. The Zynq was now fully showing up in the JTAG chain (both PS and PL system). An initial scan of the Zynq was performed using Digilent's Adept and reported both the FPGA and the ARM. The resulting report can be seen in Figure 39.

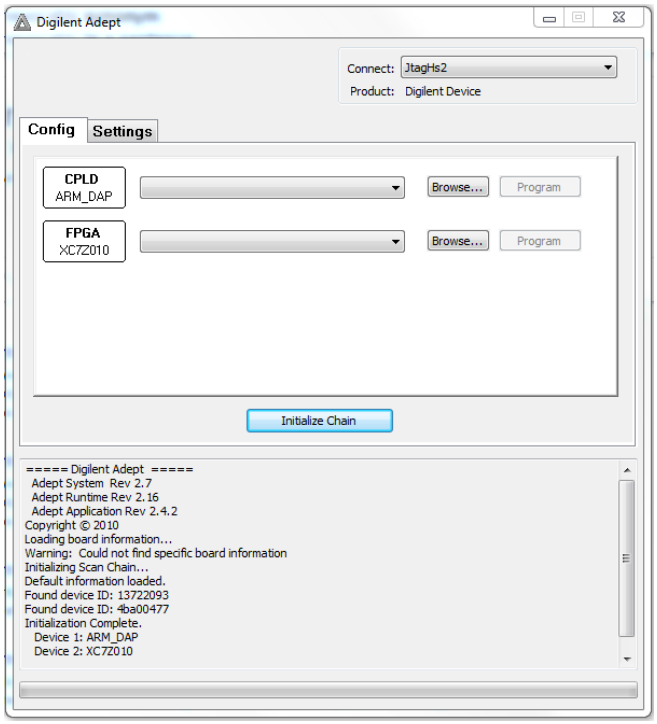

Figure 39: Report of Successful JTAG Chain Scan Demonstrating Full Communication with Zynq

Additionally, the benchtop supply allowed for more control over the supplied current. The max output current was set to 0.5A (below the OCP setting) and it was discovered that allowing the system to run for a period of time, the 3.3v supply ramped up to the 0.5A (a current draw much

higher than it should have been) and the supplied output voltage began to sag. It was now clear that something on the board was in fact drawing a considerable amount of current.

In order to determine component(s) that were drawing large amounts of current, a thermal camera was used to observe the board as it was running. The Zynq was observed to be giving off a considerable amount of heat, as it was to be expected. However, there was also one other place on the board that was noticeably warm. It was observed that the output of the 3.3v supply was glowing and as it turn out, was the source of the problem.

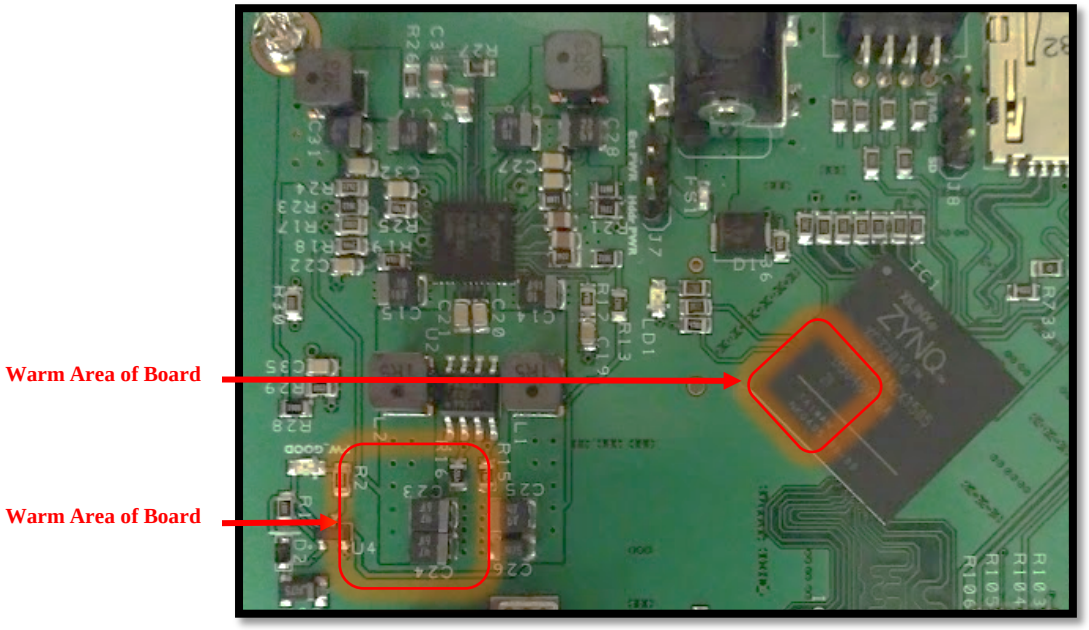

Figure 40: ZPS-Board High Current Draw Testing Using Thermal Camera Observed Thermal Hotspots

As one might note, the output capacitors on the 3.3v supply are tantalum and the bar on their packaging designates the anode of the polarized capacitor. The tantalum capacitors were attached (as they are in the image) with the anode connected to ground and were therefore reverse biased. The reverse breakdown of this capacitor on the 3.3v rail explained the entire previously observed phenomenon. In fact, as further research revealed, even the time-based/thermal behavior noticed

earlier, was caused by this. A study by QSS Group & NASA on the effects and behavior of reverse biasing tantalum capacitors, found that their breakdown behavior is tightly tied to time, temperature and the reverse bias potential relative to its forward voltage rating (Teverovsky). This explained the behavior observed throughout the testing and why the 3.3v supply output capacitor appeared to be the only one in breakdown (even though all the tantalum capacitors on the board were placed incorrectly) since its forward voltage rating was (6v) and the applied reverse voltage was 3.3v (55%). Whereas, the rest of the tantalum capacitors were being reverse biased much lower than their respective forward rating. Once all the tantalum capacitors were replaced (along with the previously damaged ADP5052) and properly oriented, the board operated nominally.

6.2.Reading & Booting from SD-Card

Now that the board was powering up nominally, the first Zynq software level test was to verify booting from the SD-card. Testing SD-card booting in fact verified two things, the proper boot-up of the Zynq, as well as, the communication path between the SD-card and the Zynq.

Initial tests were quite promising. A Zynq boot .bin file was created using Xilinx's Vivado and was comprised of three partitions. The first partition, was Xilinx's 2016.2 First Stage Boot Loader (FSBL). The other two partitions were simple test files. The .elf, was a simple "Hello World" type application and a basic bit file was used, to verify configurability of the FPGA. The FSBL was modified slightly in order to monitor the boot process via command-line outputs, by defining "FSBL_DEBUG_INFO" in the "fsbl_debug.h" file. The UART output came from ZPS-Board's external connector J6 and was connected to a PC through a FT2232H UART to USB breakout board. Upon power up, the Zynq read the FSBL file from the SD-card and properly identified its contents (as well the jumper J8 setting to boot via SD – later moved to JTAG to verify the other option was also correctly read) as shown in Figure 41.

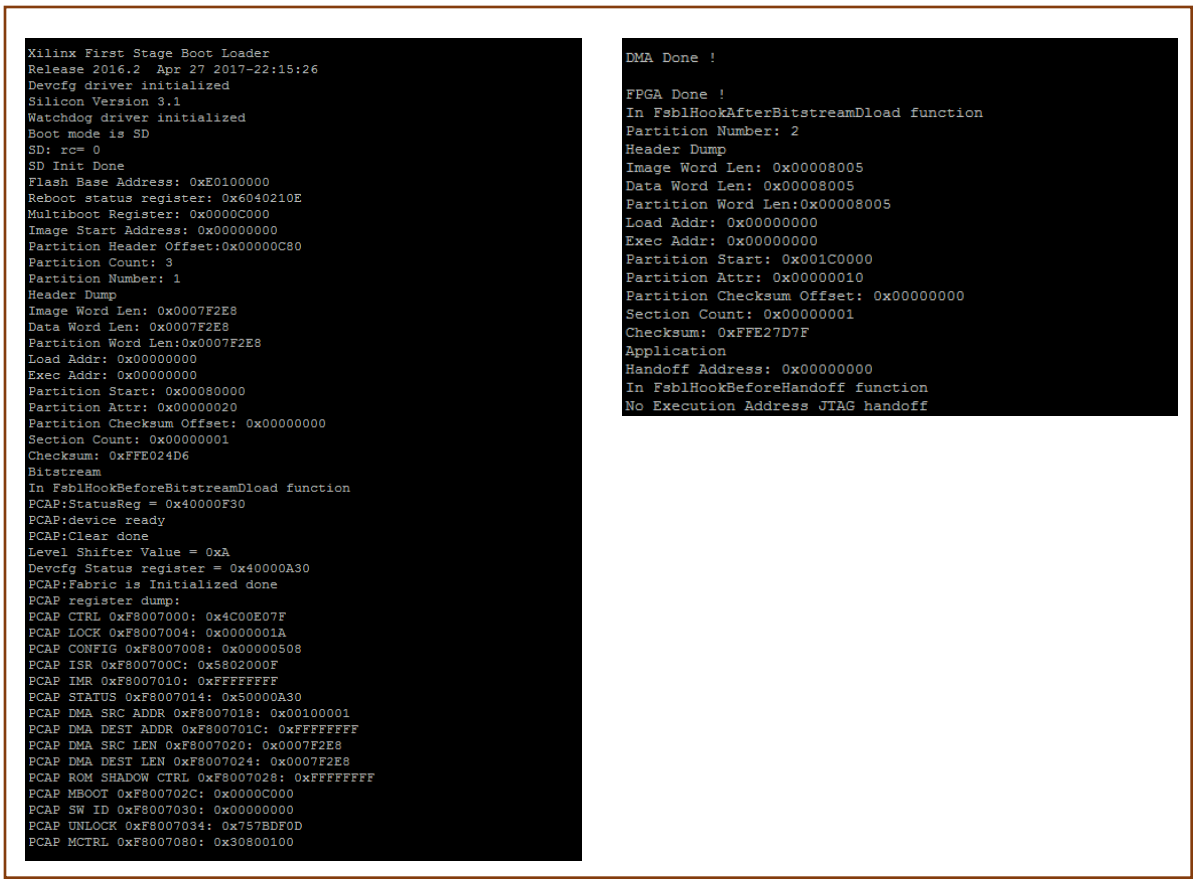

Figure 41: ZPS-Board Boot Testing -- Booting From SD-Card First Stage Boot Loader Debug Output

As one will note from the FSBL debug output (Figure 41), the boot process never properly completes a boot-up and fails to handoff the CPU to the application. This error was troubleshot extensively to no final solution. The issue in short, stems from Xilinx not currently supporting an FSBL that functions without external volatile memory (a feature that was omitted from the ZPS-Board). Since Xilinx does claim that booting from an SD-card without external memory is a function supported by the Zynq (XC7Z010-2CLG400I) and that the physical interconnect between the Zynq and the SD-card was reasonably verified, this test was not further pursued and is left to the extended testing of the ZPS-Board (see Section 7.2, for more discussion) and end-user designing/testing.

6.3.ADC Functional Testing

6.3.1.ADC Test Software

The test software that was developed using the ADC test breakout board (Section 4.2.3) was used to communicate, configure and test the ADC circuit. Since it was originally written for use on a Zybo Board, the software required some slight changes. Most of the changes were to align the configuration of the Zynq to the Peripherals on the ZPS-Board (as they are different from the Zybo). The destination hardware (Zynq) also had to be changed, since the Zynq used on the ZPS-Board is different than the one used on the Zybo. Once the changes were made, the test software was programmed onto the Zynq using the JTAG interface shown in Figure 38 (pg.56). the command-line user interface was generated via the test software running on PS (one) of the Zynq and communication was performed through the UART interface on the ZPS-Board connector J6 (same connector as the JTAG). The UART was connected to a PC through a FT2232H UART to USB breakout board. Figure 42 demonstrates the interface options generated by the software running on the Zynq, as well as, the different test and configuration options available via the software.

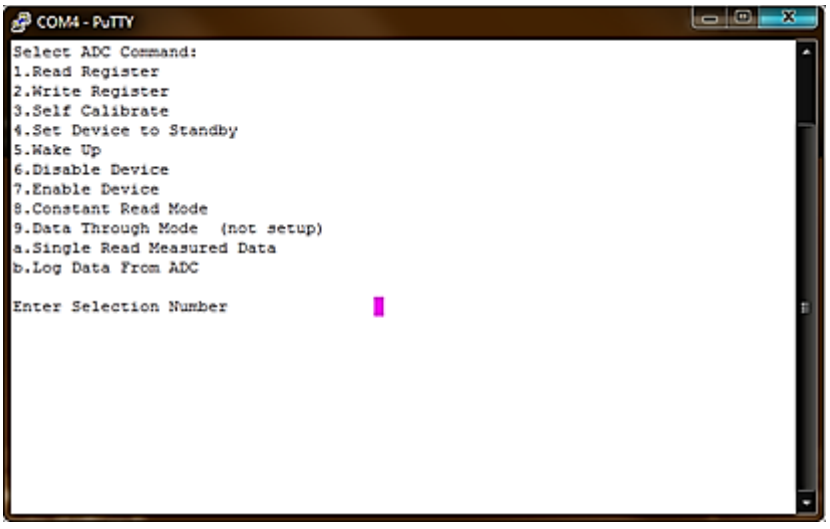

Figure 42: Example of the ADC Test-Software User Interface Command-Line Window

6.3.2.Initial ADC Serial Issues

In order to test the ADC circuit, serial communication (SPI) between the Zynq and the ADS1255 needed to be verified first. Initial attempts to communicate with the ADC failed and it appeared that ADC was not responding to any commands. The ADC circuit was then probed to insure that the ADC was in fact powered up and operating nominally. The results of the test showed that it was. Once ADC circuit was verified, the SPI lines were probed, at which point communication between the Zynq and the ADS1255 began to work. It was discovered, that loading the SCLK with the scope probe made the serial interface work.

The first and simplest assumption as to the cause of the issue is that the clock phase setting for the master was incorrect and that the capacitive loading of the clock line was causing just enough skew to correct it. To clarify this, note that there are four of what are called “modes” for SPI configurations. What this translates to is, an active low or active high clock (polarity) and either a rising edge or falling edge sampling (phase). Figure 43 offers a visual representation of this description.

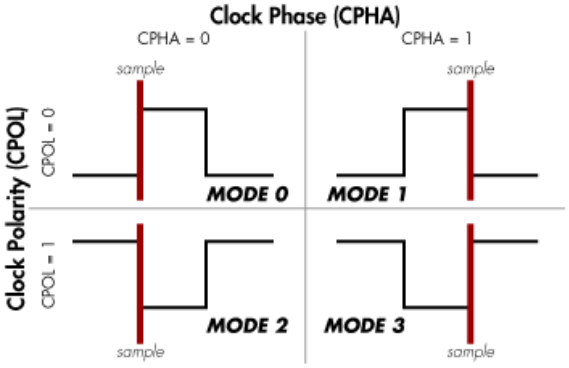

Figure 43: SPI Configuration Mode Example Diagram (Total Phase)

According to the timing diagram of the ADS1255's datasheet (Texas Instraments, SBAS288K), the slave expected a mode one configuration. To rule this out as the cause, a scope measurement of the MOSI and SCLK lines were performed and is shown in Figure 44, where the yellow is SCLK and blue is MOSI.

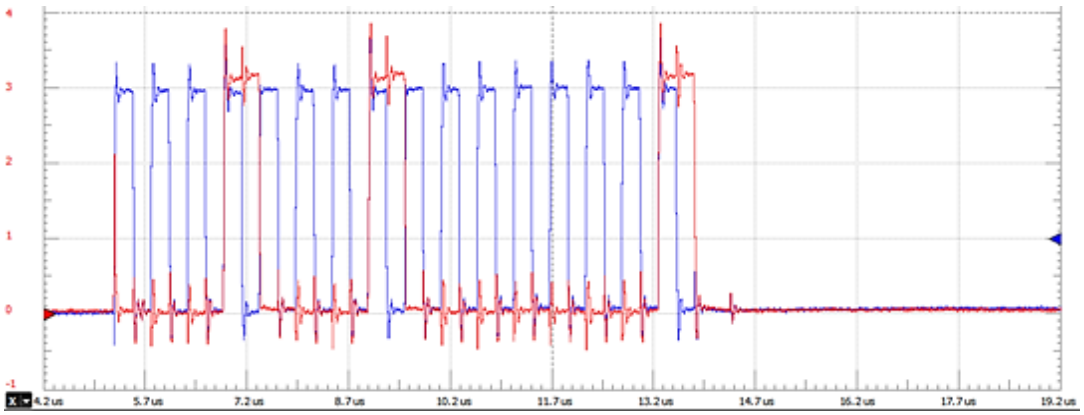

Figure 44: ZPS-Board SPI Line Oscilloscope Measurement of the SCLK and MOSI to Verify Configured to SPI Mode 1 (Blue: SCLK & Pink: MOSI)

As one will note, the results indicated that the SPI mode was configured properly as the SPI clock is idle low and the data is aligned to the falling edge.

The next assumption as to the cause was that the SPI clock line had excessive ringing due to the parasitic inductance and capacitance in the signal path and load. Fortunately, there was a series termination resistor placed on this line for the very purpose of dampening this ringing (see section 4.2.1). The resistor in place, was increased from 100Ω up to 500Ω in steps of 100 to observe if dampening had any effect, unfortunately, no influence was observed. The resistance was then decreased to 10Ω, to insure that the line wasn't over damped and causing excessive skew. Again, the test showed no positive results.

Up to this point, a grounding issue somewhere in the design was ignored, but considered to be possible. Even though probing the line added very large resistance (weak pull-down); it could

theoretically be correcting a floating reference. To investigate this more, the ADC test breakout board was used in conjunction with a Zybo board, to recreate the test environment as much as possible (when used in the past, the ADC test board's serial lines were always being monitored i.e. loaded). The reference test setup exhibited the same behavior. This new data helped to focus the list of possible causes down and shifted the focus onto integration rather than a design/fabrication flaw.

While looking over documentation for the Zynq, it was discovered that the hardware SPI controller has a multi-master mode that "three-states its output signals when the controller is not active" (Xilinx, TRM). This is of course not typical of the SPI standard where the master is always in control of the SCLK, MOSI and CS lines (as opposed to say I2C, which is a standard that supports multi-masters on the same bus). A standard SPI clock driver will commonly use a totem pole output and will hold the line at all times. It appeared that the Zynq's SPI hardware controller was letting go of the clock line and it was floating. To test this theory, a scope in single capture mode was used to measure the idling SCLK line. The probe was held above the SCLK line and then contacted, triggering the scope at 0.5v, as shown in Figure 45. This threshold point is just below the V_{IH} noise margin at $02xV_{DD}$ according to the ADS1255 datasheet (Texas Instraments, SBAS288K).

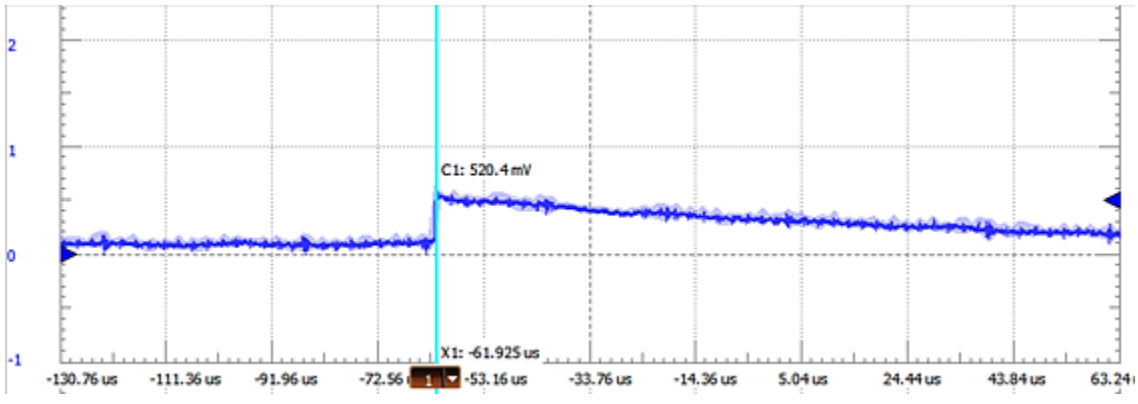

Figure 45: Oscilloscope Transient Measurement of Floating SCLK Line Between ADC and Zynq on the ZPS-Board

This discovery that the Zynq was letting the clock line float appeared to explain everything. If the clock line was left floating after a transmission, a scope probe would weakly pull the line down, as is seen in Figure 45, where the voltage is slowly pulled down. Further, this effect would explain why the communication was failing. Since the line is above the voltage threshold of the ADS1255, this would lead to what the ADS1255 would perceive as an erroneous clock edge, as the Zynq took hold of the clock line to begin a transmission.

The problem then was how to verify this assumption and correct it. The simplest fix would be to attach a pull-down resistor on the line. However, this “Band-Aid” was not reasonable, since there is no place on the PCB to properly solder a pull-down resistor. The Zynq documents were scoured to see if there was a way to disable this multi-master mode by modifying the SPI hardware controller configuration registers. The registers were found to only allow selecting slave or master mode and tri-state setting for all the PS IO lines. Unfortunately, this tri-state disabling option only allows a user to lock an IO to input (not output).

The conclusion was to fix the issue in software. Directly before beginning any communication on the SPI bus (by enabling the CS line), a fake transmission is sent. The command forces the master to take control of the SCLK line. A real command is then initiated by enabling the CS line before the SCLK line has enough time drift high. This solution worked and fixed the communication between the Zynq and the ADS1255.

6.3.3.Storing Measured ADC Data

In order to characterize how the ADS1255 performed on the ZPS-Board, data needed to be recorded and stored for post-processing. This presented a problem since the Zynq itself only offers 256kB of on-chip memory. In order to store even one second of data at the max sample rate of the

ADS1255 (30kSPS), the on-chip memory would have to store 90kB of raw data, this was not reasonable and so other storage options were pursued. Since the ZPS-Board does not have external RAM (which would be ideal for this purpose), the only other option was either to stream the data off the board, or store on an SD card. The first option that was looked into was the simplest and attempted to use the UART external connection to push the data directly to a PC in real time.

In order to meet timing requirements, a data read of the ADS1255 had to be performed and then pushed completely to the PC, before another sample was ready to be acquired (at max sample rate period of 33µsec). Figure 46 offers a visual demonstration of the timing constraints. The max SPI serial clock speed allowed by the ADS1255 is given by the datasheet as 1.92MHz (4/external-oscillator) (Texas Instraments, SBAS288K). This limits the amount of time to ≈12.5µsec (33.33µsec – 20.83), assuming a basic two byte command and three bytes of data read out. There is also overhead time required for ADS1255 to prepare data, which is ≈6.5µsec. This leaves only about 6µsec to execute the transfer of the data to a PC. The recommended max baud rate for the Zynq's UART is 921600bps, which ends up taking ≈26µsec to send 24bits (ignoring any overhead). It was thus determined that UART was not a plausible solution.

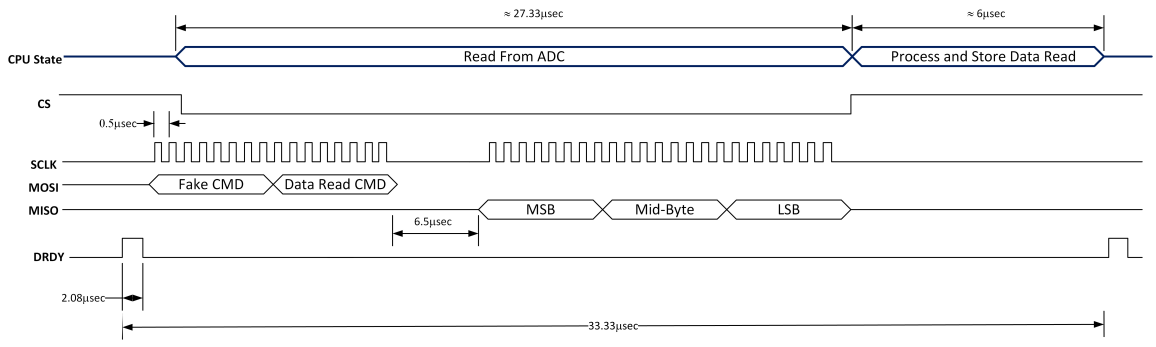

Figure 46: ADS125 Communication Timing Constraints Diagram

The SD memory write speed constraints are a slightly more complicated than the UART. SD memory usually uses 512byte blocks to break up the read and writing of the total memory. This

leads to latency considerations when attempting to run across these boundaries and the memory controller has to move to a new block. SD memory also has a spectrum of different speeds that are based on sequential write speeds ranging from 2MB/sec up to (currently) 90MB/s. The speed classing however, breaks down for random read/write use. Therefore, there is no simple formula to quantify if this method of storing data would be feasible. The only way to be certain was to test and see.

The first attempt to use SD memory, used the built in high level software drivers distributed by Xilinx for the Zynq to interface with the SD hardware controller (xilffs v3.3 library). These drivers are packaged with a simple FAT file system controller and allowed for the data to be written to the SD-card in ASCII form as a text file. This first approach was simple, but failed. The amount of time it took to write was sporadic and it turned out that the driver was not optimized for random access of the SD memory. The SD hardware controller on the Zynq has duel 512byte FIFO buffers which are used to optimize throughput for reading and writing SD memory (Xilinx, TRM). Additionally, the SD hardware controller allows for polled and interrupt writing. The software driver written by Xilinx was buffering the data and then performing a polled write to the SD card. This was causing the processor to be locked up during the actual writing of the 512byte blocks. As a result, these block writes were taking up considerably more time then available between reads of the ADS1255.

In order to circumvent this problem, the high-level file system based driver could not be used and the last-layer hardware driver (sdps_v2.8) was modified to allow for interrupt based writes. According to the documentation for sdps driver, interrupt mode is not currently supported because the only developed supporting drivers are file system based and therefore offered no improvement. The Function “XSdPs_WritePolled” under “xsdps.c” was modified to perform writes without polling. Each write to the SD card was manually buffered in 512bytes before being written to the SD card. This process greatly enhanced the writing speed and dropped the required write time

between reads from the ADC to ≈0.7µsec. This was measured using a software flag inside the test software that was connected to a GPIO signal on the Zynq (brought out to J10 pin-22 on the ZPS-Board) as shown in Figure 47.

Figure 47: ZPS-Board Measurement of GPIO Test Timing Signal – Time Required for SD-Card Data to Be Stored to Buffer

Once the data was being stored at the required rate, the test software was modified to account for these changes. The way the test software now performed was to store the 24-bit data words into a 512byte buffer and then store them onto an SD-card. Once the desired amount of measurements/run-time is completed (as controlled via the command-line interface) the data is read back through the Zynq and converted into an actual measured voltage in ASCII form and dumped to a PC via the UART. The dumped data can then be stored in a log file for post-processing.

6.3.4.ADC Characterizing

The first measurement of the ADC was performed in order characterize the ADS1255's effective number of bits (ENOB), when used on the ZPS-Board. The ENOB is a description of the ADC's dynamic range and includes not only the ADC itself, but also the associated circuitry and environment. For the sake of comparison, the test performed to characterize the ENOB, was

replicated as closely as possible to how it was performed in the ADS1255's datasheet (Texas Instraments, SBAS288K). The test parameters are shown in Table 10.

Table 10: Test Parameters Values for ENOB Testing

TEMPERATURE	25°C
ANALOG VOLTAGE	5v
DIGITAL VOLTAGE	3.3v
REFERENCE VOLTAGE	2.5v
INPUT CLOCK	7.68MHz

$$\text{ENOB} = \frac{\ln(\text{FSR}/\text{RMS Noise})}{\ln(2)}$$

The test was conducted using the test software demonstrated in Figure 42 (pg.62). The input of the ADS1255 was shorted at the input pins (the input filter was within the test circuit). The test was based on the default setting of the ADS1255. The programmable gain amplifier was set to unity and a sample rate of 30kSPS was applied using the configuration registers. Once configured, a self-calibration was performed. Approximately 34k samples were stored using the SD-card method previously described and read back to a PC using a UART interface and stored in a comma separated values (CSV) log file. The data was post-processed using MATLAB R2015b and a plot of the data is shown in Figure 48 (pg.71). The ENOB was calculated using the same method as the ADS1255 datasheet (Texas Instraments, SBAS288K) and the results are shown in Table 11.

Table 11: Measured ENOB vs. Maximum Performance at 30kSPS (Texas Instraments, SBAS288K)

	MEASURED ON ZPS-BOARD	**MAX QUOTED PERFORMANCE**
NOISE RMS	14.602µV	10.341µV
FSR	10v	10v
CALCULATED ENOB	19.385 bits	19.9 bits

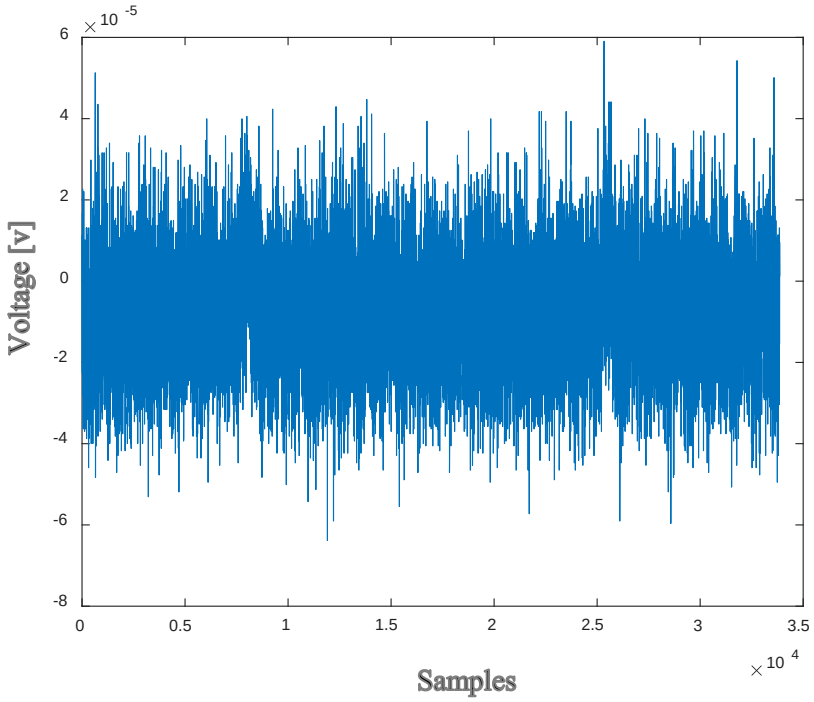

Figure 48: 30kSPS ENOB Characterization – ADC Circuit Input Shorted Test Data Plot

The results of the test are very promising. The test demonstrated that when the ADS1255 was paired with the support circuitry and subject to the noise generated by the other devices on the ZPS-Board, the device only lost 0.516 effective number of bits.

Since the ADS1255 is a ΔΣ ADC, the slower sample rate means more of input referred noise can be filtered out of the output (at the detriment to output update rate). The test was then performed once more, but now at the lowest sample rate of the ADS1255 (2.5SPS). The test used the same parameters as shown in Table 10 and the same test procedures were followed. Once the ADS1255 was configured to rate of 2.5SPS it was self-calibrated and input was again shorted. The test ran for approximately six minutes yielding ~900 samples. The data again was stored and then downloaded via UART and stored on a PC as a CSV file. The data was plotted using MATLAB and is shown in Figure 49 (pg.72).

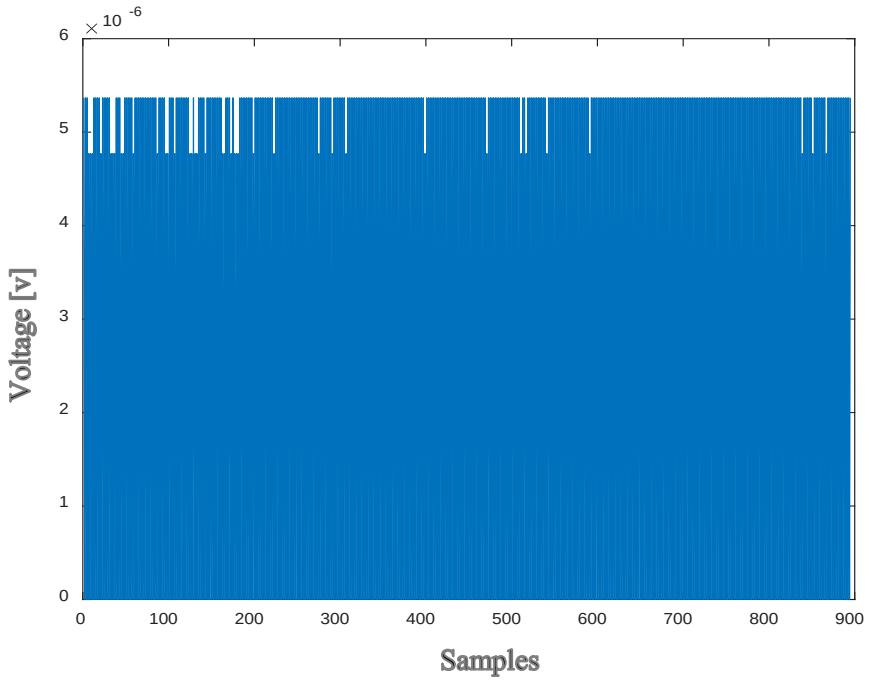

Figure 49: 2.5SPS ENOB Characterization – ADC Circuit Input Shorted Test Data Plot

As before, the ENOB was calculated using the data acquired during the test and the results are given in Table 12. When compared to the max quoted ENOB in the ADS1255 datasheet, the discrepancy is not as good as it was in the 30kSPS test, yielding a loss of ≈3.96 bits (Texas Instraments, SBAS288K). However, this test measures data points extremely close to the minimum resolution of the ADS1255 at ≈0.6µV (FSR/2^{24}) which results in quantization error at the output as ΔΣ-filter's output approaches zero.

Table 12: Measured ENOB vs. Maximum Performance at 2.5SPS (Texas Instraments, SBAS288K)

	MEASURED ON ZPS-BOARD	**MAX QUOTED PERFORMANCE**
NOISE RMS	3.763µV	0.247µV
FSR	10v	10v
CALCULATED ENOB	21.342 bits	25.3bits

One more test of the ADC was executed, in order to observe how well the ADS1255 would perform when measuring dynamic voltages. The test input was a 1kHz sine waveform, with a 2.5v DC offset and a 5v amplitude. The signal was sourced from a Digilent Analog Discovery (ver.1). The ADS1255 was configured to 30kSPS with no buffer and the PGA set to one. The ADS1255 was self-calibrated and the test software previously discussed in Section 6.3.1 was used to perform a continuous read. The data was captured and stored on the SD-card for an arbitrary amount of time. Once the test was concluded the data was dumped to a PC and post-processed using MATLAB R2015b. The resulting FFT (rectangular windowing) performed on the data is shown in Figure 50.

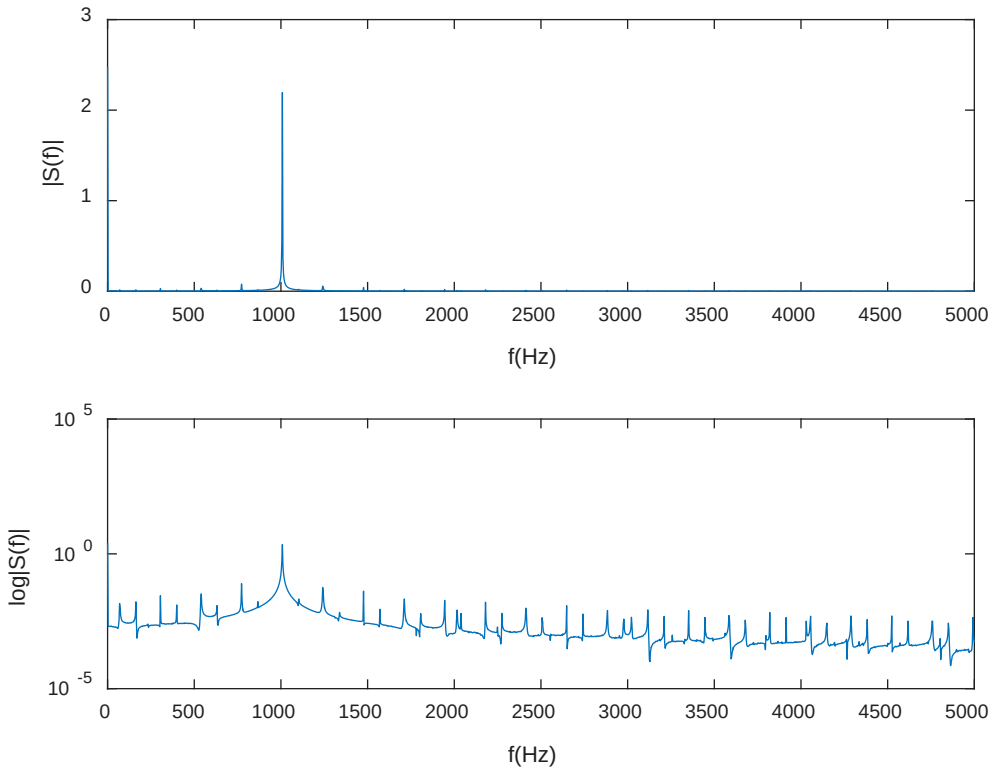

Figure 50: Dynamic Input Testing of the ADS1255 using the Analog Discovery AWG

The results of the test are as expected, with a large portion of the spectral content tightly held around 1kHz. However, as one might note from Figure 50, the data from the FFT seems to imply the

possibility of phase and/or amplitude modulated noise. This is slightly concerning since it is not clear if this is due the non-idealities of the source or the ADC itself. In order to help shed light on this, the test was performed again in the same way, except this time the source device was changed. The input of the ADC was sourced with an Agilent 33220A function generator and the input was measured using the ZPS-Board test software and processed using MATLAB. The resulting FFT is shown in Figure 51.

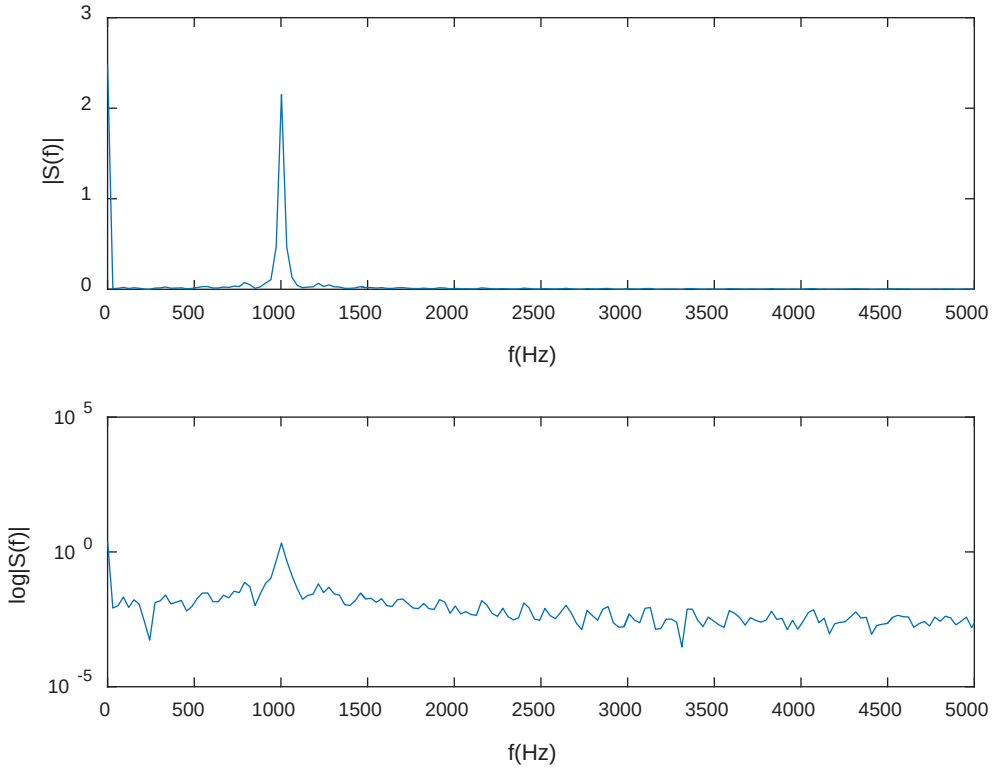

Figure 51: Dynamic Input Testing of the ADC Using Agilent 33220A Function Generator

The results of the second test were beneficial in helping rule out the ADC as the cause of the observed noise in the original test. As one will note from Figure 51, when compared to the FFT from the first test (Figure 50), the noise characteristics have dramatically changed. The noise characteristics of the first test appear to be periodic in nature with the existence of repeated spikes

slowly decreasing as their frequency moves away from the test signal at 1kHz. The second test signal has very different type of noise, exhibiting a much wider noise skirt around the test frequency (when compared to the first test). Even more telling, is that the periodic spikes do not appear in the second test data. The conclusion is that the noise observed in each data set is in fact due to the source device used in the test and not created by the ADC circuit. These tests demonstrate that the ADC circuit on the ZPS-Board is not only working as expected, but performing well.

6.4.Camera link Sub-Circuit Functional Testing

The Camera Link's main circuitry is a receiver SERDES (DS90CR288A), that takes in four data and one clock LVDS signals and deserializes (7:1) them to twenty-eight single ended CMOS parallel data lines and one clock and delivers them directly to the Zynq. The serial input data comes into the board through an impedance matched 26-pin SDR connector at 2.38Gbps (at max frequency of 85MHz). Due these high speed constraints and a closed system, simply connecting basic low-speed benchtop inputs and testing what the Zynq observed was not acceptable. Fortunately, testing Camera Link Receivers (commonly called "Frame Grabbers") is common enough that a small market exists for Cameral Link test equipment. After searching a few Camera Link Simulators (essentially just Camera Link programmable transmitters) the Vivid Engineering's CLS-211 was selected. The simulator was chosen based on meeting the minimum requirements for testing the ZPS-Board and it being the lowest priced, at $898.00.

The CLS-211 is a RS-232 command-line programmable device that can be configured to transmit simulation data based on the Camera Link standard. In order to use it to functionally test the ZPS-Board's Camera Link interface, a test setup shown in Figure 52 and Figure 53 was constructed. The CLS-211 was connected to the input of the Camera Link interface on the ZPS board via an MDR to SDR cable. A PC was connected to the RS-232 control interface of the simulator.

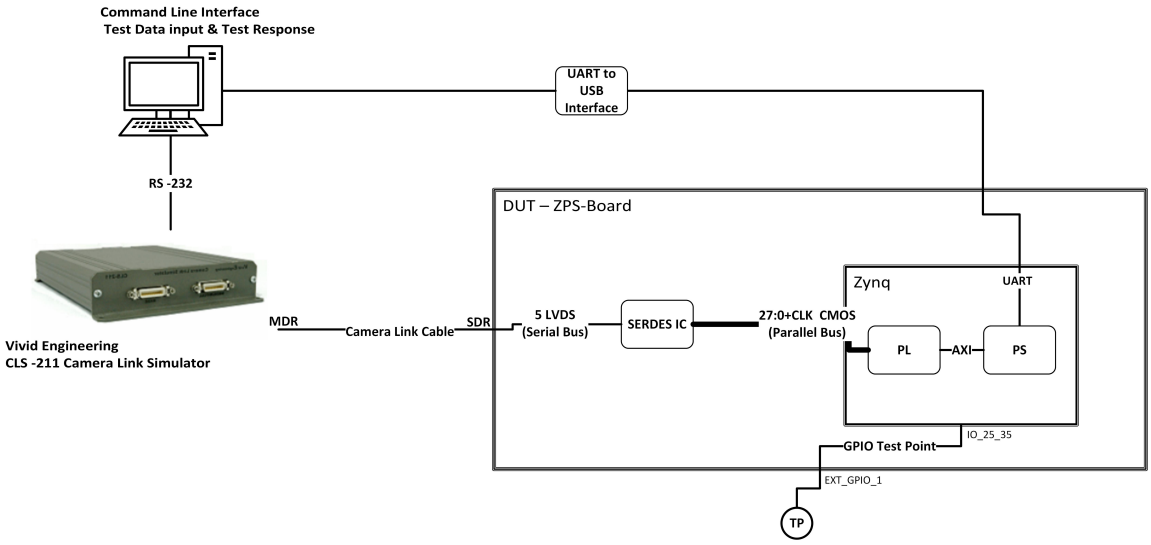

Figure 52: Drawing of System Configuration for Performing Testing of ZPS-Board's Camera Link Circuit

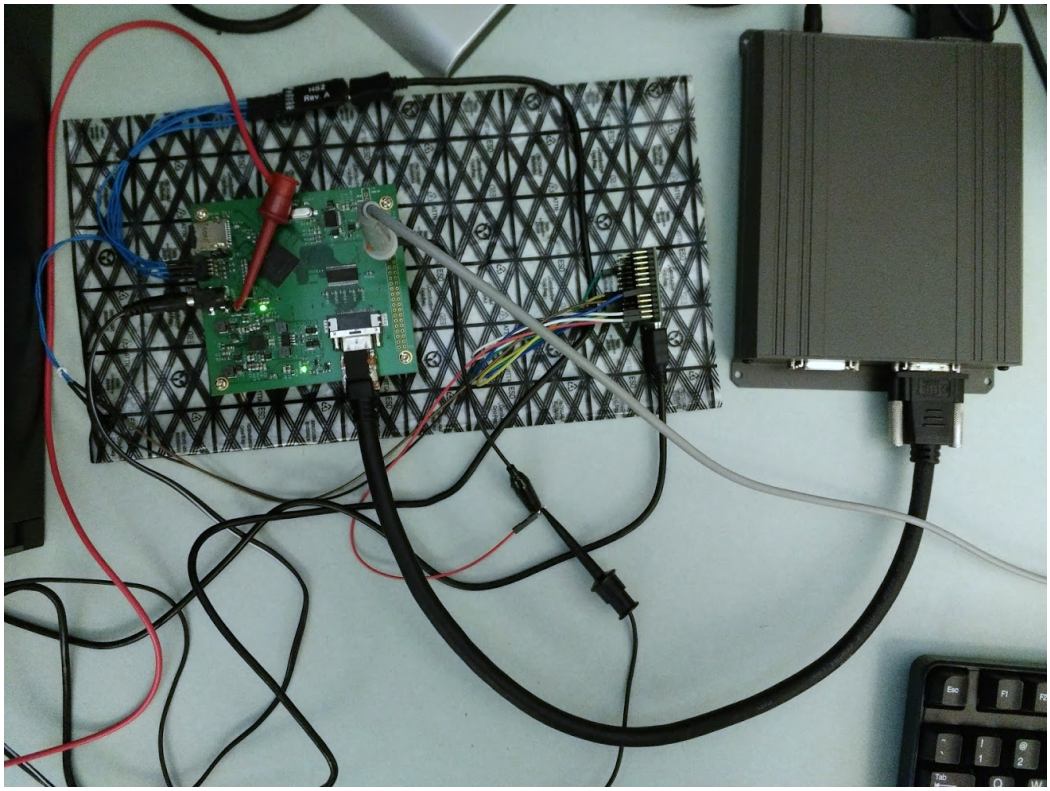

Figure 53: Picture of System Configuration for Performing Testing of ZPS-Board's Camera Link Circuit

6.4.1.SERDES Liveness Test

The first test performed, was a liveness test of the DS90CR288A IC. The ZPS-Board was powered nominally and the Zynq's PL was configured to use the ports connecting it to the DS90CR288A. A simple Verilog program was written to drive the enable pin of the DS90CR288A and the clock signal on pin IO_L7N_T1_AD2N_35 was passed through to pin IO_25_35 (EXT_GPIO_1 – SelectIO connected to the 52-pin stack-through connector). The CLS-211 was programmed to drive the DS90CR288A with a 20MHz clock signal (CLS-211 command: FREQUENCY 0x14 (Vivid Engineering)) and the EXT_GPIO_1 (labeled "TP" in Figure 52) was measured using a Keysight 100MHz 2 GSa/s oscilloscope (model: MSOX2012a). The resulting measured waveform is shown in Figure 54.

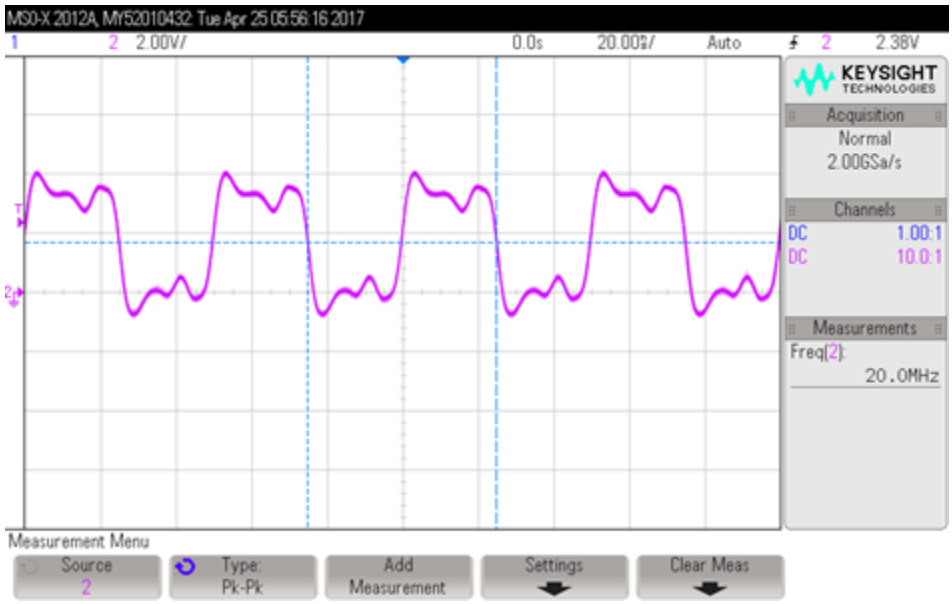

Figure 54: Oscilloscope Measurement of the 20MHz Simulator Sourced Clock Signal Passed Through to Zynq for Liveness Testing

Though the waveform seems highly corrupted in Figure 54, this is in fact, not of concern, since this path is not necessarily rated for a signal with this high of a speed. What is of importance in the

measured waveform, is that it is 20MHz, which proves not only that the DS90CR288A is in fact alive, but also that its PLL is locking and that one of the paths from the CLS-211 simulator through the DS90CR288A and into the Zynq is verified. However, to properly complete this test and verify the path and PLL locking at max frequency, an 85MHz clock frequency would need to be supplied and verified. This was achieved by commanding the CLS-211 to change its output clock to 85MHz (CLS-211 command: FREQUENCY 0x55 (Vivid Engineering)) and the TP was again measured using the oscilloscope. The measured waveform is shown in Figure 55.

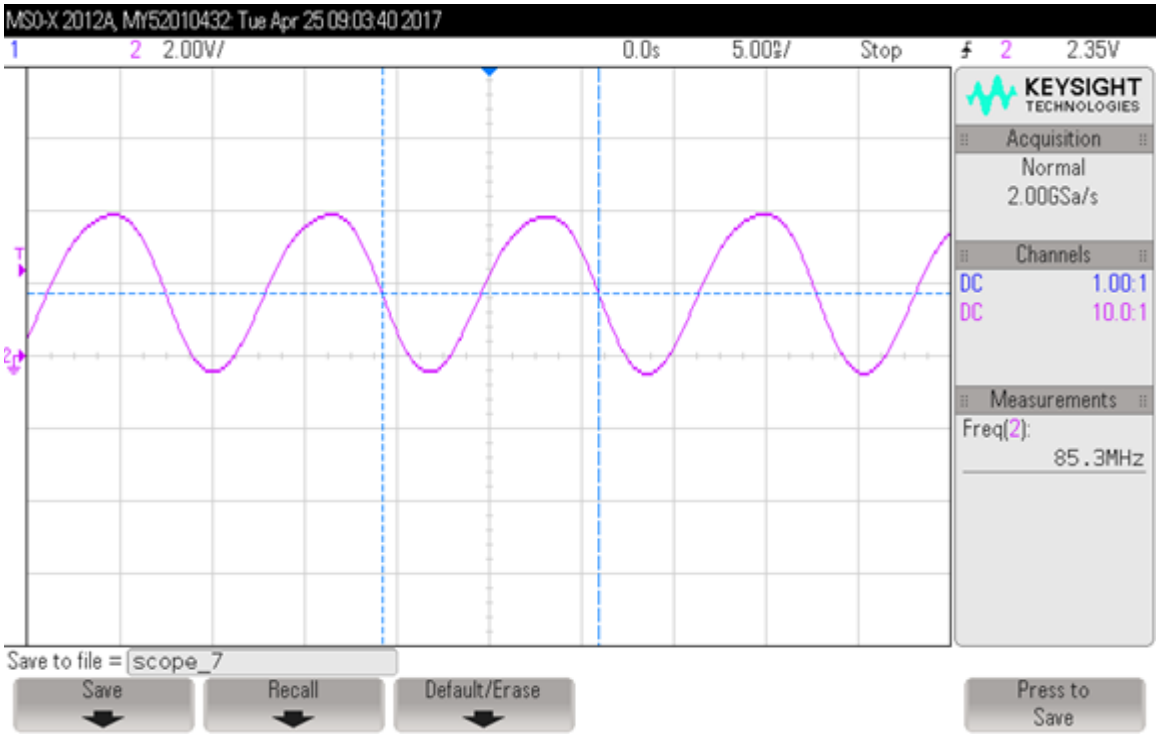

Figure 55: Oscilloscope Measurement of the 85MHz Simulator Sourced Clock Signal Passed Through to Zynq for Liveness Testing

The signal integrity observed in Figure 55 is not ideal, however, as before, this path is not built for an 85MHz signal and so corruption is to be expected. That said, the expected 85MHz signal was successfully transmitted from simulator through the DS90CR288A and received by the Zynq. The basic elements of the Camera Link circuit on the ZPS-Board were now verified to be functioning as expected.

6.4.2.Camera Link Individual Signal Testing

Now that the DS90CR288A was shown to be working nominally, it was left to verify that all input serial data was reaching the Zynq as expected. The CLS-211 doesn't allow for sending arbitrary combinations of data into the ZPS-Board, but sends fixed data sets based on the Camera Link standard. Based on this, in order to send verifiable information to the Zynq, the Camera Link standard had to be leveraged.

The Camera Link data layer is similar to most common image transmitter to receiver standards (National Semiconductor, PULNiX America, Inc and Basler). The base version allows for up to 24-bit RGB at an 85MHz pixel clock. There are two control signals that are used to indicate frame boundaries to the receiver device, the Line Valid (LVAL) and Frame Valid (FVAL) and one valid data signal (DVAL). At each strobe of the clock signal, a 24-bit (RGB) pixel is transmitted while the state of the LVAL and FVAL define where the pixel is to be drawn in the active window. Figure 56 demonstrates how each transmitted frame is communicated to the receiver.

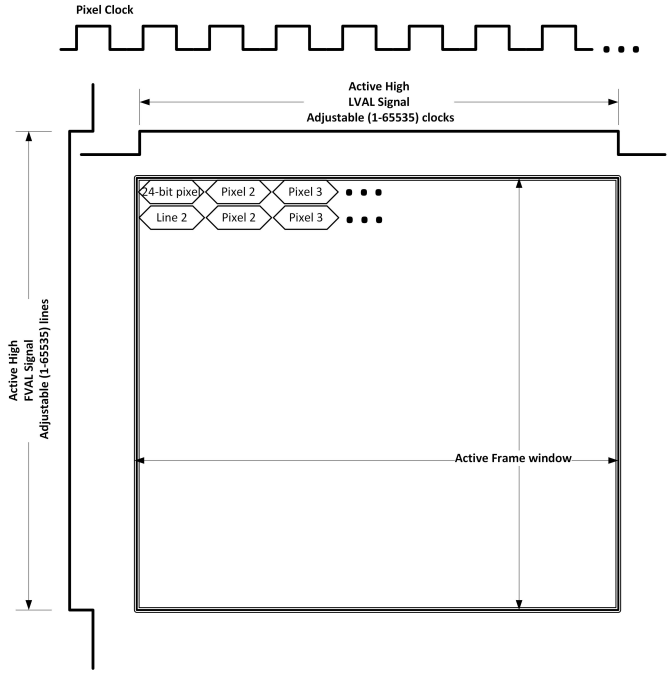

Figure 56: Example of Camera Link Active Window Drawing and Signal Definitions

The CLS-211 allows the user to control the low and high clock times for LVAL signal, as well as, the amount of lines the FVAL is low and high for. Additionally, pixel data can be controlled by changing each port individually (In Camera Link standard port A, B and C is equivalent to Red, Green and Blue values, respectively). Four options are available for setting each port: fixed, horizontal wedge, vertical wedge and diagonal wedge. Each option, creates a pattern across the active window (aside from fixed), and does so by changing the color value at a set interval as the pixel position moves across the frame.

In order to verify proper transmission of data for the individual bits, a series of tests were performed. New test software was written in order to perform these tests. The Camera Link parallel data from the SelectIO pins were monitored and the observations were communicated to the Zynq's PS. The PS system was used as the master to the programmed hardware on the PL by setting up two 32-bit AXI4 busses (one read and one write). A command-line user interface was created (built off the software written for the ADC testing, see Section 6.3.1 for more information) to run on the PS and allow for control of the test software/hardware.

The first test conducted was to verify the FVAL and LVAL signals. Using the same test configuration as shown in Figure 52, the SelectIO lines were connected to the ports that correlate to bits 25 and 24 respectively (see Table 13 pg.82 for Camera Link standard bit assignment) and were monitored using the PL. The PL was programmed to respond to commands controlled by the command-line interface shown in Figure 57.

Figure 57: Example of Camera Link Test-Software Command-line User Interface

When the PL is commanded to monitor FVAL or LVAL it counts the number of pixel clock cycles it observes and outputs it to the PS. The PS then monitors this data and reports the largest value it observes to the user via the command-line interface. The test software was run in conjunction with the CLS-211, which was programmed to output different amounts of clock cycles for the LVAL and FVAL low and high times. The observed values by the Zynq's PL matched different test cases as expected.

With the path validation of the LVAL and FVAL signals, the serial data lines "xclk" and "X3" (Figure 58) were now verified to a reasonable amount of certainty. However, in order to fully prove out the Camera Link interface on the ZPS-Board, the pixel data needed be verified. The PL was expanded to monitor Camera Link ports A, B and C as defined by Table 13 (pg.82). The data ports are spread across the serial and parallel line as shown in Figure 58 and Table 13 (pg.82). The ports were constructed in the PL by concatenating the bits together to extract the red, green and blue data information. The PL, as before, is controlled via the PS (and by extension, user controlled via command-line interface) to report back the red green and blue 8-bit pixel data. The test was conducted by commanding the CLS-211, to output port A, B and C to a fixed pattern selection (CLS-211 command: A_PATSEL 0x0, B_PATSEL 0x0, C_PATSEL 0x0) This constrains the pixel color within the active window to a constant value. Worst case data speed was used by setting the max pixel clock frequency to 85MHz (CLS-211 command: FREQUENCY 0x55). Different pixel color data was then randomly selected to be inputted into the ZPS-Board from the CLS-211 (CLS-211 command: A_FIXED, B_FIXED, C_FIXED) and the PL reported the observed colors to the PS which were output to the user command-line interface. Different values for each port were selected to insure a given port was uniquely being varied and the results met the expected value at all times. This test not only exhaustively verified the Camera Link signal path by isolating all paths, but also, due to the pixel ports being distributed asymmetrically across the serial and parallel paths, the test demonstrated strong evidence that the crosstalk and signal skew between the signals on the

board was reasonably low, as the previously performed pre-fabrication testing had shown (section 4.3.3) (Vivid Engineering).

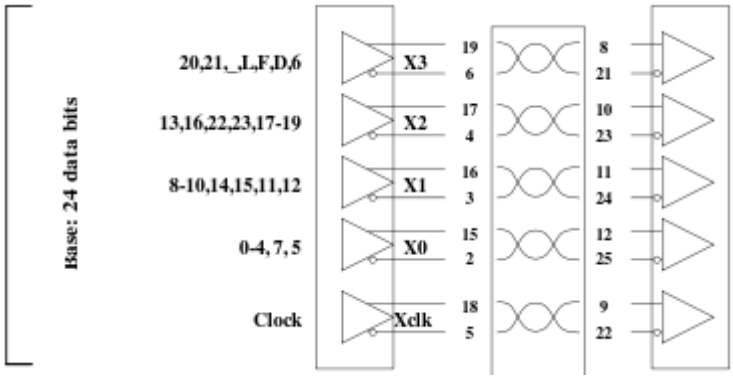

Figure 58: Camera Link Base Configuration Serial Signal Assignments (Creative Commons)

Table 13: Camera Link Base Configuration Parallel (28-bit) Signal Assignments

Port A	Bit	Port B	Bit	Port C	Bit	Control	Bit
A0	0	**BO**	7	**C0**	15	**Strobe**	clk
A1	1	**B1**	8	**C1**	18	**LVAL**	24
A2	2	**B2**	9	**C2**	19	**FVAL**	25
A3	3	**B3**	12	**C3**	20	**DVAL**	26
A4	4	**B4**	13	**C4**	21	**Spare**	23
A5	6	**B5**	14	**C5**	22		
A6	27	**B6**	10	**C6**	16		
A7	5	**B7**	11	**C7**	17		

6.5.Characterizing the Performance of the Power Circuit

Load testing was performed on the power circuit in order to insure that it would function as expected when fully loaded over its nominal load specifications. These specifications and maximum load values are discussed in section 3.4.1, please refer to this section for more discussion and in order to compare with the results of this testing. In order to properly characterize the performance of the power circuit over its potential full range, the circuit had to be fully isolated from all other load elements on the ZPS-Board. The simplest way to achieve this isolation with certainty, was to construct a ZPS-Board with all other devices not populated (aside from power circuit). In order to reduce cost by essentially wasting an entire board for this test, the board used was one the manufacturer had used to perform electrical testing and was therefore "damaged" by pad exposure. The test board was populated as it was before when constructing the aforementioned prototype ZPS-Board in Chapter 5. and is shown in Figure 59.

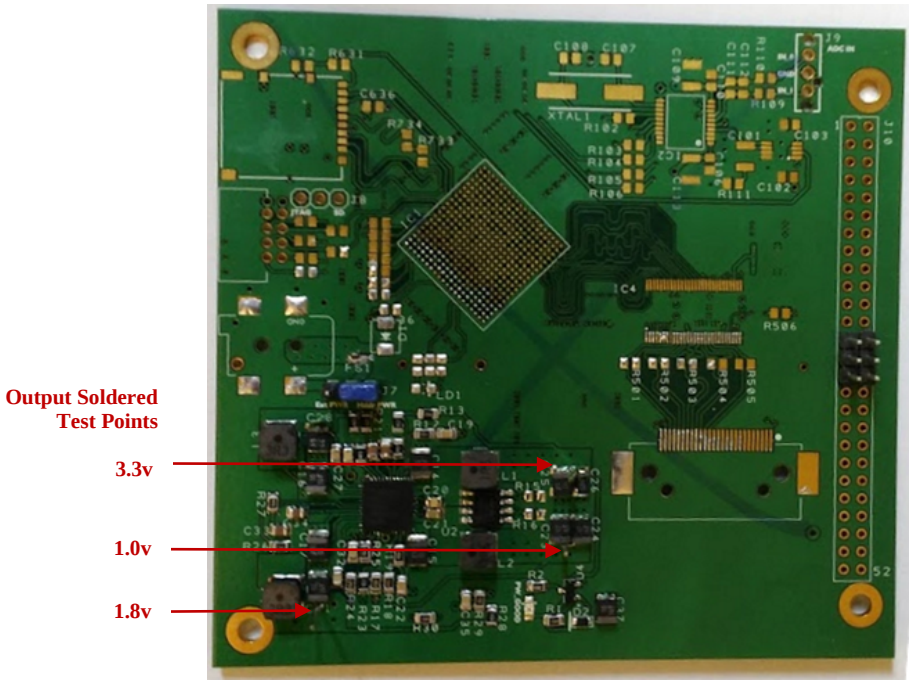

Figure 59: Populated Power Circuit Test Board Used for Isolated Testing

The output capacitors for each supply rail had a test point contact, soldered to their respective edge (Figure 59). The circuit was tested by powering the ADP5052 regulator through the input of the ZPS-Board using a benchtop power supply (a Rigol DP832) at the nominal 5.0v. The circuit was confirmed to be powered up when all rails had reached their respective voltages and the "power good" signal of the ADP5052 had illuminated its associated indicator LED. Each supply rail was then tested independently while other rails were left unloaded. An electronic load (a BK Precision 8540**)** was attached to the supply under test, as well as an oscilloscope (GW Instek GDS-1102B) and digital multimeter (Rigik DM3058E**)**. The test performed swept the electronic load at steps of 100mA, from zero to the maximum rated load for a given rail (note Table 4 on pg.18). The input current was measured by monitoring the benchtop supply current. The output DC voltage was measured using the digital multimeter and the output ripple voltage was measured using the oscilloscope. Once the test was concluded, the data was processed using Microsoft Excel. The percent output voltage ripple was calculated using the peak-to-peak output ripple, measured at a given supply's rated max load and divided by the rails nominal voltage. The load regulation was calculated using the equation $(V_{min\text{-}load} - V_{max\text{-}load})/V_{max\text{-}load}$**.** A summary of the test results are shown in Table 14.

Table 14: Power Circuit Specification Tests Results

SUPPLY VOLTAGE	PERCENT OUTPUT VOLTAGE RIPPLE	LOAD REGULATION
3.3V	5.3%	-3.02%
1.8V	13.46%	-1.15%
1.0V	30.8%	-4.25%

As one will note from the calculated results in Table 14, compared to the required specification of the ZPS-Board given in Table 4 (pg.18), all fall within specification except the output voltage ripple of the 1.8v rail and the 1.0v supply rail. Though there results are not ideal they were found to be

not unexpected. Once the discrepancy was discovered a reevaluation of the sizing of the output capacitors were examined. It was then discovered that a mistake had been made in selecting the minimum ESR requirements of the two supplies in question by approximately a factor of a hundred (equivalent ESR of 500mΩ were used instead of 5mΩ). This mistake is easily corrected by replacing the output capacitors used with ceramic equivalents (the current are tantalum), effectively reducing the ESR to meet specification requirements. Note, the reason these results did not show up in the previous ZPS-Board prototype testing was due to the equivalent bulk capacitor loading of the lines (required for the Zynq) more than compensated for the error.

The Efficiency of the power circuit for each supply rail was also calculated and plotted over its respective load range, as shown in Figure 60. For simplicity, the input power for each rail was approximated by subtracting four-fifths the no-load input current, since each supply on the regulator was populated and enabled during testing (including the optional 1.5v, and 1.8v-LDO). From the plot, one will note that the efficiency looks reasonably well at approximate seventy-five percent when above a load of ~200mA. However, as to be expected, efficiency is not as ideal below a load of ~200mA due to minimal power consumed by the power circuit, i.e. the quiescent current of the ADP5052 and element parasitics.

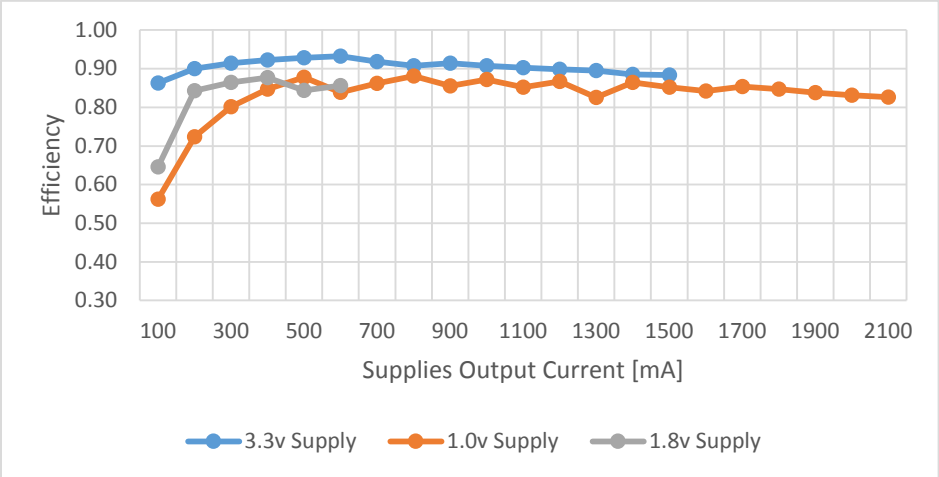

Figure 60: Power Circuit Characterization Efficiency vs. Supply Output Current Plot

7. FUTURE WORK

7.1.PCB Layout Fixes/Updates

After the initial design and fabrication of the ZPS-Board there were a few discovered errors and lessons learned that should be taken into consideration when updating the design for future work.

The simplest fix that should be performed is to flip the external barrel jack (J5) layout footprint 180 degrees. When designing the ZPS-Board a mistake was made in the J5 connector, which resulted in it being placed backwards. Due to the symmetry of the component it was still capable of being mounted, however, it cannot deliver the positive voltage to the board and currently only allows for the ground to make contact.

As discovered during testing with the ADS1255 on the ZPS-Board (Section 6.3.2), the Zynq requires a pull-down resistor on the serial clock line when interfacing to the ADS1255 via SPI. Once discovered, this issue was corrected in software by sending a fake command directly before a real command. This fix insured the clock line is pulled low before enabling communication by asserting the CS line. This method of correction is not ideal and it would be best if a pull-down resistor were placed on the serial clock line of the SPI bus between the Zynq and the ADS1255.

7.2.SD Card Booting

Since the ZPS-Board does not currently contain DDR memory for the Zynq's PS, the standard First Stage Boot Loader (FSBL) distributed by Xilinx SDK (2016.2) will not function. Whenever the Zynq is first powered up, (or reset) the BootROM is executed and the boot configuration pins are scanned to determine the boot device/medium. If SD is selected, it will scan the SD_0 peripheral for an attached device and attempt to read it. If an FSBL partition is found, it will execute it. As it

is currently written, the FSBL performs a series of system readiness checks and moves the application and configuration bit file (also located on the SD-card) into volatile memory in preparation for execution. Unfortunately, there is no external memory to move the contents to and so the FSBL fails. Xilinx AR#56044 states that it is still possible to boot up without external memory and offers code and configuration changes that need to be made in order to achieve this (Xilinx, AR# 56044). However, these changes are for older versions of Xilinx's SDK (and therefore, older FSBL versions) and do not directly port to the current version of 2016.2. In attempting to apply these suggested modifications to the current FSBL, it was discovered that there is not much current support from Xilinx on the topic. The only approach that was found was using the on chip memory (OCM) to store the boot application. This process, reallocates the 512kB L2-cache for the purpose of storing and executing the PS application. This approach requires that the linker script be edited to move the data on the SD-card to this location and requires modifying the standard FSBL code to ignore the fact that there is no DDR attached to the system. Once the files are moved to the OCM, the FSBL needs to be configured to perform a handoff of the PS to the application's new address.

7.3.Environmental Testing

As it was intended, the ZPS-Board now complete, should undergo a series of environmental testing that verifies its readiness for space environments. All components on the ZPS-Board were selected in order to comply with temperature specifications outlined in Section 3.2.2. However, there is one component that did not meet specifications; the DS90CR288A is the only 7:1 Camera Link compliant SERDES on the market and unfortunately does not offer a version that is fully rated for the free air temperature range of -30° to 20°C. The DS90CR288A is recommended to operate in the range of -10° to 70°C (Texas Instraments, SNLS056G). This recommendation meets the upper

bound but not the bottom end. However, this does not mean the device cannot operate reasonably in this range, and in fact, being at the bottom end (cold) is less concerning. Nevertheless, this is not a guaranteed operating environment for the device and should be tested and verified that, for example, a heating element is not required to insure proper device functionality.

In regards to radiation testing of the ZPS-Board, it should be taken into consideration that software and hardware redundancies are inherently available and should be exploited when testing. An example of these built in redundancies is the use of redundant boot images on the SD-card. The data stored on the flash memory is susceptible to SEU which can corrupt the boot image. However, by storing redundant versions of the images and then verifying them using the Zynq, the ZPS-Board can actively detect and counteract a corruption. Another example, is the ability of the Zynq to self-monitor and scrub the FPGA fabric. Since the PS sits as master to the PL it has the ability to constantly monitor and actively clean the PL in the event of a transistor latch up, in real time.

7.4.Adding DDR to the ZPS-Board

The ZPS-Board currently does not have external volatile memory for the Zynq. However, adding this to later versions of the design would be useful in taking full advantage of the features offered by the Zynq. With this in mind, the design of the first version of the ZPS-Board already includes some of the additional required support circuitry and layout considerations. For example, the required 1.5v supply is already built into the layout of the power circuit. Additionally, there is amply room to run the interface traces from the Zynq to the external memory on the 3rd layer of the PCB, thereby removing the need to completely redesign the stack-up of the ZPS-Board. The one key concern that will need to be evaluated in adding DDR to the ZPS-Board, is space. The current amount of space available for adding additional components, especially one that will require a large amount for vias to run traces, is minimal at best and may require the support of the Tyvak form

factor compliance to be removed. If the Tyvak stack-through connectors are removed, there will be enough room to add DDR to the bottom layer without too much re-work of the ZPS-Board layout.

7.5.Error Rate Characterization for Camera Link Interface

Though the Camera Link interface was functionally tested, its performance characteristics were not. It is advised that in performing future work on the ZPS-Board, this be taken into consideration. A test should be performed to measure the bit error rate (BER) of the high-speed interface in order to properly characterize its performance. One approach to performing this test would be to perform it on the Zynq's PL. A test written in Verilog and/or VHDL could monitor the input with a known stream of data from a simulated input and the PL would count the number of errors (i.e. the BER). This will require an explicit correlation of input data stream with respect to data observed. Therefore, if the input test device strictly adheres to the Camera Link standard and one cannot openly define the input data on each signal, the standard will have to be leveraged to perform the test. Additionally, to properly perform this test the highest level of interference needs to be simulated and therefore an uncorrelated (between individual signals) stream of data should be used.

7.6.Adding the Zynq's Internal ADC to the ZPS-Board

One simple way to increase the functionality of the ZPS-Board would be to use the Zynq's internal ADC. The Zynq contains an internal 12-bit 1MSPS ADC, with up to seventeen multiplexed differential inputs. This internal ADC was not used as the primary ADC on the ZPS-Board, since it was decided that a more advanced ADC would make the board more useful to a wider spectrum of applications. However, by adding this ADC to the ZPS-Board, one could extend the amount of analog inputs into the board, ultimately enhancing its functionality.

In order to add the second ADC option to the ZPS board, a relatively large amount of reconfiguring of the Zynq SoC will be required. As one should note from Table 7 (pg.46), the ADC reference pins are all currently tied off, since the ADC is not currently being used. These Pins will all have to be broken out from the Zynq SoC. It is advised that layer three be used for this purpose since it is currently the most open plane available on the ZPS-Board's PCB. Careful considerations should be made when also breaking out the inputs to the ADC on the Zynq, as these lines will be highly susceptible to the noise generated through the reference planes. Lastly, an external reference voltage from the power circuit is already available to be used for the Zynq's ADC and will need to be tested for nominal performance (as this was not done in the original design and testing of the ZPS-Board and therefore has no performance guarantees). The reference is supplied by the ADP5052 power IC and is a nominal 1.8v. The supplied voltage is listed in datasheet as having a low noise performance of $92\mu V_{RMS}$ ((Analog Devices). The line that will carry this reference voltage to the Zynq is also extremely susceptible to noise and should be carefully laid out with this in mind.

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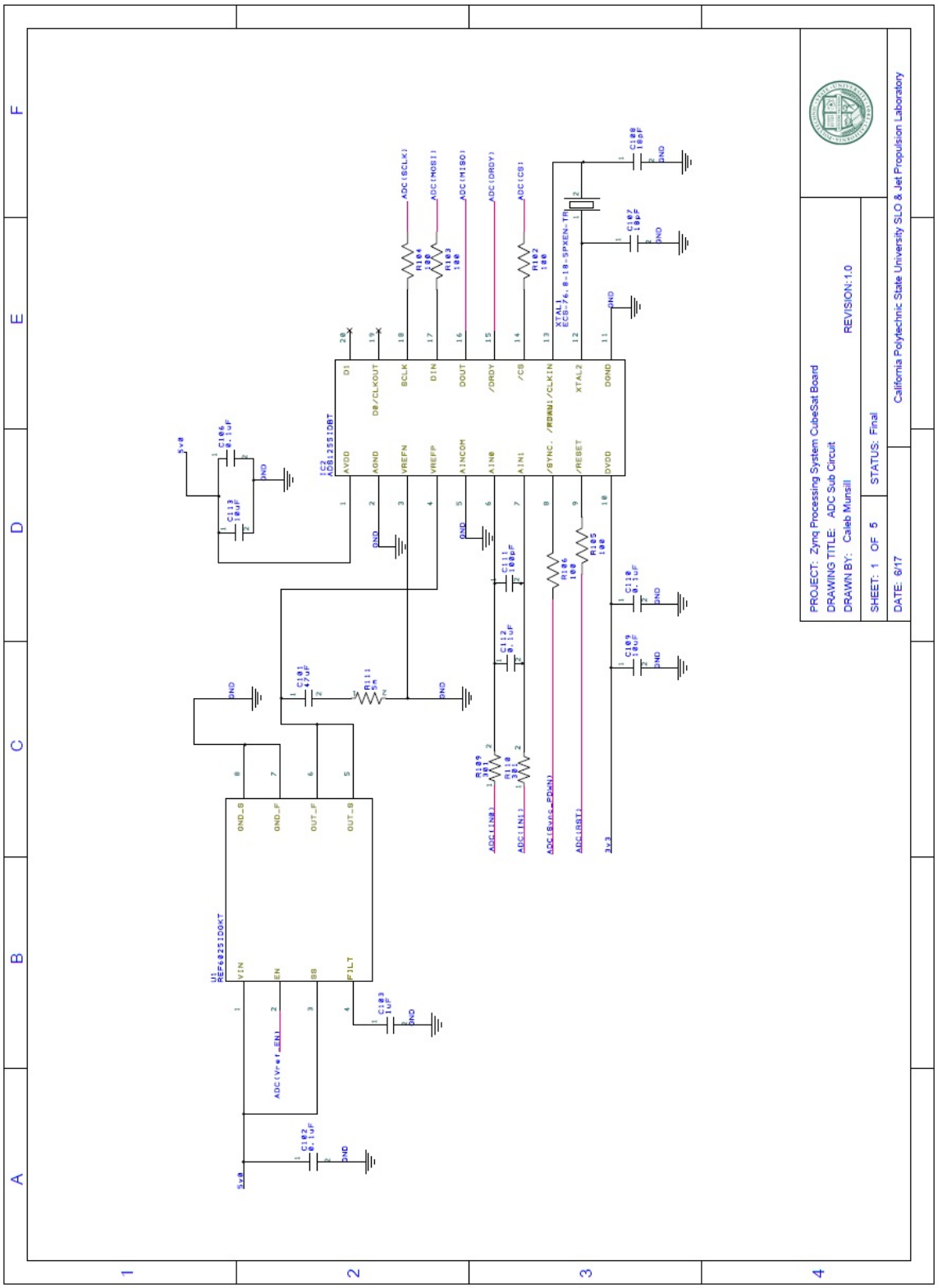
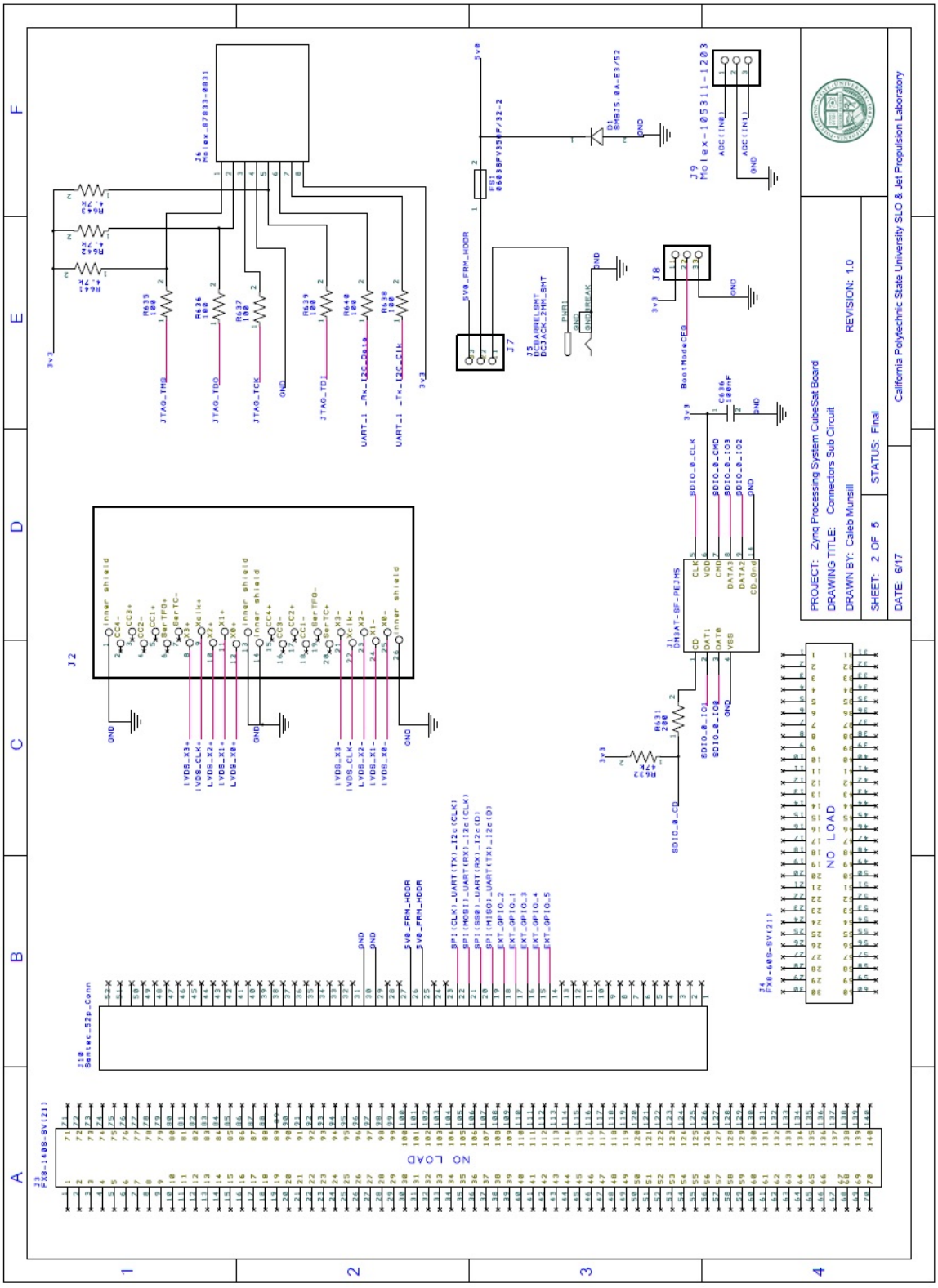
APPENDIX I – Circuit Schematics

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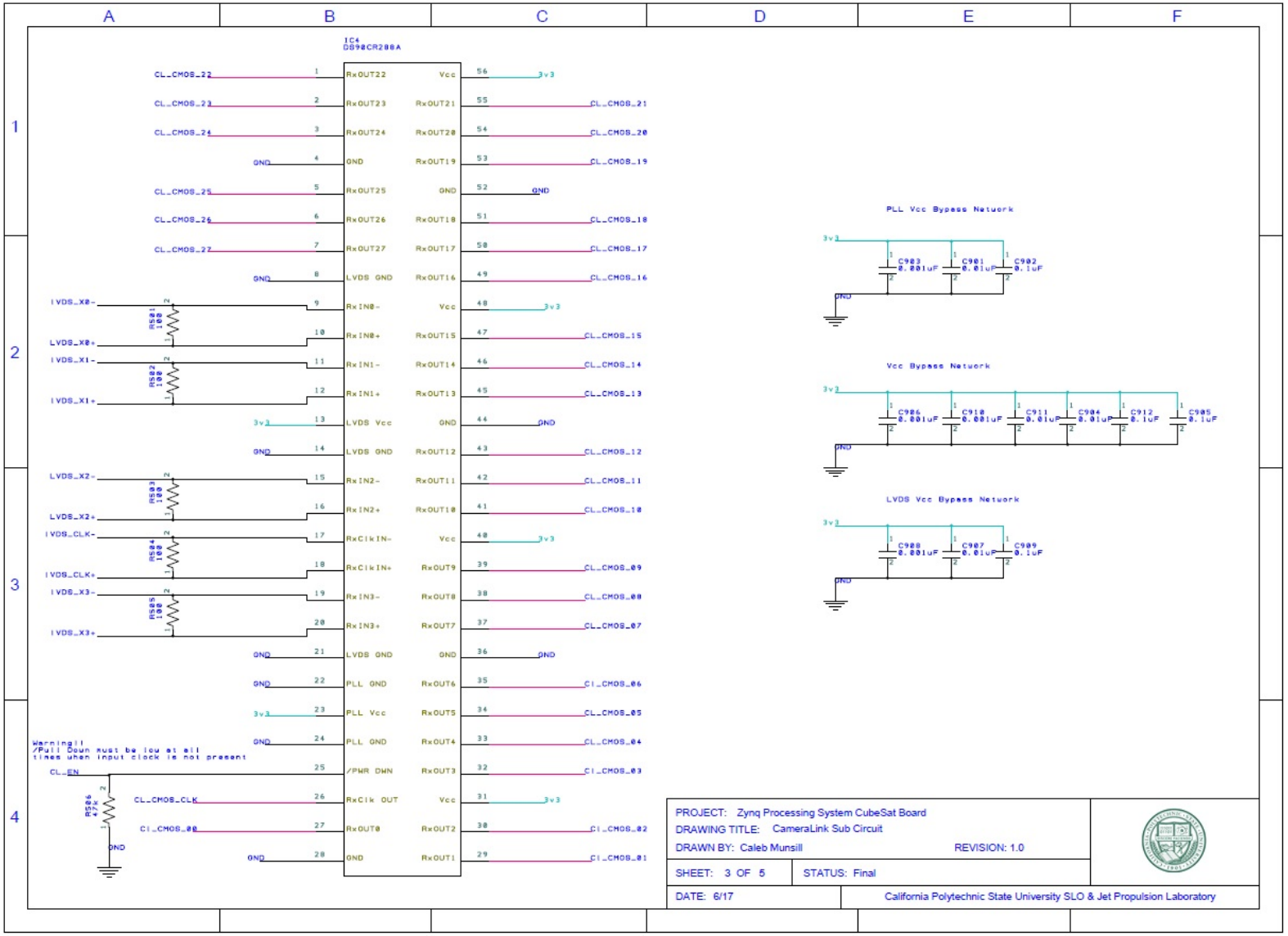
DRAWING TITLE: Connectors Sub Circuit
DRAWN BY: Caleb Mursill
REVISION: 1.0
SHEET: 2 OF 5
STATUS: Final
DATE: 6/17
California Polytechnic State University SLO & Jet Propulsion Laboratory
NO LOAD
NO LOAD


IC4
DS90CR288A
RxOUT22
RxOUT23
RxOUT24
GND
RxOUT25
RxOUT26
RxOUT27
LVDS GND
RxIN0-
RxIN0+
RxIN1-
RxIN1+
LVDS Vcc
LVDS GND
RxIN2-
RxIN2+
RxClkIN-
RxClkIN+
RxIN3-
RxIN3+
LVDS GND
PLL GND
PLL Vcc
PLL GND
/PWR DWN
RxClk OUT
RxOUT0
GND
Vcc
RxOUT21
RxOUT20
RxOUT19
GND
RxOUT18
RxOUT17
RxOUT16
Vcc
RxOUT15
RxOUT14
RxOUT13
GND
RxOUT12
RxOUT11
RxOUT10
Vcc
RxOUT9
RxOUT8
RxOUT7
GND
RxOUT6
RxOUT5
RxOUT4
RxOUT3
Vcc
RxOUT2
RxOUT1
CL_CMOS_22
CL_CMOS_23
CL_CMOS_24
CL_CMOS_25
CL_CMOS_26
CL_CMOS_27
LVDS_X0-
LVDS_X0+
LVDS_X1-
LVDS_X1+
LVDS_X2-
LVDS_X2+
LVDS_CLK-
LVDS_CLK+
LVDS_X3-
LVDS_X3+
Warning!!
/Pwr Down must be low at all
times when input clock is not present
CL_EN
CL_CMOS_CLK
CL_CMOS_00
CL_CMOS_21
CL_CMOS_20
CL_CMOS_19
CL_CMOS_18
CL_CMOS_17
CL_CMOS_16
CL_CMOS_15
CL_CMOS_14
CL_CMOS_13
CL_CMOS_12
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CL_CMOS_08
CL_CMOS_07
CL_CMOS_06
CL_CMOS_05
CL_CMOS_04
CL_CMOS_03
CL_CMOS_02
CL_CMOS_01
3v3
GND
PLL Vcc Bypass Network
C903 0.001uF
C901 0.01uF
C902 0.1uF
Vcc Bypass Network
C906 0.001uF
C910 0.001uF
C911 0.01uF
C904 0.01uF
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LVDS Vcc Bypass Network
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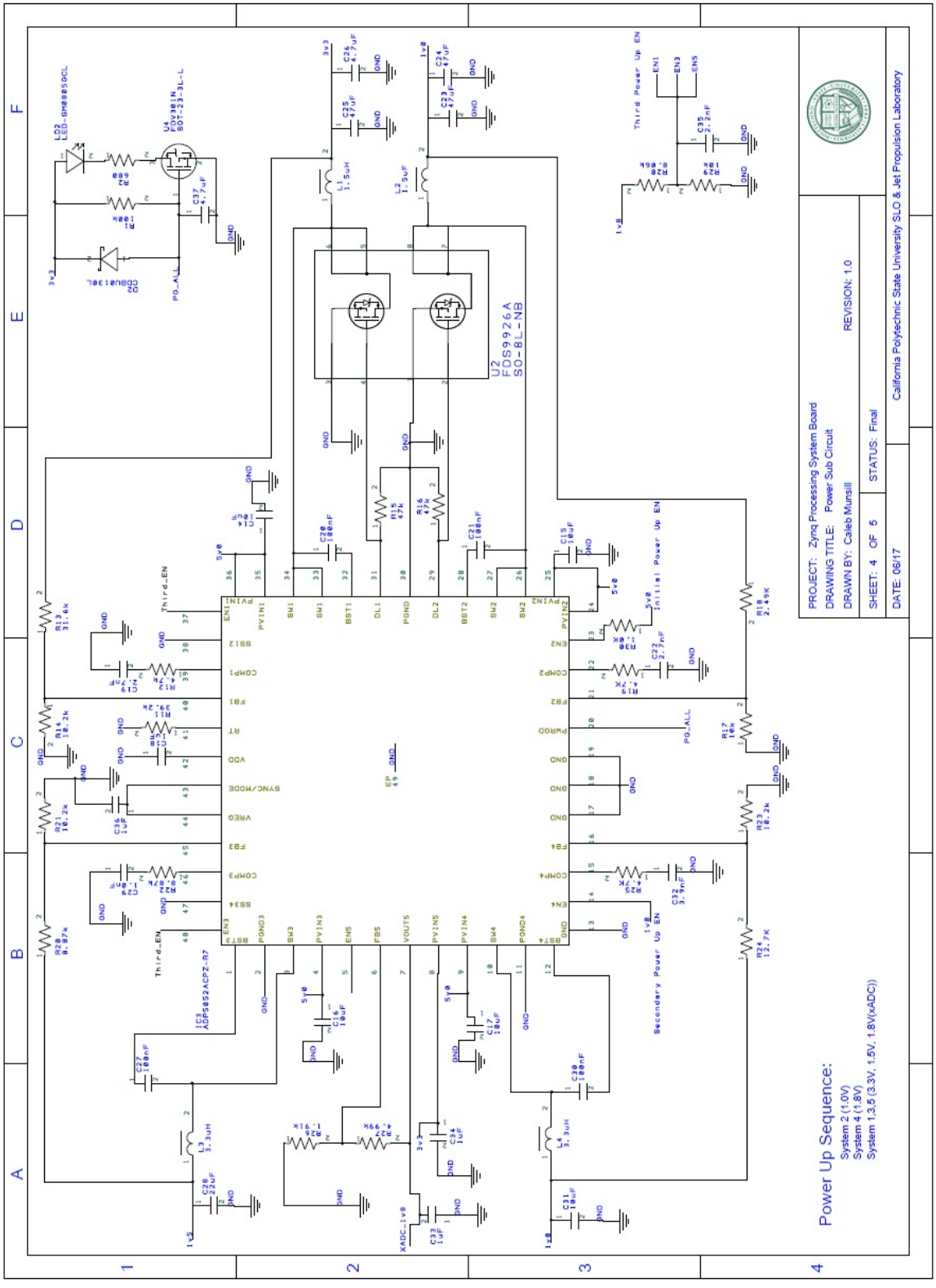
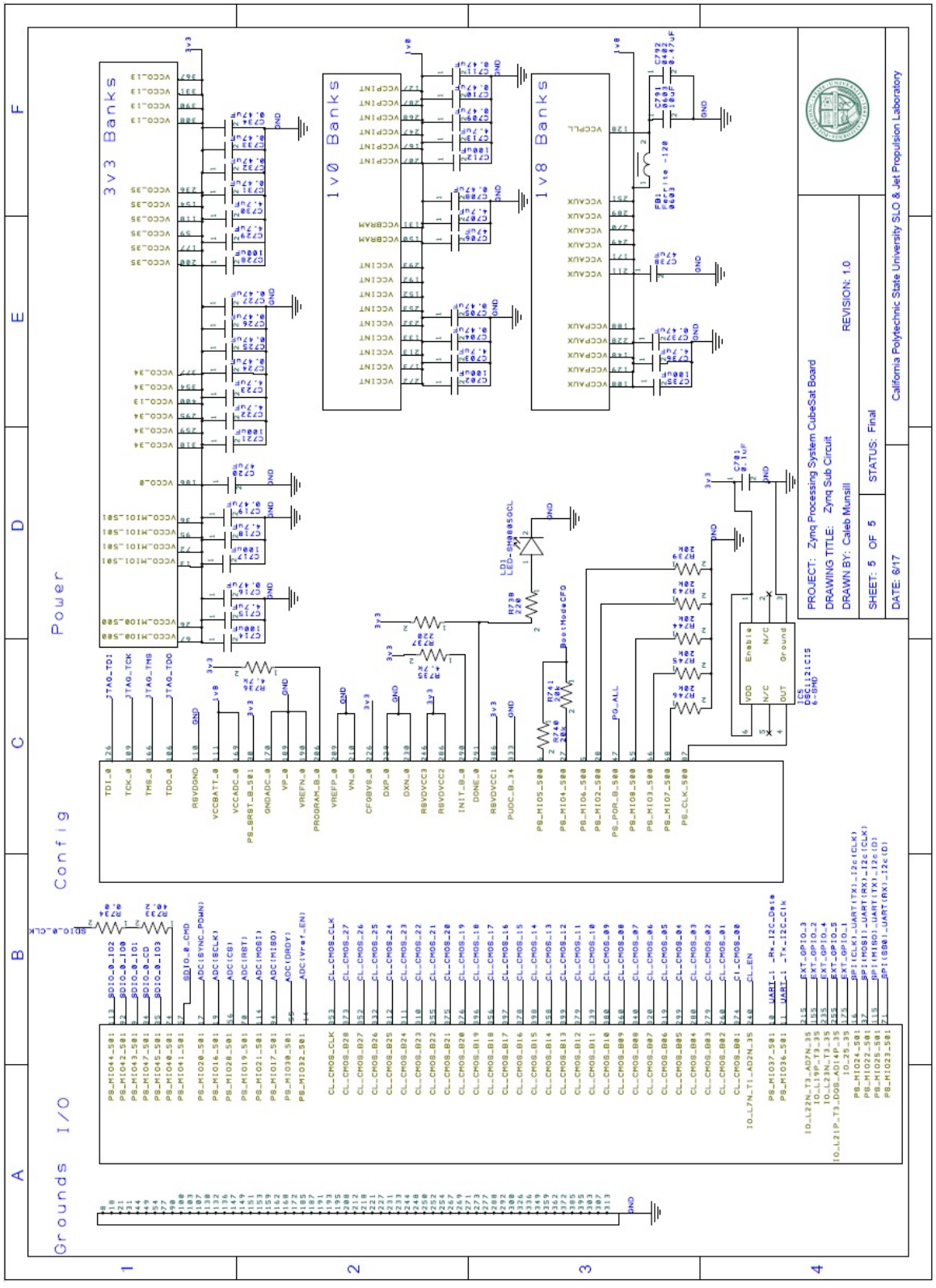
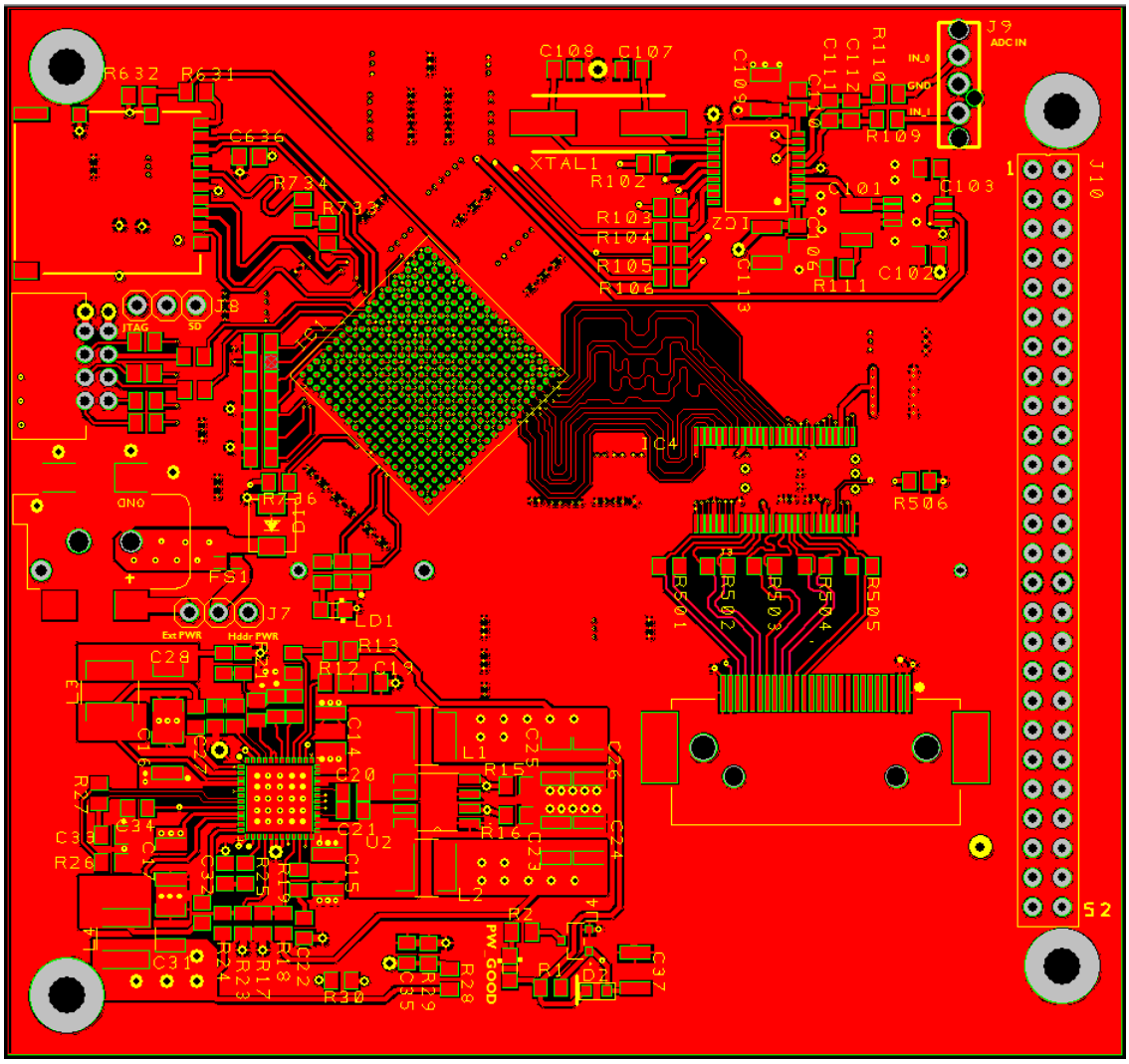
DRAWING TITLE: CameraLink Sub Circuit
DRAWN BY: Caleb Munsill
REVISION: 1.0
SHEET: 3 OF 5
STATUS: Final
DATE: 6/17
California Polytechnic State University SLO & Jet Propulsion Laboratory


PROJECT: Zynq Processing System Board
DRAWING TITLE: Power Sub Circuit
DRAWN BY: Caleb Munsill
REVISION: 1.0
SHEET: 4 OF 5
STATUS: Final
DATE: 06/17
California Polytechnic State University SLO & Jet Propulsion Laboratory
Power Up Sequence:
System 2 (1.0V)
System 4 (1.8V)
System 1,3,5 (3.3V, 1.5V, 1.8V(xADC))
U2
FDS9926A
SO-8L-NB
Third Power Up EN
Initial Power Up EN
Secondary Power Up EN
PG_ALL
Third_EN

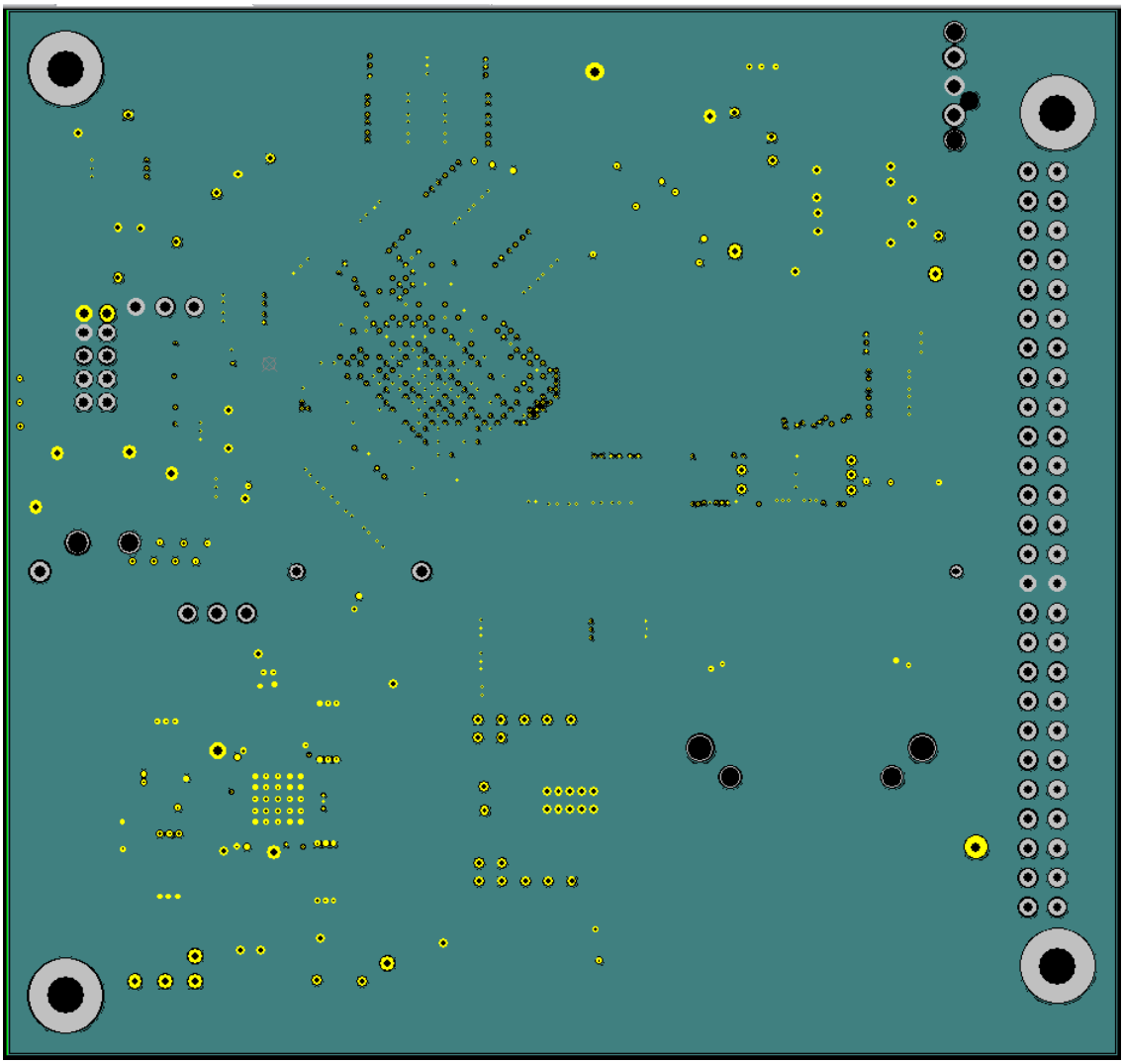

Grounds I/O
Config
Power
3v3 Banks
1v0 Banks
1v8 Banks
PROJECT: Zynq Processing System CubeSat Board
DRAWING TITLE: Zynq Sub Circuit
DRAWN BY: Caleb Munsill
REVISION: 1.0
SHEET: 5 OF 5
STATUS: Final
DATE: 6/17
California Polytechnic State University SLO & Jet Propulsion Laboratory

APPENDIX II – Board Layout

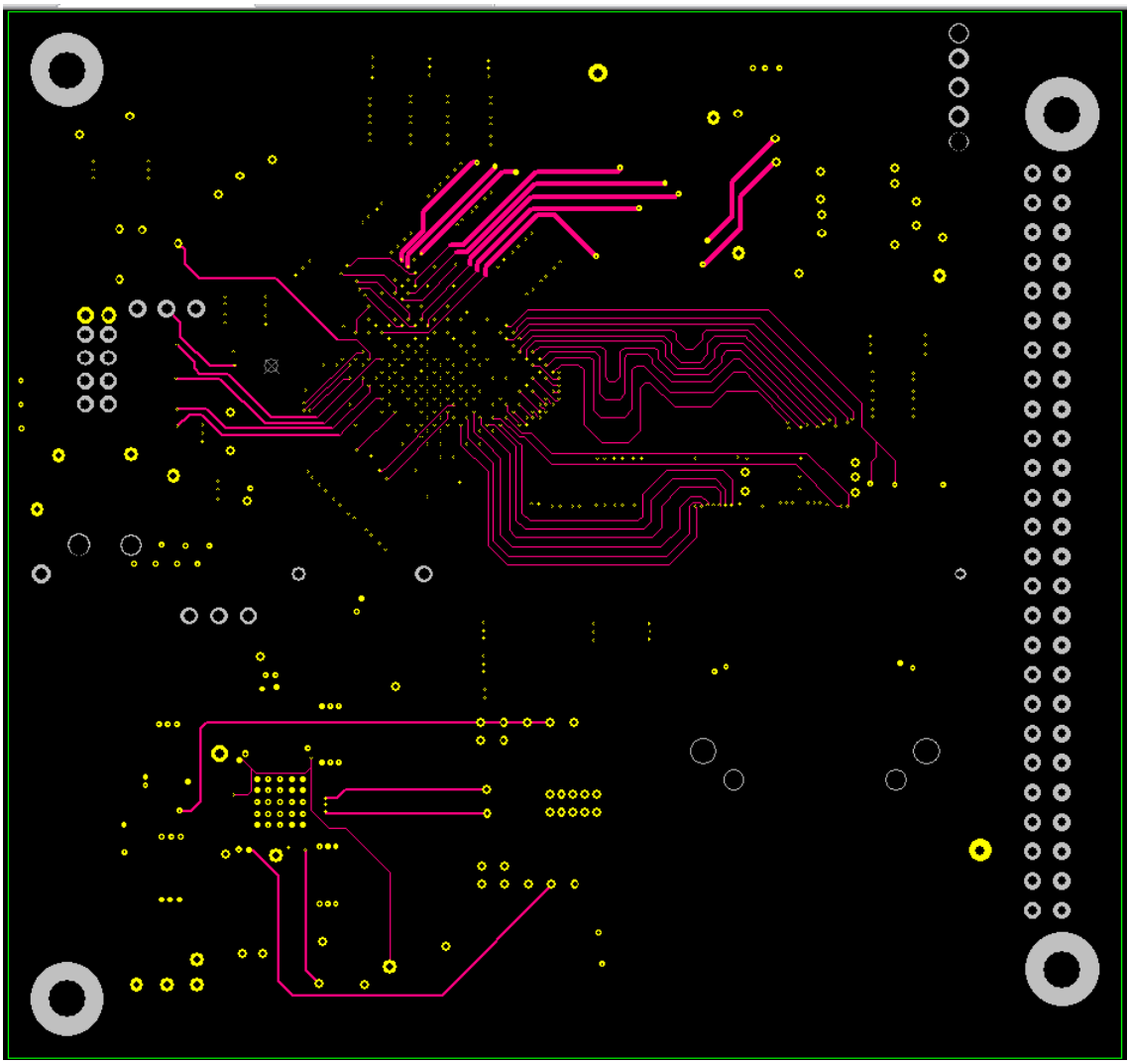
Layer 0 --- Top Board Layer



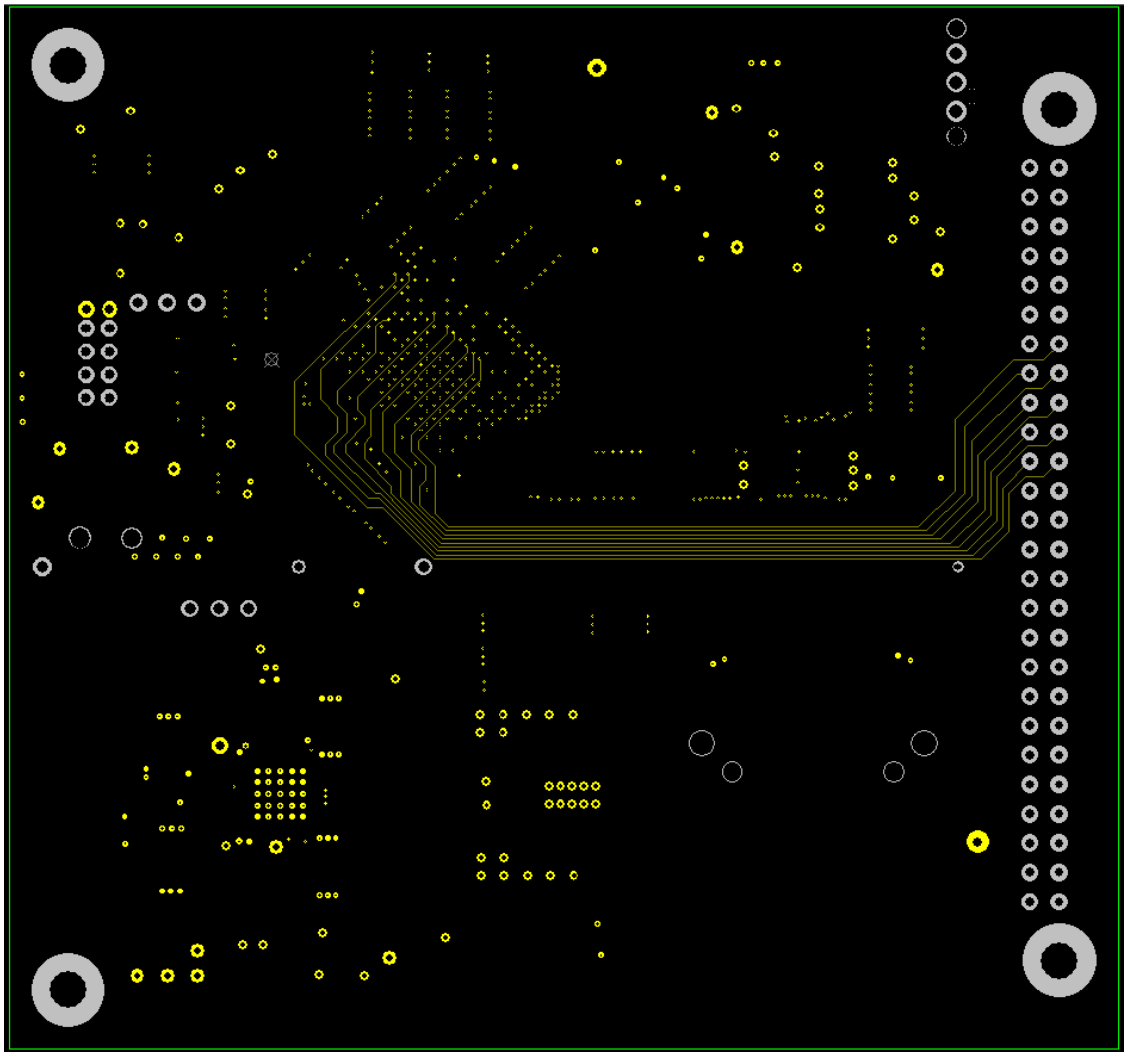
Layer 1 --- Negative Reference Plane



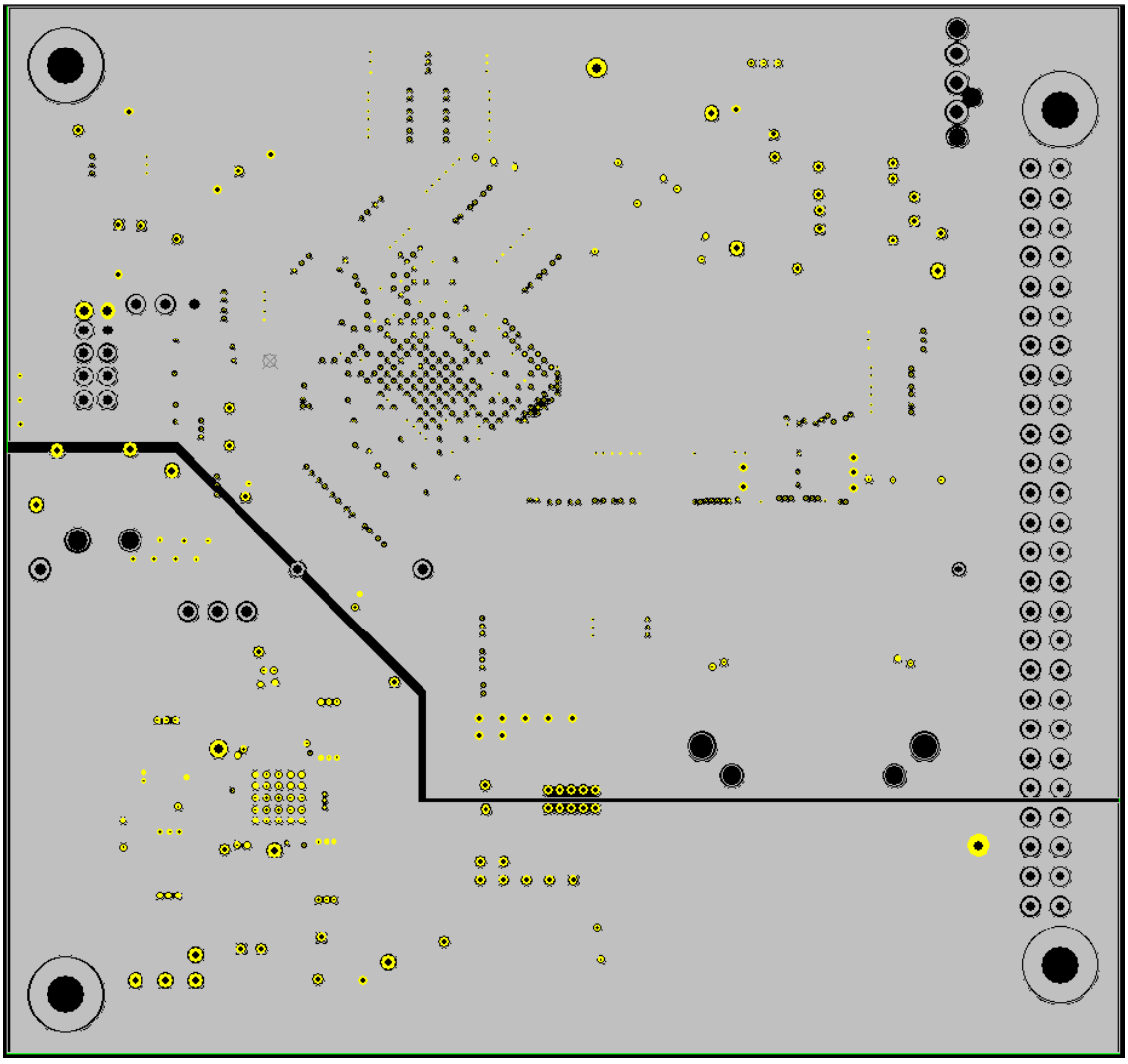
Layer 2 --- High Speed Signals



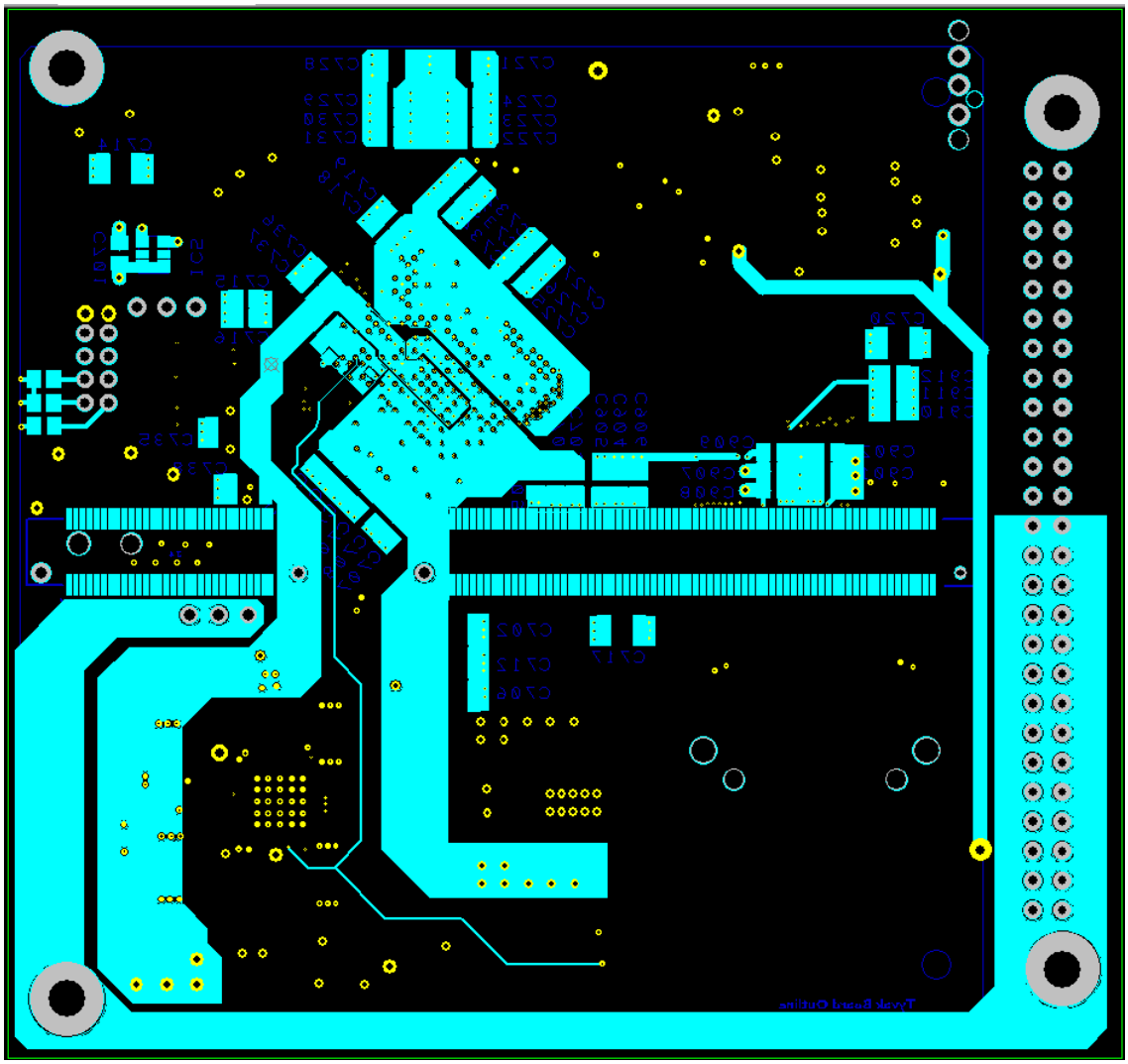
Layer 3 --- Low Speed Signals



Layer 4 --- Negative Reference Plane



Layer 5 --- Power Distribution Plane



APPENDIX III – Parts List

Major Component List							
Function	**Schem Ref ID**	**Component**	**Dimension**	**Package**	**Approx. Quiescent Power**	**Op-Temp**	**Notes**
Zynq SoC Model	IC1	XC7Z010-2CLG400I	17 x 17 mm	BGA (wire-bond)	Variable/Configurable	Industrial ver. −40°C to +100°C	Does not have high speed serial interface 100 I/O
Power Regulation	IC3	ADP5052 (ADP5052ACPZ-R7)	7 x 7mm	48-Lead Lead Frame Chip Scale Package	60mW	−40°C to +125°C	Used on Zybo Board
ADC	IC2	ADS1255IDBR	7.2x5.3mm	20SSOP	38mW (0.4mW in standby)	−40 to 85°C	24-bit 4th-order, delta-sigma 30kSPS SPI compatible 2 channels (single end)
Camera LVDS SerDes	IC4	DS90CR288AMTD/NOPB	14 × 8 mm	56 TSSOP		−10°C to+70°C	Meets functional specs but not thermal
USB/JTAG/UART (off board interface)	N.A.	FTDI FT2232HL (or HQ for smaller package)	10x10mm	LQFP-64		-40°C to 85°C	Allows UART and JTAG prog using single IC

Connector List

Component	Connector Purpose	Manufacturer	part #	Demension	Mounting	Quantity	Op-Temp	Notes
J6	8 - Pin Molax Right Angle Header	Molex	87833-0831	10.65x6.4mm	THRU HOLE	1	−55°C to +85°C	2mm Pitch
J3 - No Load	140 - pin Tyvak Interface	Hirose	140S-SV(21)-A	48 x 5.7 mm	SMD	1	−55°C to +85°C	
J4 - No Load	60 - pin Tyvak Interface	Hirose	60S-SV(21)	24 x 5.7 mm	SMD	1	−55°C to +85°C	
J2	26 - Pin 3M SDR CameraLink interface	3M	12226-8250-00FR	24.8 x 5mm	SMD	1	−40°C to +70°C	Right Angle Connection
J9	3 - pin Board Locking Header	Molex	105311-1203	10.72 x 6.36mm	THRU HOLE	1	−40°C to +115°C	2.5mm pitch
J10	52 - pin Board Inter Connect	Samtec	ESQ-126-39-G-D	4.95 x 66.55mm	THRU HOLE	1	−25 °C to +125°C	2.54 pitch
J8	3 - Pin Stan. 2.54mm Jumper header	TE	9-146278-0		THRU HOLE	1		
J7	3 - Pin Stan. 2.54mm Jumper header	TE	9-146278-0		THRU HOLE	1		
J5	DC Power Connector Berral Jack	CUI INK	PJ-002AH-SMT-TR	14.8x 9.0mm	SMD	1	−25 °C to +85°C	2mm center pin
J1	MircoSD Connector	Hirose	DM3AT-SF-PEJM5	11x16mm	SMD	1	−25 °C to +85°C	Push-Push

Sub-Component List

Component	MFG	Part #	Dimension	Package	Op-Temp	Value	Tol	Purpose	Notes	Rating	Subsystem
C101	AVX	F930J476MBA	1210	SMD	−55°C to +125°C	47 uF	20%	Vref ouput cap	Tantalum ESR:1Ω	6.3VDC	ADC
C102	AVX	08055C104K4T2A	0805	SMD	−55°C to +125°C	0.1uF	10%	Bypass	Ceramic	50VDC	ADC
C103	AVX	08055C105K4T2A	0805	SMD	−55°C to +125°C	1uF	10%	Vref Filter capacitor	Ceramic	50VDC	ADC
C106	AVX	08055C104K4T2A	0805	SMD	−55°C to +125°C	0.1uF	10%	Bypass	Ceramic	50VDC	ADC
C107	AVX	08055A180JAT2A	0805	SMD	−55°C to +125°C	18 pF	5%	xtal LD cap	Ceramic	50VDC	ADC

C108	AVX	08055A180JAT2A	0805	SMD	−55°C to +125°C	18 pF	5%	xtal LD cap	Ceramic	50VDC	ADC
C109	AVX	F931C106MBA	1210	SMD	−55°C to +125°C	10uF	20%	Bypass	Tantalum ESR:2Ω	16VDC	ADC
C110	AVX	08055C104K4T2A	0805	SMD	−55°C to +125°C	0.1uF	10%	Bypass	Ceramic	50VDC	ADC
C111	AVX	08051A101FAT2A	0805	SMD	−55°C to +125°C	100pF	1%	Input-Filter	Ceramic	50VDC	ADC
C112	AVX	08055C104JAT2A	0805	SMD	−55°C to +125°C	0.1uF	1%	Input-Filter	Ceramic	50VDC	ADC
C113	AVX	F931C106MBA	1210	SMD	−55°C to +125°C	10uF	20%	Bypass	Tantalum ESR:2Ω	16VDC	ADC
R102	ROHM	ESR10EZPF1000	0805	SMD	−55°C to +155°C	100Ω	1%	Track impead ctrl	Anti-ESD	150V, 0.4W	ADC
C14	AVX	F931C106MBA	1210	SMD	−55°C to +125°C	10uF	20%	Bypass	Tantalum ESR:2Ω	16VDC	PWR
C15	AVX	F931C106MBA	1210	SMD	−55°C to +125°C	10uF	20%	Bypass	Tantalum ESR:2Ω	16VDC	PWR
C16	AVX	F931C106MBA	1210	SMD	−55°C to +125°C	10uF	20%	Bypass	Tantalum ESR:2Ω	16VDC	PWR
C17	AVX	F931C106MBA	1210	SMD	−55°C to +125°C	10uF	20%	Bypass	Tantalum ESR:2Ω	16VDC	PWR
C18	AVX	08055C105K4T2A	0805	SMD	−55°C to +125°C	1uF	10%	VDD bypass	Ceramic	50VDC	PWR
C19	AVX	08055C272K4T2A	0805	SMD	−55°C to +125°C	2.7nF	10%	Error amplifier output Comp1	Ceramic	50VDC	PWR
C20	AVX	08055C104K4T2A	0805	SMD	−55°C to +125°C	100 nF	10%	High-Side FET Driver Power BST1	Ceramic	50VDC	PWR
C21	AVX	08055C104K4T2A	0805	SMD	−55°C to +125°C	100 nF	10%	High-Side FET Driver Power BST2	Ceramic	50VDC	PWR
C22	AVX	08055C272K4T2A	0805	SMD	−55°C to +125°C	2.7nF	10%	Error amplifier output Comp1	Ceramic	50VDC	PWR
C23	AVX	F930J476MBA	1210	SMD	−55°C to +125°C	47 uF	20%	Buck 2 output NTWK Cap 1of2	Tantalum ESR:1Ω	6.3VDC	PWR
C24	AVX	F930J476MBA	1210	SMD	−55°C to +125°C	47 uF	20%	Buck 2 output NTWK Cap 2of2	Tantalum ESR:1Ω	6.3VDC	PWR
C25	AVX	F930J476MBA	1210	SMD	−55°C to +125°C	47 uF	20%	Buck 1 output NTWK Cap 1of2	Tantalum ESR:1Ω	6.3VDC	PWR
C26	AVX	F930J475MAA	1206	SMD	−55°C to +125°C	4.7 uF	20%	Buck 1 output NTWK Cap 1of2	Tantalum ESR:4Ω	6.3VDC	PWR
C27	AVX	08055C104K4T2A	0805	SMD	−55°C to +125°C	100 nF	10%	High-Side FET Driver Power BST3	Ceramic	50VDC	PWR
C28	AVX	F930J226MBA	1206	SMD	−55°C to +125°C	22uF	20%	Buck 3 output NTWK Cap 1of1	Tantalum ESR:1.9Ω	6.3VDC	PWR
C29	AVX	08055C102K4T2A	0805	SMD	−55°C to +125°C	1nF	10%	Error amplifier output Comp3	Ceramic	50VDC	PWR

C30	AVX	08055C104K4T2A	0805	SMD	−55°C to +125°C	100 nF	10%	High-Side FET Driver Power BST4	Ceramic	50VDC	PWR
C31	AVX	F931C106MBA	1210	SMD	−55°C to +125°C	10uF	20%	Buck 4 output NTWK Cap 1of2	Tantalum ESR:2Ω	16VDC	PWR
C32	Vishay	VJ0805Y392KXACW1BC	0805	SMD	−55°C to +125°C	3.9nF	10%	Error amplifier output Comp4	Ceramic	50VDC	PWR
C33	AVX	08055C105K4T2A	0805	SMD	−55°C to +125°C	1uF	10%	LDO source (sys5) output cap	Ceramic	50VDC	PWR
C34	AVX	08055C105K4T2A	0805	SMD	−55°C to +125°C	1uF	10%	System 5 power input bypass	Ceramic	50VDC	PWR
C35	AVX	08051C222K4T2A	0805	SMD	−55°C to +125°C	2.2nF	10%	Input EN 1,3,5 bypass cap	Ceramic	100VDC	PWR
C36	AVX	08055C105K4T2A	0805	SMD	−55°C to +125°C	1uF	10%	Vreg Bypass	Ceramic	50VDC	PWR
R103	ROHM	ESR10EZPF1000	0805	SMD	−55°C to +155°C	100Ω	1%	Track impead ctrl	Anti-ESD	150V, 0.4W	ADC
R104	ROHM	ESR10EZPF1000	0805	SMD	−55°C to +155°C	100Ω	1%	Track impead ctrl	Anti-ESD	150V, 0.4W	ADC
R105	ROHM	ESR10EZPF1000	0805	SMD	−55°C to +155°C	100Ω	1%	Track impead ctrl	Anti-ESD	150V, 0.4W	ADC
R106	ROHM	ESR10EZPF1000	0805	SMD	−55°C to +155°C	100Ω	1%	Track impead ctrl	Anti-ESD	150V, 0.4W	ADC
R109	Bourns	CR0805-FX-3010ELF	0805	SMD	−55°C to +155°C	301Ω	1%	HF noise input filter	NA	150V, 1/8W	ADC
R110	Bourns	CR0805-FX-3010ELF	0805	SMD	−55°C to +155°C	301Ω	1%	HF noise input filter	NA	150V, 1/8W	ADC
R111	Vishay	WSL08055L000FEA	0805	SMD	−65°C to +170°C	5mΩ	1%	Vref cap ESR	NA	1/8W	ADC
R102	ROHM	ESR10EZPF1000	0805	SMD	−55°C to +155°C	100Ω	1%	Track impead ctrl	Anti-ESD	150V, 0.4W	ADC
R11	Bourns	CR0805-FX-3922ELF	0805	SMD	−55°C to +155°C	39.2KΩ	1%	Switching Freq Setting R	fset=497kHz	150V, 1/8W	PWR
R12	Bourns	CR0805-FX-4701ELF	0805	SMD	−55°C to +155°C	4.7kΩ	1%	Error amplifier output COMP1		150V, 1/8W	PWR
R13	Bourns	CR0805-FX-3162ELF	0805	SMD	−55°C to +155°C	41.6KΩ	1%	Feedback NTWk R1 FB1		150V, 1/8W	PWR
R14	Vishay	CRCW080510K2FKEA	0805	SMD	−55°C to +155°C	10.2KΩ	1%	Feedback NTWk R2 FB1		150V, 1/8W	PWR
R15	Bourns	CR0805-FX-4702ELF	0805	SMD	−55°C to +155°C	47kΩ	1%	Current limit setting resistor DL1		150V, 1/8W	PWR
R16	Bourns	CR0805-FX-4702ELF	0805	SMD	−55°C to +155°C	47kΩ	1%	Current limit setting resistor DL2		150V, 1/8W	PWR
R17	Bourns	CR0805-FX-1002ELF	0805	SMD	−55°C to +155°C	10KΩ	1%	Feedback NTWk R2 FB2		150V, 1/8W	PWR
R18	Bourns	CR0805-FX-2491ELF	0805	SMD	−55°C to +155°C	2.49KΩ	1%	Feedback NTWk R1 FB2		150V, 1/8W	PWR

R19	Bourns	CR0805-FX-4701ELF	0805	SMD	−55°C to +155°C	4.7KΩ	1%	Error amplifier output COMP2		150V, 1/8W	PWR
R20	Vishay	CRCW08058K87FKEA	0805	SMD	−55°C to +155°C	8.87KΩ	1%	Feedback NTWk R1 FB3		150V, 1/8W	PWR
R21	Vishay	CRCW080510K2FKEA	0805	SMD	−55°C to +155°C	10.2KΩ	1%	Feedback NTWk R2 FB3		150V, 1/8W	PWR
R22	Vishay	CRCW08058K87FKEA	0805	SMD	−55°C to +155°C	8.87KΩ	1%	Error amplifier output COMP3		150V, 1/8W	PWR
R23	Vishay	CRCW080510K2FKEA	0805	SMD	−55°C to +155°C	10.2KΩ	1%	Feedback NTWk R2 FB4		150V, 1/8W	PWR
R24	Bourns	CR0805-FX-1272ELF	0805	SMD	−55°C to +155°C	12.7KΩ	1%	Feedback NTWk R1 FB4		150V, 1/8W	PWR
R25	Bourns	CR0805-FX-4701ELF	0805	SMD	−55°C to +155°C	4.7KΩ	1%	Error amplifier output COMP2		150V, 1/8W	PWR
R26	Bourns	CR0805-FX-1911ELF	0805	SMD	−55°C to +155°C	1.91KΩ	1%	Feedback NTWk R2 FB5		150V, 1/8W	PWR
R27	Bourns	CR0805-FX-4991ELF	0805	SMD	−55°C to +155°C	4.99KΩ	1%	Feedback NTWk R1 FB5		150V, 1/8W	PWR
R28	Vishay	CRCW08058K06FKEA	0805	SMD	−55°C to +155°C	8.06KΩ	1%	V-div EN1,3,5 R1 input		150V, 1/8W	PWR
R29	Bourns	CR0805-FX-1002ELF	0805	SMD	−55°C to +155°C	10KΩ	1%	V-div EN1,3,5 R2 input		150V, 1/8W	PWR
R30	Bourns	CR0805-FX-1001ELF	0805	SMD	−55°C to +155°C	1KΩ	1%	EN 1 input		150V, 1/8W	PWR
L1	TDK	VLS5045EX-1R5N	5x5mm	SMD	−55°C to +155°C	1.5uH	30%	Buck 1 output NTWK inductor		@100k Rdc: 0.017 Isat: 7.4	PWR
L2	TDK	VLS5045EX-1R5N	5x5mm	SMD	−55°C to +155°C	1.5uH	30%	Buck 2 output NTWK inductor		@100k Rdc: 0.017 Isat: 7.4	PWR
L3	TDK	VLS5045EX-3R3N	5x5mm	SMD	−55°C to +155°C	3.3uH	30%	Buck 3 output NTWK inductor		@100k Rdc: 0.027 Isat: 5.2	PWR
L4	TDK	VLS5045EX-3R3N	5x5mm	SMD	−55°C to +155°C	3.3uH	30%	Buck 4 output NTWK inductor		@100k Rdc: 0.027 Isat: 5.2	PWR
U1	TI	REF6025IDGKT	3x5 mm	VSSOP	−40°C to +125°C	Percision Vref	±0.05%	ADC voltage V ref	NA	Tdrift (full op range)5ppm/°C	ADC
R631	ROHM	ESR10EZPF2000	0805	SMD	−55°C to +155°C	200Ω	1%	SD CD series resistance	Anti-ESD	150V, 0.4W	CONN
R632	Bourns	CR0805-FX-4702ELF	0805	SMD	−55°C to +155°C	47kΩ	1%	SD CD pull-up resistor	NA	150V, 1/8W	CONN
R635	ROHM	ESR10EZPF1000	0805	SMD	−55°C to +155°C	100Ω	1%	JTAG TMS series resistance	Anti-ESD	150V, 0.4W	CONN
R636	ROHM	ESR10EZPF1000	0805	SMD	−55°C to +155°C	100Ω	1%	JTAG TDO series resistance	Anti-ESD	150V, 0.4W	CONN
R637	ROHM	ESR10EZPF1000	0805	SMD	−55°C to +155°C	100Ω	1%	JTAG TCK series resistance	Anti-ESD	150V, 0.4W	CONN
R638	ROHM	ESR10EZPF1000	0805	SMD	−55°C to +155°C	100Ω	1%	UART Tx series resistance	Anti-ESD	150V, 0.4W	CONN
R639	ROHM	ESR10EZPF1000	0805	SMD	−55°C to +155°C	100Ω	1%	JTAG TDI series resistance	Anti-ESD	150V, 0.4W	CONN
R640	ROHM	ESR10EZPF1000	0805	SMD	−55°C to +155°C	100Ω	1%	UART Rx series resistance	Anti-ESD	150V, 0.4W	CONN

R641	Bourns	CR0805-FX-4701ELF	0805	SMD	−55°C to +155°C	4.7KΩ	1%	JTAG TMS pull-up resistor		150V, 1/8W	CONN
R642	Bourns	CR0805-FX-4701ELF	0805	SMD	−55°C to +155°C	4.7KΩ	1%	JTAG TDO pull-up resistor		150V, 1/8W	CONN
R643	Bourns	CR0805-FX-4701ELF	0805	SMD	−55°C to +155°C	4.7KΩ	1%	JTAG TCK pull-up resistor		150V, 1/8W	CONN
FS1	TE	0603SFV350F/32-2	0603	SMD	−55 C to + 125 C	3.5A	NA	System Fuse	NA	32VDC/35A	CONN
D1	Vishay	SMBJ5.0A-E3/52	2.44x4.57mm	SMD	−55 C to + 150 C	Vbr(min):6.40v	NA	Transient voltage suppressor	NA	Vbr(max):7.07 v	CONN
C636	AVX	08055C104K4T2A	0805	SMD	−55°C to +125°C	0.1uF	10%	Bypass	Ceramic	50VDC	CONN
XTAL 1	ECS	76.8-18-5PXEN-TR	11x4.8 mm	SM(XTAL)	−40°C to +85°C	7.68 MHz	30ppm (@25°C)	ADC Oscillator crystal	NA		ADC
R2	Bourns	CR0805-FX-6800ELF	0805	SMD	−55°C to +155°C	680	1%	PWR GOOD LED Current setting R		150V, 1/8W	PWR
R1	Bourns	CR0805-FX-1003ELF	0805	SMD	−55°C to +155°C	100KΩ	1%	PG_all signal Bypass Resistor		150V, 1/8W	PWR
C37	AVX	F930J475MAA	1206	SMD	−55°C to +125°C	4.7 uF	20%	PG_all signal Bypass Cap	Tantalum ESR:4Ω	6.3VDC	PWR
LD2	BIVAR	SM0805GCL	0805	SMD	−30°C to +80°C	Green		PWR GOOD LED	Von = 1.9V	30mA	PWR
D2	Comchip	CDBU0130L	0603	SMD	−25°C to +75°C	Vr =30v		PG_all Pin over voltage protection			PWR
U4	Infineon	BSS214N H6327		SOT-23	−55°C to +150°C	N-Channel FET		PWR good LED Ctrl	Vgs(th) = 950 mV		PWR
U2	Fairchild	FDS9926A		8-SOIC	−55°C to +150°C	2 N-Channel FET		Buck Switches 1 and 2		Id max:6.5A	PWR
C901	AVX	08055C103K4T2A	0805	SMD	−55°C to +125°C	0.01uF	10%	SerDes bypass cap	Ceramic	50VDC	CAM
C902	AVX	08055C104K4T2A	0805	SMD	−55°C to +125°C	0.1uF	10%	SerDes bypass cap	Ceramic	50VDC	CAM
C903	AVX	08055C102K4T2A	0805	SMD	−55°C to +125°C	1nF	10%	SerDes bypass cap	Ceramic	50VDC	CAM
C904	AVX	08055C103K4T2A	0805	SMD	−55°C to +125°C	0.01uF	10%	SerDes bypass cap	Ceramic	50VDC	CAM
C905	AVX	08055C104K4T2A	0805	SMD	−55°C to +125°C	0.1uF	10%	SerDes bypass cap	Ceramic	50VDC	CAM
C906	AVX	08055C102K4T2A	0805	SMD	−55°C to +125°C	1nF	10%	SerDes bypass cap	Ceramic	50VDC	CAM
C907	AVX	08055C103K4T2A	0805	SMD	−55°C to +125°C	0.01uF	10%	SerDes bypass cap	Ceramic	50VDC	CAM
C908	AVX	08055C102K4T2A	0805	SMD	−55°C to +125°C	1nF	10%	SerDes bypass cap	Ceramic	50VDC	CAM
C909	AVX	08055C104K4T2A	0805	SMD	−55°C to +125°C	0.1uF	10%	SerDes bypass cap	Ceramic	50VDC	CAM
C910	AVX	08055C102K4T2A	0805	SMD	−55°C to +125°C	1nF	10%	SerDes bypass cap	Ceramic	50VDC	CAM
C911	AVX	08055C103K4T2A	0805	SMD	−55°C to +125°C	0.01uF	10%	SerDes bypass cap	Ceramic	50VDC	CAM

C912	AVX	08055C104K4T2A	0805	SMD	−55°C to +125°C	0.1uF	10%	SerDes bypass cap	Ceramic	50VDC	CAM
R506	Bourns	CR0805-FX-1002ELF	0805	SMD	−55°C to +155°C	10KΩ	1%	/POWER_EN pull down resistor		150V, 1/8W	PWR
R501	ROHM	ESR10EZPF1000	0805	SMD	−55°C to +155°C	100Ω	1%	Termination resistor for LVDS0	Anti-ESD	150V, 0.4W	CAM
R502	ROHM	ESR10EZPF1000	0805	SMD	−55°C to +155°C	100Ω	1%	Termination resistor for LVDS1	Anti-ESD	150V, 0.4W	CAM
R503	ROHM	ESR10EZPF1000	0805	SMD	−55°C to +155°C	100Ω	1%	Termination resistor for LVDS2	Anti-ESD	150V, 0.4W	CAM
R504	ROHM	ESR10EZPF1000	0805	SMD	−55°C to +155°C	100Ω	1%	Termination resistor for LVDSCLK	Anti-ESD	150V, 0.4W	CAM
R505	ROHM	ESR10EZPF1000	0805	SMD	−55°C to +155°C	100Ω	1%	Termination resistor for LVDS3	Anti-ESD	150V, 0.4W	CAM
C701	AVX	08055C104K4T2A	0805	SMD	−55°C to +125°C	0.1uF	10%	Clock gen bypass Cap	Ceramic	50VDC	ZIC
R506	Bourns	CR0805-FX-4702ELF	0805	SMD	−55°C to +155°C	47kΩ	1%	CL_En Pull down resistor	NA	150V, 1/8W	CAM
C702	MuRata	GRM32EE70G107ME19L	1210	SMD	−55°C to +125°C	100uF	20%	VccINT Bypass Cap	X7U	4VDC	ZIC
C703	MuRata	GRM21BR71A475KA73K	0805	SMD	−55°C to +125°C	4.7uF	10%	VccINT Bypass Cap	X7R	10VDC	ZIC
C704	MuRata	LLM215R70J474MA11L	0805	SMD	−55°C to +125°C	.47uF	20%	VccINT Bypass Cap	X7R	6.3VDC	ZIC
C705	MuRata	LLM215R70J474MA11L	0805	SMD	−55°C to +125°C	.47uF	20%	VccINT Bypass Cap	X7R	6.3VDC	ZIC
C706	MuRata	GRM32ER70J476ME20L	1210	SMD	−55°C to +125°C	47uF	20%	Vbram Bypass Cap	X7R	6.3VDC	ZIC
C707	MuRata	GRM21BR71A475KA73K	0805	SMD	−55°C to +125°C	4.7uF	10%	Vbram Bypass Cap	X7R	10VDC	ZIC
C708	MuRata	LLM215R70J474MA11L	0805	SMD	−55°C to +125°C	.47uF	20%	Vbram Bypass Cap	X7R	6.3VDC	ZIC
C709	MuRata	LLM215R70J474MA11L	0805	SMD	−55°C to +125°C	.47uF	20%	Vccpint Bypass Cap	X7R	6.3VDC	ZIC
C710	MuRata	LLM215R70J474MA11L	0805	SMD	−55°C to +125°C	.47uF	20%	Vccpint Bypass Cap	X7R	6.3VDC	ZIC
C711	MuRata	LLM215R70J474MA11L	0805	SMD	−55°C to +125°C	.47uF	20%	Vccpint Bypass Cap	X7R	6.3VDC	ZIC
C712	MuRata	GRM32EE70G107ME19L	1210	SMD	−55°C to +125°C	100uF	20%	Vccpint Bypass Cap	X7U	4VDC	ZIC
C713	MuRata	GRM21BR71A475KA73K	0805	SMD	−55°C to +125°C	4.7uF	10%	Vccpint Bypass Cap	X7R	10VDC	ZIC
C714	MuRata	GRM32EE70G107ME19L	1210	SMD	−55°C to +125°C	100uF	20%	VccMIO500 Bypass Cap	X7U	4VDC	ZIC
C715	MuRata	GRM21BR71A475KA73K	0805	SMD	−55°C to +125°C	4.7uF	10%	VccMIO500 Bypass Cap	X7R	10VDC	ZIC
C716	MuRata	LLM215R70J474MA11L	0805	SMD	−55°C to +125°C	.47uF	20%	VccMIO500 Bypass Cap	X7R	6.3VDC	ZIC

C717	MuRata	GRM32EE70G107ME19L	1210	SMD	−55°C to +125°C	100uF	20%	VccMIO501 Bypass Cap	X7U	4VDC	ZIC
C718	MuRata	GRM21BR71A475KA73K	0805	SMD	−55°C to +125°C	4.7uF	10%	VccMIO501 Bypass Cap	X7R	10VDC	ZIC
C719	MuRata	LLM215R70J474MA11L	0805	SMD	−55°C to +125°C	.47uF	20%	VccMIO501 Bypass Cap	X7R	6.3VDC	ZIC
C720	MuRata	GRM32ER70J476ME20L	1210	SMD	−55°C to +125°C	47uF	20%	Vcc0 Bypass Cap	X7R	6.3VDC	ZIC
C721	MuRata	GRM32EE70G107ME19L	1210	SMD	−55°C to +125°C	100uF	20%	Vcc34 Bypass Cap	X7U	4VDC	ZIC
C722	MuRata	GRM21BR71A475KA73K	0805	SMD	−55°C to +125°C	4.7uF	10%	Vcc34 Bypass Cap	X7R	10VDC	ZIC
C723	MuRata	GRM21BR71A475KA73K	0805	SMD	−55°C to +125°C	4.7uF	10%	Vcc34 Bypass Cap	X7R	10VDC	ZIC
C724	MuRata	LLM215R70J474MA11L	0805	SMD	−55°C to +125°C	.47uF	20%	Vcc34 Bypass Cap	X7R	6.3VDC	ZIC
C725	MuRata	LLM215R70J474MA11L	0805	SMD	−55°C to +125°C	.47uF	20%	Vcc34 Bypass Cap	X7R	6.3VDC	ZIC
C726	MuRata	LLM215R70J474MA11L	0805	SMD	−55°C to +125°C	.47uF	20%	Vcc34 Bypass Cap	X7R	6.3VDC	ZIC
C727	MuRata	LLM215R70J474MA11L	0805	SMD	−55°C to +125°C	.47uF	20%	Vcc34 Bypass Cap	X7R	6.3VDC	ZIC
C728	MuRata	GRM32EE70G107ME19L	1210	SMD	−55°C to +125°C	100uF	20%	Vcc35 Bypass Cap	X7U	4VDC	ZIC
C729	MuRata	GRM21BR71A475KA73K	0805	SMD	−55°C to +125°C	4.7uF	10%	Vcc35 Bypass Cap	X7R	10VDC	ZIC
C730	MuRata	GRM21BR71A475KA73K	0805	SMD	−55°C to +125°C	4.7uF	10%	Vcc35 Bypass Cap	X7R	10VDC	ZIC
C731	MuRata	LLM215R70J474MA11L	0805	SMD	−55°C to +125°C	.47uF	20%	Vcc34 Bypass Cap	X7R	6.3VDC	ZIC
C732	MuRata	LLM215R70J474MA11L	0805	SMD	−55°C to +125°C	.47uF	20%	Vcc34 Bypass Cap	X7R	6.3VDC	ZIC
C733	MuRata	LLM215R70J474MA11L	0805	SMD	−55°C to +125°C	.47uF	20%	Vcc34 Bypass Cap	X7R	6.3VDC	ZIC
C734	MuRata	LLM215R70J474MA11L	0805	SMD	−55°C to +125°C	.47uF	20%	Vcc34 Bypass Cap	X7R	6.3VDC	ZIC
C735	MuRata	GRM32EE70G107ME19L	1210	SMD	−55°C to +125°C	100uF	20%	VccpAux Bypass Cap	X7U	4VDC	ZIC
C736	MuRata	GRM21BR71A475KA73K	0805	SMD	−55°C to +125°C	4.7uF	10%	VccpAux Bypass Cap	X7R	10VDC	ZIC
C727	MuRata	LLM215R70J474MA11L	0805	SMD	−55°C to +125°C	.47uF	20%	VccpAux Bypass Cap	X7R	6.3VDC	ZIC
C738	MuRata	GRM32ER70J476ME20L	1210	SMD	−55°C to +125°C	47uF	20%	VCCAux Bypass Cap	X7R	6.3VDC	ZIC
C791	MuRata	GRM188R60G106ME47D	0603	SMD	−55°C to +88°C	10uF	20%	VccPLL Bypass Cap	X5R	4VDC	ZIC
C792	MuRata	GRM155R60J474KE19D	0402	SMD	−55°C to +85°C	0.47uF	10%	VccPLL Bypass Cap	X5R	6.3VDC	ZIC
FB1	MuRata	BLM18SG121TN1D	0603	SMD	−55°C to +125°C	120Ω @100MHz	25%	VccPLL Ferrite Bead		3A	ZIC
LD1	BIVAR	SM0805GCL	0805	SMD	−30°C to +80°C	Green		PL CONF Complete LED	Von = 1.9V	30mA	ZIC

R733	Bourns	CR0805-FX-4022ELF	0805	SMD	−55°C to +155°C	40.2KΩ	1%	SDIO CLK Impeadance ctrl R1		150V, 1/8W	ZIC
R734	Bourns	CR0805-J/-000ELF	0805	SMD	−55°C to +155°C	0Ω		SDIO CLK Impeadance ctrl R2			ZIC
R735	Bourns	CR0805-FX-4701ELF	0805	SMD	−55°C to +155°C	4.7KΩ	1%	Init_B Pull Up Pin resistor		150V, 1/8W	ZIC
R736	Bourns	CR0805-FX-4701ELF	0805	SMD	−55°C to +155°C	4.7KΩ	1%	Program_B Pull Up Pin resistor		150V, 1/8W	ZIC
R737	ROHM	ESR10EZPF2200	0805	SMD	−55°C to +155°C	220Ω	1%	Done_0 Pull Up	Anti-ESD	150V, 0.4W	ZIC
R738	ROHM	ESR10EZPF2200	0805	SMD	−55°C to +155°C	220Ω	1%	Done_0 LED Current Set Resistor	Anti-ESD	150V, 0.4W	ZIC
R739	Bourns	CR0805-FX-2002ELF	0805	SMD	−55°C to +155°C	20KΩ	1%	CFG Pin Pull Down		150V, 1/8W	ZIC
R740	Bourns	CR0805-FX-2002ELF	0805	SMD	−55°C to +155°C	20KΩ	1%	CFG Pin Pull Down/Up		150V, 1/8W	ZIC
R741	Bourns	CR0805-FX-2002ELF	0805	SMD	−55°C to +155°C	20KΩ	1%	CFG Pin Pull Down/Up		150V, 1/8W	ZIC
R742	Bourns	CR0805-FX-2002ELF	0805	SMD	−55°C to +155°C	20KΩ	1%	CFG Pin Pull Down		150V, 1/8W	ZIC
R743	Bourns	CR0805-FX-2002ELF	0805	SMD	−55°C to +155°C	20KΩ	1%	CFG Pin Pull Down		150V, 1/8W	ZIC
R744	Bourns	CR0805-FX-2002ELF	0805	SMD	−55°C to +155°C	20KΩ	1%	CFG Pin Pull Down		150V, 1/8W	ZIC
R745	Bourns	CR0805-FX-2002ELF	0805	SMD	−55°C to +155°C	20KΩ	1%	CFG Pin Pull Down		150V, 1/8W	ZIC
R746	Bourns	CR0805-FX-2002ELF	0805	SMD	−55°C to +155°C	20KΩ	1%	CFG Pin Pull Down		150V, 1/8W	ZIC
U3	MicroChip	DSC1121CL5-050.0000	3.2 x 2.5 mm	SMD	−40°C to +85°C	50 MHz	10ppm	Zynq Oscilator	MEMS oscillator		ZIC