# CdTe Solar Cells: Key Layers and Electrical Effects

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# Abstract

This thesis presents various studies into the effects of both growth and processing conditions on a) the electrical properties of interfaces of the CdTe solar cell, and b) the photovoltaic (PV) performance. Annealing of the CdS/TCO (transparent conductive oxide) bilayer in both oxidising and reducing ambients was investigated in order to study changes in the electrical properties of the In/CdS/TCO structure. It was found that post-growth oxidising changed the current–voltage (*J*-*V*) characteristics from Ohmic to rectifying, which was attributed to the creation of a CdO-$n^+$/CdS-n junction, as an oxygen-rich layer was revealed by Auger electron spectroscopy (AES) on the CdS surface. A new method of testing pinholing of the CdS film was used, which gave confidence that the observed Ohmic behaviour was genuine.

Annealing CdS (in various ambients) was further investigated by studying its effect on full devices, but the effect on PV performance was insignificant. This study was paired with an investigation into a rapid screening method of optimising CdTe/CdS cell PV performance, which reduced the number of the required samples by a factor of ~ 30. This was achieved by varying the CdTe thickness by chemically bevelling the cells in a $Br_2$/methanol solution. The best performance was obtained at a CdTe thickness of ~ 3 μm, for which the $CdCl_2$ treatment used was optimum. Both the uniformity and roughness of the cell layers are vital to obtaining high quality results using this methodology.

The electrical current transport mechanism in the CdTe/CdS heterojunction was investigated as a function of a) growth technique by which devices were fabricated, and b) window layer type. Data were collected by recording *J*-*V*-*T* measurements in different light intensities (including dark), with temperature being varied in the range of 200 – 300 K. The transport mechanism was found to be dependent only on the window material under forward bias condition in the dark, but was independent of both the window layer and growth technique in a) forward bias in the light, and b) reverse bias in the dark. A new method was used to determine the diode ideality factor in the light, and therefore identify the transport mechanism.

The back contact of the CdTe/CdS cell was investigated by measuring its barrier height ($\phi_b$). In a preliminary study, two methods of $\phi_b$ measurement were compared, with the most applicable method being used to study Au, $Sb_2Te_3$ and $As_2Te_3$ contacts, with the CdTe back surface being either a) as-grown, b) nitric/phosphoric acid etched or c) plasma etched. The value of the barrier height for each contact and its impact on the cell performance are presented and discussed.

# Declaration

I declare that with the exception of those procedures listed below all the work presented in this thesis was carried out by the candidate. I also declare that none of this work has previously been submitted for any degree and that it is not being submitted for any other degree.

MOCVD samples reported in Chapters 6 and 7 were provided by Dr. Vincent Barrioz, Glyndŵr University.

GIXRD measurements in Chapter 5 were performed by Dr. Alex Pym, Durham University.

SIMS and AES measurements in Chapter 5 were performed by Loughborough Surface Analysis Ltd.

……..
Prof. Ken Durose
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……..
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I owe my deepest gratitude to my mother for her love, patience and prayers. Whatever I write here will not show my gratefulness to her, but I will say that I would never be able to finish this thesis (as all my achieved successes) without her help.

Finally, I thank my brothers, sisters and friends (they know themselves) for their kindness and support.

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| | |
|---|---|
| AES | Auger electron spectroscopy |
| BDH | $Br_2$/dichrol/hydazine |
| BM | $Br_2$/methanol |
| CBD | Chemical bath deposition |
| C-F | Capacitance-frequency |
| CSS | Close space sublimation |
| CVD | Chemical vapour deposition |
| DC | Direct current |
| DLTS | Deep level transient spectroscopy |
| EQE | External quantum efficiency |
| GIXRD | Grazing incidence X-ray diffraction |
| ITO | Indium tin oxide |
| IQE | Internal quantum efficiency |
| J-V | Current-voltage characteristics |
| J-V-T | Current-voltage-temperature characteristics |
| MOCVD | Metal-Organic Chemical Vapour Deposition |
| ND | Natural density |
| N-P | Nitric/phosphoric acid |
| PL | Photoluminescence |
| PVD | Physical vapour deposition |
| QE | Quantum efficiency |
| RF | Radio frequency |
| SCLC | Space charge limited current |
| SEM | Scanning electron microscopy |
| SIMS | Secondary ion mass spectroscopy |
| SRH | Shockley-Read-Hall |
| TCO | Transparent conductive oxide |
| XPS | X-ray photoelectron spectroscopy |
| XRD | X-ray diffraction |

# Chapter 1: Introduction

## 1.1 Energy sources and alternatives

Most of the energy currently consumed is supplied from fossil fuels. The main issue of those sources is sustainability, especially with the continuous increase of the demand for energy. Moreover, $CO_2$ emission from coal and petroleum products creates more environmental problems such as global warming. The global $CO_2$ emission has been growing rapidly as shown in Figure 1.1 [1], causing dramatic climate changes beside other health issues. However, their low cost is one of the main advantages of fossil fuels in comparison to other sources.

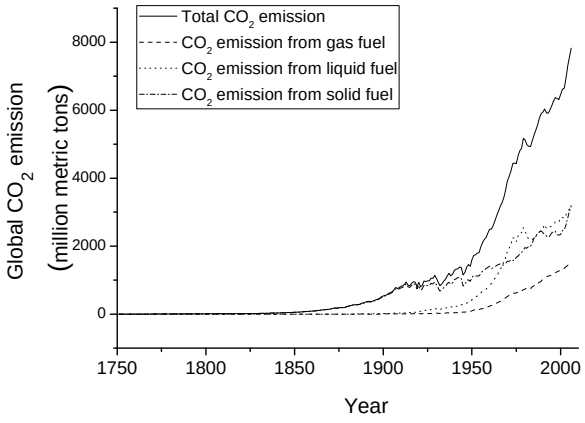


**Figure 1.1**: The rapid increase in the global $CO_2$ emission from 1950 to 2006.

Therefore, the search for other energy sources is necessary. Nuclear power and renewables seem to be promising candidates to replace fossil fuels. However, each alterative has its own problems such as the treatment of the nuclear waste and the cost of photovoltaics. Good reviews have been published for renewables such as [2, 3].

## 1.2 Solar cell development and challenges

The first reported photogalvanic behaviour was published in 1839 by Beqcuerel [4] after he produced a photocurrent by shining light on an electrode in an electrolyte solution. In 1877 Adams and Day reported photovoltaic behaviour in

selenium [5]. However, in 1954 the Si p-n [6] and $Cu_x$/CdS [7] cells were reported with efficiencies ~ 6 % for each device. Solar cells were improved rapidly in the following years in both i) performance, and ii) the variety of materials used to fabricate the cells [8-10].

Covering only 1 % of the land area on Earth with 10 % efficient solar cells would produce twice the current need of energy worldwide [11]. However, the high cost of solar cells at the present time is a significant barrier to their true mass adoption due to market forces. Certainly, the specific cost ($/$W_p$) of Si solar cells has reduced year-on-year, as is shown in Figure 1.2, and this cost reduction is itself driven by increases in high volume manufacturing (Figure 1.3) i.e. the "learning rate" of production.

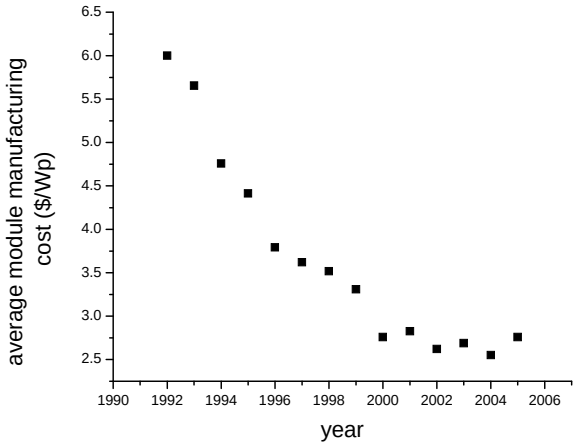


**Figure 1.2**: The average manufacturing cost of Si solar modules in the time range from 1992 to 2005 [12].

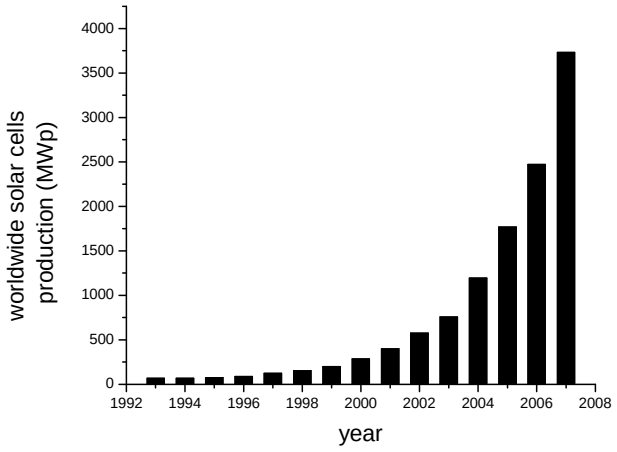


**Figure 1.3**: The increase in PV production from 1993 until 2007 [13].

An alternative means of reducing cost is to substitute the present leading technologies (bulk Si) with products having intrinsically lower cost: it is this which has motivated the drive towards thin-film PV over the past 30 years. Similarly, the promise of even lower cost PV based on organic materials has stimulated research in that area. Figure 1.4 shows the historical development of lab efficiencies for all of the main types of solar cells. The figure clearly demonstrates that the progress in efficiency improvement, as approximated by a straight line, is remarkably similar for all single junction PV technologies, regardless of their type e.g. single crystal Si improves at 0.52 % while organics improve at 0.43 % per annum, these being the fastest and slowest. Table 1.1 shows the full set of slopes. A consequence of this universal – and slow – improvement rate is that no single technology has overtaken any other. Nevertheless, efficiency improvements do contribute to a reduction in specific cost, and it is this cost which governs the relative competitiveness of each cell technology. This highlights the need to develop strategies for rapid progress in the development of new and emerging PV devices.

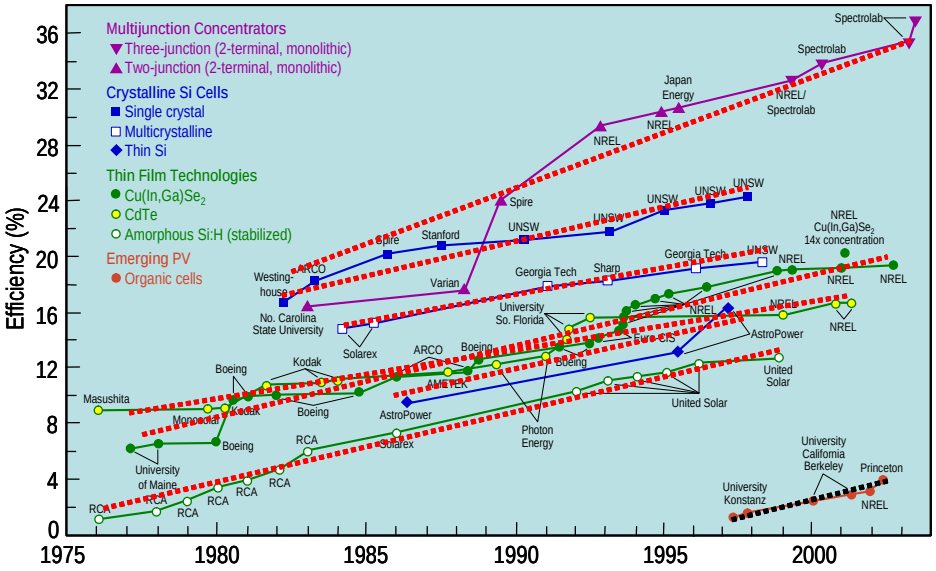


**Figure 1.4**: Progress in different PV materials from 1975 to 2003 [14]. The dashed line is the linear fit of each set of points.

| Material | Increase in η / year |
|---|---|
| Multi-junction concentrators | 0.83 |
| Si single crystal | 0.52 |
| Si multi-crystalline | 0.40 |
| Thin Si | 0.50 |
| $Cu(In,Ga)Se_2$ | 0.50 |
| CdTe | 0.46 |
| a-Si:H | 0.48 |
| organic | 0.43 |

**Table 1.1**: The improvement rate of solar cells efficiency using different PV materials, as extracted from Figure 1.4.

## 1.3 Solar resource and conversion

### 1.3.1 Solar spectrum

The Sun can be assumed to radiate as a black body with $T$ = 5760 K [8], which results in an emitted power density at its surface of ~ 62 MW/m$^2$. Based on the distance between Earth and the Sun, the power received on the Earth surface can be calculated. However, the spectrum reaching Earth is distorted by the absorption by some elements and compounds in the atmosphere such as water and $O_2$.

The effect of the atmosphere on the solar spectrum (i.e. the loss in spectrum resulting from the atmosphere) is measured by the *Air Mass* factor, which is the cosecant of the elevation angle of the sun. The standard illumination is chosen to be *Air Mass* 1.5 (or AM1.5) which corresponds to an elevation angle of 42°, and power density of ~ 1000 W/m$^2$. The AM1.5 spectrum is shown in Figure 1.5.

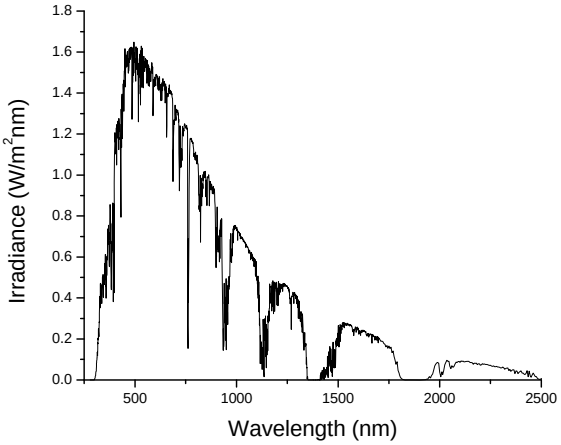


**Figure 1.5**: AM1.5 solar spectrum.

### 1.3.2 Absorption in semiconductors

Photon absorption in semiconductors depends on nature of the band gap $E_g$. There are two kinds of band gaps for semiconductors: direct and indirect. For direct band gap materials, electrons are elevated across the gap if the photon energy $\geq E_g$. However, in indirect materials, lattice vibration (phonons) should be involved in the transition process so that the momentum $k$ is conserved (Figure 1.6 shows energy versus the momentum ($k$) diagram for both processes). As a result, the absorption

probability is much higher for direct band gap materials than in indirect band gap ones. The required thickness for an indirect band gap material to absorb the solar spectrum fully is ~ 20-50 μm whereas it is only 1-3 μm in the case of a direct band gap material [15].

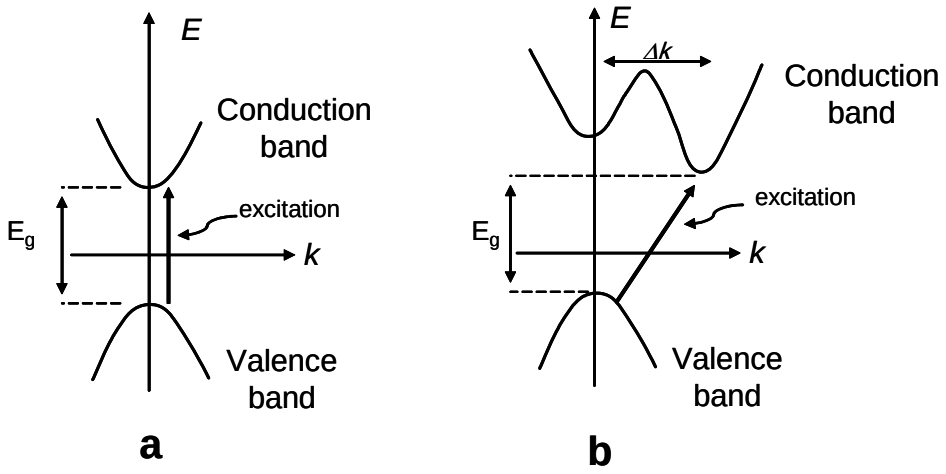


**Figure 1.6**: The direct (a) and indirect (b) band gap transitions in semiconductors.

## 1.4 Materials for solar cells

There are various materials used to fabricate solar cells. Each material has its own advantages and disadvantages. In this Section, a few of them will be discussed briefly. The world record efficiencies for devices using these materials are summarized in Table 1.2 [16], and the progress in the performance is shown in Figure 1.4.

| Material | Best η (%) |
|---|---|
| Si single crystal | 25.0 ± 0.5 |
| Si polycrystalline | 20.4 ± 0.5 |
| Si amorphous | 9.5 ± 0.3 |
| GaAs | 26.1 ± 0.8 |
| InP | 22.1 ± 0.7 |
| CIGS | 19.4 ± 0.6 |
| CdTe | 16.7 ± 0.5 |

**Table 1.2**: The world record efficiency for the most commonly used PV materials from reference 16.

### 1.4.1 Si

Si is the most dominant photovoltaic material in the PV market. It has an indirect band gap with $E_g$ = 1.1 eV. Si has been used in semiconductor applications for a long time. For example, the only widely available homojunction solar cell in 1981 was the Si cell [9]. Extensive research on Si is being conducted, providing a deep knowledge about the properties of this material.

Since it is an indirect band gap material, the thickness needed to fabricate cells is relatively high (few hundred microns thick). As a result, high diffusion lengths of the carriers are required, which therefore necessitates having highly pure Si for fabricating solar cells. These factors result in the high cost of Si cells. Cost reduction has been achieved by changing the material properties. It has been reported [10] that both the production of the raw material for Si and the processing of creating single crystal wafers represent ~ 65 % of the total cost. Hence, the use of polycrystalline Si (poly-Si) material for solar cells reduces the manufacturing cost not only by reducing the processing cost but also by allowing the use of relatively poor quality material [9]. However, poly-Si cells suffer from several factors such as the recombination in grain boundaries, which decreases their conversion efficiencies by ~ 5 % compared to crystalline Si cells (Table 1.2).

Thinner Si cells were fabricated by using amorphous Si, which has a direct band gap of 1.7 eV. Since amorphous Si (a-Si) is a direct band gap material, the

thickness required to absorb the light is smaller than that for crystalline Si. Moreover, a-Si enjoys other advantages such as the cost and the possibility of growing on various substrates [8]. Nevertheless, its amorphous nature introduces new challenges. For example, the defect density in a-Si is > $10^{16}$ $cm^{-3}$. However, this issue might be overcome by passivating the dangling bonds using hydrogen. Treatment in 5-10 % hydrogen reduces defect density to $10^{15}$ $cm^{-3}$, which may be suitable for fabricating solar cells [8]. Another issue of a-Si devices is the performance stability. When the material is exposed to light, its photoconductivity decreases due to creation of dangling bonds. This behaviour is called Staebler–Wronski effect [10]. a-Si solar cell can be paired with nanocrystalline Si cells (which have indirect $E_g$ of ~ 1.1 eV) to form a tandem solar cell [9].

### 1.4.2 III-V materials

GaAs is an example of these materials. It has a direct band gap of 1.43 eV which is close to the required value of the optimum efficiency (see Section 2.7). Like other III-V materials, GaAs has attracted attention due to its suitability for electronic applications such as the opto-electronic devices [10]. Because of the high cost of the III-V single crystal cells, they are usually used with concentrators or for space application. InP is particularly suitable to space applications owing to its high resistance to radiation.

Besides the high cost, the inadequate supply of group III elements limit the uptake of these kinds of solar cells.

### 1.4.3 Chalcopyrite materials

Because of the high cost of bulk Si and III-V solar cells, thin film solar cells are a very promising alternative. Copper indium diselenide (CIS) is one among the PV materials suitable for fabricating thin film solar cells. It has a direct band gap of 1.04 eV, however, this band gap can be engineered by introducing Ga, leading to copper indium, gallium diselenide (CIGS). The main disadvantages of CIGS are the high cost of In besides the issue of insufficient sources of Ga.

### 1.4.4 CdTe

CdTe is a direct band gap semiconductor ($E_g$ ~ 1.45 eV) having the zincblende structure and a high absorption coefficient. The first CdTe/CdS solar cell was fabricated by Bonnet and Rabenhorst [17] in 1972 with efficiency ~ 5 %. As seen in Figure 1.4, the efficiency has been developed significantly since then, and the current world record for CdTe cells is 16.5 % [18]. Since CdTe/CdS solar cells are the main topic of this thesis, a full review is provided in Chapter 3.

## 1.5 The Scope of This Thesis

This Section outlines briefly the contents of this thesis. In Chapter 2, various semiconductor junctions are described along with the basic physics of solar cells and methods of parameter extraction and transport mechanisms. Six methods of determining the ideality factor (*n*) of a p-n junction are also reviewed in Section 2.4. The electrical transport mechanisms which were observed in this work (and discussed in detail in Chapter 6) are described in Section 2.5. A new method (Section 2.5.4) was tested to identify the current transport mechanism under light conditions.

A review of CdTe devices is presented in Chapter 3, including CdS/TCO interface, CdS annealing and its effect on the PV performance, $CdCl_2$ post-growth treatment (for CdTe), intermixing between CdTe and CdS layers, current transport mechanisms in the CdTe/CdS junction and back contacts for CdTe devices.

Chapter 4 describes the experimental procedures applied in the thesis. It includes growth techniques, material processing and characterization methods used throughout this work.

The effects of a) pre-growth treatment of the TCO, and b) the post-growth treatment of the CdS on the electrical behaviour of the CdS/TCO bilayer are reported in Chapter 5. Both oxidising and reducing annealing conditions were applied to the samples in order to investigate the annealing-induced changes by recording *J-V* characteristics for each sample. The chemical changes in the samples were tested by X-ray diffraction and Auger electron spectroscopy.

In addition, Chapter 5 reports the development and use of a rapid screening / bevelling method to study the performance of the devices as a function of CdTe thickness. CdS films (in these samples) were post-growth annealed in different ambients in order to examine the effect of this treatment on the PV performance of the

complete devices. Therefore, the performance was investigated as a function of a) the CdS treatment, and b) the CdTe thickness.

In Chapter 6 the electrical transport mechanism of the carriers across the CdTe/CdS heterojunction was studied. The *J-V-T* method was applied to explore the most dominant electrical transport mechanisms for three different devices under both forward and reverse bias conditions. Dark and light *J-V-T* data were recorded for all samples so that the effect of illumination on the transport mechanism was investigated. Testing different devices allowed studying the change in the transport mechanism by changing the a) growth techniques, and b) window layer material.

The last results chapter is Chapter 7 in which the back contact of the CdTe/CdS cells was investigated. Five methods for determining the back contact barrier height were reviewed, from which the most appropriate method was chosen for investigating other contacts. The validity of this method was tested in a preliminary study. Au, $Sb_2Te_3$ and $As_2Te_3$ contacts were investigated with as-grown, N-P etched and plasma etched CdTe cells.

The conclusion of this thesis along with suggestions for future work are presented in Chapter 8. Finally, the series resistance $R_s$ of the cells was determined by several methods in order to choose the most suitable method, which was used to determine the barrier height in Chapter 7. The results of the $R_s$ study are reported in Appendix A. A mathematical derivation of the Shockley equation, and the physical meaning of the ideality factor are presented in Appendix B. Selected *J-V-T* curves for cells investigated in Chapter 6 are shown in Appendix C.

## 1.6 References for Chapter 1


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# Chapter 2: Junction Physics and Solar Cells

## 2.1 Junctions in semiconductor devices

Semiconductor junctions are categorized as: i) metal/semiconductor junctions (Schottky and Ohmic), and ii) semiconductor/semiconductor junctions (homojunction and heterojunction). These four junctions are described briefly below.

*Schottky junction*

This junction is created at a metal/semiconductor interface. The features and the behaviour of the junction vary depending on the electrical properties of materials (both the metal and the semiconductor). Figure 2.1a shows a metal and a p-type semiconductor before contact. The vacuum level is used as a reference for all other levels. The work function of the metal is assumed to be smaller than that of the semiconductor ($\phi_m < \phi_s$). After contact (Figure 2.1b), the Fermi levels on both sides should align with each other. To satisfy this condition, holes must flow from semiconductor to metal leaving behind them negatively charged acceptor atoms, until the Fermi levels become aligned. The charged atoms on the semiconductor side establish the *depletion region*. Consequently, the rest of the holes in the semiconductor side face a barrier height $\Phi$ preventing them from crossing the junction. For a Schottky contact with a p-type semiconductor [1]

$$\Phi \approx \phi_m - (\chi_s + E_g) \qquad (2.1)$$

where $\chi_s$ is the electron affinity of the semiconductor. An analogous description can be made for an n-type semiconductor.

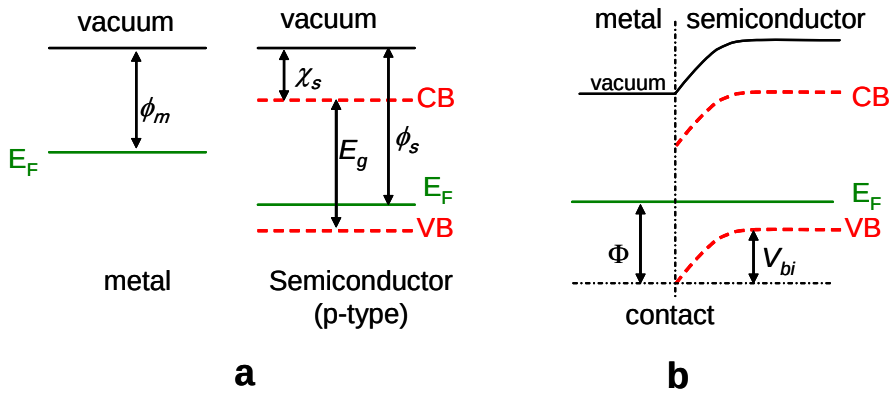


**Figure 2.1**: a) The energy band diagrams of a metal and a p-type semiconductor before contact, b) the change in the band alignment after contact showing the resulting Schottky barrier.

*Ohmic contact*

For a p-type semiconductor, Ohmic contact can be created if $\phi_m \geq \chi_s + E_g$ [1]. The energy bands for a metal and a semiconductor describing this condition are shown in Figure 2.2. In Figure 2.2b, holes in the valence band do not face any barrier, and can transport freely.

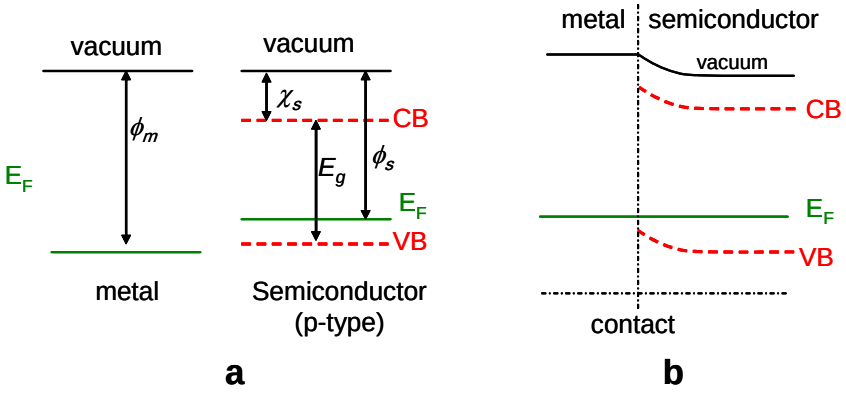


**Figure 2.2**: a) The energy band diagrams of a metal and a p-type semiconductor before contact, b) the change in the band alignment after contact showing the resulting Ohmic contact.

Another way to make an Ohmic contact is by allowing carriers to tunnel through the barrier. A condition like that can be approached by heavily doping the

semiconductor near its interface with the metal [2]. Figure 2.3 shows the same barrier as Figure 2.1b, but with the semiconductor surface being heavily doped. This kind of contact should have the same characteristics of the Ohmic one. Back contacts for CdTe cells are usually made by heavily doping the back surface before metallization. Further discussion about CdTe back contact is presented in Chapter 7.

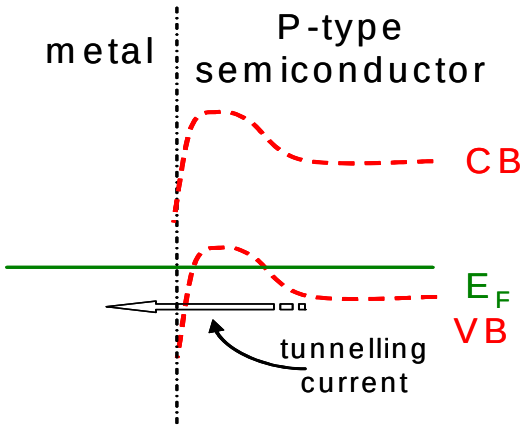


**Figure 2.3**: Changing Schottky contact to an Ohmic one by creating high density of localized states within the energy barrier.

*Homojunction*

Homojunctions arise from the contact between p- and n-type semiconductors under the condition that both parts are made of the same material. Usually this structure is manufactured by doping one side of the semiconductor with donors and the other side with acceptors. Since energy bands on both sides are identical, the junction does not have “energy spikes” i.e. barriers to transport.

As for other junctions, the Fermi level has to align in order to form the junction. Electrons flow from the n-type side to the p-type side leaving positively charged ions in the bulk close to the interface, and holes do exactly the opposite. Hence, a depleted part of the bulk (i.e. depletion region) is created with a built-in electric field opposing more carriers to move across as shown in Figure 2.4.

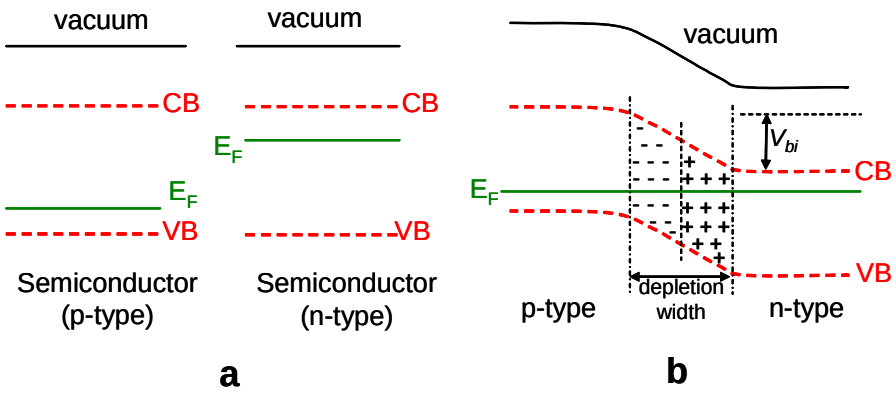


**Figure 2.4**: Semiconductor/semiconductor homojunction a) before, b) after contacting.

*Heterojunction*

This junction is established between p-type and n-type semiconductors as for the homojunction, however, unlike the homojunction, the two sides are not made of the same material and their energy bands are different. When the Fermi levels align, spikes in the bands can be created. Figure 2.5 illustrates the bands before and after contact. This junction is commonly used for solar cells fabricated with direct band gap materials.

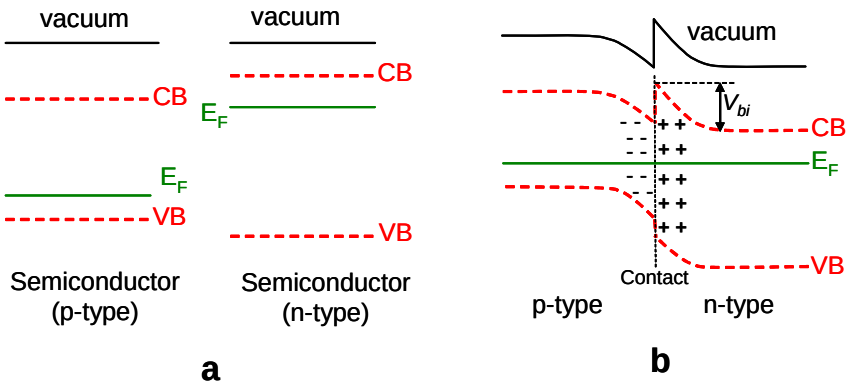


**Figure 2.5**: a) Two different semiconductors before contact, b) the heterojunction resulting from contacting the semiconductors in part a).

The energy-band diagram of heterojunction can be determined using Anderson's rule [3, 4]. In this rule, the vacuum levels of the semiconductors in both

sides are aligned before contact. However, after contact, the Fermi level should be at the same energy across both the junction and the bulk materials i.e. Fermi level is aligned. Thus, by knowing the electron affinity, the work function and the band gap of each side of the junction, both the built-in potential and the bands offsets can be calculated. The limitation of the Anderson's rule is that it considers only ideal junctions in which there are no interface traps.

## 2.2 Depletion layer capacitance

Since the CdTe/CdS heterojunction is a p-n junction, only this type of junction is considered in this Section. It is mentioned in Section 2.1 that in order to align the Fermi level across the junction, majority carriers should transfer from each side to the other, which creates the depletion region. This part of the device can be assumed as a parallel-plate capacitor due to the opposite charge distribution across it.

Based on the charge distribution, the junction can be classified as: a) abrupt, where the impurity concentration change sharply from donors to acceptors or vice versa, and b) linearly graded, where the impurity concentration changes linearly across the junction.

For the abrupt junction, solving Poisson's equation allows determination of the depletion region width (usually called depletion width) from equation 2.2 [5],

$$W = \sqrt{\frac{2\varepsilon}{q}\left(\frac{N_A + N_D}{N_A N_D}\right)V_{bi}} \qquad (2.2)$$

where $W$ is the depletion width, $\varepsilon$ is the dielectric constant of the material, $V_{bi}$ is the built-in potential, $q$ is the electronic charge and $N_A$ and $N_D$ are the doping concentrations in p- and n-side of the junction respectively. However, if one side of the junction is substantially more doped than the other (i.e. $N_A >> N_D$ or vice versa) then equation 2.2 will be

$$W = \sqrt{\frac{2\varepsilon V_{bi}}{q N_B}} \qquad (2.3)$$

where $N_B$ is the doping concentration of the lightly-doped side. This is the so-called one-sided junction. $W$ changes with the external applied voltage $V$, and can be determined from

$$W = \sqrt{\frac{2\varepsilon (V_{bi} - V)}{q N_B}} \qquad (2.4)$$

The capacitance of this junction $C$ is defined as

$$C = \frac{\varepsilon}{W} \qquad (2.5)$$

By using equations 2.4 and 2.5

$$C = \sqrt{\frac{\varepsilon q N_B}{2 (V_{bi} - V)}} \qquad (2.6)$$

or

$$\frac{1}{C^2} = \frac{2(V_{bi} - V)}{q\varepsilon N_B} \qquad (2.7)$$

Equation 2.7 implies that both $N_B$ and $V_{bi}$ can be determined from the slope and the intercept of the line resulting from plotting $1/C^2$ as a function of $V$ respectively. This is usually achieved by applying variable external voltage across the junction and measure the capacitance. This kind of experiment is called *C-V measurement*, and it was used to analyse some samples in Chapter 6.

## 2.3 The diode equation

The key part of the solar cell is the device junction (e.g. Schottky, homojunction or heterojunction). The basic idea is to generate electrical carriers by absorbing the visible light in (or at least near) the junction. The generated carriers are

driven by the built-in electric field within the depletion region to the external circuit. The dark current of the ideal p-n junction solar cell is described by the Shockley diode equation [6],

$$J = J_0[\exp(\frac{qV}{nkT}) - 1] \qquad (2.8)$$

where $J$ is the current density, $J_0$ is the saturation current density, $q$ is the electronic charge, $V$ is the applied voltage, $k$ is Boltzmann constant, $T$ is the temperature and $n$ is the ideality factor (see Appendix B for the derivation of Shockley equation). The physical meaning of the ideality factor and its mathematical origin are discussed in Section 2.4 and Appendix B).

If the cell is illuminated then it will produce a light generated current $J_L$ and equation 2.8 becomes

$$J = J_0[\exp(\frac{qV}{nkT}) - 1] - J_L \qquad (2.9)$$

The equivalent circuit of the ideal solar cell is illustrated in Figure 2.6 [7].

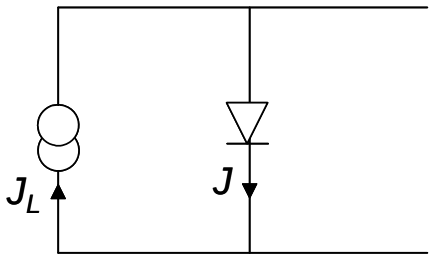


**Figure 2.6**: The equivalent circuit of an ideal solar cell.

In the actual devices there are two resistances added to the equivalent circuit as they considerably affect the PV performance of the cells. The first is the *series resistance* $R_s$, which is due to both the bulk material and the contacts of the device. The second is the *shunt resistance* $R_{sh}$ which is due to leakage such as pinholes. Series and shunt resistances can be added to equation 2.9 to give

$$J = J_0\{\exp[\frac{q(V - JR_s)}{nkT}] - 1\} + \frac{V - JR_s}{R_{sh}} - J_L \qquad (2.10)$$

For the ideal cell $R_s = 0$ and $R_{sh} = \infty$ which returns equation 2.10 to equation 2.9. The solar cell equivalent circuit including these resistances is shown in Figure 2.7. The effect of these resistances on solar cell performance is discussed in Section 2.8.

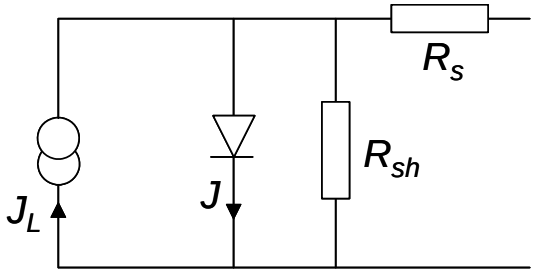


**Figure 2.7**: The equivalent circuit of the non-ideal solar cell including series and shunt resistances.

## 2.4 Ideality factor

This factor (sometimes called diode factor – *n*), which is mentioned in equation 2.8, indicates the ideality of the junction i.e. the validity of describing the junction behaviour by the Shockley equation (equation 2.8), and should have a value of unity for the ideal junction, where diffusion dominates the current [2]. However, *n* will have higher values if the junction deviates from the ideal case e.g. as recombination currents start to dominate. The behaviour of this factor as a function of temperature plays an important role in determining the electrical transport mechanisms across the junctions (see Chapter 6). More details about the variation of this factor with different current transport processes are presented in Appendix B.

Many methods have been applied to determine the value of the ideality factor from experiments and some are now described.

a) *Sites and Mauk method*

Sites and Mauk [8] differentiated equation 2.10 and expressed it in the following from:

$$\frac{dV}{dJ} = R_s + V_0 \left( \frac{1 - R_{sh}^{-1} \frac{dV}{dJ}}{J + J_L - \frac{V}{R_{sh}}} \right) \qquad (2.11)$$

where $V_0 = \frac{nkT}{q}$ . Thus, plotting $\frac{dV}{dJ}$ versus the value between the parentheses in equation 2.11 should yield a straight line, and the ideality factor can be extracted from the slope. In the case that $R_{sh}$ is sufficiently large, equation 2.11 becomes

$$\frac{dV}{dJ} = R_s + \frac{V_0}{J + J_L} \qquad (2.12)$$

For this case, $n$ can be calculated from the slope of $\frac{dV}{dJ}$ versus $\frac{1}{J + J_L}$. Hence in order to apply this model to real devices (i.e. equation 2.11) the values of $R_s$, $R_{sh}$ and $J_L$ must be known.

b) *Quanxi and Enke method*

Quanxi and Enke [9] reported measurement of $n$ by an analytical method. They defined a linear relationship between $J$ and $V$ by equation

$$J = \frac{J_{sc}}{V_{oc}} V \qquad (2.13)$$

where $J_{sc}$ is the short circuit current density and $V_{oc}$ is the open circuit voltage. The intersection of this line with the illuminated $J$-$V$ curve was defined as a point $P$, having coordinates $J_p$, $V_p$, and being different from the maximum power point. Based

on the calculations made, $n$ can be determined for ideal solar cells ($R_s = 0$ and $R_{sh} = \infty$) from the equation

$$n = \frac{V_{oc} q}{nkT} \frac{m-1}{\ln(1-m)} \tag{2.14}$$

where $m = \frac{V_p}{V_{oc}}$, $V_P$ being determined from the intercept as described above. However, if either $R_s$ or $R_{sh}$ have significant values, equation 2.14 becomes more complicated. For example, if both resistances are not negligible then equation 2.14 will be

$$n = \frac{\frac{(m-1)V_{oc} + mJ_{sc}R_s}{nkT/q}}{\ln\left\{\frac{J_{sc}(1+R_s/R_{sh})(1-m) - mV_{oc}/R_{sh}}{J_{sc}(1+R_s/R_{sh}) - V_{oc}/R_{sh}}\right\}} \tag{2.15}$$

Besides the complexity of the calculation in this method, it requires the values of several parameters such as $m$, $R_s$, $R_{sh}$, $J_{sc}$ and $V_{oc}$.

c) *Jain and Kapoor method*

This method calculates $n$ by using a Lambert W-function [10], which is a mathematical function for solving transcendental equations. Equation 2.10 was solved as a transcendental equation, and expressed (by using Lambert W-function) for $J$ as

$$J = \frac{V_{oc}}{R_s + R_{sh}} + \frac{Lambert\,W\left[\frac{R_s J_0 R_{sh}\left[R_{sh}(V + R_s + J_0 + R_s + J_L)/(nV_{th}(R_s + R_{sh})\right]}{nV_{th}(R_s + R_{sh})}\right] nV_{th}}{R_s} + \frac{R_{sh}(J_0 + J_L)}{R_s + R_{sh}} \tag{2.16}$$

Although no approximations are made in this method, $V_{oc}$, $R_s$, $R_{sh}$, $J_0$ and $J_L$ must be known in order to extract $n$ by using it i.e. the inaccuracy in these values may affect

the accuracy of the method itself. Moreover, this method requires a relatively long calculation in comparison to the slope method (described below) for example.

e) *Rau and Schock method*

Rau and Schock [11] described the current in Cu(In,Ga)$Se_2$ solar cells by the equation

$$J = J_0 \exp(\frac{qV}{nkT}) - J_{sc} = J_{00} \exp(\frac{-E_a}{nkT}) \exp(\frac{qV}{nkT}) - J_{sc} \qquad (2.17)$$

where $J_{00}$ is a constant and $E_a$ is the activation energy. Under the open-circuit condition equation 2.17 will be

$$V_{oc} = \frac{E_a}{q} - \frac{nkT}{q} \ln(\frac{J_{00}}{J_{sc}}) \qquad (2.18)$$

Thus, plotting $V_{oc}$ as a function of ln $J_{sc}$ (usually achieved by measuring the PV performance at various light intensities) would result in a straight line from which $n$ is calculated. The advantage of this method is that it avoids complications from $R_s$ as it has no influence under open-circuit condition.

f) *Slope method*

The value of $n$ can be easily determined by using equation 2.8 (for dark measurements), where exp($qV/nkT$) - 1 can be approximated as exp($qV/nkT$), and the equation can be rewritten as

$$\ln J = \ln J_0 + \frac{qV}{nkT} \qquad (2.19)$$

By plotting ln $J$ versus $V$ (for forward bias) the values of $n$ and $J_0$ can be extracted from the slope and the intercept of the resultant line respectively. Equation 2.19 assumes that $R_s$ and $R_{sh}$ are negligible. This approximation is valid at only some parts of the plot. It is seen in Figure 2.8 that the plot of the “ideal” diode is a straight line as expected from equation 2.19. However, if $R_s$ is not negligible the line deviates

from linearity. The slope from which $n$ is extracted should be calculated from the straight part (i.e. where $R_s$ has a negligible influence).

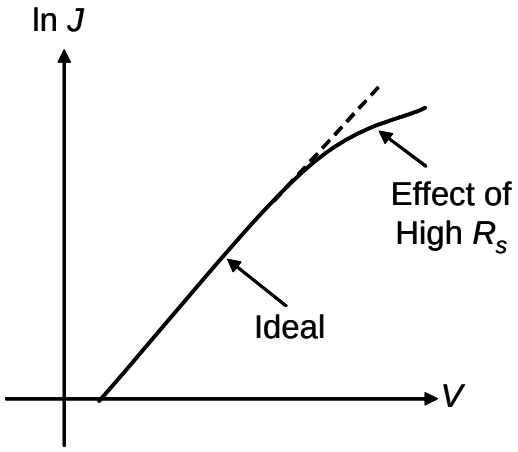


**Figure 2.8**: An example of plotting ln $J$ versus $V$ in the forward bias. The figure shows the effect of $R_s$ on the linear behaviour of the resulted curve. The dashed line represents the difference between the ideal and the deviated curves.

The last method (f) extracts $n$ directly from a single $J$-$V$ curve without the need for values of other parameters. Bayhan [12] has calculated $n$ by both this method and Lambert W-function, and the results extracted from both methods were in a very good agreement. For these reasons the slope method was chosen to determine $n$ values for CdTe solar cells in the analysis undertaken in Chapter 6.

This method (i.e. the slope method) was selected to determine the ideality factor in previous studies such as [13]. Some of the methods mentioned above and others are reviewed by Bashahu and Nkundabakura [14].

The slope method can be generalised for use with light $J$-$V$ data as follows: As a simplification, $J_L$ can be equalised to $J_{sc}$ [15]. Then as for the slope method in dark, $J_0$ and $n$ can be evaluated by plotting ln $(J+J_{sc})$ as a function of $V$ according to equation 2.9. However, in practice the slope method did not give acceptable results when it was used to analyse the light data, as will be discussed in Chapter 6.

## 2.5 Some models for the electrical transport mechanisms in p-n junctions and experimental methods of identifying the mechanism

### 2.5.1 Introduction

The electrical current in the p-n junction is due to the flow of the minority carriers on each side of the junction. It was mentioned in Section 2.4 that the ideal case for which Shockley equation is valid is when the current is governed by diffusion i.e. $n = 1$. However, in some cases, recombination of the carriers contribute to the current, which affects the value of the ideality factor i.e. $1 < n < 2$.

The recombination current is defined as the current originating from the flow of carriers (both electrons and holes) that recombine in the depletion region [16]. Therefore, recombination may be considered to contribute to the current transport in the p-n junction. This process may happen via direct recombination (i.e. band-to-band) or indirect recombination (i.e. when the localised states within the band gap participate in the process) [5].

Besides the processes mentioned above, there are a number of transport processes describing the flow of current though both the bulk and the junction of the p-n junction, which are collectively referred to as *electrical transport mechanisms*. Only mechanisms which were observed in this work will be described in detail in the following sections.

In order to determine the electrical transport mechanisms operating in semiconductor junctions by experiment, a family of *J-V* curves should be recorded at different temperatures i.e. *J-V-T*. The method is to investigate the behaviour of the slope of the *J-V* curves, the saturation current and the ideality factor as functions of *T*, and then diagnose the carrier flow mechanisms [8, 17-21]. Details follow in the descriptions of current transport mechanisms that follow.

Further to this, a novel method of determining the ideality factor (and therefore the transport mechanism) from light *J-V* data is presented in Section 2.5.4. It has the feature that the absolute intensity of the incident light need not to be known, allowing the method to be applied easily in the laboratory using filters.

### 2.5.2 Multi-step tunnelling

This model has been proposed by Riben and Feucht in 1966 [22]. It was developed from a transport model describing direct carrier tunnelling (i.e. band to band) combined with recombination for the n-Ge/p-GaAs heterojunction [23]. Traps were assumed to be uniformly distributed in the energy gap through which carriers tunnel prior to recombination.

In this model electrons tunnel from the conduction band of the n-side (in a p-n junction) to the close localised states in the energy gap. Next, electrons continue tunnelling in a staircase path among the states where they recombine with holes eventually. A schematic diagram of this mechanism across a p-n junction is illustrated in Figure 2.9.

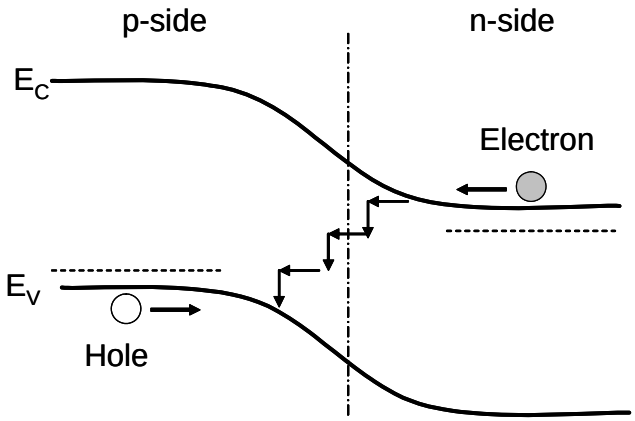


**Figure 2.9**: A schematic diagram of a p-n junction demonstrating carrier paths which are proposed in the multi-step tunnelling model, where $E_c$ and $E_v$ are the conduction and the valence bands respectively.

a) *Forward bias behaviour*

If the electrical transport mechanism is governed by this model in the p-n junction, then its forward current $J_f$ is expressed as [17, 24]:

$$J_f = J_0(T)\exp(AV) \tag{2.20}$$

with

$$J_0 = J_{00}\exp(BT) \tag{2.21}$$

where $A$ is the slope of ln$J$ versus $V$, $J_0$ is the saturation current, $V$ is the applied voltage and $B$ and $J_{00}$ are constants. The behaviour of $A$ as a function of $T$ may be used to identify situations in which the multi-step tunnelling mechanism is operating: Typically $A$ is independent of $T$ [6]. However, in practice, the experimental values of $A$ were reported to vary slightly with $T$ [24-26]. The characteristic behaviours of both $A$ as well as that of $J_0$ (as equation 2.21 implies) with $T$ were used to evidence that some samples in Chapter 6 obeyed this model.

Another use of $A$ is that it can be used to determine the number of tunnelling steps ($R$) required for carriers to pass the depletion region by using the following equation [27]:

$$A = \alpha R^{-1/2} K \tag{2.22}$$

where,

$$\alpha = (\frac{\pi}{4\hbar})(\frac{m_n \varepsilon_p}{N_A})^{1/2}, \tag{2.23}$$

$$K = 1 + (\frac{\varepsilon_p N_A}{\varepsilon_n N_D}), \tag{2.24}$$

where $m_n$ is the electron effective mass, $\varepsilon_n$ and $\varepsilon_p$ are the dielectric constants of the n- and the p-side of the junction respectively and $N_A$ and $N_D$ are the doping concentration of acceptors and donors respectively.

b) *Reverse bias behaviour*

The reverse current depends on the applied voltage according to the equation [24],

$$\ln\frac{J_r}{V} = -\beta(E_g + \Delta E_v)\sqrt{\frac{E_r}{V_{bi} - V}} \qquad (2.25)$$

where $J_r$ is the reverse current density, $V$ is the applied voltage, $V_{bi}$ is the built-in potential, $E_g$ is band gap, $\Delta E_v$ is the valence band offset, $E_r$ is the barrier height for one tunnelling step and $\beta$ the number of steps required for tunnelling under reverse bias conditions. The trap density required for tunnelling ($N_t$) can be calculated from the equation [28]

$$\frac{J_r}{V}\exp(\gamma[V_{bi} - V]^{-1/2}) = aq^2\frac{N_t}{h} \qquad (2.26)$$

Where $\gamma$ is a constant, $a$ is the lattice constant, $h$ is Planck's constant. Equation 2.26 can be rearranged as

$$\ln\frac{J_r}{V} = \ln\left(aq^2\frac{N_t}{h}\right) - \gamma[V_{bi} - V]^{-1/2} \qquad (2.27)$$

This equation implies that when multi-step tunnelling process dominates the reverse current, plotting ln $(J_r/V)$ against $(V_d - V)^{-1/2}$ should give a straight line with a negative slope. The intercept of this line can be used to extract $N_t$.

In general, the power dependence of $J_r$ on $V$ is evaluated by measuring $m$ from the equation

$$J_r \alpha V^m \qquad (2.28)$$

The value of $m$ is determined from ln$J$ vs. ln$V$ plot. It has been reported that $m$ decreases as $T$ increases when the $J_r$ flow obeys multi-step tunnelling model in both CdTe/CdS and CdTe/ITO solar cells [28, 29]. When observed, this behaviour is

therefore an evidence that multi-step tunnelling process is dominant for reverse current.

### 2.5.3 Shockley-Read-Hall recombination (SRH)

This model describes recombination which takes place via the localized levels (i.e. recombination centres) within the energy band gap rather than band-to-band recombination. It was proposed and discussed by Shockley and Read [30] and also by Hall [31]. SRH is a non-radiative recombination process.

The recombination centres capture carriers from both the conduction and the valence bands. There are two possibilities for a trapped carrier: a) it gains sufficient energy by thermal activation and, as a result, releases itself, or b) the trap captures another carrier with opposite polarity, then these two carriers recombine in the trap which therefore becomes empty.

For a single trap there are four possible processes (for an acceptor type trap i.e. the trap is neutral when it does not contain an electron) as shown in Figure 2.10:

i) Capture of an electron from the conduction band to the trap (Figure 2.10a),

ii) Emission of an electron from the trap to the conduction band (Figure 2.10b),

iii) Capture of a hole from the valence band to the trap that contain an electron i.e. emission of an electron from the trap to the valence band (Figure 2.10c),

iv) Emission of a hole from a trap (neutral) to the valence i.e. capture of an electron from the valence band to the trap (Figure 2.10d).

This model is well known and has been discussed in detail in many text books such as [2, 7, 32].

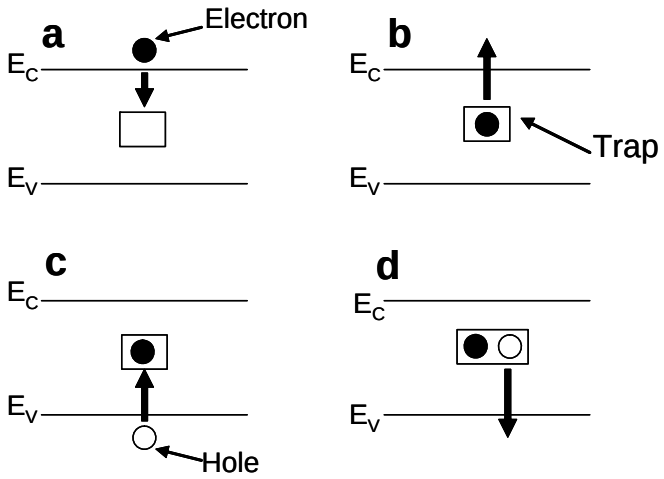


**Figure 2.10**: The four possible processes for recombination described by SRH model for a single trap. a) electron capture, b) electron emission, c) hole capture and d) hole emission.

Sze [2] and Mitchell *et al.* [33] reported that for recombination dominated current transport the value of the diode factor (*n*) characteristically is 2. This value of *n* occurs when carriers recombine via traps localised near the middle of the band gap (i.e. trap energy ~ $E_g/2$), for which the recombination probability is maximum (see Appendix B for more details). For this case, the current can be described by equation 2.8

$$J = J_0[\exp(\frac{qV}{nkT}) - 1] \qquad (2.8)$$

where

$$J_0 = J_{00}\exp(-\frac{\Delta E}{nkT}) \qquad (2.29)$$

and $J_{00}$ is a constant and $\Delta E$ is the activation energy, which is related to the built-in potential $V_{bi}$ by the equation

$$n\Delta E = V_{bi} \qquad (2.30)$$

Finally it should be mentioned that the diode ideality factor $n$ is invoked in the description of a diode in which recombination may be important (Appendix B). However, in the literature it is common to see numerical values of $n$, and for example their temperature dependence, used as a fingerprint for identifying alternative current transport mechanisms. This is done even though the physical basis of equation 2.8 is not really appropriate to the mechanisms involved (e.g. as for multi-step tunnelling). This approach is nevertheless used in this thesis and the reader is reminded of the limits of the physical appropriateness of the use of $n$.

### 2.5.4 Experimental determination of the recombination mechanism from illuminated *J-V* data

The recombination mechanisms may be identified from the characteristic *J-V-T* behaviour expected for SRH, Auger and radiative recombination dominated transport. For example multi-step tunnelling conforms to equation 2.20 (under forward bias) and $A$ is independent of $T$, as discussed in Section 2.5.2. In addition, the value of the diode factor $n$ is an indicator of the mechanism. For the case of illuminated diodes, $n$ may be evaluated by examining the behaviour of $V_{oc}(T)$ as follows:-

$$V_{oc} = \frac{nkT}{q}\ln\left(\frac{J_{sc}}{J_0}+1\right) \qquad (2.31)$$

where $J_{sc}$ was substituted by $J_L$ in equation 2.31 as an approximation [15] (see Section 2.6 for further discussion of this equation). $J_{sc}$ is linearly proportional to the light intensity [7], and then it can be written

$$V'_{oc} = \frac{nkT}{q}\ln\left(\frac{XJ_{sc}}{J_0}+1\right) \qquad (2.32)$$

where $X$ is the light intensity and $V'_{oc}$ is the open-circuit voltage corresponding to this light intensity. Since $J_{sc} >> J_0$, equation 2.32 can be rearranged to be

$$V'_{oc} = \frac{nkT}{q}\left(\ln\frac{J_{sc}}{J_0} + \ln X\right) \qquad (2.33)$$

Or by using equation 2.31

$$V'_{oc} = V_{oc} + \frac{nkT}{q}\ln X \qquad (2.34)$$

This analysis suggests an alternative methodology using a variable light intensity that has been devised and used in this work: It is assumed that measurements are taken under for example two intensities *aX* and *bX*, where the intensity ratio is known from the neutral density filters used in experiment, and the absolute intensity of the source (*X*) is constant. From this:-

$$V_{oc}(a) = V_{oc} + \frac{nkT}{q}\ln aX \qquad (2.35)$$

and

$$V_{oc}(b) = V_{oc} + \frac{nkT}{q}\ln bX \qquad (2.36)$$

By subtracting equations 2.36 from 2.35:

$$V_{oc}(a) - V_{oc}(b) = \frac{nkT}{q}\ln(\frac{aX}{bX}) \qquad (2.37)$$

$$V_{oc}(a) - V_{oc}(b) = \frac{nkT}{q}\ln(\frac{a}{b}) \qquad (2.38)$$

Equation 2.38 therefore eliminates the absolute intensity of the incident light.

$V_{oc}$ varies as $\frac{2kT}{q}\ln X$, $\frac{kT}{q}\ln X$ and $\frac{2kT}{3q}\ln X$ for Shockley-Read-Hall (SRH), radiative and Auger processes respectively [7], where k is Boltzmann constant, T is temperature, q is electronic charge and X is the absolute intensity of the light source.

Therefore, using equation 2.38, the ideality factor can be determined from the slope of the line resulting from the plot of $V_{oc}(a) - V_{oc}(b)$ against $T\ln\left(\frac{a}{b}\right)$. According to the discussion above, if n = 2, 1 or 2/3 then the dominant process is SRH, radiative or Auger respectively. Table 2.1 summarises the equations describing the relation between $J$ and $V$ for seven different transport mechanisms. In addition, it shows the characteristics of each mechanism by which it may be identified. A review of experimental observations of transport in CdTe/CdS solar cells is given in Chapter 3.

| **Current transport mechanism** | **Equation** | **Diagnostic** |
|---|---|---|
| Diffusion (no recombination) | $J = J_0[\exp(\frac{qV}{nkT}) - 1]$<br>$J_0$ is the saturation current | $n$ =1<br>$\ln J_0 \propto -1/T$ |
| Recombination in depletion region | $J = J_0[\exp(\frac{qV}{nkT}) - 1]$,<br>$J_0 = J_{00}\exp(-\frac{\Delta E}{nkT})$ | $n$ =2<br>$n\Delta E = V_{bi}$<br>$\ln J_0 \propto -1/T$ |
| Multi-step tunnelling (forward bias) | $J_f = J_0(T)\exp(AV)$,<br>$J_0 = J_{00}\exp(BT)$<br>(see note on $n$ below)* | $n \downarrow as\ T \uparrow$<br>$A$ independent of $T$<br>$\ln J_0 \propto T$ |
| Multi-step tunnelling (reverse bias) | $\ln\frac{J_r}{V} = -\beta(E_g + \Delta E_v)\sqrt{\frac{E_r}{V_{bi} - V}}$<br>$J_r \alpha V^m$ | $ln(J_r/V) \propto -(V_d - V)^{-1/2}$<br>$m \downarrow as\ T \uparrow$ |
| SRH recombination | $V_{oc}(a) - V_{oc}(b) = \frac{nkT}{q}\ln(\frac{a}{b})$ | $n$ =2 |
| Auger recombination | $V_{oc}(a) - V_{oc}(b) = \frac{nkT}{q}\ln(\frac{a}{b})$ | $n$ =2/3 |
| Radiative recombination | $V_{oc}(a) - V_{oc}(b) = \frac{nkT}{q}\ln(\frac{a}{b})$ | $n$ =1 |

**Table 2.1**: Current transport mechanisms considered in this work. The table shows a) the equations describing each mechanism, and b) the diagnostic characteristics used to identify the transport mechanism. See text above for the meaning of the symbols shown. The reader is reminded that while the diode factor $n$ is used as a fingerprint for current transport mechanisms, it has a particular physical meaning as explained in Section 2.5.3 and Appendix B. * e.g. $n$ does not describe multi-step tunnelling physics, but its behaviour with $T$ is nevertheless used as a diagnostic tool.

## 2.6 *J-V* characteristics and parameters of solar cells

Solar cell performance is typically tested by applying an external voltage across the cell and measuring the current passing though it i.e. the *J-V* characteristics. This test can be carried out in dark or under illumination to extract important data by which the performance of the cell is evaluated. Equations 2.8 and 2.9 predict the dark and the light *J-V* characteristics respectively for the p-n junction solar cell, and they are illustrated in Figure 2.11. Ideally, the light curve should be identical to the dark one except that it is shifted downward by an amount equals to $J_L$. This condition is called *the superposition principle*.

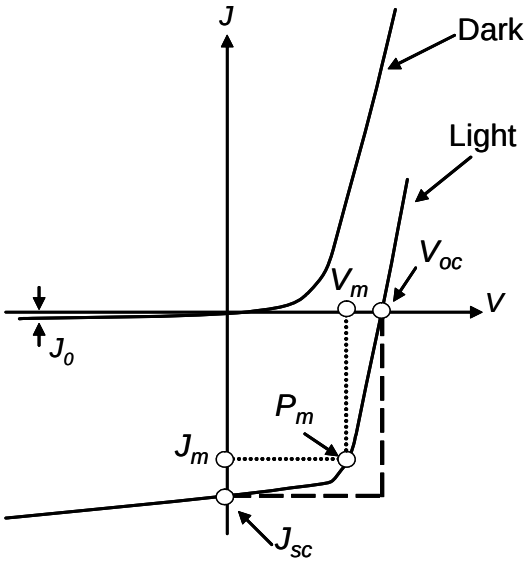


**Figure 2.11**: The dark and light *J-V* curves for the ideal solar cell.

There are four basic parameters to test the performance of the cells. Firstly, the *open circuit voltage,* $V_{oc}$, which is defined as the voltage between the cell terminals (contacts) when they are isolated i.e. the voltage when no current flows in the external circuit. Applying this definition to equation 2.9, $V_{oc}$ is expressed as mentioned in equation 2.31 (Section 2.5.4) as

$$V_{oc} = \frac{nkT}{q}\ln\left(\frac{J_L}{J_0}+1\right) \qquad (2.31)$$

Figure 2.11 shows that $V_{oc}$ is determined from the intercept of the light *J-V* curve with the voltage axis (i.e. when $J = 0$).

$V_{oc}$ is related to $V_{bi}$ according to the equation, [34]:

$$V_{oc} = \frac{nkT}{q}\ln\left(\frac{J_{sc}}{J_{00}}\right) + V_{bi} \qquad (2.39)$$

The built-in potential $V_{bi}$ of the main junction, therefore, can be evaluated by plotting $V_{oc}$ versus $T$: Equation 2.39 implies that plotting $V_{oc}$ against $T$ should give a straight line, which its intercept with the $V_{oc}$ axis (at $T = 0$) gives the built-in potential $V_{bi}$.

The current density of the illuminated cell with directly connected terminals (no external voltage is applied) is called the *short circuit current density* $J_{sc}$, which is the second basic parameter for solar cells. It is the intercept of the light *J-V* curve with the current density axis as shown in Figure 2.11. Usually in calculations, this value substitutes the light-generated current $J_L$ as a valid approximation [15].

The third parameter is called the *fill factor, FF*. It measures the coincidence of the maximum power point $P_m$ with the value of multiplying $V_{oc}$ by $J_{sc}$.

$$FF = \frac{P_m}{V_{oc}J_{sc}} = \frac{V_m J_m}{V_{oc}J_{sc}} \qquad (2.40)$$

where $V_m$ and $J_m$ are the voltage and the current density corresponding to $P_m$. From Figure 2.11, *FF* can be expressed as the ratio between the rectangle defined by the dotted lines and the rectangle defined by the dashed lines. The maximum value of the *FF* is 100 % which means that the *J-V* curve is a perfect rectangular at the fourth quarter of the *J-V* plot.

The last parameter is the conversion efficiency (usually called efficiency), $\eta$. It evaluates the ratio between the maximum power generated by the cell to the power of the incident light $P_s$. AM1.5 spectrum (which results in $P_s$ = 1000 W/m$^2$) is the typical spectrum under which $\eta$ is measured. Therefore, the efficiency is expressed as

$$\eta = \frac{P_m}{P_s} = \frac{V_{oc}J_{sc}FF}{P_s} \qquad (2.41)$$

## 2.7 Quantum efficiency

The quantum efficiency (QE) of a solar cell is defined as the ratio of the collected light-generated carriers to the number of incident light photons [35]. It therefore measures the probability of generating an electron–hole pair from each incident photon [7]. There are two kinds of QE: a) external quantum efficiency (EQE) which is the ratio of the collected photocurrent to the total incident light [35], and b) internal quantum efficiency (IQE), which is the same as EQE except that only the absorbed light is considered (i.e. losses in light such as reflection and transmission are not considered in the measurements) [35].

Each layer of the cell contributes to the results of the EQE. For example, Figure 2.12a shows the ideal EQE response for a CdTe/CdS cell. The square shape of the EQE curve (as shown in Figure 2.12a) is obtained if both the CdS and the CdTe are thick enough and if the junction is located in the right position i.e. at the interface between these two materials. Photons with energy > CdS $E_g$ are absorbed in the CdS layer, yet they do not contribute to the photocurrent. The loss in carriers generated in CdS may be due to a) higher conductivity of CdS compared to that of CdTe, which creates a one-sided junction i.e. the depletion region of the heterojunction is approximated to be created entirely in the CdTe layer. This may result in inability of separating the carriers, and b) the very short diffusion lengths of the carriers in CdS, which enhances recombination and therefore losing the carriers. Similarly, photons with energy < CdTe $E_g$ will not be absorbed by either CdS or CdTe, and hence they do not generate carriers. Only photons having energies < CdS $E_g$ and > CdTe $E_g$ can generate current and hence contribute to the EQE signal.

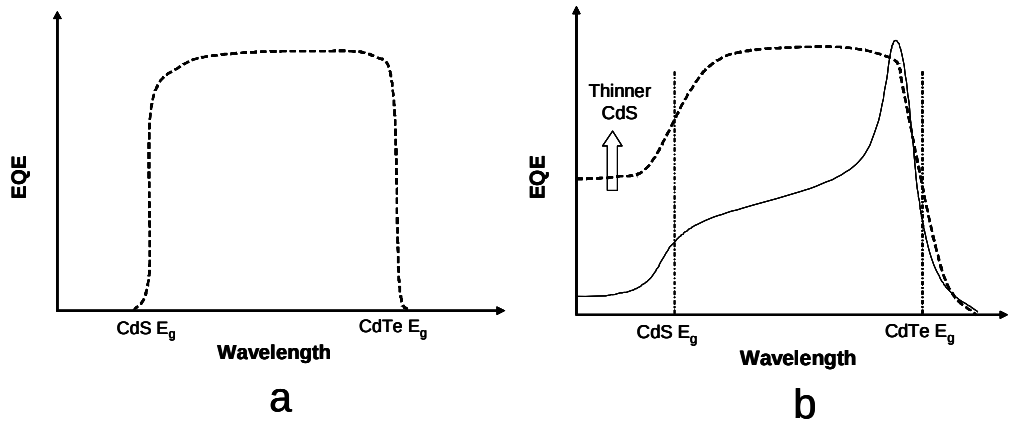


**Figure 2.12**: a) a schematic diagram of an idealised EQE curve for CdTe/CdS cells. b) the dashed line shows the typical EQE for the CdTe/CdS cells whereas the solid line shows the EQE of a buried junction.

It is seen in Figure 2.12b that if the CdS is thin enough, it partially allows photons with energy > CdS $E_g$ to pass though it, as thin CdS is not capable of absorbing all of them. Those photons are then absorbed in the CdTe, and therefore generate current. This behaviour will raise the EQE curve near the CdS cut-off, as seen in Figure 2.12b. In the case of having a buried homojunction (i.e. a homojunction within the bulk of the CdTe), the EQE will have the shape shown by the solid line in Figure 2.12b. The loss in current in this case (in the short wavelength region) is due to the generation of the carriers in regions near the CdTe/CdS interface which is away from the buried homojunction i.e. the electric field of the buried homojunction is incapable of separating carriers generated near the CdTe/CdS interface by photons having short wavelength. There is therefore no sweeping of the carriers to the external circuit [36].

## 2.8 Losses in the conversion efficiency

The conversion efficiency for solar cells depends on several factors, for example, high ambient temperature has a deleterious effect on the performance of solar cells. Increasing the temperature would increase $J_0$ exponentially. This results in a considerable decrease in both $V_{oc}$ and $FF$ [6]. Therefore, the efficiency of the cell is significantly reduced as temperature increases.

Additionally, the intrinsic properties of the materials used to fabricate solar cells can create more losses. Two of these properties are discussed briefly below.

*Losses due to the band gap*

Since the energy conversion for solar cells relies on light absorption, the band gap of the absorber layer in the cells has a crucial effect on the efficiency. Low $E_g$ allows more photons to be absorbed from light spectrum. However, the maximum possible value of $V_{oc}$ cannot exceed $E_g$ of the absorber layer. Lower value of the band gap would produce higher current but lower voltage. In contrast, using a semiconductor with relatively high $E_g$ would result in generating high voltage but low current. It is a trade off between $V_{oc}$ and $J_{sc}$ in order to generate the maximum available power. The maximum theoretical value of the efficiency was calculated as a function of $E_g$ as illustrated in Figure 2.13 [7]. The highest possible power that would be generated using solar cells requires a material with $E_g$ ~ 1.5 eV. This value is close to the band gap of the CdTe as shown in the same figure.

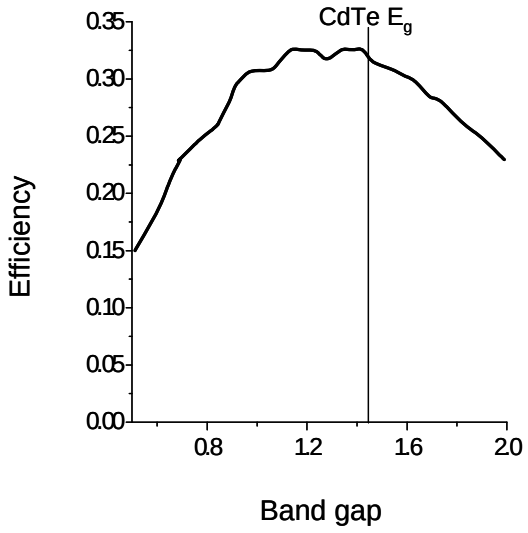


**Figure 2.13**: The theoretical conversion efficiency of single-junction solar cells as a function of the band gap $E_g$.

*Parasitic resistances*

The two resistances mentioned in Section 2.3 ($R_s$ and $R_{sh}$) are called the parasitic resistances as they affect the performance of the solar cell. $R_s$ is a common issue for solar cells and its effect is shown in Figure 2.8. Both resistances, $R_s$ and $R_{sh}$, can significantly influence the efficiency of the cells. As seen in Figure 2.14a and

Figure 2.14b, the parasitic resistances change the *J-V* curves of illuminated cells. The obvious effect of them (from the figure) is the reduction of *FF*, and therefore the efficiency. However, high $R_s$ and low $R_{sh}$ may also reduce $J_{sc}$ and $V_{oc}$, respectively [7]. It is worth mentioning again that the ideal case for solar cells is to have $R_s = 0$ and $R_{sh} = \infty$.

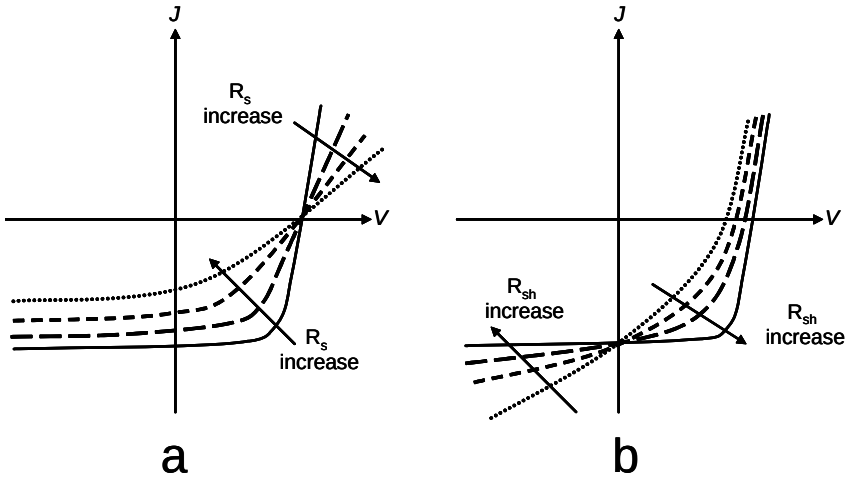


**Figure 2.14**: The effect of $R_s$ and $R_{sh}$ on the illuminated *J-V* curves of solar cells are shown in figures a and b respectively.

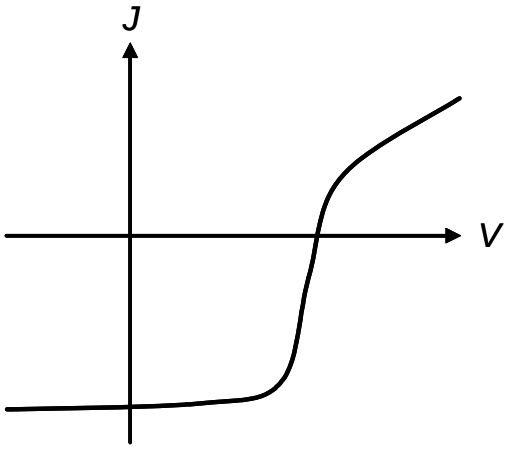


**Figure 2.15**: *J-V* characteristics showing the roll-over effect at high forward bias.

For the CdTe solar cells there is a further effect influencing the shape of *J-V* curves that arises from the contact to the CdTe itself. Contacting to CdTe is discussed more fully in Section 3.7. It is a particular problem since the contacts are invariably

associated with a Schottky barrier in opposition to that of the main junction. This combination of opposing diodes sometime gives rise to the *J-V* shape shown in Figure 2.15, and is known as “roll-over”. A characteristic of this is that at high forward biases the current is limited by the back contact barrier.

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# Chapter 3: Review of Interfaces, Processing and Transport in CdTe/CdS Solar Cells

## 3.1 Introduction

Almost all CdTe/CdS–based solar cells have the so called "superstrate" configuration shown in Figure 3.1. In this arrangement, the light is incident on a glass sheet, and the layer stack is deposited on its reverse side. Firstly a transparent conductive oxide (TCO) is deposited, and this acts as an n-type conductive contact for the n-CdS of the p-CdTe/CdS junction. Typically the TCO is $SnO_2$, ZnO or ITO, or a multi-layer stack composed of these materials. The CdS is usually known as the "window layer" since light transmitted by it is absorbed by the "absorber", i.e. the CdTe itself. There is a well known loss in CdTe/CdS cells arising from the fact that blue (and shorter wavelength) light absorbed by the CdS does not generate photo-carriers (see Section 2.7 for more details). Most absorption takes place in the CdTe, which is highly absorbing (absorption coefficient $\alpha \sim 10^5$ $cm^{-1}$ at the band edge). The uppermost part of the structure in the diagram (i.e. the dark side) is the contact to the CdTe. It is technologically more convenient that the contact is the last layer to be deposited and hence this can be done at low temperatures so as to afford some control over diffusion of impurities.

The role and the required properties for each layer differ from one layer to another. These properties can be altered by both the growth and processing conditions. For example, the TCO layer is required to have a resistivity < 10 Ω/□ and transparency > 80 % for visible light. The CdS film is preferred to be as thin as possible but also pinhole free. These requirements may allow light to pass though both the TCO and CdS layers, and therefore be absorbed in the CdTe layer. Both the intrinsic properties of the layers (e.g. morphology) and the processing procedure (e.g. annealing) may affect these layers significantly, and hence affect the performance of the subsequent full device. This Chapter reviews the main features of these layers along with the possible changes that occur to them during the fabrication and processing, which may affect the performance of the cell. Section 3.2 reviews the interface between the TCO and the window layers, and the effects that the TCO may introduce on both the interface and the window layer itself. Treatment conditions for

the CdS (e.g. temperature and ambient) affect not only CdS but also the PV performance for completed devices, as discussed in Section 3.3. The application, role and optimisation of the activation step of CdTe cells (i.e. $CdCl_2$ treatment) are reviewed in Section 3.4. Such a treatment may not only improve the PV performance of the cells but also enhance the intermixing between CdTe and CdS as reviewed in Section 3.5. The current transport mechanisms in the CdTe solar cell junction may vary depending on several factors such as the post-growth treatment and the ambient temperature. This is reviewed in Section 3.6. The difficulty of forming a low resistance back contact to CdTe cells represents a major limitation of the performance. The barrier height of the Schottky contact that may be created between CdTe and the back contact depends on both the electronic properties of the contact material and the processing of the CdTe back surface prior metallization. Both the materials and processes used to contact CdTe cells are described in Section 3.7.

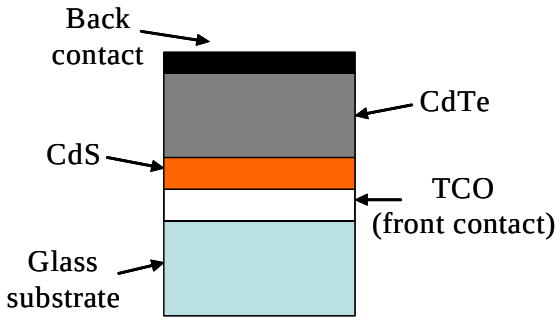


**Figure 3.1**: The typical structure of the CdTe/CdS solar cell.

## 3.2 CdS/TCO layers and junction properties

The CdS/TCO interface plays an important role in the performance of solar cells. Although the main purpose of the TCO is to serve as an electrode it can significantly affect both the growth of the CdS window layer, and the effects of device processing (as described below). Chemical and thermal stabilities are essential requirements for this layer. Ideally the CdS/TCO junction should also be Ohmic.

Fritsche *et al.* [1] used XPS to study different cleaning procedures of the $SnO_2$/ITO/glass bi-layer substrates and their influences on the properties of the CdS window layer. It was found that treating the TCO changed its electronic properties. For example, the work function for the as-grown film (measured at $SnO_2$ surface) was

4.1 eV but it increased to 4.35 eV after rinsing the films in isopropanol, and to 5 eV by heating at 400°C in vacuum. This behaviour was attributed to hydroxide species and carbon contamination. The treatment of the TCO changed not only the electronic properties, but also the subsequent growth of the CdS: the heat treated substrates encouraged more complete CdS coverage compared with the other samples.

The dependence of the behaviour of CdS grown on ITO of various thicknesses has been studied by Romeo *et al.* [2]. For CdS films that had been grown on 0.5 μm thick ITO, and then $CdCl_2$ treated, the CdS grain size was 0.2 – 0.3 μm. However, for CdS films grown on 1.8 – 2 μm thick ITO, the grain size was 0.05 μm, and was invariant on the $CdCl_2$ treatment i.e. the grain size of CdS grown on relatively thick ITO (1.8 – 2 μm thick) remained the same before and after the $CdCl_2$ treatment. The authors interpreted this as being due to an additional factor: sodium was postulated to enhance CdS grain growth, and the thicker ITO prevented such growth by blocking diffusion of sodium from the glass substrates. Moreover, the electrical performance of the cells was found to be influenced by the ITO thickness: fill factor was found to vary strongly, whereas $V_{oc}$ and $J_{sc}$ did not show a significant variation. Surprisingly, the roll-over effect (see Section 2.8) was reliant on the thickness of the ITO. Again, this effect was speculated to be due to sodium diffusion from the glass through the CdS then into the CdTe. Na is an acceptor dopant in CdTe. Therefore, the existence of Na near the CdTe/CdS junction may dope the CdTe in that region and, as a result, create a p/p+ junction in the CdTe bulk. This presence of Na was verified by Emziane *et al.* by comparing CdTe/CdS devices fabricated on both glass [3] and sapphire [4] substrates in Romeo's lab. The composition in both structures was probed by SIMS for a) as-grown, and b) $CdCl_2$ treated devices in order to explore the origin of the impurities. The Na profile was found to be $10^{15}$ $cm^{-3}$ and $10^{17}$ $cm^{-3}$ for as-grown and processed glass-based cells respectively. On the other hand, for cells grown on sapphire substrates it was $6 \times 10^{13}$ $cm^{-3}$ for unprocessed devices and increased to be $4 \times 10^{16}$ $cm^{-3}$ after processing. It can be confirmed, therefore, that although Na contamination was introduced by the $CdCl_2$ treatment, it was also originated from the glass substrate. An alternative explanation for the influence of increasing the ITO thickness on both *FF* and roll-over is that this will reduce the series resistance of devices. This will have a direct effect on *FF*. Although roll-over is considered to be a feature of the contact to the CdTe, it is nevertheless influenced by all of the collective equivalent circuit elements in the cell.

Wu *et al.* [5] investigated the benefits of introducing a buffer layer of $Zn_2SnO_4$ (ZTO) between the CdS and two different TCOs, $SnO_2$ and $Cd_2ZnO_4$ (CTO). It was found that ZTO improved the performance significantly. The efficiencies for CdTe/CdS/$SnO_2$ and CdTe/CdS/CTO cells were 13.5 % and 14 %, respectively. However, they were improved to 14.8 % and 15.8 % for CdTe/CdS/ZTO/$SnO_2$ and CdTe/CdS/ZTO/CTO devices respectively. The cells were examined by X-ray photoelectron spectroscopy (XPS) and secondary-ion mass spectroscopy (SIMS), showing that ZTO intermixed with the CdS film at annealing temperature of 550-650°C in Ar atmosphere. However, intermixing occurred at 400-420°C when $CdCl_2$ was introduced. The interdiffusion between the CdS and the ZTO may lead to several beneficial effects:

a) Intermixing between the CdS and both the ZTO and CdTe reduced the thickness of the CdS widow layer. This improves the quantum efficiency at short wavelengths as the absorption of the CdS is reduced. By this method, thinning the CdS layer was achieved without creating pinholes, and therefore, without decreasing $V_{oc}$ and $FF$.

b) The diffusion of Zn into the CdS film increases its band gap, allowing more photons to pass though to the absorber layer, and hence, generate more carriers.

c) ZTO improves the adhesion of the films to the substrate even after a severe $CdCl_2$ treatment. In [5] ninety eight CdTe/CdS samples with different substrates (i.e. with and without ZTO) were annealed subsequent to dipping in a 100 % saturated $CdCl_2$ solution. The adhesion was improved from only 7 % for cells without ZTO to 90 % and 95 % for ZTO/$SnO_2$ and ZTO/CTO based cells, respectively. This finding may facilitate the optimization of the $CdCl_2$ treatment for solar cells.

Alamri and Brinkman [6] tested the effect of the CdS post-growth annealing on the electrical properties of both CdS/$SnO_2$ and CdS/ITO bi-layers. The work was prompted by the disparity in the performance of cells which were grown on $SnO_2$ and ITO substrates, but which were otherwise identical. Their efficiencies were 10.1 % ($SnO_2$ substrate) and 4.6 % (ITO substrate). Furthermore, the roll-over effect was more severe for the samples grown on ITO. It was assumed that the poor performance of the cells based on ITO was due to the TCO since the back contact was the same for all devices. In order to test this hypothesis, CdS films were grown on both kinds of TCOs then annealed in air for 30 minutes at 400°C after which the CdS was contacted with In and the *I-V* curves measured. While that for the In/CdS/$SnO_2$ sample was Ohmic, the In/CdS/ITO was rectifying. The effect was further investigated by

annealing CdS/ITO samples for 10, 20 and 30 minutes in air. The CdS/ITO interface became fully rectifying after annealing for 20 minutes. This behaviour was attributed to the change of the work function of the buried ITO due to oxidation during annealing the samples in air.

Figure 3.2 (which was drawn by the author using Anderson's rule, see Section 2.1) shows changes occurring in the junction before (a) and after (b) increasing the work function of the ITO (as Alamri and Brinkman speculated). These diagrams support the findings of ref [6]. However, the original paper does not consider the possibilities that the electrical changes are due to either a) In diffusion from the ITO into the CdTe, where it acts as an n-dopant or b) modifications of the CdS itself by the annealing. The latter is therefore explored in Chapter 5 of this thesis.

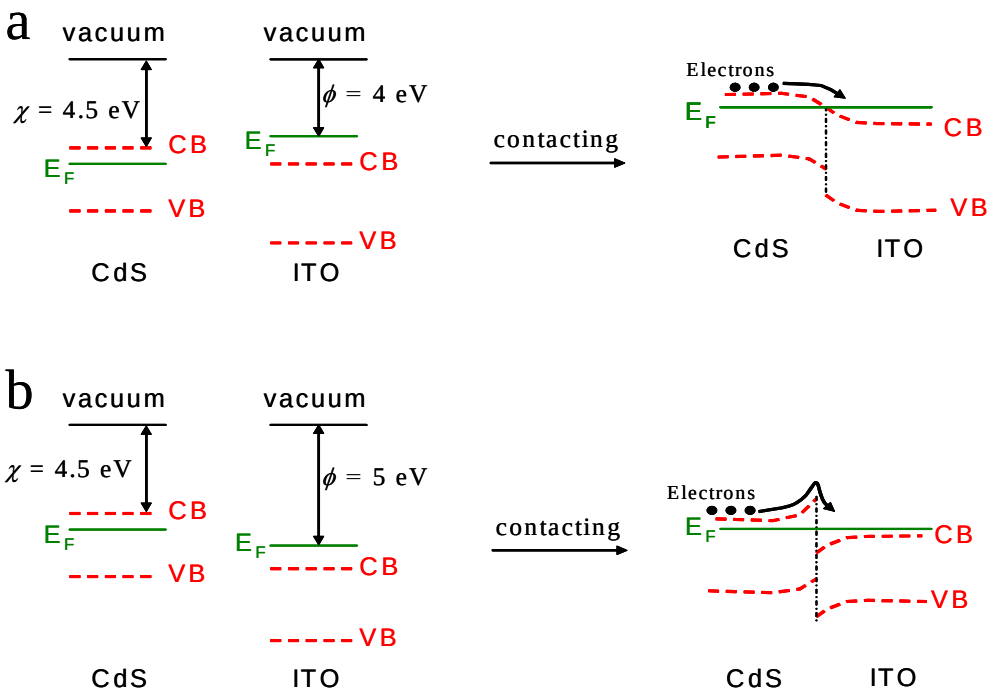


**Figure 3.2**: The change in the CdS/ITO junction as the ITO work function increases. The figure shows that electrons face no energy barrier (Ohmic junction) when the ITO work function was relatively small (a). However, they face a barrier (rectifying junction) at the interface in the case that the ITO work function increases (b). The values of both work function ($\phi$) and electron affinity ($\chi$) were taken from [6].

## 3.3 CdS annealing (changes in both CdS itself and the performance of the cell)

Annealing polycrystalline CdS films may result in significant changes in the properties of the material itself. Goto *et al.* [7] used the photoluminescence (PL) technique to study the defects in CdS films deposited chemically on $In_2O_3$ coated glass substrates. The samples were annealed in either $N_2$, $O_2$ or air at 200-500°C. The defect concentration was increased by increasing the annealing temperature in the $N_2$ ambient. This result was attributed to sulphur evaporation from the film. On the other hand, there was a significant reduction in the defects for samples annealed in $O_2$. Since oxygen and sulphur are from the same group, oxygen was assumed to compensate sulphur deficiency. The existence of oxygen in these samples was confirmed by AES. However, for the air-annealed CdS the defect reduction was less significant than in the case of $O_2$-annealed samples. A lower concentration of oxygen was observed (by AES) in the air-annealed samples in comparison to $O_2$-annealed ones. Thus, Goto *et al.* recommended annealing the CdS in $O_2$ ambient in order to reduce the defects in the CdS, and therefore improve the performance of the CdS based solar cells.

The optical properties of CdS may also be affected by thermal treatment. Metin and Esen [8] grew CBD-CdS on commercial glass slides and then annealed them in a $N_2$ atmosphere for one hour in the temperature range 100 - 600°C. XRD results showed that the structure of the films became more hexagonal after annealing. The optical band gap of the CdS was decreased from 2.42 eV to 1.9 eV, which may occur from the reorganization of the material for example by sulphur evaporation or film oxidation. Although the annealing took place in a $N_2$ ambient, it was speculated that water confined within the CdS film caused oxidation. Trapped water from the CBD process may also create pores in the film.

Similarly, the electrical properties of the CdS can be modified by annealing. Zinoviev and Zelaya-Angel [9] reported changes in the resistivity of the CdS films when they were thermally treated in $H_2$, $H_2$ + In, $H_2$ + Cd and Ar ambients. The In- and Cd-containing ambients were created by flowing $H_2$ though a tube which had either In or Cd (highly pure) held in a boat at a temperature maintained at 330 - 500°C. The high resistivity samples were measured by the two probe method whereas the low resistivity ones were measured by the four probe method, all the

measurements being undertaken at room temperature. The most pronounced change was observed in the CdS samples annealed in $H_2$ atmosphere: Over the range of annealing temperature 200-250°C, the resistivity decreased by more than eight orders of magnitude. However, when the temperature was increased to higher values (up to 300°C), the resistivity rapidly increased. The interpretation of this behaviour [9] is as follows: Annealing in $H_2$ passivates oxygen in the CdS grain boundaries, which was assumed to be the reason of reducing the resistivity. However, when the annealing temperature was further increased, the stiochiometry of the samples was changed which increased the resistivity again. The study shows that the S/Cd ratio – which was determined by EDX – was consistent with the values of the resistivity at high annealing temperatures. The effect of annealing in either Ar, $H_2$ + In or $H_2$ + Cd was not as pronounced as the effect of annealing in pure $H_2$. It was attributed to the faster reaction of the pure $H_2$ with the CdS to create $H_2S$. Hiie *et al.* [10] treated CBD-CdS grown on glass in $H_2$ ambient. It was observed that the values of the lateral resistivity (which was measured by the four point probe method) fluctuated with the annealing temperature. The resistivity decreased in the temperature range of 100-320°C but it increased for higher temperatures. The changes in the resistivity were assumed to be attributed to: a) the removal of the oxides, b) re-crystallisation (which was proved by XRD), and c) the contribution of the residual $CdCl_2$ in the CdS films. However, annealing introduced porous CdS as a result of the removal of the chlorides.

The effects of annealing the CdS on the performance of the CdTe/CdS cells were also investigated. Chu *et al.* [11] annealed the CdS in a $H_2$ atmosphere at 400°C for 20 minutes. This treatment removed 20-30 nm a thick layer from the CdS surface, leading to a clean surface prior to the growth of the CdTe. CdTe cells were fabricated using both a) treated CdS, and b) as-grown CdS. It was found that the electrical transport mechanism in the main junction for the treated-CdS based cells was controlled by thermally activated recombination even at low temperature (200 K). On the other hand, for the as-grown-CdS based cells, the carrier flow in the junction was controlled by recombination at $T > 300$ K, and it changed to tunnelling at $T < 300$ K. The authors performed capacitance-frequency (*C-F*) measurements on the devices, which showed a higher dependence of capacitance on frequency for the as-grown-CdS based cells compared to the treated-CdS based cells. This indicates that the interface states in the as-grown-CdS devices were more responsive to the ac signals.

Ferekides *et al.* [12] treated the CdS in either $H_2$, He or a mixture of both at temperatures in the range 300-450°C. The authors reported that $H_2$ ambient had the most pronounced effect on the CdS compared to either the pure He or the mixed ambients. Both the grain size and the band gap of the CdS were increased after $H_2$ treatment. Moreover, the depletion width of the CdTe/CdS junctions using the $H_2$ treated CdS was 3-4 times wider than the depletion width of the junctions using either as-grown CdS or He treated CdS. The ideality factor of the junction decreased as the annealing time increased (in $H_2$ ambient) i.e. the quality of the junction was improved by longer thermal treatment. However, a reduction in the $J_{sc}$ was noted for samples annealed for 30 minutes at 450°C. This was thought to be attributed to the loss in light transmission occurring from the reduction of the underlying $SnO_2$ layer. Based on the results above, the authors recommended annealing CdS in order to maintain the better PV performance.

CDB-CdS was annealed in $N_2$, Ar, a mixture of 20 % $H_2$/80 % $N_2$ and $CdCl_2$ in the study reported by Kim and Kim [13]. The authors tested the effect of the annealing on both a) the properties of the CdS films, and b) the performance of the cells. They annealed the CdS in 1 Torr of either pure $N_2$ or 20 % $H_2$/80 % $N_2$ for 10 minutes in 400°C as a first annealing step. The second step was annealing the same sample at 530°C in 20 Torr of Ar for 13 minutes to mimic the CdTe growth. The $CdCl_2$ treatment included annealing at 450°C for 20 and 50 minutes in $N_2$ ambient after applying the $CdCl_2$. The $H_2$ treatment did not change the morphology of the film even after the second annealing step (i.e. annealing at 530°C). However, annealing in pure $N_2$ at 400°C created pores at grain boundary triple junctions. This was interpreted by considering that the grain boundary triple junctions vaporize faster than the other parts of the CdS film as they have higher energy states. Although the gas mixture (20 % $H_2$/80 % $N_2$) created smoother surfaces, it also resulted in larger pores. This behaviour occurred from the relatively fast vaporisation of sulphur in the $H_2$ atmosphere. Large pores were also reported for the $CdCl_2$ treated CdS. Higher performance was observed for the cells with $H_2$ treated CdS compared to the cells with as-grown or $N_2$ treated CdS. The improvement in the $V_{oc}$ was attributed to the better adhesion between the CdS and the CdTe due to the smoothness of the $H_2$-treated CdS. $J_{sc}$ increase was attributed to thinning the CdS, which occurred due to the annealing in the $H_2$ ambient.

The $CdCl_2$ treatment was applied to CdS by Calixto *et al.* [14] in various ways to investigate its effect on the performance of CdTe/CdS cells. They grew bi-layers of CBD CdS, layer I being 120 nm and layer II 40 nm thick. There were four configurations: A) $CdCl_2$ was introduced on layer I (i.e. between layer I and layer II), B) $CdCl_2$ on both layer I and layer II, C) no $CdCl_2$ and D) $CdCl_2$ on layer II (i.e. no $CdCl_2$ between layer I and layer II). After each $CdCl_2$ deposition, the samples were annealed in air at 400°C for 30 minutes. The CdTe for all samples was also $CdCl_2$ treated by the same way, and the thickness of $CdCl_2$ for all cases was 200 nm. The efficiencies of the cells A, B, C and D were 4.05 %, 0.6 %, 2.63 % and 6.55 % respectively. The *J-V* characteristics for cell B showed Ohmic behaviour. The conclusion of this study was that the $CdCl_2$ treatment to the CdS is a necessary step to have a good performance. However, the order of applying the $CdCl_2$ treatment plays an important role in this process.

## 3.4 $CdCl_2$ treatment

The treatment discussed in this Section is the CdTe post-growth treatment with $CdCl_2$ (sometimes called *activation step*), with the treatment of the CdS having already been discussed in Section 3.3.

This treatment is undertaken by applying $CdCl_2$ on the back surface of the CdTe layer prior to annealing. The application of the $CdCl_2$ can be done a) ex-situ by either i) covering the CdTe sample with a saturated $CdCl_2$/methanol solution, or ii) evaporating a $CdCl_2$ thin film, and b) in-situ [15, 16]. This treatment is essential to obtain highly efficient CdTe solar cells. Although the exact role of this treatment is not clear, it affects the cell in several ways such as p-doping the material [17], enhancing CdTe re-crystallisation [18] and CdTe/CdS intermixing (interdiffusion) [19], which reduces interface state density in the CdTe/CdS interface [15].

Since the aim of this treatment is to diffuse Cl into the CdTe, its effectiveness depends on the annealing conditions (e.g. time, temperature and ambient [20]) and moreover, these must be optimised for CdTe deposited by different methods e.g. having different grain size. Gupta *et al.* [21] optimised the $CdCl_2$ treatment for fully sputtered CdTe/CdS cells with various CdTe thicknesses. The treatment of all cells was performed in $CdCl_2$ vapour at $T \sim 390$°C for various durations. While the optimum annealing time was ~ 30 minutes for a cell with 2.3 μm thick CdTe, only 10

minutes gave the best efficiency when the CdTe thickness was reduced to 0.87 μm (the efficiencies were 13 % and 11.8 % for cells with 2.3 and 0.87 μm thick CdTe films respectively). Although both the thickness of the back contact and the post-contact annealing was different in each cell (to obtain the best performance), the $CdCl_2$ treatment required may differ based on the nature of the CdTe (i.e. thickness in this case).

Major and Durose [22] used both OBIC and EQE technique to investigate the junction in the CdTe/CdS cell. Cells with three CdTe thicknesses (2, 4 and 6 μm) were treated by evaporating 200 nm thick $CdCl_2$ prior to annealing in air at 400°C, for durations between 20 and 50 minutes. The position of the junction in all cells was located at the same depth from the back contact for all samples, implying that it was formed due to the $CdCl_2$ diffusion in the CdTe. This means that $CdCl_2$ treatment must be optimised in order to diffuse Cl to the optimum position (i.e. the heterojunction) to avoid creating a buried junction (i.e. a homojunction within CdTe).

Hence, optimising the $CdCl_2$ treatment conditions for CdTe cells is necessary to achieve good performance. Insufficient treatment creates a buried junction (as discussed above) whereas over treatment may delaminate the films from the substrate.

## 3.5 Interdiffusion between CdTe and CdS

Interdiffusion between the CdTe and the CdS in their interface has been investigated by various techniques. It has been found that the materials can alloy either by the migration of Te or S across the junction [23, 24]. The intermixing process depends on various factors such as the growth temperature, post-growth annealing and the grain structure of the films. Usually the CdTe and the CdS intermix due to the post-growth thermal treatment. The diffusion of the materials into each other can be enhanced by introducing Cl prior to annealing [25]. However, it has been reported that the intermixing during the growth can be controlled by changing the CdTe growth conditions [26]. The effect of the intermixing on the performance of CdTe/CdS cells is significant. For example, $V_{oc}$ can vary as a function of the level of the intermixing [27]. Additionally, the CdTe band gap may be modified as a result of this process [26], and therefore, the EQE and the overall performance of the devices may be altered [28].

## 3.6 Transport mechanisms in the CdTe/CdS solar cells

Various transport mechanisms for carriers in the CdTe/CdS junction have been reported. Tunnelling and recombination transport mechanisms are among the most commonly reported mechanisms dominating the carrier flow. This may be a result of the high value of the mismatch between the CdTe and the CdS which is about 10.8 % [29]. Bayhan and Ercelebi [30] found that recombination of carriers in the interface states dominates the transport of the carriers at $T > 280$ K for both as grown and air annealed cells. However, annealing in air after applying $CdCl_2$ resulted in changing the transport mechanism to recombination in depletion region. This change was attributed to the reduction in the interface trap density due to the $CdCl_2$ treatment. For all cases, they found that for $T < 280$ K multi-step tunnelling dominated the transport of carriers. The improvement due the $CdCl_2$ annealing was also reported by Al-Allak *et al*. [31]. However in Al-Allak's work [31], for both a) as-grown and b) air-annealed samples, carriers obeyed the tunnelling recombination mechanism whereas the mechanism for $CdCl_2$ treated samples was thermal emission across the junction. The reason was again ascribed to be the decrease of the interface states due to the $CdCl_2$ treatment. In a study done by Linam *et al.* [32] the mechanism was seen to change from generation recombination at high voltage to tunnelling through defects at lower voltages. Tunnelling was assisted by higher intensities of the incident light. On the other hand, according to Mitchell *et al.* [33] recombination in depletion region dominated at $T > 294$ K but it changed to tunnelling at lower temperatures. A similar result was published by Chu *et al.* [11]. Also, Bayhan [34] found that tunnelling dominated at $T < 240$ K for both as-grown and $CdCl_2$ treated cells.

Even though tunnelling generally controls the carrier transport at lower temperature [35], dominance of tunnelling at 350, 370 and 410 K has been observed by Ou *et al.* [36], Sergue *et al.* [37] and Ercelebi *et al.* [38] respectively. In a recent study, Alnajjar *et al.* [39] concluded that the most dominant mechanism at room temperature was tunnelling recombination for cells annealed at different temperatures.

Other mechanisms have been observed in the CdTe/CdS heterojunction. Recombination at the junction interface was reported by Nollet *et al.* [40] for devices tested under illumination with different wavelengths of monochromatic light. The same result was found by Mahesha *et al.* [41] for low voltages, yet, the mechanism changed to space charge limited current (SCLC) when voltage increased. According to the calculation published by Kosyachenko *et al.* [42] both the thermal emission and

the generation-recombination currents may be the constituents of the dark current in the CdTe/CdS devices. Field-assisted drift was also reported for this heterojunction [43]. Shockley-Read-Hall (SRH) recombination was reported as the dominant transport mechanism by Oman *et al.* [44] and Hegedus *et al.* [45].

## 3.7 Contacting the back surface of CdTe/CdS cell

Various materials have been used in order to form back contacts for CdTe solar cell, and they are either Cu-containing or Cu-free. Cu is introduced in the back contact as it heavily dopes the back surface of CdTe. The formation of a $p^+$-layer between the absorber and the back contact leads to a better Ohmic contact. Cu is applied by several methods such as using graphite paste doped with Cu or evaporation of a thin layer of Cu on the back surface of CdTe [46]. However, Cu-containing contacts are potentially problematic, as Cu is a fast diffuser in CdTe, which degrades the PV performance of the cell [47, 48]. This degradation is thought to occur via: a) segregation at grain boundaries in CdTe, which creates shunting paths, and b) diffusion to the CdTe/CdS interface, and therefore increasing the resistivity of CdS by creating deep levels capturing electrons [49]. However, in a recent work Romeo *et al.* [49] reported that if a very thin layer of Cu (~ 2 nm) is evaporated on an etched CdTe back surface, devices do not suffer from degradation. Furthermore, Romeo *et al.* [49] invented a stable Cu containing contact by sputtering Mo/Cu($\leq$20 nm)/$As_2Te_3$ onto as-grown CdTe back surface (i.e. no etching was applied prior metallization) in order to form a stable $Cu_xTe$ phase, where $x < 1.4$. This phase can be achieved if Cu is deposited at $T$ = 200°C: Cu displaces As to form the desired phase and the free As evaporates [50]. A cell with this contact was reported to have $\eta$ of 15.8 % [50]. For this contact, there is no need for the Te-rich layer (which is formed by etching) as it is replaced by the $As_2Te_3$ layer, which forms the desired contact material by reacting with Cu as mentioned above.

Cu-free contacts such as Ni-P [51] and Ni [52], are used to overcome the instability issue due to Cu-containing materials. Moreover, Romeo *et al.* reported conversion efficiencies in the range of 14.6 – 16 % [2, 49, 53] for CdTe/CdS cells with Mo/$Sb_2Te_3$ back contact (the CdTe was etched chemically). The stabilities of both Mo/$Sb_2Te_3$ and Mo/Sb contacts were found to be superior to other contacts such as Mo/Cu [54].

Doping CdTe with As was investigated by Zoppi [17] in order to provide highly conductive p-type CdTe suitable for a tunnelling junction. Although As concentrations as high as $2 \times 10^{19}$ atom/cm$^3$ were achieved (as revealed by SIMS results), the lowest resistivity obtained was 200 Ω.cm (for As concentration of $2 \times 10^{18}$ atom/cm$^3$), which is not high enough for a tunnelling junction. The high resistivity of CdTe was attributed to a) the creation of [$V_{Cd}$-$As_{Te}$] complexes and [$As_{Cd}$] donors, and b) high density of grain boundaries with the incorporation of As with them. Contrary to this, Barrioz *et al.* [55] fabricated two CdTe:As/CdS cells, and compared their PV performance using different methods of back-surface treatment prior to metallization: a) etching the cell in $Br_2$/methanol solution (to create a Te-rich layer), and b) in-situ depositing CdTe:$As^+$ layer. Au was used to contact both devices. The CdTe:$As^+$-based cell showed better PV performance compared to the other cell. The etched cell showed a clear roll-over, while this effect disappeared for the cell with the CdTe:$As^+$ contact, indicating a significant improvement in the back contact.

Fahrenbruch [56] reported that applying heavily doped p-type semiconductors (such as $Cu_xTe$ and $Sb_2Te_3$) on CdTe back surface before metallization may facilitate carrier transport through the back contact by a) reducing the barrier height of the junction between CdTe and the semiconductor, and b) allowing carrier to tunnel from the semiconductor to the metal as the junction between these two materials is very thin. The band diagrams proposed by Fahrenbruch [56] for CdTe contacts using either $Cu_xTe$ or $Sb_2Te_3$ are shown in Figure 3.3.

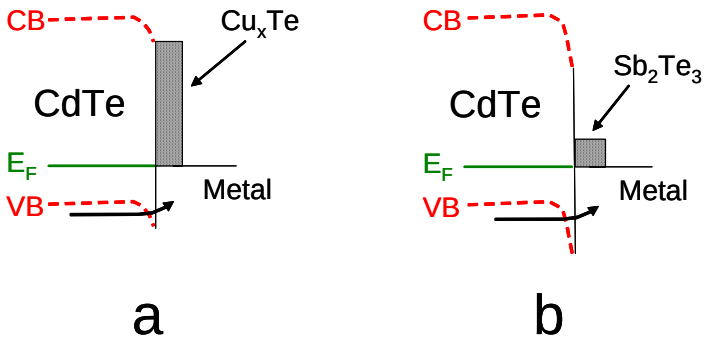


**Figure 3.3**: Band diagrams for a) metal/$Cu_xTe$/CdTe and b) metal/$Sb_2Te_3$/CdTe. The figure shows the mechanism by which holes transport from CdTe to the back contact in solar cells.

Forming a Te-rich layer on the back surface is a typical step for contacting CdTe cells before metallization [46]. Te is known to dope CdTe, creating a $p^+$-layer between it and the contact, similar to the Cu doping role explained above. This can be achieved by either wet or dry etching. However, wet etching is arguably more advantageous than dry etching since it is faster, easier and requires no heating [46]. Various etching solutions are used for this aim such as $Br_2$/methanol (BM), $Br_2$/dichrol/hydazine (BDH) and nitric/phosphoric acid (N-P) [46].

The chemical reactions between CdTe and N-P solution were proposed to be [57]

$$3CdTe(s) + 8HNO_3(aq) \rightarrow 3Te(s) + 3Cd(NO_3)_2(aq) + 2NO(g) + 4H_2O$$

and

$$CdTe(s) + 4NHO_3(aq) \rightarrow Te(s) + Cd(NO_3)_2(aq) + 2NO_2(g) + 2H_2O$$

The reactions above show that a Te excess results from this process by removing Cd from the film, which is preferable for contacting cells as explained earlier.

Another method to form the Te layer is by evaporating it to the back surface of cells directly, and Kraft *et al.*[58] compared contacts formed on the back surface of CdTe cells by both N-P etching and evaporation. They reported a barrier height of ~ 0.7 eV for both cases. On the other hand, Fritsche *et al.* [59] compared the experimentally determined band diagrams of back contacts with Te layers formed by etching and evaporation as well. They found that the band diagrams were dissimilar, and concluded that it is more effective to form the Te layer by etching rather than evaporation.

## 3.8 References for Chapter 3


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# Chapter 4: Experimental Methods

## 4.1 Introduction

This Chapter describes the experimental techniques that were used in this work for the fabrication, processing and characterising of devices, starting with the deposition techniques used (Section 4.2). Following that, in Section 4.3.1, a detailed description of the typical fabrication steps for device production is presented. Section 4.3.2 discusses special processing procedures employed in this work. Finally, analytical techniques by which the devices were investigated are described in Section 4.4.

## 4.2 Deposition techniques

### 4.2.1 Chemical bath deposition (CBD)

Chemical bath deposition (CBD) relies on a chemical reaction taking place in a solution in which substrates are immersed. Various semiconductor materials have been successfully deposited by CBD such as CdO [1], $Bi_2O_3$ [2] and ZnS [3]. CBD has several advantages such as simplicity and low cost. However, the large amount of the liquid waste of CBD can be problematic, especially if the waste contains poisonous materials.

This work includes samples incorporating CdS films grown by CBD. The structural, optical and electrical properties of the CBD-CdS principally depend on the growth conditions such as the recipe of the reacting chemicals [4] and the deposition temperature [5]. There are numerous recipes in the literature, however, the recipe used in this work was the standard one commonly used at Cranfield University [6] where the films were grown by the author. A deposition solution containing $CdCl_2$ (0.0024M), $NH_4Cl$ (0.028M) and $CSN_2H_4$ (0.057M) was diluted in DI water and contained in a water-jacket beaker, which was itself placed in an ultrasonic bath. The total volume of the solution was 500 ml. Figure 4.1 shows a schematic diagram of the apparatus used for the CBD-CdS deposition.

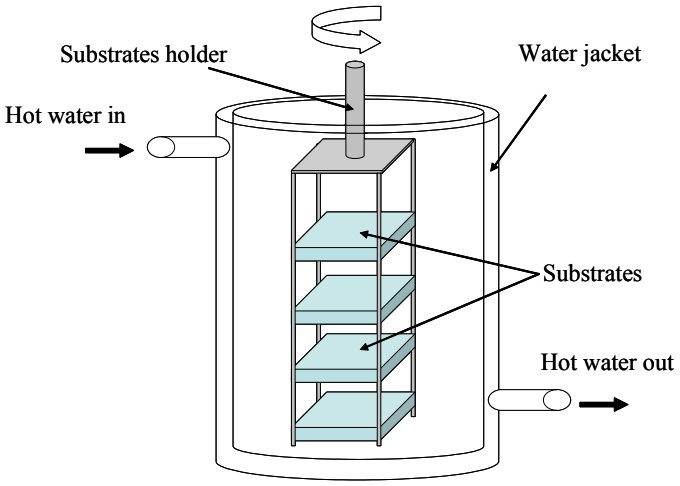


**Figure 4.1**: A schematic diagram of the apparatus used for depositing CdS by the CBD technique.

After cleaning the substrates (see Section 4.3.1) they were placed in a quartz holder prior to immersion in the solution. The holder (Figure 4.1) held up to four 5×5 cm substrates for simultaneous deposition. The deposition temperature was kept at ~ 70°C and controlled by circulating hot water in the water-jacket beaker. When the temperature of the solution reached ~ 70°C, 28 ml of 35% $NH_3$ solution was added to it, which started the deposition. During the whole process, the solution was stirred by rotating the holder by means of a small electrical motor. The deposition time was ~ 15 minutes and resulted in 150 – 200 nm thick CdS films.

### 4.2.2 Close space sublimation (CSS)

Physical vapour deposition (PVD) techniques are used to deposit thin films in vacuum by evaporation or sublimation. Close space sublimation is a PVD technique where deposition takes place by sublimation and the source tray is close to the substrate. Since it is difficult to evaporate materials with high melting point, sublimation represents a suitable alternative as it takes place at lower temperatures. CdTe (melting point = 1365°C [7]) is widely deposited by this technique since its vapour pressure is ~ 0.1 Torr at 600°C, which is one order of magnitude larger than the estimated vapour pressure required to generate functional condensation rates [8]. However, the separation between the source material and the substrate is therefore

much shorter in the CSS technique compared to standard evaporation one in order to reduce the vapour loss.

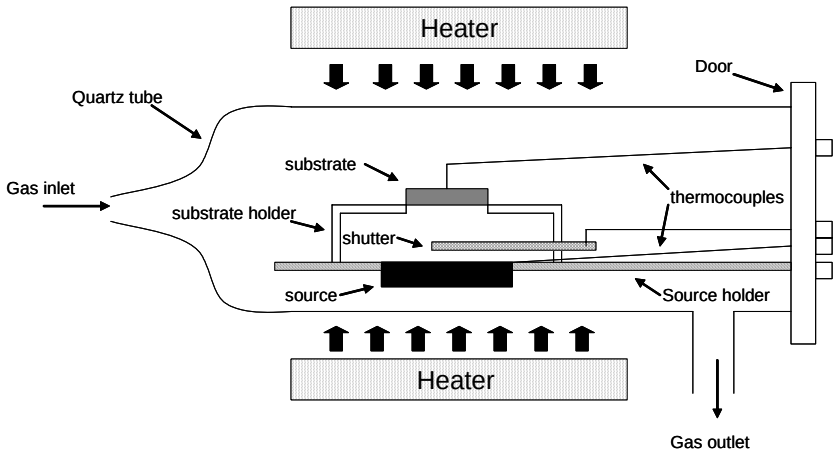


**Figure 4.2**: **A** schematic diagram of the CSS reactor.

The CSS kit used in this work was built by Electro Gas System Ltd. Figure 4.2 shows a schematic diagram of the reactor in this kit. The tube and the furniture inside are made from quartz to minimise the inclusion of impurities. The separation between the substrate and the source material is ~ 12 mm. There are two thermocouples inside the reactor: one touches the tray of the source material and the other touches the substrate. Heating is provided by two separate heaters (upper and lower), each with a separate temperature control. Various gases such as $O_2$, $N_2$ and $H_2$ can be introduced into the reactor. The chamber pressure is controlled by both automatic and manual valves placed between the reactor and a scroll pump.

A separate but identical reactor is used for each material deposition i.e. CdTe and CdS. The source materials for both cases are supplied by Alfa Aesar as powder with purity of 5N. A variety of gaseous ambients and growth conditions (e.g. temperature and time) were used throughout this work. Specific details for each growth run are given in the appropriate chapter.

### 4.2.3 Sputtering

Sputtering is a vacuum technique in which deposition takes place by ejecting atoms from the target material by bombarding it with energetic ions. Those sputtered atoms then condense on the surfaces of the surrounding objects e.g. substrates. Electric and magnetic fields are used in sputtering process so that a) the ions gain enough kinetic energy, and b) they can be aimed to the target. Sputtering usually uses un-reactive ions, notably argon and is therefore suitable for a wide range of materials [8].

Sputtering types are categorised based on the applied electric field between the target and the substrate into: a) DC, and b) RF (radio frequency). The DC type is suitable for sputtering only conductive materials, due to charge accumulation on the surface of non-conductive materials. This issue may be overcome by using RF sputtering instead [9].

AJA International, Inc. ATC ORION sputtering systems were used to deposit the materials in this work, with the sputtering targets also being supplied by AJA.

The study concerning devices fabricated with sputtered CdS is presented in Section 5.3.2.1. Those CdS films were sputtered from a 5N CdS target at room temperature with an RF power of 200 W. The total pressure in the chamber was 5 mTorr provided by an $O_2$/Ar mix with a 5 % $O_2$ concentration. The deposition time was 16.5 minutes, and the thickness of the films was ~ 200 nm as measured by an Ambios XP 200 profiler (see Section 4.4.4 for details of thickness measurement).

### 4.2.4 Metal organic chemical vapour deposition (MOCVD)

This technique is a specific kind of chemical vapour deposition (CVD) [10]. The required chemicals are admitted to the deposition chamber in the vapour phase, and then react near a heated substrate [11]. Since the deposition is due to chemical vapour reaction, it is not a vacuum technique. CdTe and CdS layers grown by MOCVD in this thesis were fabricated at Bangor University. The precursors used for CdTe growth were dimethylcadmium (DMCd) and diisopropyltelluride (DIPTe) while they were dimethylcadmium (DMCd) and ditertiarybutylsulphide (DTBS) for CdS. For these devices, the $CdCl_2$ treatment was applied in-situ by MOCVD, using dimethylcadmium (DMCd) and tertiarybutylchloride (tBuCl) or *n*-hexylchloride (*n*-

HexCl) alkyl precursors. More detailed description about the deposition procedures is reported by Barrioz *et al.* [12-14].

### 4.2.5 Thermal evaporation

Thermal evaporation is another kind of PVD technique, and it is commonly used for depositing thin films. It is the most effective method to deposit materials with low melting points [8]. This technique is similar to CSS in the sense that deposition relies on heating the source material under vacuum. However, in thermal evaporation the vaporisation takes place from a liquid phase, whereas in CSS it occurs from a solid phase. As the vapour pressure is much grater than for CSS deposition, the separation between the substrate and the source could be few tens of centimetres.

Thermal evaporation was used to deposit three materials in this work: $CdCl_2$, In and Au.

*$CdCl_2$*

The evaporator used to deposit this material is custom made, and consists of a single chamber connected to both rotary and diffusion pumps. Deposition took place at a pressure of ~ $10^{-5}$ Torr, with the deposited thickness being in-situ monitored. The source material was a powder with purity of 4N supplied by Aldrich.

*In*

Evaporation of In was similar to that of $CdCl_2$ but in a separate evaporator. However, there was no thickness monitoring during In deposition.

*Au*

Au was deposited by UNIVEX 300 evaporator at a pressure of ~ $10^{-5}$ Torr. The Au was 6N pure and supplied by Advent. Various masks were custom made and used for contacting samples. The thickness of the deposited films was in-situ monitored.

## 4.3 Device fabrication and material processing

### 4.3.1 Device fabrication steps

Details of the cleaning, growth and processing procedures used in device fabrication used in this thesis are now provided.

a) Cleaning the TCO substrates.

- Rubbing each plate by tissues saturated with Decon90 soap solution.
- Rinsing thoroughly by DI water.
- Soaking in Decon90 soap solution combined with ultrasonication for 30 minutes.
- Rinsing thoroughly by DI water.
- Soaking in acetone combined with ultrasonication for 15 minutes.
- Soaking in iso-propanol combined with ultrasonication for 15 minutes.
- Drying with dry $N_2$.

b) Growth of the CdS

CdS films were grown by either CBD, sputtering, CSS or MOCVD see Section 4.2 for more details.

c) Optional post-growth treatment of the CdS

The typical treatment for the CdS performed in the device fabrication was post-growth annealing in $H_2$ ambient in the CdTe CSS reactor. However, for investigations of the CdS/TCO bilayer (Chapter 5), CdS annealing was also performed in either $O_2$ or $N_2$. Heating was provided by either the upper of the lower heater. Details of annealing conditions (e.g. time and temperature) are given for each experiment specifically in later chapters.

d) Growth of the CdTe

The growth of the CdTe was undertaken by either CSS or MOCVD, see Section 4.2 for details.

e) Chloride treatment

*Deposition*

The treatment was applied by thermal evaporation of $CdCl_2$ layers on the back surface of the CdTe, see Section 4.2.5 for details.

*Annealing*

After applying the $CdCl_2$, all samples were annealed in air using a tube furnace. The samples were placed on a silicon wafer held on a quartz frame. The duration of annealing started when the sample was put in the middle of the furnace, and ended when it was removed to the edge of the furnace tube. A range of temperatures and annealing times were used in this work, specific details are given in the relevant chapters.

*Cleaning*

Following annealing, all samples were washed by hot DI water to remove any excess amount of $CdCl_2$ left after treatment. Next, the samples were washed thoroughly by DI water prior to drying by a flow of $N_2$.

f) Preparation of the CdTe surface for back contacting

In the case of this work different etching techniques were used to prepare the back surface of devices for contacting. The procedure of each technique is described below, while a study of contacting is presented in Chapter 7.

i) N-P etching

N-P etching is a typical processing step for fabricating devices. It was used with most of cells investigated in this work. The steps of etching are as following:

- Each sample was etched in a solution comprising 70 % $H_3PO_4$, 29 % $H_2O$ and 1 % $HNO_3$ [15] for 10 seconds, with timing being started from immersion in the solution.
- Rinsed thoroughly by DI water,
- Blowing dry with $N_2$,

ii) Plasma etching

This process was performed in the sputtering system using an $Ar^+$ plasma. Etching was performed at room temperature under a pressure of 10 mTorr of Ar using a DC power of 25 W. The etching rate of the conditions described above was ~ 7 nm/minute.

g) Contact deposition

Different materials applied by different deposition techniques were used to contact samples investigated in this work, as described below.

i) Thermal evaporation

Au contacts were always applied by thermal evaporation, see Section 4.2.5. Similarly, In contacting (for the CdS/TCO bilayer study in Chapter 5) was done by this technique as well.

ii) Sputtering

In Chapter 7, besides using Au, either $As_2Te_3$ or $Sb_2Te_3$ were DC sputtered as back contacts for the devices. The deposition conditions for both $As_2Te_3$ and $Sb_2Te_3$ were similar and as follows: DC power was 25 watts with a chamber pressure of 5 mTorr (pure Ar). The deposition time was 30 minutes at temperature of 300°C, resulting in a 100 nm thick film. Subsequently, both materials were covered by a layer of 200 nm Mo sputtered by: 100 watts (DC) at 5 mTorr pressure (Ar) for 25 minutes at 300°C.

### 4.3.2 Materials processing steps for special studies (bevel etching)

The bevel etching of CdTe cells was undertaken in order to prepare cells for rapid screening experiments (see Section 5.3).

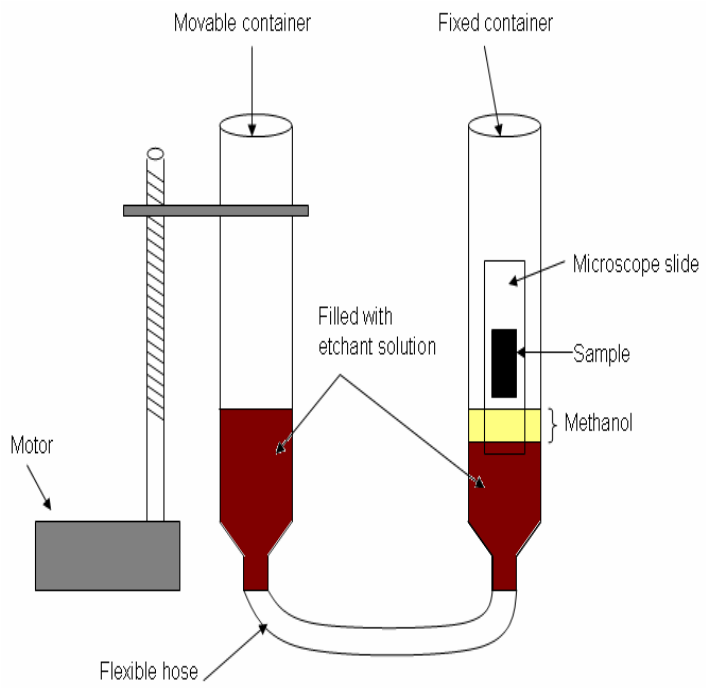


**Figure 4.3**: A schematic diagram of the bevelling apparatus.

Figure 4.3 shows a schematic diagram of the apparatus used for bevelling the samples, with the bevelling process being as follows. Each sample was attached to a microscope slide by wax prior to etching. Next, bevelling was performed by immersing the sample at a speed of 2 mm/min into a solution comprising 4.5% bromine, 25.5% methanol and 70% ethylene glycol (by volume). Immersion rate was controlled by means of an apparatus comprising two containers connected by a flexible tube. The sample was fixed in one, and the level of the liquid was controlled by moving the other by means of a lead screw driven by a slow motor. There was ~ 1 cm deep layer of pure methanol on top of the etchant solution in the container holding the sample, (Figure 4.3), in order to protect the sample from being etched due to the etchant solution vapour [16]. Figure 4.4 illustrates complete CdTe/CdS cells before and after bevelling and contacting. Details of the order of bevelling, $CdCl_2$ treatment and contacting used in specific studies may be found in Section 5.3.

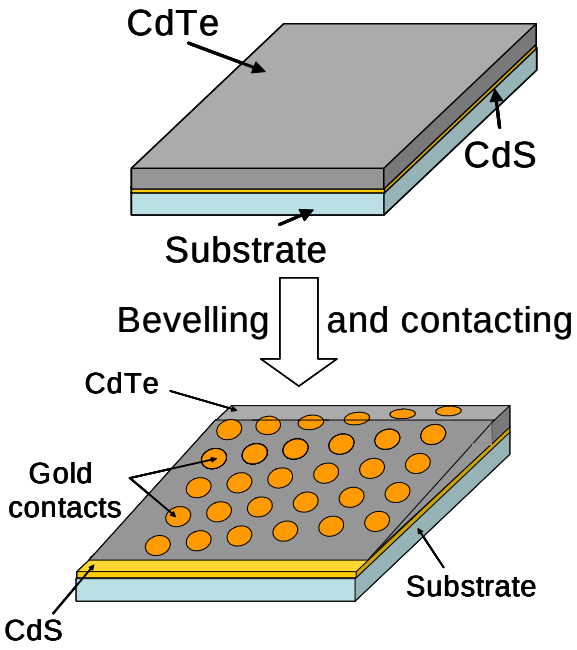


**Figure 4.4**: CdTe/CdS sample before (upper) and after (lower) bevelling and contacting.

## 4.4 Characterisation methods

### 4.4.1 *J-V* characterisation

The *J-V* measurements were carried out in this work by applying a voltage across the device terminals using a Keithley 2400 source meter, which also measured the resultant current. The *J-V* data were fed into a Labview programme in order to determine the basic PV working parameters i.e. $\eta$, $FF$, $V_{oc}$ and $J_{sc}$.

The *J-V* measurements were done in both dark or under light. An Oriel 81160 solar simulator was used to provide the AM1.5 illumination for light measurements (see Section 1.3.1 for more details about the AM1.5 spectrum).

### 4.4.2 *J-V-T* characterisation

In this method a family of *J-V* curves are recorded for a range of temperature ($T$). The same setup described in the previous Section was used for this measurement. However, in order to perform the *J-V* characterisation at varying $T$, the samples were mounted inside a cryostat chamber. The cryostat system consisted of a CTI Cryogen

*J-V-T* measurements were performed in both dark and at various light intensities. Light from the simulator was transferred into the cryostat by mirrors and its intensity was controlled by natural density (ND) optical filters.

### 4.4.3 Light biased external quantum efficiency (EQE)

The EQE measurements in this work have been performed by the author at Glyndŵr University, using a PVE300 photovoltaic spectral response kit supplied by Bentham. The wavelength range scanned was 300 – 950 nm, quantified by a calibrated silicon photodiode. The bias light (AM1.5) was delivered to the sample by fibre optic bundle from quartz halogen source, and was used over a uniform 1 $cm^2$ area.

### 4.4.4 Film thickness measurement

An Ambios XP 200 profiler was used to measure the thickness of the deposited films. In case of CdTe, the film was scribed by a scalpel prior to measuring the depth of the resultant grove i.e. the CdTe thickness. On the other hand, as it is hard to create a groove on the CdS films by scribing, a cotton bud saturated with HCl was used to dissolve part of the CdS film. The profiler determined CdS thickness by measuring the height difference between the CdS and the revealed substrate. Figure 4.5 illustrates the groove in a layer scanned by the profiler in order to determine the thickness.

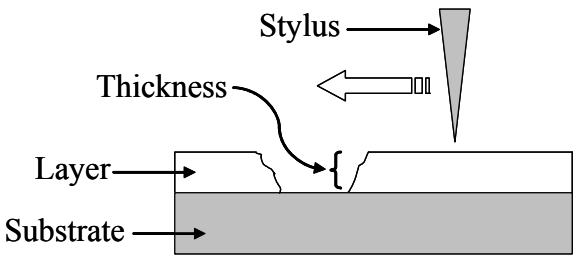


**Figure 4.5**: Thickness measurement of a thin film using a stylus profilometer.

### 4.4.5 Compositional analysis techniques

#### 4.4.5.1 Secondary ion mass spectroscopy (SIMS)

This is a destructive technique used to profile the composition of thin films. It sputters the surface of the investigated sample by a focused *primary ion beam* (see Section 4.2.3 for more details about sputtering). The sputtered *secondary ions* are then detected and analysed based on their mass/charge ratio [17]. The primary ions not only eject the secondary ions but also remove layers of the surface, resulting in a *crater*. As the primary ions continue bombarding, they sputter and probe the newly revealed layer of the sample. Therefore, depth profiles of the sample composition can be determined. The depth resolution of SIMS can be as shallow as 5 – 10 nm [18]. Due to the sensitivity of mass spectrometer detection, SIMS may be used to profile both major components and trace components, for example dopants in semiconductors.

#### 4.4.5.2 Auger electron spectroscopy (AES)

This characterisation technique is based on the Auger effect. If a core electron is sufficiently excited to create a core hole, another electron from an outer shell will recombine with this hole. The recombination results in an X-ray photon which is capable of ejecting a second electron from the same atom. This emitted electron is called Auger electron, which is a characteristic of the atom.

In AES a primary electron beam is used to emit Auger electrons from the sample. Those ejected electrons are detected and used to identify the elements of the sample. Auger analysis can be combined with sputtering so that a compositional depth profile of the sample is obtained [19]. Since the escape depth of Auger electrons is short [18], the surface sensitivity of AES is extreme. Therefore it is a powerful tool to investigate surfaces.

In this work both SIMS and AES runs were performed and analysed by Loughborough Surface Analysis Ltd.

#### 4.4.5.3 Grazing incidence X-ray diffraction (GIXRD)

This is a special kind of X-ray diffraction technique (XRD). In standard XRD, the samples are investigated by illuminating them with X-ray beams and detecting the scattered (diffracted) beams resulting. According to Bragg's law, if the lattice planes (formed by the atoms in the crystal) are perfect and spaced by a distance *d* as shown in Figure 4.6, then the "reflection" of a monochromatic beam takes place only at a certain angle which satisfies the following equation [20]

$$\lambda = 2d_{hkl} \sin\theta \qquad (4.1)$$

where *h*, *k* and *l* are the Miller indices of the plane, $\lambda$ is the wavelength of the beam and $\theta$ is the incidence angle (and the reflection angle too as reflection is assumed to be elastic). Equation 4.1 implies that by using a monochromatic X-ray (with a known wavelength) and detecting the diffraction angles, *d* values can be calculated. These data are then compared to the standard values to probe the crystallinity and the composition of the material.

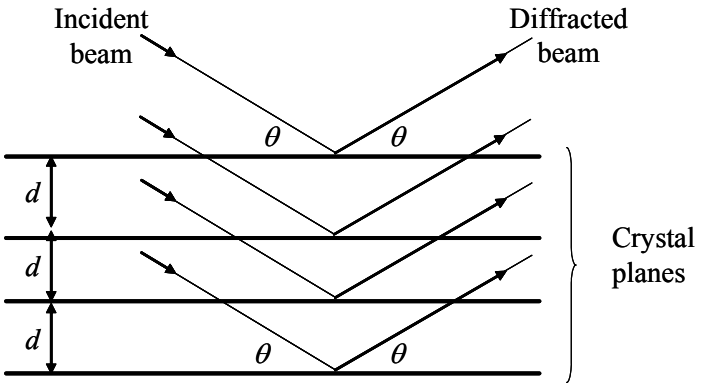


**Figure 4.6**: A perfect crystal with incident and diffracted beams. *d* is the spacing between each two adjacent planes and $\theta$ represents both incident and diffracted angles.

In GIXRD, the incident angle is chosen to be very small, which results in shallow penetration into the material. Therefore, the diffracted beams give information about the surface rather than the bulk. The surface sensitivity can be increased by further reducing the incidence angle [21]. The GIXRD runs in this work were carried out by another research group at Durham University.

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# Chapter 5: CdS Window Layers: Junction Properties, Processing and their Influence on Devices

## 5.1 Introduction

This Chapter presents two studies: the first part (Section 5.2) is concerned with annealing the TCO prior to and after the growth of the CdS. The ambients in which annealing took place were chosen to a) oxidise or b) reduce the substrates and the films. The aim was to establish the effects of such treatment on the electrical junction properties of the CdS/TCO bilayers which are themselves reviewed in Section 3.2. In particular the present work was motivated by that of Alamri and Brinkman [1] in which it was shown that when the substrate comprises ITO/glass, then post-growth annealing of the CdS in air transforms the junction from Ohmic to rectifying. Alamri's attribution of this to a change in the ITO itself is a hypothesis that is tested in the present work. An alternative explanation based on the formation of a CdO over layer is proposed.

In the second part (Section 5.3), the work was extended to the study of full device structures. Their photovoltaic device performance was investigated after annealing the CdS in either $H_2$, $N_2$ or $O_2$ ambients. It is well known that for any given CdTe processing conditions the outcome also depends upon the thickness of the CdTe layers itself. As described in the review (Section 3.4), the CdTe thickness directly affects the proximity of the chlorine diffusion front to the CdTe/CdS junction for example. The effect of the thickness of the CdTe on the performance of each device set was therefore studied. However, instead of fabricating devices with different CdTe thicknesses by multiple growth runs, a rapid screening methodology of varying the thickness of the CdTe film was developed. The method involved bevel etching the devices to create films having wedged profiles, allowing different thicknesses of the CdTe film to be tested in the same sample. The success of this method depends initially on the uniformity of the photovoltaic performance of the starting material. Section 5.2 therefore contains details on the growth conditions explored in preliminary studies to establish process uniformity prior to the rapid screening. It was found that the quality of results depends on the smoothness and uniformity of the

CdTe layers. The method was demonstrated to be viable. It was used to show that moderate oxidising or reducing treatment of the CdS prior to the CdTe growth did not have a major influence on the PV device performance.

## 5.2 The effect of annealing the CdS films and substrates on the CdS/TCO interface properties

### 5.2.1 Preface of this Section

As stated in Section 5.1, in this Section the effects of a) pre-annealing the TCO substrates and b) the post-growth annealing of CdS/TCO bilayers were investigated. The experiments are described in Section 5.2.2. Prior to the actual measurements of the *I-V* characteristics of CdS/TCO junctions, it was necessary to devise and test a method of checking for pinholes in the CdS. This is also outlined in Section 5.2.2. The results of the *I-V* tests as a function of substrate type and annealing in various oxidising and reducing ambients are presented in Section 5.2.3. Since the evidence pointed to a chemical change in the CdS layers taking place, physical and analytical tests were undertaken and are presented and discussed in Sections 5.2.3 and 5.2.4.

### 5.2.2 Experimental (CdS/TCO bilayer)

*Sample preparation: bilayers, pre- and post-growth treatment*

The growth, annealing and contacting details for all samples studied in Section 5.2 are shown in Table 5.1. Growth of the CdS films was undertaken by close space sublimation (CSS) using the apparatus described in Section 4.2.2. The source temperature was 650°C, while the substrate temperature was in the range 490-550°C. Most films were grown on 5×5 cm ITO/glass substrates supplied by either VisionTek or Delta Tech. with some additional tests being done on $SnO_2$/glass (Pilkington TEC 8) substrates (see Table 5.1).

For the work on ITO/glass substrates, annealing took place either a) prior to the CdS growth i.e. pre-annealing of the ITO substrates or b) post-growth. For the pre-annealing (a), the ITO/glass substrates were heated in the CSS reactor in one of two

gaseous ambients: i) 100 Torr of $O_2$ or ii) 15 Torr of $H_2$ + 60 Torr of $N_2$. In both cases the substrates were heated to 400°C for 10-40 minutes using the substrate heater only (see Section 4.2.2 for details of the apparatus). One further pre-annealing run under $O_2$ was undertaken at 550°C for 40 minutes in order to investigate the effects of more severe oxidising conditions.

After annealing, the TCO substrates were allowed to cool in the chamber and the system was flushed with $N_2$ to remove the annealing ambient prior to CdS deposition. It should be noted that for the $H_2$ + $N_2$ annealing, vacuum was not broken prior to the CdS deposition, as the CdS source remained in the CSS chamber during annealing. However, in the case of $O_2$ annealing the source was removed prior to annealing to protect it from oxidisation. This meant that vacuum needed to be broken to replace the source before the CdS deposition. Nineteen CdS growth runs were made for this part of the work.

To study the post-growth treatment (b) of the CdS, three CdS films were deposited on non-treated substrates (two Delta Tech. and one VisionTek ITO). The post-growth annealing procedure was the same as that for the pre-growth annealing in the same ambients (see Table 5.1).

Since Alamri's work suggests that the post-growth oxidation of CdS/ITO and CdS/$SnO_2$ gave different results, further runs were done on the latter for comparison.

All samples were finally contacted with a matrix of sixteen In dots (2 mm diameter) which was applied by thermal evaporation at a pressure of ~ $10^{-5}$ Torr. In was used since it makes an Ohmic contact with CdS [1], allowing any rectification behaviour to be credited to the CdS/ITO interface. The dark *I-V* characteristics were measured using the equipment described in Section 4.4.1 and the results of the investigation are presented in Section 5.2.3.

| Sample | TCO supplier (type) | TCO treatment | | | CdS treatment | | | Contact | Results of *I-V* curve |
|---|---|---|---|---|---|---|---|---|---|
| | | Gas and pressure (Torr) | *T* (°C) | Time (min) | Gas and pressure (Torr) | *T* (°C) | Time (min) | | |
| 49 | VisionTek (ITO) | $O_2$ (100) | 400 | 40 | ---- | ---- | ---- | In (then Au) | Ohmic (for Au see text) |
| 50 | VisionTek (ITO) | $O_2$ (100) | 400 | 30 | ---- | ---- | ---- | In | Ohmic |
| 51 | VisionTek (ITO) | $O_2$ (100) | 400 | 20 | ---- | ---- | ---- | In | Ohmic |
| 52 | VisionTek (ITO) | $O_2$ (100) | 400 | 10 | ---- | ---- | ---- | In | Ohmic |
| 53 | VisionTek (ITO) | ---- | ---- | ---- | ---- | ---- | ---- | In | Ohmic |
| 54 | VisionTek (ITO) | $O_2$ (100) | 550 | 40 | ---- | ---- | ---- | In | Ohmic |
| 55 | VisionTek (ITO) | $H_2$ (15) + $N_2$ (60) | 400 | 10 | ---- | ---- | ---- | In | Ohmic |
| 56 | VisionTek (ITO) | $H_2$ (15) + $N_2$ (60) | 400 | 20 | ---- | ---- | ---- | In | Ohmic |
| 57 | VisionTek (ITO) | $H_2$ (15) + $N_2$ (60) | 400 | 30 | ---- | ---- | ---- | In | Ohmic |
| 58 | VisionTek (ITO) | $H_2$ (15) + $N_2$ (60) | 400 | 40 | ---- | ---- | ---- | In (then Au) | Ohmic (for Au see text) |
| 60 | Delta Tech. (ITO) | ---- | ---- | ---- | ---- | ---- | ---- | In | Ohmic |
| 61 | Delta Tech. (ITO) | $O_2$ (100) | 400 | 10 | ---- | ---- | ---- | In | Ohmic |
| 62 | Delta Tech. (ITO) | $O_2$ (100) | 400 | 20 | ---- | ---- | ---- | In | Ohmic |
| 63 | Delta Tech. (ITO) | $O_2$ (100) | 400 | 30 | ---- | ---- | ---- | In | Ohmic |
| 64 | Delta Tech. (ITO) | $O_2$ (100) | 400 | 40 | ---- | ---- | ---- | In (then Au) | Ohmic (for Au see text) |
| 65 | Delta Tech. (ITO) | $H_2$ (15) + $N_2$ (60) | 400 | 10 | ---- | ---- | ---- | In | Ohmic |
| 66 | Delta Tech. (ITO) | $H_2$ (15) + $N_2$ (60) | 400 | 20 | ---- | ---- | ---- | In | Ohmic |
| 67 | Delta Tech. (ITO) | $H_2$ (15) + $N_2$ (60) | 400 | 30 | ---- | ---- | ---- | In | Ohmic |
| 68 | Delta Tech. (ITO) | $H_2$ (15) + $N_2$ (60) | 400 | 40 | ---- | ---- | ---- | In (then Au) | Ohmic (for Au see text) |
| 74 | VisionTek (ITO) | ---- | ---- | ---- | 100Torr $O_2$ | 400 | 40 | In | Rectifying |
| 75 | Delta Tech. (ITO) | ---- | ---- | ---- | 100Torr $O_2$ | 400 | 40 | In | Rectifying |
| 97 | Delta Tech. (ITO) | ---- | ---- | ---- | $H_2$ (15) + $N_2$ (60) | 400 | 40 | In | Ohmic |
| T1 | Pilkington TEC 8 ($SnO_2$) | ---- | ---- | ---- | ---- | ---- | ---- | In | Ohmic |
| T2 | Pilkington TEC 8 ($SnO_2$) | ---- | ---- | ---- | 100Torr $O_2$ | 400 | 40 | In | Rectifying |
| G | Delta Tech. (ITO) | ---- | ---- | ---- | No CdS | No CdS | No CdS | Au | Ohmic |

**Table 5.1**: The annealing details for i) the ITO/glass (samples 46-68), ii) the CdS/ITO bilayers (samples 74-97) and iii) the CdS/$SnO_2$ (samples T1 and T2). The table contains the contact types and the results of the *I-V* characteristics.

*Testing the coverage of the CdS film:*

The presence of pinholes in the CdS film may result in misleading *I-V* curves for the In/CdS/ITO structure. If In has a direct contact with the ITO at some areas of the sample, the resulting *I-V* curve will be Ohmic regardless of the junction type at the CdS/ITO interface. Therefore, it was an essential requirement that the coverage of the CdS film be tested before undertaking the study.

In this work a method of testing the CdS film continuity was devised. It is well known that Au makes a Schottky contact with CdS [2]. Hence, a structure comprising Au/CdS/ITO should always display rectifying behaviour even when the CdS/ITO junction is Ohmic. However, when pinholes in the CdS are present, then a direct Ohmic contact will be established between the Au and the TCO, and the *I-V* curve will be Ohmic. Moreover, Au was also evaporated directly on as-grown Delta Tech. ITO (sample G, Table 5.1). The aim of this control was to measure the resistance of the direct contact between Au and the ITO in order to compare it with the resistance of the other Ohmic contacts in this study. Results are presented in Section 5.2.3.

*Material analysis*

Instrumental methods of physical and chemical analysis were applied to the CdS in order to evaluate changes that occurred to it during annealing. Surface structure was evaluated by grazing incidence XRD while the surface and the bulk chemistries of the layers were evaluated by AES and SIMS respectively. The latter were undertaken by Loughborough Surface Analysis Ltd. Details of the methods are given in Section 4.4.5.

### 5.2.3 Results

*Continuity of the CdS films*

In order to validate the method of using Au contacts to test the continuity of the CdS/ITO films, samples 49, 58, 64 and 68 were contacted with an 11×11 matrix of 2 mm diameter Au dots (this step took place subsequent to recording the *I-V* curves for In/CdS/ITO dots, the Au dots being interspersed between the In ones). For each sample, the *I-V* curves of thirty dots were measured. Three lines of dots were selected so as to probe the whole of each substrate: these formed a central cross and a line along one edge.

For all samples (49, 58, 64 and 68) there was a mixture of both rectifying and Ohmic behaviour for the Au/CdS/ITO junctions measured. Figure 5.1a shows a typical example of rectifying behaviour. Since for a contact comprising a Au dot applied directly to the ITO the behaviour was Ohmic, this rectification is considered to be due to the Au/CdS junction itself as expected. However, for other dots there is Ohmic behaviour (Figure 5.1b) which may be attributed to pinholing in the CdS. It may therefore be concluded that the method is capable of detecting pinholes in CdS.

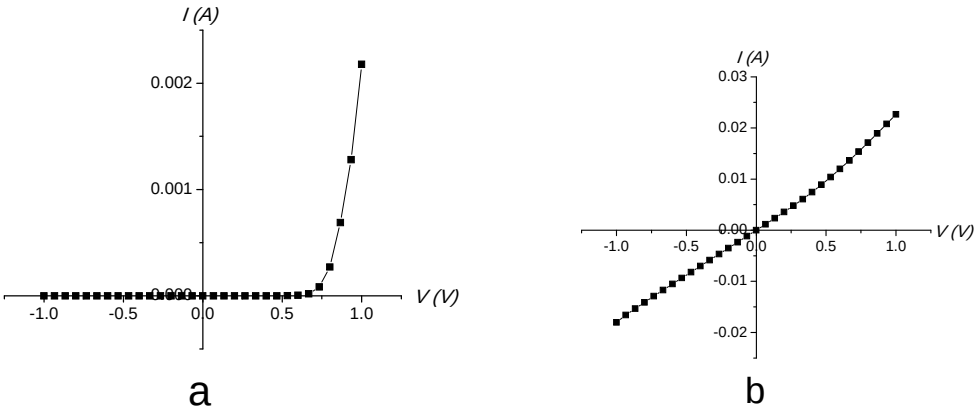


**Figure 5.1**: *I-V* curve for a) an Au/CdS/ITO structure showing non Ohmic behaviour, indicating that the CdS layer was pinhole free. b) The Ohmic behaviour of another dot on the same sample (sample 64, see Table 5.1) indicated the presence of pinholes.

The data for samples 49, 58, 64 and 68 also allowed comparison of the integrity of CdS layers grown under identical conditions on VisionTek and Delta Tech. substrates respectively. Whereas 56 % of the contacts on VisionTek ITO were Ohmic, the percentage for layers on Delta Tech. substrates was typically 10 %. The practical implication of this result is that more significance should be attached to the results for Delta Tech. substrates since they were much less likely to have pinholes. In addition, it was found that the uniformity of CdS growth had an effect on pinholing: generally there was a higher incidence of pinholes in the CdS near the substrate edge as it was thinner in these regions. Overall it was found that CdS with high integrity was grown in regions > 1 cm from the substrate edge. This material was therefore selected for the experiments.

*CdS films grown on pre-treated ITO substrates*

The *I-V* curves for all CdS samples grown on either as-grown or pre-treated ITO substrates (both oxidised and reduced) and then contacted with In were found to be straight lines i.e. Ohmic as illustrated in Figure 5.2. Those shown in the figure were selected from the results of samples 54, 60, 64 and 68 (see Table 5.1 for both the growth and the treatment conditions).

In order to test the possibility that pinholes in the CdS were responsible for this Ohmic behaviour two samples (64 and 68) were checked using the Au dot method. Each In dot was surrounded by four Au dots, with the separation between the In dot and each of its neighbouring Au dots being < 2 mm. The *I-V* characteristics for all neighbouring Au dots were rectifying, implying the absence of pinholes in the CdS at those areas.

Although all the *I-V* characteristics for In/CdS/ITO dots (Figure 5.2) were Ohmic for all the annealing ambients (i.e. oxidising and reducing), their resistance varied. The resistance values determined by testing all the In dots of samples 64 (oxidised) and 68 (reduced) were 21.5 ± 3.9 Ω and 15.3 ± 3.2 Ω respectively. For a control sample G (see Table 5.1) having a direct Au/ITO contact, the resistance was 18.1 ± 3.1 Ω, while the resistance of the Ohmic Au/CdS/ITO contacts (i.e. the Au contacts of the pinholey CdS as shown in Figure 5.1b) was 56.5 ± 4.8 Ω . These findings are summarised in Table 5.2 and discussed in 5.2.4.

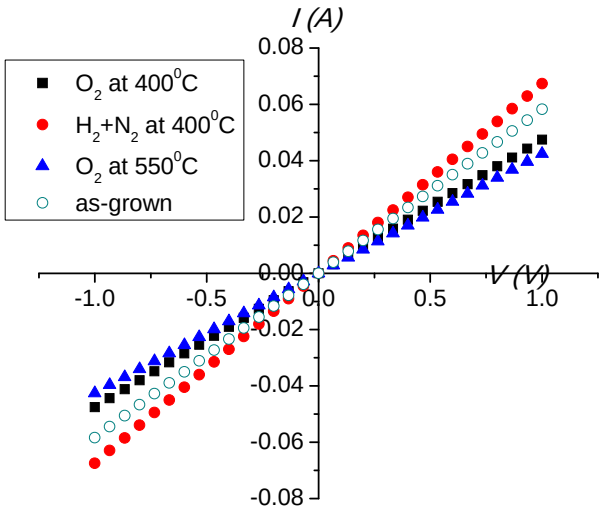


**Figure 5.2**: Typical results showing the Ohmic behaviour of the In/CdS/(Delta)ITO structure. The ITO was either as-grown (hollow circles) or pre-treated in a) $O_2$ at 400°C (squares), b) $H_2$ at 400°C (solid circles), or c) $O_2$ at 550°C (triangles). These curves were selected from the data from samples 54, 60, 64 and 68 (see Table 5.1).

| Structure | Sample | Treatment of the CdS layer | Resistance |
|---|---|---|---|
| In/CdS/ITO | 64 | Pre-growth in $O_2$ | 21.5 ± 3.9 Ω |
| In/CdS/ITO | 68 | Pre-growth in $H_2$ + $N_2$ | 15.3 ± 3.2 Ω |
| In/CdS/ITO | 97 | Post-growth in $H_2$ + $N_2$ | 17.7 ± 3.2 Ω |
| Au/CdS/ITO | 64 | Pre-growth in $O_2$ | 56.5 ± 4.8 Ω |
| Au/ITO | G | No CdS | 18.1 ± 3.1 Ω |

**Table 5.2**: Resistance values obtained from Ohmic metal/CdS/ITO structures. Each value is the average of 16 readings ± 1 SD except for Au/CdS/ITO (in sample 64) from which 3 readings were recorded.

*Post-growth annealed CdS/ITO films*

The post-growth treated CdS/ITO samples showed a different behaviour. The CdS/ITO annealed in a $H_2$ + $N_2$ ambient typically had Ohmic behaviour as shown in Figure 5.3a. All the sixteen In dots on sample 97 (see Table 5.1) had the same Ohmic

*I-V* characteristics with a resistance of 17.7 ± 3.2 Ω. Since this sample was on Delta Tech. ITO pinholing is not thought to be responsible and the CdS/ITO junction itself is therefore considered to be Ohmic.

On the other hand, the shape of the *I-V* curve of the In/CdS/ITO using $O_2$-annealed CdS changed dramatically as shown in Figure 5.3b. After this treatment, the *I-V* curves showed a significant change from being Ohmic (for non-treated CdS-based samples) to fully rectifying. This behaviour (also observed by Alamri [1]) implies that a significant change had happened to at least one of the two interfaces in the tested structure (i.e. the In/CdS or CdS/ITO interface).

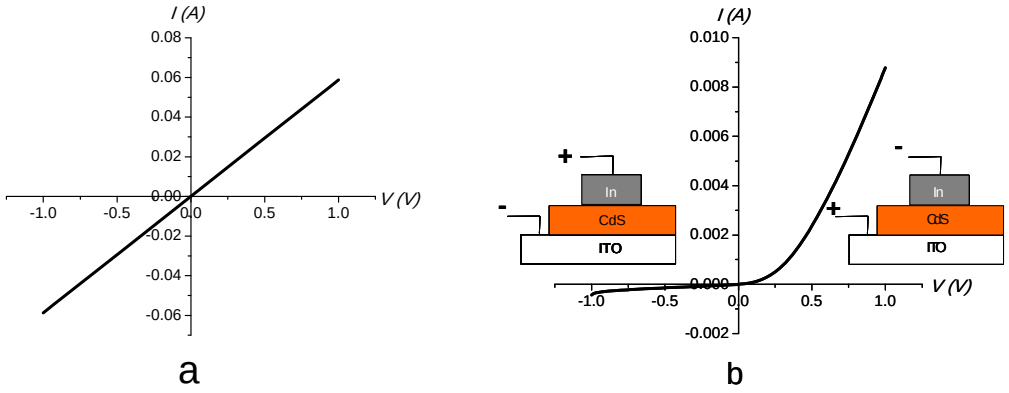


**Figure 5.3**: The *I-V* curves for post-growth annealed CdS/ITO contacted with In. a) $H_2 + N_2$ treated CdS displaying Ohmic behaviour (sample 97). b) Rectifying behaviour after annealing the CdS in an $O_2$ atmosphere (sample 75). The polarity of the electrodes used to record the *I-V* curve is shown. The field in this structure has the opposite sense to that in full CdTe/CdS solar cell structures.

*Post-growth annealed CdS/$SnO_2$ films*

The results of the *I-V* testing of In/CdS/$SnO_2$ structures both before and after post-growth annealing of the CdS in $O_2$ are shown in Figure 5.4a and Figure 5.4b respectively. While the as-grown structure is almost Ohmic, the oxidation has introduced rectifying behaviour. The appearance of this is contrary to Alamri's findings in which the CdS/$SnO_2$ remained Ohmic upon $O_2$ annealing. This is discussed in Section 5.2.4.

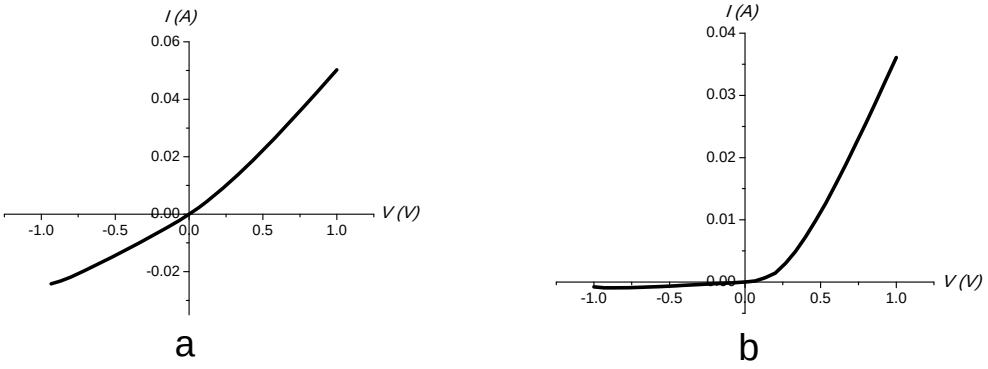


**Figure 5.4**: The *I-V* characteristics behaviour for the In/CdS/$SnO_2$ structure for a) as-grown, and b) post-growth oxidised CdS.

*Structural and compositional analysis of CdS/ITO*

The next stage was to investigate the compositional changes due to the post-growth oxidation of the CdS/ITO samples. The GIXRD results for as-grown and annealed CdS films are shown in Figure 5.5. It is seen from the figure that there was no detectable change in the composition before and after annealing i.e. no new peaks appeared. However, the preferred orientation of the annealed (hexagonal) CdS seems to be slightly affected. For example, the 002 orientation was more pronounced after annealing while the intensity for 103 slightly decreased.

Figure 5.6a shows a comparison of the In profiles. For both films there is evidence of In diffusion into the CdS from the ITO. However, for the annealed sample, the In concentration is higher and the diffusion has penetrated more deeply into the CdS.

Figure 5.6b shows the SIMS depth profiles of oxygen in both the non-treated and the treated CdS films. In both samples the curves are comparable: throughout the bulk of the films there is a low background signal which rises rapidly at the CdS/ITO interface. The apparent small peak at the layer surface may be genuine, but since such peaks are known to appear from plasma start-up artefacts in SIMS, this was further investigated by AES (Figure 5.7). While there was evidence of a small oxygen peak for the as-grown sample, AES showed the CdS surface was very significantly oxidised for case of the treated sample, the peak being > 3 times higher.

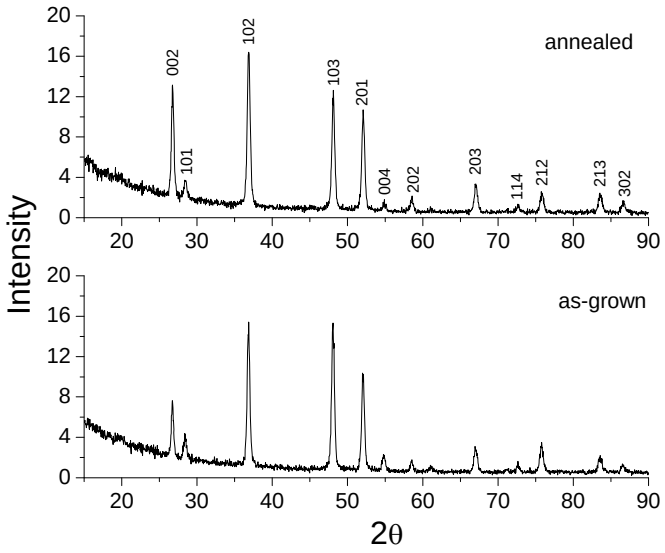


**Figure 5.5**: GIXRD for two CdS/ITO samples: annealed in $O_2$ (upper) and as-grown (lower) indexed as for the wurtzite phase of CdS. There is no evidence of a new phase forming after annealing. The samples were identical to samples 75 and 60 respectively (Table 5.1).

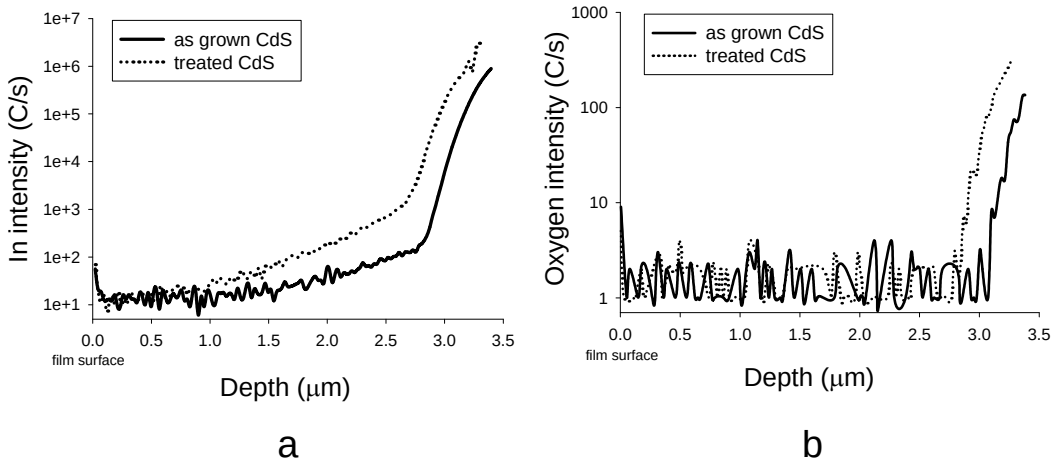


**Figure 5.6**: SIMS depth profiles of (a) In and (b) oxygen for as-grown and treated CdS/ITO films. (Displacement of the curves is due to minor differences in the CdS thickness at each sampling point).

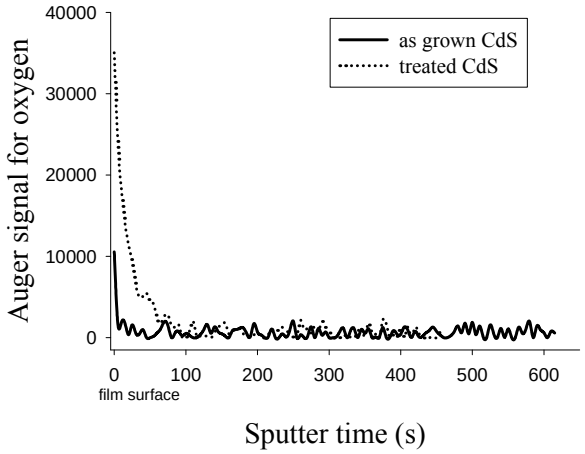


**Figure 5.7**: Auger depth profile for oxygen in both as-grown and treated CdS/ITO films. This confirms the presence higher concentration of oxygen on the surface of the annealed CdS.

### 5.2.4 Discussion

The pinhole test using Au contacts revealed that Delta Tech. ITO/glass substrates promoted CdS coverage that was superior to that for VisionTek. substrates. The increased pinhole density in the latter might be attributed to the following factors: a) The roughness of the ITO films. ITO is known to be rough, with spikes in the material being problematic for thin film device fabrication e.g. organic LED's. In this case differences in the manufacturing of the two substrates types might account for their different performance. VisionTek. ITO was seen to be considerably rougher than Delta Tech. ITO by SEM imaging, b) The influence of impurities on the CdS growth. For example, it has been postulated that out-diffusion of sodium from the glass influences CdS growth [3] (see Section 3.2). Differences in the ITO and glass may promote this for same substrate types, c) Water and carbon absorption may differ for the two, and influence the CdS growth [4].

Comparison of the resistance values for the structures displaying Ohmic behaviour was made (Table 5.2) to gain some insight into the validity of the Au rectification test and to gauge the influence of processing on the CdS and ITO. Generally, for all of the genuinely Ohmic In/CdS/ITO structures, the resistances varied only slightly, and were to a first approximation independent of

oxidation/reduction of the ITO and reduction of the CdS. Moreover, the resistances were comparable to those of Au/ITO control samples. The more significant difference (i.e. > 1 SD) was observed between samples 64 and 68 i.e. for CdS films grown on oxidised and reduced ITO, the latter being more conductive. While this finding would agree with the increase in conductivity expected from reduction, confirmation of the result could require more repeat runs to eliminate possible random error from substrate to substrate variation. Pinhole testing of sample 64 revealed a small number of dots which had Ohmic behaviour, this was attributed to defects in the CdS film. Since for a typical contact with pinholes the resistance was ~ 3 times higher than for a genuinely Ohmic part of the film, it was estimated that ~ 1/3 of the film area comprises pinholes. In fact this value was obtained from a dot near to the substrate edge where the CdS is known to be of low quality.

Having established that the CdS films of good quality could be identified and selected for experiments, the results of the *I-V* tests as a function of the processing are now discussed. It is a significant finding that none of the oxidising and reducing treatments applied to the ITO films prior to the CdS growth had any influence on the junction performance, which was always found to be Ohmic. Possible reasons for this are considered as follows: a) The oxidising and reducing conditions used were more severe (temperature and gas composition) than those used by Alamri [1] for which significant changes in the *I-V* curves were induced. It is therefore reasonable to assume that the invariant Ohmic behaviour was not due to insufficient processing. b) It has been considered whether heating the samples to the CdS growth temperature somehow normalized the condition of the ITO. However, since this heating takes place under a vacuum of ~ 0.5 Torr, significant re-oxidation is unlikely but not impossible.

Hence, direct testing of Alamri's [1] hypothesis (that annealing of CdS/ITO bilayers in air oxidised the underlying ITO) failed to confirm this as the cause of rectification for CdS grown on pre-oxidised ITO substrates. Nevertheless, rectification was easily obtained by repeating Alamri's oxidation test on complete bilayers. Furthermore, oxidation of CdS/$SnO_2$ bilayers also gave rectification, contrary to the findings of Alamri, whose samples remained Ohmic and were presumed to be more stable than those grown on ITO.

Of the physical tests performed on the oxidised CdS the most significant was the finding of an oxygen-rich surface layer by AES. This result is consistent with

reports from a number of authors [5-7] that oxidation of the CdS surfaces results in the formation of a CdO surface layer. CdO is a degenerate semiconductor (i.e. $n^+$-semiconductor) having a band gap close to that of CdS. The possibility that it is in fact the CdO/CdS junction that accounts for rectification is now explored with the aid of band diagrams for the interfaces in the In/CdO/CdS/ITO structure.

Figure 5.8a shows the band structure of isolated components as determined from the band gaps, work functions and electron affinities obtained from the references shown in Table 5.3. There is some disagreement in the literature concerning the $E_g$ of CdO. The direct $E_g$ varies in the range ~ 2.2-2.5 eV for thin films [8-14] however, as $E_g$ depends on the grain size [11], it can have higher values for CdO nanostructures e.g. up to 3.69 eV [15]. The value of CdO $E_g$ was chosen to be 2.4 eV in Figure 5.8a since values close to this were reported in the references mentioned above for thin films.

Using these data, a band diagram for the complete structure was proposed (using the principles outlined in Section 2.1) and is shown in Figure 5.8b. This diagram indicates that electrons may flow freely from both the CdS into the (degenerate) ITO and from the CdO into the In contact (the latter is confirmed by experiment [16]). However, electrons would face an energy barrier ($\phi_{CdO/CdS}$, see Figure 5.8b) when they flow from the CdO to the CdS: this is an $n^+$/n junction. In fact the polarity of the field of this junction is consistent with the sense of the rectification of the complete In/"CdS"/ITO junction identified by experiment and shown in Figure 5.3b.

| | CdS | CdO | ITO | In |
|---|---|---|---|---|
| Work function $\phi$ | [17] | [18] | [19] | [20] |
| Electron affinity $\chi$ | [21] | [18] | [22] | --- |
| Band gap $E_g$ | [21] | [6] | [23] | --- |

**Table 5.3**: The references from which the values of the parameters in Figure 5.8a were extracted.

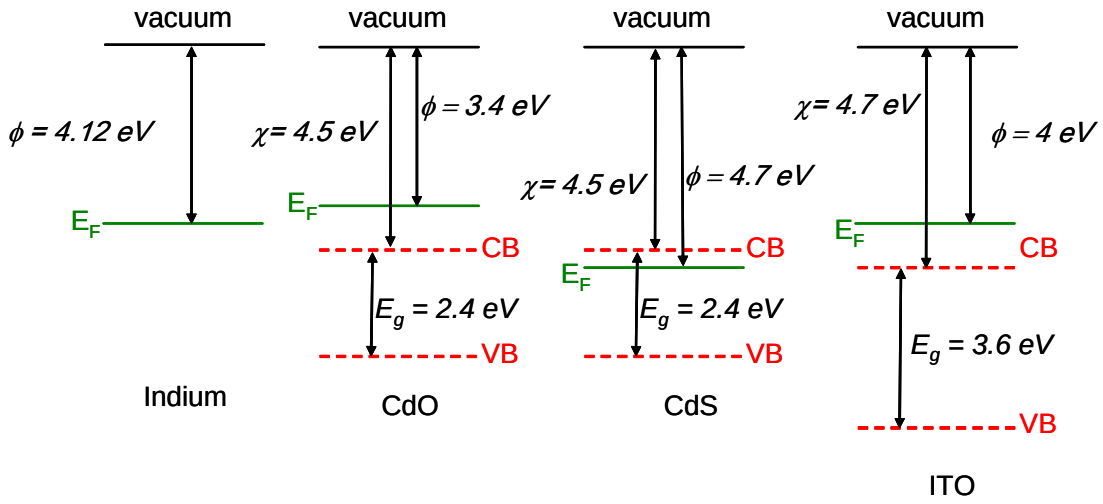


**Figure 5.8a**: The electronic details of each layer for the proposed structure of the annealed CdS, where *CB*, *VB*, $E_F$, $E_g$, $\chi$ and $\phi$ are the conduction band, valence band, Fermi level, band gap, electron affinity and work function respectively.

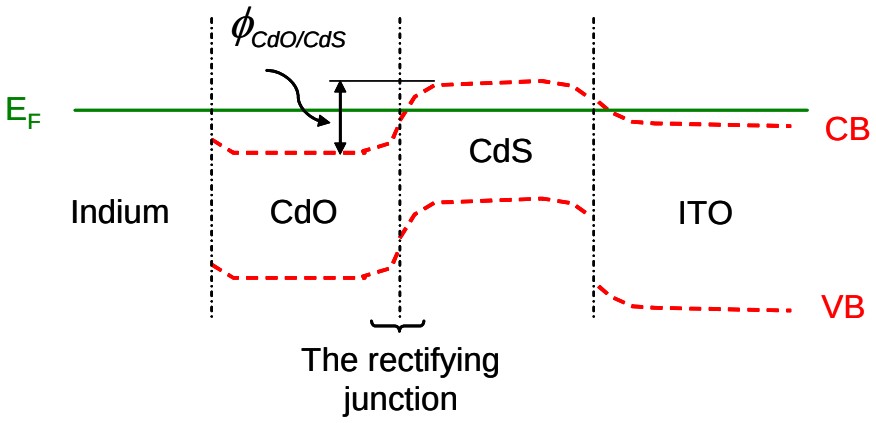


**Figure 5.8b**: Proposed band alignments of the In/CdO/CdS/ITO junctions.

It might therefore be concluded that Alamri's hypothesis that annealing of CdS/ITO modifies the ITO is insufficient to explain the oxidation induced rectification, and that formation of CdO is more likely explanation. Moreover, the finding here that oxidation induced rectification could be demonstrated for both CdS/ITO and CdS/$SnO_2$ supports the conclusion that the CdS is modified and not the buried CdS/TCO interface. (It is possible that Alamri's Ohmic result for CdS/$SnO_2$ was the result of pinholes in the CdS). Further evidence for this is that a recent study (employing photoelectron spectroscopy and sputtering depth profile to investigate the

band offset of the TCO/CdS interface) [24] has shown that post-growth oxidation of the CdS/ITO does not change the band alignment of the interface itself.

## 5.3 Rapid screening method for investigating the performance of devices as a function of i) CdTe thickness, and ii) the treatment of the CdS layer

### 5.3.1 Introduction

The thermal treatment of the CdS layers could lead to dramatic changes in not only the properties of the CdS but also the performance of the photovoltaic devices fabricated using the treated CdS. The severity of these changes is known to depend on the annealing conditions: the temperature, the duration and the ambient (see Section 3.3).

It is well known that for the case of the CdTe/CdS/TCO/glass solar cell, post-growth treatment of the CdTe layer with $CdCl_2$ increases performance. It is also known that heating of the structure (both the temperature and the duration) may influence interdiffusion at the CdTe/CdS interface, and that this also influences device performance, these two factors being interlinked. Moreover, the thickness of the CdTe also dictates the choice of thermal treatment conditions that are optimal for the $CdCl_2$ processing step. The overall situation is one in which there is a complex interaction between process variables. Accordingly, full optimisation of a processing route may require some hundreds of growth runs, taking months to complete.

Figure 1.4 and Table 1.1 in Section 1.2 summarise the improvement of performance of different kinds of solar cells during the last three decades. Surprisingly, the rate of development for the single junction devices is ~ 0.47 ± 0.04% per annum for all technologies. As a result there is a scope for rapid screening methodologies to be developed with the aim of reducing the number of samples required in order to fully explore a region of processing parameter space. Such methods may find application both with existing technologies, and for new and emerging thin film systems.

One particular embodiment of rapid screening is the use of a wedge-shaped sample in order to simultaneously explore a range of film thicknesses in a single processing run. This methodology was achieved by polishing the samples and has been used to study both III-V and II-VI materials [25]. However, the wedge-shaped samples can be achieved for those materials by chemical etching as well [26, 27]. It has been reported that chemical etching was used for the CdTe/CdS cells for the

purpose of characterisation using PL [28, 29] and grain size analysis [30]. However, this is the first report to the author's knowledge of the use of the bevel-etching in rapid screening for thin film PV device fabrication.

In this work the use of a bevelling method to produce CdTe/CdS samples having a range of CdTe thicknesses has been explored. Different growth conditions have been tested in this work to explore the validity of bevelling methodology as a means of rapid screening of the performance of CdTe solar cells. These methodologies were applied to all these kinds of cells in which the CdS had itself been processed differently i.e. with $N_2$, $H_2$ and $O_2$.

### 5.3.2 Fabricating the samples, and their results and discussion

This Section is divided into four main parts: the Preliminary Study, Bevel 1, Bevel 2, and Bevel 3. Each section starts with experimental details for the investigated samples, followed by the results and discussion. Section 5.3.2.1 represents a preliminary study done to choose the most suitable growth conditions for the samples used for bevelling / rapid screening methodology. Next, three different runs have been carried out using this methodology. They are denoted as Bevel 1, Bevel 2 and Bevel 3, and described and discussed in Sections 5.3.2.2, 5.3.2.3 and 5.3.2.4 respectively.

Throughout this Chapter devices were fabricated using 2 mm diameter circular dot contacts to the CdTe. In this way large numbers of device results were observed quickly to generate the systematic data sets reported here. It should be mentioned however that area under the dots was not isolated by scribing through the CdTe. When scribing is used it is generally thought to improve the reliability of *J-V* and efficiency measurements by eliminating edge collection and current leakage effects. However, to do this in the present work would have necessitated scribing around several hundred dots by hand. Hence it is to be expected that the *J-V* results shown here are subject to a systematic error, but to have scribed around the dots would itself have generated a random error from the difficulties in precisely scribing around each dot with an accurately defined circle.

#### 5.3.2.1 Preliminary study to test the performance uniformity across samples

*Experimental (preliminary study)*

The aim of this Section was to establish a set of conditions suitable for the production of appropriate samples for bevelling / rapid screening. The requirements were the uniformity over a given plate and relatively low roughness (the latter being a requirement for bevel etching).

Table 5.4 summarises the growth and treatment conditions for the thirty samples fabricated in this preliminary study using both CBD and sputtered CdS. 5×5 cm Pilkington TEC 8 and TEC 15 glass plates served as substrates. The CdS film was deposited by two techniques: CBD and sputtering. CBD CdS samples were grown by the author at Cranfield University [31] (see Section 4.2.1 for details of deposition) or else were RF sputtered from a 5N target in Durham. Sputtering took place at room temperature in an ambient of 5 % $O_2$/Ar, since sputtering without $O_2$ led to pinholey films. The thickness of the CdS films was ~ 150-200 nm in both cases. The post-growth annealing of the CdS was in either $N_2$, $H_2$ or $O_2$ (and following this the CdTe was grown). Annealing was performed under pure flowing gas (50 sccm) or at 3 Torr for 5 minutes. The procedure was to set the substrate temperature at 400°C with the source heater and the sample in vacuum. Introduction of the gas flow caused a rapid drop in temperature to as low as 270°C, this recovering to 350°C at the end of a run.

The CdTe film was deposited by CSS for all samples. However, two different sets of growth conditions were embraced. In the first, CdTe was grown in a flow of $O_2$ at ~ 2 Torr with the source temperature being held at ~ 600°C and the average substrate temperature being ~ 520°C. In the second, a higher static pressure of $N_2$ (~ 100 Torr) was used, but the temperatures were similar. The thickness of the CdTe films was ~ 9 μm in both cases.

Each 5×5 plate denoted by a three figure reference number was cut into four equal quarters denoted by a fourth number. Samples xxx-1, 2, 3 and 4 were then each subjected to different $CdCl_2$ treatment (layer thickness, time and temperature) in order to achieve optimum results for each plate. Finally, the substrates were contacted by etching the CdTe surface in nitric/phosphoric acid (N-P etch – see Section 4.3.1f) for 10 seconds followed by evaporation of 2 mm diameter Au dots. The dot contacts were applied on a 4 mm square grid, there being 25-36 dots on each ~ 25×25 mm sample.

| Sample | Substrate | CdS growth technique | CdTe growth | | $CdCl_2$ treatment | | |
|---|---|---|---|---|---|---|---|
| | | | Gas | Pressure (Torr) | Thickness (nm) | *T* (°C) | Time (min) |
| 361-1 | TEC8 | CBD | $O_2$ | 2 (flow) | 200 | 425 | 10 |
| 362-1 | TEC15 | CBD | $O_2$ | 2 (flow) | 200 | 425 | 10 |
| 361-2 | TEC8 | CBD | $O_2$ | 2 (flow) | 0 | 0 | 0 |
| 362-2 | TEC15 | CBD | $O_2$ | 2 (flow) | 0 | 0 | 0 |
| 361-3 | TEC8 | CBD | $O_2$ | 2 (flow) | 50 | 400 | 5 |
| 362-3 | TEC15 | CBD | $O_2$ | 2 (flow) | 50 | 400 | 5 |
| 361-4 | TEC8 | CBD | $O_2$ | 2 (flow) | 50 | 400 | 10 |
| 362-4 | TEC15 | CBD | $O_2$ | 2 (flow) | 50 | 400 | 10 |
| 373-1 | TEC8 | CBD | $N_2$ | 100 (static) | 0 | 0 | 0 |
| 374-1 | TEC15 | CBD | $N_2$ | 100 (static) | 0 | 0 | 0 |
| 373-2 | TEC8 | CBD | $N_2$ | 100 (static) | 50 | 400 | 10 |
| 374-2 | TEC15 | CBD | $N_2$ | 100 (static) | 50 | 400 | 10 |
| 373-3 | TEC8 | CBD | $N_2$ | 100 (static) | 200 | 425 | 10 |
| 374-3 | TEC15 | CBD | $N_2$ | 100 (static) | 200 | 425 | 10 |
| 373-4 | TEC8 | CBD | $N_2$ | 100 (static) | 100 | 400 | 10 |
| 374-4 | TEC15 | CBD | $N_2$ | 100 (static) | 100 | 400 | 10 |
| 440-1 | TEC8 | Sputtering | $O_2$ | 2 (flow) | 200 | 400 | 2 |
| 439-1 | TEC15 | Sputtering | $O_2$ | 2 (flow) | 200 | 400 | 2 |
| 440-2 | TEC8 | Sputtering | $O_2$ | 2 (flow) | 0 | 0 | 0 |
| 439-2 | TEC15 | Sputtering | $O_2$ | 2 (flow) | 0 | 0 | 0 |
| 440-3 | TEC8 | Sputtering | $O_2$ | 2 (flow) | 50 | 400 | 10 |
| 439-3 | TEC15 | Sputtering | $O_2$ | 2 (flow) | 50 | 400 | 10 |
| 443-1 | TEC8 | Sputtering | $N_2$ | 100 (static) | 0 | 0 | 0 |
| 442-1 | TEC15 | Sputtering | $N_2$ | 100 (static) | 0 | 0 | 0 |
| 443-2 | TEC8 | Sputtering | $N_2$ | 100 (static) | 350 | 400 | 20 |
| 442-2 | TEC15 | Sputtering | $N_2$ | 100 (static) | 350 | 400 | 20 |
| 443-3 | TEC8 | Sputtering | $N_2$ | 100 (static) | 50 | 400 | 10 |
| 442-3 | TEC15 | Sputtering | $N_2$ | 100 (static) | 50 | 400 | 10 |
| 443-4 | TEC8 | Sputtering | $N_2$ | 100 (static) | 500 | 400 | 20 |
| 442-4 | TEC15 | Sputtering | $N_2$ | 100 (static) | 500 | 400 | 20 |

**Table 5.4**: Summary of the growth and treatment conditions of samples tested in the preliminary bevel / rapid screening study. CdS was grown by either CBD or sputtering. CdTe was grown in either high pressure of $N_2$ or low pressure of $O_2$. Details of the various $CdCl_2$ treatment conditions applied to each sample are also shown.

After investigating the runs above, the growth conditions for the most efficient cells were chosen to fabricate three other samples. The aim of this set of devices was to test the performance uniformity across each sample. 5×5 cm Pilkington TEC 8 glass served as substrates for all runs. However, only ~ 2.5×2.5 cm was cut then from

the central part of each 5×5 cm plate before processing. The growth and treatment conditions used for this set of cells are shown in Table 5.5. The growth procedure for each layer has been already described previously in this Section.

| Sample | CdS | CdTe | | $CdCl_2$ | | |
|---|---|---|---|---|---|---|
| | | Gas | Pressure (Torr) | Thickness (nm) | *T* (°C) | Time (min) |
| 445 | sputtering | $N_2$ | 100 | 350 | 400 | 20 |
| 451 | sputtering | $N_2$ | 100 | 0 | 0 | 0 |
| 454 | CBD | $O_2$ | 2 | 50 | 400 | 10 |

**Table 5.5**: Growth conditions and techniques used to grow samples tested in order to investigate the performance uniformity.

*Results and discussion (preliminary study)*

The performance of all devices described in Table 5.4 was tested and summarised in Table 5.6 in order to find the best combination of growth conditions.

The table shows that cells fabricated on TEC 15 glass (e.g. samples 362-2 and 362-3) had a higher incidence of short-circuits, irreproducibility and low performance compared to those made on TEC 8 (e.g. samples 361-2 and 361-3): the latter was therefore adopted for this work. Moreover, particular combination of CdS and CdTe growth methods were found to give higher PV performance than others. CBD CdS has better performance with CdTe:$O_2$ (low pressure), however, sputtered CdS performs better with CdTe:$N_2$ (high pressure). An explanation of this behaviour is that the intermixing of the CdTe with the CdS was insufficient in the case of "low-pressure" growth conditions (growth time is 6 minutes). However with "high-pressure" route, in which growth duration was 50 minutes, the intermixing was sufficient. Major [32] studied the performance of the CSS-CdTe/CSS-CdS devices as a function of the growth pressure of the CdTe, and found that devices grown at high pressure (200 Torr compared to 2 Torr) had better performance. This improvement was attributed to the longer deposition time resulting in more intermixing between the CdS and the CdTe. The same argument can be used for the behaviour of CBD CdS and "high pressure" grown CdTe, it can be assumed that over-intermixing between

layers is the reason for the poor performance of this kind of junctions. Romeo *et al.* [33] reported that CBD-CdS can be totally consumed during the growth and the treatment of the CdTe due to excessive intermixing, leading to poor performance.

| sample | Average of performance | | | | Best $\eta$ | SC |
|---|---|---|---|---|---|---|
| | $\eta$ (%) | $FF$ (%) | $J_{sc}$ (mA/cm$^2$) | $V_{oc}$ (V) | | |
| 361-1 | Totally delaminated | | | | | |
| 362-1 | Totally delaminated | | | | | |
| 361-2 | 2.7 | 38.6 | 10.9 | 0.61 | 3.7 | 1/23 |
| 362-2 | 2.7 | 37.3 | 11.6 | 0.6 | 4 | 7/27 |
| 361-3 | 1.9 | 32.5 | 9.5 | 0.6 | 3.3 | 1/25 |
| 362-3 | 1.8 | 31.8 | 9.3 | 0.6 | 3.1 | 10/29 |
| 361-4 | 6.3 | 51.1 | 17.6 | 0.67 | 8.8 | 1/23 |
| 362-4 | 3.5 | 48.4 | 11.3 | 0.62 | 6.9 | 1/35 |
| 373-1 | $\eta << 1\%$ | | | | | |
| 374-1 | $\eta << 1\%$ | | | | | |
| 373-2 | $\eta << 1\%$ | | | | | |
| 374-2 | $\eta << 1\%$ | | | | | |
| 373-3 | Totally delaminated | | | | | |
| 374-3 | Totally delaminated | | | | | |
| 373-4 | $\eta << 1\%$ | | | | | |
| 374-4 | $\eta << 1\%$ | | | | | |
| 440-1 | Totally delaminated | | | | | |
| 439-1 | Totally delaminated | | | | | |
| 440-2 | $\eta << 1\%$ | | | | | |
| 439-2 | $\eta << 1\%$ | | | | | |
| 440-3 | $\eta << 1\%$ | | | | | |
| 439-3 | $\eta << 1\%$ | | | | | |
| 443-1 | 3.7 | 50.9 | 10.8 | 0.66 | 5.2 | 1/29 |
| 442-1 | 0.8 | 32 | 4.7 | 0.55 | 1.9 | 2/24 (Partially delaminated) |
| 443-2 | 6.2 | 54.6 | 15.8 | 0.7 | 8.8 | 0/30 |
| 442-2 | 0.6 | 29.5 | 5.3 | 0.43 | 1.2 | 8/19 (Partially delaminated) |
| 443-3 | 5.1 | 47.8 | 15.9 | 0.66 | 6.4 | 7/25 |
| 442-3 | 1 | 29.8 | 7.4 | 0.44 | 2.2 | 9/28 |
| 443-4 | 4.4 | 45.2 | 14.1 | 0.67 | 7.3 | 1/25 |
| 442-4 | Totally delaminated | | | | | |

**Table 5.6**: The working parameters of devices described in Table 5.4. SC is the ratio of short circuited dots to the total number of cells in each sample. The best average performance were found for samples 361-4 (CSS CdTe with $O_2$/CBD CdS) and 443-3 (CSS CdTe with $N_2$/sputtered CdS). Material was therefore produced using similar growth conditions for use in the rapid screening studies, shown in Table 5.7.

Although the $CdCl_2$ treatment was not fully optimised for these devices, it can be seen from the results (in Table 5.6) that it affected the performance. For example, samples 361-1, 362-1 and 442-4 were completely delaminated due to the over treatment. On the other hand, under-processed samples had poor performance such as samples 361-3 and 362-3.

Based on the results presented in Table 5.6, devices number 361-4 ($CdTe:O_2$/CBD-CdS) and 443-3 ($CdTe:N_2$/sputtered-CdS) had the best *average* PV performance. Therefore, these devices were reproduced and denoted as 454 and 445 respectively as shown in Table 5.5. Cell number 451 (Table 5.5) was fabricated in order to test the effect of the $CdCl_2$ treatment on the performance uniformity as explained below.

The average and the standard deviation of the performance parameters for all dots in each sample described in Table 5.5 were calculated, allowing examination of the performance across each plate. These results are shown in Table 5.7.

| **Sample** | $\eta$ **(%)** | | $FF$ **(%)** | | $J_{sc}$ **(mA/cm$^2$)** | | $V_{oc}$ **(V)** | |
|---|---|---|---|---|---|---|---|---|
| | **Avg** | **SD** | **Avg** | **SD** | **Avg** | **SD** | **Avg** | **SD** |
| 445 ($CdTe:N_2$/sputtered-CdS) | 3.6 | 1.6 | 56.6 | 3.3 | 9.6 | 2.9 | 0.64 | 0.06 |
| 451 (as 445 but without $CdCl_2$ treatment) | 1.5 | 0.5 | 48.1 | 2.9 | 4.9 | 1.5 | 0.6 | 0.03 |
| 454 ($CdTe:O_2$/CBD-CdS) | 5 | 0.6 | 51.8 | 2.4 | 16.1 | 1.2 | 0.6 | 0.02 |

**Table 5.7**: The average and the standard deviation of all working parameters for cells described in Table 5.5. It shows that the performance of cells comprising CBD CdS combined with $CdTe:O_2$ (sample 454) is more uniform than the performance of other cells.

It is seen in the table that the performance of sample 445 was non-uniform. The SD of $\eta$ was ~ 44 % of its average value. The possibility that the non uniformity issue was due to the $CdCl_2$ treatment was examined by testing the performance of an identical sample but without treatment (sample 451, see Table 5.5). However, the improvement in the performance was not significant i.e. the efficiency SD was ~ 33 %

of the average value for this sample. Another issue with these samples (445 and 451) was that they comprised CdTe layers grown at high pressure, which results in large grains and correspondingly rough films: this made them unsuitable for bevelling (see Section 5.3.2.4). The performance non uniformity of rough CdTe was confirmed by further investigation (see results of Bevel 2 and Bevel 3 below).

In contrast, the SD of $\eta$ for sample 454 (see Table 5.7) was 12 % of its average value i.e. more uniform than the other two samples above. Furthermore, use of $O_2$ in the growth ambient produces smoother CdTe films by reducing the grain size [34]. Therefore, the growth conditions of this sample were chosen for the rest of the study.

#### 5.3.2.2 Bevel 1: trial run using CSS CdS

*Experimental (Bevel 1)*

It is important to remark that this run was done before the preliminary study described in Section 5.3.2.1, and the growth conditions were not therefore optimised for uniformity.

The experimental details of both growth and processing for these samples are described in detail below and are summarised in Table 5.8.

CSS CdS (nominal thickness 150 – 200 nm) was grown on Pilkington TEC 8 5×5 cm substrates, from which 2.5×2.5 cm central parts were cut for device processing. It was grown using 5N material (Alfa-Aesar) under 1.5 Torr of $O_2$ on substrates held at 530°C, the source being held at 650°C.

Post-growth annealing of the CdS was conducted in ~ 3 Torr of either $O_2$, $N_2$, or $H_2$, with each run being at 400°C for 4 minutes. This annealing was done in-situ in the CdTe growth chamber, with heating being provided by the substrate heater only. CdTe was grown under 200 Torr of $N_2$ using 5N Alfa Aesar material at an average substrate temperature of 530°C.

After bevelling (which is described in detail in Section 4.3.2), $CdCl_2$ processing was done by evaporating 200 nm of $CdCl_2$ followed by annealing at 400°C for 10 minutes in air. Back contact arrays comprising ~ 25 – 36 × 2mm diameter dots were deposited onto the CdTe surfaces after etching in "N-P" solution [35] for 10 seconds. These contact dots were measured without scribing.

| Step | Bevel 1 | Bevel 2 | Bevel 3 |
|---|---|---|---|
| 1 | CdS deposition: by CSS under 2 Torr of $O_2$ | CdS deposition: by CBD | CdS deposition: by CBD |
| 2 | Post-growth CdS annealing: 3 Torr of either i) $N_2$, ii) $H_2$ or iii) $O_2$ at a nominal temperature of 400°C for 4 minutes | Post-growth CdS annealing: 3 Torr of either i) $N_2$, ii) $H_2$ or iii) $O_2$ at a nominal temperature of 400°C (see Section 5.3.2.1) for 5 minutes | Post-growth CdS annealing: 3 Torr of either i) $N_2$, ii) $H_2$ or iii) $O_2$ at a nominal temperature of 400°C (see Section 5.3.2.1) for 5 minutes |
| 3 | CdTe: CSS in 200 Torr of $N_2$ | CdTe: CSS in 2 Torr of $O_2$ | CdTe: CSS in 2 Torr of $O_2$ |
| 4 | Bevel CdTe | Bevel CdTe | 50 nm of $CdCl_2$, annealed at 400°C for 25 minutes |
| 5 | 200 nm of $CdCl_2$, annealed at 400°C for 20 minutes | 50 nm of $CdCl_2$, annealed at 400°C for 10 minutes | Bevel CdTe |
| 6 | N-P etch and matrix of dot contacts | N-P etch and matrix of dot contacts | N-P etch and matrix of dot contacts |

**Table 5.8**: The growth and processing steps used in the bevelling / rapid screening experiments. For each of the three sets, the CdS was annealed in neutral, reducing and oxidising conditions. Bevel 1 was a trial run using cells made with CSS CdS. Bevel 2 and Bevel 3 were undertaken with devices made on CBD CdS which had better uniformity and gave clearer results. Theses two differ in the order in which the bevelling and $CdCl_2$ treatment were applied (steps 4 and 5).

The CdTe thickness at each dot position was measured with a stylus profiler. In order to maximize the number of CdTe thickness values investigated, the matrix was applied at an offset angle of ~ 10°, see Figure 4.4. *J-V* characteristics were measured under approximate AM1.5 conditions (Oriel solar simulator, 1000 W/m$^2$). SEM was used to record images of the surface of the CdTe.

*Results and discussion (Bevel 1)*

The working parameters (i.e. $\eta$, $FF$, $J_{sc}$, $V_{oc}$) extracted from the *J-V* analyses of all samples are presented in Figure 5.9 as functions of the CdTe thickness. Although there is some scatter, there are some clear trends in the behaviour of efficiency with thickness, and these reflect the trends in $FF$, $J_{sc}$ and $V_{oc}$ responsible

for them. Prior to describing the specific behaviour of each of the cell sets processed in $N_2$, $H_2$ and $O_2$ it is therefore necessary to outline the principles responsible for the variation in *FF*, $J_{sc}$ and $V_{oc}$ with thickness with reference to the influence of both shunt and series resistances for the device dots. It was explained in Section 2.8 that both series and shunt resistances ($R_s$ and $R_{sh}$ respectively) may affect the *FF* because they change the "squareness" of the *J-V* curve. Although the back contact of the CdTe cell is thought to dominate $R_s$, the bulk material (i.e. CdTe) may also influence its value. The values of $R_s$ and $R_{sh}$ may increase upon increasing the CdTe thickness due to the bulk material itself and also a reduced incidence of shunting (e.g. pinholes). Hence, for devices located at the thick part of the bevelled film, it can be generally assumed that both $R_s$ and $R_{sh}$ have relatively high value while these values decrease at areas of thin CdTe film. This may change the *FF* across the bevelled sample as the *FF* increases with both increasing $R_{sh}$ and decreasing $R_s$, and vice versa. The trade-off between these resistances may be the reason for having relatively high *FF* for thick and thin parts of some bevelled samples (see for example the *FF* data for the sample in which CdS was treated in $N_2$ in Figure 5.9). The $V_{oc}$ value depends on $R_{sh}$ and the $CdCl_2$ treatment. This means that $V_{oc}$ is likely to have high values at thick parts compared to thin parts due to the absence of leakage paths. However, if the $CdCl_2$ treatment is sufficient to treat only the thin part of the sample, then $V_{oc}$ may be higher in this part than the thick part (see results of Section 5.3.2.3 for more details about the $CdCl_2$ effects). The increase in $J_{sc}$ is expected to take place at the thin part due to shunting paths and pinholes (see later). Nevertheless, $J_{sc}$ may also depend on the $CdCl_2$ treatment as the latter may affect the position of the junction, which as a result affects the photocarrier collection as reviewed in Section 3.4. It is worth mentioning again that the effects discussed above might be masked by the high level of scattering for results shown in Figure 5.9.

It is expected that the sample for which the CdS was post-growth annealed in $O_2$ will have retained the characteristics of the as-grown sample, and its behaviour shall be described first. It is most striking that as the thickness of CdTe decreases below ~ 3 μm, the efficiency apparently increases. This behaviour is dominated by an increase in the $J_{sc}$ values, with unexpectedly high current values being reached for the lowest thicknesses – this being accompanied by a drop in shunt resistance ($R_{sh}$), as shown in Table 5.9. It may be concluded that for thicknesses < 3 μm the CdTe is subject to shunting, and this results in high leakage currents. Investigation by SEM

shown in Figure 5.10 for devices ~ 1 μm thick did not reveal any physical pinholes, and so it is presumed that the shunting is due to materials inhomogeneities e.g. grain boundaries or perhaps bad grains with non-average properties.

For samples with CdS annealed in $N_2$, the device working parameter had similar behaviour to that observed for $O_2$ annealing i.e. an apparent increase in both $\eta$ and $J_{sc}$ for CdTe thickness < 3 μm (see Figure 5.9). This is expected since the CdS itself was grown under $O_2$ at ~ 530°C, and the annealing under $N_2$ at 400°C should not be significant.

The samples having CdS annealed with $H_2$ did however display differences from those annealed with $O_2$ and $N_2$. Firstly it should be pointed out that the greater scatter of data for the $H_2$ samples is attributed to local variability in the CdS thickness (see later). Overall, the device results for $H_2$ show a general increase in the apparent efficiency and $J_{sc}$ values with decreasing thickness. There is also a corresponding drop in *FF*, but the increase in $J_{sc}$ is not so marked as for the other cells. The general conclusion that the behaviour of these cells is dominated by leakage remains for the case of $H_2$ annealing. Nevertheless, the samples treated in $H_2$ do show a trend to slightly higher $V_{oc}$ values than for those annealed in $N_2$ and $O_2$. Moreover, for the $H_2$ samples, there is a trend to increasing $V_{oc}$ with increasing thickness, although the high degree of scattering in the data does not allow this to be stated as a firm conclusion.

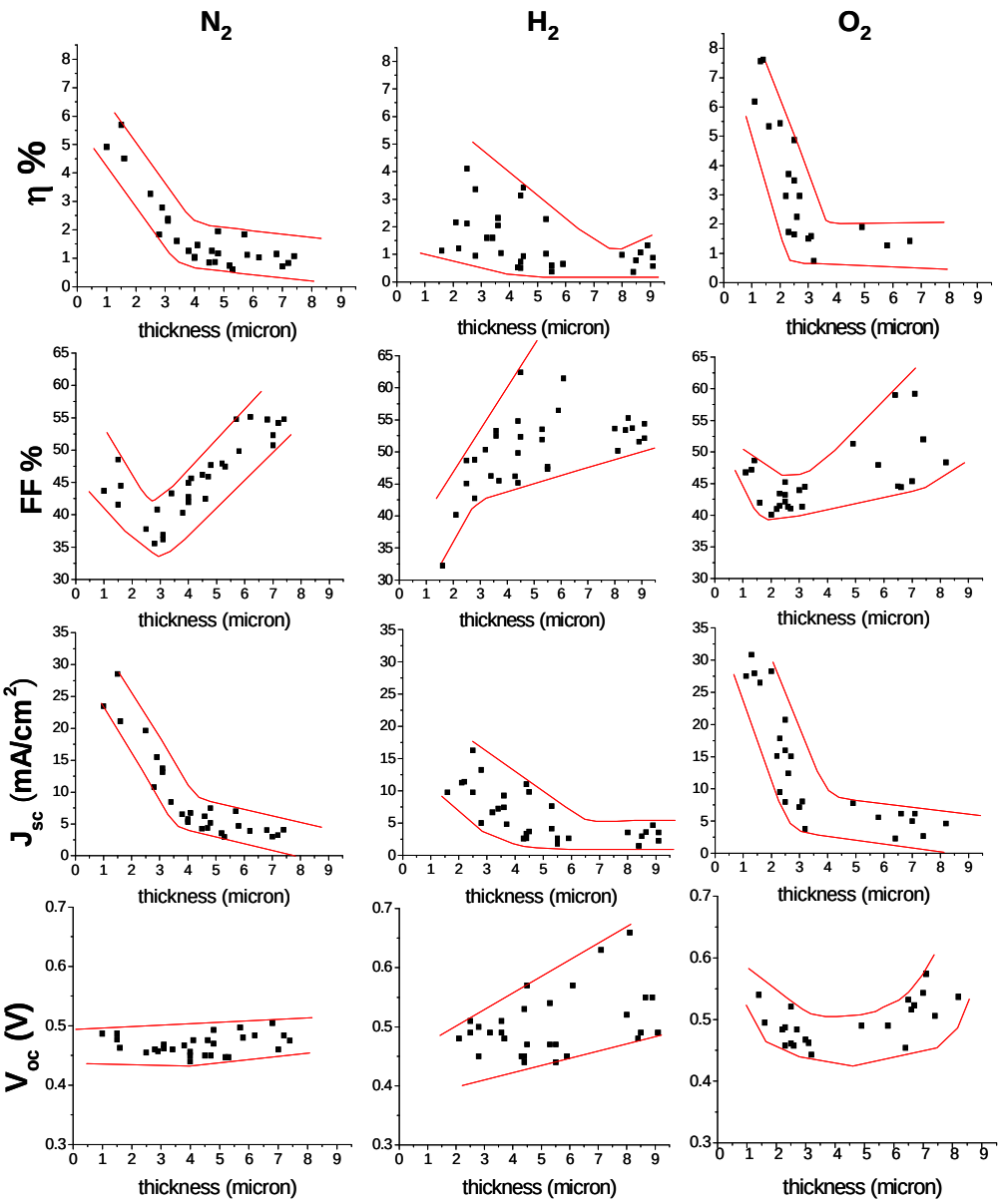


**Figure 5.9**: Working parameters of the solar cells fabricated using CdS annealed in $N_2$, $H_2$ and $O_2$ (Bevel 1). The cells were bevelled, and each graph therefore shows the variation of a parameter with the thickness of the CdTe. The guide lines indicate the spread of the data.

| Gas used for treating CdS | CdTe thickness (μm) | $R_{sh}$ ($\Omega.cm^2$) |
|---|---|---|
| $N_2$ | 7.4 | 4417 |
| | 4.1 | 156 |
| | 1 | 84 |
| $H_2$ | 8.6 | 1189 |
| | 5.3 | 397 |
| | 2.5 | 134 |
| $O_2$ | 8.2 | 442 |
| | 4.9 | 199 |
| | 1.4 | 103 |

**Table 5.9**: Variation of shunt resistance ($R_{sh}$) with thickness for selected cells (from the Bevel 1 set) fabricated on plates having CdS annealed in $N_2$, $H_2$ and $O_2$ environments. There is a clear trend to shunting for the lowest thicknesses.

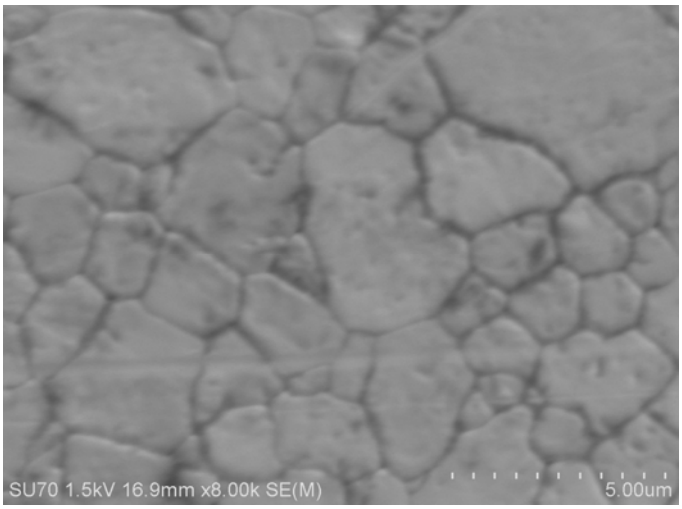


**Figure 5.10**: SEM image for a CdTe film from the "Bevel 1" sequence at a position having a thickness of ~ 1 μm. It does not show physical pinholes, which suggests that shunting at thin parts of the CdTe film is due to material inhomogeneities.

The scatter of data in Figure 5.9 was attributed to the variation in the CdS thickness and the high roughness of both CdS and CdTe films. It has been noticed that the thickness of the CSS CdS varies across the sample i.e. it is always significantly thicker at the centre of the sample than at the edges. Moreover, since the substrate temperature in the CSS technique is high, the CdS grain size and, therefore, the

roughness of the layers created by this method are always greater than for other techniques using lower deposition temperature such as CBD [36, 37]. To compound this, applying relatively high *pressure* during the growth of the CdTe causes a substantial increase in the grain size [38]. Large grains are shown in Figure 5.11 for a CdTe sample grown in 200 Torr of $N_2$ and these layers are correspondingly rough.

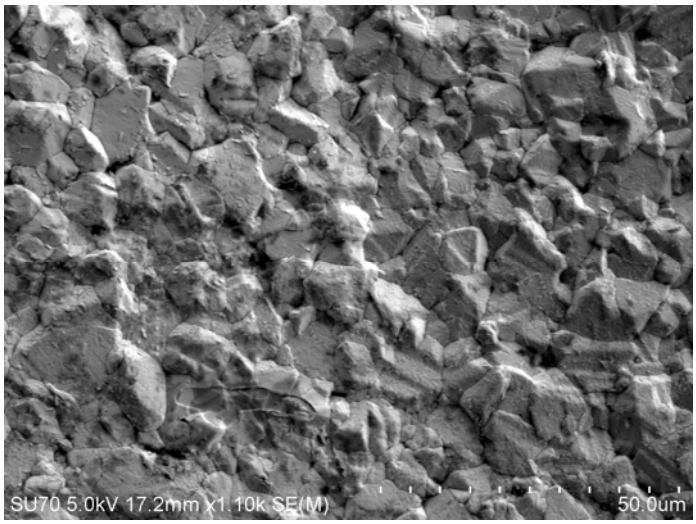


**Figure 5.11**: SEM image for a CdTe film grown at 200 Torr of $N_2$ as used in the "Bevel 1" sequence. The grain size (up to ~ 10 μm) is relatively large and is associated with high roughness.

Due to the level of scattering in the results of the Bevel 1 experiment, it was decided to repeat the experiment after developing smoother samples. This was achievable by modifying the growth conditions of each layer of the devices as explained in the preliminary study in Section 5.3.2.1. The modified conditions were used in both the Bevel 2 and Bevel 3 experiments as described below. One outcome of this was to generate data sets with less scatter than in Bevel 1 and hence reveal details of the effects of $CdCl_2$ treatment more clearly.

#### 5.3.2.3 Bevel 2: device with CBD CdS and with $CdCl_2$ applied after bevelling

*Experimental (Bevel 2)*

This experiment was performed subsequent to the preliminary study in Section 5.3.2.1. Bevel 2 used CBD CdS in an attempt to reduce the scatter in data observed in Bevel 1, which was presumed to arise from the use of (non-uniform) CSS CdS. The CdTe roughness was also reduced by the use of low pressure growth with $O_2$ present. The steps of fabricating the samples are outlined in Table 5.8 and are similar to those described in Section 5.3.2.1. However, in Bevel 2 treating the CdS was undertaken by using the lower heater (source heater, see Section 5.3.2.1) while it was done by using the upper heater in Bevel 1. Also light biased (1 sun) EQE curves were obtained for these samples by the author using a Bentham system at Glyndŵr University.

*Results and discussion (Bevel 2)*

Figure 5.12 shows the working parameters as functions of the CdTe thickness. There is a clear reduction in the scatter of data points obtained compared to that in Figure 5.9.

The efficiency curves each show a maximum response for a value of CdTe thickness of ~ 3 μm, irrespective of the treatment applied to the CdS. Examination of Figure 5.12 indicates that these curves are dominated by the behaviour of $J_{sc}$, which generally shows a peak at ~ 3 μm also. For thickness values >3 μm, $\eta$ decreases, and this is the general behaviour for $FF$, $J_{sc}$ and $V_{oc}$ also.

The superior homogeneity of samples used in Bevel 2 generated results with less scatter, which allowed more details of the $CdCl_2$ treatment to be revealed. The factors that may affect the variation of the cell working parameters were discussed in Section 5.3.2.2. The same argument can be used to discuss the results shown in Figure 5.12. However, the peaks shown in the Figure suggest that the results were controlled by the $CdCl_2$ treatment (see below) rather than the CdTe thickness. For example, the behaviour of $J_{sc}$ implies that leakage current might have a role in the increase of the values at thin parts, but the fact that $J_{sc}$ (as other parameters) decreased for CdTe thickness < 3 μm dismisses this speculation. The dominance of leakage current in $J_{sc}$ would have resulted in a continuous increase of $J_{sc}$ with decreasing thickness i.e. peaks would not appear in the curves, like the results of Bevel 1 shown in Figure 5.9.

These findings indicate that a CdTe thickness of ~ 3 μm is the optimum for the $CdCl_2$ processing conditions used. While the exact concentration profile resulting from this diffusion has not been measured, it might be speculated that the profile is optimal for 3 μm for CdTe i.e. it generates the junction position that gives the best collection performance. It may also be inferred that for thicknesses greater than 3μm, the extent of diffusion is insufficient to form a junction with a maximum collection efficiency i.e. the cell is under processed. Moreover, for thicknesses less than 3μm, this $CdCl_2$ treatment gives over processed cells. This was explored further by light biased EQE and it was found that the thicker parts of the cells had buried junction behaviour (see Section 2.7), while the optimum thicknesses had normal behaviour as illustrated in Figure 5.13. The observation that the efficiency is dominated by $J_{sc}$ is consistent with this.

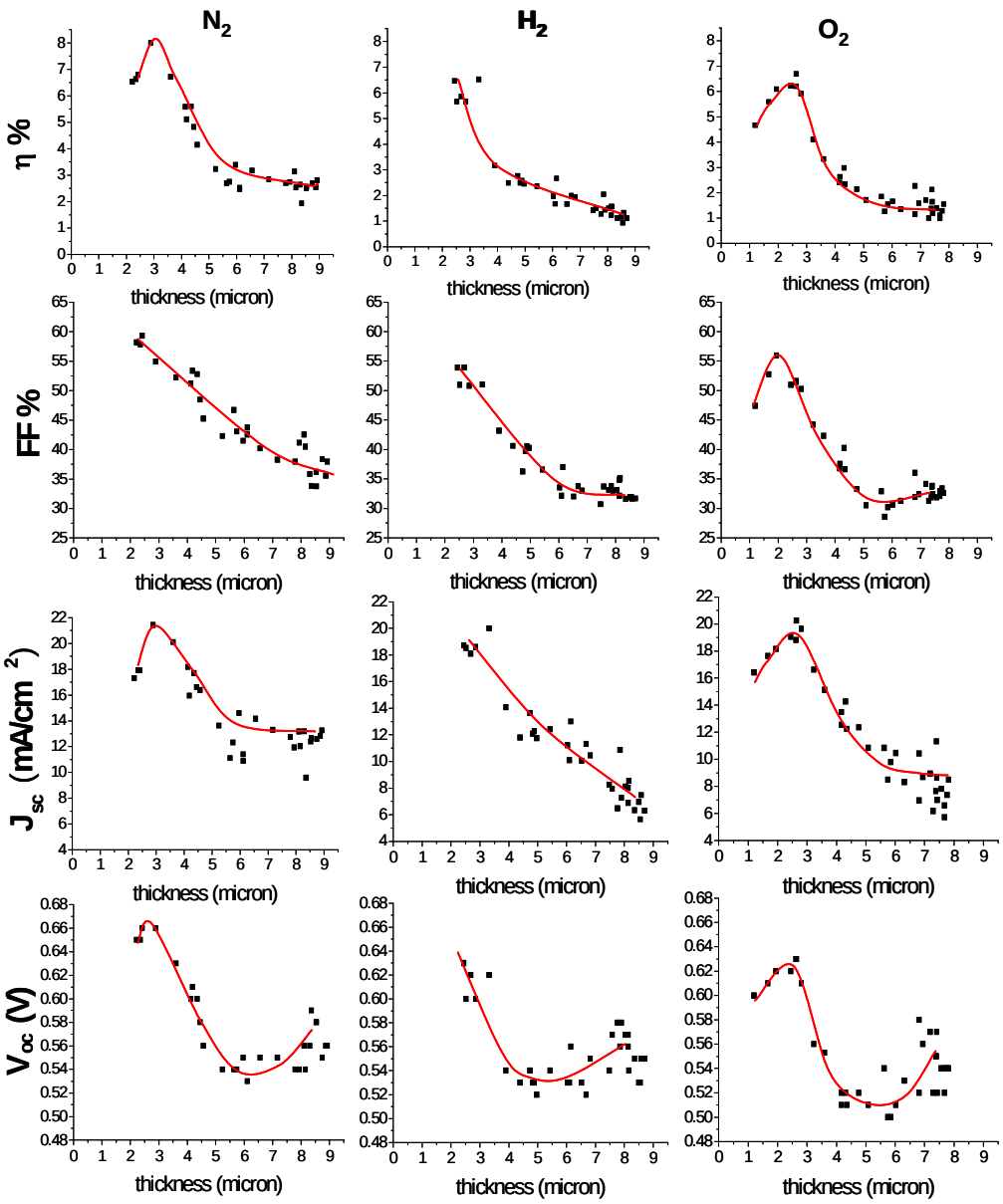


**Figure 5.12**: Working parameters of the solar cells used in Bevel 2 experiment. The lines indicate the general trend of the data.

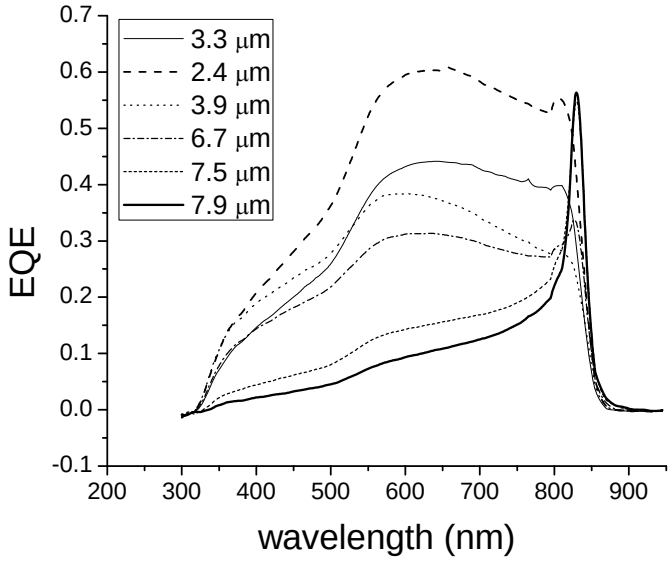


**Figure 5.13**: Light biased EQE data from dot contacts corresponding to different CdTe thicknesses across the same bevelled sample ($H_2$ annealed CdS-based sample from Bevel 2) . It shows a typical buried junction EQE curves for thick parts of CdTe, indicating insufficient $CdCl_2$ treatment for these areas.

The behaviour for high CdTe thickness values (Figure 5.12) is now described: Firstly in this region all of the graphs show increased scatter. Examination of the roughness data (Figure 5.14) indicates that this could be due to the increased roughness of the thicker parts of the samples. Figure 5.15a and 5.15b show SEM images for a thin and a thick part of the same bevelled sample respectively. Smaller grains at the thin part of bevelled CdTe samples has been reported in the literature [30] and here this is associated with a smoother surface. Secondly notwithstanding this scatter, there is an apparent increase in $V_{oc}$ at high thickness in all samples. It may be speculated that this results from the fact that in the thicker parts of the samples there is a reduced opportunity for leakage via accidental conductive paths.

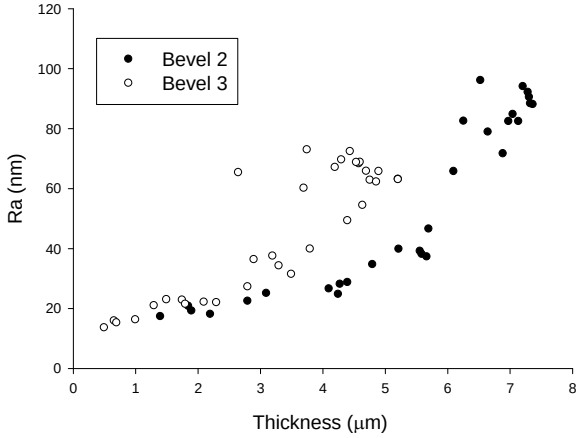


**Figure 5.14**: Roughness of two samples, one from the Bevel 2 batch and the other from Bevel 3. Roughness has been measured using an Ambios profilometer.

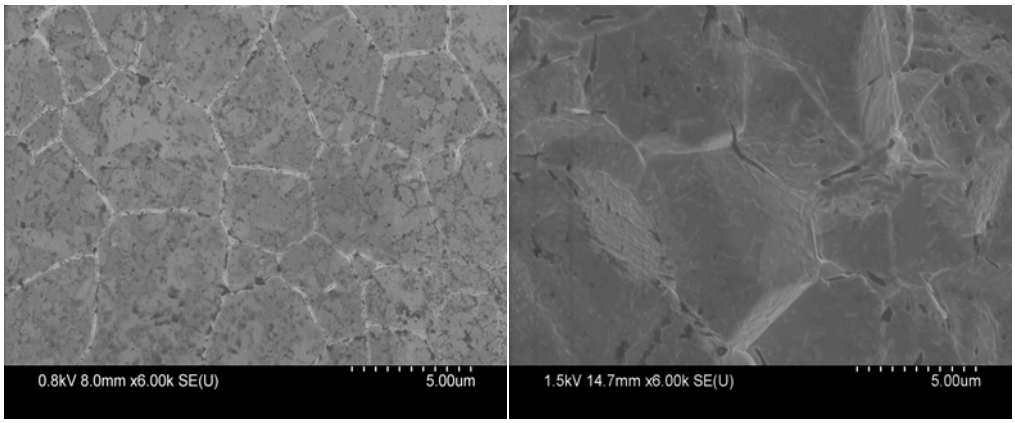


**Figure 5.15**: SEM images of thin (a) and thick (b) parts of a bevelled CdTe sample. The roughness has been reduced in the bevelled part confirming data in Figure 5.14.

#### 5.3.2.4 Bevel 3: device with CBD CdS and with bevelling done after $CdCl_2$ processing

*Experimental (Bevel 3)*

This experiment is the same as Bevel 2 except for two differences: i) the bevelling and $CdCl_2$ steps were reversed i.e. in Bevel 3 the samples were $CdCl_2$ treated then bevelled, ii) the $CdCl_2$ treatment was more severe i.e. the annealing time was increased to 25 minutes in order to have deeper chlorine diffusion. All the other

experimental steps (outlined in Table 5.8) were identical to those of Bevel 2 (Section 5.3.2.3).

*Results and discussion (Bevel 3)*

A data set of equivalent extent to that shown in Figure 5.9 and Figure 5.12 was obtained from the Bevel 3 experiment and is shown in Figure 5.16.

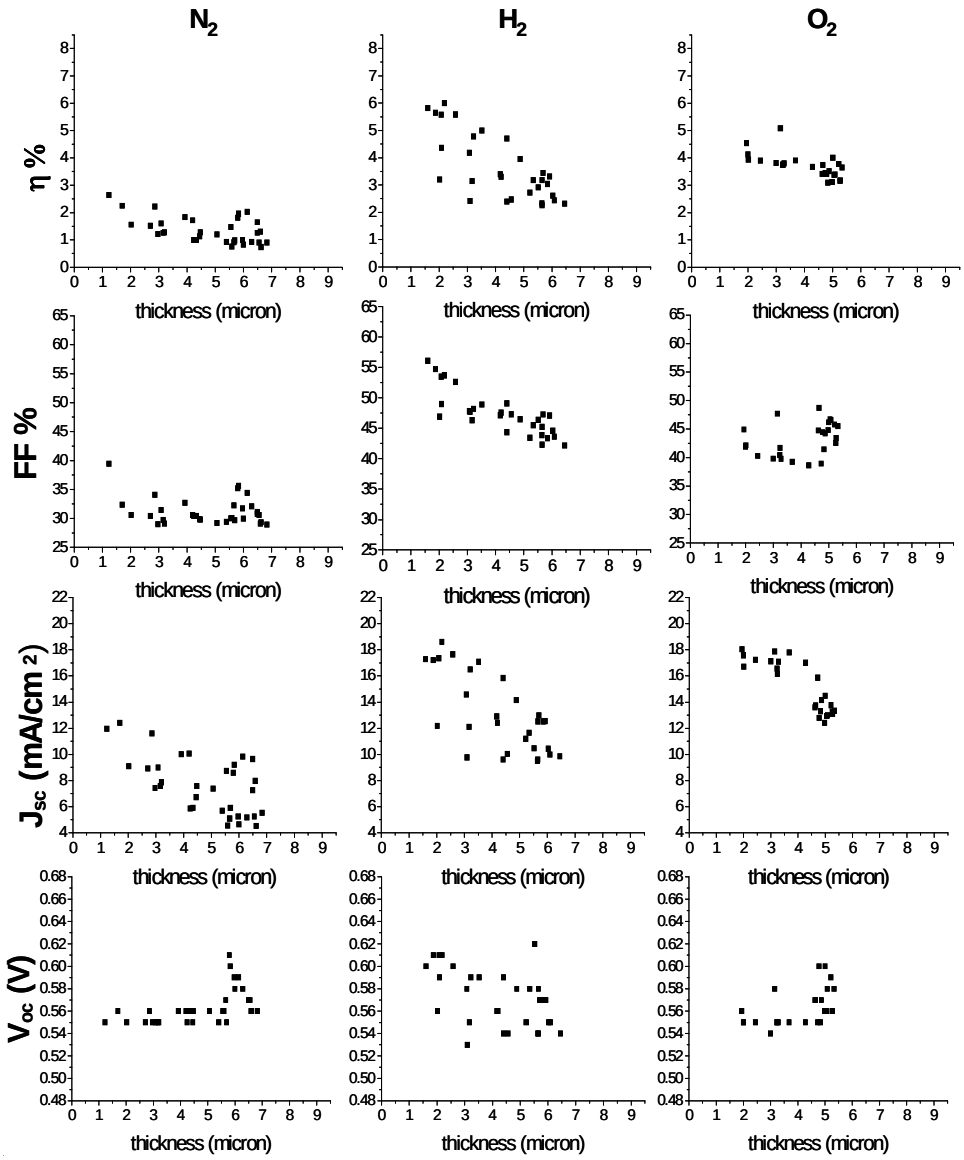


**Figure 5.16**: Working parameters of the solar cells used in Bevel 3 experiment.

Significant differences in the two data sets for Bevel 2 and Bevel 3 were observed as follows:

i) The points had greater scatter for Bevel 3. It was accompanied by a significant increase in surface roughness, as shown in Figure 5.14. This is considered to arise from the $CdCl_2$ treatment (annealing in air) that preceded the bevel etching in this part of the experiment. Oxide layers on CdTe are known to inhibit etching with $Br_2$-based solution, as was shown to be the case for work on oxidised single crystals [39]. It is likely that local masking effects due to non-uniform coverage by oxide have lead directly to the increased roughening of samples subjected to the process of Bevel 3. This roughness variation may be expected to lead directly to increased scatter of the data,

ii) While all working parameters of the cells decreased with increasing CdTe thickness as before, the data showed no major peaks,

iii) Contrary to the results in Figure 5.12, differences in the influence of the processing gases were seen: while $H_2$ and $O_2$ gave efficiencies in the range ~ 2.5-6%, $N_2$ acted to depress the efficiency to the level of ~ 0.5-2.5%. No immediate explanation is available for this behaviour and it should be investigated by repeat runs.

There is weak evidence that etching off the back surface of the CdTe after $CdCl_2$ treatment may give a slight increase in performance compared to un-etched cells. This is most clearly seen in Figure 5.16 in the $V_{oc}$ data for the sample having its CdS treated in $N_2$. There is an apparent peak in $V_{oc}$ at thickness ~ 6 μm, and this is also visible in the *FF* and $\eta$ curves for the same cell. There is no clear reason why this should occur for $N_2$ but not $H_2$ or $O_2$ but it may be the case that scatter masks any similar behaviour in those samples.

## 5.4 Discussion

In the first part of this Chapter the pre- and the post-growth thermal treatments of the CdS/TCO bilayers were investigated. ITO substrates supplied by either VisionTek or Delta Tech. were examined. Neither oxidation nor reduction of the ITO prior to the growth of the CdS affected the *I-V* characteristics of the In/CdS/ITO

structure. All the *I-V* curves were Ohmic (straight lines) which could be due to either there being: i) no change in the interfaces of the In/CdS/ITO, or ii) having direct contact between In and ITO through pinholes in the CdS layer. The latter was tested by evaporating Au contacts on four samples prior to measuring the *I-V* characteristics for the Au/CdS/ITO structure. Since most of them had rectifying *I-V* behaviour (i.e. Schottky junctions) with the CdS (especially with Delta Tech. substrates), the possibility of the presence of pinholes was dismissed. The advantages of the Au method are its simplicity and the reliability for testing the presence of pinholes. The electrical nature of this method allows it to probe pinholing in thin films even if it cannot be detected visually.

However, post-growth oxidation of the CdS/ITO bilayer changed the *I-V* curves from Ohmic to rectifying. Therefore, further analytical tests for the CdS film were needed to explore the reason of this change. The chemical changes on the CdS surface due to oxidation were investigated by testing as as-grown and an oxidised CdS/ITO samples by GIXRD, SIMS and AES. GIXRD showed similar peaks for both samples with a slight change in the preferred orientation. On the other hand, SIMS showed a comparable profile for oxygen in both samples, yet it showed that In had deeper diffusion in the treated CdS. AES analysis showed that oxygen had a higher concentration on the surface of the treated CdS. It is therefore likely that the surface comprises CdO. It can, for that reason, be speculated that the rectification was due to the CdO-$n^+$/CdS-n junction. This is consistent with the character of band diagrams for this junction presented in Figure 5.8b.

The same *I-V* behaviour for both as-grown and oxidised CdS films grown on $SnO_2$:F (Pilkington TEC 8 glass) was observed as for samples grown on ITO. This is contrary to the work of Alamri [1] who found that post-growth oxidation changed the *I-V* characteristics of ITO-based samples and not the $SnO_2$ ones. This discrepancy could be attributed to the presence of pinholes in the CdS used in the In/CdS/$SnO_2$ structure in Alamri's work. The behaviour illustrated in Figure 5.4 supports the assumption that CdO-$n^+$/CdS-n junction is responsible of the rectifying behaviour of the oxidised CdS samples.

The polarity of the field for the CdTe/CdS solar cells is opposite to that for the proposed CdO/CdS junction. Thus, the presence of the CdO would have a deleterious effect on the performance of the CdTe/CdS cells. Hence, this study recommends

removing any oxide layer that could be created on the surface of the CdS before growing the CdTe, or else avoiding surface oxidation.

The second part of the Chapter discussed the performance of complete devices as a function of the combination of: a) annealing the CdS in different ambients, and b) the CdTe thickness. A rapid screening methodology was used to conduct the experiments of this part. In order to select suitable growth conditions for this experiment, a preliminary study was undertaken using various growth techniques. CdTe:$O_2$/CBD-CdS structure was adopted to perform the rapid screening method since this it produces smooth and uniformly performing devices.

Three different experiments were developed as follows: for Bevel 1 experiment, the effect of post-growth annealing of CdS layers - in $O_2$, $N_2$ and $H_2$ (400°C for 4 minutes) - upon the performance of CSS-grown CdTe/CdS/TCO (TCO = TEC 8) has been investigated. Treatment of the CdS with $O_2$ and $N_2$ gave similar results as neither treatment was expected to have a strong influence on the CdS, which was itself grown at 530°C under 1.5 Torr of $O_2$. For these samples, there was however a profound change in PV performance with thickness, with samples less than 3 μm in thickness having high efficiency, dominated by unexpectedly high $J_{sc}$ values. *FF* and $R_{sh}$ were also low in this regime, indicating that there was high leakage current though the material (even in the absence of physical pinholes).

The high scatter of the data was the major limitation of Bevel 1. It was attributed to the local variation of thickness and roughness of both CdS and CdTe layers. The latter was confirmed by measuring the roughness and the SEM images.

The quality of the results was improved in Bevel 2 by depositing the CdTe in a relatively low pressure of $O_2$ on CBD CdS. The clear trends in device performance parameters seen in Figure 5.12 give some confidence that the device uniformity was sufficiently high for the only variable to be the CdTe thickness.

Application of a standard post-growth $CdCl_2$ annealing step (400°C for 10 minutes in air) to the bevelled sample plates (CdTe:$O_2$) allowed identification of an optimum thickness for the CdTe that was exactly compatible with this processing. The efficiency of devices on the plate was controlled by $J_{sc}$, leading to the hypothesis that the performance is controlled by the junction position. This hypothesis was confirmed by the light-biased EQE test.

The second variable investigated in this work was post-growth annealing of the CdS with $N_2$, $H_2$ and $O_2$. However it was shown that this annealing step had no influence on the device results for any CdTe thickness. There are two possible explanations of the null result: i) that the temperature and duration of the annealing were insufficient to effect significant change to the material, or ii) that any annealing-induced change was eliminated by the ramp up to the CdTe growth conditions.

This bevel-etch based screening method is subjected to data scatter that is controlled by surface roughness. In particular it was found that i) high thicknesses of CdTe and ii) samples which were first $CdCl_2$ treated and then bevelled (Bevel 3) were subjected to greater data scatter than others.

The quality of the results acquired from the rapid screening method relies on the smoothness and uniformity of the samples. It has been demonstrated that this methodology was successfully applied to investigate the performance of the CdS/CdTe devices. Each sample plate used in this work had 25-36 contact dots, allowing the same number of CdTe thickness values to be investigated. Hence the screening method accelerates parameter studies by a factor of ~ 30 i.e. one sample replaces a series of 30 conventional growth runs. Moreover, since an investigation may be concluded over a smaller number of growth runs, the requirements for run-to-run reproducibility are relaxed. It may be concluded that the use of this and similar rapid screening methodologies will be of advantage in the empirical development of both new and emerging solar cell processing technologies.

## 5.5 Conclusions

### 5.5.1 CdS/TCO bilayer

The effect of substrate treatment and post-growth annealing of CdS/TCO on its junction performance was investigated. Both ITO/glass substrates and $SnO_2$/glass were used in this study. Both reduction and oxidation of a) the ITO, and b) CdS/ITO bilayer have been investigated by recording the *I-V* characteristics of the In/CdS/ITO structure.

- A method using Au contacts was invented to test the continuity of the CdS layer grown on the ITO.

- Neither reduction nor oxidation of the ITO prior to the growth of the CdS affected the behaviour of the *I-V* characteristics of In/CdS/ITO test structures.
- While the reduction of the CdS/ITO bilayers did not affect the *I-V* curves, post-growth oxidation of the CdS changed it from being Ohmic to be rectifying.
- The oxygen concentration was higher on the oxidised CdS surface of the CdS/ITO bilayer in comparison to the as-grown one as revealed by the AES analysis.
- The transformation of the *I-V* characteristics (i.e. from Ohmic to rectifying) was similar for both ITO and $SnO_2$ substrates. This supports the conclusion that oxidation modified the CdS surface rather than the CdS/TCO interface.
- The finding that CdS/$SnO_2$ may become rectifying upon oxidation is contrary to the findings of Alamri [1]. It is speculated that Alamri's work was marred by pinholes in the CdS.
- The reason for rectification is likely to be due to the creation of a CdO layer on the surface of the CdS, leading to an $n^+/n$ junction.
- The presence of oxide layers between the CdTe and the CdS films could depress the PV performance.

### 5.5.2 Bevel / rapid screening

A bevel / rapid screening method was used to investigate: a) thermal treatment of the CdS in various ambients, and b) the CdTe thickness on the PV performance of complete devices. It is essential to have smooth and uniformly performing samples in order to obtain good quality results using the rapid screening method. A combination of CdTe:$O_2$/CBD-CdS was found to produce suitable samples for the experiments of this method. However, for samples that were bevelled after $CdCl_2$ treatment, the resulting oxidation could introduce additional roughness and data scatter. All sources of roughness lead to scatter in the results.

- Use of the method to investigate the effects of cells grown on CdS that had been annealed in either $O_2$, $N_2$ or $H_2$ revealed no major differences between the three. Either the conditions used were insufficiently severe to induce the effects expected from Section 5.2, or the conditions of the CdTe over growth caused the CdS surface to be re-normalised.

- For the conditions used in this work, it was found that a CdTe thickness of ~ 3 μm is optimum for the $CdCl_2$ treatment used i.e. $T$, time and thickness.
- The performance was dominated by the $J_{sc}$, leading to the assumption that the position of the junction varied across the sample. This assumption was confirmed by the light-biased EQE results.
- The rapid screening method reduced the number of the required samples by a factor of ~ 30.

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# Chapter 6: Electrical Transport Mechanism in the Main Junction of CdTe/CdS Solar Cells

## 6.1 Introduction

In this Chapter an experimental study of the current transport mechanism in three different kinds of CdTe-based cells is presented. The materials that were compared were: a) CSS-CdTe/CdS, b) MOCVD-CdTe/CdS and c) MOCVD-CdTe/CdZnS, this set allowing both the influence of growth method and the type of window layer to be compared.

Current transport phenomena in p-n junctions have been reviewed in Chapter 3, along with the experimental methods used to distinguish them (see Table 2.1). In this Chapter information was extracted from *J-V* curves and also from their temperature dependence. Where appropriate, the light dependence of the *J-V* behaviour was measured and interpreted. In particular, the new light-dependent method of determining the diode factor from relative light intensity measurements (equation 2.38) was used.

The current transport behaviour was investigated for each sample under the following conditions:

a) forward bias in the dark (Section 6.3.2)

b) forward bias in the light (Section 6.3.3)

c) reverse bias in the dark (Section 6.3.4).

Details of the sample fabrication and the data collection are given in Section 6.2 and conclusions are drawn in Section 6.3.

## 6.2 Experimental

### 6.2.1 Fabrication of the samples

Three different samples have been fabricated in order to study the carrier transport mechanisms. Samples number 254 and 305 were fabricated in Bangor University using MOCVD (for more details about the technique see Section 4.2.4) whereas the third one (number 290) was fabricated by CSS in Durham. Table 6.1 summarises the structures of these devices, see text below for more details.

| Sample number | Substrate | Window (growth technique) | Absorber (growth technique) | N-P etch | Contact size |
|---|---|---|---|---|---|
| 290 | FTO | CdS (CSS) | CdTe (CSS) | Yes | Au 2 mm diameter dot |
| 254 | ITO | CdS (MOCVD) | CdTe:$As^+$/CdTe:As (MOCVD) | No | Au 2 mm diameter dot |
| 305 | ITO | CdZnS (MOCVD) | CdTe:$As^+$/CdTe:As (MOCVD) | No | Au 5×5 mm square |

**Table 6.1**: Description of the main layers in each device investigated in this Chapter.

Sample 290 was fabricated by the CSS technique. A 300 nm thick CdS film was deposited on Pilkington TEC 8 glass at a source temperature of ~ 650°C in $O_2$ ambient with a pressure of ~ 1 Torr. Next, the CdS film was in-situ annealed at 400°C in 3 Torr of $H_2$ prior to the CdTe growth. CdTe was grown under a pressure of 100 Torr of $N_2$ and using a source temperature of about 605°C. The deposition time for CdTe was 45 minutes which resulted in a 8 µm thick film. A 200 nm thick $CdCl_2$ film was thermally evaporated on the back surface of the cell at a pressure of ~ $10^{-5}$ Torr. The device was then annealed in air at 400°C for 20 minutes.

The structure of sample 305 was as follows: CdTe:$As^+$(250nm)/CdTe:As(2um)/CdZnS(240nm)/ITO followed by an in-situ $CdCl_2$ treatment. Sample 254 comprises: CdTe:$As^+$(250nm)/CdTe:As(2um)/CdS(240nm)/ITO followed by the same $CdCl_2$ treatment. The only difference in the structure between these two samples was the window layer. The aim of using CdZnS as a window layer is to allow more photons to reach the CdTe, as CdZnS has a higher band gap in comparison with that of the CdS, see for example references [1-3].

For both samples, a layer of the CdTe:$As^+$ was introduced between the CdTe and the back contact to improve the back contact performance [4]. The role and the effect of this layer on the performance of the back contact are discussed in Chapter 7.

All samples were contacted with Au in this lab. Sample 290 was N-P etched for 10 seconds before applying a matrix of 2 mm dot contacts. However, samples 254 and 305 were not etched as they had the CdTe:$As^+$ layer on the back surface. Sample 254 had the same contacts as sample 209 whereas sample 305 had 5×5 mm square contacts.

### 6.2.2 Collecting data

In order to record *J-V-T* characteristics for these devices, each sample was mounted in the cryostat subsequent to connecting the Au contacts with fine copper wires using conductive carbon paste (for more details about the experimental setup see Section 4.4.2). The temperature of the samples varied from 300 K to 200 K with a step of 10 K. At each temperature, the *J-V* data were recorded under illumination of: 0 % (dark), 10 %, 20 %, 50 %, 79 % and 100 % of the AM1.5 spectrum having a nominal intensity of 1000 $Wm^{-2}$. 201 data points were recorded for each *J-V* run. Selected *J-V-T* curves are shown in Appendix C.

The current transport mechanism for each device was investigated under three different conditions: forward bias in dark, forward bias under light and reverse bias in dark.

For measurements under reverse bias, although *V* varied from -1 V to 0 V during recording *J-V-T* characteristics, only the range ~ - 0.3 V to - 0.9 V was considered in the study to avoid: a) possible break-down at high *V*, and b) noise in *J* values at low *V* since they are extremely small (especially at low *T*).

## 6.3 Results and discussion

### 6.3.1 Introduction

The results are divided into three parts based on the experimental conditions under which the data were collected: forward bias in dark (Section 6.3.2), forward bias under light (Section 6.3.3) and reverse bias in dark (Section 6.3.4). The reason for excluding the reverse bias data under light from this work (noise) is mentioned in Section 6.4.

### 6.3.2 Measurement in forward bias under dark conditions

By using the slope method (which is explained in Section 2.4f), the ideality factor $n$ and the saturation current $I_0$ were calculated for each device and the results are summarised in Table 6.2 for all samples.

| | **Sample 290 CSS CdS window** | | **Sample 254 MOCVD CdS window** | | **Sample 305 MOCVD CdZnS window** | |
|---|---|---|---|---|---|---|
| ***T* (K)** | ***$I_0$* (A)** | ***n*** | ***$I_0$* (A)** | ***n*** | ***$I_0$* (A)** | ***n*** |
| 300 | 1.4E-11 | 1.7 | 6.9E-12 | 1.5 | 2.6E-9 | 2.1 |
| 290 | 1.1E-11 | 1.8 | 2.8E-12 | 1.5 | 1.2E-9 | 2.1 |
| 280 | 5.6E-12 | 1.8 | 1.4E-12 | 1.5 | 4.2E-10 | 2.1 |
| 270 | 3.1E-12 | 1.9 | 4.7E-13 | 1.6 | 1.4E-10 | 2.1 |
| 260 | 1.3E-12 | 2 | 1.2E-13 | 1.6 | 4.1E-11 | 2.1 |
| 250 | 7.1E-13 | 2 | 8.8E-14 | 1.7 | 9.9E-12 | 2 |
| 240 | 4.4E-13 | 2.1 | 3.8E-14 | 1.7 | 3.1E-12 | 2 |
| 230 | 2.5E-13 | 2.2 | 1.4E-14 | 1.8 | 1.4E-12 | 2.1 |
| 220 | 1.4E-13 | 2.4 | 4.8E-15 | 1.8 | 3.6E-13 | 2.1 |
| 210 | 8.1E-14 | 2.5 | 1.9E-15 | 1.9 | 1.3E-13 | 2.1 |
| 200 | 3.5E-14 | 2.7 | 5.4E-16 | 2 | 2.8E-14 | 2.2 |

**Table 6.2**: The values of the ideality factor $n$ and the saturation current $I_0$ under dark conditions for all samples studied in this Chapter, as a function of temperature.

a) *Samples 290 and 254 (with CdS window layer)*

The *J-V-T* data obtained from samples 290 and 254 were analysed according to the models described in Section 2.5 and Table 2.1. The most appropriate fit was that expected for multi-step tunnelling. Plots of ln $J$ versus $V$ for each curve generally showed straight line behaviour at low voltage i.e. in the region free from influence of the rectifying back contact. Such plots allowed the constant $A$ (see equation 2.20) to be extracted and Figure 6.1 shows its variation with $T$ for each of the three cells studied. For samples 290 and 254, $A$ is only weakly dependent on $T$, indicating that multi-step tunnelling is likely to be operating. Indeed, none of the other mechanisms is expected to display temperature independent slopes in this way.

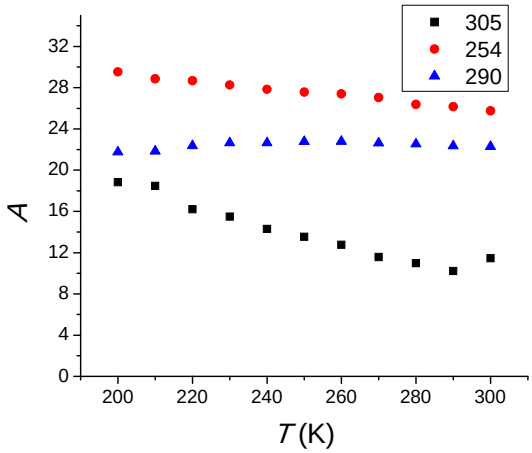


**Figure 6.1**: The values of $A$ (i.e. the slope of ln$J$ versus $V$ at forward bias under dark conditions, equation 2.20) as a function of $T$ for the samples described in Table 6.1

Further evidence of this mechanism is that the diode factor ($n$) decreased with $T$, as shown in Table 6.2. For the case of multi-step tunnelling it is this dependence that is an indicator of the mechanism, rather than the absolute value of $n$ at any given $T$. Moreover, testing for the temperature dependence of $J_0$ versus $T$ (equation 2.21) by plotting ln $J_0$ versus $T$ as shown in Figure 6.2 gave a linear fits as expected (the reader is referred to Table 2.1 for a note on the physical appropriateness of the use on $n$ in diagnosing current transport mechanism).

Having established that the data conform to the case of multi-step tunnelling as described by equations 2.20 and 2.21, it is therefore appropriate to extract the number of tunnelling steps ($R$) for this process, as described in Section 2.5.2.

In order to obtain the value of $R$, both $\alpha$ and $K$ needed to be calculated from equations 2.23 and 2.24 respectively. However, equation 2.24 implies that if the doping concentration in the CdS is considerably higher than that of the CdTe (i.e. $N_D >> N_A$), then $K \approx 1$. This approximation has been used for CdTe/CdS cells by both Ercelebi *et al.* [5] and Al-Allak *et at.* [6]. Equation 2.23 requires the value of doping concentration of the CdTe in order to determine $\alpha$. Consequently, $C$-$V$ measurements (see Section 2.2 for a description of this test) were carried out in the dark at a frequency of 150 KHz. The resulting curves for samples 290 and 254 are shown in Figure 6.3.

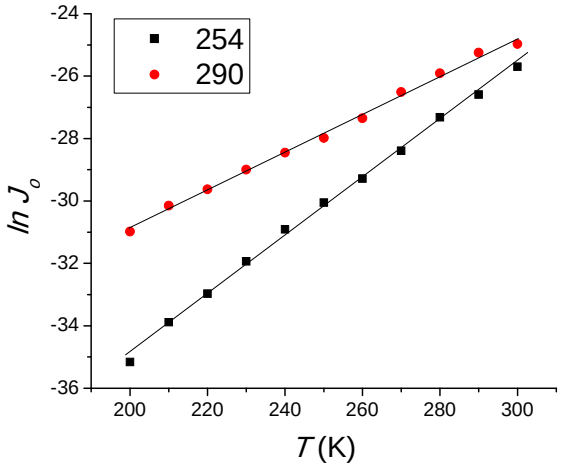


**Figure 6.2**: The linear relationship between $lnJ_0$ and $T$ for samples 254 and 290 under dark conditions.

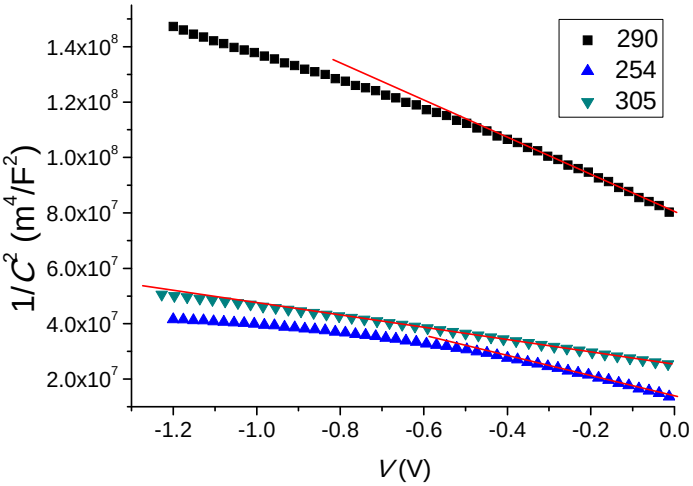


**Figure 6.3**: $1/C^2$ versus reverse $V$ for samples 254, 290 and 305 under dark conditions. The lines show the linear fits of the data from which both the doping concentration near the junction ($N_A$) and the built-in potential $V_{bi}$ were extracted.

Using both equation 2.7 and the linear parts (discussed later) in Figure 6.3, $N_A$ was found to be $2.07 \times 10^{15}/cm^3$ and $5.36 \times 10^{15}/cm^3$ for samples 290 and 254

respectively. For the CdTe, the values of $\varepsilon$ and $m_n$ were chosen to be 10.36 $\varepsilon_0$ and 0.096 $m_e$ respectively [7]. $R$ values at room temperature were determined by using this information as shown in Table 6.3. These were of the same order of magnitude as the results found by Al-Allak *et al.* [6].

| **Sample** | **Doping/cm$^3$** | $\alpha$ | **Slope of ln $J$ vs. $V$, ($A$)** | **Number of tunnelling steps ($R$)** |
|---|---|---|---|---|
| 290 | $2.07\times10^{15}$ | 462.9 | 22.3 | 432 |
| 254 | $5.36\times10^{15}$ | 287.8 | 25.8 | 125 |

**Table 6.3**: Parameters extracted from samples 290 and 254 to determine the number of tunnelling steps $R$.

It was mentioned earlier that doping concentrations of the cells were determined using both equation 2.7 and the $1/C^2$ versus $V$ plot (Figure 6.3). However, it is seen in the figure that only data at low reverse bias were considered. The reason of selecting reverse bias was to avoid the diffusion capacitance, which arises under forward bias conditions [8]. It is known that the depletion region width increases with increasing the reverse bias applied. This may affect the results obtained from the $C$-$V$ measurements. For example, at sufficiently high reverse bias, the CdTe side of a CdTe/CdS cell was reported to be fully depleted [9], which affect the linearity of the line in the $1/C^2$ versus $V$ plot. Therefore, in the calculation above, low reverse voltages were considered in order to avoid probing the material away from the heterojunction.

b) *Sample 305 (with CdZnS window layer)*

The analysis of $J$-$V$-$T$ data for sample 305 was in accordance with the mechanism of recombination in the depletion region mechanism, which is described in Section 2.5.3. Contrary to samples 290 and 254, the constant $A$ decreased with increasing $T$ as illustrated in Figure 6.1, indicating that the transport mechanism is thermally activated. The ideality factor $n$ was approximately 2 and was invariant with $T$ as shown in Table 6.2, which is the value expected for a depletion region recombination dominated current transport mechanism (see Section 2.5.3). Moreover, the temperature independence of $n$ has previously been reported for CdTe/CdS cells in

which the current transport was dominated by recombination processes [10, 11]. Furthermore, Figure 6.4 shows that ln $J_0$ varied linearly with 1/$T$ (equation 2.29) also suggesting this transport mechanism.

Since the ionic radius of Zn is smaller than of Cd, CdZnS has a smaller lattice constant in comparison to CdS. This may increase the mismatch between the CdZnS and CdTe layers compared to CdTe and CdS layers, which is 10.8 % [12]. This mismatch may create interface states that may affect the electronic properties of the interface, and therefore, the behaviour of carriers passing this region. Zn diffusion into CdTe may also a) alter both optical and electrical properties of the material [13], and b) increase intermixing between the layers compared to the case for CdS.

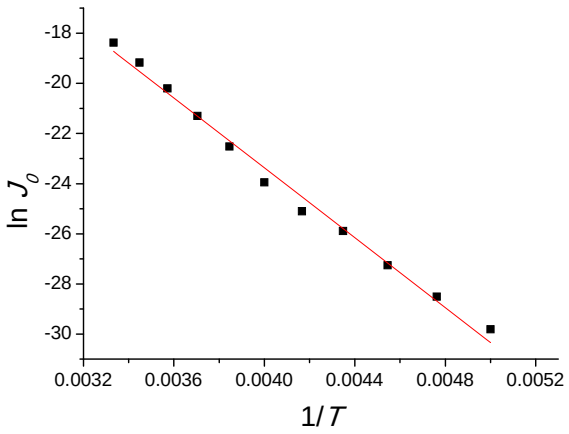


**Figure 6.4**: ln $J_o$ versus 1/$T$ for sample 305.

It was discussed in Sections 2.5.2 and 2.5.3 that a multi-step tunnelling mechanism requires a uniform trap distribution, while recombination in the depletion region requires traps localised near the middle of the band gap. Therefore, it may be assumed that using CdZnS as a window layer changed the trap distribution in the heterojunction to be more concentrated near the mid gap, whereas traps were uniformly distributed within the energy gap when CdS was used. This transferred the current transport mechanism from multi-step tunnelling to recombination in depletion region when CdS was replaced by CdZnS.

### 6.3.3 Measurement in forward bias under light conditions

The results extracted from the *J-V* curves under 100 % illumination (approximately 1000 $Wm^{-2}$ AM1.5), and which were used to determine the built-in potential ($V_{bi}$) for the investigated devices are discussed first. $V_{oc}$ is plotted as a function of $T$ for all cells in Figure 6.5 in order to determine $V_{bi}$ of the main junction (i.e. CdTe/CdS heterojunction) by using equation 2.39 as explained in Section 2.6.

The intercept of the of the resulting line with the $V_{oc}$ axis (at $T = 0$), as shown in Figure 6.5, gives the built-in potential $V_{bi}$, which was found to be 1.26, 1.15 and 1.19 V for samples 290, 254 and 305, respectively. It is seen in Figure 6.5 that below $T \sim 230$ K the data for samples 290 and 305 deviates from linearity which is attributed to carrier freeze-out [14].

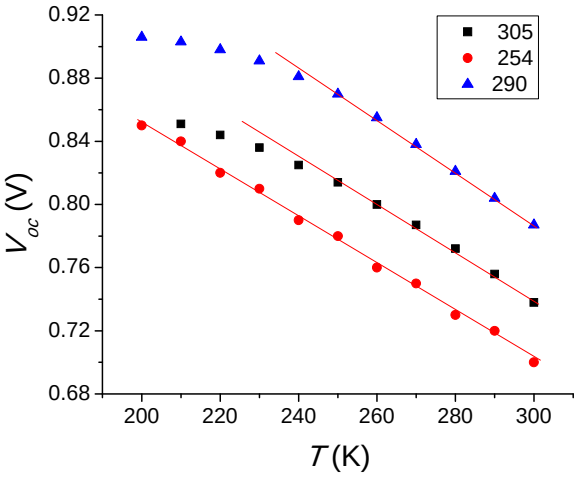


**Figure 6.5**: The $V_{oc}$ for all samples as a function of $T$. The lines represent the straight parts which were extrapolated to the $V_{oc}$ axis to determine the built-in potential.

The built-in potential for all samples was determined also from the *C-V* measurements (equation 2.7). Using the intercept values from Figure 6.3, $V_{bi}$ was 1.2, 0.43 and 1.12 V for samples 290, 254 and 305 respectively.

Moreover, as recombination in the depletion region was the most dominant current process for sample 305, $V_{bi}$ for this cell was evaluated as follows: The activation energy ($\Delta E$) was determined from the slope of the line in Figure 6.4 by using equation 2.29,

$$J_0 = J_{00} \exp(-\frac{\Delta E}{nkT}) \qquad (2.29)$$

The value of $\Delta E$ was found to be 0.6 eV. Knowing that $n \sim 2$ (Table 6.2) and using equation 2.30,

$$n\Delta E = V_{bi} \qquad (2.30),$$

yielded that $V_{bi}$ = 1.2 V for sample 305. The values of $V_{bi}$ as determined from the different methods mentioned above are summarised in Table 6.4.

| **Sample** | $V_{bi}$ **(V)** | | |
|---|---|---|---|
| | $V_{oc}$ **vs.** $T$ **method** | $C$-$V$ **method** | $\Delta E$ **method** |
| 290 | 1.26 | 1.2 | - |
| 254 | 1.15 | 0.43 | - |
| 305 | 1.19 | 1.12 | 1.2 |

**Table 6.4**: $V_{bi}$ values for all cells as extracted using different methods.

It is seen in Table 6.4 that the values of the built-in potential determined by using the methods described above for samples 290 and 305 are in a good agreement (1.23 ± 0.03 and 1.17 ± 0.04 V for samples 290 and 305 respectively). However, it varied from 1.15 V to 0.43 V for sample 254. The discrepancy in $V_{bi}$ values for sample 254 may occur from the inaccuracy of the built-in potential value extracted from the $C$-$V$ measurements. It has been reported that the $C$-$V$ data could lead to erroneous results for the built-in potential values due to various reasons such as the localized states in the energy gap [15]. The presence of interface states in the junction may change the intercept of the line of $V$ versus $C^{-2}$ plot, which changes the extracted value of $V_{bi}$. However, this may not change the slope of the line i.e. the value of doping concentration may not be affected by such interface states [10]. Hence, Table 6.4 implies that sample 254 might have more interface states than samples 290 and 305. Therefore, $V_{bi}$ extracted from Figure 6.5 (i.e. $V_{oc}$ vs. $T$ method) are used for calculations in following sections due to its greater reliability compared to the results of the $C$-$V$ measurements.

The current transport mechanism under forward bias and light conditions is now discussed. Both $I_0$ and $n$ were evaluated by using the slope method (for light data, see Section 2.4f). The results calculated for sample 254 using this method are resented in Table 6.5.

The $n$ values determined by the method described above varied in the range 3.8 (300 K) to 13 (200 K) even though $n$ is only expected to have a physical meaning in the range $1 \leq n \leq 2$ [8]. (The physical meaning of $n$ is discussed in both Section 2.4 and Appendix B).

| $T$ (K) | $I_o$ (A) | $n$ |
|---|---|---|
| 300 | 2.18E-06 | 3.8 |
| 290 | 2.12E-06 | 4 |
| 280 | 3.98E-06 | 4.8 |
| 270 | 6.361E-06 | 5.5 |
| 260 | 4.61E-06 | 5.4 |
| 250 | 6.2E-06 | 6.1 |
| 240 | 1.14E-05 | 7.2 |
| 230 | 1.54E-05 | 8.1 |
| 220 | 2.15E-05 | 9.2 |
| 210 | 4.71E-05 | 11.9 |
| 200 | 5.25E-05 | 13 |

**Table 6.5**: The values of both saturation current and ideality factor for sample 254 (under AM1.5 illumination) as extracted from equation 2.9.

Illumination can make dramatic changes to the shape of the *J-V* curve of solar cells. For example, the superposition principle is known to be invalid for CdTe/CdS cells, which means that the behaviour of the *J-V* curve varies under light in comparison to that in the dark [16, 17]. The light absorbed in the CdS layer was reported to cause steeper *J-V* characteristics than the dark ones due to ionisation of deep traps in the CdS [18]. The non-ideal behaviour of the illuminated *J-V* curve affects the values of both slope and intercept extracted by using equation 2.9. Hence, the method used to determine $n$ and $I_0$ in dark (i.e. the slope method) is not reliable to analyse data collected under illumination. The illuminated data, therefore, were analysed using the new method described in Section 2.5.4, which revealed that SRH recombination is operating for all cells under both forward bias and illumination.

Figures 6.6 – 6.8 show the plots of equation 2.38 at various light intensities for samples 290, 254 and 305 respectively. The results of these plots are summarised in Tables 6.6 – 6.8 respectively.

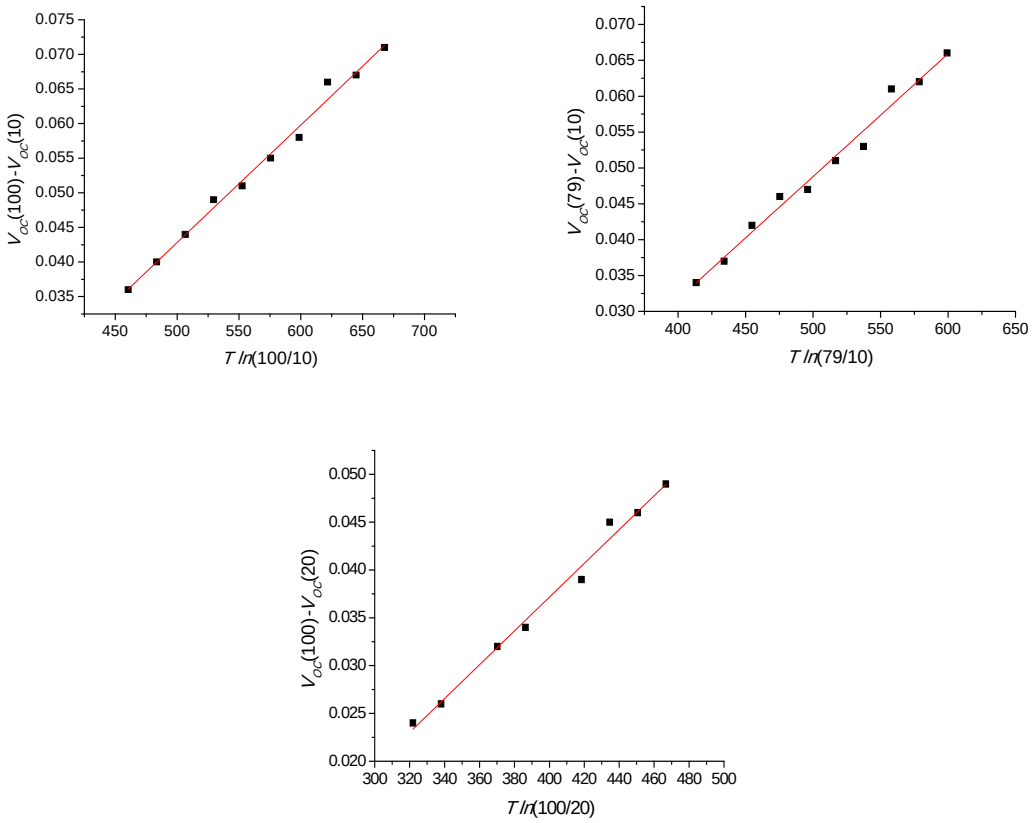


**Figure 6.6**: $V_{oc}(a) - V_{oc}(b)$ versus $T \ln(\frac{a}{b})$ according to equation 2.38 for sample 290.

In each figure the light relative intensity ($a$/$b$) used is shown in the y-axis values.

| **Light intensities** | **Slope (V/K)** | ***n*** |
|---|---|---|
| 100 % to 10 % | 1.69E-4 | 1.96 |
| 100 % to 20 % | 1.76E-4 | 2.04 |
| 79 % to 10 % | 1.71E-4 | 1.98 |
| Average of *n* values | | 1.99 |
| SD of *n* values | | 0.04 |

**Table 6.6**: Slopes of lines in Figure 6.6 and the calculated values of *n* for sample 290. The table shows also the average and the standard deviation of the *n* values.

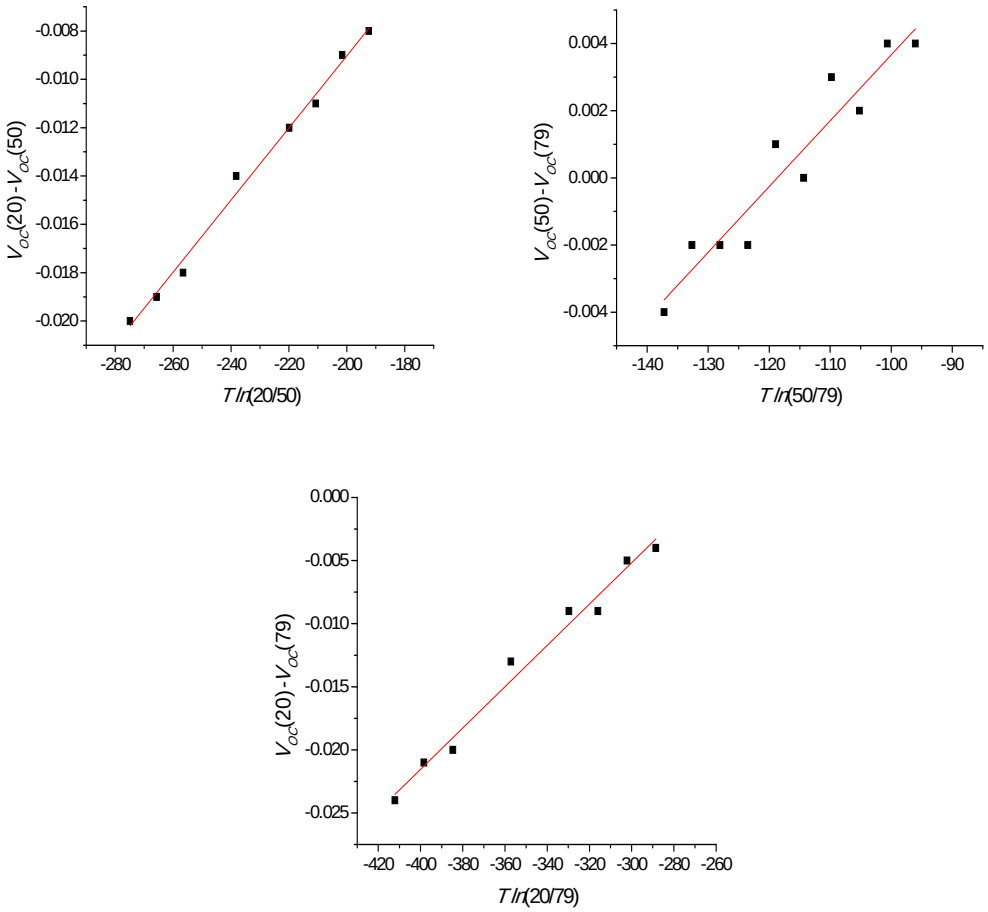


**Figure 6.7**: $V_{oc}(a) - V_{oc}(b)$ versus $T\ln(\frac{a}{b})$ according to equation 2.38 for sample 254.

In each figure the light relative intensity ($a$/$b$) used is shown in the y-axis values.

| **Light intensities** | **Slope (V/K)** | ***n*** |
|---|---|---|
| 20 % to 50 % | 1.49E-04 | 1.73 |
| 50 % to 79 % | 1.96E-04 | 2.27 |
| 20 % to 79 % | 1.63E-04 | 1.89 |
| Average of *n* values | | 1.96 |
| SD of *n* values | | 0.28 |

**Table 6.7**: Slopes of lines from Figure 6.7 and the calculated values of *n* for sample 254. The table shows also the average and the standard deviation of the *n* values.

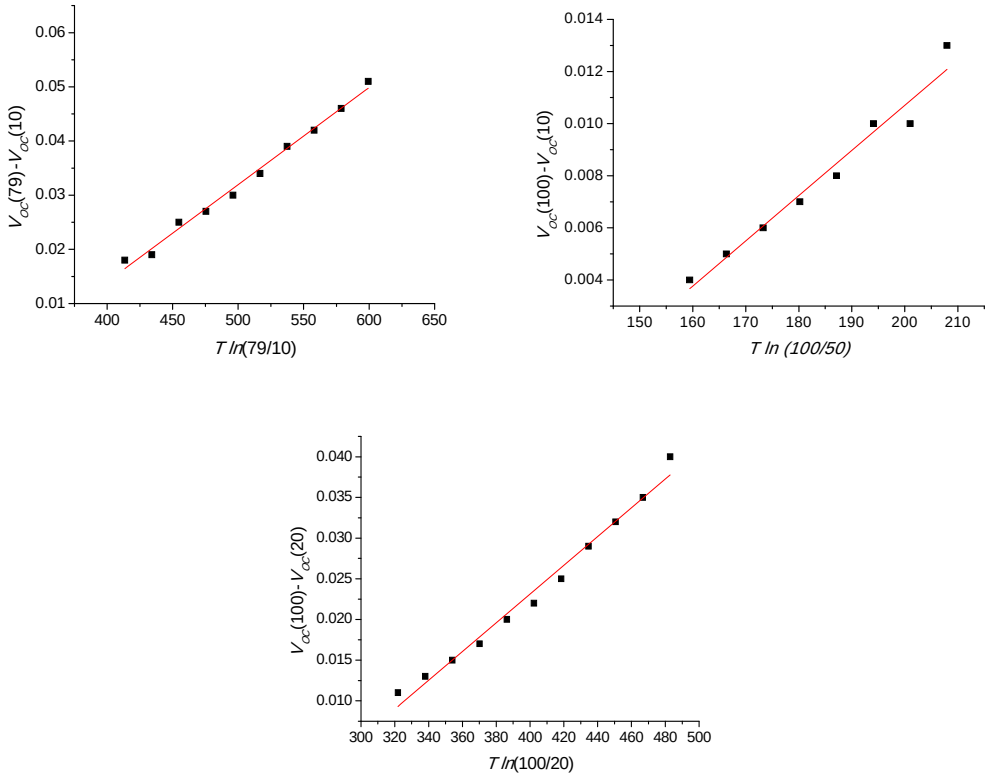


**Figure 6.8**: $V_{oc}(a) - V_{oc}(b)$ versus $T \ln(\frac{a}{b})$ according to equation 2.38 for sample 305.

In each figure the light relative intensity ($a$/$b$) used is shown in the y-axis values.

| **Light intensities** | **Slope (V/K)** | ***n*** |
|---|---|---|
| 100 % to 50 % | 1.73E-4 | 2 |
| 79 % to 10 % | 1.79E-4 | 2.07 |
| 100 % to 20 % | 1.76E-4 | 2.04 |
| Average of *n* values | | 2.04 |
| SD of *n* values | | 0.04 |

**Table 6.8**: Slopes of lines in Figure 6.8 and the calculated values of *n* for sample 305. The table shows also the average and the standard deviation of the *n* values.

Tables 6.6 – 6.8 show that $n \sim 2$ for all samples. It can be concluded, therefore, that SRH recombination is the most probable transport mechanism in the forward bias regime under illumination as explained in Section 2.5.4. This mechanism has been reported for CdTe/CdS cells by both Oman *et al.* [19] and Hegedus and McCandless [14].

The reason for having a different transport mechanism under illumination (compared to the dominating mechanisms in the dark) could be attributed to the light-induced changes in the material. For example, it has been reported that illumination had a significant effect on the interface states for CdTe/CdS cells [20]. The photogenerated carriers fill the interface states which may lead to different electrical behaviour in the CdTe/CdS junction.

### 6.3.4 Measurement in reverse bias in the dark

Analysis of the *J-V-T* characteristics for all three devices indicated that under reverse bias conditions in the dark, the current transport process was dominated by multi-step tunnelling. The relationship between $J_r$ and $V$ under reverse bias was investigated by testing the power dependence of $J_r$ on $V$ using equation 2.28 (see Section 2.5.2b). The power values ($m$) (from equation 2.28) as a function of $T$ for all samples are summarised in Table 6.9.

| ***T*** | ***m* values** | | |
|---|---|---|---|
| | **Sample 305** | **Sample 245** | **Sample 290** |
| 300 | 1.08 | 1.21 | 1.08 |
| 290 | 1.10 | 1.30 | 1.00 |
| 280 | 1.11 | 1.44 | 1.02 |
| 270 | 1.13 | 1.79 | 1.05 |
| 260 | 1.15 | 2 | 1.02 |
| 250 | 1.18 | 2.24 | 1.02 |
| 240 | 1.21 | 2.36 | 1.03 |
| 230 | 1.29 | 2.57 | 1.04 |
| 220 | 1.29 | 2.27 | 1.07 |
| 210 | 1.33 | 2.44 | 1.11 |
| 200 | 1.40 | 2.80 | 1.16 |

**Table 6.9**: The values of $m$ (the slope of $\ln J_r$ versus $\ln V$, equation 2.28) at all temperatures tested in this experiment.

As seen in the table, *m* generally decreased as *T* increased. This behaviour has been reported for tunnelling dominated transport mechanism by Yakubu [21] and Vatavu and GaSin [22] for CdTe/ITO and CdTe/CdS devices respectively.

Additionally, data of all cells conformed equation 2.27, which is further evidence of the domination of multi-step tunnelling mechanism on current transport. The values of the built-in potential $V_{bi}$ extracted from Figure 6.5 (i.e. $V_{oc}$ vs. $T$) were used in this calculation. Figures 6.9 – 6.11 show the ln $(J_r/V)$ against $(V_{bi} - V)^{-1/2}$ plots as $T$ varied from 200 K to 300 K for samples 290, 254 and 305 respectively.

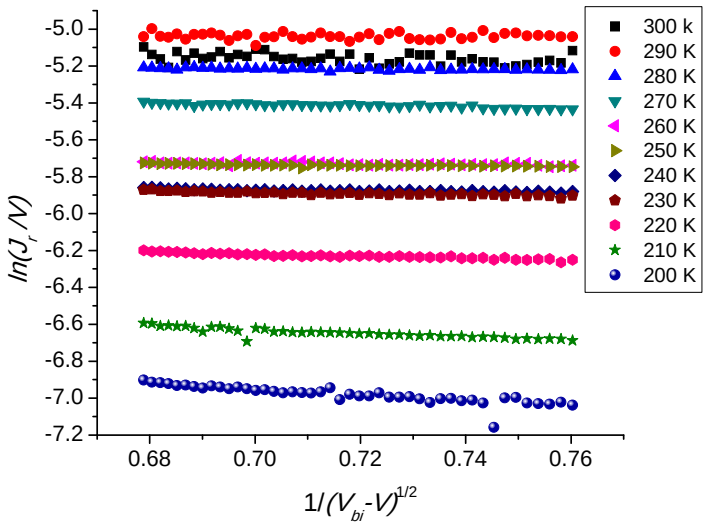


**Figure 6.9**: *ln* $(J_r/V)$ vs. $(V_{bi} - V)^{-1/2}$ for sample 290 at $T$ = 200 – 300 K (reverse bias in the dark).

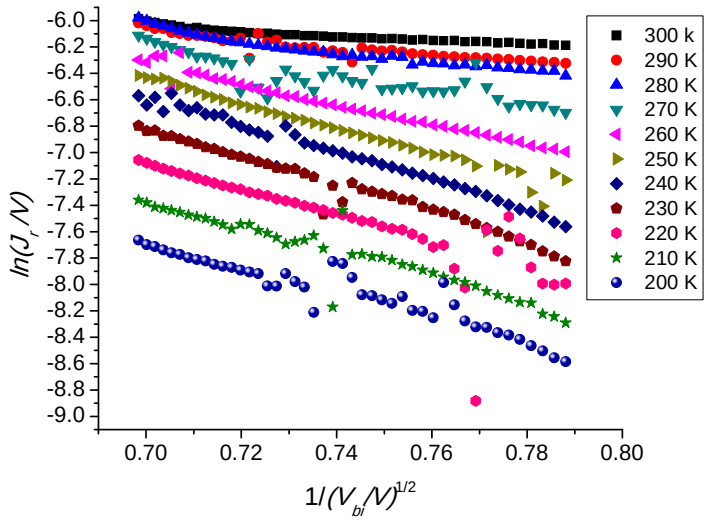


**Figure 6.10**: *ln* $(J_r/V)$ vs. $(V_{bi} - V)^{-1/2}$ for sample 254 at $T$ = 200 – 300 K (reverse bias in the dark).

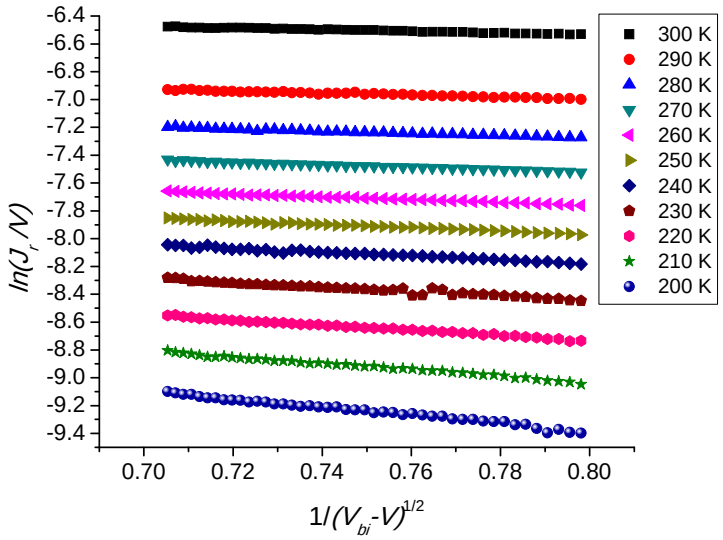


**Figure 6.11**: *ln* $(J_r/V)$ vs. $(V_{bi} - V)^{-1/2}$ for sample 305 at $T$ = 200 – 300 K (reverse bias in the dark).

The slope and the intercept of each line in the figures above are summarised in Table 6.10. Figure 6.10 shows that the curves of sample 254 were noisier than those for other samples. However, its general behaviour is governed by equation 2.27.

| *T* | Sample 290 | | Sample 254 | | Sample 305 | |
|---|---|---|---|---|---|---|
| | slope | intercept | slope | intercept | slope | intercept |
| 300 | -0.192 | -17.74 | -1.26 | -17.91 | -0.634 | -16.62 |
| 290 | -0.0198 | -17.74 | -2.7 | -16.91 | -0.798 | -16.96 |
| 280 | -0.153 | -17.82 | -4.611 | -15.57 | -0.799 | -17.23 |
| 270 | -0.454 | -17.81 | -7.883 | -13.19 | -0.857 | -17.43 |
| 260 | -0.164 | -18.33 | -8.615 | -13 | -0.957 | -17.59 |
| 250 | -0.211 | -18.3 | -9.147 | -12.77 | -1.169 | -17.63 |
| 240 | -0.278 | -18.39 | -9.966 | -12.34 | -1.284 | -17.74 |
| 230 | -0.363 | -18.35 | -10.45 | -12.23 | -1.447 | -17.87 |
| 220 | -0.58 | -18.53 | -9.135 | -13.42 | -1.741 | -17.93 |
| 210 | -0.963 | -18.67 | -11.356 | -12 | -2.119 | -17.93 |
| 200 | -1.428 | -18.67 | -7.699 | -15.06 | -2.678 | -17.83 |

**Table 6.10**: The values of slopes and intercepts extracted from Figures 6.9 – 6.11.

Generally, slopes of all samples decreased as *T* increased. This behaviour was reported by Ercelebi *et al.* [5] and was attributed to the temperature dependence of the band gap. However, it is seen in Table 6.10 that there is some inconsistency in this behaviour for some values such as the slopes of samples 290 and 254 at 290 K and 200 K respectively. This could arise from errors in measuring the slopes due to the scattering of the data.

Since the current transport obeyed multi-step tunnelling model under the reverse bias condition as discussed above, equation 2.27 was also used (in addition to the intercept values in Table 6.10) to determine the trap density $N_t$ as explained in Section 2.5.2b. The lattice constant (*a*) for the CdTe was chosen to be 6.48 Å [23]. $N_t$ values for all samples in the temperature range 200 – 300 K are summarised in Table 6.11.

$N_t$ values for samples 290 and 305 agree with those measured by Proskuryakov *et al.* [9] using admittance spectroscopy for CdTe:As/CdS cells. Proskuryakov reported that $N_t$ was found to be ~ $10^{14}$/cm$^3$ and $10^{15}$/cm$^3$ for shallow and deep traps respectively. Furthermore, Al-Amri [24] used the space charge limited current (SCLC) theory to calculate $N_t$ as a function of *T* (which varied in a range of ~ 220 – 330 K) for both $CdCl_2$-treated and untreated cells. All results [24] were found to be in the same order of magnitude ($10^{14}$/cm$^3$) with higher values for the untreated cells. Therefore, the slight increase in the values of $N_t$ for samples 305 and 290 compared to those reported by Al-Amri [24] may arise from the insufficient $CdCl_2$

treatment for devices investigated in this work, which may lead to relatively higher values of the trap density. $N_t$ values for sample 254 varied with $T$ inconsistently as seen in Table 6.11. This behaviour can be attributed to errors from scatter of data in Figure 6.10.

| | $N_t$ (cm$^{-3}$) | | |
|---|---|---|---|
| **$T$ (K)** | **Sample 290** | **Sample 254** | **Sample 305** |
| 300 | 1.84E+15 | 2.19E+15 | 6.06E+14 |
| 290 | 1.85E+15 | 8.09E+14 | 8.45E+14 |
| 280 | 2.01E+15 | 2.1E+14 | 1.11E+15 |
| 270 | 1.98E+15 | 1.96E+13 | 1.36E+15 |
| 260 | 3.33E+15 | 1.62E+13 | 1.59E+15 |
| 250 | 3.25E+15 | 1.28E+13 | 1.66E+15 |
| 240 | 3.55E+15 | 8.33E+12 | 1.86E+15 |
| 230 | 3.4E+15 | 7.46E+12 | 2.12E+15 |
| 220 | 4.08E+15 | 2.46E+13 | 2.24E+15 |
| 210 | 4.7E+15 | 5.94E+12 | 2.23E+15 |
| 200 | 4.68E+15 | 1.27E+14 | 2.02E+15 |

**Table 6.11**: Trap density ($N_t$) of all samples in the whole range of $T$ used in the study (dark conditions).

It can be concluded that multi-step tunnelling is the most dominant transport mechanism for dark reverse current for all samples investigated in this study. This transport process has also been reported by several authors to be the dominant transport mechanism for CdTe/CdS solar cells under reverse bias condition [5, 20, 22, 25].

It is known that the depletion region width increases with increasing the reverse applied voltage. Hence, the effect of the presence of Zn in the CdTe/window interface for sample 305 may have been negligible as the depletion region increased i.e. the effects of both Zn diffusion in the CdTe and CdTe/CdZnS intermixing (near the interface) might be masked by effects occurring due to the “wide” depletion width under the reverse bias condition.

## 6.4 Conclusion

The electrical current flow process in CdTe heterojunction solar cells was investigated for three different devices. The transport mechanisms were studied in both forward and reverse biases, with and without illumination. The results obtained in this Chapter are summarised in Table 6.12.

| Cell (growth technique) | Bias | Illumination | Transport mechanism |
|---|---|---|---|
| 290 CdTe/CdS (CSS) | Forward | Dark | Multi-step tunnelling |
| | Reverse | Dark | Multi-step tunnelling |
| | Forward | Light | SRH |
| 254 CdTe/CdS (MOCVD) | Forward | Dark | Multi-step tunnelling |
| | Reverse | Dark | Multi-step tunnelling |
| | Forward | Light | SRH |
| 305 CdTe/CdZnS (MOCVD) | Forward | Dark | Recombination in depletion region |
| | Reverse | Dark | Multi-step tunnelling |
| | Forward | Light | SRH |

**Table 6.12**: The current transport mechanism for cells studied in this Chapter. The table shows both bias and illumination conditions under which the data were collected, and the transport mechanisms identified.

Multi-step tunnelling was found to be the dominant process in the dark forward current for CdTe/CdS cells fully grown by either CSS or MOCVD (samples 290 and 254). However, the current transport for the MOCVD-CdTe/CdZnS (sample 305) cell was governed by recombination in depletion region. In other words, the transport mechanism in the dark forward bias seems to be dependent on the type of the window layer rather than the growth technique. The Zn diffusion-induced changes in the electronic properties for the CdTe/CdZnS interface were speculated to be the reason of this behaviour.

It is important to point out that the method used to extract the ideality factor values in dark was not capable of giving reasonable results under light. Therefore, the transport mechanism under illumination was investigated by considering a new

method, which relies on the behaviour in the $V_{oc}$ as a function of $T$ in two different light intensities. For measurements carried out under forward bias in the light, SRH recombination was the most probable mechanism for all samples. Light-induced changes in the materials were speculated to be responsible of the transformation of the transport mechanisms between dark and light.

In case of the reverse bias in the dark, multi-step tunnelling was again dominating the flow of carriers for all the devices investigated in this Chapter. The transport mechanism under reverse bias was independent of both a) the growth techniques by which the devices were fabricated, and b) the window layer type. It was mentioned earlier that for sample 305, the diffusion of Zn in the CdTe layer was assumed to be the reason of having different transport mechanism for this sample compared to the other samples (samples 290 and 254). However, this effect might be masked due to the increase in the depletion width for the heterojunction for sample 305 under the reverse bias condition.

By using the multi-step tunnelling model, it was possible to measure a) the number of the required tunnelling steps to traverse the junction under forward bias conditions, which was found to be 432 and 125 steps for samples 290 (all CSS) and 254 (MOCVD) respectively. These values are comparable to those reported by Al-Allak *et al.* [6] for CdTe/CdS cells, which was 294 steps. b) the trap density in the reverse bias, which was ~ $10^{15}$ $cm^{-3}$ for samples 290 and 305 (MOCVD with CdZnS window layer). The values agree with those reported by Proskuryakov *et al.* [9], but one order of magnitude higher that Al-Amri's results [24], which may be attributed to the $CdCl_2$ treatment. Both recombination and tunnelling processes require a high density of localised levels, which might result from the mismatch between the CdTe and the window layers. The lattice mismatch can be increased by the different thermal expansion coefficients of CdTe and window layer materials [26].

The reverse bias measurements in light were not analysed in this work because of the high noise in the data. Light generated current $J_L$ is greatly higher than the saturation current $J_0$, and therefore, any disruption in the $J_L$ could dominate the whole reverse current in light. The noise could be generated from flickering of the light source in the solar simulator which, at the time of performing the experiments, was visible by eye. Moreover, $J_L$ cannot be directly extracted from the whole reverse current under light due to the invalidity of the superposition principle for the studied devices, which is beyond the scope of this thesis. To the author's knowledge, there is

no published work regarding the analysis of the reverse bias behaviour of these cells under light conditions reported in the literature. This could be a topic for further investigation.

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# Chapter 7: Measuring the Barrier Height of the CdTe Back Contact

## 7.1 Introduction

Making low resistance (i.e. Ohmic) back contacts for CdTe cells is one of the major barriers to improving the efficiency of these devices. Although high back contact barrier height affects neither $V_{oc}$ nor $J_{sc}$, it deteriorates *FF* and, therefore, the $\eta$ [1, 2]. This can be understood by considering that the back contact increases $R_s$. As a result, the slope of the *J-V* curve in the forward bias changes (i.e. becomes less steep) and reduces the "squareness" of the curve i.e. reduces *FF*.

It is discussed in Section 2.1 that creating an Ohmic contact (i.e. low resistance contact) to a p-type semiconductor requires that $\phi_m \geq \chi_s + E_g$. In the case of CdTe, $\chi_s$ and $E_g$ are 4.5 eV and 1.4 eV respectively [3], which means that in order to form a low resistance contact to p-type CdTe the metal work function must be ≥ 5.9 eV. Such a metal does not exist. Hence, it is necessary to find alternative methods to overcome this issue. These methods can be categorised in general as follows [4]:

i) Creating a tunnelling contact by heavily doping the back surface of the semiconductor to produce a $p^+$-type layer between it and the metal. This behaviour is explained in Section 2.1.

ii) Changing the stiochiometry of the semiconductor surface (to Te-rich in the case of CdTe cells) by etching, which leads to the same effect.

iii) Introducing a highly conductive p-type semiconductor (which can be contacted more easily with metals) with high electron affinity and low $E_g$ on the back surface of the cell.

A survey for five methods of the back contact barrier height measurement is presented in Section 7.2. Two of these methods were selected to conduct a preliminary study in Section 7.3, in which the validity of these two methods was investigated by comparing the values of the barrier height extracted by using them. The samples investigated in the preliminary study are the same samples studied in Chapter 6. The most appropriate method was used to investigate various contacts in Section 7.4. These contacts were either Au, $Sb_2Te_3$ or $As_2Te_3$, combined with either

as-grown or etched CdTe back surface. Two methods were used for etching, dry by $Ar^+$ plasma and wet by N-P solution. The conclusion of this Chapter is presented in Section 7.5.

## 7.2 Measuring the back contact barrier height $\phi_b$

Five methods of measuring the back contact barrier height for CdTe solar cells are discussed in this Section and two of these were selected for use in experiments. Most, but not all of the methods use *J-V-T* data.

*Method I*

Bätzner *et al.* [5] measured $R_s$ of a solar cell as a function of $T$. The authors proposed that $R_s(T)$ can be separated into a) an Ohmic part, and b) an exponential part resulting from passage of the carriers over the back contact barrier by thermionic emission. As a result, $R_s$ is expressed as

$$R_s = R_{\Omega 0} + \frac{\partial R_{\Omega 0}}{\partial T} T + \frac{C}{T^2} \exp(\frac{\phi_b}{kT}) \qquad (7.1)$$

where $R_{\Omega 0}$ and $\frac{\partial R_{\Omega 0}}{\partial T}$ are the Ohmic resistance and its temperature coefficient respectively, $C$ is a fitting parameter, $k$ is the Boltzmann constant and $\phi_b$ is the back contact barrier height. Fitting of $R_s(T)$ to this equation was used to determine $\phi_b$ in [6] and [7].

*Method II*

Stollwerck and Sites [1] measured the barrier height by proposing the two-diode model, which assumes the back contact and main junctions as two separate diodes. This assumption is valid when the total thickness of absorber layer is larger than the sum of depletion regions for both main and back junctions. These two diodes are connected back-to-back to each other. Furthermore, the back diode was assumed to be both partially shunted and light insensitive.

The procedure of the above method is to fit the experimental *J-V* data to equation 2.10

$$J = J_0\{\exp[\frac{q(V - JR_s)}{nkT}] - 1\} + \frac{V - JR_s}{R_{sh}} - J_L \qquad (2.10)$$

The fit was performed [1] by using the experimental values of $J$ and then calculating $V$ for each data point. The difference between experimental and calculated values of $V$ is called $\Delta V$, which was assumed to be the voltage drop across the back contact. $\Delta V$ was then fitted to the equation

$$J = -J_{0b}\left(\exp[\frac{-q\Delta V}{kT}] - 1\right) + \frac{\Delta V}{R_b} \qquad (7.2)$$

where

$$J_{ob} = J_{00}\exp\left(\frac{-q\phi_b}{kT}\right) \qquad (7.3)$$

and

$$J_{00} = qN_A V_{th} \qquad (7.4)$$

where $J_{0b}$ is the saturation current for the back diode, $R_b$ is the shunt resistance of the back diode, $\phi_b$ is the back contact barrier height, $N_A$ is the doping concentration of the absorber layer in the solar cell, $V_{th}$ is the thermal velocity and the rest of symbols have their usual meanings. It is seen from equation 7.3 that $\phi_b$ can be evaluated from the semi-log plot of $J_{0b}$ versus $1/T$.

*Method III*

Koishiyev *et al.* [8] used the same two-diode model as in Method II to evaluate the barrier height of the back contact. In this method, the value of $J$ in which $J$-$V$ curve starts to roll-over was called the turning current $J_t$. $J_t$ was determined as the intercept of two straight lines which are the resultants of linear fits to the data before

and after roll-over in the *J-V* curve, as shown in Figure 7.1. $J_t$ was considered as the saturation current for the back contact diode $J_{0b}$, which is given by

$$J_{0b} = J_t = A^* T^2 \exp\left(\frac{-q\phi_b}{kT}\right) \qquad (7.5)$$

where $A^*$ is the Richardson constant and the rest of symbols have their usual meanings. The experimental data of $J_t$ versus $T$ were fitted to equation 7.5 with both $A^*$ and $\phi_b$ being adjustable parameters. The fits are relatively insensitive to the values of $A^*$ used, and choosing reasonable estimates for both parameters allows a solution to be converged upon rapidly.

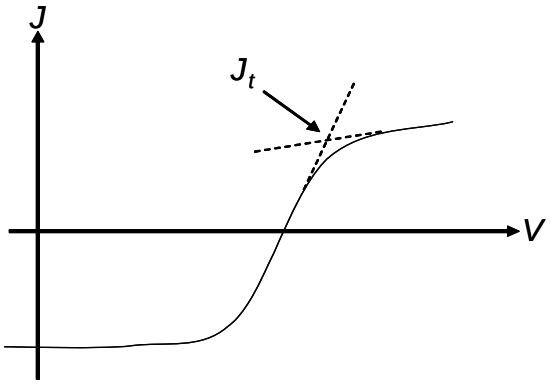


**Figure 7.1**: A *J-V* curve showing roll-over effect. The dashed lines represent the linear extrapolation by which $J_t$ is determined.

*Method IV*

McCandless *et al.* [9] also used the two-diode model to develop a method for measuring the barrier height. Furthermore, $R_s$ was assumed to be the sum of a) the back contact resistance $R_c$, and b) a temperature-independent lumped resistance $R_0$.

$$R_s = R_c + R_0 \qquad (7.6)$$

The back contact diode current $J_c$ is expressed as

$$J_c = -J_{0b}\left(\exp\left(\frac{-qV_c}{n_c kT}\right)-1\right) \qquad (7.7)$$

where

$$J_{0b} = J_{00c}\exp\left(\frac{-\phi_b}{kT}\right) \qquad (7.8)$$

$J_{00c}$ is a constant, $V_c$ is the voltage across back contact and $n_c$ is the ideality factor for back contact. If $\frac{qV_c}{n_c kT} << 1$, then equation 7.7 can be rewritten as

$$J_c \approx \frac{qV_c J_{00c}}{n_c kT}\exp\left(\frac{-\phi_b}{kT}\right) \qquad (7.9)$$

By using equations 7.6 and 7.9

$$R_c = R_s - R_0 \approx \frac{n_c kT}{qJ_{00c}}\exp\left(\frac{\phi_b}{kT}\right) \qquad (7.10)$$

$R_0$ is determined using the assumption that $R_c \approx 0$ at high temperature, and therefore $R_0 \sim R_s$. After measuring $R_s$ at various $T$, $\phi_b$ can be determined from plotting $R_c$ versus $1/T$ (equation 7.10).

*Method V*

Demtsu and Sites [10] simulated the *J-V* curve by generating it analytically as follows: $J_m$ and $J_b$ are the current densities across main and back junctions respectively, and they can be expressed as

$$J_m = J_{m0}\left[\exp\left(\frac{qV_m}{nkT}\right)-1\right] - J_L + \frac{V_m}{R_{sh}} \qquad (7.11)$$

and

$$J_b = -J_{b0}\left[\exp\left(\frac{qV_b}{kT}\right)-1\right]+\frac{V_b}{R_{sh}^b} \qquad (7.12)$$

where $J_{m0}$ is the saturation current density for main junction, $V_m$ is the voltage drop across main junction, $R_{sh}$ is the shunt resistance of main junction, $J_{b0}$ is the current density of back junction, $V_b$ is the voltage drop across back junction, $R_{sh}^b$ is the shunt resistance of back junction and the rest of symbols have their usual meanings. Since the same current passes in both junctions, equations 7.11 and 7.12 give

$$J_{m0}\left[\exp\left(\frac{qV_m}{nkT}\right)-1\right]-J_L+\frac{V_m}{R_{sh}}+J_{b0}\left[\exp\left(\frac{qV_b}{kT}\right)-1\right]-\frac{V_b}{R_{sh}^b}=0 \qquad (7.13)$$

The values of $J_{m0}$, $n$ and $R_{sh}$ are obtained experimentally [10]. $J_{bo}$ is the current where roll-over starts to appear in the *J-V* curve (as explained in Method III, equation 7.5 and Figure 7.1). Equation 7.13 was solved analytically, and the resulting data were fitted to the experimental *J-V* characteristics in order to obtain other parameters. The value of the back contact barrier height is estimated from this fitting.

Of the five methods discussed above, Methods I and III were selected for use in the present work. Firstly, both of these methods do not suffer from the difficulties in implementation of the others. For example, Method II requires accurate values of both $R_{sh}$ and $R_s$ in order to perform correct fitting to equation 2.10. Additionally, this method requires data fitting three times in order to determine $\phi_b$, which increases the possibility of errors. In Method IV it is assumed that $R_s = R_0 + R_c$, where $R_c = 0$ at high $T$. However, the temperature at which this approximation becomes valid is not known with any certainty. In Method V, the direct fitting of *J-V* curves demands accurate knowledge of a number of unknown variables which must be determined from other experiments. On the other hand, Method I is a self-contained fitting procedure for $R_s$ versus $T$ that may be applied to any cell device. Method III utilises the roll-over of *J-V* curves that is known to be a consequence of the back contact barrier itself. Moreover, Methods I and III invoke different physics for the analysis,

and hence provide an interesting comparison of methods for determining $\phi_b$. This is explored in the preliminary study presented in Section 7.3.

## 7.3 Preliminary study to test the validity of two different methods of measuring $\phi_b$

### 7.3.1 Introduction

$\phi_b$ was evaluated by two different methods, Method I and Method III from Section 7.2, in order to examine the validity of these tests by comparing their values with each other. The approach is completely different in each method as explained in Section 7.2. While Method I relies on the dependence of $R_s$ on $T$, Method III determines $\phi_b$ by considering the roll-over behaviour in $J$-$V$ characteristics at a range of $T$ i.e. $J_t$ versus $T$.

In this work Method I (Bätzner *et al.* [5]) was modified slightly. While Bätzner used a three term fit to the temperature dependence of $R_s$, as shown in equation 7.1, this was re-evaluated using the $R_s$ versus $T$ data in ref. 5. At high temperature, the first (constant) and second (linear) terms are greater than the third (exponential) term. However, at low temperature i.e. $\leq$ 300 K, the exponential term is much greater than the constant and linear terms combined. Typically, this term is at least $10^2$ and often $10^5$ times higher. Hence for data recorded at $T \leq$ 300 K – as in the experiments that follow – it is valid to approximate equation 7.1 as

$$R_s = \frac{C}{T^2}\exp\left(\frac{\phi_b}{kT}\right) \qquad (7.14)$$

Equation 7.14 is therefore used instead of 7.1 for the rest of this work.

The second method used here (Method III) depends on locating the turning point of the $J$-$V$ curve in order to identify a current value $J_t$. While Koishiyev [8] achieved this by extrapolation, in this work the differential plot $dJ/dV$ versus $V$ was used as shown in Figure 7.2b. This has the advantage that the turning point may be established from curves for which the roll-over effect is weak, as shown in Figure 7.2. $J_t$ is therefore easier to distinguish using this method than by extrapolation. This method also has the advantage that the voltage associated with the turning point itself

is accurately identified, whereas the intercept method used in reference 8 leads to a slight systematic over estimation of this value.

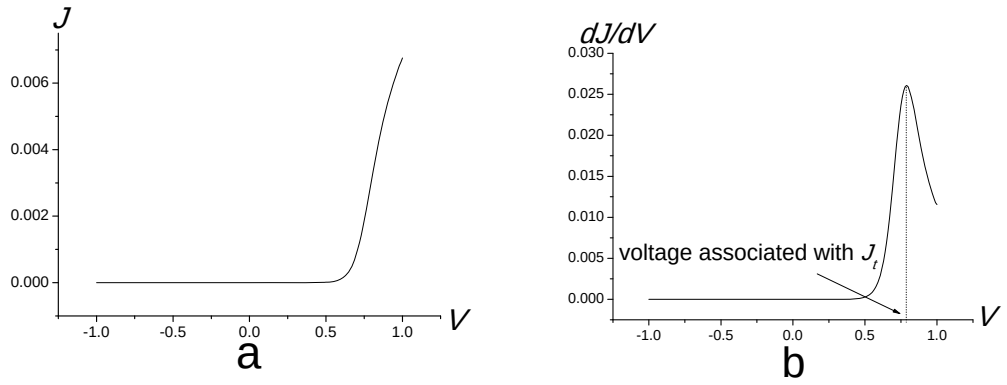


**Figure 7.2**: a) A normal *J-V* curve showing a slight roll-over effect. b) *dV/dJ* vs. *V* for the same data in (a) showing a clearer turning point i.e. $J_t$, which was used to determine $\phi_b$.

It is important to note that only dark *J-V-T* data were considered to determine $\phi_b$. This eliminates illumination-induced changes such as heating and possible changes in light intensity. Moreover, it has been reported that there was no variation in $\phi_b$ values extracted from both dark and light *J-V-T* [11]. This behaviour agrees with the assumptions of the two-diode model i.e. that diodes are independent and that the back diode is light insensitive. Light is not expected to reach the back contact for cells investigated in this work since CdTe thickness for all devices studied varied in the range of ~ 2.3 – 8 μm, and so visible light will be completely absorbed before reaching the back contact.

### 7.3.2 Experimental

#### 7.3.2.1 Sample fabrication

The samples investigated in this part were the same samples studied in Chapter 6 i.e. the samples for which the current transport mechanism was investigated. For details of the growth and processing the reader is referred Section 6.2.1 while a summary of the samples' components is given in Table 6.1. The principal difference of relevance to this Chapter is that sample 290 was CSS-grown

and has an Au/N-P etched contact while samples 254 and 305 are MOCVD-grown and have Au/CdTe:$As^+$ contacts. The contact types are listed along with the barrier height results in Table 7.1.

#### 7.3.2.2 *J-V-T* measurements

The dark *J-V-T* data obtained in Chapter 6 were used again in this Section. Only dark *J-V-T* data were considered as discussed above. $R_s$ was obtained from the slope of *J-V* curves under forward conditions (Method A in Appendix A) for Method I. $J_t$ values were determined as explained in Section 7.3.1 for measuring $\phi_b$ using Method III.

### 7.3.3 Results and discussion for the preliminary study

Figure 7.3 shows plots of $R_s$ versus $T$ for samples 290, 254 and 305. Fitting of these plots using Method I allowed extraction of values for the barrier height $\phi_b$. Figure 7.4 shows $J_t$ versus $T$ for the same cells, with $\phi_b$ being extracted using Method III. The results obtained from both methods are compared in Table 7.1.

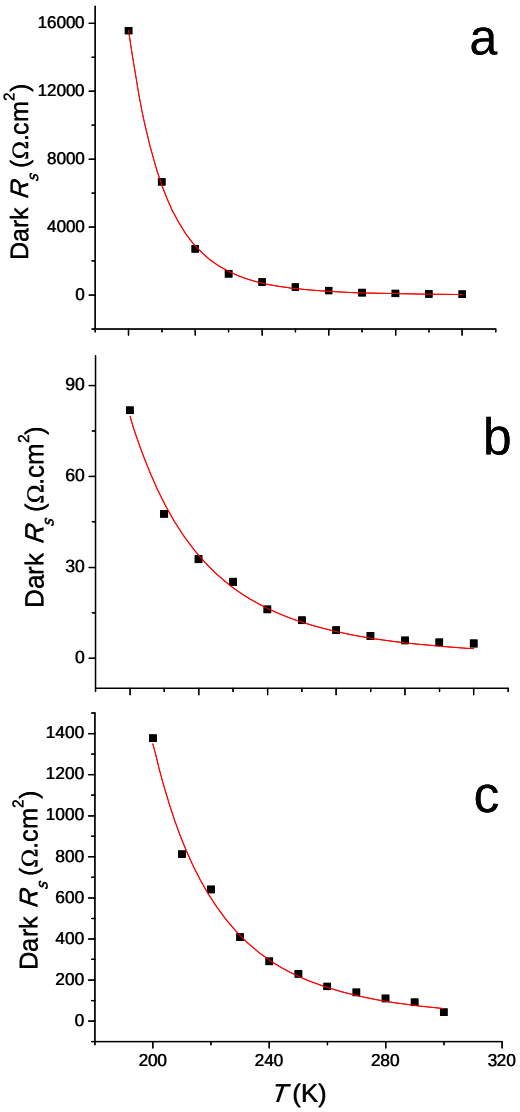


**Figure 7.3**: $R_s$ versus $T$ curves used to determine $\phi_b$ using Method I as described in Sections 7.2 and 7.3.1. a) sample 290, $\phi_b$ = 0.28 eV, b) sample 254, $\phi_b$ = 0.13 eV and c) sample 305, $\phi_b$ = 0.12 eV.

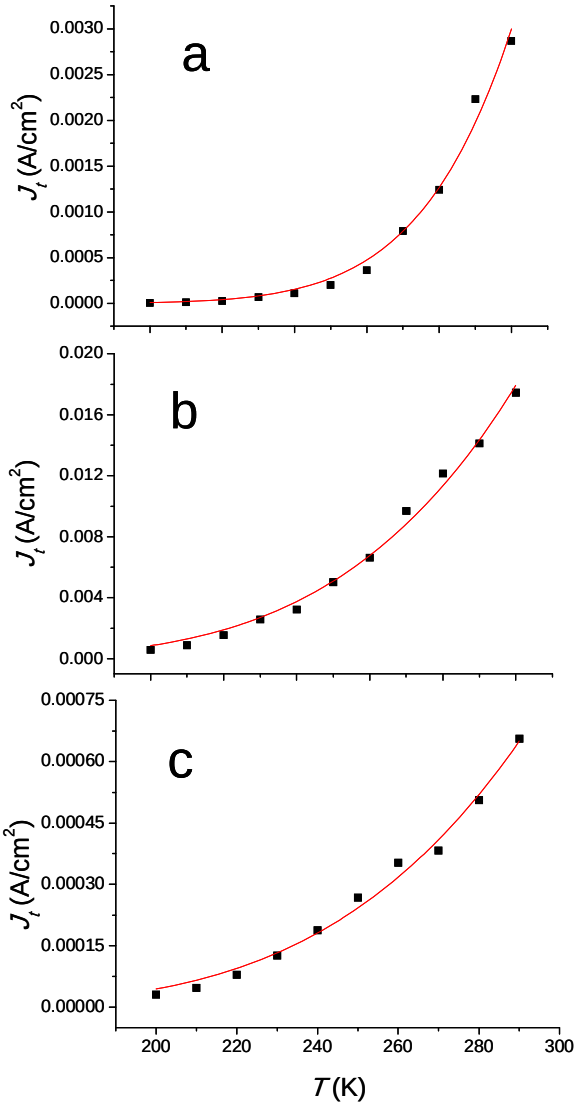


**Figure 7.4**: $J_t$ versus $T$ curves used to determine $\phi_b$ using Method III as described in Sections 7.2 and 7.3.1. a) sample 290, $\phi_b$ = 0.26 eV, b) sample 254, $\phi_b$ = 0.12 eV and c) sample 305, $\phi_b$ = 0.11 eV.

| Cell | Contact | Barrier height $\phi_b$ (eV) | |
|---|---|---|---|
| | | Method I | Method III |
| 290 | 2 mm dot Au/etched back surface | 0.28 | 0.26 |
| 254 | 2 mm dot Au/CdTe:$As^+$ | 0.13 | 0.12 |
| 305 | 5×5 mm square Au/CdTe:$As^+$ | 0.12 | 0.11 |

**Table 7.1**: The values of $\phi_b$ extracted by using Methods I and III for samples 290, 254 and 305.

It may be seen from the table that for each sample, Methods I and III yield barrier heights that agree to within ± 0.01 eV, this level of agreement being observed for samples with the lowest (~ 0.12 eV) and highest (~ 0.27 eV) barriers. This degree of agreement implies that either of the two methods may be used to give a comparable result. Moreover, since the two methods agree, even though the physical basis of each is different, this gives some confidence that both are giving a genuine measurement of the barrier height (this being despite slight modifications having been applied to both methods).

The fact that samples 254 and 305 had identical Au/CdTe:$As^+$ back contacts, which differed only in their size (254, 2 mm circular dot; 305, 5×5 mm square dot) allows further conclusions to be drawn about Method I. In particular since the series resistances of the two contacts differed in value by a factor of ~ 17 (see Figure 7.3 b and c), but the barrier heights nevertheless agree to ± 0.01 eV, it is clear that the absolute values of $R_s$ do not influence the outcome. Rather it is the temperature dependence behaviour of $R_s(T)$ that is important, and this is consistent with the approximation made for $R_s$, i.e. equation 7.14. It may be considered that the $\frac{C}{T^2}\exp\left(\frac{e\phi_b}{kT}\right)$ dependence of $R_s$ dominates the temperature-independent resistance ($R_0$). This is further confirmed by considering the factors that contribute to $R_s$ e.g. the grain size (large-grained samples have lower resistance) [12], the contribution of the TCO resistance ($R_s \propto$ the square of the lateral length of the current path in the TCO) [13], and the thickness of the TCO [14]: In all these three cases, their contribution to $R_s(T)$ is generally dominated by that of the back contact, as per equation 7.14. Further to this, it may be appreciated that errors in the measurement of $R_s$ have a little impact

on this temperature dependence, and do not therefore have a strong influence on the values of $\phi_b$ determined. This point was made in reference [7].

As discussed above, Method I relies only on the behaviour of $R_s(T)$, whereas Method III relies on $J_t(T)$. This means that Method III may not be usable unless roll-over appears in the *J-V* curves, which limits its applicability. Hence, Method I was selected for the comparison of the contacts in Section 7.4 as it is more applicable in comparison to Method III.

## 7.4 Investigation of materials and procedures for contacting CdTe solar cells

### 7.4.1 Introduction

This Section is concerned with using different materials for back contacting CdTe/CdS solar cells. Besides Au, which is the typical contact material for devices fabricated in research labs, both $Sb_2Te_3$ and $As_2Te_3$ were used to form back contacts. The CdTe back surface was either a) non-treated i.e. as-grown, or b) etched with i) N-P solution (wet etching), or ii) plasma (dry etching) prior to application of the contact layer.

### 7.4.2 Experimental

Eleven contact types were investigated in this Section. 5×5 cm TEC 15 Pilkington glass served as a substrate for all samples. CdS was grown by CBD by the author at Cranfield University as explained in Section 4.2.1. Prior to CdTe growth, CdS was annealed in $H_2$ ambient as described in Section 5.3.2.1. CdTe was grown by the CSS technique under a static pressure of ~ 6 Torr of $N_2$, while the source temperature was kept at 605°C and the substrate temperature was varied in the range of 460 - 510°C. The resultant thickness of the CdTe film was ~ 3 μm. All the CdTe growth runs took place consecutively and used the same source material to enhance the reproducibly of samples.

Each 5×5 cm plate was cut into four identical quarters prior to evaporating a 100 nm $CdCl_2$ and then annealing at 380°C for 10 minutes in air. The CdTe back surface was treated by either N-P wet etching or plasma dry etching for contacting. As

mentioned in Chapter 5, each sample was denoted by four digits, the first three together denote the plate number while the fourth denotes the quarter. The details of both wet and dry etching procedures are described in Section 4.3.1f. The back surface treatment was the same for three of the quarters from the same plate. However, an un-etched sample from each different plate was contacted with Au for comparison.

The Au contact was applied by thermal evaporation whereas $As_2Te_3$, $Sb_2Te_3$ were deposited by sputtering followed by metallization with Mo. For more details about the deposition procedures for each material see Section 4.3.1g. No annealing treatment was undertaken after depositing the contacts. Table 7.2 summarises both the etching methods and contact materials used for all samples.

| **Sample** | **Etching** | **Contact** | ***T*** |
|---|---|---|---|
| 574-2 | N-P | Au | RT |
| 574-3 | None | Au | RT |
| 576-2 | Plasma | 100 nm $As_2Te_3$ then 200 nm Mo | 300°C |
| 576-3 | Plasma | 100 nm $Sb_2Te_3$ then 200 nm Mo | 300°C |
| 576-4 | Plasma | Au | RT |
| 578-1 | None | Au | RT |
| 578-2 | N-P | 100 nm $As_2Te_3$ then 200 nm Mo | 300°C |
| 578-4 | N-P | 100 nm $Sb_2Te_3$ then 200 nm Mo | 300°C |
| 579-1 | None | Au | RT |
| 579-2 | None | 100 nm $As_2Te_3$ then 200 nm Mo | 300°C |
| 579-3 | None | 100 nm $Sb_2Te_3$ then 200 nm Mo | 300°C |

**Table 7.2**: The contact and etching types for each sample investigated in this work. *T* represents deposition temperature of the contact, where RT means room temperature.

The contact size was controlled by a shadow mask, which has 5×5 mm square holes. The CdTe was scribed around each contact manually by using a scalpel in order to avoid edge effects i.e. collecting extra current from edges of the contact. Dark *J-V-T* characteristics were recorded for each back contact as explained in Section 7.3.2.2. Furthermore, Method I was used to determine $\phi_b$ as discussed in Section 7.3.3. PV performance for all cells was measured under an approximate AM1.5 spectrum at ~ 1000 $Wm^{-2}$.

### 7.4.3 Results and discussion

Figure 7.5 shows the fits of $R_s$ values versus $T$ to equation 7.14 for all samples. The values of $\phi_b$ obtained from the graphs are summarised in Table 7.3, along with the working parameters of the cells.

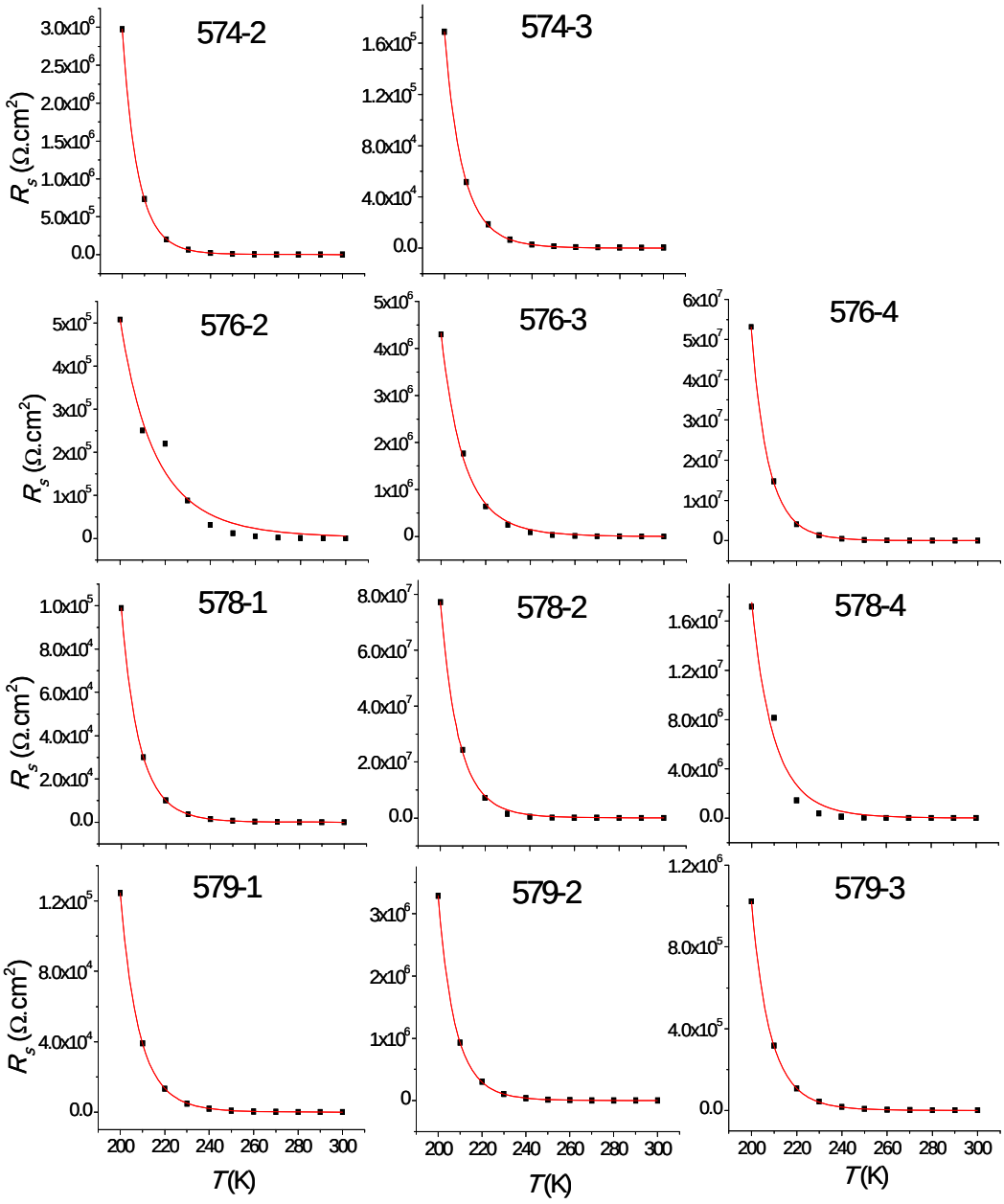


**Figure 7.5**: $R_s$ vs. $T$ for all contact types studied. The lines show the best fit to equation 7.14 using the barrier height $\phi_b$ as an adjustable parameter. Sample types are indicated on each graph by numbers – see Table 7.3 for details.

| Sample | Etching | Contact | $\phi_b$ (eV) | $\eta$ (%) | $FF$ (%) | $J_{sc}$ (mA/cm$^2$) | $V_{oc}$ (V) |
|---|---|---|---|---|---|---|---|
| 574-2 | N-P | Au | 0.47 | 5.4 | 45.37 | 18.51 | 0.64 |
| 574-3 | No | Au | 0.39 | 4.4 | 44.19 | 15.35 | 0.65 |
| 576-2 | Plasma | 200 nm Mo/100 nm $As_2Te_3$ | 0.19 | 3.1 | 36.05 | 17.57 | 0.61 |
| 576-3 | Plasma | 200 nm Mo/100 nm $Sb_2Te_3$ | 0.31 | 1.3 | 25.44 | 9.1 | 0.58 |
| 576-4 | Plasma | Au | 0.44 | 1.9 | 25.06 | 15.92 | 0.48 |
| 578-1 | No | Au | 0.4 | 5.7 | 49.21 | 18.96 | 0.61 |
| 578-2 | N-P | 200 nm Mo/100 nm $As_2Te_3$ | 0.4 | 3.5 | 31.6 | 18.71 | 0.6 |
| 578-4 | N-P | 200 nm Mo/100 nm $Sb_2Te_3$ | 0.32 | 2.3 | 23.95 | 15.87 | 0.61 |
| 579-1 | No | Au | 0.39 | 5.6 | 48.79 | 19.22 | 0.6 |
| 579-2 | No | 200 nm Mo/100 nm $As_2Te_3$ | 0.42 | 5.4 | 41.47 | 21.61 | 0.6 |
| 579-3 | No | 200 nm Mo/100 nm $Sb_2Te_3$ | 0.39 | 3.6 | 29.35 | 20.37 | 0.6 |

**Table 7.3**: $\phi_b$ values and PV performance parameters for the samples listed in Table 7.2.

*Control samples with Au/non-etched CdTe*

The Au contact with no pre-etching was applied to samples grown in three separate CSS-runs and therefore acted as a control. These samples (574-3, 578-1 and 579-1) all gave barrier height of 0.39 ± 0.1 eV, demonstrating the reproducibility of contacting and of the measurement method. Furthermore, since the PV performance of the three cells varied by a factor of ~ 0.7, these measurements demonstrated that the barrier height measurement method is to some extent independent of the conversion efficiency. Hence the methodology of this work, i.e. to use non-optimised cells, is demonstrated to be a valid means of assessing the barrier height.

*Au contact with N-P and dry etching*

As seen in Table 7.3 that both etching procedures (wet and dry, samples 574-2 and 576-4 respectively) acted to increase the barrier height of Au contacts in comparison with non-etched samples, the increase being from 0.39 to 0.47 and 0.44 eV respectively.

Plasma etching happens by "sputtering" layers from the CdTe back surface by bombarding it with Ar ions. The aim of this kind of etching is to remove oxide layers from CdTe surface before contacting. However, if damage resulting from plasma etching is severe, it may result in lowering *FF* and therefore $\eta$, of cells due to the plasma-induced damages on the surface. This damage forms defects in the contact/CdTe interface reducing carrier collection (that may occur due to carrier recombination via these defects), *FF* and $\eta$ [15]. Plasma etching conditions (e.g. flux, temperature and time) are known to affect the resultant PV performance [15]. These conditions were not optimised in this study, which may lead to considerable damage for CdTe back surface.

Moreover, after plasma etching, the sample was removed from the sputtering unit in order to evaporate Au in a thermal evaporator. This means that vacuum was broken and the sample was exposed to air, which may create oxides on the back surface of the device. Both factors, a) the surface damage due to etching, and b) the surface oxidation because of exposure of air, may act together to increase $\phi_b$ for sample 576-4 compared to other samples with Au contact and non-treated CdTe.

The effect of N-P etch on the cell performance, on the other hand, is known to depend on: a) the exact composition of the etching solution [16], and b) the time of etching [6]. Proskuryakov *et al.* [6] reported that $\phi_b$ was reduced from 0.56 to 0.49 and 0.47 eV after etching in the same N-P solution used in this work for 5 and 10 seconds respectively, whereas it did not change with longer etching times up to 90 seconds. However, the timing procedure was different from that used in this work. While etching time started from immersing samples in the solution in this work, it started in Proskuryakov's work after the creation of small bubbles on CdTe back surface. In the author's experience, these bubbles take ~ 30 – 40 seconds to form, which means that the shortest actual etching time in Proskuryakov's work was at least 35 seconds. Hence, the etching time used in this work (10 seconds) may be inadequate to remove oxides and form a Te-rich layer on the back surface of the cells.

The observed increase in $\phi_b$ caused by N-P etching with the Au contact (574-2) may be due to a variety of causes. For example, the etching is known to attack the grain boundaries [17], to reduce the CdTe thickness and to promote the formation of a Te-rich surface. It is also possible that the DI water of washing step after etching (Section 4.3.1f) caused water to be trapped in the fissures remaining at grain boundaries. This could itself form oxides on the CdTe such as $CdTe_2O_5$, CdO [17]

and $CdTeO_3$ [15]. Ambient humidity is sufficient for formation of oxide layers which can increase the resistivity of CdTe surface [18]. Such oxides would create an M-I-S structure that could increase the observed barrier height, and therefore reduce *FF* [15].

*$Sb_2Te_3$ contact*

The barrier height for $Sb_2Te_3$ contacts on non-etched CdTe (Table 7.3, sample 579-3) was the same as for Au on a non-etched surface. However, contrary to the case for Au, deposition on both wet- and dry-etched CdTe *reduced* the barrier height to 0.32 and 0.31 eV respectively.

Both $Sb_2Te_3$ contact and the subsequent Mo layer were deposited at $T$ = 300°C as shown in Table 7.3. Hence, it can be speculated that any excess water left after N-P etch (as explained for the Au/N-P etched sample) was evaporated upon heating prior to application of the contact. This would eliminate the harmful effect of trapped water on the back contact of CdTe cells as discussed above. On the other hand, plasma etching reduced the barrier height due to removing oxide layers from CdTe back surface. Both plasma etching and contacting were undertaken in the same unit i.e. without exposure to air. Plasma etching conditions used in this work is expected to induce surface damage (as in the case of Au contact), however, the deleterious effect of it seems to be insufficient to increase $\phi_b$ when it was not combined with the exposure to $O_2$-containing ambient.

*$As_2Te_3$ contact*

$\phi_b$ for the $As_2Te_3$ contact was 0.42 for non-etched, decreasing to 0.4 eV for the N-P etched cell (samples 579-2 and 578-2 in Table 7.3). The same argument (as that for $Sb_2Te_3$) can be made for $As_2Te_3$ since its deposition conditions were identical to those for $Sb_2Te_3$ i.e. the removal of excess water due to high deposition temperature of the contact may help form a better contact than for room temperature metallization. However, for a plasma etched sample contacted with $As_2Te_3$ (sample 576-2), the barrier height was 0.19 eV, which is much lower than other contacts. This result may be inaccurate due to bad fit as shown in Figure 7.5. The reason of this behaviour is not clear and should be confirmed by repeating this run.

*Comments on device performance*

The performance of all devices varied significantly as seen in Table 7.3. However, this variation appears to be unrelated to the barrier height values. It was mentioned in Section 7.1 that high $\phi_b$ may affect only *FF* but not $V_{oc}$ or $J_{sc}$. Nevertheless, these two parameters (i.e. $V_{oc}$ and $J_{sc}$) did vary for these samples – for example, $V_{oc}$ varied from 0.65 V to 0.48 V (samples 574-3 and 576-4) while $J_{sc}$ varied from 21.61 mA/cm$^2$ to 9.1 mA/cm$^2$ (samples 579-2 and 576-3). This implies that the back contact was not the only limiting factor for PV performance.

Performance may vary across the same sample for several reasons such as thickness uniformity of layers, pinholes and heat distribution during $CdCl_2$ treatment. More variation may occur for samples with either $Sb_2Te_3$ or $As_2Te_3$ contacts due to the contact deposition temperature (= 300°C) compared to Au contact-based samples which was deposited at room temperature i.e. the additional heat treatment for $Sb_2Te_3$ and $As_2Te_3$ contact-based cells may be itself non-uniform. *FF* may change due to changes in $R_s$ that can occur from various origins as discussed in Section 7.3.3, which means that *FF* need not depend only on $\phi_b$. The effect of the barrier height may be dominated by the effects of other factors, which resulted in the inconsistency of the performance with variation in $\phi_b$.

By comparing all values of $\phi_b$ in Table 7.3, it can be concluded that $Sb_2Te_3$ is a promising back contact for CdTe devices, although the PV performance for cells contacted with it happened to be poorer in comparison with other cells. The performance of cells contacted with $Sb_2Te_3$ depends on the thickness, deposition temperature, sputtering power and post-growth annealing for back contact (both $Sb_2Te_3$ and Mo) [15]. In addition, dry etching can affect the performance of cells depending on its ambient, power and time [15]. More runs are needed to optimise both a) its growth conditions, and b) etching conditions in order to improve the performance of cells.

## 7.5 Conclusion

This Chapter started with describing the problematic feature of the CdTe contact, which occurs due to the fact that the electron affinity of CdTe is sufficiently high that there is no metal that may satisfy the equation $\phi_m \geq \chi_s + E_g$, i.e. capable of

making an Ohmic contact with CdTe. High resistive (rectifying) contacts may have a deleterious effect on the conversion efficiency of solar cells. The techniques commonly used to overcome this issue were outlined in Section 7.1.

Five methods of determining the back contact barrier height $\phi_b$ were described briefly in Section 7.2, from which the most applicable and potentially accurate two methods were selected (Methods I and III). However, slight modifications were applied to both methods in order to obtain more accurate results (Section 7.3.1). A preliminary study was performed on three CdTe cells having different contacts to compare their results with each other, and therefore test the reliability of the measurements. Both methods (Methods I and III) gave similar results for $\phi_b$ with a difference of ± 0.01 eV, leading to the conclusion that the determined values of $\phi_b$ are valid. Nevertheless, Method I was chosen to determine $\phi_b$ for other contacts in this Chapter due to its higher applicability compared to Method III (which may be used only if the roll-over effect appears in the *J-V* curve). The results obtained from the preliminary study showed that the barrier height is independent of a) PV performance of the cell, b) contact size and c) contact geometry.

The barrier height of contacts made with three materials (Au, $Sb_2Te_3$ and $As_2Te_3$) was investigated in Section 7.4, each material being paired with either N-P or plasma etching or else without pre-treatment. A set of three control samples (Au/non-etched CdTe) was investigated, and showed good reproducibility of the results ($\phi_b$ = 0.39 ± 0.01 eV). Both wet and dry etching increased $\phi_b$ for Au contacts ($\phi_b$ = 0.47 eV and 0.44 eV respectively). Water trapped on the CdTe (due to cleaning following the N-P etching) was speculated to create oxides on the CdTe back surface, leading to higher values $\phi_b$ in comparison with $\phi_b$ values of the control samples. On the other hand, the combination of a) surface damage that may be created from a severe plasma etching, and b) the possible formation of oxides (due to breaking vacuum during contacting process) may be responsible of deteriorating the contact in the case of the plasma-etched sample.

The behaviour of the $Sb_2Te_3$ contacts differed from that of Au contacts although $\phi_b$ for both contacts (i.e. Au and $Sb_2Te_3$) with non-etched CdTe was similar. The improvement of the $Sb_2Te_3$ contact by N-P etching may be attributed to the evaporation of any excess water present on the CdTe as the contact deposition took place at $T$ = 300°C. The fact that $Sb_2Te_3$ was sputtered directly after plasma etching

of CdTe may suggest that the etching-induced surface damage was inadequate to increase $\phi_b$ in the absence of exposing the sample to an $O_2$-containing ambient before applying the contact.

The reason for the slight improvement of the $As_2Te_3$ contact with N-P etching compared to the non-etched one may be similar to that of $Sb_2Te_3$ contact i.e. evaporation of water during contacting. However, the bad fit of the data of $As_2Te_3$/plasma-etched sample to equation 7.14 (see Figure 7.5) may have resulted in an erroneous value of $\phi_b$, which therefore needs to be verified by further tests.

PV performance varied from a sample to another, with the variation being inconsistent with the values of the barrier height. The variation in performance among samples could be due to a) non-uniformity across each 5×5 cm plate, and b) irreproducibility of both growth runs and $CdCl_2$ treatment rather than the barrier height.

Finally, $Sb_2Te_3$ contacts gave the lowest barrier height among all other contacts, which implies that it can be a promising contact candidate for CdTe solar cells. However, a precise conclusion about the performance of this contact needs further tests in order to optimise its a) most suitable pre-growth treatment, b) growth conditions, and c) post-growth thermal treatment.

## 7.6 References for Chapter 7


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# Chapter 8: Summary, Conclusions and Suggestions for Further Work

## 8.1 Treatment of the CdS and its effect on devices as determined by a rapid screening method

The first part of Chapter 5 (Section 5.2) is concerned with both pre- and post-growth annealing of CdS/TCO bilayers. This work was motivated by that done by Alamri and Brinkman [1], in which both CdS/ITO and CdS/$SnO_2$ bilayers were post-growth oxidised. They found that (using In to contact the CdS) only CdS/ITO bilayer changed from being Ohmic to rectifying while CdS/$SnO_2$ remained Ohmic. This behaviour was attributed to the increase of the ITO work function due to oxidation. However, the results obtained from this work differed from these obtained by Alamri and Brinkman as discussed below.

It was essential to establish a test by which the coverage quality of CdS on the TCO could be examined. Au was used for this aim as it makes a Schottky contact with CdS, allowing to test the coverage simply by recording the *I-V* characteristics of the Au/CdS/TCO structure. The method – in which pinholes gave Ohmic behaviour and complete layers a Schottky contact – was successfully used to distinguish between good and bad layers. This gave confidence that the results obtained were not due to pinholes or shunting paths in the CdS. Use of this test allowed the selection of a high quality brand of ITO and the optimisation of sample preparation methods – both of which led to the fabrication of devices having a low density of pinholes.

Pre-growth treatment of the CdS/ITO bilayers was performed in both oxidising and reducing ambients, for various durations. The samples were contacted with In dots which makes an Ohmic contact with CdS, allowing to ascribe any change in the *I-V* characteristics to a change in the CdS/ITO interface. All samples showed Ohmic behaviour, suggesting no significant annealing-induced change in the CdS/ITO interface. However, post-growth treatment (same ambients used in the pre-growth treatment) displayed different effects than that of the pre-growth treatment. While post-growth reduction of the bilayers showed an Ohmic *I-V* behaviour, the *I-V* characteristics of the oxidised samples changed from Ohmic to rectifying, implying

changes on the surface of the CdS rather than the CdS/ITO interface. A high concentration of oxygen on the CdS surface was revealed using AES. The speculated reason for the rectification, therefore, was the creation of a CdO-$n^+$/CdS-n junction on the surface of the CdS. Contrary to Alamri's work, both CdS/ITO and CdS/$SnO_2$ bilayers behaved similarly. Therefore, the attribution of the rectification proposed by Alamri was unlikely and the Ohmic behaviour of the Alamri's oxidised CdS/$SnO_2$ sample is considered more likely to have occurred due to pinholes in the CdS.

The sense of rectification for the post-growth oxidised CdS/TCO bilayer (see Figure 5.3b) was opposite to that of the CdTe/CdS solar cell. This indicates that formation of oxides on the CdS surface may act to deteriorate the performance of the cell by blocking carriers. Therefore, this result suggests that CdS surface oxidation must be avoided during the fabrication process of the CdTe/CdS cells.

Annealing the CdS was further investigated in the second part of Chapter 5 (i.e. Section 5.3). The annealing was undertaken in three ambients, $N_2$, $H_2$ and $O_2$, prior to the growth of the CdTe to fabricate full devices. Moreover, this study included investigating the performance of the devices as a function of the CdTe thickness, which was performed by a rapid screening method. The methodology was to form a wedge–shaped CdTe layer on each CdS substrate by chemical bevelling the full device gradually, which allowed the performance to be tested as a function of CdTe film thickness. A preliminary study was conducted in order to choose the most suitable growth conditions for the sample used (Section 5.3.2.1): The experiments demanded smooth films for bevelling. The best set of results was obtained from a sample comprising CSS-CdTe:$O_2$/CBD-CdS/TEC 8 glass (Bevel 2). The performance of these cells showed a peak at CdTe thickness ~ 3 μm, which resulted from an optimum $CdCl_2$ treatment for this thickness i.e. $CdCl_2$ treatment was insufficient for thicknesses > 3 μm while thicknesses < 3 μm were over treated.

Furthermore, this was true for samples annealed under reducing, oxidising or neutral conditions. It has therefore been demonstrated that treating the CdS had an insignificant effect on the performance of all the cells, indicating that either a) annealing conditions used were unable to produce influential changes, or b) annealing effects were masked by those induced from the CdTe growth. A severe CdS treatment (i.e. higher temperature and ambient pressure than what was used in this study) may be worth investigating to test its ultimate effects on the PV performance.

The number of growth runs required to generate these results were reduced by a factor of ~ 30 compared to the number of conventional growth runs required to investigate the same range of thicknesses. The success of the application of this methodology may be of great importance for rapid screening the fabrication conditions for CdTe devices. The need of such experiments may help to increase the rapidity of improving the PV performance for all kinds of technologies, as it reduces not only the number of the required growth runs but also the need for run-to-run reproducibility of the runs.

The rapid screening method study applied here provided information about the optimum CdTe thickness for the $CdCl_2$ treatment used. However, a fully optimised cell may require a series of bevelled CdTe/CdS samples, for which various $CdCl_2$ treatments (i.e. $CdCl_2$ thickness, annealing time and annealing temperature) are used for optimisation. Such a series of samples may lead to obtain the best possible PV performance.

The wedge shape of the CdTe layer was formed by chemical etching as explained earlier. However, this shape might alternatively be created during the growth of the CdTe layer itself, so that the compositional changes introduced from etching can be avoided. This might be achieved, for example, by growing the CdTe layer using the sputtering technique without the rotation of the substrate. Such methods may be useful especially when etching the CdTe back surface is not desired.

## 8.2 Current transport mechanism in CdTe solar cells

The electrical current transport mechanism in CdTe solar cells was studied in Chapter 6 as a function of a) layer growth techniques, and b) window type. Both CSS- and MOCVD-grown cells were investigated, with the window layer being CdS for the former and either CdS or CdZnS for the latter. The current transport process for each cell was investigated under both forward and reverse bias conditions, in both the dark and the light (various intensities). *J-V-T* data collected under these conditions were analysed based on the transport mechanisms reviewed in Sections 2.5 and 3.6 to find the best fit of the data. Table 6.12 summarises the results obtained in Chapter 6.

It is seen from the table that under the forward bias condition in the dark, the current for CdTe/CdS cells grown by either CSS or MOCVD techniques was dominated by the multi-step tunnelling process. However, the transport mechanism

was by recombination in the depletion region for the CdTe/CdZnS cell, implying that the current transport process depended on the material rather than the growth technique used. Changes in the CdTe/CdZnS interface introduced by the diffusion of Zn into CdTe were thought to be the reason of having a different transport mechanism for the CdZnS-based cell (sample 305) compared to that for the CdS-based cells (samples 290 and 254). This assumption may be confirmed by characterising and comparing the trap distribution in such samples using techniques such as Deep Level Transient Spectroscopy (DLTS).

Contrary to the findings for forward biased current in the dark, current under the reverse bias condition in the dark was controlled by multi-step tunnelling for all cells i.e. the transport mechanism was independent of both the growth technique by which the layers of the cells were fabricated, and the material of the window layer. The reason for this could be the dominance of effects due to the relatively wide depletion region (due to the reverse bias conditions) over those that might arise from the diffusion of Zn near the CdTe/CdZnS interface as explained in Section 6.3.4.

It was possible to determine both the number of tunnelling steps ($R$) (under forward bias) and trap density ($N_t$) (under reverse bias) for samples having their current transport dominated by multi-step tunnelling. The values obtained ($R \sim 125 - 432$ steps and $N_t \sim 10^{14} - 10^{15}$ cm$^{-3}$) were comparable to those in the literature (Al-Allak *et al.* [2] for $R$ and Proskuryakov *et al.* [3] and Al-Amri [4] for $N_t$).

The method used to determine the ideality factor ($n$) for dark data (and therefore identify the transport mechanism) was unsuitable for light data. Thus, a new method (Section 2.5.4) was used for this, which uses the dependence of $V_{oc}$ on temperature. Moreover, by comparing various light intensities, the absolute intensity of the light source was eliminated from the calculations, which allows the method to be applied very easily. For all cells Shockley-Read-Hall (SRH) recombination dominated the current transport in the light under the forward bias. Light-induced changes in the material were speculated to be the reason for the change in the transport mechanism in the light compared to that in the dark. Carriers generated by the incident photons may neutralise/charge the interface states and therefore affect the electronic properties of the junction, which may in turn alter the current transport mechanism.

Both the noise and the domination of $J_L$ over the reverse current data in the light prevented investigation of the transport mechanism under these conditions. The

noise was attributed to flickering of the light source. On the other hand, the extraction of the absolute reverse current from the data (i.e. eliminating the effect of $J_L$ from the reverse data) was beyond the scope of this work. These issues may be the reason for the lack of studies regarding the current transport mechanism for illuminated devices under reverse bias in the literature.

It can be concluded from this work that recombination processes dominate the current transport mechanism in CdTe solar cells. This may arise from the localised energy states in the band gap created due to point defects or the mismatch between CdTe and the window layer for example. Carrier recombination may lead to [5] a) reduction in $J_L$ (or $J_{sc}$), and b) increase in the saturation current ($J_0$). These effects may reduce $V_{oc}$ (see equation 2.31), and therefore deteriorate the PV performance. Deep knowledge of the current transport in solar cells may facilitate the performance improvement by providing a means to evaluate the effect of processing designed to overcome limiting effects, for example, recombination. A known example is the effect of the $CdCl_2$ treatment on the reduction of interface states (and therefore recombination) in CdTe/CdS cells (see Section 3.6). This results in substantial improvement in efficiency from 1 – 3 to > 10 % or more.

## 8.3 Back contact for CdTe solar cells

Chapter 7 was concerned with determining the barrier height of the back contact of CdTe solar cells. Five methods used to determine the barrier height were reviewed in Section 7.2, from which two methods were chosen to conduct a preliminary study, by which the validity of their results was tested. Although the physical approach was different in each method (Method I relies on $R_s(T)$ while Method III relies on the roll-over effect as a function of temperature), the barrier height values were comparable. The samples investigated in the preliminary study allowed testing of the effect of a) N-P etching, and b) heavy As doping of the CdTe back surface, before metallization. Au was used to contact all samples, however, the size of the Au contacts differed between the samples (two samples had 2 mm diameter dot contacts while the third had 5 × 5 mm square contacts). The results showed that the barrier height was independent of both contact size and PV performance. The bigger contacts showed higher absolute values of $R_s$ than the small ones. However, the experimental component of the temperature dependence dominated all others and

hence the same value of contact barrier height was obtained for all contact sizes. This implies that the error in determining the absolute value of $R_s$ is negligible in comparison to the variation of $R_s$ with temperature.

Eleven contact types were investigated in Section 7.4 and they used combinations of a) various materials (Au, $Sb_2Te_3$ and $As_2Te_3$), and b) different CdTe etching methods (N-P and plasma). The back contact barrier height varied from contact type to type in these samples: Both etching methods increased the barrier height for Au contacts. This behaviour was attributed to a) water remaining on the CdTe back surface from the CdTe wet etching (N-P) step, b) etching-induced surface damage due to plasma etching and c) exposure to air before metallization (for the plasma etched sample). The *combination* of the last two reasons (b and c) were speculated to cause the increase of the barrier height for the Au/plasma-etched sample.

For $Sb_2Te_3$ and $As_2Te_3$ contacts, both etching methods reduced the barrier height (see Table 8.1), which was attributed (for N-P etched samples) to the evaporation of the remaining water (i.e. the trapped water speculated to be the reason of the increase of $\phi_b$ for Au/N-P etched sample) due to heating at a temperature of ~ 300°C during contacting. The reduction in the barrier height for the plasma etched samples was attributed to the removal of oxides from the CdTe back surface. The possible surface damage occurring from plasma etching did not increase the barrier height since no oxidation (i.e. exposure to air before metallization) was combined with it, as in the case of the Au contact. However, the bad fit of the $Sb_2Te_3$ contact data gave much lower value of the barrier height compared to other contacts, which requires repeat runs to be confirmed.

Although the back contact barrier height may affect the cell performance significantly, the variation in performance for cells investigated in Chapter 7 may be attributed to other reasons. It was mentioned in Section 7.1 that high barrier height reduces efficiency by reducing the *FF*. However, the variation in other parameters (i.e. $J_{sc}$ and $V_{oc}$) indicates that the variation of the efficiency independent from the *FF* is due to sources other than the back contact. The variation of a) TCO, b) CdS, c) $CdCl_2$ treatment (i.e. $CdCl_2$ itself, time and temperature) and d) the uniformity and coverage of the layers may introduce significant variation in the performance.

| Contact material | Etching method | $\phi_b$ (eV) |
|---|---|---|
| $Sb_2Te_3$ | None | 0.39 |
| | N-P | 0.32 |
| | Plasma | 0.31 |
| $As_2Te_3$ | None | 0.42 |
| | N-P | 0.4 |
| | Plasma | 0.19 |

**Table 8.1**: A summary of the barrier height values for both $Sb_2Te_3$ and $As_2Te_3$ contacts, with various etching methods for the CdTe back surface.

It has been reported that if the back contact barrier height is < 0.3 eV, it does not affect PV performance [6], and it can be considered as an Ohmic contact [7]. Therefore, a "suitable" back contact may be defined as the contact for which the barrier height is < 0.3 eV. Another consideration for choosing the back contact is the cost. It was mentioned in Section 1.2 that the manufacturing cost of PV represents the main limitation of this technology, therefore, using a relatively cheap contact may help to cut the cost and facilitate using PV.

The three materials used to contact the cells are now discussed. Au is widely used contact for p-type CdTe [8]. It is usually applied subsequent to etching the CdTe back surface, which creates a Te-rich layer (see Section 3.7). Besides the relatively high work function for Au (5.31 – 5.47 eV [9]), Au may diffuse in CdTe assisted by $V_{cd}$, and increase p-doping [8]. Moreover, the formation of $AuTe_x$ may act to reduce the barrier height too [8]. However, using Au for back contacting devices in industry may increase the manufacturing cost, and therefore using it is arguable.

Exploring the band alignment of both $Sb_2Te_3$ and $As_2Te_3$ with CdTe may help to compare between these materials in terms of performance as back contacts. A basic estimate of these band alignments may be determined using Anderson's rule (Section 2.1). However, they are not shown here due to the lack of information about the electronic properties of these materials in the literature.

The heavily doped CdTe back surface (i.e. CdTe:$As^+$ in the preliminary study, Section 7.3) showed a promising potentiality to make low resistance contact. The barrier height for the Au contact with N-P etching was higher than that of Au with

CdTe:$As^+$- based samples by a factor of > 2 (Table 7.1), which suggests this kind of surface treatment to be an alternative to etching. This layer (i.e. CdTe:$As^+$) should therefore be investigated with various metallization in order to choose the best material and treatment combination in terms of a) performance, and b) cost.

Both $As_2Te_3$ and $Sb_2Te_3$ were used to contact CdTe cells in this work as mentioned above. It was discussed in Section 3.7 that based on the work published by Romeo *et al.* [10], the advantage of the $Sb_2Te_3$ contact is that no Cu is required to achieve good performance, which leads to high stability for the cells. It does however require etching the CdTe back surface chemically, which may not be preferable for industry. $As_2Te_3$ on the other hand may be used without surface etching since the Te-rich layer formed by etching is replaced by the $As_2Te_3$ layer, which reacts with the Cu layer to form the desired $Cu_xTe$ phase for back contacting the devices. However, the Cu thickness and the substrate temperature must be monitored with a high level of precision to ensure the stability of the PV performance remains high. It was mentioned in Section 3.7 that the Cu layer must be 2 – 20 nm thick to avoid Cu diffusion in CdTe, and therefore avoid degradation. The uncertainty in applying such thicknesses may be high, for example if the Cu thickness required is 2 nm, adding another nm is a 50 % error. Also, the $Cu_xTe$ phase formed on the back surface varies with the substrate temperature. In the case of $As_2Te_3$ deposition, Cu needed to be deposited at a substrate temperature in the range 100 – 200 °C to ensure the desired $Cu_xTe$ phase was present [10]. Romeo *et al*. [10] reported that the conversion efficiencies were ~ 16 and 15.8 % for cells with $Sb_2Te_3$ and $As_2Te_3$ contacts respectively, showing that both contacts have comparable performance. Hence, other limiting factors such as cost and stability must be considered when comparing these two materials. Figure 3.3 shows the advantage of using such materials for contacting CdTe devices.

CdTe solar cell modules have been successfully mass produced for the PV market, a prime example of this being First Solar, currently the largest producer of PV modules in the world [11]. However, there is still significant room for improvement in the performance for CdTe devices. At present, the highest efficiency CdTe/CdS cell reported is 16.5 % [12], with $V_{oc}$ and $J_{sc}$ that are ~ 58 and 87.7 % of their maximum values respectively, suggesting that $V_{oc}$ may have the highest scope for improvement.

*FF* (which was 75.51 % for the record cell) may be increased by increasing $R_{sh}$ and decreasing $R_s$ for cells. The latter may be achieved through using a low resistance back contact. The back contact used in this record cell contained HgTe:CuTe-doped carbon paste. However, as mentioned earlier, using a Cu-containing contact might be problematic for the stability of devices, especially in the long term. Hence, forming a low resistance (i.e. Ohmic) and stable contact for CdTe cells may still be a demand for enhancing their performance.

The main factors believed to increase the efficiency of CdTe cells involve increasing carriers in CdTe, reducing recombination and reducing the back contact barrier height [13]. This discussion shows that the PV performance for CdTe cells may be further improved, which may in turn lead to cheap and stable modules. Such improvements require profound understanding of the CdTe properties, which may make CdTe a rich area of research.

## 8.4 References for Chapter 8


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# Appendix A: Methods for determining series resistance of solar cells ($R_s$)

## A.1 Introduction

Six methods were used to determine the series resistance $R_s$ of the solar cell. In Chapter 7, the barrier height of the CdTe/CdS solar cell back contact was determined using a method relying on the behaviour of $R_s$ as a function of $T$ (Method I in Section 7.2). Therefore, it was important to test various methods to select the most suitable one for the back contact study.

This Appendix presents a brief description for these methods along with the results extracted from them. In each section, the behaviour of $R_s(T)$ is demonstrated by plotting selected values of $R_s$ versus $T$.

## A.2 Experimental

*J-V-T* data (both in dark and under various light intensities) for one CSS-CdTe/CdS sample were used in all methods in this Appendix. Both the experimental setup and the procedure for this measurement are described in Section 4.4.2. Details of the sample (sample 290) are presented in Section 6.2.1.

## A.3 Methods and Results

*Method A:*

$R_s$ can be calculated form the inverse of the slope of the *J-V* curve at $V \sim V_{oc}$ (for light data), as shown in Figure A.1a. If $R_{sh}$ is high, then equation 2.10 can be rearranged for $V$ as

$$V = \frac{nkT}{q}\ln\left(\frac{J + J_{sc} - J_0}{J_0}\right) + JR_s, \qquad \text{(A.1)}$$

Differentiating equation A.1 gives

$$\frac{dV}{dJ} = \frac{nkT}{q}\left(\frac{1}{J + J_{sc} - J_0}\right) + R_s, \qquad \text{(A.2)}$$

Under the open-circuit conditions (i.e. $V = V_{oc}$ and $J = 0$), equation A.2 becomes

$$R_s = \left.\frac{dV}{dJ}\right|_{V=V_{oc}} - \frac{nkT}{q}\left(\frac{1}{J_{sc} - J_0}\right) \qquad \text{(A.3)}$$

The second term in the RHS of equation A.3 is negligible in comparison to the resistance of the cell [1]. Therefore, for the illuminated *J-V* curve

$$R_s = \left.\frac{dV}{dJ}\right|_{V=V_{oc}} \qquad \text{(A.4)}$$

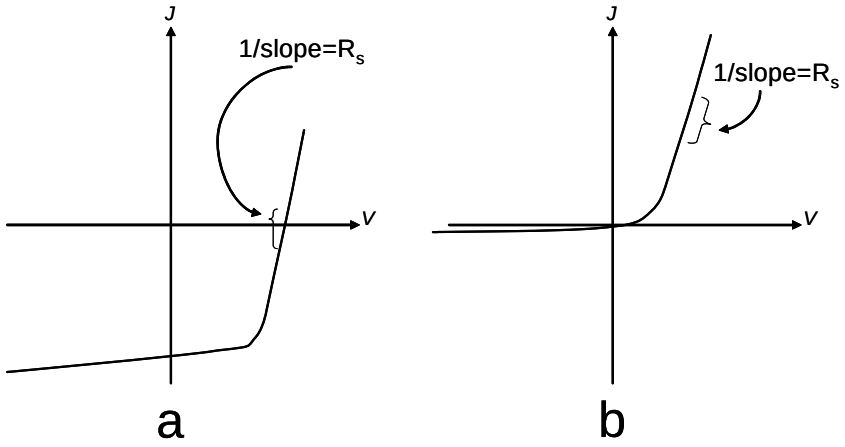


**Figure A.1**: Typical *J-V* curves for solar cells under illumination (a) and in the dark (b). The figure shows (in each curve) the division of the cureve from which $R_s$ is measured.

Similarly, dark $R_s$ can be calculated from dark *J-V* data by considering the slope of the curve in the forward region as shown in Figure A.1b. Several studies determined $R_s$ using this method [1-4].

Table A.1 and Figures A.2 and A.3 summarise the values of $R_s$ obtained using this method both in the dark and under illumination for a temperature range of 200 – 300 K.

| ***T*** ***(K)*** | ***$R_s$* dark** **($\Omega.cm^2$)** | ***$R_s$* light** **($\Omega.cm^2$)** |
|---|---|---|
| 300 | 39 | 8 |
| 290 | 50.9 | 9.3 |
| 280 | 86.7 | 10.6 |
| 270 | 127.2 | 11.7 |
| 260 | 253.2 | 12.6 |
| 250 | 456.6 | 13.3 |
| 240 | 757.6 | 13.4 |
| 230 | 1234.7 | 14.3 |
| 220 | 2708.2 | 14.6 |
| 210 | 6662.2 | 15.9 |
| 200 | 15556.7 | 17.9 |

**Table A.1**: The $R_s$ values extracted using method A in both the dark and the light.

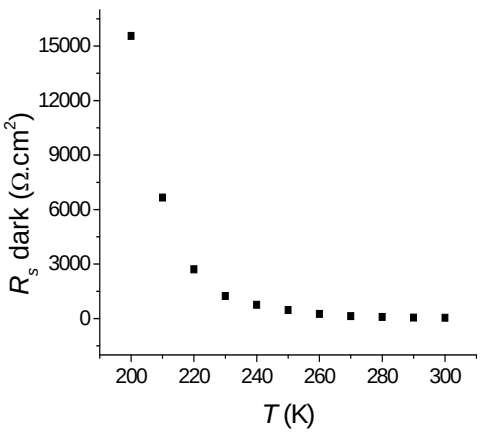


**Figure A.2**: Dark $R_s$ versus *T* as extracted using Method A.

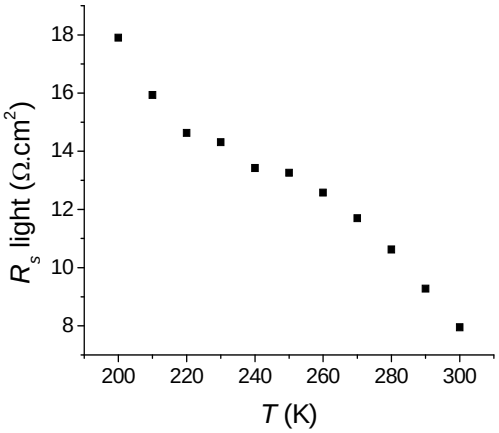


**Figure A.3**: Light $R_s$ versus $T$ as extracted using Method A.

*Method B:*

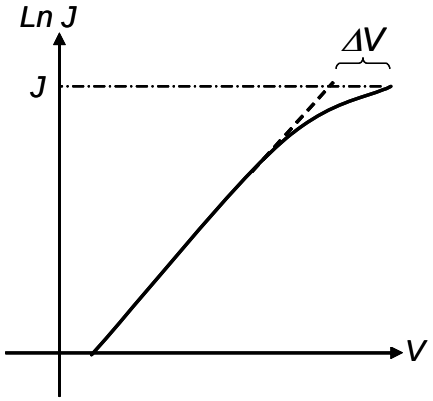


**Figure A.4**: ln$J$ versus $V$ plot illustrating the values needed to extract $R_s$ by using Method B.

In Section 2.4f and particularly in Figure 2.8, the effect of the $R_s$ on the plot ln$J$ versus $V$ (in forward bias) was illustrated i.e. deviation from linearity. This distortion can be used to determine $R_s$. In this method, $R_s$ is calculated from,

$$R_s = \frac{\Delta V}{J}, \qquad \text{(A.5)}$$

where $\Delta V$ is the difference in the voltage values between the experimental curve and its linear extrapolation as seen in Figure A.4, and $J$ is the current density corresponding to $\Delta V$. The determination of the $R_s$ by this method was reported by several authors e.g. [5, 6]. Table A.2 and Figure A.5 show the results of dark $R_s$ as a function of $T$.

| $T$ | $R_s$ dark ($\Omega.cm^2$) |
|---|---|
| 300 | 31.6 |
| 290 | 42.4 |
| 280 | 71 |
| 270 | 124.7 |
| 260 | 271.9 |
| 250 | 518.9 |
| 240 | 974.4 |
| 230 | 1642.3 |
| 220 | 3666.5 |
| 210 | 9030.5 |
| 200 | 18812.4 |

**Table A.2**: The $R_s$ values extracted using Method B in the dark.

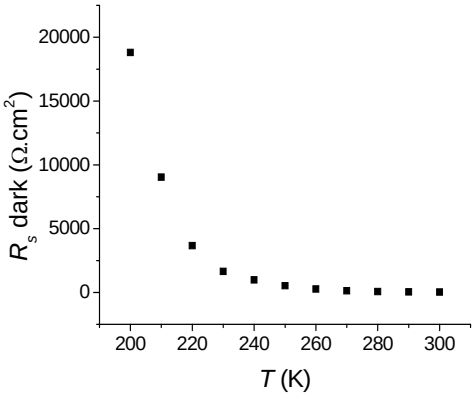


**Figure A.5**: Light $R_s$ versus $T$ as extracted using Method B.

Only dark values of the $R_s$ were determined by using this method. Light data were not analyzed due to the impossibility of taking the logarithm of negative values of the currents for $V < V_{oc}$. Furthermore, the roll-over effect dominated the currents for all $V > V_{oc}$.

*Method C:*

This method was proposed by Singh and Singh [7], in which the maximum power point ($P_{max}$) was used. At this point

$$\frac{dP}{dV} = 0, \qquad \text{(A.6)}$$

where $P$ is the power generated by the cell, and

$$P = (J_L + J_0)V - J_0 V\left[\exp\left(\frac{q(V + JR_s)}{nkT}\right)\right] \qquad \text{(A.7)}$$

Equation A.6 is equivalent to

$$\left(\frac{dJ}{dV}\right)_{P\max} = -\left(\frac{J}{V}\right)_{P\max} \qquad \text{(A.8)}$$

Using equation A.8 and differentiating equation 2.10 (assuming that $R_{sh}$ is sufficiently high)

$$\frac{J_{\max}}{V_{\max}} = J_0\left[\exp\left(\frac{q(V + JR_{s)}}{nkT}\right)\right]\frac{q}{nkT}\left(1 - \frac{J_{\max}R_s}{V_{\max}}\right) \qquad \text{(A.9)}$$

where $V_{max}$ and $J_{max}$ are voltage and current corresponding to the maximum power point generated by the solar cell. By using equation 2.10 at the maximum power point, equation A.9 can be rewritten as

$$\frac{J_{\max}}{V_{\max}} = \left(J_L - J_{\max}\right)\frac{q}{nkT}\left(1 - \frac{J_{\max}R_s}{V_{\max}}\right), \qquad \text{(A.10)}$$

or

$$R_s = \frac{V_{\max}}{J_{\max}} - \frac{nkT}{q(J_L - J_{\max})} \qquad \text{(A.11)}$$

The approximation that $J_L = J_{sc}$ was used in calculations. It is seen from equation A.11 that this method is not applicable for the dark data due to the existence of $V_{max}$ and $J_{max}$ in the equation. Table A.3 presents $R_s$ values for all the light intensities used in this study. Figure A.6 shows $R_s$ results corresponding to the 100 % illumination as a function of $T$.

| | **$R_s$ ($\Omega$.cm$^2$)** | | | | |
|---|---|---|---|---|---|
| ***T*** | **100 % light** | **79 % light** | **50 % light** | **20 % light** | **10 % light** |
| 300 | 63.6 | 80 | 122 | 287.1 | 498.8 |
| 290 | 78.1 | 97.5 | 148.9 | 365.7 | 675.3 |
| 280 | 80.1 | 100.8 | 153.6 | 379.7 | 687.1 |
| 270 | 82.3 | 103.5 | 157.4 | 379.1 | 723.2 |
| 260 | 84.3 | 104.9 | 158.5 | 382.5 | 704.8 |
| 250 | 84.4 | 105.7 | 160 | 395.2 | 724.7 |
| 240 | 83.7 | 105.6 | 157.8 | 387.8 | 710.7 |
| 230 | 84.7 | 105.3 | 159.5 | 382 | 731.8 |
| 220 | 84.2 | 105.9 | 159.5 | 380.2 | 699.6 |
| 210 | 88.1 | 110.3 | 165.8 | 394 | 783.3 |
| 200 | 90.3 | 113.9 | 167.8 | 397.1 | 736.7 |

**Table A.3**: The $R_s$ data extracted using Method C for different light intensities.

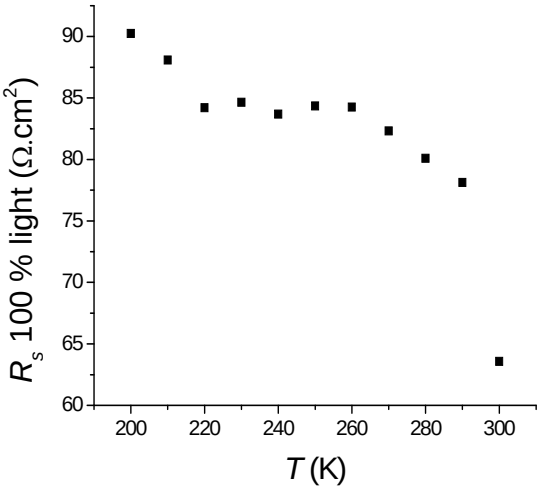


**Figure A.6**: The results of $R_s$ for the cell under 100 % illumination (AM1.5) versus $T$ as extracted using Method C.

*Method D:*

Method D uses both dark and light *J-V* data to extract $R_s$. If $R_{sh}$ is high then equation 2.8 can be used to express the dark current $J_d$ as [8]

$$V_d = \frac{nkT}{q}\ln(\frac{J_d}{J_0}) - J_d R_s \qquad \text{(A.12)}$$

where $V_d$ is the voltage corresponding to $J_d$. If $J_L >> J_0$, then equation 2.31 becomes

$$V_{oc} = \frac{nkT}{q}\ln(\frac{J_L}{J_0}) \qquad \text{(A.13)}$$

By subtracting equation A.13 from equation A.12 (and considering $J_L = J_{sc}$)

$$V_d - V_{oc} = \frac{nkT}{q}\left[\ln\frac{J_d}{J_0} - \ln\frac{J_{sc}}{J_0}\right] - J_d R_s \qquad \text{(A.14)}$$

$$V_d - V_{oc} = \frac{nkT}{q}\left[\ln J_d - \ln J_0 - \ln J_{sc} + \ln J_0\right] - J_d R_s \qquad \text{(A.15)}$$

$$V_d - V_{oc} = \frac{nkT}{q}\left[\ln J_d - \ln J_{sc}\right] - J_d R_s \qquad \text{(A.16)}$$

$$V_d - V_{oc} = \frac{nkT}{q}\ln\frac{J_d}{J_{sc}} - J_d R_s \qquad \text{(A.17)}$$

$$R_s = \frac{1}{J_d}\left(\frac{nkT}{q}\ln\frac{J_d}{J_{sc}} - V_d + V_{oc}\right) \qquad \text{(A.18)}$$

The $R_s$ effect on the *J-V* curve of a solar cell is more pronounced at high voltage than low voltage (Figure 2.8). Hence, $V_d$ was chosen to be 1 V, which was the maximum value of the voltage applied. The results obtained using this method are summarized in Table A.4 and shown in Figure A.7.

| ***T*** | ***R<sub>s</sub>*** **(Ω.cm$^2$)** |
|---|---|
| 300 | 38.9 |
| 290 | 67.4 |
| 280 | 111 |
| 270 | 192 |
| 260 | 323.3 |
| 250 | 527.3 |
| 240 | 730.8 |
| 230 | 1023.3 |
| 220 | 1216.3 |
| 210 | 1383.5 |
| 200 | 1396.6 |

**Table A.4**: The $R_s$ data extracted using Method D.

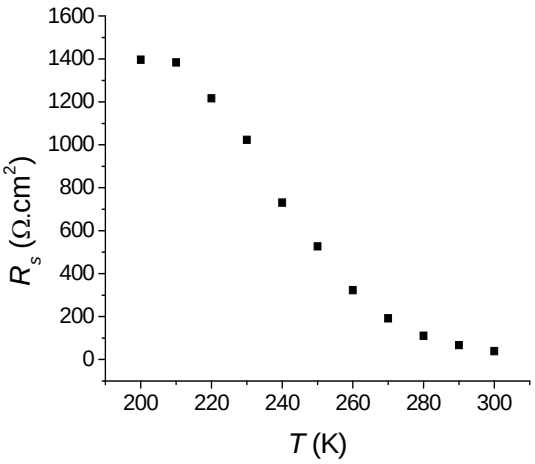


**Figure A.7**: The results of $R_s$ extracted from Method D as a function of $T$.

*Method E:*

This method was proposed by El-Adawi and Al-Nuaim [9]. Equation A.1 is rearranged to be

$$JR_s = V - \frac{nkT}{q}\ln\left(\frac{J + J_L + J_0}{J_0}\right) \qquad \text{(A.19)}$$

By applying this equation to any two points on the $J$-$V$ curve (and assuming that $J_0$ is negligible compared to $J_L$), and then subtract the resulting equations from each other $R_s$ can be expressed as

$$R_s = \frac{nkT}{q}\frac{1}{J_2 - J_1}\ln\left[\frac{J_L - J_2}{J_L - J_1}\right] - \left(\frac{V_2 - V_1}{J_2 - J_1}\right), \qquad \text{(A.20)}$$

where $J_1$, $J_2$, $V_1$, and $V_2$ are current densities and voltages for the two points selected from $J$-$V$ curve respectively. $R_s$ was measured for data collected under different light intensities as shown in Table A.5. The result of $R_s$ versus $T$ for 100 % illumination is shown in Figure A.8.

| | $R_s$ ($\Omega$.cm$^2$) | | | | |
|---|---|---|---|---|---|
| ***T*** | **100 % light** | **79 % light** | **50 % light** | **20 % light** | **10 % light** |
| 300 | 65.3 | 80.4 | 124.2 | 230.1 | 307.1 |
| 290 | 76.3 | 101.2 | 160.7 | 271.8 | 390.1 |
| 280 | 83.6 | 115.9 | 168 | 382.1 | 531.7 |
| 270 | 100.6 | 127.6 | 215.8 | 443.4 | 769.7 |
| 260 | 96.3 | 162.9 | 233.4 | 589.5 | 943.2 |
| 250 | 105.4 | 148.2 | 272.2 | 527.4 | 1059.2 |
| 240 | 129.2 | 149.5 | 289.2 | 724.2 | 1219.2 |
| 230 | 128.9 | 147.5 | 284.9 | 872.6 | 1362.8 |
| 220 | 106.2 | 135.1 | 241.2 | 762.9 | 1375.9 |
| 210 | 101 | 122.9 | 236.9 | 651.6 | 1519.1 |
| 200 | 80.3 | 105 | 215.4 | 600.4 | 1505 |

**Table A.5**: The $R_s$ data extracted by using Method E for different light intensities.

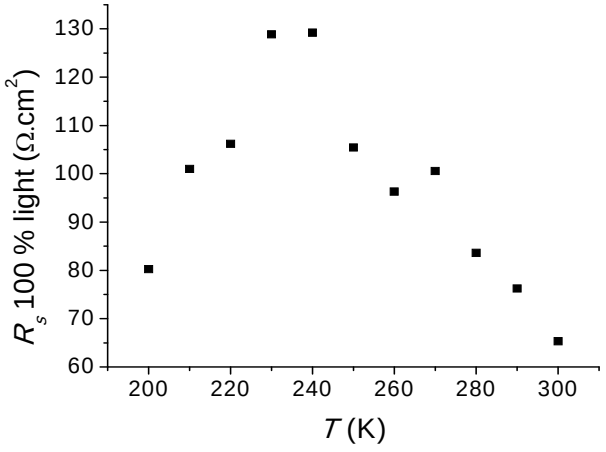


**Figure A.8**: The results of $R_s$ (Method E) for the cell under 100 % illumination (AM1.5) versus *T*.

*Method F:*

$R_s$ was measured by using a characterizing software called CurVA, which was created and developed in Colorado State University. The theoretical background of CurVa is based on a paper published by Hegedus and Shafarman [10]. By recalling equation 2.10, and considering the case where $R_{sh} = \infty$ and $R_s$ has a finite value, it can be written that

$$\frac{dV}{dJ} = R_s + \frac{nkT}{q(J + J_L)} \qquad \text{(A.21)}$$

Therefore, $R_s$ is the intercept of *dV/dJ* versus $(J + J_L)^{-1}$ plot. $R_s$ was evaluated for both dark and 100 % illuminated data by using CurVA. The results of these curves are summarized in Table A.6, and the dark results are shown in Figure A.9.

| ***T*** | **$R_s$ dark ($\Omega.cm^2$)** | **$R_s$ light ($\Omega.cm^2$)** |
|---|---|---|
| 300 | 19.5 | 0.7 |
| 290 | 23.7 | -2.6 |
| 280 | 81 | 4.2 |
| 270 | 35 | -5.8 |
| 260 | 50.9 | -0.1 |
| 250 | 120.8 | 2.4 |
| 240 | 177.2 | 0.5 |
| 230 | 349.5 | 4.5 |
| 220 | 601 | 7.1 |
| 210 | 1153.7 | 4.7 |
| 200 | -704.4 | 2.7 |

**Table A.6**: The $R_s$ values extracted by using Method F in both dark and light.

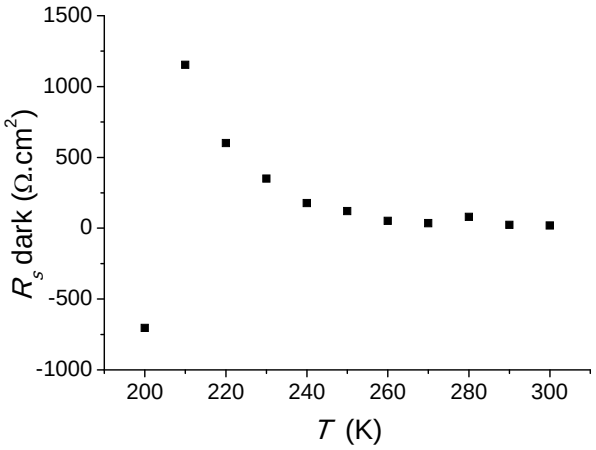


**Figure A.9**: Dark $R_s$ versus $T$ as extracted from method F.

## A.4 Discussion and conclusion

$R_s$ values varied massively depending on the method from which these values were extracted. Sabry and Ghitas [11] reported substantial variations in $R_s$ values extracted using seven different methods. This variation was attributed to several factors such as the theoretical model used (e.g. one or two diode models), the assumption of a constant ideality factor with variable temperature and illumination and the infiniteness of $R_{sh}$. Those factors may be the same source for the variation of results presented in this Appendix, for example, $R_{sh}$ was always considered to be infinite in this work.

The variation in $R_s$ values using different methods (reported by Sabry and Ghitas [11]) was (for some models) ~ 2 orders of magnitude for the same $T$ and illumination. Moreover, $R_s$ did not only vary vastly among models but also had: a) negative values, and b) inconsistent behaviour of the variation with both illumination and $T$. These issues were experienced in this work as shown in the results in Section A.3. For example, beside the variation in values as shown in the tables Section A.3, $R_s$ extracted using Method A behaved differently with $T$ compared to values extracted using Method E, see Figure A.3 and Figure A.8 respectively. In addition, Model F gave negative values for $R_s$, see Table A.6. This behaviour (beside the inconsistency of values obtained using Method F) may be attributed to the high scatter in the $dV/dJ$ versus $(J + J_L)^{-1}$ plot obtained using CurVA. Zoppi [12] used Method F to determine $R_s$ and $n$ for CdTe/CdS cells, prior to reusing these values to fit the single diode

equation to real solar cell *J-V* data. This fit was good in both reverse and low forward biases but not at high forward bias. The bad fit was attributed to a) invalidity of the assumption that $J_{sc} = J_L$ at high forward bias, and b) the dependence of the current collection on voltage.

Sabry and Ghitas concluded that there is no accurate model for evaluating $R_s$, which can be concluded from this work as well. However, Model A was chosen to determine $R_s$ for the back contact study in Chapter 7 due to: a) simplicity, and b) consistency of $R_s$ behaviour with $T$ (see Chapter 7 for more details).

## A.5 References for appendix


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# Appendix B: The Shockley Diode Equation

## B.1 Introduction

This appendix is concerned with the derivation of Shockley equation, which describes the relation between current and voltage for the ideal p-n junction i.e. current flow due to diffusion only. Furthermore, the physical meaning of the ideality factor *n* is described with reference to the dominant current transport mechanism operating in the junction.

## B.2 Shockley equation and the ideal p-n junction

The main assumptions for the ideal p-n junction which are embodied in the Shockley equation are [1]:

1- The junction is abrupt.
2- Boltzmann approximation is valid throughout the depletion region.
3- Low injection conditions apply.
4- No generation current presents in the depletion region.
5- Both electron and hole currents are constant through the depletion region.

Since two charge carriers contribute to currents in semiconductors, electrons and holes, the current depends on their concentration in the conduction and valence bands for electrons and holes respectively. These concentrations are determined by considering the position of the Fermi level ($E_F$), which is defined as the energy level above which all energy levels are empty whereas they are filled below it at $T = 0$ K.

If the semiconductor is pure i.e. without impurities and defects, then it is called *intrinsic semiconductor*, in which the Fermi level is called the *intrinsic Fermi level* ($E_{Fi}$), and is located close to the middle of $E_g$. Electron and hole concentrations are both equal to the intrinsic carrier concentration ($n_i$) in this case.

However, in case of doping for example, $E_F$ changes its position and becomes closer to the conduction and the valence band for n-type and p-type materials respectively, as shown in Figure B.1. At thermal equilibrium e.g. without external applied voltage or change in temperature, the equilibrium carrier concentrations for electrons, $n_0$ and holes, $p_0$ are given by

$$n_0 = n_i \exp\left(\frac{E_F - E_{Fi}}{kT}\right) \qquad \text{(B.1)}$$

and

$$p_0 = n_i \exp\left(\frac{E_{Fi} - E_F}{kT}\right) \qquad \text{(B.2)}$$

where $k$ is Boltzmann's constant and $T$ is temperature.

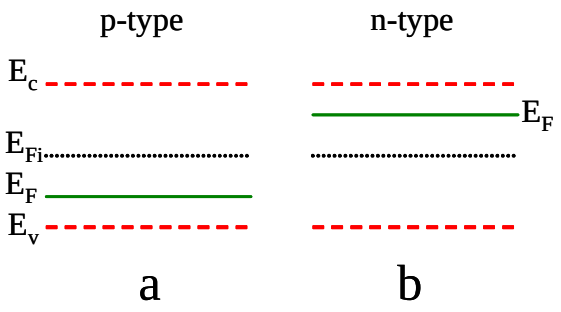


**Figure B.1**: Band diagrams for a) p-type and b) n-type semiconductors. The figure shows the intrinsic Fermi level ($E_{Fi}$), and the change in its position (to $E_F$) within $E_g$ as doping changes.

When a p-n junction is formed, the Fermi level must be aligned across the device as discussed in Section 2.1 i.e. the Fermi level has the same value across the whole device. However, its position may be disturbed if there are excess carriers due to an external voltage or thermal excitation for example. The new position for the Fermi level is called the *quasi Fermi level*, and denoted as $E_{Fn}$ and $E_{Fp}$ for n- and p-sides of the device respectively (Figure B.2). The new carrier concentrations, including the excess carriers are expressed as

$$n_0 + \delta n = n_i \exp\left(\frac{E_F - E_{Fi}}{kT}\right) \qquad \text{(B.3)}$$

and

$$p_0 + \delta p = n_i \exp\left(\frac{E_{Fi} - E_F}{kT}\right) \qquad \text{(B.4)}$$

for the n- and p-sides respectively, where $\delta n$ and $\delta p$ are the excess electron and hole concentrations.

The excess hole concentration (minority carriers) within the n-side of the device is given by [2]

$$\delta p = p_{n0}\left[\exp\left(\frac{qV_{bi}}{kT}\right) - 1\right]\exp\left(\frac{x_n - x}{L_p}\right) \qquad \text{(B.5)}$$

where $V_{bi}$ is the built in potential in the junction, $p_{n0}$ is the equilibrium minority carrier hole concentration, $L_p$ is the hole diffusion length and $x_n$ is the distance between the centre of the depletion region and the end of it in the n-side as seen in Figure B.2.

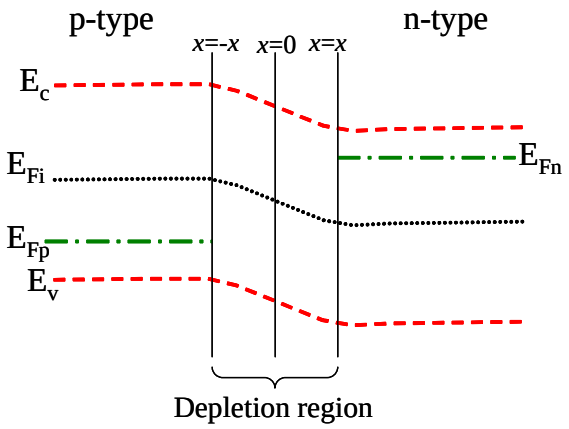


**Figure B.2**: A p-n junction showing the quasi Fermi levels for both n- and p-side, $E_{Fn}$ and $E_{Fp}$ respectively.

The hole diffusion current $J_p$ at $x = x_n$ can be calculated from the equation [2]

$$J_p(x_n) = -qD_p \left. \frac{dp_n(x)}{dx} \right|_{x=x_n} \qquad \text{(B.6)}$$

where $D_p$ is the hole diffusion coefficient, $q$ is the electronic charge and $p_n$ is the minority carrier hole concentration in the n-side of the device. Since doping is assumed to be uniform, $p_0$ is constant. Hence by using equation B.4, equation B.6 can be rewritten as

$$J_p(x_n) = -qD_p \left. \frac{d\delta_n(x)}{dx} \right|_{x=x_n} \qquad \text{(B.7)}$$

By deriving equation B.5 and then substituting in equation B.7,

$$J_p(x_n) = \frac{qD_p p_{n0}}{L_p} \left[ \exp\left( \frac{qV_{bi}}{kT} \right) - 1 \right] \qquad \text{(B.8)}$$

By the same argument for minority carrier electron in the p-side, the electron diffusion current $J_n$ at $x = - x_p$ can be expressed as

$$J_n(-x_p) = \frac{qD_n n_{p0}}{L_n} \left[ \exp\left( \frac{qV_{bi}}{kT} \right) - 1 \right] \qquad \text{(B.9)}$$

where $D_n$ is the electron diffusion coefficient, and $n_{p0}$ is the minority carrier electron concentration.

The total current in the junction (as it is mentioned in the assumptions earlier in this Section) is the sum of both electron and hole minority currents i.e. the total current $J$ is the sum of $J_p$ and $J_n$, therefore it can be written by using equations B.8 and B.9

$$J = J_p(x_n) + J_n(-x_p) = \left[\frac{qD_n n_{p0}}{L_n} + \frac{qD_p p_{n0}}{L_p}\right]\left[\exp\left(\frac{qV_{bi}}{kT}\right) - 1\right] \qquad \text{(B.10)}$$

or

$$J = J_p(x_n) + J_n(-x_p) = J_0\left[\exp\left(\frac{qV_{bi}}{kT}\right) - 1\right] \qquad \text{(B.11)}$$

where

$$J_0 = \frac{qD_n n_{p0}}{L_n} + \frac{qD_p p_{n0}}{L_p} \qquad \text{(B.12)}$$

$J_0$ is called the saturation current. Equation B.11 is the Shockley equation, which is used for the ideal p-n junction.

For a one-sided junction i.e. when $N_A >> N_D$, where $N_A$ and $N_D$ are the doping concentration of p- and n-sides respectively, the first term in the RHS of equation B.12 can be neglected, and [1],

$$J_0 \approx \frac{eD_p p_{n0}}{L_p} \approx T^{(3+C/2)} \exp\left(-\frac{E_g}{kT}\right) \qquad \text{(B.13)}$$

where $C$ is a constant. The term $T^{(3+C/2)}$ is negligible in comparison to the exponential term, leading to that ln $J_0$ is proportional to -1/$T$.

## B.3 Effect of recombination on the Shockley equation

Under forward bias condition for a p-n junction which have localised *traps* in the depletion region, excess carriers (both electrons and holes) are injected in the depletion region, which increases the probability of their capture at traps, and therefore recombination. The recombination rate of the excess carriers $U$ based on Shockley-Read-Hall (SRH) theory is given by [2],

$$U = \frac{np - n_i^2}{\tau_{p0}(n + n') + \tau_{n0}(p + p')} \qquad \text{(B.14)}$$

where $n'$ ($p'$) is the electron (hole) concentration that would be in the conduction (valence) band if the trap energy $E_t$ coincided with $E_F$, $n$ and $p$ are the electron and hole concentrations in the conduction and valence bands respectively and $\tau_{n0}$ and $\tau_{p0}$ are the excess minority carrier electron and hole lifetimes respectively.

The forward applied voltage $V$ can be expressed using $E_{Fn}$ and $E_{Fp}$ as (see Figure B.2) [2],

$$\left(E_{Fn} - E_{Fi}\right) + \left(E_{Fi} - E_{Fp}\right) = qV \qquad \text{(B.15)}$$

The complete recombination process requires that the trap captures an electron and a hole from the conduction and the valence bands respectively. Hence, the location of the trap within $E_g$ affects the recombination probability taking place in it. The maximum recombination rate occurs, therefore, when the traps are located at $E_{Fi}$ (middle of $E_g$) i.e. $E_t = E_{Fi}$, then $n' = p' = n_i$. This rate decays sharply as $E_t$ moves away from $E_{Fi}$. By considering equation B.15, at the centre of the depletion region,

$$E_{Fn} - E_{Fi} = E_{Fi} - E_{Fp} = \frac{qV}{2} \qquad \text{(B.16)}$$

As a result, equations B.1 and B.2 then become

$$n = n_i \exp\left(\frac{qV}{2kT}\right) \qquad \text{(B.17)}$$

and

$$p = n_i \exp\left(\frac{qV}{2kT}\right) \qquad \text{(B.18)}$$

Recalling that $n' = p' = n_i$ and $\tau_{n0} = \tau_{p0} = \tau_0$ for traps at the centre of depletion region, equation B.14 becomes

$$U_{\max} = \frac{n_i}{2\tau_0} \frac{\left[\exp\left(qV/kT\right)-1\right]}{\left[\exp\left(qV/2kT\right)+1\right]} \qquad \text{(B.19)}$$

where $U_{max}$ is the maximum recombination rate. If $V >> kT/q$ then 1 can be neglected from both numerator and denominator, and then

$$U_{\max} = \frac{n_i}{2\tau_0} \exp\left(\frac{qV}{2kT}\right) \qquad \text{(B.20)}$$

The recombination current under forward bias is then calculated from

$$J = \int_0^W qU dx \qquad \text{(B.21)}$$

$$J = J_0 \exp\left(\frac{qV}{2kT}\right) \qquad \text{(B.22)}$$

where

$$J_0 = \frac{qWn_i}{2\tau_0} \qquad \text{(B.23)}$$

and $W$ is the depletion width. Due to the relationship between $n_i$ and $T$ as seen in equations B.1 and B.2, ln $J_0$ may vary linearly with -1/$T$.

Under the reverse bias condition, generation current dominates rather than recombination due to the lack of excess carriers i.e. current is due to carriers which are thermally generated via traps. The reverse generation current has a similar expression to that of $J_0$ in equation B.23 [2], but with a minus sing due to its direction. Therefore the general equation for the current in a p-n junction having the features described above is

$$J = J_0\left[\exp\left(\frac{qV}{2kT}\right)-1\right] \qquad \text{(B.24)}$$

which is similar to equation B.11, describing the diffusion current, except that there is 2 in the denominator of the exponential power for this equation. Hence, current in the p-n junction can be described more generally by

$$J = J_0\left[\exp\left(\frac{qV}{nkT}\right)-1\right] \qquad \text{(B.25)}$$

where *n* is the ideality factor, which is = 1 or 2 if the current is controlled by diffusion or recombination transport mechanisms respectively.

## B.4 References for appendix B

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# Appendix C: *J-V-T* Curves for Samples Investigated in Chapter 6

This Appendix shows the *J-V-T* characteristics of the samples studied in Chapter 6 (i.e. samples 290, 254 and 305). The experimental details of these samples are described in Section 6.2.1. Each Figure in this Appendix shows the *J-V* curves for temperatures in the range of 200 – 300 K at a certain light intensity. Six different light intensities (including dark) were used in Chapter 6, however, only four of them were selected (100 %, 50 % and 20 % of the nominal 1000 $Wm^{-2}$ of the 1.5AM spectrum and in the dark) for demonstration in this Appendix. The procedure of collecting the data is described in Section 6.2.2.

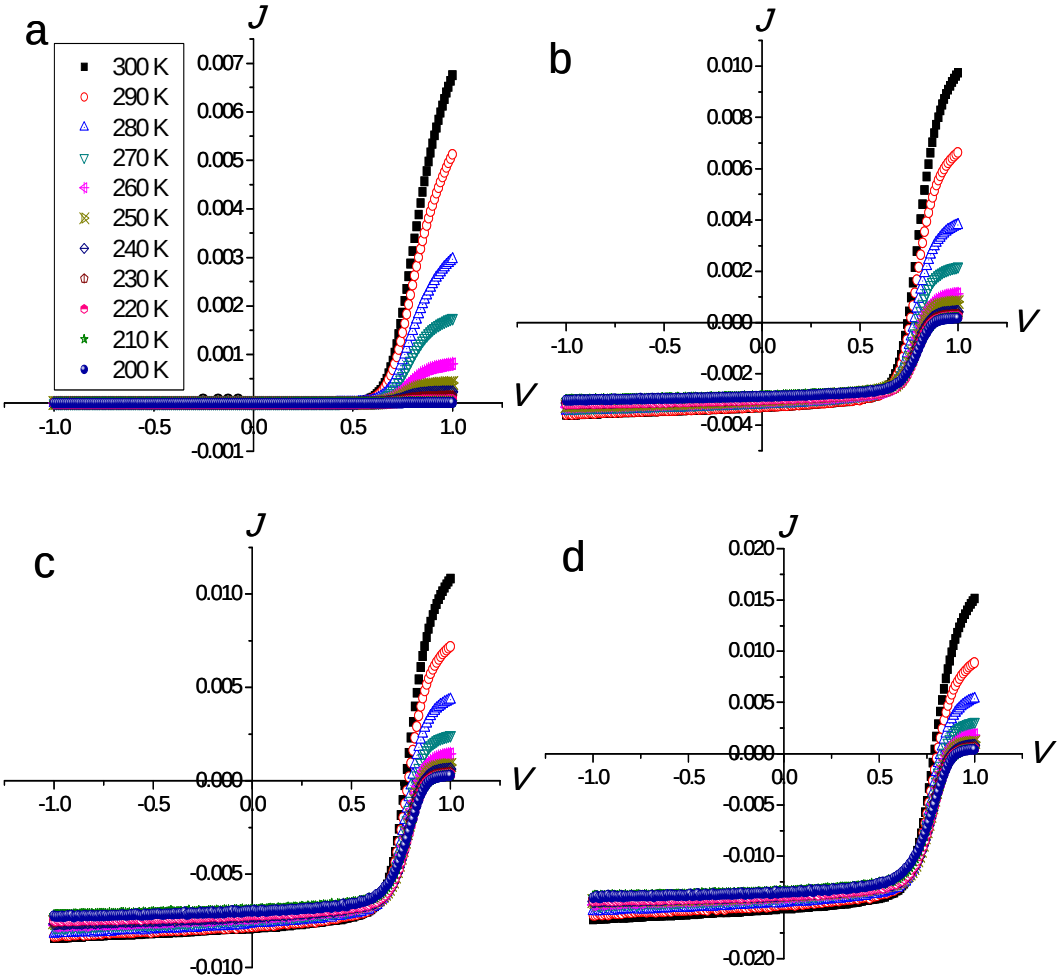


**Figure C.1**: *J-V-T* characteristics for sample 290. Figures a, b, c and d show the curves in the dark and under 20 %, 50 % and 100 % of the nominal 1000 $Wm^{-2}$ of the 1.5AM spectrum respectively.

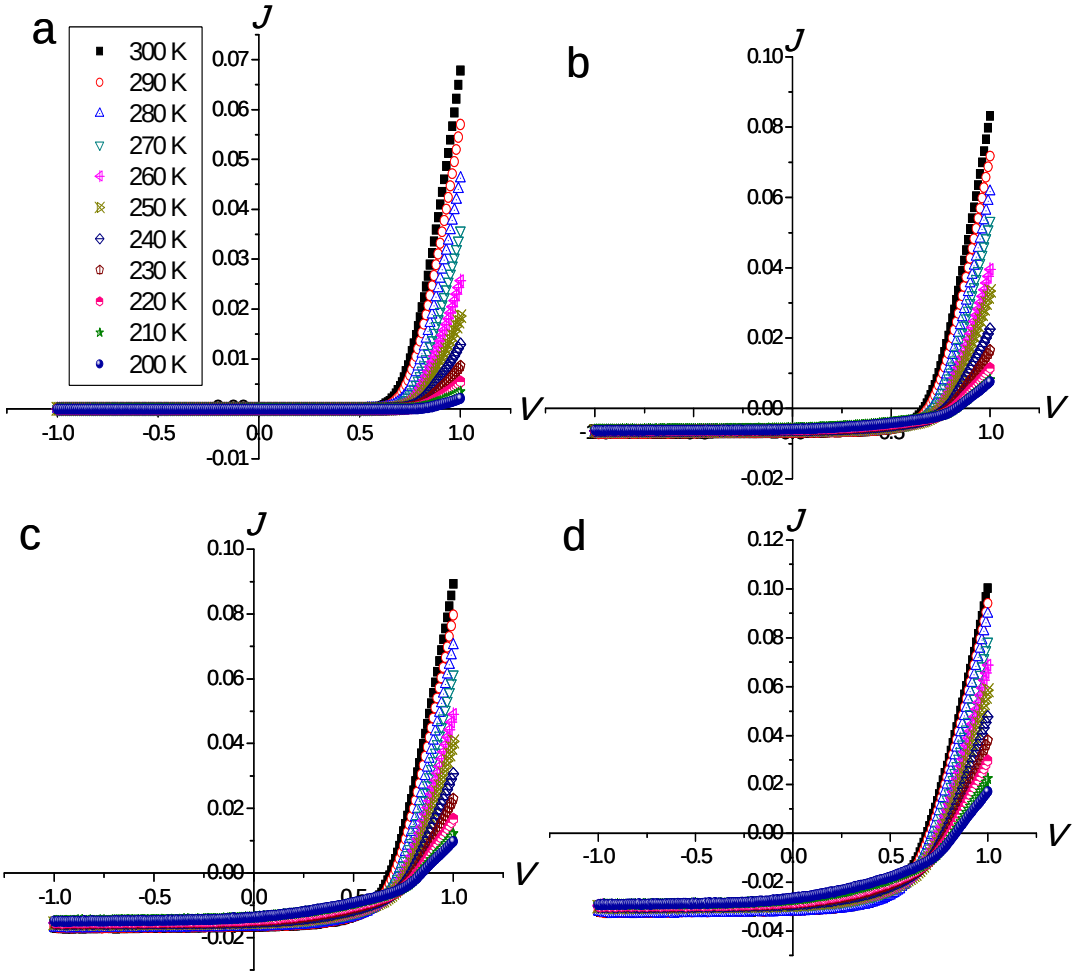


**Figure C.2**: *J-V-T* characteristics for sample 254. Figures a, b, c and d show the curves in the dark and under 20 %, 50 % and 100 % of the nominal 1000 $Wm^{-2}$ of the 1.5AM spectrum respectively.

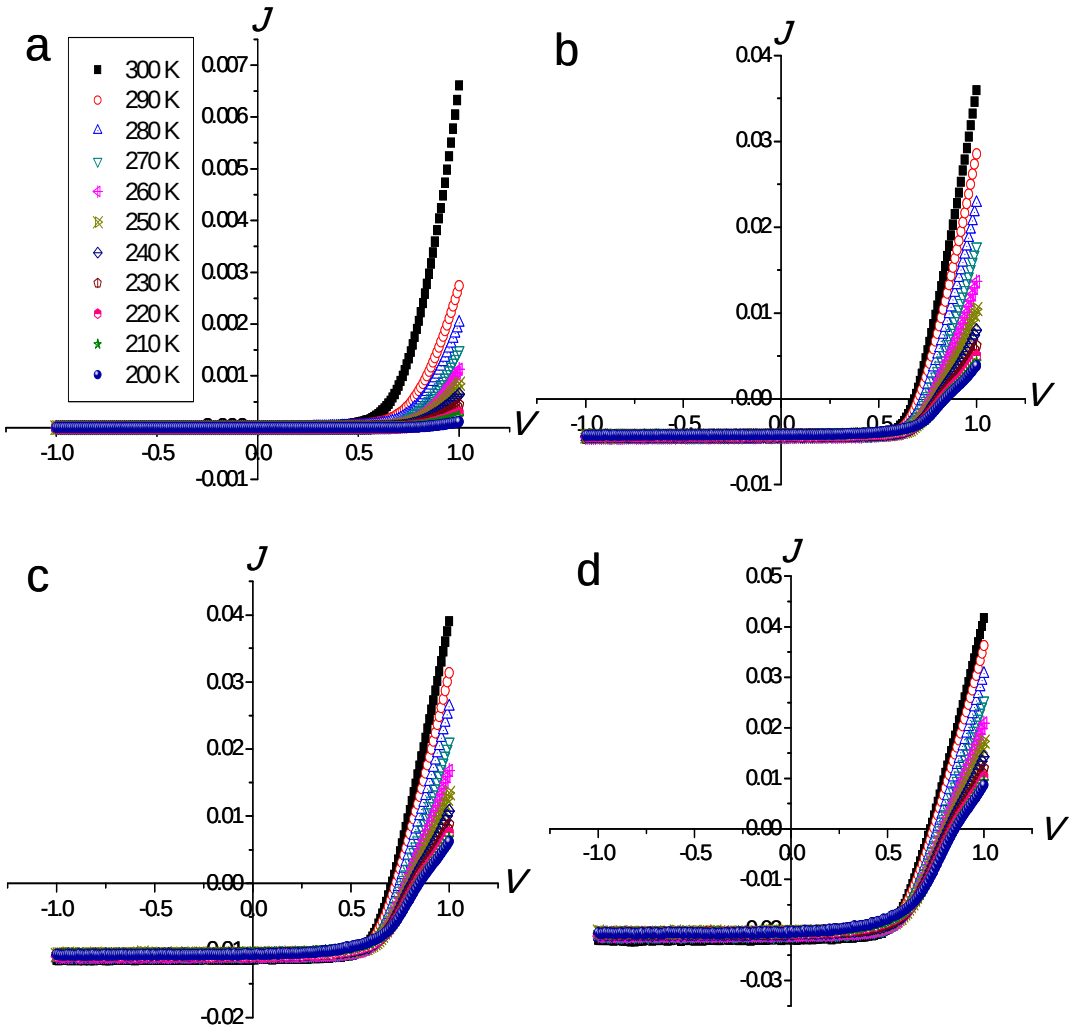


**Figure C.3**: *J-V-T* characteristics for sample 254. Figures a, b, c and d show the curves in the dark and under 20 %, 50 % and 100 % of the nominal 1000 $Wm^{-2}$ of the 1.5AM spectrum respectively.

# Appendix D: List of Publications

M. K. Al Turkestani, J. D. Major, R. E. Treharne, Y. Y. Proskuryakov and K. Durose (2010). Recent research trends in thin film solar cells. 4th Saudi Science Conference, Madina, Saudi Arabia.

Y. Y. Proskuryakov, K. Durose, M. K. Al Turkestani, I. Mora-Sero, G. Garcia-Belmonte, F. Fabregat-Santiago, J. Bisquert, V. Barrioz, D. Lamb, S. J. C. Irvine and E. W. Jones (2009). Impedance spectroscopy of thin-film CdTe/CdS solar cells under varied illumination. Journal of Applied Physics **106**(4) p: 44507-44515.

Y. Y. Proskuryakov, K. Durose, J. D. Major, M. K. Al Turkestani, V. Barrioz, S. J. C. Irvine and E. W. Jones (2009). Doping levels, trap density of states and the performance of co-doped CdTe(As,Cl) photovoltaic devices. Solar Energy Materials and Solar Cells **93**(9) p: 1572-1581.

M. K. Al Turkestani, K. Durose, B. Wakeling, D. Lane, S. J. C. Irvine and V. Barrioz (2009). A rapid screening method for investigating the effect of processing parameters on CdTe/CdS solar cell performance. Material Research Society Symposium Proceeding, San Francisco, CA, USA **1165** p: 191-196

M. K. Al Turkestani, K. D. (2008). A rapid screening study of the influence of interfaces and thickness on CdTe/CdS solar cells. PVSAT-4, Bath University, UK.

M. K. Al Turkestani and Ken Durose (2007). Modifications to the I-V behaviour of In/CdS/ITO interfaces. PVSAT-3, Durham University, UK.