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Electrical performance of III-V gate-all-around nanowire transistors

Pedram Razavi and Giorgos Fagas
Tyndall National Institute, University College Cork, Lee Maltings, Dyke Parade, Cork, Ireland

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The performance of III-V inversion-mode and junctionless nanowire field-effect transistors are investigated using quantum simulations and are compared with those of silicon devices. We show that at ultrascaled dimensions silicon can offer better electrical performance in terms of short-channel effects and drive current than other materials. This is explained simply by suppression of source-drain tunneling due to the higher effective mass, shorter natural length, and the higher density of states in the confined channel. We also confirm that III-V junctionless nanowire transistors are more immune to short-channel effects than conventional inversion-mode III-V nanowire field-effect transistors. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4817997]

Metal-oxide-semiconductor field-effect transistors (MOSFETs) will reach sub-10 nm regime within the next few years.[1] At this length scale, there are fundamental challenges posed to devices due to electrostatic and quantum mechanical tunneling effects.[2,3] III-V compound semiconductor materials are attractive candidates for next generation MOSFETs because their high mobility allows for the increase of drive current over silicon without increasing gate capacitance. Besides their higher mobility,[4,5] III-V semiconductors offer unique possibilities to control the device dimensions, doping, and composition and to achieve bandgap engineering during fabrication.[6,7] However, in devices scaled below 10 nm, the classic transfer characteristics are not necessarily determined by physical parameters such as the mobility[1] and expectations from classical device concepts need to be tested. To this end, we investigate the use of III-V semiconductors in state-of-the-art nanotransistor architectures and compare their electrical performance with Si channels.

We consider gate-all-around (GAA) transistors made of III-V channels. The multiple-gate design has now been adopted by the semiconductor industry as it increases the electrostatic control of the gate over the carriers in the channel, thereby improving short-channel effects in nanotransistors.[8,9] The fabrication process of ultrascaled devices is another challenge. Direct coupling between source and drain contact through tunneling must be avoided[2,10] and extremely high doping concentration gradients are needed to form ultra-sharp p-n junctions at small gate lengths. As an alternative, junctionless nanowire transistors (JNTs) use homogeneous doping in the source, drain, and channel regions.[11,12] Here, we study the short-channel characteristics of III-V GAA nanowire MOSFETs using both JNT and conventional inversion-mode (IM) architecture. Using quantum mechanical simulations, we calculate the transfer characteristics in short-channel devices and extract the subthreshold slope (SS), drain-induced barrier-lowering (DIBL), and drive current (I_{ON}) characteristics. Our comprehensive analysis shows that in ultrascaled nanowire transistors, quantum confinement and source-drain tunneling, both determined by the channel material effective mass, along with the dielectric properties of the channel, counteract the commonly anticipated performance of III-V high mobility materials.

Our technology evaluation tools are based on solving the Schrödinger and Poisson equations self-consistently via the non-equilibrium Green's function approach. The method and implementation have been described elsewhere.[1,13] Different III-V materials such as GaAs, InP, and GaSb have been considered as channel materials of n-type ⟨100⟩-oriented gate-all-around nanowire transistors with square cross-sections. The devices are fabricated on (010)-oriented wafers. Fig. 1 shows a schematic view of GAA junctionless and inversion-mode nanowire transistors as well as the doping profile in the longitudinal direction for both devices. The gate length and cross-section under consideration are 10 nm and 5×5 nm^2, respectively. A uniform doping concentration of 1×10^{20} cm^{-3} is used throughout the channel and source/drain regions in the junctionless devices. In IM transistors, the source and drain junctions are assumed to be abrupt and

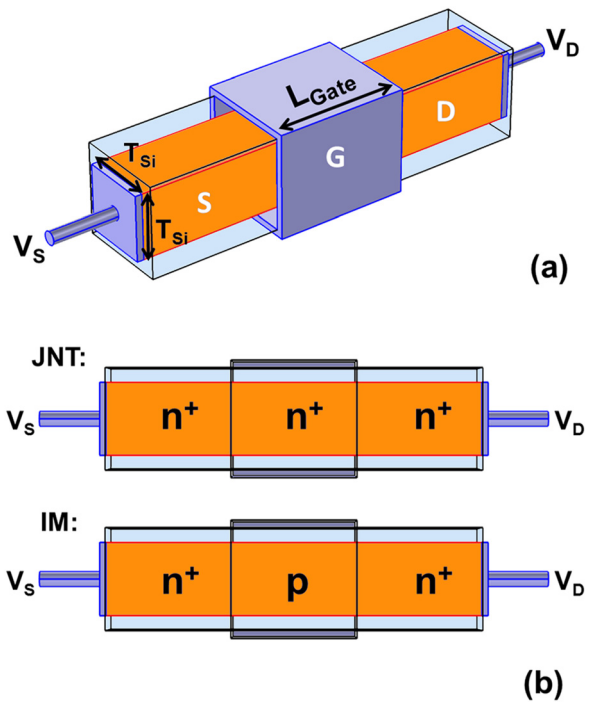

FIG. 1. (a) Bird eye's view of a gate-all-around nanowire MOSFET and (b) doping profile in the longitudinal direction in junctionless nanowire transistors and inversion-mode devices.

TABLE I. Material properties for Si and III-V compound semiconductors where E_g^{Γ} and E_g^{X} are bandgaps, ΔE_L and ΔE_X are the L- and X- valley band-offsets from the Γ-valley, and m_t, m_l, and m_Γ are transverse, longitudinal, and isotropic Γ-valley effective masses, respectively (m_0 is the free electron mass).

	Dielectric constant	$E_g^{\Gamma}(eV)$	$\Delta E_{L\ (eV)}$	$\Delta E_{X\ (eV)}$	m_{Γ}/m_0	$m_t/m_0, m_l/m_0\ (L)$	$m_t/m_0, m_l/m_0\ (X)$
InP	*12.4*	*1.353*	*0.59*	*0.85*	*0.08*	*0.13, 1.64*	*0.34, 1.26*
GaAs	*12.9*	*1.422*	*0.29*	*0.48*	*0.067*	*0.075, 1.9*	*0.27, 1.98*
GaSb	*15*	*0.727*	*0.063*	*0.329*	*0.039*	*0.1, 1.3*	*0.22, 1.51*
		Dielectric constant		$E_g^{X}(eV)$	ΔE_L (eV)	$m_t/m_0, m_l/m_0\ (X)$	$m_t/m_0, m_l/m_0\ (L)$
Si		11.7		1.12	0.88	0.19, 0.98	0.12, 1.7

doping concentrations in the source/drain regions are $1 \times 10^{20}\,\mathrm{cm}^{-3}$, while the channel region itself is undoped. The effective oxide thickness (EOT) is equal to 1 nm for all devices. We consider smooth surfaces neglecting the effect of interface roughness in short channels. Although interface roughness is a significant factor that typically limits the mobility, for the device dimensions considered here scattering at the channel-oxide interface is expected to have a small effect on suppressing the drive current.[14,15] The supply voltage is equal to 0.65 V and all transistors are designed to have the same off-current of 100 nA/μm by tuning the gate work-function, which is suitable for high performance logic technologies. Band-to-band tunneling (BTBT) has not been considered in the simulations. It is worth noting that, because of the strong quantization effect, the band gap in the simulated nanowires becomes even larger than bulk devices as the channel thickness becomes smaller and, as a result, BTBT is considerably decreased.[16]

The material properties used in the simulations are listed in Table I.[17,18] In ultra-scaled devices, maintaining good sub-threshold characteristics and low DIBL are very important.[19] Therefore, we use the SS and DIBL as performance indicators in our simulations. SS shows the rate of current increase with gate voltage below threshold and represents the efficiency of the gate control over the channel potential. The variation of threshold voltage with drain voltage is expressed by DIBL.

Output characteristics of both conventional (N^+-P-N^+) and junctionless (N^+-N^+-N^+) devices were simulated. In Fig. 2, I_{ds}-V_{gs} characteristics of Si and GaAs GAA nanowire channels are simulated with and without electron-phonon interactions. Optical and acoustic phonon scattering in Si and acoustic and polar optical scattering have been considered in GaAs. Evidently electron-phonon (e-ph) interaction does not considerably affect the current characteristics of the ultrascaled devices with 10 nm gate length. Similar results are obtained for the other III-V materials, and therefore, e-ph scattering has not been considered in further simulations.

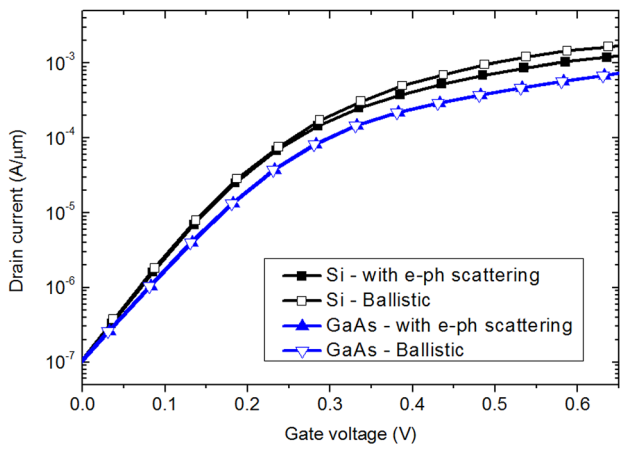

FIG. 2. Transfer characteristics of Si and GaAs channels ($L_{gate} = 10$ nm).

The subthreshold swing, DIBL, and drive current of InP, GaAs, GaSb devices compared to the Si nanowire device are shown in Fig. 3. Focusing on Figs. 3(a) and 3(b), JNTs and IM devices with Si channels exhibit smaller SS and DIBL, i.e., they are more immune to short-channel effects. This can be explained by the value of transport effective mass and the natural length concept. The latter quantifies the extension of electric fields from the source and drain sides of the device into the channel. To suppress the short channel effects, a larger ratio of effective gate length to the natural length is required. The natural length for GAA nanowire transistors with square cross-section is $\lambda = \sqrt{t_{ox}t_{semicon}\varepsilon_{semicon}/(4\varepsilon_{ox})}$.[20] Here, $\varepsilon_{semicon}$ is the permittivity of the channel material, ε_{ox} is the permittivity of the gate oxide, t_{ox} is the gate oxide thickness, and $t_{semicon}$ is the nanowire thickness. Fig. 4 shows the natural lengths of Si and other III-V compound materials for the simulated nanowire device. The reduced SS and DIBL for the 10 nm gate length Si devices are to be anticipated by the smallest value of the natural length. We note the dependence of the natural length on ε_{ox}. Alternative gate stacks can be used to tune this parameter, including high-k dielectrics or organic molecular coatings.[21–23] For example, nanowire transistors with molecular gating have been proposed as low power chemical sensors.[24]

Among the III-V compound semiconductor nanowire devices simulated here, InP has the smallest subthreshold swing. This is due to the larger effective mass of InP along the current direction which suppresses the source-to-drain tunneling current. On the contrary, GaSb has the smallest transport effective mass and thus shows the worst subthreshold swing. Nevertheless, the contribution of L-valleys to transport at higher gate voltages in GaSb is the reason for its higher on-current in comparison to the other simulated III-V nanowires as seen in Fig. 3(c). Our study also confirms that JNTs are more immune to short-channel effects than conventional IM devices and present smaller subthreshold swing and DIBL. This is traced back to the larger effective gate length that decreases source-to-drain tunneling.[1]

Furthermore, it is found that at this scale devices made of silicon nanowire channels have better drive current (Fig. 3(c)) and on-to-off current ratio (not shown) compared to III-V GAA devices. This is not only due to the better subthreshold swing of the silicon devices but also due to the fact

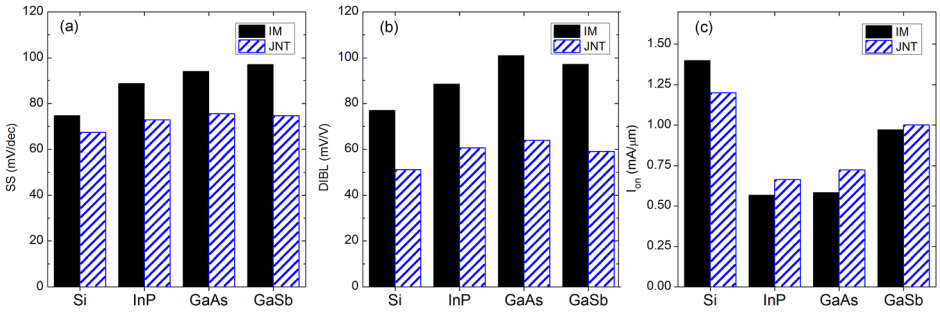

FIG. 3. Subthreshold swing, DIBL, and drive current of GAA nanowire transistors made of Si and III-V compound semiconductors (I_{on} extracted at $V_{GS} = 0.65$ V and DIBL is defined as $V_{th}(V_{DS} = 0.05\ V)$-$V_{th}(V_{DS} = 0.65\ V)$/(0.65–0.05)).

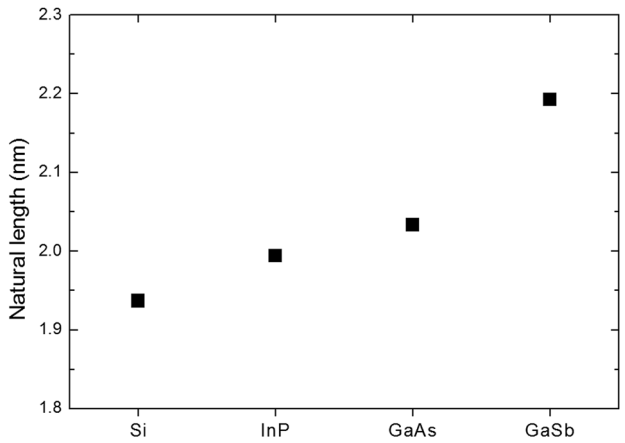

FIG. 4. Natural length of Si and other III-V compound materials for the simulated nanowire device.

that III-V materials have a low density of states (DoS) in the Γ-valley, which results in the reduction of the drive current.[25] Similar to the subthreshold swing the off current of the III-V nanowire channels is largely affected by source-drain tunneling compared to the silicon nanowire device due to their smaller effective mass along the transport direction.

To summarize, we showed that ultrascaled gate-all-around junctionless and inversion mode silicon transistors have better subthreshold swing and less short-channel effects than III-V nanowire devices. This electrical performance is explained simply by suppression of source-drain tunneling due to the higher effective mass and the shorter natural length for Si. Higher on-current is also observed for the Si device as the mobility concept does not apply at this length scale and the drive current is largely determined by the density of states in the confined channel. These considerations are important to take into account when designing transistors at the nanoscale.

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[1]P. Razavi, G. Fagas, I. Ferain, R. Yu, S. Das, and J.-P. Colinge, J. Appl. Phys. **111**(12), 124509 (2012).
[2]L. Ansari, B. Feldman, G. Fagas, J.-P. Colinge, and J. C. Greer, Appl. Phys. Lett. **97**(6), 062105 (2010).
[3]I. Ferain, C. A. Colinge, and J.-P. Colinge, Nature (London) **479**(7373), 310 (2011).
[4]J. A. del Alamo, Nature (London) **479**(7373), 317 (2011).
[5]M. Bescond, N. Cavassilas, K. Kalna, K. Nehari, L. Raymond, J. L. Autran, M. Lannoo, and A. Asenov, in *IEEE International Electron Devices Meeting (IEDM Technical Digest), Washington, DC, 5 December 2005*, pp. 526–529.
[6]M. Abul Khayer and K. Lake Roger, *Modeling and Performance Analysis of III-V Nanowire Field-Effect Transistors*, edited by N. Lupu (InTechOpen, 2010).
[7]K. Tomioka, M. Yoshimura, and T. Fukui, Nature (London) **488**(7410), 189 (2012).
[8]J.-P. Colinge, Microelectron. Eng. **84**(9–10), 2071 (2007).
[9]N. Singh, A. Agarwal, L. K. Bera, T. Y. Liow, R. Yang, S. C. Rustagi, C. H. Tung, R. Kumar, G. Q. Lo, N. Balasubramanian, and D. L. Kwong, IEEE Electron Device Lett. **27**(5), 383 (2006).
[10]D. Sharma, L. Ansari, B. Feldman, M. Iakovidis, J. C. Greer, and G. Fagas, J. Appl. Phys. **113**(20), 203708 (2013).
[11]J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A.-M. Kelleher, B. McCarthy, and R. Murphy, Nat. Nanotechnol. **5**(3), 225 (2010).
[12]C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J.-P. Colinge, Appl. Phys. Lett. **94**(5), 053511 (2009).
[13]P. Razavi, G. Fagas, I. Ferain, R. Yu, and S. Das, in *Proceedings of the European Solid-State Device Research Conference (ESSDERC), Bordeaux, France, 17–21 September 2012*, pp. 326–329.
[14]K. SungGeun, M. Luisier, A. Paul, T. B. Boykin, and G. Klimeck, IEEE Trans. Electron Device **58**(5), 1371 (2011).
[15]G. Fagas and J. C. Greer, Nano Lett. **9**(5), 1856 (2009).
[16]D. Kim, T. Krishnamohan, Y. Nishi, and K. C. Saraswat, in *International Conference on the Simulation of Semiconductor Processes and Devices, Monterey, California, 6–8 September 2006*, pp. 389–392.
[17]M. Lundstrom, *Fundamentals of Carrier Transport*, 2nd ed. (Cambridge Univ. Press, Cambridge, 2000).
[18]I. Vurgaftman, J. R. Meyer, and L. R. Ram-Mohan, J. Appl. Phys. **89**(11), 5815 (2001).
[19]T. Skotnicki and F. Boeuf, in *Symposium on the VLSI Technology (VLSIT), Honolulu, Hawaii, 15–17 June 2010*, pp. 153–154.
[20]J.-P. Colinge, Solid-State Electron. **48**(6), 897 (2004).
[21]Y. Paska, T. Stelzner, O. Assad, U. Tisch, S. Christiansen, and H. Haick, ACS Nano **6**(1), 335 (2012).
[22]B. Wang and H. Haick, ACS Appl. Mater. Interfaces **5**(6), 2289 (2013).
[23]B. Wang and H. Haick, ACS Appl. Mater. Interfaces **5**(12), 5748 (2013).
[24]E. Buitrago, G. Fagas, M. F.-B. Badia, Y. M. Georgiev, M. Berthomé, and A. Mihai Ionescu, Sens. Actuators B **183**(0), 1 (2013).
[25]A. Pethe, T. Krishnamohan, K. Donghyun, O. Saeroonter, H. S. P. Wong, Y. Nishi, and K. C. Saraswat, in *IEEE International Electron Devices Meeting (IEDM Technical Digest), Washington, DC, 5 December 2005*, pp. 605–608.