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Gate-Controlled Heat Generation in ZnO Nanowires FETs †

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Nanoscale heating production using nanowires has been shown particularly attractive for a number of applications including nanostructure growth, localized doping, transparent heaters and sensing. However, all proof-of-concept devices proposed so far relied on use of highly conductive nanomaterials, typically metals or highly doped semiconductors. In this article we demonstrate a novel nanoheater architecture based on single semiconductor nanowire field-effect transistor (NW-FET). Nominally undoped ZnO nanowires were incorporated into three-terminal devices whereby control of the nanowire temperature at a given source-drain bias was achieved by additional charge carriers capacitatively induced via the third gate electrode. Joule-heating selective ablation of poly(methyl methacrylate) deposited on ZnO nanowires was shown, demonstrating the ability of the proposed NW-FET configuration to enhance by more than one order of magnitude the temperature of a ZnO nanowire, compared to traditional two-terminal configurations. These findings demonstrate the potential of field-effect architectures to improve Joule heating power in nanowires, thus vastly expanding the range of suitable materials and applications for nanowire-based nanoheaters.

1 Introduction

The ability to generate localized heating at micro-nano scale is a current technological challenge holding tremendous potential towards the realization of multifunctional platforms for the investigation of biological and chemical processes as well as growth, doping and chemical functionalization of semiconductor nanostructures. Nanowires and nanobelts have been so far structures of choice for nanoheater devices due to their reduced dimensionality and the possibility to force high current densities within the one-dimensional channel, therefore giving rise to large temperature gradients. In addition, the availability of well-developed bottom-up and top-down growth techniques, as well as the existence of established fabrication methods for nanowire-based devices, allowed to explore a variety of materials and electrically addressable configurations, including singles and arrays of nanowires for multiplexing control of chemical processes.[1–4]

For instance, in biological applications nanowire array microheaters were used for manipulation of proteins,[5] cell lysis[6] and protein synthesis[7]. In material chemistry, nano-heater arrays of higly-doped Si and metal nanowires were used as platforms to grow oxide nanowires at precise locations,[8–10] to selectively coat nanowires with metal nanoparticles[11] and to fabricate arrays of heterogeneous nanostructures.[12] Park *et al.* demonstrated selective functionalization of Si nanowires on silicon-on-insulator (SIO) substrates *via* Joule heating ablation of a protective polymer (polytetrafluoethylene, PTFE) layer prior surface functionalization with chemical linker molecules.[13] Cross-linking of PS-b-PSN3 azide-terminated polystyrene was also demonstrated with a Cr nanowire platform, which provided local and ultrafast temperature modulation in nanoscale space (2.2 K/nm temperature gradient and heating/cooling time $< 2\ \mu s$).[14] Moreover, Ag nanowires networks, interconnected *in situ via* Joule heating process, were also recently proposed as promising candidate for transparent electrodes and transparent film heaters.[15–18] While a consistent effort has been devoted to the exploration of a broad range of applications for nano-heater devices, much less attention has been dedicated to the development of novel device designs able to improve heating efficiency and to address outstanding material limitation, requiring the use of highly conductive materials. In fact, so far only few materials, mainly metal (Cr, Ag) or heavily

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‡ Additional footnotes to the title and authors can be included *e.g.* 'Present address:' or 'These authors contributed equally to this work' as above using the symbols: ‡, §, and ¶. Please place the appropriate symbol next to the author's name and include a `\footnotetext` entry in the the correct place in the list.

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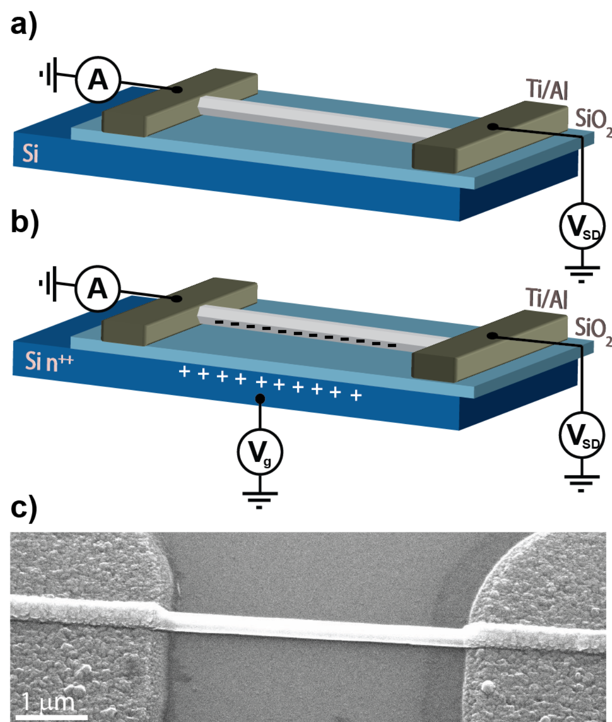

Fig. 1 Schematic representation of a) two-terminal nanowire-based heater device and b) three-terminal NW-FET heater device. c) Representative SEM image of a fabricated ZnO NW-FET with Ti/Al (10 nm/90 nm) pads separated by 5 μm.

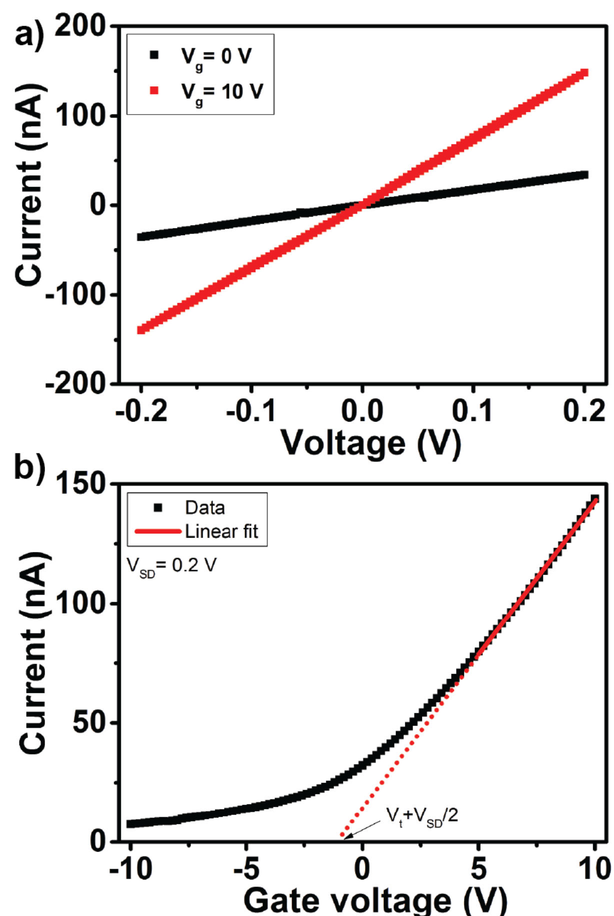

Fig. 2 Electrical characterization of a representative device in air including a) I-V characteristic of the NW-FET with applied back-gate voltage of 0 and 10V and b) I-V_g characteristic with V_{SD}=0.2V. The red line is the linear fit used to calculate the transconductance.

doped semiconductor (p-doped Si) nanowires, were implemented in Joule heating nanodevices. In this work an alternative route to overcome the above restrictions was explored based on the use of a three-terminal field-effect transistor (FET) architecture. The Joule heating process occurring in ZnO nanowire FETs (NW-FET) was investigated demonstrating the ability of the three-terminal device to enhance the heating power of the ZnO nanowire by more than one order of magnitude compared to the heating power generated in the traditional two-terminal configuration. The effective control of the nanowire temperature reachable at a given source-drain bias was ascribed to the additional charge carriers capacitatively induced via a third gate electrode. Selective ablation of poly(methyl methacrylate) (PMMA) spin coated on the NW-FET device was achieved, thus demonstrating the abilities of lightly doped materials ($n \sim 10^{17}$cm^{-3}), such as as-grown ZnO nanowires, to be successfully used as nanoheaters. The observed performance was supported by finite-element method (FEM) simulations, predicting maximum temperatures above 300 °C in the middle of the nanowire, enough to promote selective ablation of PMMA (complete degradation in thermogravmetric analysis is around 300-400 °C).[19] This novel nano-heater design can be conveniently used to enhance the heating power in semiconductor nanowire-based devices and, most importantly, can sensibly expand the range of materials suitable for Joule-heating applications.

2 Results and discussion

Figure 1a-b compare a traditional two-terminal architecture and the proposed three-terminal architectures for nanowire heater devices. In the two-terminal configuration, depicted in figure 1a, the source-drain current uniquely regulated the nanowire temperature during Joule heating process. Under steady-state conditions unavoidable heat flow, constantly dissipated through the metal contacts and the substrate both at room temperature,[20] enforces a temperature gradient to occur along the nanowire, with the highest temperature reached in the middle (for a case whereby metal-nanowire contacts displayed negligible resistance compared to the nanowire channel). In this configuration, since the Joule heating power increases quadratically with the current, the channel resistivity needs to be low enough so that a modest voltage applied (typically below 50 V) can increase the nanowire temperature to the desired value. From the heat diffusion equation, it can be shown that the maximum temperature variation along the nanowire $T_{max} - T_0$, where T_0 is the nanowire temperature at the metal contacts, is

$$T_{max} - T_0 \sim \frac{V^2}{\rho} \quad (1)$$

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with ρ being the nanowire resistivity. Small channel resistivities of the order of $10^{-4}\Omega\cdot$m or lower, found in heavily doped semiconductors and metal nanowires, are often used to reach temperature larger than 300 °C. On the other hand, materials with resistivities in the range of 10^{-1}-10^{-2} $\Omega\cdot$m, such as undoped or lightly doped nanowires, are not suitable for this application, as more than 10 times higher voltages are required to reach comparable temperature ranges. Nevertheless, the additional nanowire-gate capacitance C in the three-terminal NW-FET configuration (figure 1b) can be used to increase the channel conductivity by applycation of an appropriate gate voltage V_g, resulting in a variation in resistivity $\Delta\rho$ of (approximation valid in the linear regime with $V_{SD} \ll V_g$)

$$\Delta\rho \sim \frac{1}{C\Delta V_g} \tag{2}$$

and eventually reaching the required resistivity.

Nanowire field-effect transistors were fabricated by mechanical dispersion of ZnO nanowires on a clean Si(n^{++})/SiO_2 (300 nm) substrate and deposition of source/drain ohmic metal contacts by standard optical lithography and evaporation of Ti/Al 10 nm/90 nm. The nanowire channel was $\sim$5 μm in length, the nanowire diameters were in the range 300-500 nm and the substrate was used as gate electrode. Figure 1c shows an SEM image of a typical device with a single ZnO nanowires contacted with Ti/Al pads.(figure 1c).

A prototypical ZnO NW-FET device (Figure 2a) showed linear I-V characteristics under different back-gate biases applied, indicating an Ohmic behaviour with a resistivity of $7.7\cdot10^{-2}$ $\Omega\cdot$m. The measured resistance of 5.76 ± 0.07 10^6 Ω with the back-gate grounded (V_g=0 V) decreased by a factor 4 to 1.39 ± 0.02 10^6 Ω upon application of 10 V to the back-gate. Figure 2b shows the effect of the gate voltage on the source-drain current (V_{SD}=0.2 V), indicating an evident n-type conduction in the ZnO nanowires. Al pads, with a lower workfunction (4.33 eV) compared to ZnO (4.65 eV),[21] were specifically selected to minimize the contact resistance between the nanowire and the metal. In fact, from the I-V_g curve of the device the contact resistivity was estimated to be in the range $10^{-11} - 10^{-10}$ $\Omega\cdot m^2$ (see SI), in reasonable agreement with the reported value in literature for ZnO-Al contacts.[22] This contact resistivity led to a total contact resistance of $R_c \sim 10^3$ Ω, more than 2 orders of magnitude lower than the nanowire resistance. The threshold voltage V_t was calculated by direct extrapolation as showed in figure 2b, where the value on the V_g axes is the quantity $V_t + \frac{V_{SD}}{2}$.[23] For the measured device V_t=-1.07±0.02 V was obtained, confirming the presence of unintentional n-type doping.[24] Using V_t and the transconductance (dI_{SD}/dV_g=1.27±0.01 10^{-8} S) calculated in the linear region (for V_g > 5 V), it was possible to obtain a field-effect electron mobility of 50 cm^2/V·s, in agreement with previous reports,[25] and a carrier concentration of $\sim10^{17}$ cm^{-3}.

The conductivity of ZnO nanowires measured in air was found strongly affected by the adsorption of oxygen species trapping free electrons at the ZnO surface and increasing the resistivity.[26–30] For comparison, the electrical properties of a ZnO NW-FET covered by a PMMA layer, thus not exposed to air, are shown in figure 3a-b. The I-V curve (figure 3a) at V_g=0 V indicated a resistance of 7.187±0.001 10^5 Ω, nearly one order of magnitude less that the resistance measured in air. It should be noticed that this variation in the nanowire resistance was found consistent with the variation observed in nanowires measured in air and in vacuum (see SI), thus excluding the presence of alternative processes such as unintentional doping of the ZnO nanowire by the polymer or parallel electrical conductivity of the PMMA layer (the resistance of an empty electrode gap with PMMA is on the order of GΩ). Accordingly, from the I-V_g curve characteristic (figure 3b), the transconductance increased to 1.962±0.006 10^{-8} S and the V_t shifted sensibly to a larger negative voltage (-13.8±0.06 V). Using these values, a resistance of $3\cdot10^5$ Ω with V_g=20 V applied (we assumed V_{SD}=0.2 V) was expected to be reached. The overall improvement in conductivity obtained by gating the nanowire (estimated to be a factor $\sim$20 at V_g=20 V) should also lead to a temperature enhancement by a similar factor, according to eq.1.

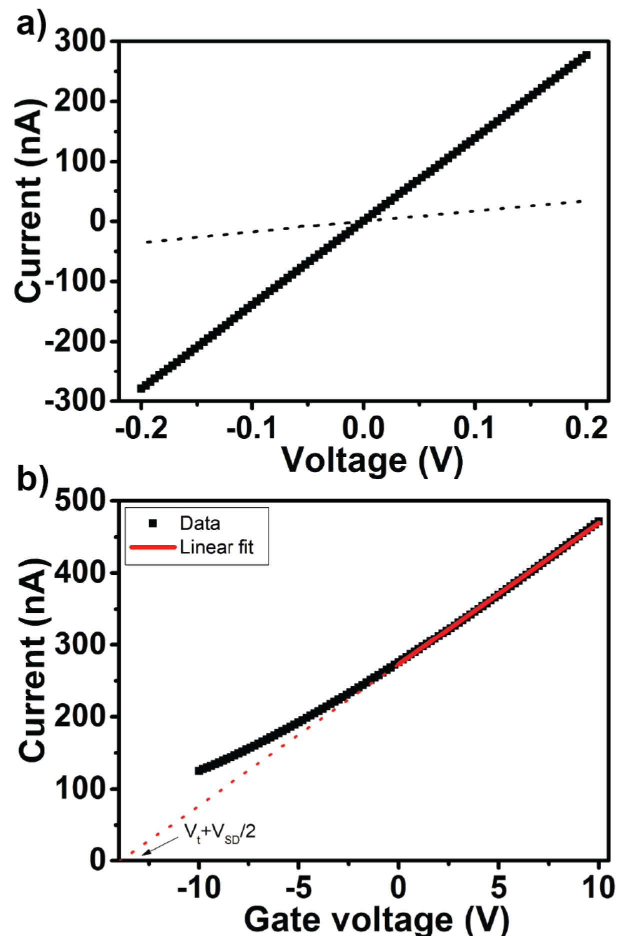

Fig. 3 a) I-V characteristic of the NW-FET covered by PMMA compared to the I-V without PMMA (dotted line) of figure 2a and b) I-V_g characteristic of the device with PMMA.

In order to quantify the enhancement in Joule heating performance provided by the NW-FET compared to the traditional two-terminal configuration, figure 4a-b show the temperature profile in a nanowire with similar electrical properties and gate voltages between 0 and 40 V simulated by a finite element method

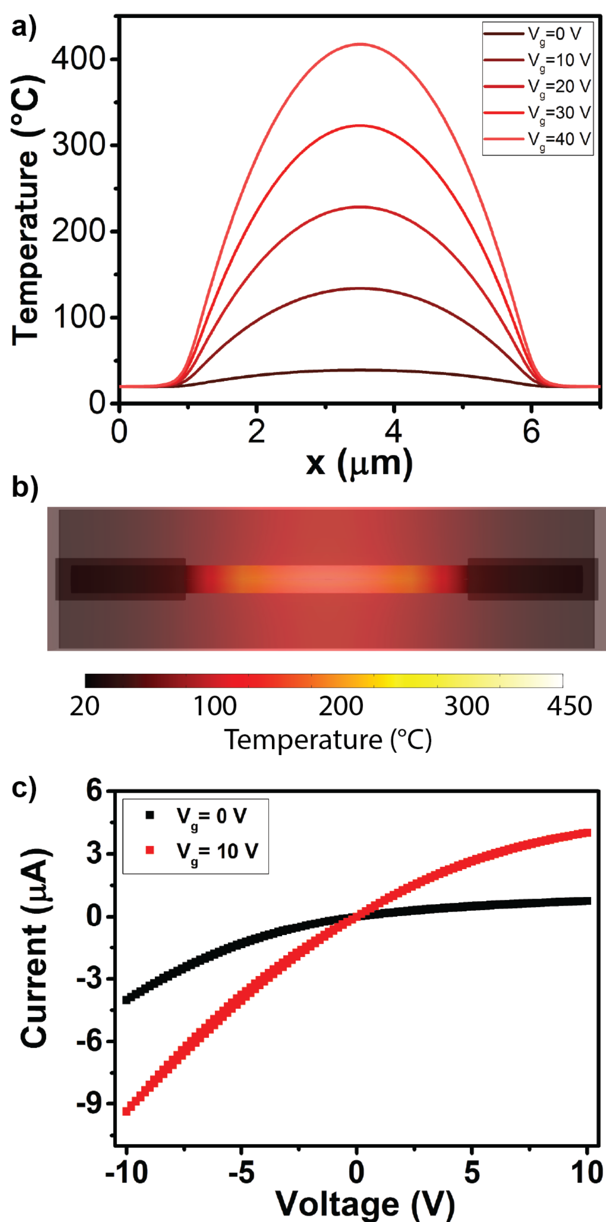

Fig. 4 Finite-element method simulation of a cylindrical nanowire with a radius of 245 nm and two rectangular electrodes separated by a 5 μm gap placed on 300 nm of SiO_2 substrate covered by PMMA. The nanowire resistivity was assumed to be $7.7{\cdot}10^{-2}$ Ω·m, the contact resistance between the metal and the nanowire 10^{-11}Ω·m^2, the heat capacities C_p and the thermal conductivites k for ZnO and SiO_2 were 40.3, 703 J/kg·K and 110 and 1.38 W/m·K, respectively. a) Temperature profile in the center of a nanowire for different V_g values and 40 V applied between source and drain. b) Temperature distribution generated around the nanowire with V_g=40 V (top view).c)I-V at large V_{SD} of the NW-FET without PMMA with V_g=0 V and V_g=0 V.

software (COMSOL Multiphysics 5.0). According to the simulation results, the temperature reached the maximum in the center of the nanowire (figure 4a), as expected in the case of negligible contact resistance. Most importantly, the figure shows that in absence of an applied gate voltage the resistivity of the ZnO nanowire (V_g=0 V) would allow to reach only ∼20 degrees more than room temperature. On the other hand, for a back-gate voltage of 40 V applied, the maximum temperature predicted along the nanowire was 418 °C, more than one order of magnitude larger than the value achievable in absence of applied back-gate. Such encouraging simulation results validated the use of the proposed NW-FET architecture to improve the Joule heating capabilities of semiconductor nanowires.

In agreement with these predictions, PMMA ablation was expected to take place in NW-FETs when few tens of Volts were applied to both the gate and the source-drain. Under these conditions an unavoidable capacitative coupling between the electrodes and the substrate functioning as back-gate (as depicted in figure 1b) should take place. Specifically, an asymmetric behaviour between positive and negative bias applied to the source-drain electrodes could result from the interaction with the back-gate. Figure 3c shows the I-V curve for a high source-drain bias of ±10 V with the back-gate at V_g=0 V (black curve) and at V_g=10 V (red curve) for a device without PMMA. Both curves showed sign of saturation at V_g=10 V whereas at V_g=-10 V the source-drain current was more than double and no saturation was observed. This behaviour was ascribed to additional charges induced on the back-gate due to the coupling with the biased source electrode (drain electrode was grounded during the measurements). In fact, since positive V_g are required to increase the nanowire conductivity, large positive source bias screened the effect of the back-gate thus lowering the current. On the other hand, negative source voltages added positive induced-charges on the back-gate and contributed to enhance the effect on the nanowire channel.

Under these optimized conditions, Joule heating experiments were performed on several NW-FET devices covered with a PMMA layer of ∼200 nm, in order to demonstrate the capabilities of the system to reach temperatures of the order of 300-400 °C required to ablate the polymer.[12]

Experiments conducted with V_g=0 (V_{DS} up to 40 V) were not successful in producing any PMMA ablation (data not shown). On the other hand, figure 5a-d reports the entire set of measurements for a representative NW-FET device before and after the Joule heating process. From the measured I-V and I-V_g characteristics of the device covered by PMMA, a resistance of 1.8368±0.0003 10^5 Ω, a transconductance dI_{SD}/dV_g= 4.522±0.005 10^{-8} S and a threshold voltage V_t=-24.02±0.03 V were obtained. Using the nanowire radius r=254 nm and length L=5.96 μm an electron mobility of μ= 88 $cm^2/V \cdot s$ and a nanowire resistivity at V_g=20 V of $4.52{\cdot}10^{-3}$Ω·m were calculated. Following initial electrical characterization, three sweeps from 0 up to -40 V applied to the source-drain electrodes with a constant back-gate voltage of 20 V were performed, as shown in figure 5b. The first sweep (black curve) from 0 to -30 V was not effective in producing any relevant change. However, a clear jump in resistivity was observed between the second and the third sweep with the extended range

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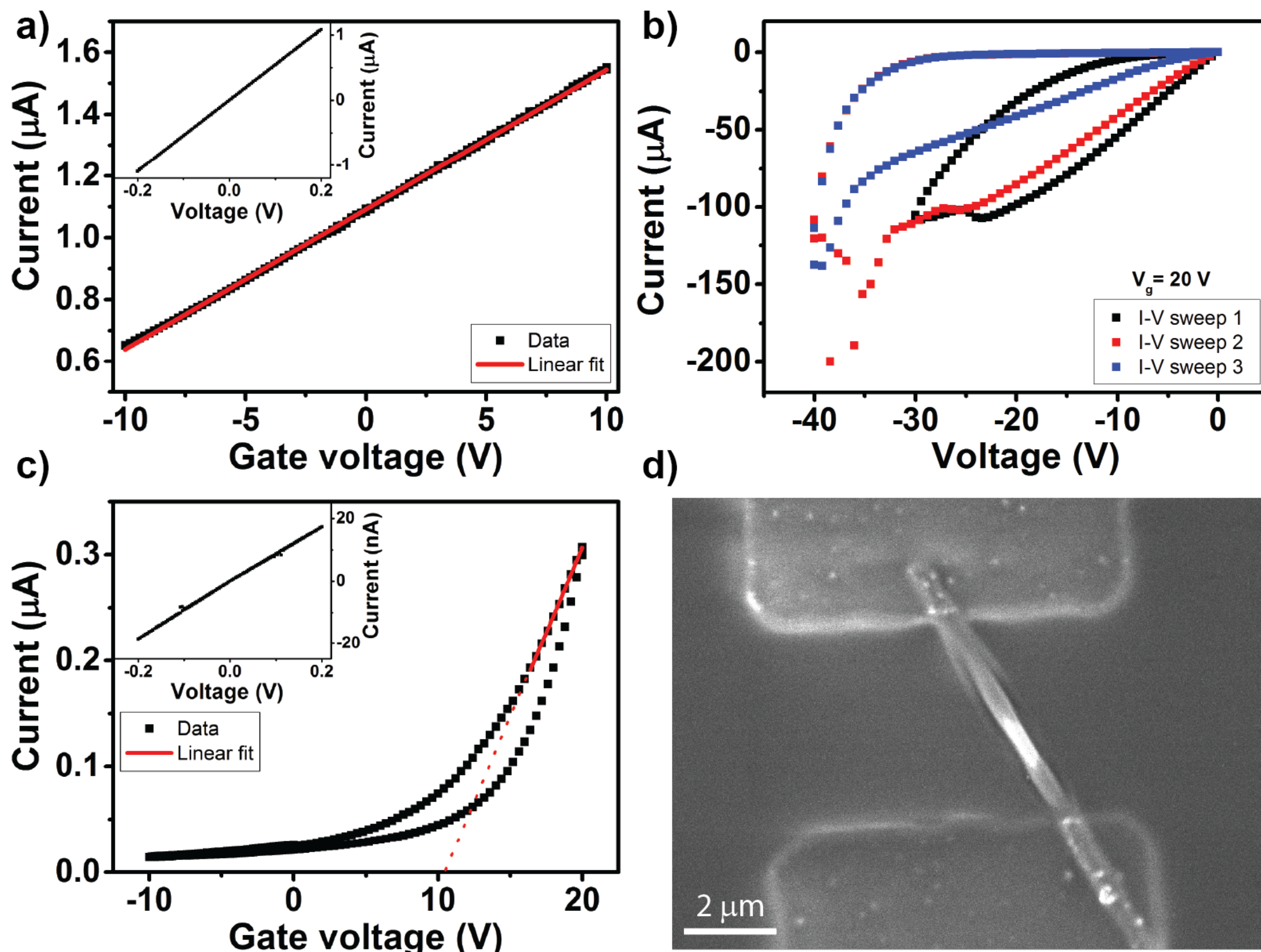

Fig. 5 Ablation of PMMA layer by Joule heating in ZnO nanowire FET device a) I-V and I-V_g characteristics of a representative device before ablation. b) I-V sweeps from 0 V to -40 V with V_g=20 V were performed to force a current through the nanowire and heat it up via Joule heating. c) I-V and I-V_g characteristics after ablation. d) SEM image of the device at the end of the process. A clear sign of PMMA ablation is visible.

0/-40 V (red and blue curves, respectively). The abrupt change in the I-V characteristic was attributed to polymer ablation and consequent exposure of the nanowire surface to air, that reduced the channel conductivity. Accordingly, the nanowire FET resistivity, transconductance and threshold voltage calculated from the I-V and I-V_g characteristics measured after the process and shown in figure 5c were $3.8{\cdot}10^{-1}\Omega{\cdot}$m (at V_g=0), $3.21\pm0.03{\cdot}10^{-8}$ S and +10.36 V, respectively. An increase of the nanowire resistivity of almost two orders of magnitude and a large shift towards positive voltages of V_t were observed. In particular, the resistivity measured after the process was comparable with the nanowire resistivity in air (see SI). The variation in the electrical properties of the device associated with PMMA ablation is further demonstrated by the SEM image (figure 5d) displaying a complete ablation of the PMMA from the center and the side of the nanowire. Residual resist was found closer to the metal contacts where a lower temperature was expected, in good agreement with the theoretical temperature profile showed in Figure 4.

3 Conclusion

In conclusion, evidence of nanoheating by the ablation of PMMA deposited on ZnO nanowires with resistivities in the range of 10^{-1}-10^{-2} $\Omega{\cdot}$m was achieved by incorporation of the nanowires into a FET architecture. Notably, although the intrinsic electrical properties of the ZnO nanowires used in this work did not allow a relevant temperature rise in a two-terminal contacted configuration, the application of a back-gate resulted in a reduction of the nanowire resistivity by more than one order of magnitude. This in turn was enough to substantially boost the Joule heating power, eventually promoting deposited polymer ablation. Experimental data were supported by theoretical findings, thus providing clear evidence of the usability of NW-FET architectures for Joule heating. However, the presented NW-FET nanoheater device is not exempt from limitations. For example, the capacitative coupling between the source-drain contact and the back-gate reduced the range of applicable voltages and forced a specific bias configuration to avoid negative interference. Furthermore, the gate voltage could be greatly reduced by increasing the nanowire-gate capacitance, for instance by reducing the oxide thickness or by using a lateral gate electrode configuration instead of the back-gate lay-

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out used in this work. Nevertheless, the presented results corroborate the effectiveness of using an FET architecture to greatly broaden the Joule heating capabilities of nanowires and provided a scheme of work to explore a larger variety of semiconductor materials for micro and nano-heater applications. The presented approach opens the way to a number of promising nanoheater-based material manipulation capabilities including nanomaterial growths, radial doping, single core-shell heterostructuring and selective single nanowire functionalization.

Methods

ZnO nanostructures were grown by a simple vapour transport techniques enable by the vapor-liquid-solid (VLS) mechanism in a high temperature tube furnace as described elsewhere.[31]

Scanning electron microscopy (SEM) images of nanostructures were acquired using a field emission SEM (JSM-7500F, JEOL UK Ltd.) operating at beam voltages of 5 kV.

Electrical contacts were fabricated by metal evaporation of Ti/Au 90nm/50nm and Ti/Al 10nm/190nm. Size of each electrical pad was 200×200 μm. Metalization was patterned using standard photolithography and lift-off techniques. I-V characteristics of ZnO nanowire field-effect transistor were performed with a parameter analyzer (E5270B) by direct probing using a Wentworth micromanipulator 6200 probe station. The measurements were carried out at room temperature in air under ambient light conditions. For the Joule heating experiments the entire sample were previously covered with a PMMA (ARP679.04) layer having thickness of $\sim$200 nm by spin-coating (at 6000 rpm).

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