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# Characterization of Strontium Oxide Layers on Silicon for CMOS High-K Gate Stack Scaling

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High dielectric constant films have started to replace thin silicon oxynitride insulating layers in gates of MOSFET devices. Gate-stacks are commonly comprised of a TiN metal-gate electrode, a $HfO_2$ high-K dielectric and a very thin lower-K interfacial $SiO_2$ or SiO(N) layer on Si and deliver equivalent oxide thicknesses of ~10A. For high-performance logic technology, the International Technology Roadmap for Semiconductors indicated an EOT of 5.5 Å will be needed for bulk planar transistors with metal gate electrodes manufactured in 2014 [1]. It has been recently demonstrated that further scaling with the Hf-based dielectric can be achieved by replacing the SiO(N) interfacial layer with a thin high-permittivity strontium oxide (SrO) film [2]. In a low-temperature gate-last process equivalent oxide thickness (EOT) of 5 Å is measured, with competitive leakage current and interface trap density. Additionally the Sr-induced negative flatband voltage shift is suitable for n-channel transistors.

The $HfO_2$/SrO/Si(100) MOS capacitors were fabricated in a TiN gate-last process with a maximum process temperature of 400°C (forming gas anneal, FGA). Gate dielectrics were grown by ultra-high-vacuum molecular beam deposition (MBD) of epitaxial SrO followed by 20 Å $HfO_2$ as described in detail in [2,4]. After air transfer, TiN gate electrodes were formed. TEM analysis was carried out using a FEI F20 TEM/STEM and a TITAN Cs probe-corrected STEM. It is proposed that epitaxial SrO growth, such as is commonly used in the epitaxial growth of perovskites on Si(100) [3], passivates the Si surface and prevents deleterious $SiO_x$ formation [2]. Oxidation conditions were optimized using X-ray photoemission spectroscopy (data not shown) to ensure minimal $SiO_2$, strontium silicide, and hafnium silicide as well as stoichiometric $HfO_2$.

A high-angle annular dark field scanning transmission electron microscopy (STEM) micrograph taken at 1Å resolution of the TiN/HfO2/SrO/p-Si gate stack after device processing is shown in Fig. 1a. A distinct layer having a lower average atomic mass than that of $HfO_2$ is visible between the $HfO_2$ and the atomically flat Si channel, with a thickness of ca. 0.3–0.5 nm. This layer is thinner than typically observed after inadvertent Si surface oxidation during $HfO_2$ deposition. Line-profiles extracted from EDX spectral-line data confirms that the interface layer is Sr rich( fig 2a). The absence of a bright plane row of dots above the flat Si (100) surface indicates that this SrO rich-layer is amorphous with no epitaxial Sr (fig 1b). The EELS and EDX line-profile shows further that there is $HfO_2$-SrO intermixing (fig 2a & b). In addition the presence of Si in the interface layer is shown in the profile the Si L23 edge by EELS (fig 3). We note that all profiles recorded resulted in some visible damage after the scan even for low doses and is the cause for the extended O profile into the Si substrate (fig 2b) rather than there being O within the Si channel.

The deposition of the SrO is found to provide an equivalent thickness benefit of more than 3 Å. This interlayer scaling is due to the elimination of the $SiO_2$ layer and the formation of the higher K $Sr_xSi_yO_z$. It is suggested that the disruption of the epitaxial Sr layer is due to the intermixing of SrO

and HfO2 and the interfacial $Sr_xSi_yO_z$ formation and occurs either during the $HfO_2$ deposition or the FGA.

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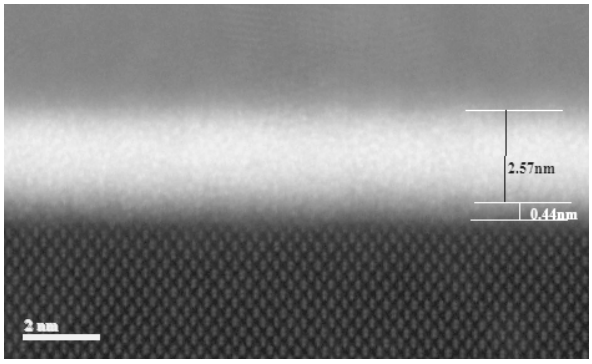


FIG. 1a. HAADF image of pSi/SrO/HfO2/TiN stack after 400C anneal. Shows atomically abrupt Si intertace

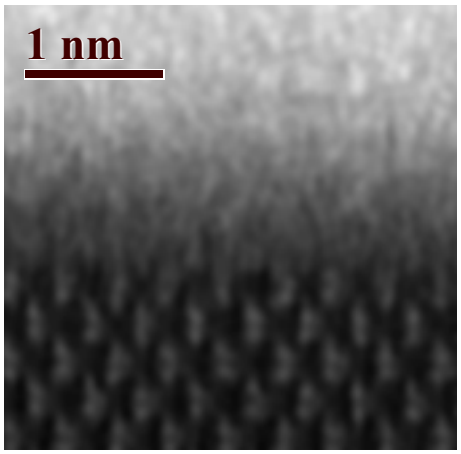


FIG 1b. Close-up of interface layers indicates the interface layer is disordered.

FIG. 3 (right) EELS profile indicating Si is present as a SrSiOx interface layer

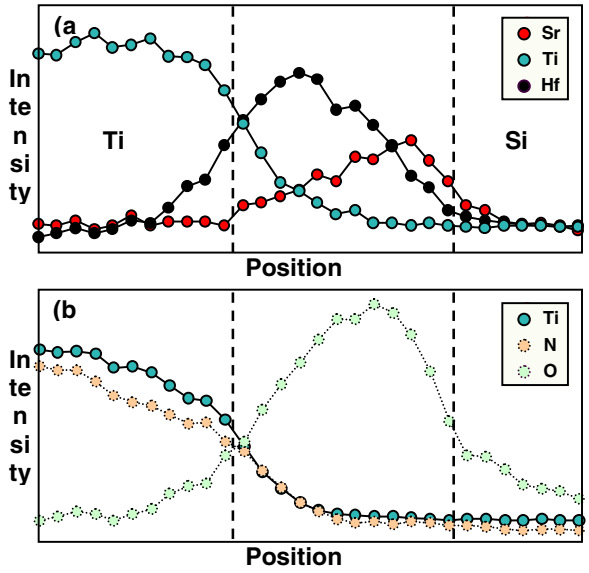


FIG.2. a) EDX profile and b) EELS indicates Sr rich interface layer and Sr interdiffusion into HfO2 layer. O is detected into Si channel due to radiation induced damage