Jinst

PUBLISHED BY IOP PUBLISHING FOR SISSA MEDIALAB

RECEIVED: *September 26, 2012*
ACCEPTED: *October 15, 2012*
PUBLISHED: *November 28, 2012*

TOPICAL WORKSHOP ON ELECTRONICS FOR PARTICLE PHYSICS 2012,
17–21 SEPTEMBER 2012,
OXFORD, U.K.

Upgrade of the cathode strip chamber level 1 trigger optical links at CMS

K. Ecklund,[a] **J. Liu,**[a] **A. Madorsky,**[b] **M. Matveev**[a,1] **and P. Padley**[a]

[a] *Rice University,*
Houston, TX 77005 U.S.A.
[b] *University of Florida,*
Gainesville, FL 32611, U.S.A.

E-mail: matveev@rice.edu

ABSTRACT: At the Large Hadron Collider (LHC) at CERN, the CMS experiment's Level 1 Trigger system for the endcap Cathode Strip Chambers (CSC) has 180 optical links to transmit Level 1 trigger primitives from 60 peripheral crates to the CSC Track Finder (CSCTF) which reconstructs muon candidates. Currently there is a limit of 3 trigger primitives per crate serving a cluster of 9 chambers. With the anticipated LHC luminosity increase up to $10^{35}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ at full energy of 7 TeV/beam the Muon Port Card (MPC), which transmits the primitives, the receiver in the CSCTF (Sector Processor) and the optical transmission system itself need to be upgraded. At the same time it is very desirable to preserve all the old optical links intact for compatibility with the present Track Finder during transition period. We present here the results of our efforts in the past two years to upgrade the MPC board, including the hardware developments, data transmission tests and latency measurements.

KEYWORDS: Trigger concepts and systems (hardware and software); Optical detector readout concepts; Trigger algorithms

[1] Corresponding author.

doi:10.1088/1748-0221/7/11/C11011

Contents

2012 JINST 7 C11011

1 Introduction

The CMS Muon System consists of three sub-detectors: the barrel Drift Tubes (DT), the barrel and endcap Resistive Plate Chambers (RPC), and the endcap Cathode Strip Chambers (CSC) [1]. There will ultimately be 540 CSC chambers. Currently there are 473 installed and operational since 2009, and 67 more are being fabricated. The CSC chambers are arranged in two endcaps, with four layers (or "stations") of chambers in each endcap. The Level 1 CSC Trigger system comprises the following parts (figure 1):

- On-chamber mounted electronics: Cathode Front End Boards (CFEB); Anode Front End Boards (AFEB); Anode Local Charge Track (ALCT) cards;
- Peripheral electronics housed in sixty 9U$\times$400 mm crates on the periphery of the return yokes of CMS: Trigger Motherboards (TMB), Muon Port Card (MPC), Clock and Control Board (CCB);
- The Track Finder (TF) crate in the CMS Underground Support Cavern with 12 Sector Processors (SP), one CCB and one Muon Sorter (MS) board.

The anode and cathode trigger primitives are combined together by the TMB and are called Local Charged Tracks (LCT). Each TMB serves one chamber. There are 9 TMB boards in the peripheral crate and they provide up to two LCT each to the MPC board; each LCT is represented by a 32-bit word that contains the anode and cathode hit coordinate and pattern type, as well as a trigger primitive quality. The MPC selects the three best primitives based on quality value and transmits them to the SP via the optical links at 1.6 Gbps rate. Each SP reconstructs up to three tracks. They are transmitted to a final stage of the CSC trigger, the MS board via the custom backplane. The MS selects the four best trigger tracks and transmits them via four copper links to the CMS Global Muon Trigger (GMT) crate, where they are combined with the DT and RPC candidates.

Our approach to the MPC upgrade and initial results were presented in the paper [2]. The idea was to replace the MPC mezzanine card with a new one, comprising not only the higher

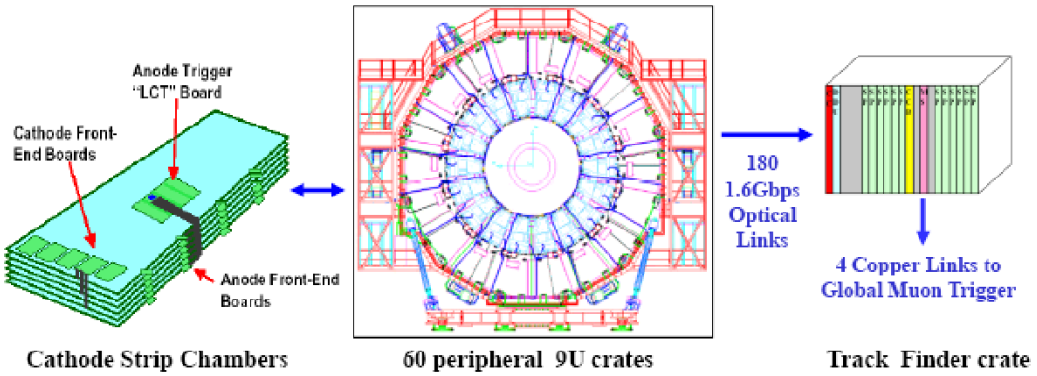

Figure 1. Block diagram of the Level-1 CSC Trigger electronics.

performance FPGA, but also an optical transmitter. The three old optical links are located on the main 9U MPC board and remain there, supported by the new FPGA. The proposal to upgrade the CSC TF was presented in the paper [3]. Below we provide more details on MPC mezzanine design, including the first prototype, based on Virtex-5 FPGA, and the second one, based on Spartan-6 FPGA with the embedded serial links. The first results of tests with the upgraded SP prototype SP10 are also given.

2 Performance of the existing link system and upgrade requirements

CSC Level 1 Trigger optical links have been operating reliably since 2009. One of the important tests conducted in October 2011 was a series of special LHC fills with two high intensity bunches colliding $> 2.4 \times 10^{11}$ protons/bunch and a 25 ns bunch spacing. It was shown that even with the small bunch spacing (as opposed to the present 50 ns spacing), a high number of collisions per bunch crossing, or pile-up (50–100), and a wide L1A coincidence window, there are only ~ 0.015 LCT per collision, integrated over all most critical inner CSC ME1/1 chambers. This means that under such conditions the optical links from the MPC to the TF, which can deliver up to 3 LCTs per bunch crossing from a cluster of 9 chambers, provide an adequate data throughput and do not reach saturation.

Within the next 10 years the LHC energy and luminosity will reach 7 TeV/beam and $10^{35}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ respectively. While the initial focus of the CMS muon system was triggering on isolated high momentum muons, interest in searching for lepton jets has arisen. For example, there are new physics scenarios where a Higgs decays to jets comprised of leptons [4] and there are proposed solutions to the dark matter problem that give rise to lepton jets observable at the LHC [5]. With the present selection algorithm "3 best LCT out of 18" the SP will see a mix and match of stubs from different muons. As a result, efficiency to reconstruct two energetic muons from a muon jet will be reduced. The ultimate solution would be to be able to transmit all the 18 LCTs from the MPC to the new SP board. At the same time the MPC FPGA should be able to perform the LCT sorting "N out of 18" (currently, N=3) if fewer than 18 LCTs are required. Support of the three older optical links residing on the main board is also needed for compatibility with the existing

2012 JINST 7 C11011

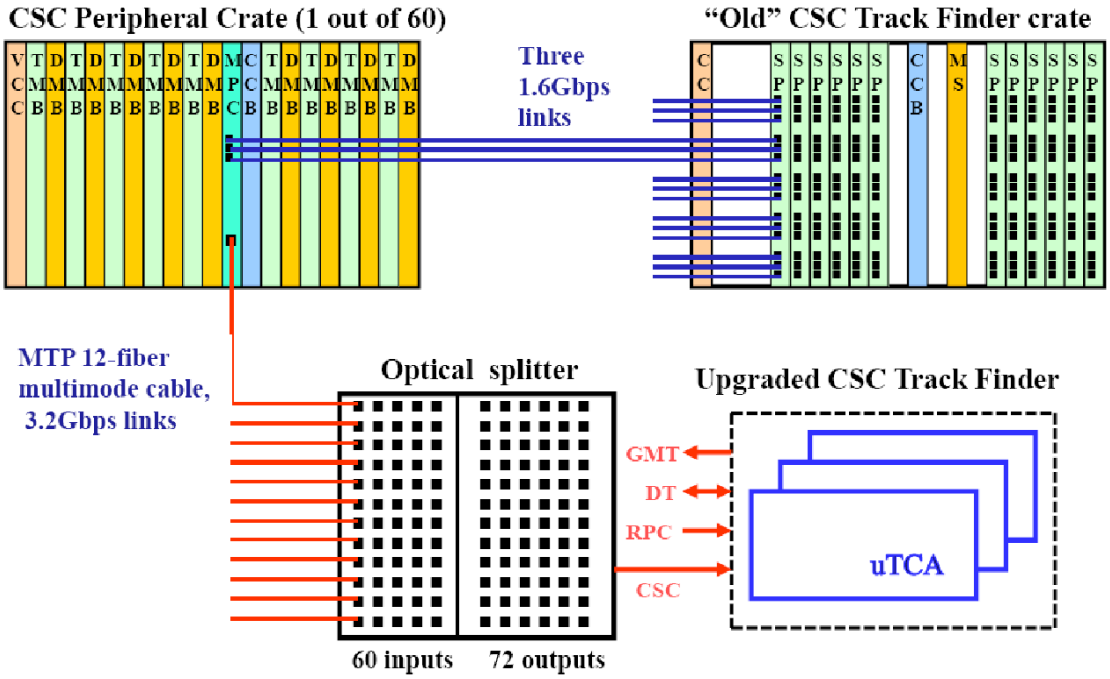

Figure 2. Block diagram of the upgraded CSC optical link system.

TF during a transition period. The upgraded CSCTF will be robust to higher occupancies, provide improved transverse momentum assignment and increased precision of muon output variables.

With the focus on commercial technologies, our choice is a Xilinx for the FPGA as before, and a SNAP12 standard [6] for the optical link. SNAP12 link with 12 independent fibers in the core cable can transmit all the 18 LCTs via single optical cable at a modest data rate of 2.4 Gbps or 3.2 Gbps per fiber. Two of these possibilities are described below. The block diagram of an optical data transmission system is shown in figure 2.

One of the requirements for the upgraded TF is that each SP must consider LCTs from the neighboring sector's chambers that overlap with its own sector, to provide better track reconstruction on sector's edge. It is sufficient for each SP to consider overlapping chambers on only one side of the sector. The overlap zone on the other side is processed by next sector's SP. To implement this requirement, the LCTs from chambers on the edge of each sector should be transmitted to two SPs simultaneously. The LCTs from all chambers that border another sector are sent to the TF via separate individual fibers inside the 12-core cable, fanned-out in the optical splitter (figure 2) and fed into two SPs. The new SP is currently being prototyped in the uTCA standard. It is expected that the upgraded TF with 12 new SP boards will occupy three uTCA crates. It will also accommodate interfaces to the DT and RPC trigger systems and provide optical outputs to the GMT.

3 Tests of the first mezzanine prototype based on Virtex-5 FPGA

The first prototype of the upgraded mezzanine was based on Virtex-5 XC5VLX110-FF1153 FPGA [2]. In spring of 2011 the board was slightly modified, with better clock and power dis-

2012 JINST 7 C11011

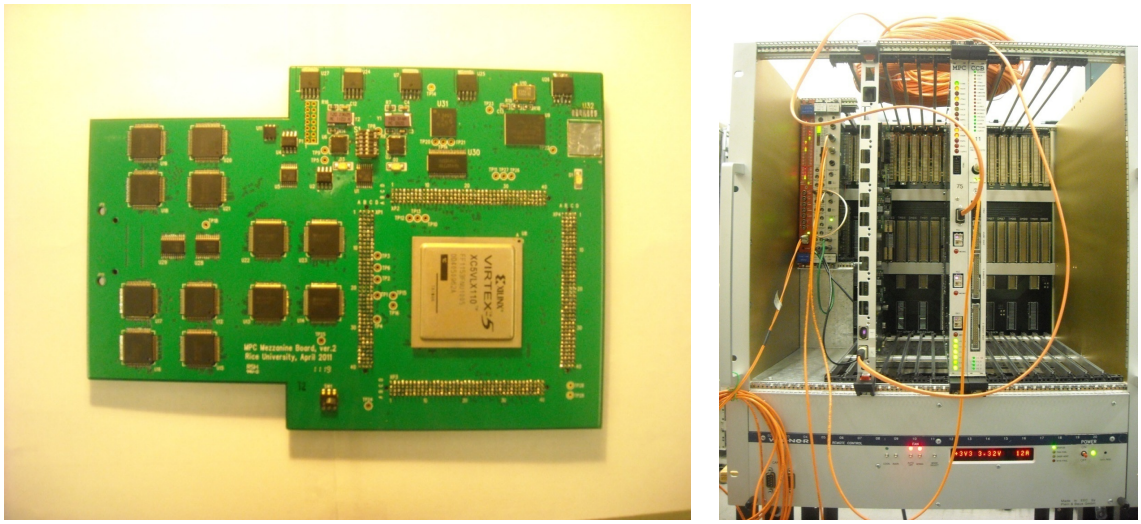

Figure 3. Virtex-5 FPGA Mezzanine (left) and upgraded optical link under test (right; the upgraded MPC board is in the middle of the crate, the SP10 is on the left).

tribution circuitry and an additional PROM option (XCF32P) (figure 3). Three spare MPC were equipped with the new mezzanines. They successfully passed data transmission tests with nine TMB boards in the peripheral crate. We also performed optical transmission tests with the upgraded prototype of the Sector Processor, SP10, designed at the University of Florida. The SP10 is a 9U VME board compatible with the existing TF crate. It includes five SNAP12 receivers and GTX deserializers implemented in the Virtex-6 FPGA. All 12 optical links from the MPC were running at 2.4 Gbps. The data rate limit is due to the TLK2501 transmitters since their highest parallel clock frequency is 125 MHz. The pseudo-random bit stream (PRBS) transmission from the TLK2501 transmitters to the GTX receiver showed no errors up to BER $< 10^{-13}$ per channel (it took approximately 90 minutes to run such a test). Data transmission from the output buffer in the Virtex-5 transmitter to the input buffer in the Virtex-6 receiver was also error free, although much lower statistics was accumulated due to slow software control over the test procedure.

The latency of serialization in the TLK2501 transmitter and deserialization in the GTX receiver were measured to be 15 ns and 101 ns respectively at 120 MHz. The receiver latency was minimized by bypassing its FIFO buffer. For comparison, these numbers at 80 MHz for the TLK2501 transmitter and TLK2501 receiver (current optical link) are equal to 23 ns and 57 ns respectively.

4 Second mezzanine prototype based on Spartan-6 FPGA

One of the disadvantages of the design described above is a relatively low data rate per channel due to discrete serializers. It would be natural to use a parallel frequency of ~ 160.32 MHz (quadruple the LHC operating frequency of ~ 40.08 MHz) and serial transmission rate of 3.2 Gbps, but the fastest device in the TLK family, the TLK3101, is limited to 156 MHz. The other disadvantage is a large power consumption of 12 TLK2501 transmitters. Embedded transceivers in the FPGA devices provide a good alternative. Among several families, the Spartan-6 from Xilinx seems to

2012 JINST 7 C11011

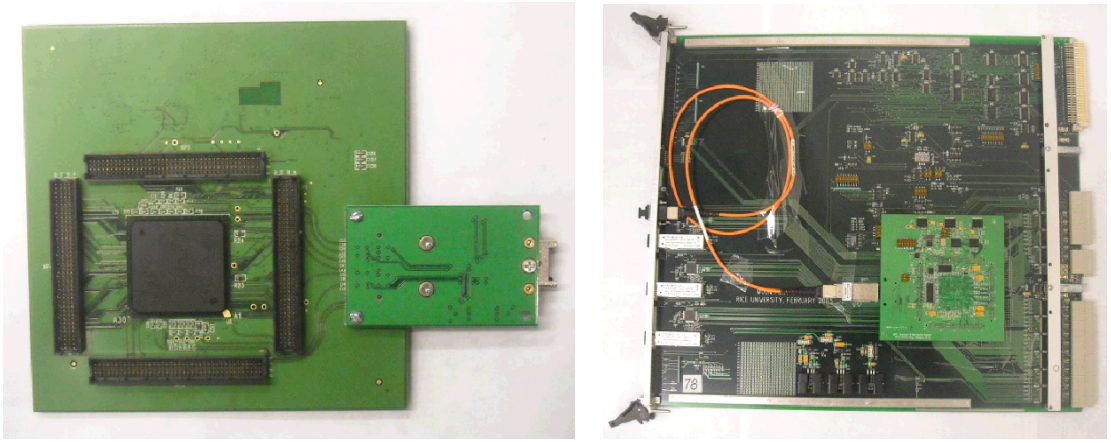

Figure 4. Spartan-6 FPGA mezzanine board (left) and the main MPC board (right).

be the most attractive. The GTP transceivers support transmission rate up to 3.75 Gbps and the largest device has 8 such links that are sufficient (after minor modifications in the present data format) to transmit all the 18 LCTs. Then only 8 out of 12 fibers are actually needed for the optical link. The largest 900-ball package has enough inputs and outputs to implement all the inter-board connections, and, of critical importance, they all are fully compatible with the 3.3 V CMOS logic levels on the main MPC board. The other advantages are lower power consumption ($\sim$ 50% less than for the XC5VLX110) and much lower cost ($\sim$ 5 times less expensive than the XC5VLX110 device). The new mezzanine has been designed in the fall of 2011. It carries the XC6SLX150T-3FGG900C FPGA with two XCF32P PROMs and the same SNAP12 plug-in transmitter card as the previous mezzanine (figure 4).

The firmware was modified to allow internal operation at 160 MHz, with embedded serializers. Xilinx ISE development systems allows to generate both uncompressed (for 2 PROMs) and compressed (for one PROM) versions of the configuration file. The fastest configuration times of 108 ms (uncompressed file) and 82 ms (compressed file) are achievable with the external clock of 40 MHz provided to the USERCLK pin of the FPGA from an external oscillator. It takes $\sim$ 20 minutes to program the compressed .svf file of $\sim$ 68 MB in size into one XCF32P PROM via the VME bus.

Two boards were built and tested with the Sector Processor SP10 in April 2012. After fixing the initial soldering errors the pseudo-random pattern transmission test showed no errors (BER $< 10^{-13}$). A limited number (few thousands) of random patterns from the output buffer of the transmitter FPGA to the input buffer of the receiver FPGA was sent under software control without errors as well. The new mezzanines were installed on a production MPC boards and tested in the peripheral crate with nine TMB boards. The "safe window" of data latching into the Spartan-6 FPGA was measured and found to be the same as the one of the present board ($\sim$ 7 ns within the 12.5 ns clock period).

The latency of the GTP transmitter in Spartan-6 without the TX buffer is equal to 6.5 cycles of the TXUSRCLK clock (320 MHz in our case), or $\sim$ 20 ns. This is slightly better than the latency of the current TLK2501 transmitter operating at 80 Mhz ($\sim$ 22 ns). The latency of the receiving GTX block in the Virtex-6 FPGA without the RX buffer is $\sim$ 69 ns.

2012 JINST 7 C11011

The Spartan-6 XC6SLX150T FPGA with the fully functional firmware consumes ~ 1 A on Vccint (1.2 V) and ~ 0.8 A (1.2 V) for GTP blocks. With all the GTP transmitters active, the device remains comfortably warm and doesn't require an external heatsink. The MPC with the Spartan-6 mezzanine attached consumes less than 4 A on 3.3 V.

5 Conclusion

Given its high performance, low cost and low power consumption, the Spartan-6 FPGA with 8 GTP serial links is the optimal choice for the Muon Port Card transmitter. The SNAP12 optical standard allows us not only to simplify the optical plant by having one optical cable per peripheral crate, but also introduces intrinsic redundancy for data transmission. Four remaining optical channels out of 12 can be used to transmit more data patterns at a lower rate, if needed.

Initial test results have demonstrated reliable data transmission at 3.2 Gbps with low latency of ~ 90 ns for serialization and deserialization. We plan to make some minor schematic improvements and replace the connector to attach the optical transmitter plug-in card with a more reliable one. Then in the fall of 2012 we will proceed with the fabrication of the pre-production mezzanine board. Irradiation tests are planned.

Another advantage of Spartan-6 devices is the ability to detect Single-Event Upsets and correct single-bit flips with the embedded Xilinx mitigation tools. Unlike the TF, all the MPC boards are located in the experimental hall and are subject to irradiation effects. While this mitigation core hasn't been implemented in our present design, we consider this possibility for the future. The other (commonly used at the CMS) mitigation scheme implies the reloading of the FPGA firmware from its PROM on periodical "Hard Reset" signal.

We expect that the upgrade of all MPC boards will be completed in 2014, during the first long LHC shutdown. The CSC Track Finder upgrade plans extend for a few more years beyond the 2013–14 shutdown period.

References

[1] CMS collaboration, S. Chatrchyan et al., *The CMS experiment at the CERN LHC*, 2008 *JINST* **3** S08004.

[2] M. Matveev and P. Padley, *Upgrade of the CSC endcap muon port card at CMS*, 2010 *JINST* **5** C11013.

[3] D. Acosta et al., *Commissioning of the CSC Level 1 Trigger Optical Links at CMS*, proceedings of the *TWEPP-09: Topical Workshop on Electronics for Particle Physics*, Paris France, September 21–25 2009, CERN-2009-006, pg. 431–434.

[4] A. Falkowski, J.T. Ruderman, T. Volansky and J. Zupan, *Discovering Higgs Decays to Lepton Jets at Hadron Colliders*, *Phys. Rev. Lett.* **105** (2010) 241801 [arXiv:1007.3496].

[5] N. Arkani-Hamed, D.P. Finkbeiner, T.R. Slatyer and N. Weiner, *A Theory of Dark Matter*, *Phys. Rev.* **D 79** (2009) 015014 [arXiv:0810.0713].

[6] SNAP12 specifications, available at http://www.reflexphotonics.com/PDFs/SNAP12_MSA_Rev1–1.pdf.

2012 JINST 7 C11011