Design and Analysis of Integrated CMOS High-Voltage Drivers in Low-Voltage Technologies

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Abstract

With scaling technology, the nominal I/O voltage of standard transistors has been reduced from 5.0 V in 0.25-μm processes to 2.5 V in 65-nm. However, the supply voltages of some applications cannot be reduced at the same rate as that of shrinking technologies. Since high-voltage (HV-) compatible transistors are not available for some recent technologies and need time to be designed after developing a new process technology, designing HV-circuits based on stacked transistors has better benefits because such circuits offer technology independence and full integration with digital circuits to provide system-on-chip solutions. However, the HV-circuits, especially HV-drivers, which are used for switching circuits, have a low efficiency because of the high on-resistance resulted by the stacked transistors.

Therefore, the main goal of this work is to design HV-drivers with a minimum on-resistance. To achieve this goal, initially, the gate voltage of each N-stacked transistor is calculated for driving the maximum current in the pull-up and pull-down paths of the HV-driver for various supply voltages. This calculation is performed using the computer algebra system MAXIMA. Regarding the results, which are presented in mathematical formulae, a circuit design methodology is presented to design a circuit to provide the required gate voltage of the each stacked nMOS or pMOS transistor of an HV-driver.

Based on this design methodology, a 2-stacked and a 3-stacked CMOS HV-driver is designed in 65-nm TSMC with I/O standard transistors with a nominal voltage of 2.5 V. The simulation results show that the provided gate voltages track approximately the ideal values. In comparison to prior work, the pull-up on-resistances of these HV-drivers are improved about 36% for the maximum allowed supply voltages of 5.0 V and 7.5 V and the pull-down on-resistances have an improvement of 40% and 46%, respectively. For switching a buck converter, the designed 3-stacked CMOS HV-driver is optimised by increasing the number of transistors in each stack. The circuit defined as *3HVDv1* with an area of about 0.187 mm^2 (435×431 μm^2) is implemented and fabricated on chips using two different package technologies: chip-in-package and chip-on-board. The parasitic effects of bond wires and packaging are discussed in detail. Both chips with different loads and overvoltage protections (OVP) are measured. The characteristics of the output signals and efficiencies are compared to each other. After increasing the supply voltage from 3.6 V to 5.5 V, the measurement results show that the chips using OVP have about 8%–10% higher efficiency in comparison to the efficiency of other chips. The output low-peaks (LP) of chips using a capacitor of 2.5 nF at the output, while switching a buck converter, varies from –2.1 V to –1.1 V, whereas that of chips with OVP is in the range from –0.8 V to –0.6 V, which is a substantial improvement. Furthermore the output of these chips with

OVP has significantly lower rise- and fall times than chips using capacitance of 2.5 nF for damping the output overvoltages.

In addition to this main goal, 3- and a 4-stacked CMOS HV-drivers, *3HVDv2* and *4HVDv3*, are designed in view of the drawbacks identified during the design, implementation, simulations and measurements; however, the second design (*4HVDv3*) is an improved form of the first one (*3HVDv2*). This HV-driver, *4HVDv3*, has improved benefits compared to the other designed circuits and also the common HV-drivers, because it can be applied for supply voltages ranging from 3.5 V to 7.5 V. This range is extended by 66%; no reference voltages are required since the regulating of the stacked main transistors is achieved by using a self-biasing cascade method, and also the circuit is stable for different process variations and temperatures between −40 °C and 125 °C.

To simplify the design of HV-circuits or interconnecting between these and low-voltage (LV-) circuits, the high-levels of the input signals should be reduced; therefore, three circuits, HLV-LS A, HLV-LS B and HLV-LS C, are designed to reduce the levels of a high-input signal up to 5.0 V to the lower levels between 0 V and 2.5 V. The HLV-LS C is an improved form of both circuits HLV-LSs A and B.

Zusammenfassung

Mit der Skalierung der CMOS-Technologie wurde die Nominal-Spannung der I/O Transistoren von 5,0 V in 0,25-μm Prozess auf 2,5 V in 65-nm reduziert. Es kann jedoch nicht die Versorgungsspannung von einigen Anwendungen mit derselben Rate verringert werden. Daher werden hochspannungskompatible Transistoren für die Schaltungsentwicklung eingesetzt, aber diese speziellen Komponenten sind noch nicht für die neuentwickelten Technologien verfügbar und werden erst in einiger Zeit einsatzbereit sein. Daher ist die Kaskadierung ("stacken") von einzelnen Standard MOS-Transistoren vorteilhaft, da nicht nur eine erhöhte Spannungsfestigkeit erreicht wird, sondern diese Methode Technologie-Unabhängigkeit bietet und volle Integration mit digitalen Schaltungen, System-On-Chip, ermöglicht. Jedoch haben die Hochspannungs- (HV-) Schaltungen basierend auf dieser Methode, wie Treiber, die Abwärtswandler umschalten, einen niedrigen Wirkungsgrad aufgrund des hohen "On"-Widerstandes durch die gestapelten Transistoren.

Das Ziel dieser Arbeit ist, einen HV-Treiber mit einem minimalen "On"-Widerstand zu entwickeln. Um das zu erreichen, wird zuerst die Gate-Spannung jedes gestapelten Transistors zum Antreiben mit dem maximalen Strom im Pull-up und Pull-down-Pfad des HV-Treibers für verschiedene Versorgungsspannungen berechnet. Diese Berechnung wird mit Hilfe des Computer-Algebra-Systems "MAXIMA" durchgeführt. Im Hinblick auf die Ergebnisse, die in mathematischen Formeln erfolgen, wird eine Methodologie für Schaltungsentwürfe dargestellt, um die erforderten Gate-Spannungen zu generieren.

Auf Basis dieser Design-Methodik, wird ein 2- und ein 3-fach gestapelter CMOS HV-Treiber in 65-nm-TSMC Technologie mit I/O-Standard-Transistoren mit einer Nennspannung von 2,5 V entworfen. Die Simulationsergebnisse zeigen, dass die generierten Gate-Spannungen in etwa den Idealwerten entsprechen. Für die maximal zulässigen Versorgungsspannungen von 5,0 V und 7,5 V, sind die Pull-up "On"-Widerstände der entwickelten HV-Treiber etwa 36% und die Pull-down "On"-Widerstände 40% und 46% im Vergleich zu einer früher veröffentlichten Arbeit verbessert.

Für die Umschaltung eines Abwärtswandlers wird der entworfene 3-fach gestapelte CMOS HV-Treiber durch Erhöhung der Transistoren-Anzahl in jedem Stapel optimiert, und als 3HVDv1 definiert. Die Schaltung hat eine Fläche von etwa 0.187 mm^2 (435×431 μm^2) und ist auf Chips implementiert. Zwei verschiedene Gehäusetechnologien - Chip-in-Package und Chip-on-Board - wurden gefertigt. Die parasitären Effekte von Bonddrähten und des Gehäuses werden ausführlich in dieser Arbeit diskutiert. Beide Chips sind mit unterschiedlichen Belastungen und Überspannungsschutz mit einer Kapazität von 2,5 nF oder Schottky Dioden (OVP) gemessen worden und deren Ausgangssignale und Effizienz wurden miteinander verglichen. Bei einer Versorgungsspannung von 3,6 V bis 5,5 V, haben

Chips mit OVP eine höhere Effizienz von ca. 8%-10%, im Vergleich zu Chips ohne Schottky Dioden.

Neben diesem Hauptziel, verbesserte 3- und 4-fach gestapelte CMOS HV-Treiber, 3HVDv2 und 4HVDv3, zu entwerfen; ist jedoch der zweite Treiber (4HVDv3) eine verbesserte Form des ersten (3HVDv2) und kann für Versorgungsspannungen im Bereich von 3,5 V bis 7,5 V, der eine Erweiterung von 66% im Vergleich zu üblichen Treiber aufweist, angewendet werden. Aufgrund des Selbstvorspannungs-Verfahren, werden die Haupttransistoren des Treibers ohne zusätzliche Referenzspannung für die aktive Pull-Down und Pull-Up Zustände reguliert. Die Schaltung weist keine Überspannungen bei verschiedenen Verfahrensvarianten und Temperaturen zwischen –40 °C und 125 °C auf.

Um das Design von HV-Schaltungen zu vereinfachen, oder die Funktion mit Niederspannung- (LV-) Schaltungen zu ermöglichen, sollten die Hochpegel der Eingangssignale reduziert werden. Daher sind drei Pegel-Wandler, HLV-LS A, HLV-LS B und HLV-LS C, entworfen worden, um die Pegel eines Hochspannungs-Signals bis zu 5,0 V auf Werte zwischen 0 V und 2,5 V zu reduzieren. Der Pegel-Wandler HLV-LS C ist eine verbesserte Form der beiden Schaltungen HLV-LSs A und B.

To my husband,

Dieter Obergassel

In memory of my father,
Dr. MD Asghar Pashmineh Azar

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List of Abbreviations and Symbols

Abb. & Symbols	**Descriptions**
3HVDv1	3-stacked CMOS HV-Driver version 1
3HVDv2	3-stacked CMOS HV-Driver version 2
4HVDv3	4-stacked CMOS HV-Driver version 3
$\mathrm{A_b}$	Cross-sectional area of bond wire
$\mathrm{A_{SE}}$	Cross-sectional area of skin layer
BC (bc)	Buck converter
C5OVP	Chip-in-package no. 5 using Schottky diode (OVP)
$\mathrm{C_{GB}}$	Capacitance between gate and bulk of MOS transistor
$\mathrm{C_{GD}}$	Capacitance between gate and drain of MOS transistor
$\mathrm{C_{GS}}$	Capacitance between gate and source of MOS transistor
Channels C1–C4	Channels of oscilloscope
Chips C2–C6	Chip-in-package no. 2–6
Chips C3x–C6x	Chips in-package with a capacitive load Cx
CIP	Chip-in-package
CL	Load Capacitor
COB	Chip-on-board
COB2	Chip-on-board no. 2
COB5	Chip-on-board no. 5
$\mathrm{C_{ox}}$	Gate-oxide capacitance of MOS transistor
Cx	Capacitive load at output node of chip (driver)
D	Duty-cycle of driver input signal Vin
$\mathrm{D_b}$	Diameter of bond wire
DNW	Deep n-Well
$\mathrm{D_p}$	Duty-cycle of driver output signal Vout
GC-circuits	Gate-controlling circuits
GCnk	Gate-controlling circuit of kth–stacked nMOS transistor
GCpk	Gate-controlling circuit of kth–stacked pMOS transistor
HLV-LS	High-to-low voltage level-shifter
HP	High-peak of driver output voltage (positive overvoltage)
HV-	High-voltage
$\mathrm{I_{bc}}$	Current flowing through buck converter
$\mathrm{I_{DR}}$	Current of driver ($\mathrm{I_{DR}}$)
$\mathrm{I_{out}}$	Output current
$\mathrm{I_{RL}}$	Current flowing through load-resistor
$\mathrm{I_{VHdd}}$	Current flowing from source ($VHdd$)

$\mathrm{ID_n}$	Pull-down current of driver
$\mathrm{ID_p}$	Pull-up current of driver
L	Inductor
l_b	Length of bond wire
$\mathrm{L_b}$	Inductance of bond wire
$\mathrm{L_{bc}}$	Inductor of buck converter
l_f	Length of lead finger
$\mathrm{L_f}$	Inductance of lead finger
LP	Low-peak of driver output voltage (negative overvoltage)
LS	Level-shifter
LV-	Low-voltage
OVP	Overvoltage protection using Schottky diode
N	Number of stacked transistors
Mnk	kth-stacked nMOS transistor of HV-driver
Mpk	kth-stacked pMOS transistor of HV-driver
r_b	Radios of bond wire
RL	Load resistor
Ron (ron)	On resistor of transistor or driver
t_f	Thickness of lead finger
$\mathrm{V_{bc}}$	Output voltage of buck converter
Vdd	Supply low-voltage
$\mathrm{VD_{pk}}$	High rail voltage of GCnk
$\mathrm{VD_{nk}}$	Low rail voltage of GCpk
VGnk	Gate-voltage of kth-stacked nMOS transistor
VGpk	Gate-voltage of kth-stacked pMOS transistor
VHdd	Supply high-voltage
Vin	Input signal
Vn	Nominal voltage of transistor
Vout	Output voltage of driver
Vpin	Input signal of driver's pull-up path
VSnk	Source-voltage of kth-stacked nMOS transistor
VSpk	Source-voltage of kth-stacked pMOS transistor
$\mathrm{V_{thn}}$, $\mathrm{V_{Thn}}$	Threshold voltage of nMOS-transistor
$\mathrm{V_{thp}}$, $\mathrm{V_{Thp}}$	Threshold voltage of pMOS-transistor
α_{HV}	Ratio of VHdd to nominal voltage (Vn)
α_n	Value between 0 V and threshold voltage of nMOS transistor
α_p	Value between 0 V and absolute value of $\mathrm{V_{thp}}$

β	Transconductance parameter of MOSFET $=\mu_0 C_{ox} \times (W/L)$
η	Efficiency
δ	Thickness of skin effect
ρ_b	Electrical resistivity of bond wire
μ	Electron mobility
w_f	Width of lead finger

DNW nMOS Transistor	
D1, D1’	Parasitic diode across bulk-source/bulk-drain junctions
D2	Parasitic diode across bulk-DNW junction
D3	Parasitic diode across Psub-DNW junction
Q1, Q’	Parasitic npn BJT formed by bulk (base), source/drain (emitter) and DNW (collector)
Q2	Parasitic pnp BJT formed by DNW (base), bulk (emitter) and Psub (collector)
B	Bulk node
D	Drain node
G	Gate node
S	Source node
Psub	P-substrate node
$\mathrm{R_D}$	Parasitic resistance of drain layer
$\mathrm{R_S}$	Parasitic resistance of source layer
$\mathrm{R_{DNW}}$	Parasitic resistance of DNW layer
$\mathrm{R_{Psub}}$	Parasitic resistance of p-substrate layer
$\mathrm{R_{BS}}$	Parasitic resistance between bulk and source
$\mathrm{R_{BD}}$	Parasitic resistance between bulk and drain
$\mathrm{R_B}$	Parasitic resistance between bulk and DNW
$\mathrm{R_{Psub}}$	Parasitic resistance between Psub and DNW

Parasitic Bipolar Transistor	
B	Base node
C	Collector node
E	Emitter node
$\mathrm{R_b}$	Parasitic resistance of base layer
$\mathrm{R_c}$	Parasitic resistance of collector layer
$\mathrm{R_e}$	Parasitic resistance of emitter layer
$\mathrm{V_{BE}}$	Base-emitter voltage
$\mathrm{V_{BC}}$	Base-collector voltage
$\mathrm{V_{CE}}$	collector-emitter voltage

Buck Converter	
D	Duty-cycle of driver input signal Vin
D_p	Duty-cycle of driver output signal Vout
D_{bc}	Duty-cycle of driver output signal Vout ($=D_p$)
I_{bc}	Current flowing through buck converter
L, L_{bc}	Inductor of buck converter
VGnk	Gate-voltage of kth-stacked nMOS transistor
VGpk	Gate-voltage of kth-stacked pMOS transistor
VHdd	Supply high-voltage
Vin	Input signal
Vn	Nominal voltage of transistor
Vout	Output voltage of driver
Vpin	Input signal of driver's pull-up path
VSnk	Source-voltage of kth-stacked nMOS transistor
VSpk	Source-voltage of kth-stacked pMOS transistor
V_{bc}	Output voltage of buck converter

Contents

Chapter 1

Introduction

1.1 Motivation

Power management circuits are used extensively in electronic systems for consumers, sensors and automotive electronics. They are responsible for setting the input voltages in different and stable internal supply voltages as required by sub-circuits in the systems [9]. Therefore, high-voltage integrated circuits such as low-dropout voltage regulators (LDOs) and drivers for switching converters are required to provide a stable DC voltage, to step-up and/or step-down a DC supply voltage. In addition to power management, HV-circuits are also required in interfaces to other systems such as between I/Os of integrated circuits and bus controls such as USBs.

With scaling technology, the nominal I/O voltage of standard transistors has been reduced from 5.0 V in 0.25 μm processes to 2.5 V in 65-nm. However, the supply voltages of some applications cannot be reduced at the same rate of shrinking technologies.

Since the standard transistors of nanometer CMOS technologies are only compatible with low voltages within technology limits and cannot handle the higher voltages, HV-circuits are often designed using high-voltage compatible transistors [1][3][4][40][45]. However, these transistors are not available in some recently developed processes such as the 28-nm TSMC (**T**aiwan **S**emiconductor **M**anufacturing **C**ompany Limited) technology and will take a while to be developed.

A comparison between the technologies of TSMC is shown in Figures 1a and 1b for March 2011 and May 2016 respectively. As can be seen in 2011, HV-compatible transistors were not available for 65-nm technology; however, they have been recently developed for 65-nm, and for 40-nm technology they are still in the process according to the technology portfolios presented in May 2016.

The other decisive disadvantage of the HV-compatible transistors [31] is the cost, be-

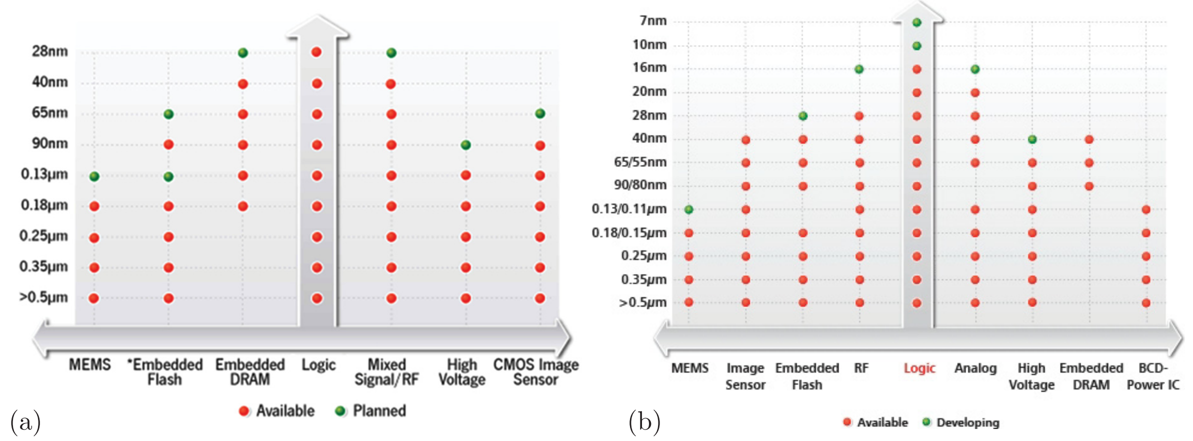


Figure 1.1: Technology Portfolios of TSMC in a) March 2011 [9], and b) May 2016 [10]

cause these transistors require extra steps and mask sets during processing. In the worst case, since they are not compatible with CMOS technology, two separate chips are required, which increases the size and also the cost of the system. Informations on doping profiles, steps of processing and other resources for HV-transistors are not always available [31]. The other drawback is that the parasitic behaviour of HV-compatible transistors is not well modelled [31]. Furthermore, for some HV-transistors such DMOS (**D**ouble-diffused **MOS**) transistors, a low doped n-type drain layer is used to increase the breakdown voltage; however, this increases the on-resistance [31][49].

An alternative solution to these problems is to use stacked low-voltage standard CMOS transistors. This method is technology independent and is compatible with scaled technologies [2][30]–[36]. Since this method requires no extra mask sets, it is also attractive in terms of cost. Additionally, the parasitic behavior of these transistors is very well modelled [31]. The major point of this method is to maintain the voltage between gate (G), drain (D), source (S) and bulk (B) terminals within the technology-limited range, as shown in Figure 1.2, where Vn is defined for the nominal voltage of the transistor.

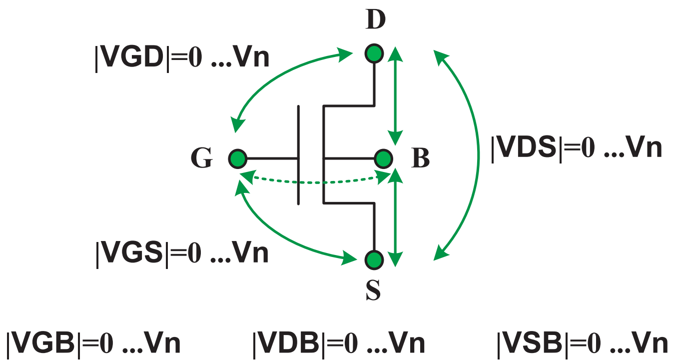


Figure 1.2: Low-voltage standard transistor

In this work, the designed circuits are based on stacked I/O-nMOS "*nch_25*" and I/O-pMOS transistors "*pch_25*" obtained from 65-nm technology of TSMC with a nominal I/O voltage of 2.5 V. According to the data sheet, the operating bias conditions for these transistors are as follows:

$$0 \leq |VGS| \leq 2.5\,V,\ 0 \leq |VDS| \leq 2.5\,V,\ 0 \leq |VGD| \leq 2.5\,V,$$

$$0 \leq |VSB| \leq 2.5\,V,\ 0 \leq |VGB| \leq 2.5\,V,\ 0 \leq |VDB| \leq 2.5\,V$$

where 2.5 V is the nominal voltage (*Vn*) of the mentioned transistors and the terms *VGS*, *VDS*, *VGD*, *VSB*, *VGB* and *VDB* are defined as the gate-source, drain-source, gate-drain, source-bulk, gate-bulk and drain-bulk voltages respectively. The junction breakdown voltages determine the safe operating area of a transistor, but to ensure the extendibility of the models, the devices have been measured by the company TSMC up to 1.2 times the nominal voltage of 2.5 V, i.e. 3.0 V. Although the upper limits of the above range are up to 3.0 V ($1.2\times Vn$), in this work the voltage difference between the terminals of each transistor is considered to be 2.5 V with a tolerance of 5% in order to allow for some design margin because of undesired overvoltages during switching.

1.2 Objectives

By scaling down in the CMOS technology, the gap between the main supply voltage of a power management circuit and the internal supply voltages of its sub-circuits has increased; therefore, step-down DC-DC converters, defined as buck converters, are required to reduce the main supply voltage to the desired lower voltages. To achieve higher power conversion efficiency, the buck converter should be switched by a high-voltage (HV-) driver containing MOS transistors instead of diodes [5, pp 63–74][6]–[8].

Since the supply voltage is higher than the nominal voltage of the standard transistors, according to the cascade technology, HV-drivers are designed based on stacked CMOS transistors. However, because of the on-resistance of each transistor, the circuit based on the cascade technology increases the power loss of the buck converter, which is switched by such a driver. Furthermore, the on-resistances of the stacked transistors also increase the switching time of the buck converter.

Therefore, the main objective of this thesis is to reduce the pull-up and pull-down on-resistances of HV-drivers. To achieve this goal, firstly, theories are presented for the gate voltage of each transistor of an N-stack CMOS HV-driver to drive the maximum current in the pull-up and pull-down paths. The theories are valid for two groups of supply voltages: divisible and indivisible by the nominal voltage of the transistor used in the cascade technology. According to these theories, a circuit design methodology is introduced for gate-controlling circuits to regulate stacked transistors and to drive the maximum current in the HV-driver paths, which indicates that the driver has a minimum on-resistance.

In pursuance of the theory and circuit methodology, a 2- and a 3-stacked CMOS HV-driver with nearly minimum on-resistance are designed. The provided gate voltages are compared to the ideal values and to prior work. The design of the presented 3-stacked CMOS HV-driver is optimized for switching a buck converter and implemented on chips. The chips are mounted on printed circuit boards using two package technologies: chip-in-package and chip-on-board. Both are measured with different loads and compared to each other.

In view of the drawbacks, which were identified during the design, implementation, simulations and measurements and also the requirements of pre-circuits for regulating the HV-circuits, the following HV-circuits are designed in addition to the above goal:

- two HV-drivers with different circuit design methodologies
- low- to high-voltage level-shifters published in [Pub3],[Pub4] and [Pub5]
- high- to low-voltage level-shifters

1.3 Thesis Structure

The content of this work is structured as follows.

Following this introduction, Chapter 2 presents a brief overview of buck converter switching using a high-voltage driver. Additionally, the structure, characteristics and an equal circuit model of a deep-nWell nMOS transistor are presented.

Chapter 3 describes the operation of an HV-driver in detail. Furthermore, to minimize the pull-down and pull-up on-resistances of an N-stacked CMOS HV-driver, theories and a circuit design methodology to control the stacked CMOS transistor for driving the maximum currents in both driver's paths are presented.

Based on the presented circuit designs providing the gate voltages, a 2-stacked and a 3-stacked CMOS HV-driver are designed, which are described in Chapter 4. The circuits are proved for various supply voltages. The provided gate voltages are compared to a published work and also to the ideal values presented in Chapter 3.

Chapter 5 introduces a 3-stacked CMOS HV-driver (*3HVDv1*), which is optimised for switching a buck converter and is implemented on chips with two different package technologies, chip-in-package and chip-on-board. The layout, simulation and measurement results are represented.

Chapter 6 presents the level-shifters used in the HV-circuit *3HVDv1* and two improved HV-drivers with different circuit designs. Furthermore, three concepts are introduced to reduce the high levels of an input signal to lower levels, which are defined as high-to-low level-shifter. The work will be closed with a discussion and conclusion in Chapter 7.

The presented circuits in this work have been published in various conference articles. However, the simulation results and also the circuit designs in this work may be different from the published results, as the respective circuits have been optimized further since the results were published.

Chapter 2

State Of The Art

This section covers the state-of-the-art of the buck converter, which is the main application of the designed 3-stacked CMOS HV-driver (*3HVDv1*) implemented on chips in this work. A buck converter is a DC-DC power converter, which steps down the supply (battery) voltage to a required voltage at its output load. The principle of the system is introduced. In addition, the structure and characteristics of a **D**eep **N**-**W**ell **n**-type **MOS** **T**ransistor, abbreviated as **DNW nMOSFET** or **DNW nMOS** transistor, which are used in the circuit *3HVDv1* of this work, are presented.

2.1 Buck Converter

Over the last few years, consumer demands for battery-operated portable electronic products such as smart-phones, tablet computers and laptops have been growing, and becoming increasingly evident. In these devices, the main power for the sub-circuits is provided by a battery. By scaling down the CMOS technology, the gap between the battery voltage and the required internal supply voltages of the sub-circuits has been increased; therefore, step down DC-DC converters, which are defined as buck converters, are desired to reduce the battery voltage to the required voltages. To achieve higher power conversion efficiency, the buck converter should be switched by MOS transistors instead of diodes [5, pp 63–74][6]–[8].

2.1.1 Operation Principle

Figure 2.1a shows the principle of a buck converter, which contains a battery voltage of *VHdd*, a load resistance R_L and an LC low-pass filter consisting of an inductor L and a capacitor C_L [5] and two switches *S1* and *S2*. The buck converter steps down the battery voltage (*VHdd*) to the required voltage V_{bc} at its output load. The node voltage between both switches is labeled *Vout*. HV-compatible CMOS transistors [45][49], Mn and Mp, which are switched by the input signal *Vin*, are employed instead of the switches *S1* and *S2*, respectively, as shown in Figure 2.1b.

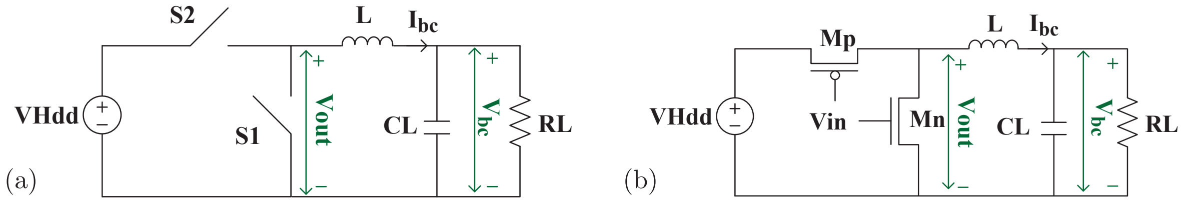


Figure 2.1: Principle of a buck converter with (a) two switches *S1* and *S2* and, (b) a CMOS containing Mn and Mp as switches

The node between both transistors is either connected to the supply (battery) voltage *VHdd* in the off-state, when the input signal is low enough to switch the MOS transistors Mp on and Mn off, or to ground in the on-state, when the input signal is high enough to turn Mn on and Mp off.

It should be mentioned that since the main goal of this research is to design an HV-driver switching a buck converter, the on- and off-states relate to the input signal (*Vin*) of HV-drivers, when the signal is high or low respectively. According to the high and low levels of the input signal *Vin*, the pull-down network of an HV-driver should also be on or off respectively. The term "*D*" relates also to the duty-cycle of *Vin*. The input power source of the buck converter refers to the supply voltage *VHdd*.

By periodically switching the transistors due to an input pulse signal, the node voltage (*Vout*) between both transistors can be provided as a rectangular wave with two levels *VHdd* and 0 V, duty cycle D_p and a period of T, as depicted in Figure 2.2 [5]. The duty cycle (D) of the input signal *Vin* is equal to (1–D_p). As can be seen in Figure 2.2, the inductor current waveform (I_{bc}) increases during the off-state (Mp is on) and then reduces during the on-state (Mp is off). The LC low-pass filter (L and C_L) provides the desired voltage V_{bc} as an average voltage of *Vout*, thus the buck converter steps down the supply voltage *VHdd* to V_{bc} at its output load. The ideal voltage conversion ratio of a buck converter is the ratio of the stepped down voltage to the supply voltage and can be expressed as follows [5][11]–[16]:

$$M(D) = D_p = \frac{V_{bc}}{VHdd} = 1 - D, \tag{2.1}$$

where D and D_p are defined as the duty-cycle of *Vin* and *Vout*, respectively.

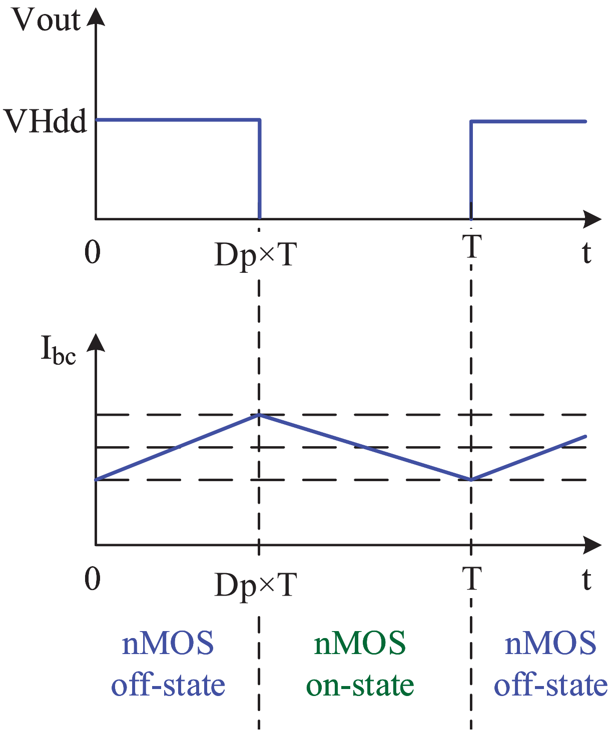


Figure 2.2: The driver output voltage and inductor current of the buck converter

Since the converter has various power losses because of the non-ideal switches (Mp and Mn), conductors, gate-charging and discharging and also passive components, the ratio of the converter output voltage and supply voltage is not equal to the duty-cycle of *Vout*. In terms of neglecting a short-circuit current between both switches and power losses, the efficiency (η) of the buck converter can be defined as [11]:

$$\eta = \frac{V_{bc}}{VHdd \times D_p} = \frac{V_{bc}}{VHdd \times (1 - D)} \tag{2.2}$$

2.1.2 HV-Driver based on Stacked Standard CMOS

In this work, the standard low-voltage (LV-) transistors, which were described in Section 1.1, are used. To avoid overvoltages, circuits are designed based on stacked LV-transistors. Therefore, for switching the described buck converter, N-stacked pMOS transistors should be inserted between the supply and the node "**ns**" and also N-stacked nMOS transistors between the node **ns** and ground (Figure 2.3) [43][44]. The node **ns** is the connection node between the transistors and the inductor of the buck converter. Both types of transistors build a driver, which is called a high-voltage (HV-) driver. The number of stacked transistors depends on the high-supply voltage *VHdd* and the nominal operating voltage (Vn) of the LV-transistors.

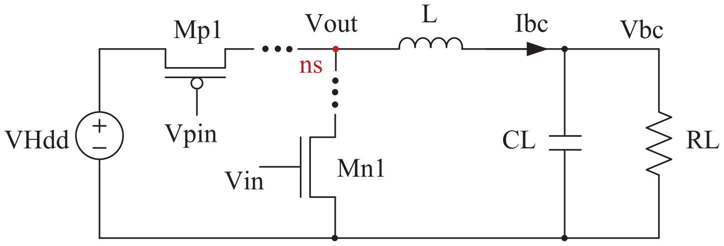


Figure 2.3: Buck converter switched by an HV-driver based on stacked standard CMOS

A MOS transistor contains parasitic capacitances such as the gate-source (C_{GS}) and gate-drain (C_{GD}) capacitances, which impact the charging and discharging times of the drain and source nodes. Since during switching, the gate-source and gate-drain capacitances of each transistor are not equal to each other, an overvoltage would occur in an HV-circuit. Therefore, avoiding an overvoltage is a major consideration for the circuit design based on stacked LV-transistors. With respect to the transient gate-source voltage characteristic, Figure 2.4 shows the gate-source (C_{GS_Mn1}) and gate-drain (C_{GD_Mn1}) capacitances of the input nMOS transistor Mn1 used in the HV-driver (*3HVDv1*) designed in this work.

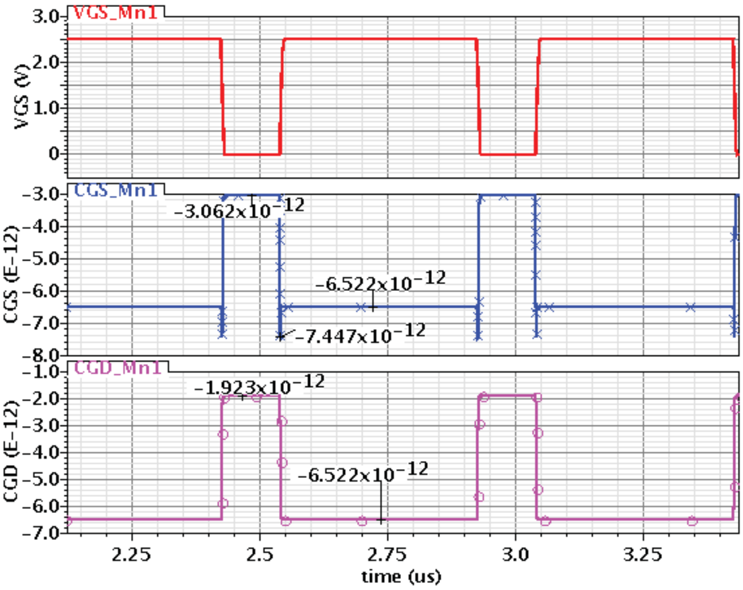


Figure 2.4: Transient characteristics of the parasitic source-gate and drain-gate capacitance

As can be seen, during switching, the absolute value of C_{GS_Mn1}, varying between 3.1 pF and 7.4 pF, is higher than that of C_{GD_Mn1} changing between 1.9 pF and 6.5 pF. In the on-state, both capacitances are equal, since the transistor Mn1 operates in the linear region.

2.1.3 Principle of the System

In this work, a 3-stacked standard CMOS HV-driver is designed to switch a buck converter stepping down the supply voltage from 5.5 V to 1.2 V with a frequency (f_s) of 2 MHz (Figure 2.5). The standard transistors have a nominal I/O voltage of 2.5 V. The HV-driver contains three pMOS transistors Mp1, Mp2 and Mp3 in the pull-up path and three nMOS transistors Mn1, Mn2 and Mn3 in the pull-down path. The input transistors Mp1 and Mn1 are switched by the input signals *Vin* and *Vpin*, whereas *Vpin* is level-shifted from *Vin* due to a circuit called a level-shifter. The other stacked transistors should be regulated by external circuits $\mathrm{GC_{n2}}$, $\mathrm{GC_{n3}}$, $\mathrm{GC_{p2}}$ and $\mathrm{GC_{p3}}$ defined as gate-control circuits according to the input signal *Vin* varying between ground (0 V) and a voltage equal to the nominal operating voltage (*Vn*= 2.5 V) of the standard transistors. To switch the pMOS transistor Mp1, the signal levels of *Vpin* have to be 5.5 V (*VHdd*) and 3.0 V (*VHdd–Vn*).

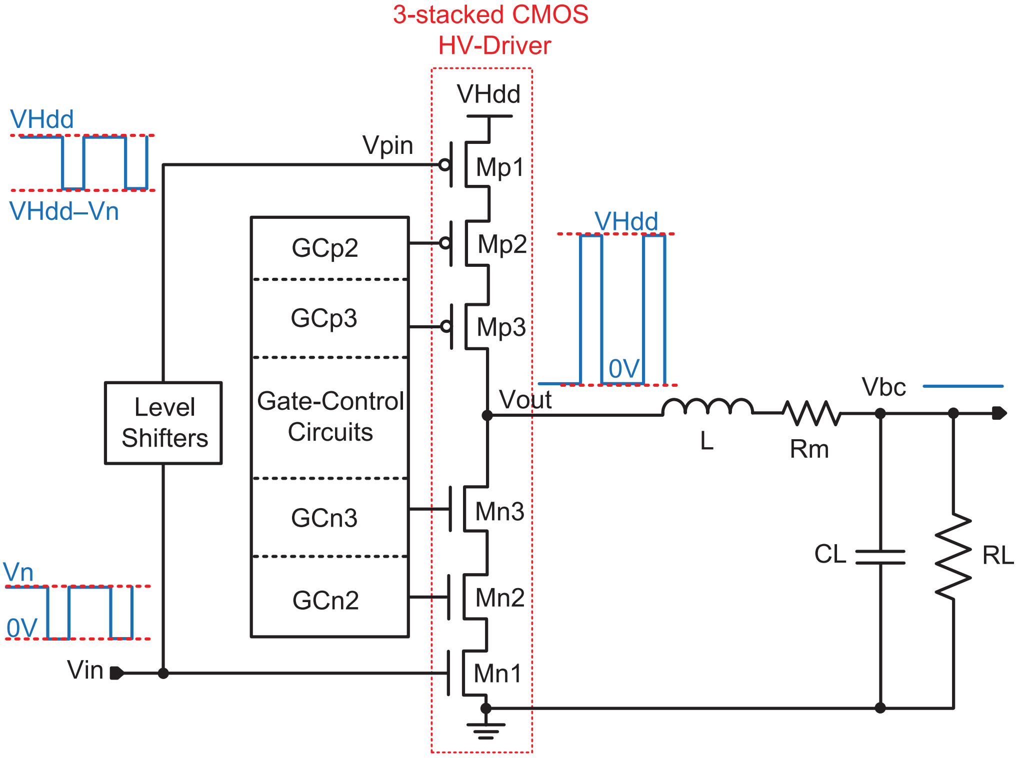


Figure 2.5: Principle of a buck converter switched by the designed 3-stacked CMOS HV-driver

The load resistor R_L and the capacitor C_L of the proposed buck converter have a value of 12 Ω and 10 μF, respectively. From the determined components' values, a current of 100 mA (ΔI_{bc}), which is the average of I_{bc}, is expected to flow through the converter output load. Then, the inductor of the buck converter can be calculated using the following equation [11]:

$$L = \frac{V_{bc} \times (VHdd - V_{bc})}{VHdd \times fs \times \Delta I_{bc}} = 4.69\mu H \approx 4.7\mu H \tag{2.3}$$

One major drawback of the circuit design based on stacked transistors is that switching the buck converter is slow because of the pull-down and pull-up on-resistances of the HV-driver, which depend on the on-resistance of each stack transistor.

By increasing the number of stacks, the driver on-resistance of each path also increases. Therefore, the main goal of this work is to reduce the driver on-resistance, so that the switching becomes faster; the efficiency of the buck converter would also be higher since the conduction and switching power losses of a buck converter are dependent upon the on-resistance of switches (*S1* and *S2*) and the switching times, respectively.

2.1.4 Power Loss

The efficiency of a buck converter is negatively impacted by the non-ideality of the system components. In the following sub-sections, the major types of power losses are introduced [14]–[17].

2.1.4.1 Conduction Loss

When a transistor is in the on-condition, it conducts current; however, it is not an ideal conductor as a result of having a resistance called the on-resistance (*Ron*). The dissipated energy due to this resistance is called the conduction loss and given as follows [14]–[17]:

$$P_{cond\_S1} = I_{bc}^2 \times Ron_{pullDown} \times D \tag{2.4}$$

$$P_{cond\_S2} = I_{bc}^2 \times Ron_{pullUp} \times D_p \tag{2.5}$$

where $Ron_{pullDown}$ and Ron_{pullup} express the driver pull-down and pull-up on-resistances, respectively and P_{cond_S1} and P_{cond_S2} represent respectively the conduction losses of the switches *S1* and *S2* in Figure 2.1a.

2.1.4.2 Switching Loss

Since the switching of the driver-stacked transistors is not instantaneous, energy is dissipated during the switching time from the on- to off-condition ($\tau_{\_on}$) and vice versa ($\tau_{\_off}$). This is defined as the power-switching loss and can be expressed for a MOS transistor in accordance with [14]–[17], as follows:

$$P_{sw} = f_s \times VDS \times I_{bc} \times (\tau_{\_on} + \tau_{\_off})/2, \tag{2.6}$$

where f_s is the switching frequency (2 MHz in this work) and VDS is the drain-source voltage in the off-state of the respective transistor. For the N-stacked transistors, the switching loss is the sum of P_{sw} of each transistor; therefore, VDS can be assumed to be the amplitude of the driver output voltage $Vout$, which approaches the voltage of $VHdd$.

2.1.4.3 Gate Drive Loss

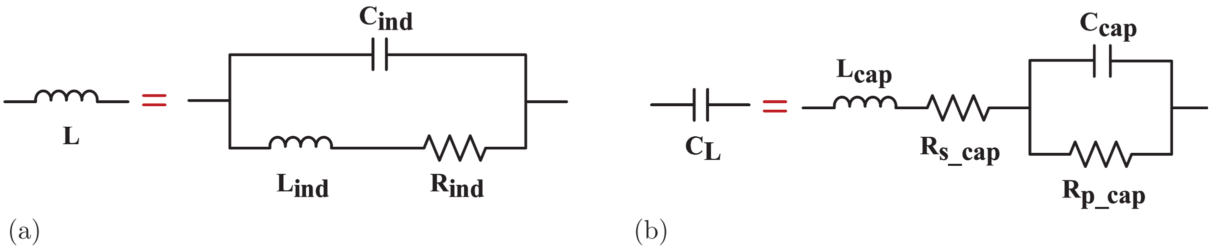
Due to the gate-resistance, the energy of charging and discharging the gate-source (C_{GS}) and the gate-drain capacitance (C_{GD}) of each stacked transistor is dissipated, which is defined as gate drive loss and expressed as follows [14]–[17]:

$$P_g = C_g \times VGS^2 \times f_s = Q_g \times VGS \times f_s, \tag{2.7}$$

where $\mathrm{C_g}$ is the total parasitic gate capacitance, VGS is the gate drive voltage and $\mathrm{f_s}$ is the switching frequency, which is set at 2 MHz in this work.

2.1.4.4 Loss due to Parasitics of Passive Components

Since the real passive circuit components do not have an ideal structure, the simulation of the designed HV-drivers switching the proposed buck converter is accomplished by using the equivalent circuits of the inductor L and the load capacitor C_L as shown in Figures 2.6a and 2.6b, respectively. The real inductor (L) contains an inductor (L_{ind}) connected in-series with a resistance (R_{ind}) and these two are in parallel with a capacitance (C_{ind}).



(a) (b)

Figure 2.6: Equivalent circuits of the buck converter's (a) inductor L and (b) capacitor C_L

The real load capacitor (C_L) consists of a capacitance (C_{cap}) being in parallel with a very high resistance (R_{p_cap}) and these two are connected in-series with an inductor (L_{cap}) and a resistance (R_{s_cap}). The parameters are set according to the appropriate data sheets, as given in Table 2.1.

Table 2.1: Parameter values of the real passive components of the proposed buck converter

L	L_{ind}	C_{ind}	R_{ind}	
	4.7 μH	3.371 pF	20.0 mΩ	
$\mathbf{C_L}$	C_{cap}	R_{p_cap}	L_{cap}	R_{s_cap}
	10 μF	10 MΩ	480 pH	2.03 mΩ

2.2 Technology Background

In this work, deep n-wells are used to isolate the nMOS transistors and also to reduce the substrate noise, which is the induced currents caused mainly by diffusion impact ionisation, capacitive and inductive coupling. The inductive parasitic effects are caused due to bond wires, the package lead frame and interconnection conductors [50]–[56].

2.2.1 Semiconductor Structure

A deep n-well (DNW) is an n+-buried layer and implemented deeper than the n-well layer as can be shown in the cross-sectional view of a DNW nMOS transistor illustrated in Figure 2.7a. The gate, drain, source, bulk, deep n-well and p-substrate terminals of the transistor are termed in this figure as **G**, **D**, **S**, **B**, **DNW** and **Psub**, respectively. The expressions *RG0*, *RD0*, *RS0*, *RB0*, *RDNW0* and *RPsub0* represent the parasitic resistances of the appropriate wire line. Each layer also contains parasitic resistance.

Because of the p-n junctions of the bulk-source, bulk-drain, bulk-DNW and also p-substrate-DNW layers, parasitic diodes *D1*, *D1'*, *D2* and *D3* occur respectively across these junctions. The diodes *D1/D1'* and *D2* form npn bipolar transistors *Q1* and *Q1'* where the bulk, source/drain and DNW serve as the base, emitter and collector, respectively. A pnp bipolar transistor (*Q2*) is formed by the diodes *D2* and *D3*, where its nodes emitter, base and collector are served by the bulk, DNW and p-substrate, respectively as can be seen in Figure 2.7b.

The DNW nMOS transistor also contains gate oxide, overlap and junction parasitic capacitances, which are termed as C_{GS}, C_{GD}, C_{GB}, C_{DS}, C_{BS}, C_{BD}, C_{DNW} and C_{Psub}. These represent the gate-to-source, gate-to-drain, gate-to-bulk, drain-to-source, bulk-to-source, bulk-to-drain, bulk-to-DNW and DNW-to-p-substrate capacitors, respectively, as shown in Figure 2.8. The drain (R_D), source (R_S) and DNW (R_{DNW}) resistances include the in-series connected resistances of the respective interconnection wire and layer diffusions. The resistances R_S and R_D also include the shallow-junction source and drain extensions [58]. The resistances between the transistor nodes bulk-source (R_{BS}), bulk-drain (R_{BD}), bulk-DNW (R_B) and Psub-DNW (R_{Psub}) additionally consist of the respective junction resistance.

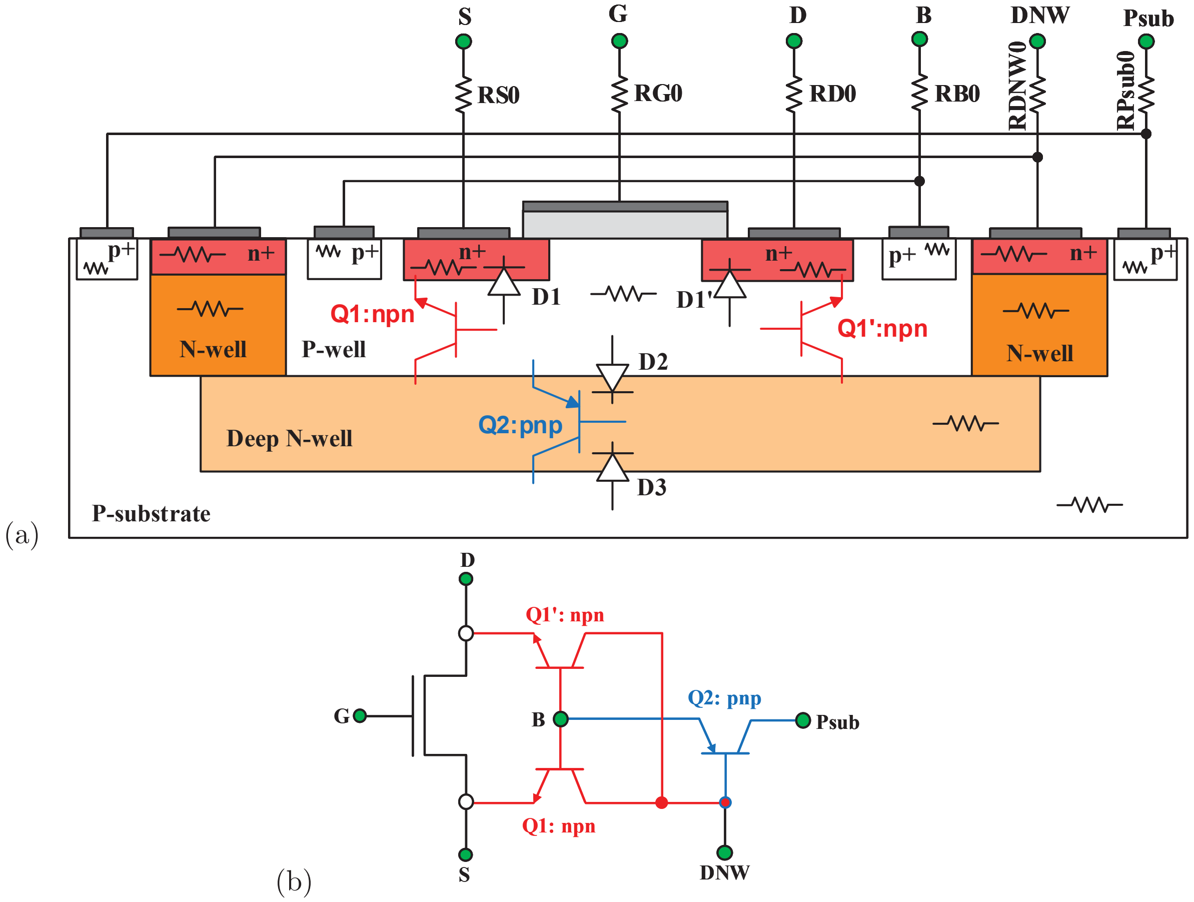


Figure 2.7: (a) Cross-sectional view of a DNW nMOS transistor, and (b) its model including parasitic bipolar transistors

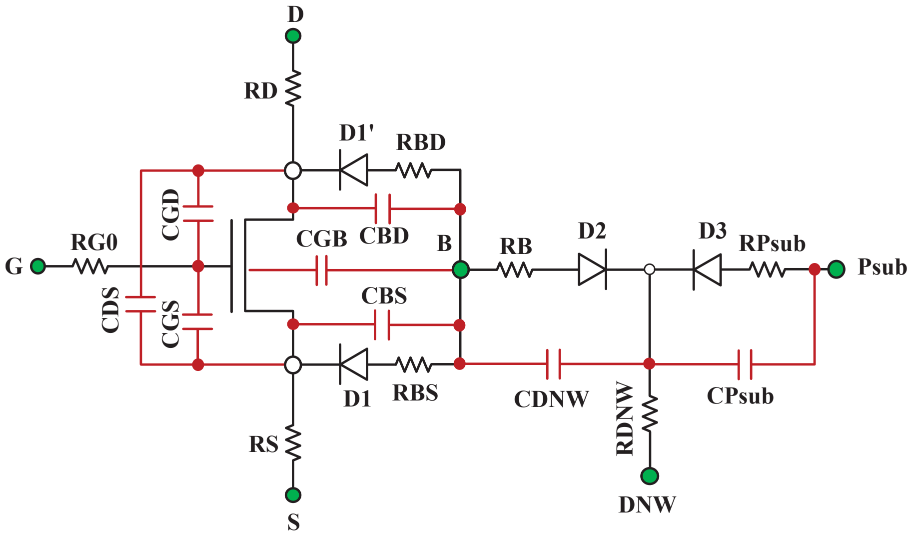


Figure 2.8: Equivalent circuit of a DNW nMOS transistor including the parasitic resistances, capacitors and diodes

2.2.2 Implementation on Chips

Since the parasitic effects of the deep n-well nMOS transistors are not well modelled, a DNW nMOS transistor used in the pull-down path of the HV-driver *3HVDv1*, is designed and implemented separately with isolated pads on chips to analyse the behaviour and parasitic effects of this device due to measurement. The number of gate fingers, length and total width of the transistor are set to be 18, 280 nm and 900 μm, respectively and are identical to the size of the DNW nMOS transistors used in the driver *3HVDv1* presented in Chapter 5.

The layout and microphotograph of the implemented DNW nMOS transistor are shown in Figures 2.9a and 2.9b, in which the standard nMOS transistor "nch_25" having 18 gate fingers is set inside the deep n-well area, viewed from the top. The transistor is surrounded by an n-well as sidewalls in terms of connecting the DNW node to the deep n-well layer.

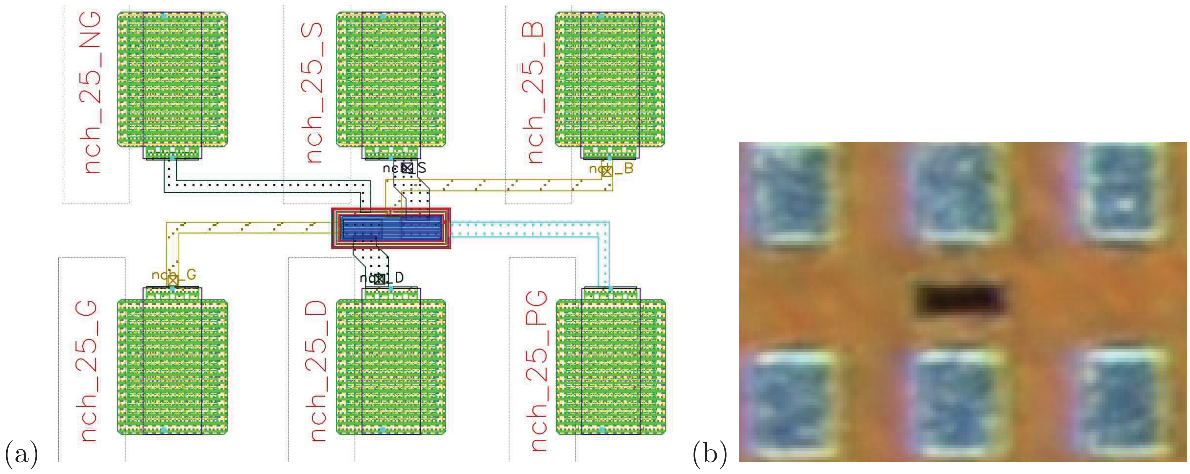


Figure 2.9: (a) Layout and (b) microphotograph of the implemented DNW nMOS transistor

Because of the number of fingers, each transistor node: source, drain and gate, contains detached layers. These are manually and respectively connected together according to the ideal layout of an RF DNW-transistor (*nmos_rf_25_6t*) being available in the same technology (65-nm TSMC). The surface of the connecting layer is set according to the current flowing through the drain/source for the maximum gate-source and drain-source voltages within the technology limit of 2.5 V. Six pads, which are termed as *nch_25_NG*, *nch_25_D*, *nch_25_S*, *nch_25_G*, *nch_25_B* and *nch_25_PG*, are connected to the deep n-well (**DNW**), drain (**D**), source (**S**), gate (**G**), bulk (**B**) and p-substrate (**Psub**) transistor's layers, respectively.

To test the DNW nMOS transistor, six chips, *A*, *B*, *C*, *D*, *E* and *F*, are stuck in three ceramic **DIL16** packages. The connection between the transistor pads and the package is achieved by aluminum bonding wires, as shown in Figure 2.10. The measurements are accomplished due to *Agilent Technologies E5270B* using the test fixture *Agilent 16442B*.

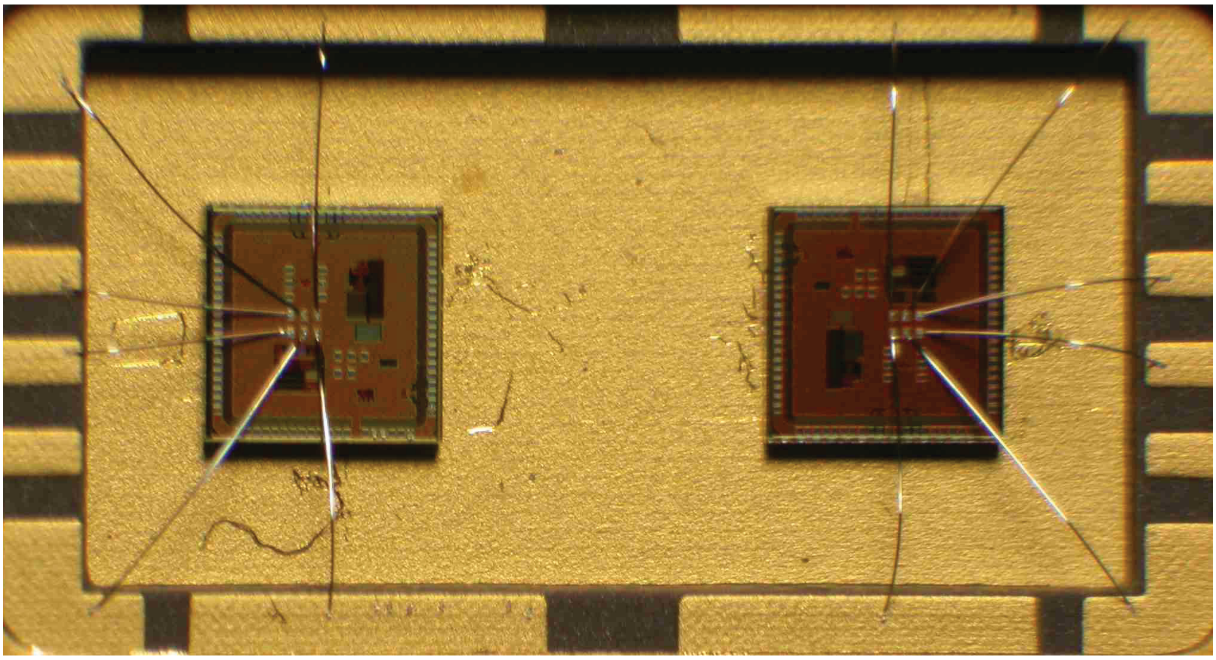


Figure 2.10: Wire bonding between two DNW nMOS transistors implemented on chips and a ceramic *DIL16* package

2.2.3 Characteristics

To analyse the behaviour and physical effects of this transistor, the following measurement procedure is conducted.

2.2.3.1 ID-VGS Characteristic

To measure the drain current characteristics with respect to the gate-source voltage, the source, bulk, and p-substrate nodes are grounded and the drain and DNW node voltages are set at 2.5 V and 5.5 V, respectively. The measured drain currents of the three DNW nMOS transistors (*B*, *E* and *F*) for the respective gate voltage varying from 0 V to 2.5 V are plotted in Figure 2.11. The results for chips *A*, *C* and *D* do not operate correctly since current flows even when the gate-source voltage is lower than their threshold voltage. The transistor structure could be unsuccessfully manufactured by a fabrication process or damaged during the wire bonding procedure.

The drain transistor currents of other chips meet the expected current characteristics

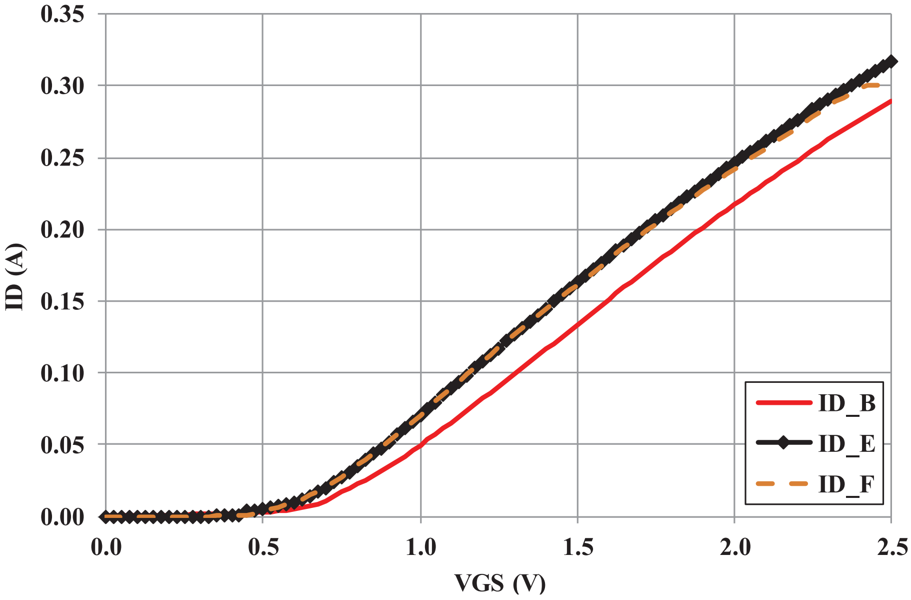


Figure 2.11: Drain current versus the gate-source voltage (*VDS*=2.5 V)

for operating the transistor in the saturation region. The currents of the transistor on chips *E* and *F* are nearly identical, although that of chip *B* is lower. As can be seen, the transistors of chips *B*, *E* and *F* start driving current (*ID*), when the gate-source voltage (*VGS*) exceeds the value of about 0.46 V, which is defined as the threshold voltage. Figure 2.12 shows the drain current characteristics of chip *F* with respect to *VGS* for different drain-source voltages of 1.0 V, 1.5 V, 2.0 V and 2.5 V. The results for *VDS* of 2.0 V and 2.5 V are identical and approach a straight line. In contrast, the characteristics for *VDS* of 1.0 V and 1.5 V show a significant deviation from the straight line being affected by mobility degradation [62].

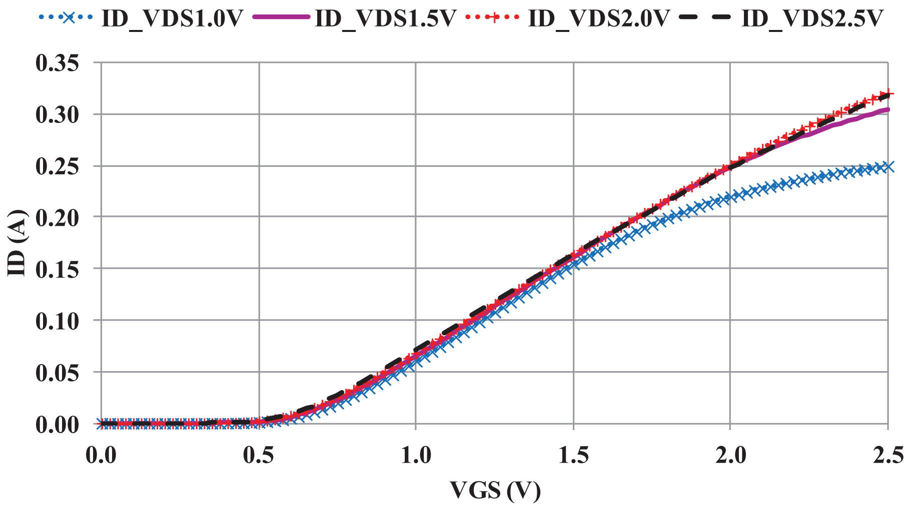
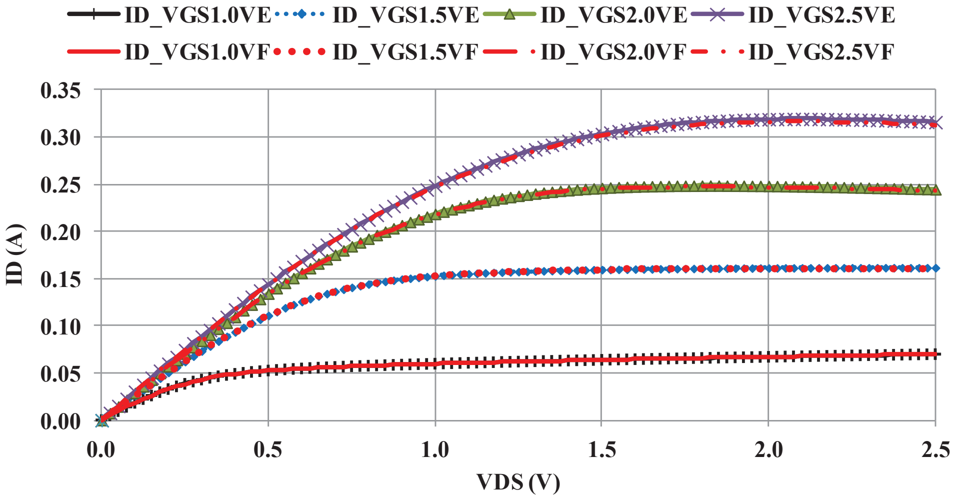


Figure 2.12: Drain current versus the gate-source voltage for different *VDS*

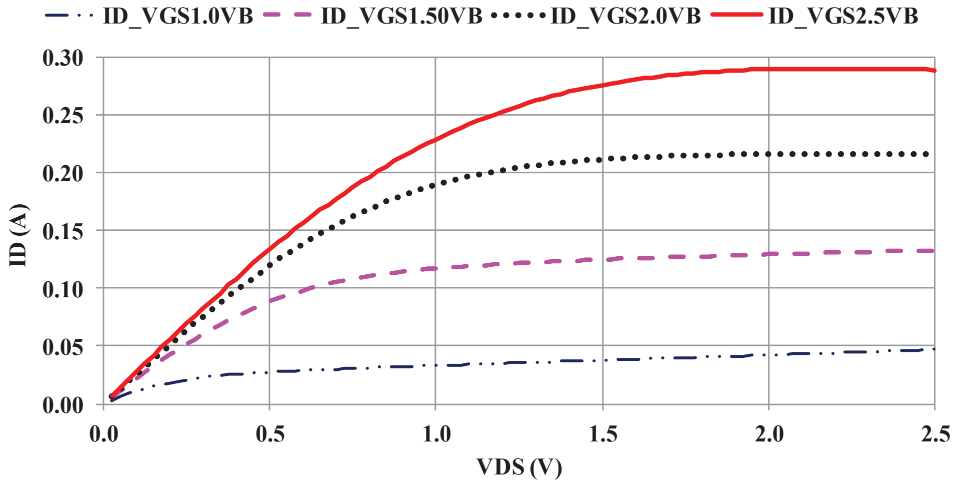
2.2.3.2 ID-VDS Characteristic

With respect to the drain-source voltage in the range from 0 V to 2.5 V, the drain currents of chips *B*, *E* and *F* are measured for different gate-source voltages (1.0 V, 1.5 V, 2.0 V and 2.5 V). The results are plotted in Figure 2.13a for chips *E* and *F* and in Figure 2.13b for chip *B*. The measurements are accomplished by setting the source, bulk, substrate voltages at 0 V and DNW voltage at 5.5 V. The drain currents of transistors *F* and *E* are very nearly equal to each other and approach constant in the saturation region, whereas those of *B* are lower and increase slightly when the drain-source voltage reaches to 2.5 V.

The increase of *ID* in the saturation region for $VGS \leq 1.5$ V is caused by at least two effects: (1) channel length modulation and (2) drain-induced barrier lowering [57]. However, it can be assumed that the current differences between transistors *B* and *E*/*F*



(a)



(b)

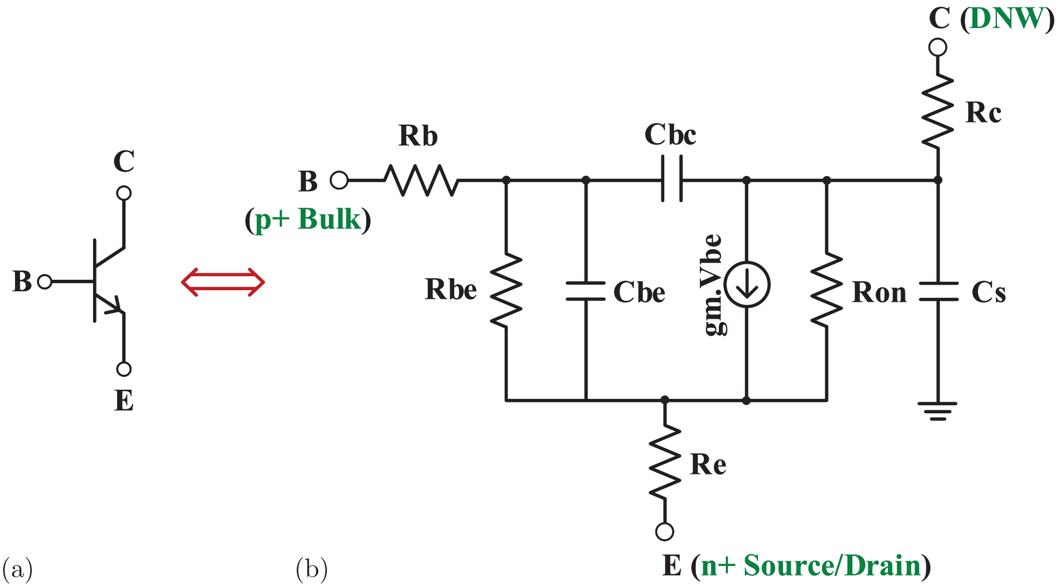
Figure 2.13: Drain current characteristics vs. the drain-source voltage for different gate-source voltages for the DNW nMOSMOSFETs (a) *E*, *F* and (b) *B*

depend on process variations during chip fabrication and/or wire bonding. Increasing temperature leads to decreasing carrier mobility [62][65]. This effect can be seen for *VGS* of 2.0 V and 2.5 V, the drain current decreases slightly when the darin-source voltage varies from 2.0 V to 2.5 V.

2.2.3.3 Parasitic NPN Bipolar Junction Transistor

The source/drain, bulk and deep n-well layers of a DNW nMOS transistor form parasitic npn bipolar transistors such as *Q1* and *Q1'* in Figures 2.7a and 2.7b, and they are referred to as emitter (***E***), base (***B***) and collector (***C***), respectively.

Figure 2.14b shows the small-signal equivalence circuit of an npn bipolar transistor represented by the symbol, as shown in Figure 2.14a. The terms R_b, R_c and R_e express the parasitic resistances of the bulk, DNW and drain/source layers, respectively. The stored-charge and depletion-layer capacitances across both the p-n (***E-B*** and ***C-B***) junctions are summed for each junction and expressed as C_{be} and C_{bc}. The capacitance C_s represents the output capacitance between the DNW (***C***) and the adjacent layer, which here is the p-substrate [57].



(a) (b)

Figure 2.14: (a) The symbol and (b) equivalent circuit of an npn bipolar transistor

To obtain the current-voltage characteristics of the bulk node, the gate, bulk and substrate voltages are set at 0 V and the voltage (V_E) of the drain and source terminals, which are tied together, is varied from –900 mV to 0 V. As a consequence, the base-emitter voltage (V_{BE}) increases from 0 V to 900 mV. In this condition, the diodes (*D1* and *D1'*) of the bulk-source and bulk-drain junctions are forward-biased and the diode *D2* of the bulk-DNW junction is reverse-biased.

The measurement results of I_{Bulk} (base current) and I_{DNW} (collector current) are accomplished for various DNW voltages: 0.0 V, 1.83 V, 3.67 V and 5.5 V, as shown respectively in Figures 2.15 and 2.16 for transistor F. When the base-emitter voltage (V_{BE}) exceeds the barrier voltage (ca. 0.75 V), the I_{Bulk} and I_{DNW} currents start increasing.

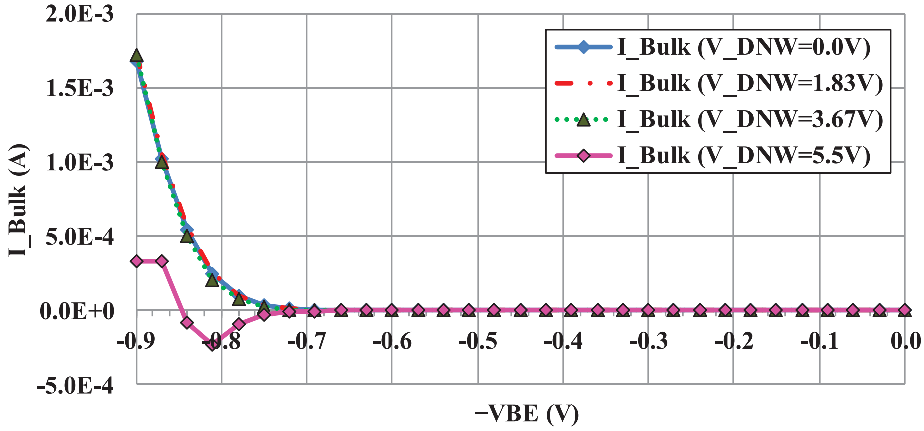


Figure 2.15: Current characteristics of the bulk node as the base of the parasitic npn BJT in transistor F for different DNW voltages vs. $-V_{BE}$

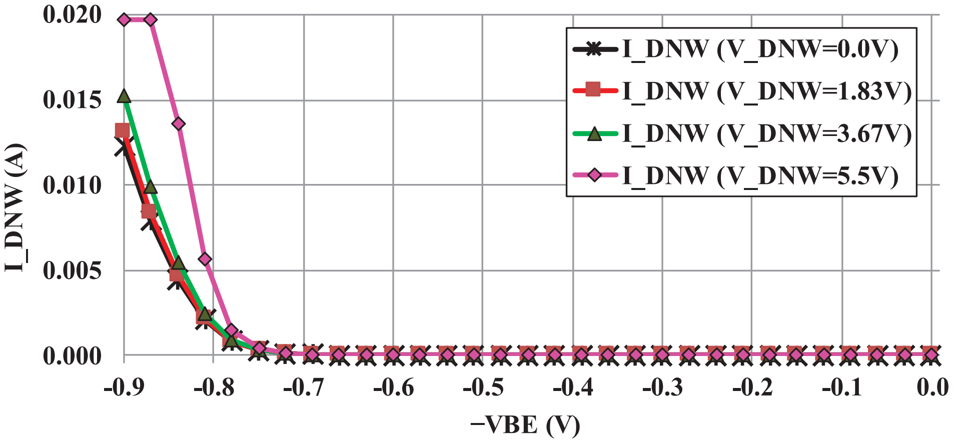


Figure 2.16: Current characteristics of the DNW node as the collector of the parasitic npn BJT in transistor F for different DNW voltages vs. $-V_{BE}$

For this measurement, the compliance limit of the collector current (I_{DNW}) is set at 20 mA; however, the result shows that at V_{BE} of 0.90 V, the current I_{DNW} is higher than 20 mA. In terms of this setting, the appropriate I_{Bulk} is also limited to 0.33 mA. Therefore, the I–V characteristic for V_{DNW} of 5.5 V is not completed.

For V_{EB} (the emitter-base voltage) between –0.85 V and –0.75 V and V_{DNW} of 5.5 V, I_{Bulk} is negative. A possible reason may be suggested that the width of the DNW layer is not broad enough to maintain the depletion zone of the bulk-DNW junction, since the DNW voltage of 5.5 V increases the electric field intensity across this junction, which could potentially break the depletion zone down and the bulk-layer injects holes in the DNW layer, so the current begins to flow. This can be observed from measured currents in the critical range of V_{EB} e.g. at –0.810 V, the collector current (I_{DNW}) of 5.601 mA is higher than the emitter current (I_E) of 5.294 mA, while the base current (I_{Bulk}) is –0.2326 mA.

In a small range of V_{EB}, between –900 mV and –870 mV, the reciprocal value of the slope in the I-V-characteristic represents the total base resistance (R_{b_tot}), which contains the in-series connected parasitic resistances of the bulk (R_b), emitter (R_e) and the np-diodes *D1* and *D1'* across the bulk-drain and bulk-source junctions (R_{be}). R_e is the resistance of in-parallel connected drain and source layers. The total base resistance (R_{b_tot}) is calculated to be 44.1 Ω for DNW of 0 V, 1.83 V and 3.67 V.

Figure 2.17 shows the emitter current (I_E) characteristics over the source/drain voltage, which is the sum of the collector (I_{DNW}) and base (I_{Bulk}) currents for the DNW voltages of 0 V, 1.83 V and 3.67 V.

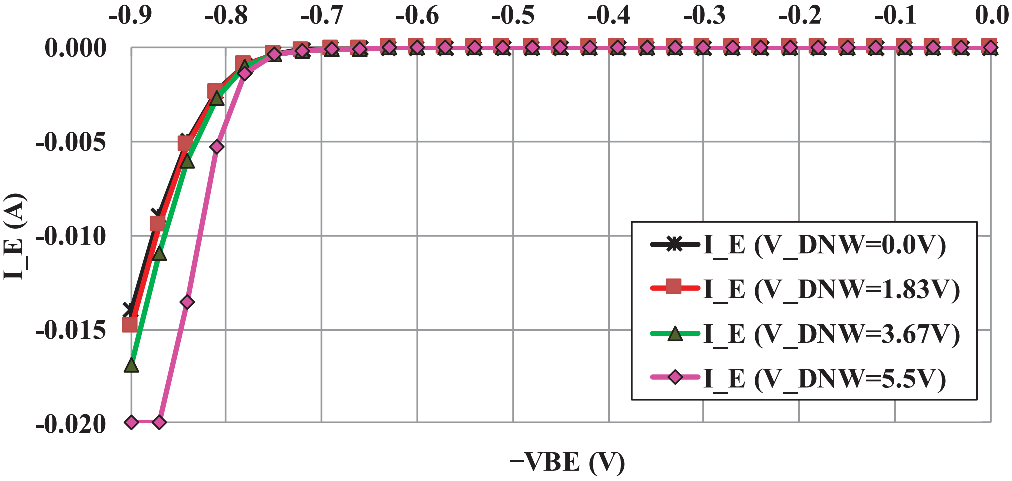


Figure 2.17: Current characteristics of the drain/source node as the emitter of the parasitic npn BJT in transistor *F* for different DNW voltages vs. $-V_{BE}$

The on-resistance (*Ron*) of the npn bipolar transistor is the ratio of ΔV_{CE} to ΔI_C ($=\Delta I_{DNW}$) and is calculated as detailed in Table 2.2, where V_{CE} and I_C express the collector-emitter voltage and the collector voltage, respectively. As can be observed, the on-resistance decreases by increasing the DNW voltage, since more current (I_{DNW}) flows through the collector (DNW) toward the emitter (drain/source) nodes.

Table 2.2: On-resistance of the parasitic npn BJT obtained from the measurement results for different DNW voltages and –900 mV$\leq V_{EB} \leq$–0.870 mV

V_{DNW} [V]	ΔV_{CE} [mV]	ΔI_{DNW} [mA]	Ron [Ω]
0.00	30	4.41	6.80
1.83	30	4.72	6.35
3.67	30	5.29	5.68
5.5	30	8.03	3.76

2.2.3.4 Parasitic PNP Bipolar Junction Transistor

The bulk, deep n-well (DNW) and p-substrate (Psub) layers form a parasitic pnp bipolar junction transistor and they are referred to as emitter (***E***), base (***B***) and collector (***C***), respectively.

To obtain the current-voltage characteristic of the DNW, the drain, source, gate and bulk voltages are set to 0.0 V and the voltage of the DNW node, which is tied to the p-substrate (collector), is decreased from 0 V to –900 mV. The result is plotted in Figure 2.18. Since the voltage difference between the base and collector (V_{BC}) of the parasitic pnp BJT is 0 V; therefore, the diode *D3* across the p-substrate and DNW junction is neglected and *D2*, the diode of the bulk-DNW junction, is forward-biased. The parasitic resistance between the emitter (bulk) node and the DNW is calculated to be about 30.7 Ω, obtained from ratio ΔV_{DNW} over ΔI_{DNW} of the I-V-characteristic in Figure 2.18.

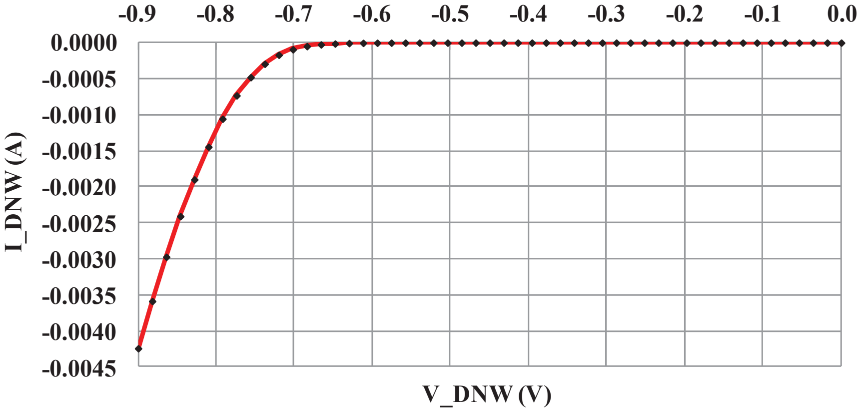


Figure 2.18: The current-voltage characteristic of the DNW-terminal

2.2.3.5 Parasitic PN (Psub-DNW) Diode

Figure 2.19 illustrates the current-voltage characteristic of the parasitic diode across the p-substrate and DNW junction by adjusting the voltage of Psub-node from 0 V to 1.0 V. The DNW, drain, source, gate and bulk voltages are set to 0 V. Therefore, the pnp bipolar transistor enters the reverse-active region, where the DNW-bulk junction is reverse-biased and the junction between DNW and the p-substrate layer is forward-biased.

Figure 2.20 shows the equivalent circuit between Psub and DNW nodes. The internal resistance R_s, which contains in-series connected parasitic resistances of DNW, Psub and the pn-junction, is 34.2 Ω, obtained from the ratio of ΔV_{Psub} to ΔI_{Psub}.

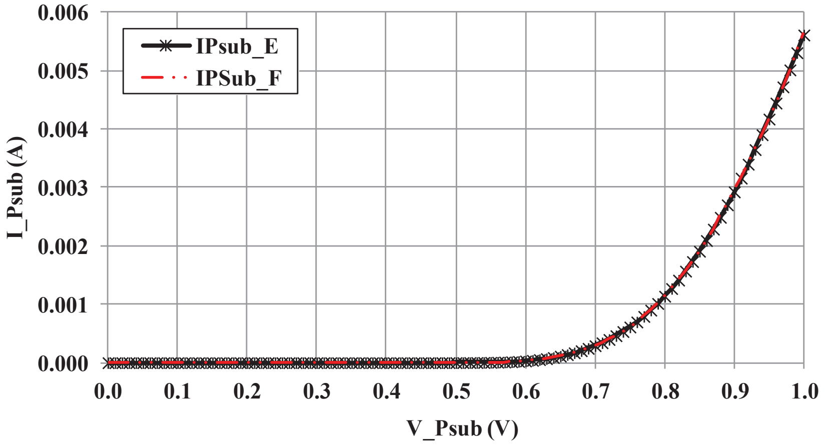


Figure 2.19: The current-voltage characteristic of the Psub-terminal

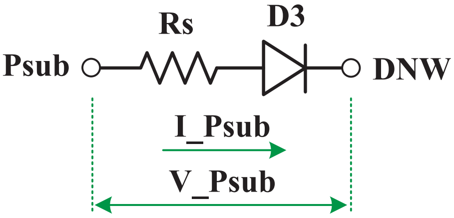


Figure 2.20: The parasitic pn-diode across the Psub and DNW junction

2.2.4 Modeling

Taking account of the measurement results, which present the behaviour and parasitic effects of the implemented DNW nMOSFET, an equal circuit model has been designed for the implemented DNW nMOS transistor. It is an extension of the basic nMOSFET model "*nch_25*" in the 65-nm TSMC technology with a nominal voltage of 2.5 V.

As illustrated in Figure 2.21, the model contains six terminals: *Gate*, *Source*, *Drain*, *Bulk*, *DNW* and *Psub*, two parasitic npn and two pnp bipolar transistors. The parasitic resistances R_{b1}/R_{b2}, R_{D1}/R_{D2} and R_{Psub} refer to the bulk, *DNW* and p-substrate layers, respectively. The base (***B***) of each npn BJT is regulated by a current-controlled current

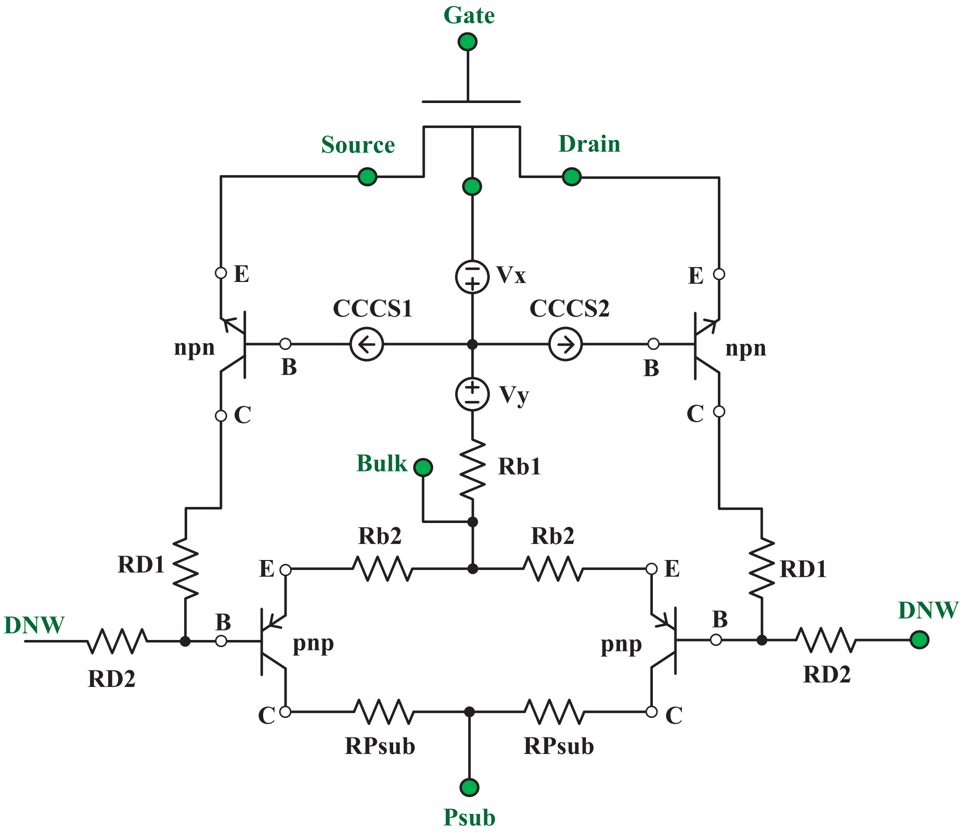


Figure 2.21: Equivalent circuit model of the implemented DNW nMOS transistor

source (*CCCS1* and *CCCS2*), which is controlled by the currents flowing through two voltage sources V_x and V_y.

Both npn bipolar transistors are assumed to be identical. Their emitter, base and collector nodes are respectively connected to the *Source*/*Drain*, parasitic resistances R_{b1} of *Bulk* and R_{D1} of *DNW*. Each of the pnp BJTs are formed by the parasitic diodes *D2* and *D3* indicated in Figure 2.7a. Both pnp BJTs are also identical. The emitter, base and collector nodes of pnp BJTs are tied to R_{b2} of *Bulk*, R_{D2} of *DNW* and R_{Psub} of *Psub*. The parameters of the designed model are obtained from the measurement and also simulation results, as given in Table 2.3.

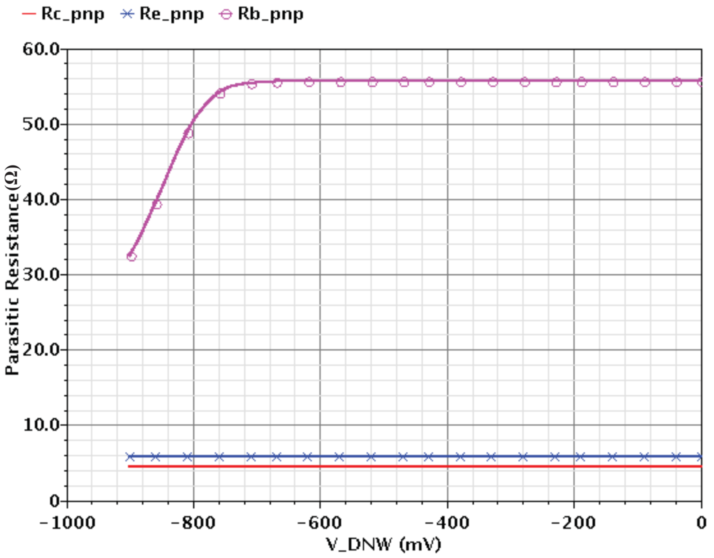
It should be noted that the bipolar transistors used in this model themselves also have parasitic resistances in accordance with the condition of the transistors. For example, the collector, base and emitter parasitic resistances, R_{c_pnp}, R_{b_pnp} and R_{e_pnp}, of one of

Table 2.3: Parameters of the parasitic components in the equivalent model (DNW nMOS)

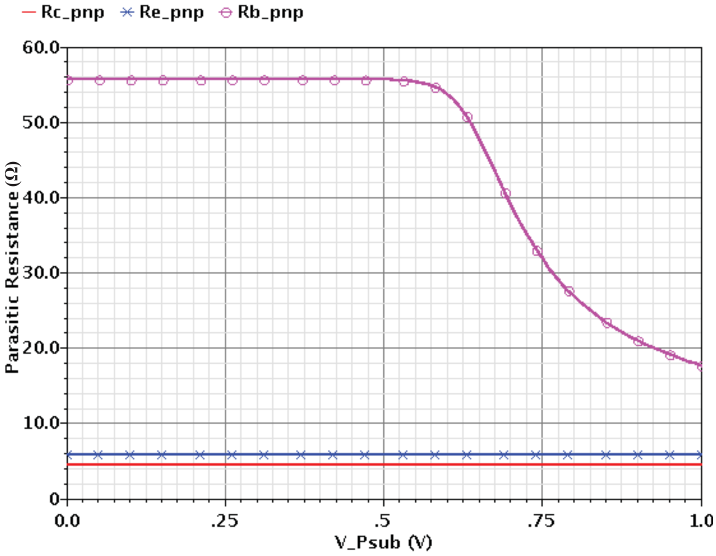
$\mathbf{R_{b1}}$	$\mathbf{R_{b2}}$	$\mathbf{R_{D1}}$	$\mathbf{R_{D2}}$	$\mathbf{R_{Psub}}$	**npn BJT**	**pnp BJT**
34.7 Ω	1 Ω	1.5 Ω	19 Ω	27.7 Ω	10 μm×10 μm /m=1	5 μm×5 μm/m=1

the pnp transistors are plotted in Figures 2.22a and 2.22b, respectively for two different conditions ***I*** and ***II***. The diagram (a) of Figure 2.22 is for the condition in which the *DNW* and p-substrate (*Psub*) nodes are connected together; the voltages of the drain (*VD*), source (*VS*) and bulk (*VB*) nodes are all set at 0 V and the DNW voltage decreases from 0 V to –900 mV, so that the bulk-DNW diode becomes forward biased.

Figure 2.22b is for the condition ***II*** where the pnp transistor is in the reverse-active mode, the voltages of the drain, source, bulk and DNW nodes are set at 0 V and the p-substrate voltage increases from 0 V to 1.0 V, so that the diode of the p-substrate/DNW junction becomes forward biased. In both modes, the total parasitic resistance of the base layer (R_{b_pnp}) varies from 55.7 Ω to 32.7 Ω and 17.7 Ω, respectively, according to the



(a)



(b)

Figure 2.22: Resistance-characteristics of the pnp bipolar transistor used in the circuit model presented in Figure 2.21 for the conditions (a) *I* and (b) *II*

voltage difference across the respective nodes. The parasitic resistances of the collector (R_{c_pnp}) and emitter (R_{e_pnp}) layers are 4.49 Ω and 5.82 Ω, respectively.

To compare the equivalent circuit presented in Figure 2.21 with the proposed DNW nMOS transistor implemented on chips, the model (Figure 2.21) is simulated according to the measurement procedures in Sections 2.2.3.3, 2.2.3.4 and 2.2.3.5. The results presented in Figures 2.23, 2.24 and 2.25 show that the ratio of $\Delta V_{Bulk}/\Delta I_{Bulk}$, $\Delta V_{DNW}/\Delta I_{DNW}$ and $\Delta V_{Psub}/\Delta I_{Psub}$ are calculated to be 44.2 Ω, 30.7 Ω and 34.2 Ω, respectively, which are equal to the measurement results.

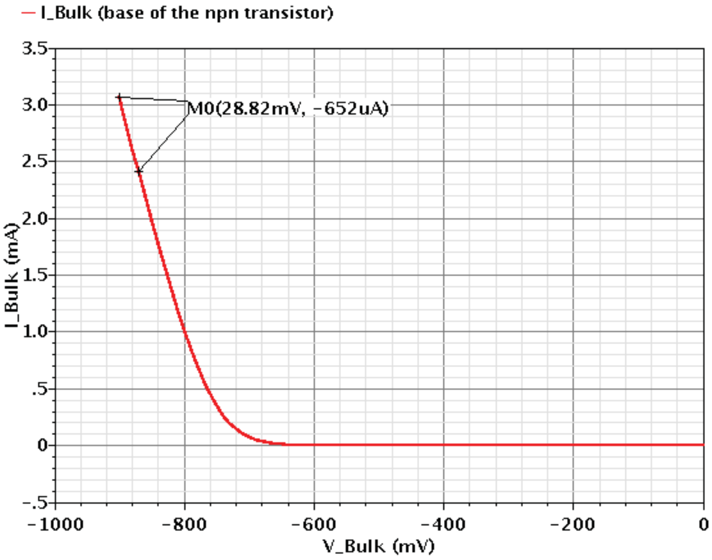


Figure 2.23: I-V characteristic of the bulk serving as a base of the parasitic npn BJT

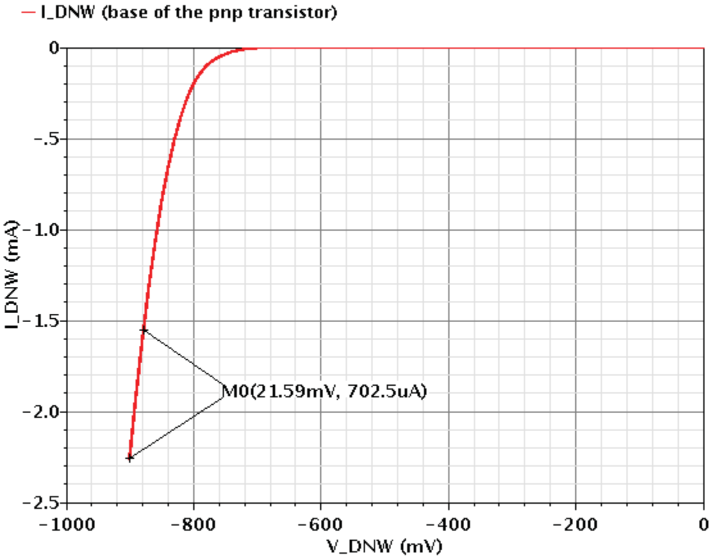


Figure 2.24: I-V characteristic of the DNW serving as a base of the parasitic pnp BJT

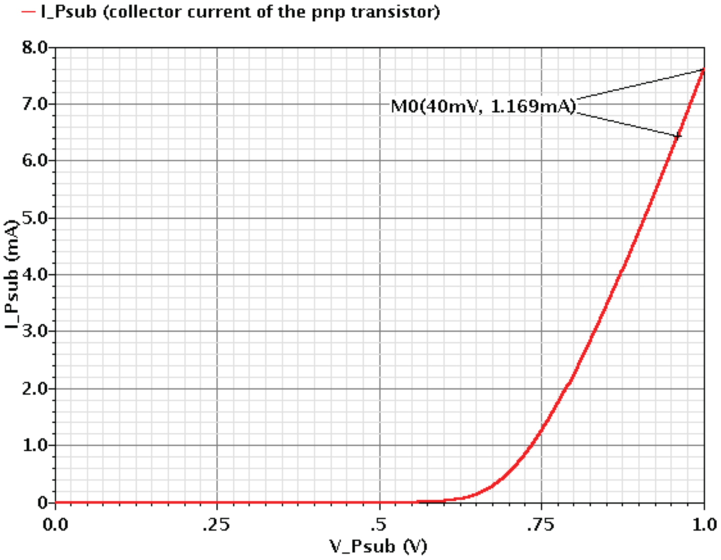


Figure 2.25: I-V characteristic of the p-substrate serving as a collector of the pnp BJT

It should be noted that this circuit model may not be inserted as a DNW nMOS transistor for the designed circuit HV-driver *3HVDv1*, which is implemented on the chip, for the following reasons:

- In the layout, the width of the DNW layer and also the surface of the drain, source and gate layers are set manually for each nMOS transistor.
- In most cases, there is more than one nMOS transistor in each stack, which are enclosed within one DNW layer.
- Also in most cases, the transistors have different widths.

All these reasons lead to the conclusion that the DNW nMOS transistors used in *3HVDv1* behave differently to the circuit model presented in Figure 2.21, since they have different parasitic resistances and bipolar transistors.

Chapter 3

Principle of Drivers Based on Stacked MOSFETs

In the previous section, a brief overview of the high-voltage drivers based on stacked CMOS transistors switching buck converters was given. In this section, the principle of design and operation of these HV-drivers are described in detail. As previously mentioned in Section (1.2), the on-resistances of the stacked transistors impact negatively upon the switching times of drivers. To reduce this problem, theories based on Level 1 model of MOSFET are presented to drive the maximum current in the driver's pull-up and pull-down paths according to the off- and on-state, considering the transistors' safe operating area, which indicates a reduced on-resistance in each path. In the inactive condition, the voltage drops across each transistor (pMOSFETs in the driver's on-state and nMOSFETs in the off-state) should be equal to each other and also within technology limits in order to avoid a negative impact on the transistors' lifetime. Regarding these theories, a circuit design methodology is introduced to control the stacked transistors in the on- and off-states.

3.1 Design Principle

High-voltage drivers are constitutive circuits in switching converters and amplifiers and are widely used in power management systems. The schematic of a high-voltage driver based on N-stacked standard CMOS transistors is given in Figure 3.1a. The driver is supplied by the high-voltage *VHdd* and has two input signals, *Vin* and *Vpin*, which switch the input CMOS transistors (Mn1 and Mp1), respectively.

It should be noted that in this work the on-state is assumed as a condition, in which the input signal *Vin* of the driver is high, and in contrast, the off-state is a condition when

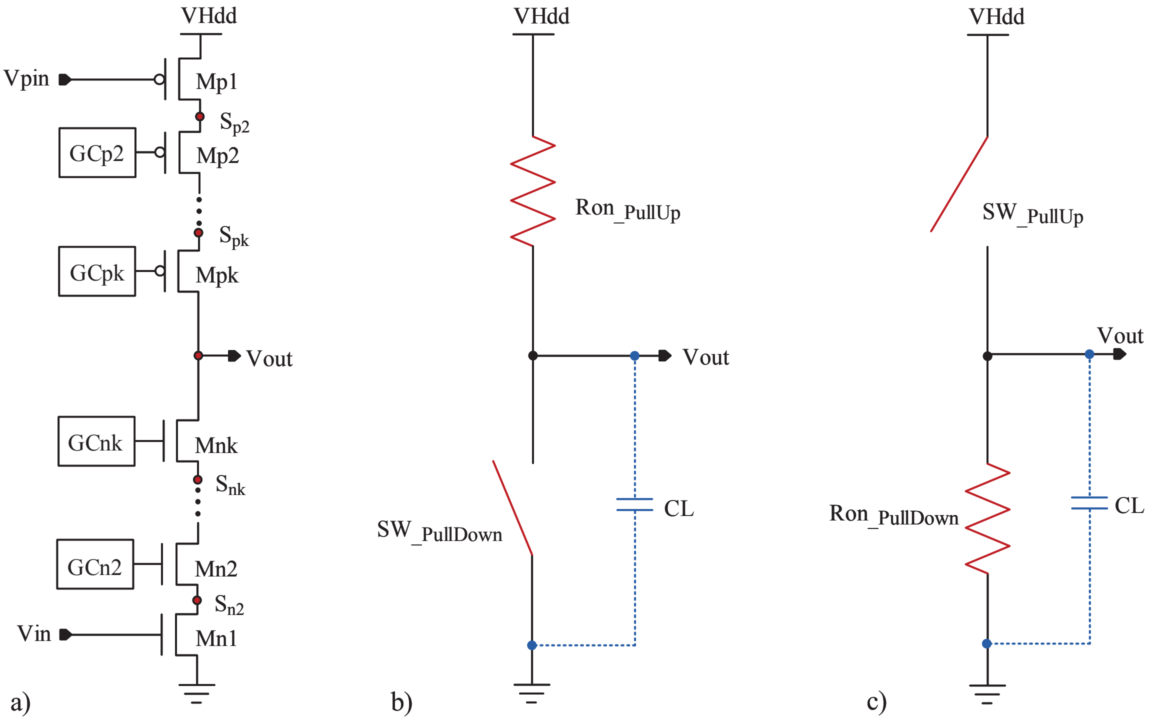


Figure 3.1: (a) High-voltage driver based on stacked CMOS transistors and the principle of its operation in the (b) off-state (pull-up active) and (c) on-state (pull-down active)

Vin is equal to 0 V. In terms of switching the system, the HV-driver consists of two parts, as shown in Figures 3.1a–c, where C_L expresses the output capacitance of the driver:

1. a pull-up network built from N-stacked pMOS transistors (Mp1–Mpk) delivers the current from the supply to the driver output load in the active condition of the pMOS transistors, in which the driver operates in the off-state with an input signal *Vin* of 0 V (Figure 3.1b), and

2. a pull-down network implemented with N-stacked nMOS transistors (Mn1–Mnk) pulls the driver output to the ground in the on-state, when *Vin* is high (Figure 3.1c).

In the active condition, each of the networks has an on-resistance (Ron_{PullUp} and $Ron_{PullDown}$) because of the involved transistors, which are not ideal conductors, when they switch on.

In order to avoid prejudicing the lifetime of the transistors, the voltage between the terminals of each transistor should be within the technology limits. For this reason, the number of stacked transistors of a high-voltage driver depends on the ratio (α_{HV}) of the supply voltage to the nominal voltage (Vn) of the standard transistors and should be at least the factor "N", which is the rounded-up integer of this ratio. The maximum supply voltage ($VHdd_{max}$) can be an N-multiple of Vn as can be seen in the following expression:

$$(N-1) < (\frac{VHdd}{Vn} = \alpha_{HV}) \leq (N = \frac{VHdd_{max}}{Vn}) \tag{3.1}$$

For example, when using 65-nm CMOS Technology with a nominal I/O voltage of 2.5 V, an HV-driver with a supply voltage between 5.0 V and 7.5 V has to be based on at least 3-stacked CMOS transistors. A maximum voltage of 7.5 V can be applied for this 3-stacked CMOS driver.

As previously mentioned, the input signal *Vin* regulates the first nMOS transistor Mn1 of the pull-down path and the level-shifted signal *Vpin* from *Vin* controls the first pMOS transistor Mp1 of the pull-up path.

In order to operate the HV-driver depending on the on- and off-state, the gate voltages of the stacked transistors also need to be regulated, and this will be explained in the next section.

3.2 Operation Principle

The input signal of the pull-down path (*Vin*) varies in the range between 0 V and *Vn*, which are the low and high levels, respectively, where *Vn* is the nominal voltage of the standard transistors used in the HV-drivers and is 2.5 V in this work. Depending on these levels, which switch the first nMOS transistor off/on, the HV-driver should also operate in the off-/on-state respectively.

The input signal of the pull-up path (*Vpin*) is generated by a level shifter, which shifts up the levels of the input signal *Vin* from *0 V/Vn* (low/high) to *“VHdd-Vn”/”VHdd”*. The difference between the high and low levels of each signal is maintained at the nominal voltage *Vn* (2.5 V).

3.2.1 On-State (Pull-Down Active)

In the on-state, when the input signal is high enough to turn the transistor Mn1 on, the node ($\mathrm{S_{n2}}$) between this transistor and the second nMOS transistor Mn2 is discharged to the ground. To activate the pull-down path, the other nMOS transistors (Mn2–Mnk) have to be turned on due to external circuits providing voltages for regulating the gate nodes of the respective transistors.

In the steady on-state, since the nodes of the pull-down should discharge to the ground, the maximum gate voltages of the nMOS transistors cannot be more than the nominal voltage *Vn* (2.5 V) in order to maintain the gate-source and the gate-drain voltages of each stacked nMOS transistor within the technology limits. As a result, the driver output can be pulled down to the ground.

In the same state, the pMOS transistors have to be turned off to prevent current flowing from the supply to the driver output load. To achieve this while also keeping the transistors within their safe operating area, the gate voltage (*Vpin*) of the first pMOS (Mp1) has to be the same as the supply voltage *VHdd* in order to turn this transistor off. The absolute value of the gate-source voltages of the other stacked pMOS transistors (Mp2–Mpk) must be equal to or less than the absolute value of their threshold voltage in order to turn off the appropriate transistors.

Since, due to the active pull-down path, the driver output voltage is discharged to the ground, the node voltages of the pull-up network in the steady on-state are determined as follows to obtain an equal drain-source voltage drop across each pMOS transistor within the technology limits:

$$VS_{pk} = \frac{(N-k+1)\times VHdd}{N} \tag{3.2}$$

$$\frac{(N-k+1)\times VHdd}{N} - |V_{THp}| \leq VG_{pk} \leq \frac{(N-k+1)\times VHdd}{N}, \tag{3.3}$$

where VS_{pk} and VG_{pk} are defined for the source and gate node voltages of the k-th N-stacked pMOS transistor as shown in Figure 3.2a.

For instance, the pull-up node voltages ($\mathrm{S_{p2}}$ and $\mathrm{S_{p3}}$) of a 3-stacked CMOS driver supplied with 7.5 V have to be 2.5 V and 5.0 V respectively. The terms $\mathrm{S_{p2}}$ and $\mathrm{S_{p3}}$ present the source nodes of Mp2 and Mp3, respectively. To achieve these node voltages, the gate voltages VG_{p1}, VG_{p2} and VG_{p3}, are required to be in the ranges of 7.04 V–7.5 V, 5.04 V–5.5 V and 2.04 V–2.5 V, respectively with a threshold voltage of 0.46 V.

3.2.2 Off-State (Pull-Up Active)

With an input signal of 0 V, the driver enters the off-state, the pull-down path is turned off and the pull-up path is active. Due to a level-shifter, the low level of the input signal *Vin* is shifted up to "*VHdd–Vn*" to turn the pMOS transistor Mp1 on. The other stacked pMOS transistors must also be on to activate the pull-up path and thus deliver current from the supply to the driver output node.

Since Mn1 is off, the node $\mathrm{S_{n2}}$ between transistors Mn1 and Mn2 can be charged until the transistor Mn2 turns off as determined by its gate voltage. The other nodes ($\mathrm{S_{n3}}$–$\mathrm{S_{nk}}$) are charged consecutively in the same procedure (Figure 3.2b).

Two major points to consider during charging the pull-down nodes are that each

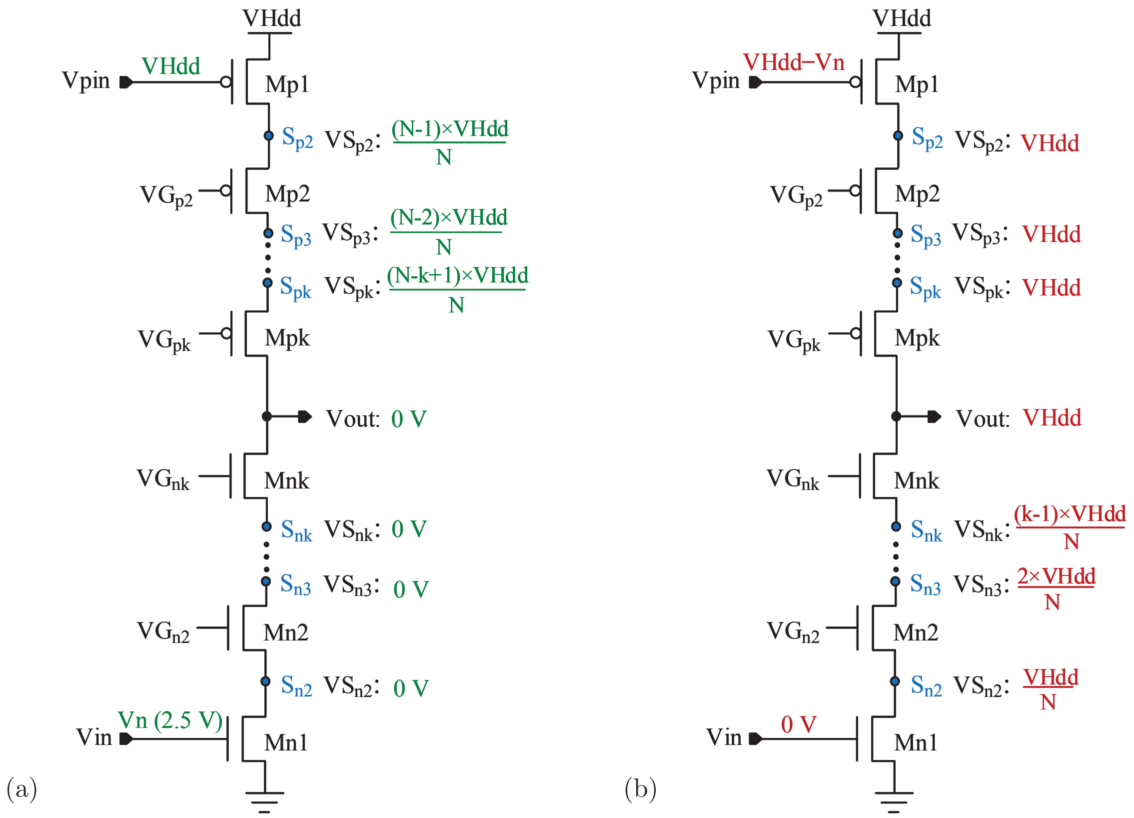


Figure 3.2: Node voltages of the pull-up and pull-down paths of an HV-driver with N-stacked CMOS in the (a) steady on-state *Vin*='high', and (b) steady off-state *Vin*='low'

transistor should be operated within the technology limits, and an equal drain-source voltage across each nMOS transistor should be obtained to avoid prejudicing the lifetime of the transistors. To achieve these points, the gate voltages of Mn2–Mnk have to be regulated in accordance with the following expression:

$$VG_{nk} \leq \frac{(k-1) \times VHdd}{N} + V_{THn} \tag{3.4}$$

Therefore, the pull-down nodes can be charged until the gate-source voltage of each transistor reaches the threshold voltage V_{THn}:

$$VS_{nk} \leq \frac{(k-1) \times VHdd}{N}, \tag{3.5}$$

where VS_{nk} and VG_{nk} are defined as the source and gate node voltages of the k-th N-stacked nMOS transistor as shown in Figure 3.2b.

Consequently, the driver output can be charged from ground to the high supply voltage *VHdd* as the pMOS transistors Mp1–Mpk are on and delivering current from the supply. Therefore, the gate-source voltages of the pMOS transistors have to be higher than the absolute value of their threshold voltage to turn the corresponding transistors on. Hence, the pull-up nodes (S_{pk}) are also charged to *VHdd*.

With respect to the technology limits and the active pull-up network, the gate voltage of the *k*-th stacked pMOS transistor should be in the following range:

$$VHdd - V_n \leq VG_{pk} < VHdd - |V_{THp}| \tag{3.6}$$

3.3 On-Resistance

The resistance of the active path of an *N*-stacked CMOS HV-driver, which is the result of the on-resistances of the involved stacked transistors, negatively impacts on the switching times of drivers and also causes conduction power loss.

When designing an HV-driver switching a buck-converter, three points are considered in the main goal of this work to reduce the on-resistance of the HV-driver:

1. Using *N*-stack CMOS-transistors, where *N* is the rounded-up integer of the ratio of the supply voltage to the nominal voltage (*VHdd/Vn*).
2. Regulating the gates of stacked transistors for driving the maximum current in the driver's pull-up and pull-down paths
3. Connecting more transistors in parallel in each stack and increasing the width of transistors

To keep the driver on-resistance as low as possible, firstly, the minimum number of stacked transistors (N) is adopted for the design of the proposed HV-driver because the more stacked transistors are used, the higher the on-resistance of the HV-driver.

In the next sub-section, the second point that needs to be considered for reducing the on-resistance of an HV-driver will be explained in detail from theory to the circuit design of gate-controlling circuits.

3.4 Gate-Controlling Circuits

Before designing circuits to regulate the gates of stacked transistors in the sense of reducing the driver on-resistance, their gate voltages are calculated to drive the maximum currents in the driver's pull-down and pull-up paths. This calculation is based on the level 1 MOSFET model and is performed using the computer algebra system "**MAXIMA**". Therefore, the discussion of this issue is described in two stages: theory and circuit design.

3.4.1 Theory

It should be considered that if the on-resistance of the pull-down and pull-up networks is at a minimum, then the maximum current can flow in the corresponding path. Therefore, the gate voltage of each transistor has been calculated to control the transistors in order to allow this. For the 65-nm process technology with a nominal I/O voltage of 2.5 V, as used in this work, the calculation of the node voltages of stacked transistors is accomplished for on- and off-states and in each case, two different groups of supply voltages are considered:

1. when the supply voltage is a multiple of the nominal voltage:
   $VHdd = N \times Vn$

2. otherwise, when the supply voltage is not divisible by the nominal voltage and is in the range between "$(N–1) \times Vn$" and "$N \times Vn$", which can be expressed as:
   $(N–1) \times Vn < VHdd < N \times Vn$.

3.4.1.1 On-State (Pull-Down Active)

In this state, the input signal is high, and is assumed to be equal to *Vn* (2.5 V). The gates of other stacked transistors are calculated to drive the maximum current in the pull-down path, whereas the driver output node discharges from *VHdd* to the ground.

For the first step of the calculation, the supply voltage of the HV-driver is assumed to be divisible by the nominal voltage, which will be presented in the next section.

3.4.1.1.1 Supply Voltage is a Multiple of Vn

For an HV-driver supplied with a voltage *VHdd*, which is *N* times greater than the nominal voltage ($N \times Vn$), the node voltages of each stacked transistor is calculated for driving the maximum current using drain current equations for cutoff, linear and saturation conditions. These calculations have been performed for 2-, 3- and 4-stacked CMOS HV-drivers.

The calculation results for a 2-stacked CMOS HV-driver with a supply voltage of 5.0 V are shown in Figure 3.3a. The driver output *Vout* is discharged from 5.0 V to the ground, whereas the pull-down node S_{n1} (source node of the nMOS transistor Mn2) is also discharged but from 2.5 V to 0 V. The gate voltage VG_{n2} of this transistor has an offset of 2.5 V to the respective source voltage. The relationship between the gate (VG_{n2}), source (VS_{n2}) voltages of Mn2 and the driver output voltage (*Vout*) can be mathematically expressed by the following equations:

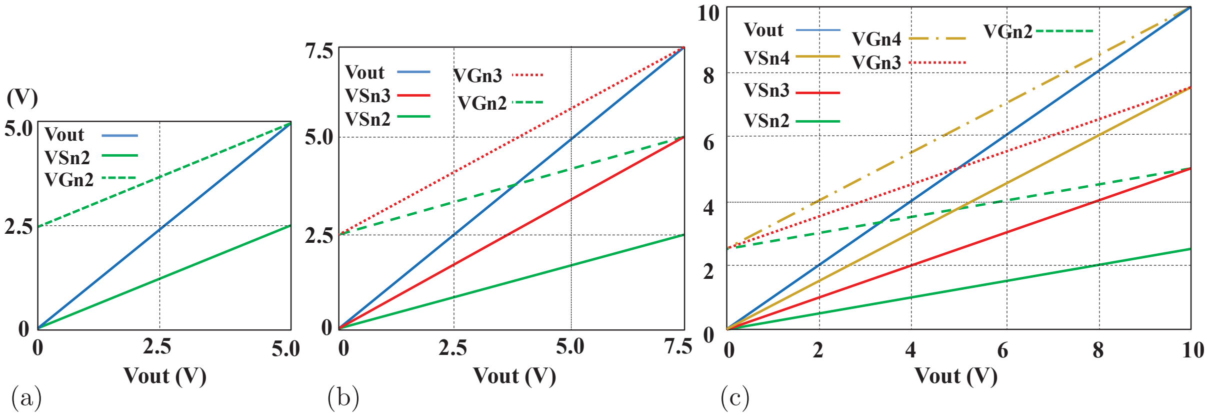


Figure 3.3: Node voltage characteristics of a (a) 2- (b) 3- (c) 4-NMOS driver for a maximum drain current (in the on-state using the level 1 MOSFET model)

$$VS_{n2} = \frac{Vout}{2} \tag{3.7a}$$

$$VG_{n2} = \frac{Vout}{2} + 2.5\,V \tag{3.7b}$$

Figure 3.3b shows the node voltage characteristics of the 2nd and 3rd nMOS transistors of a 3-stacked CMOS driver with a supply voltage of 7.5 V. The pull-down node voltages VS_{n2}, VS_{n3} and *Vout* are discharged respectively from 2.5 V, 5.0 V and 7.5 V to the ground. The gate voltages VG_{n2} and VG_{n3} of Mn2 and Mn3 have an offset of 2.5 V to the corresponding source voltages. These node voltages can be determined according to the following expression:

$$\mathrm{VS}_{n2} = \frac{Vout}{3} \quad (3.8a) \qquad \mathrm{VG}_{n2} = \frac{Vout}{3} + 2.5\,V \quad (3.8b)$$

$$\mathrm{VS}_{n3} = \frac{2\times Vout}{3} \quad (3.8c) \qquad \mathrm{VG}_{n3} = \frac{2\times Vout}{3} + 2.5\,V \quad (3.8d)$$

The gate voltages of a 4-stacked nMOS driver with a supply voltage of 10.0 V are also calculated for driving the maximum current, whereas the voltages of the pull-down nodes VS_{n2}, VS_{n3}, VS_{n4} and *Vout* are discharged respectively from 2.5 V, 5.0 V, 7.5 V and 10 V to the ground. Figure 3.3c depicts the node voltages characteristics of the 4-stacked nMOS driver, which can be mathematically expressed as follows:

$$\mathrm{VS}_{n2} = \frac{Vout}{4} \quad (3.9a) \qquad \mathrm{VG}_{n2} = \frac{Vout}{4} + 2.5\,V \quad (3.9b)$$

$$\mathrm{VS}_{n3} = \frac{2\times Vout}{4} \quad (3.9c) \qquad \mathrm{VG}_{n3} = \frac{2\times Vout}{4} + 2.5\,V \quad (3.9d)$$

$$\mathrm{VS}_{n4} = \frac{3\times Vout}{4} \quad (3.9e) \qquad \mathrm{VG}_{n4} = \frac{3\times Vout}{4} + 2.5\,V \quad (3.9f)$$

In the same procedures, the gate and source voltages of the N-stacked nMOS for maximum pull-down current can be defined by Equations (3.10) and (3.11), respectively:

$$VS_{nk} = \frac{(k-1) \times Vout}{N} \tag{3.10}$$

$$VG_{nk} = \frac{(k-1) \times Vout}{N} + 2.5\,V \tag{3.11}$$

The calculated results for the maximum current indicate that the gate voltage of each N-stacked nMOS transistor is a straight line with an offset of Vn (2.5 V) to the corresponding source voltage, when the appropriate nMOS transistor operates in the triode region. However, for operation in the saturation region, the gate voltage has plurality values, which build a parallelogrammatic region such as area ***B*** in Figure 3.4. Point ***A*** indicates the boundary between the triode and the saturation regions, which will be determined in the following step. In accordance with the theory of the simple model describing the characteristics of the nMOS transistors, it has been assumed that the operating condition in the triode (linear) region occurs when the drain-source voltage is less than the value of the difference between the corresponding gate-source and the threshold voltages. This can be expressed for a k-th stacked nMOS transistor as follows:

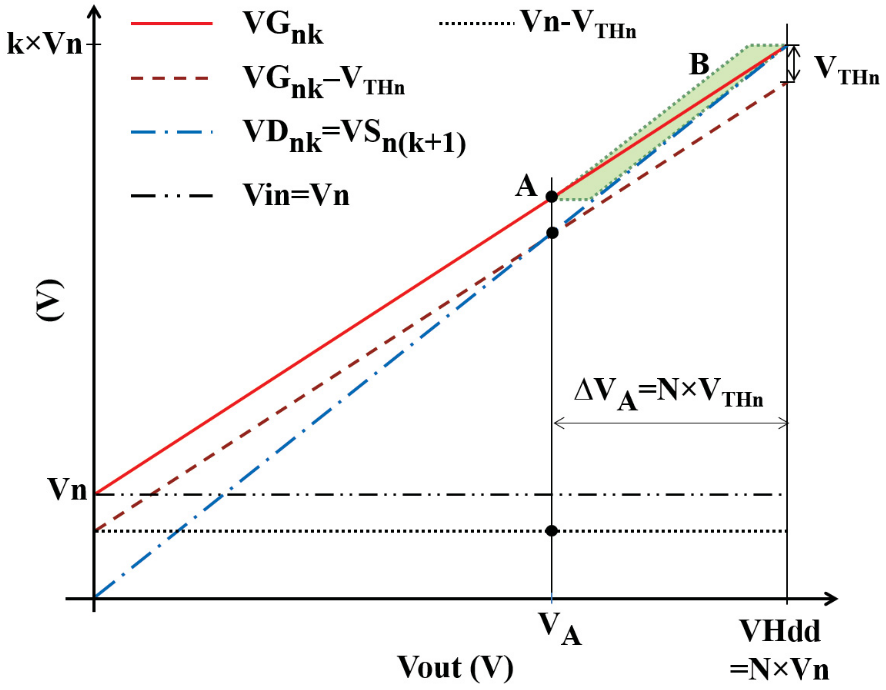


Figure 3.4: Gate and source voltage of the k-th nMOS driver (in the on-state)

$$(VGS_{nk} - V_{THn}) > (VD_{nk} - VS_{nk}) \tag{3.12a}$$

Since VD_{nk} is equal to $VS_{n(k+1)}$, the expression can be written in the following form:

$$(VG_{nk} - VS_{nk} - V_{THn}) > (VS_{n(k+1)} - VS_{nk}), \tag{3.12b}$$

and simplified to:

$$(VG_{nk} - V_{THn}) > VS_{n(k+1)} \tag{3.13}$$

This relation expresses the condition of the triode operating for the maximum drain current up to the boundary point ***A*** and it can be defined according to Equations (3.10) and (3.11) as:

$$\frac{(k-1) \times Vout}{N} + 2.5\,V - V_{THn} > \frac{k \times Vout}{N} \tag{3.14}$$

From these, the output voltage $\boldsymbol{V_A}$ at the boundary point ***A*** in Figure 3.4 can be obtained as follows:

$$\overset{Vout=V_A}{\rightarrow} V_A = N \times (2.5\,V - V_{THn}) \tag{3.15}$$

Region ***B*** helps to simplify circuit design generating gate voltages VG_{nk} because the required voltage does not need to track exactly the red line according to Equation (3.11) shown in Figure 3.4 in the saturation region.

3.4.1.1.2 Verification of Theory

Regarding the drain current equations in the triode and saturation regions [61]–[64], the relationship between node voltages of stacked transistors, as expressed in Equations (3.10) and (3.11), will be proved in the following hereinafter.

The drain current of the k-th stacked nMOS transistor (Mn2–Mnk) for triode operation can be defined as:

$$\begin{aligned} ID_{tr} =& \beta \times \Big[(VG_{nk} - VS_{nk} - V_{THn}) \times (VS_{n(k+1)} - VS_{nk}) \\ &- \frac{(VS_{n(k+1)} - VS_{nk})^2}{2}\Big] \end{aligned} \tag{3.16}$$

where β is the transconductance parameter and given as: $\beta = \mu_0 C_{ox}(W/L)$. The terms

C_{ox}, W and L express the gate-oxide capacitance, width and length of the respective transistor respectively.

This current of the driver is regulated by the input signal *Vin*, which controls the gate of the first transistor Mn1 that drives the same current:

$$ID_{tr} = \beta \times \left[(Vin - V_{THn}) \times VS_{n2} - \frac{VS_{n2}^2}{2} \right] \text{ with } VS_{n2} = \frac{Vout}{N} \tag{3.17}$$

In both terms, two major points have to be considered: the terms of (3.16) are affected by similar terms of the drain current of Mn1 (3.17) and are identical to them as well. The second point is, in order to avoid a negative impact on the lifetime of transistors, not only must the voltage between each transistor remain within the technology limits, but also the voltage drops across each stacked transistor must be equal to each other.

Regarding the above points, the gate-source and drain-source voltages from the current Equations (3.16) and (3.17) can be expressed as:

$$VG_{nk} - VS_{nk} = Vin = 2.5\,V \tag{3.18}$$

$$VS_{n(k+1)} - VS_{nk} = VS_{n2} = \frac{Vout}{N} \tag{3.19}$$

Equation (3.19) indicates that the voltage drop across each transistor is equal to *Vout/N*. From this, the source voltage of each transistor can be obtained as:

$VS_{nk} = \frac{(k-1) \times Vout}{N}$,

which is identical to the calculated source voltage in (3.10).

Inserting the above equation for the source voltage of the k-th stacked nMOS transistor into (3.18) yields the respective gate voltage as follows, which is equal to Equation (3.11):

$VG_{nk} = \frac{(k-1) \times Vout}{N} + 2.5\,V$

The following Equations (3.20) and (3.21) define the saturation drain currents driven by Mn1 and the other transistors Mnk respectively:

$$ID_{satMn1} = \frac{\beta}{2} \times (Vin - V_{THn})^2 = \frac{\beta}{2} \times (2.5\,V - V_{THn})^2 \tag{3.20}$$

$$ID_{satMnk} = \frac{\beta}{2} \times (VG_{nk} - VS_{nk} - V_{THn})^2 \tag{3.21}$$

The drain current ID_{satMn1} of the transistor Mn1 is the same drain current ID_{satMnk} as for the other stacked nMOS transistors (Mn2–Mnk). Therefore, the terms of (3.20) are identical to (3.21), which confirms the offset of 2.5 V between the gate and source voltages.

The operation condition of nMOS transistors for the saturation region can be obtained from the expression (3.13) as:

$$(VG_{nk} - V_{THn}) \leq VS_{n(k+1)} \tag{3.22}$$

From this condition and the expression of VG_{nk} defined in (3.21), it is possible to determine several gate voltages. These results build a parallelogrammatic region ***B*** in Figure 3.4. For example, the standard, upper and lower values of the gate voltages VG_{n2} and VG_{n3} of a HV-driver based on 3-stacked CMOS transistors with a nominal I/O voltage of 2.5 V, are given in Table 3.1 to drive the maximum current at the output voltage of 6.5 V. The driver is supplied with 7.5 V. The respective source voltages have an offset of 2.5 V to the appropriate gate voltage, as indicated in this table. It should be noted that the threshold voltage V_{THn} of the nMOSFETs is assumed to be 0.5 V. The boundary between the linear and saturated operations is at Vout of 6.0 V.

Table 3.1: Gate and source voltages of the 2nd and 3rd nMOSFETs of a 3-stacked CMOS driver operating in the saturation region, which are involved in forming the parallelogrammatic area shown in Figure 3.4 (V_{THn}=0.46 V).

Position	VG_{n2} [V]	VS_{n2} [V]	VG_{n3} [V]	VS_{n3} [V]
lower limit	4.5	2.0	6.5	4.0
standard value	4.667	2.167	6.833	4.333
upper limit	4.833	2.333	7.167	4.667

In the next step, the node voltages of N-stacked nMOS transistors of HV-drivers will be calculated for the second type of supply voltages.

3.4.1.1.3 Supply Voltage is not Divisible by Vn

In this section, the supply voltage is assumed to be a value that is not divisible by the nominal voltage. First, we look on the pull-down path. The calculation results of the node voltages of 3-stacked nMOS transistors driving the maximum drain current are demonstrated in Figure 3.5. The HV-driver operates with a supply voltage of 5.5 V.

During the discharge of the driver output node from the 5.5 V to V_I, the gate voltages VG_{nk} remain constant. The expression V_I is defined as the output voltage at the intersection point between the *Vout*–axis and the vertical line ***I*** as depicted in Figure 3.5, which is here 4.5 V. During the discharge of Vout from V_I to the ground, the gate and source volt-

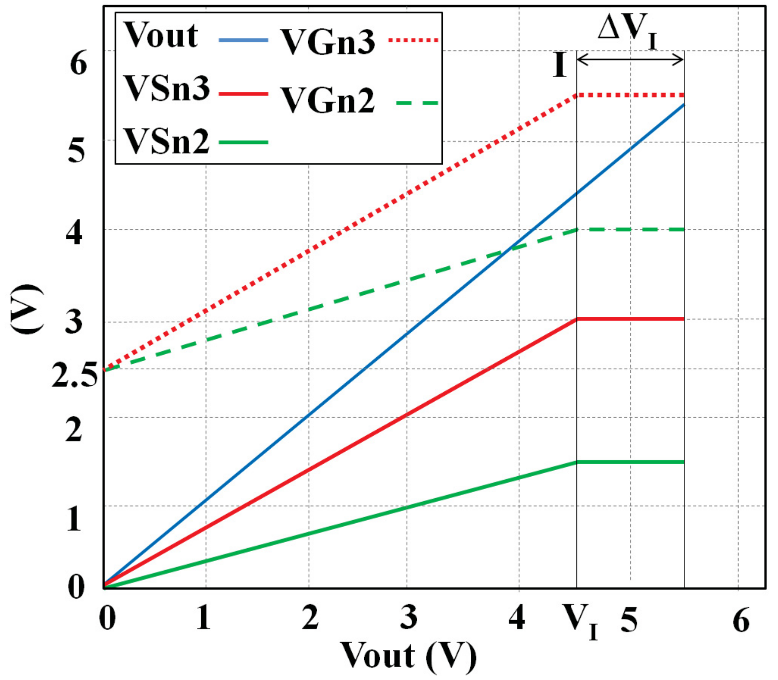


Figure 3.5: Node Voltages of a 3-stacked nMOS driver in the on-condition with a supply voltage *VHdd* of 5.5 V

ages of the 2nd and 3rd nMOS transistors follow the theory according to Equations (3.10) and (3.11).

Table 3.2 gives the calculated gate voltages of the *k*-th stacked nMOS transistor of a 2-, 3- and 4-stacked nMOS driver for driving the maximum current, while the output node discharges from *VHdd* to V_I. The HV-driver is supplied with a high voltage, which is not divisible by the nominal voltage *Vn*. It should be noted, that the numerical algorithm for the 4-stacked nMOS driver has an inaccuracy of ± 0.05 V.

Table 3.2: Gate voltages of a 2, 3 and 4-stacked driver for various values of *VHdd* in the on-state [V] (based on the level 1 MOSFET model)

2-stacked driver		**3-stacked driver**			**4-stacked driver**			
VHdd	VG_{n2}	*VHdd*	VG_{n2}	VG_{n3}	*VHdd*	VG_{n2}	VG_{n3}	VG_{n4}
5.0	5.0	7.5	5.0	7.5	10.0	5.0	7.5	10.0
4.5	4.5	7.0	4.75	7.0	9.5	4.75	7.125	9.5
4.0	4.0	6.5	4.5	6.5	9.0	4.5	6.75	9.0
3.5	3.5	6.0	4.25	6.0	8.5	4.25	6.375	8.5
3.0	3.0	5.5	4.0	5.5	8.0	4.0	6.0	8.0

In the same procedures of these calculation results, the following expression can be obtained for the gate voltages of the *k*-th *N*-stacked nMOS transistors (Mn2–Mnk) for driving the maximum current with a supply voltage between "(*N–1*)× *Vn*" and "*N*× *Vn*":

$$VG_{nk} = VHdd - [(N-k) \times (Vn - \Delta V_I)] \quad \text{for} \quad Vout > V_I \tag{3.23}$$

$$VG_{nk} = \frac{(k-1) \times Vout}{N} + 2.5\,V \qquad \text{for} \quad Vout \leq V_I \tag{3.24}$$

The voltage V_I can be determined as follows:

$$V_I = VHdd - \Delta V_I\ , \tag{3.25}$$

where ΔV_I, the difference between the supply voltage *VHdd* and V_I, is given in Table 3.3 for different supply voltages and numbers of stacked nMOS transistors.

As can be seen, by increasing the number of stacked nMOS transistors, ΔV_I decreases. With regard to the parallelogrammatic area in Figure 3.4, the gate voltages follow the rule (3.11) for a higher N-stacked nMOS.

Table 3.3: ΔV_I of drivers' pull-down path based on 2-, 3- and 4-stacked nMOS transistors for various supply voltages

2-stacked driver		**3-stacked driver**		**4-stacked driver**	
VHdd [V]	ΔV_I *[V]*	*VHdd [V]*	ΔV_I *[V]*	*VHdd [V]*	ΔV_I *[V]*
5.0	0.0	7.5	0.00	10.0	0.000
4.5	0.5	7.0	0.25	9.5	0.125
4.0	1.0	6.5	0.50	9.0	0.250
3.5	1.5	6.0	0.75	8.5	0.375
3.0	2.0	5.5	1.00	8.0	0.500

During discharge of the driver output node due to the active pull-down path, the pMOS transistors Mp1–Mpk have to be off to avoid current flow from the supply to the output node. This can be achieved by regulating the pMOS transistors. Therefore, the signal *Vpin*, which is shifted up from the input signal *Vin* and regulates the first pMOS transistor Mp1, has to be *VHdd* to turn off this transistor.

As previously mentioned, in order to avoid a negative impact on the transistors' lifetime, the voltage drop across each pMOS transistor has to be equal to each other and also within technology limits. Hence, by discharging the output node from *VHdd* to the ground, the voltage drop across each pMOS has to be one N-th of the supply voltage *VHdd*. The voltage drop can be expressed as the following equation for the source-drain voltage VSD_{pk} of each pMOS transistor:

$$VSD_{pk} = \frac{VHdd}{N} \tag{3.26}$$

Therefore, the source node of the k-th stacked pMOS transistor has to be discharged from *VHdd* to the following value:

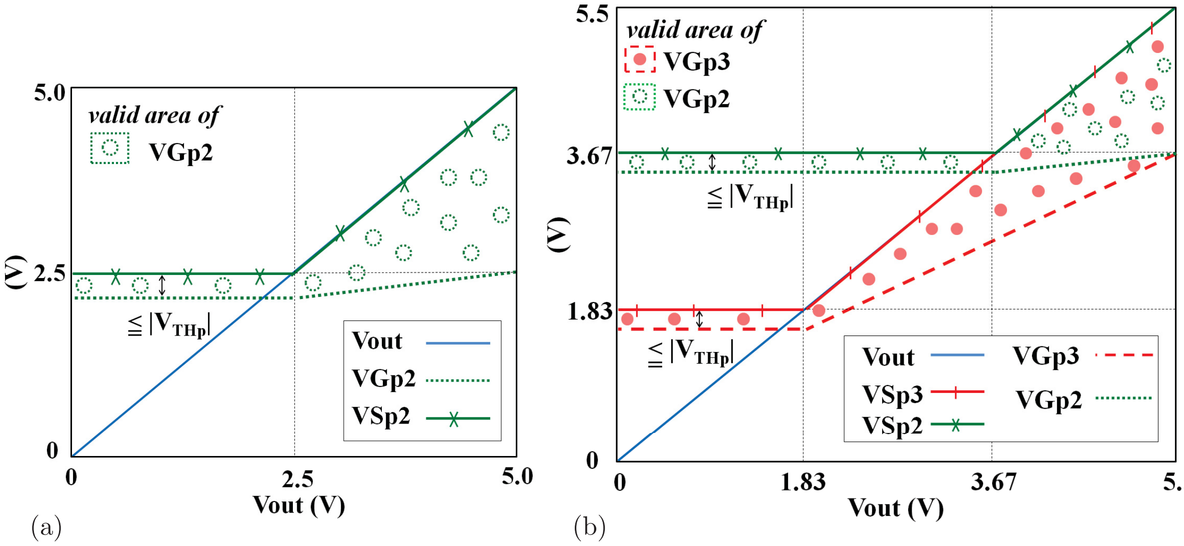
$$VS_{pk} = \frac{(N-k+1)\times VHdd}{N} \quad \text{for} \quad 0 \leq Vout \leq \frac{(N-k+1)\times VHdd}{N} \tag{3.27}$$

This can be achieved by using the appropriate gate voltage, which turns the corresponding transistor off at the required source voltage. Otherwise, the source voltage tracks the output voltage while the respective pMOS transistor is still on:

$$VS_{pk} = Vout \tag{3.28}$$

In the driver on-state, the node voltages of the second pMOS transistor Mp2 of a 2-stacked CMOS driver with a supply voltage of 5.0 V are depicted in Figure 3.6a. By discharging the output node from 5.0 V to the ground, the source voltage of Mp2 is discharged from 5.0 V to half of *VHdd* (2.5 V). To achieve this, the transistor Mp2 has to be turned off at an output voltages of 2.5 V.

Figure 3.6b shows the node voltages of the second and third pMOS transistors Mp2 and Mp3 of a 3-stacked CMOS driver with a supply voltage of 5.5 V. By discharging the output node from *VHdd* to the ground, the source voltages of Mp2 and Mp3 are discharged from *VHdd* to two-thirds (3.67 V) and one-third (1.83 V) of *VHdd*. To achieve these, the transistors Mp2 and Mp3 have to be turned off at output voltages of $2 \times VHdd/3$ (3.67 V) and *VHdd*/3 (1.83 V) respectively.



(a) (b)

Figure 3.6: Node Voltages of (a) 2-stacked pMOS driver supplied with 5.0 V, and (b) 3-stacked pMOS driver supplied with 5.5 V in the driver on-state

3.4.1.2 Off-State (Pull-Up Active)

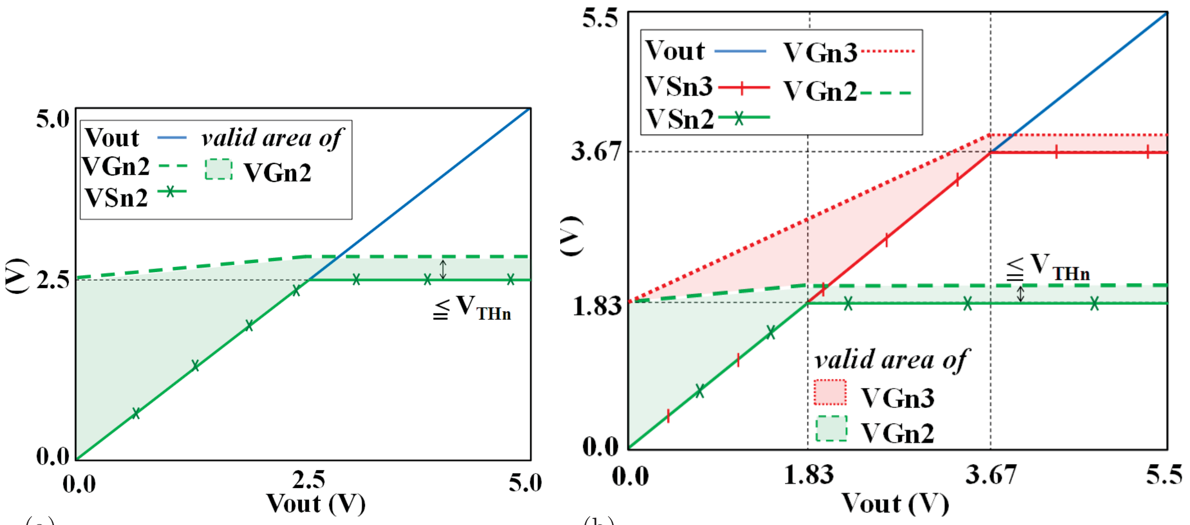
In the off-state, the input signal of 0 V turns the nMOS transistor Mn1 off. In terms of charging the driver output node to *VHdd* while considering the safe operating region of the transistors, the gate voltages of the other stacked nMOS transistors Mn2–Mnk have to turn off the corresponding transistors on time, when their source voltages reach the following values:

$$VS_{nk} = \frac{(k-1) \times VHdd}{N} \quad \text{for} \quad \frac{(k-1) \times VHdd}{N} \leq Vout \leq VHdd \tag{3.29}$$

These values can be achieved when the gate-source voltage of each transistor is equal to or less than the threshold voltage of the nMOS transistors. As a consequence, the driver output node can be charged to *VHdd*, as shown in Figures 3.7a and 3.7b for pull-down node voltages of a 2- and a 3-stacked CMOS driver with a supply voltages of 5.0 V and 5.5 V, respectively.

In the case that the supply voltage of a 3-stacked CMOS HV-driver is 7.5 V, which is divisible by the nominal voltage, the maximum current can flow in the pull-up path of this driver when the level-shifted signal *Vpin* is 5.0 V and the gate voltages of the 2nd- and 3rd-stacked pMOS transistor track the following expressions, which are derived from the calculation results in Figure 3.8:

$$\mathrm{VG}_{p2} = \tfrac{Vout}{3} + 2.5\,V \quad (3.30a) \qquad \mathrm{VG}_{p3} = \tfrac{2 \times Vout}{3} \quad (3.30b)$$



(a) (b)

Figure 3.7: Node voltages of (a) a 2-stacked nMOS with *VHdd* of 5.0 V, and (b) a 3-stacked nMOS driver with *VHdd* of 5.5 V in the off-condition

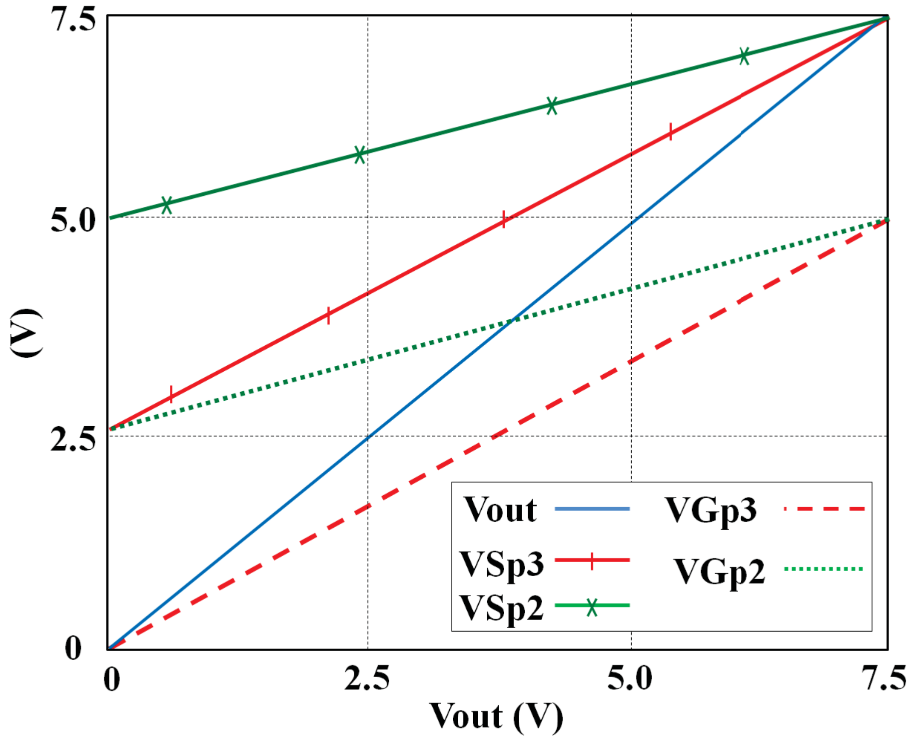


Figure 3.8: The node voltages of a 3-stacked pMOS driver in the off-condition ($VHdd$=7.5 V)

According to these calculations, the source voltages of Mp2 and Mp3 have an offset of 2.5 V to the appropriate gate voltages and can be expressed by the following formulae:

$$\mathrm{VS}_{p2} = \tfrac{Vout}{3} + 5.0\,V \quad (3.31a) \qquad \mathrm{VS}_{p3} = \tfrac{2\times Vout}{3} + 2.5\,V \quad (3.31b)$$

From these and the calculation results of a 2- and 4-stacked CMOS driver, the source and gate voltages (VS_{pk} and VG_{pk}) of the k-the pMOS transistor of an N-stacked HV-driver for driving the maximum pull-up current can be obtained as in the following equations:

$$VS_{pk} = \frac{(k-1)\times Vout}{N} + (N+1-k)\times 2.5\,V \tag{3.32}$$

$$VG_{pk} = \frac{(k-1)\times Vout}{N} + (N-k)\times 2.5\,V \tag{3.33}$$

For a supply voltage indivisible by Vn (2.5 V), the gate and source voltages of the k-th N-stacked pMOS transistors (Mp2–Mpk) for driving the maximum current can be expressed from the calculation results presented in Table 3.4 as follows:

Table 3.4: Gate voltages of a 2 and 3-stacked CMOS driver for various *VHdd* in the off-state

2-stacked driver			
VHdd [V]	V_{Ip} *[V]*	VG_{p2} *[V]*	
		$Vout \leq V_{Ip}$	$Vout=V_{Ip}$
3.0	2.0	0	0.5
4.0	1.0	0	1.5

3-stacked driver					
VHdd [V]	V_{Ip} *[V]*	$Vout \leq V_{Ip}$		$Vout=V_{Ip}$	
		VG_{p2} *[V]*	VG_{p3} *[V]*	VG_{p2} *[V]*	VG_{p3} *[V]*
5.5	1.0	1.5	0	3.0	3.0
6.5	0.5	2.0	0	4.0	4.0

$$VG_{pk} = (N-k) \times (Vn - \Delta V_I) \quad \text{for} \quad 0 \leq Vout \leq V_{Ip} \tag{3.34}$$

$$\begin{aligned} VG_{pk} = &\frac{(VHdd - Vn) - (N-k) \times (Vn - \Delta V_I)}{(VHdd - \Delta V_I)} \times (Vout - \Delta V_I) \\ &+ (N-k) \times (Vn - \Delta V_I) \\ &\qquad\qquad\qquad\qquad \text{for} \quad V_{Ip} \leq Vout \leq VHdd \end{aligned} \tag{3.35}$$

where ΔV_I, the difference between the supply voltage 0 V and V_{Ip}, can be obtained in Table 3.3 and the term V_{Ip} is equal to ΔV_I.

In the next section, a circuit design methodology to generate the desired gate voltages will be described.

3.4.2 Circuit Design

In the previous section, theories to calculate the gate voltages of an N-stacked CMOS driver were introduced for driving the maximum drain current in the active path and also for switching off the transistors in the inactive path depending on whether the driver pull-up or pull-down network has to be inactive. In the course of these calculations, various supply voltages were considered. In this sub-section, according to the calculated gate voltages, the designs of circuits $\mathrm{GC_{n2}}$ and $\mathrm{GC_{n3}}$, which provide the required gate voltages of the 2nd- and 3rd-stacked nMOS transistors respectively, are described. With regard to these, a circuit design methodology generating the gate voltages of the k-th stacked nMOS and pMOS transistor are also presented. It should be noted that the bulk and source nodes of each transistor are tied together.

3.4.2.1 Gate-Controlling Circuit GC_{n2}

The circuit design of GC_{n2}, the sub-block shown in Figure 3.9a, is illustrated in Figure 3.9b. The term GC_{n2} is defined as the **G**ate-**C**ontrolling Circuit providing VG_{n2}, the gate voltage of the 2nd-stacked nMOS transistor Mn2. The circuit is built up of three in-series connected pMOS transistors: mp_{21}, mp_{22} and mp_{23}. The transistors mp_{22} and mp_{23} have the same size, while the dimensions of mp_{21} keep the transistor mp_{22} in the saturation region for the on-condition.

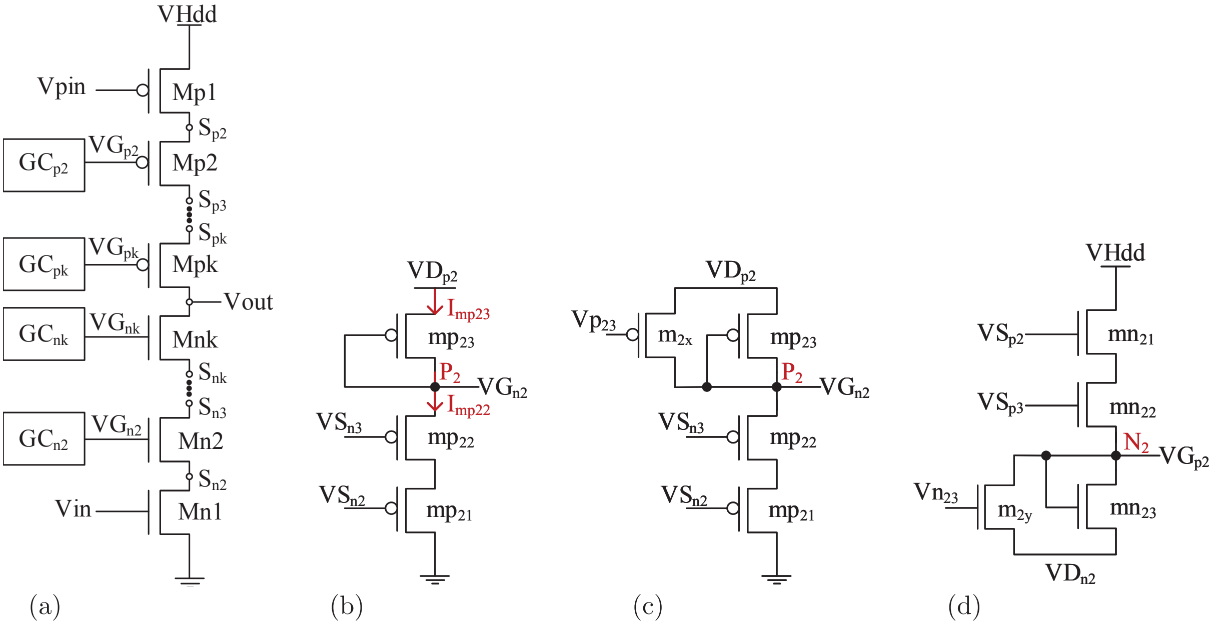


Figure 3.9: (a) HV-driver based on N-stacked CMOS, and circuit design of the gate-controlling circuits (b) GC_{n2}, (c) with an extra transistor, and (d) GC_{p2}

The circuit is supplied by VD_{p2}. Depending on the on- and off-states of the driver, VD_{p2} switches between two values "$VHdd\text{-}(N\text{-}2)\times(Vn\text{-}\Delta V_I)$" and "$(VHdd/N)+\alpha_n$", where α_n is between 0 V and the threshold voltage (V_{THn}) of the stacked nMOS transistors and the value of ΔV_I can be obtained from Table 3.3 for different drivers and supply voltages. For example, for a 3-stacked nMOS driver, VD_{p2} switches between 5.0 V and "2.5 V+α_n" for a supply voltage of 7.5 V and between 4.0 V and "1.83 V+α_n" for $VHdd$ of 5.5 V.

The nodes of the driver pull-down path, S_{n2} and S_{n3}, control the gates of mp_{21} and mp_{22}, whereas the drain and gate terminals of mp_{23} are connected together. The node ***P2*** between mp_{22} and mp_{23} provides the required gate voltage VG_{n2}, which will be further described below.

In the on-state, the input signal is 2.5 V and the driver pull-down path is active. The currents I_{mp22} and I_{mp23} of the transistors mp_{22} and mp_{23} respectively can be expressed as in the following equations for operating in the saturation area:

$$I_{mp23} = \frac{\beta_p}{2} \times (VD_{P2} - V_{P_2} - |V_{THp}|)^2 \tag{3.36}$$

$$I_{mp22} = \frac{\beta_p}{2} \times (V_{P2} - VS_{n3} - |V_{THp}|)^2, \tag{3.37}$$

where V_{P2} is the voltage of the node ***P2*** representing the source and gate voltages of the transistors mp$_{22}$ and mp$_{23}$ respectively.

If the HV-driver is based on 2-stacked transistors, the gate voltage of mp$_{22}$ is set to the output voltage *Vout* instead of VS_{n3}. Since the currents in Equations (3.36) and (3.37) are both flowing in the same wire, they are identical to each other and therefore, the voltage V_{P2} can be solved as:

$$V_{P2} = \frac{VS_{n3}}{2} + \frac{VD_{p2}}{2}\ , \tag{3.38}$$

where the source voltage of the 3rd-stacked nMOS transistor can be deduced from Equation (3.10) as follows:

$$VS_{n3} = \frac{2 \times Vout}{N} \tag{3.39}$$

As a result, the provided gate voltage in Equation (3.38) can be represented by:

$$V_{P2} = \frac{Vout}{N} + \frac{VD_{p2}}{2}\ , \tag{3.40}$$

which is equal to the desired gate voltage VG_{n2} as calculated in Equation (3.10).

It has to be taken into account that the current I_{mp23} can flow when the absolute value of the gate-source voltage of mp$_{23}$ exceeds its absolute value of the threshold voltage. This limits the required voltage VG_{n2} to "($Vout/N$+2.5 V)–$|V_{THp}|$" at the beginning of the process of discharging the output load. In order to avoid this problem, a pMOS transistor such as m$_{2x}$ in Figure 3.9c, which is regulated by the reference voltage Vp_{23}, is connected in parallel to mp$_{23}$. On the other side, the parallelogram-shaped region ***B*** in Figure 3.4 helps to simplify the problem, since the desired voltage VG_{n2} does not need to follow exactly the line of Equation (3.11), when the transistor Mn2 operates in the saturation region. Due to the extra transistor m$_{2x}$, the provided gate voltage VG_{n2} can be nearly constant as indicated in Equation (3.23) for supply voltages, which are indivisible by the nominal voltage *Vn*.

In the off-state, the input signal *Vin* is 0 V, VD_{p2} is switched from "($k \times Vn$)–ΔV_I" to

"($VHdd/N$)+α_n". As previously mentioned, the term α_n is between 0 V and the threshold voltage (V_{THn}) of the stacked nMOS transistors.

Meanwhile, the node ***P2*** charges to "($Vout/N$)+α_n", which turns the transistor Mn2 off when the driver node S_{n2} is charged to $Vout/N$. As an example, S_{n2} of a 2-stacked CMOS driver with a supply voltage of 5.0 V charges to 2.5 V. Consequently, the other driver pull-down nodes (S_{n3}, ..., S_{nk}) can be further charged over $Vout/N$.

The circuit GC_{p2}, gate-controlling circuit providing the gate voltage of the 2nd pMOS transistor Mp2, is the complementary form of GC_{n2}, as indicated in Figure 3.9d. The circuit chains the upper and lower supply rails, whose potentials are set to *Vout* and VD_{n2}, respectively. Depending on the on- and off-state of the driver, VD_{n2} switches between "(N–1)×$Vout/N$–α_p" and "(N–2)×(Vn–ΔV_I)", where α_p is between 0 V and the absolute value of the threshold voltage (V_{THp}) of the stacked pMOS transistors. The value of ΔV_I can be obtained from Table 3.3.

3.4.2.2 Gate-Controlling Circuit GC_{n3}

Figure 3.10a depicts the gate-controlling circuit GC_{n3}, which generates the gate voltage VG_{n3} of the third driver nMOS transistor. The circuit consists of five in-series connected pMOS transistors, mp_{31}–mp_{35}. Whereas the gates of mp_{31}, mp_{32} and mp_{33} are fed by the pull-down nodes S_{n2}, S_{n3} and S_{n4}, respectively, and the gate nodes of mp_{34} and mp_{35} are tied to their corresponding drain terminals. In the case of a 3-stacked CMOS driver, mp_{33} is connected to the driver output, which is represented as the node S_{n4}.

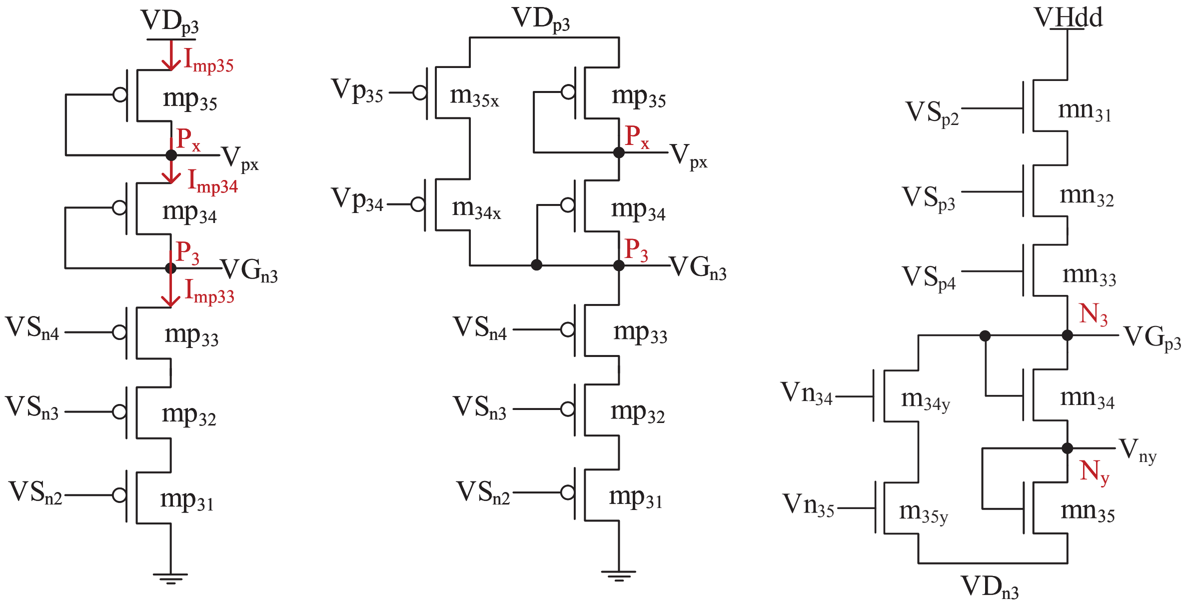
The circuit is supplied by VD_{p3}, which is switched between "$VHdd$–(N–3)×(Vn–ΔV_I)" and "(2×$VHdd/N$)+2×α_n" depending on the on- and off-state of the driver. For a 3-stacked CMOS driver with a supply voltage of 7.5 V, VD_{p3} switches between 7.5 V and "5.0 V+2×α_n". The dimensions of mp_{31} and mp_{32} should keep the transistor mp_{33} operating in the saturation area. The node ***P3*** between mp_{33} and mp_{34} provides the required gate voltage VG_{n3}, as will be proved in hereafter.

In the on-state, the saturation currents I_{mp33}, I_{mp34} and I_{mp35} of the transistors mp_{33}, mp_{34} and mp_{35} respectively can be written according to the following equations:

$$I_{mp33} = \frac{\beta_p}{2} \times (V_{P3} - VS_{n4} - |V_{THp}|)^2 \tag{3.41}$$

$$I_{mp34} = \frac{\beta_p}{2} \times (V_{Px} - V_{p3} - |V_{THp}|)^2 \tag{3.42}$$

$$I_{mp35} = \frac{\beta_p}{2} \times (VD_{p3} - V_{px} - |V_{THp}|)^2 \tag{3.43}$$



(a) (b) (c)

Figure 3.10: Circuit design of gate-controlling circuits (a) GC$_{n3}$, (b) with extra transistors and (c) GC$_{p3}$

where V_{Px} is the the voltage of the node ***Px*** representing the source and gate voltages of the transistors mp$_{24}$ and mp$_{35}$ respectively.

From Equations (3.41) and (3.42), the voltage of the node ***P3***, and from Equations (3.42) and (3.43) the voltage of the node ***Px*** are solved as:

$$V_{P3} = \frac{VS_{n4}}{2} + \frac{V_{Px}}{2} \tag{3.44}$$

$$V_{Px} = \frac{VD_{p3}}{2} + \frac{V_{P3}}{2} \tag{3.45}$$

From these, the provided voltage at the node ***P3*** can be calculated as follows:

$$V_{P3} = \frac{2 \times VS_{n4}}{3} + \frac{VD_{p3}}{3}\ , \tag{3.46}$$

where the source voltage of the 4th-stacked nMOS transistor can be set using the Equation (3.10):

$$VS_{n4} = \frac{3 \times Vout}{N} \tag{3.47}$$

The provided voltage V_{p3} can be deduced by substituting Equation (3.47) into Equation (3.46) to obtain:

$$V_{P3} = \frac{2 \times Vout}{N} + \frac{VD_{p3}}{3} \ , \tag{3.48}$$

which is equal to the desired gate voltage VG_{n3} as calculated in Equation (3.11) for supply voltages being divisible by the nominal voltage.

The current in the circuit $\mathrm{GC_{n3}}$ can only flow when the gate-source voltage of each transistor exceeds its threshold voltage. This problem limits the required voltage VG_{n3} and can be prevented in the same way as mentioned previously for the circuit design of $\mathrm{GC_{n2}}$, by adding two in-series connected pMOS transistors, such as $\mathrm{m_{34x}}$ and $\mathrm{m_{35x}}$ in Figures 3.10b, in parallel to $\mathrm{mp_{34}}$ and $\mathrm{mp_{35}}$. The reference voltages Vp_{34} and Vp_{35} regulate both transistors, respectively. In the off-state, the input signal *Vin* is 0 V, VD_{p3} is switched from "$VHdd–(N–3)\times(Vn–\Delta V_I)$" to "$(2\times VHdd/N)+2\times\alpha_n$".

During charging of the pull-down nodes in the off-state, the node ***P3*** charges to about "$(2\times VHdd/N)+2\times\alpha_n$". When the driver node voltage VS_{n3} reaches "$2\times VHdd/N$", the provided gate voltage VG_{n3} at the node ***P3*** turns the transistor Mn3 off. For example, for a 3-stacked CMOS driver, $\mathrm{S_{n3}}$ charges to 5.0 V and 3.67 V with a supply voltage of 7.5 V and 5.5 V respectively.

The circuit $\mathrm{GC_{p3}}$, which provides the gate voltage of the third pMOS transistor Mp3, is the complementary form of $\mathrm{GC_{n3}}$, as indicated in Figure 3.10c. The circuit connects the upper and the lower supply rails, whose potentials are set to *VHdd* and VD_{n3}, respectively. The voltage VD_{n3} switches between "$(N–2)\times VHdd/N\text{-}2\times\alpha_p$" and "$(N–3)\times(Vn–\Delta V_I)$" according to the on- and off-state of the driver,.

3.4.2.3 Gate-Controlling Circuit $\mathrm{GC_{nk}}$

With the same procedure, the gate-controlling circuit $\mathrm{GC_{nk}}$ of a *k*-th nMOS transistor of an *N*-stacked CMOS driver consists of two groups of pMOS transistors, as illustrated in Figure 3.11:

1. "***k***" pMOS transistors ($\mathrm{mp_{k1}}$-$\mathrm{mp_{kk}}$) connected in series, which are regulated by the driver pull-down nodes, and
2. "***k–1***" gate-drain-connected pMOS transistors. To avoid the problem of limiting the provided voltage, "***k–1***" pMOS transistors connected in-series are tied parallel to this group. They are regulated with reference voltages.

The circuit $\mathrm{GC_{nk}}$ is supplied by VD_{pk}. According to the on- and off-state, VD_{pk} switches between "$VHdd–(N–k)\times(Vn–\Delta V_I)$" and "$((k–1)\times VHdd/N)+(k–1)\times\alpha_n$". The voltage V_{Pk} of the node ***Pk*** between both groups of pMOS transistors can be written as:

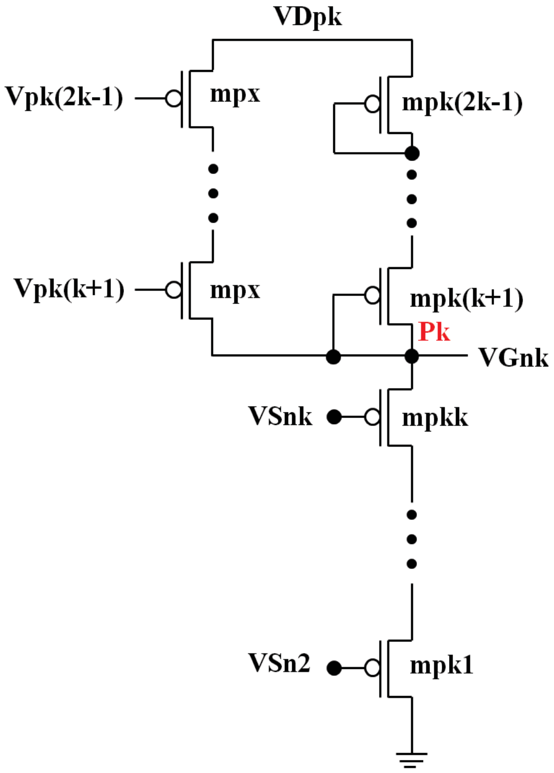


Figure 3.11: Circuit design of the gate-controlling circuit $\mathrm{GC_{nk}}$

$$V_{Pk} = \frac{(k-1) \times VS_{n(k+1)}}{k} + \frac{VD_{pk}}{k} \tag{3.49}$$

For the case if the supply voltage of the driver is divisible by the nominal voltage Vn (2.5 V), the upper rail voltage VD_{pk} of $\mathrm{GC_{nk}}$ is "$k\times$2.5 V", while the driver operates in the on-state. The provided gate voltage V_{Pk} in the above equation can be deduced by substituting Equation (3.10) as follows:

$$\begin{aligned} V_{Pk} &= \frac{(k-1)}{k} \times \frac{k \times Vout}{N} + \frac{k \times 2.5\,V}{k} \\ &= \frac{(k-1) \times Vout}{N} + 2.5\,V, \end{aligned} \tag{3.50}$$

which is equal to the required gate voltage VG_{nk}, as calculated in Equation (3.11).

Due to extra transistors $\mathrm{mp_x}$, as shown in Figure 3.11, the provided gate voltage VG_{nk} can be nearly constant regarding Equation (3.23) for supply voltages which are indivisible by the nominal voltage Vn.

For the circuit design of $\mathrm{GC_{pk}}$ to generate the gate voltages of k-th stacked pMOS transistors of an HV-driver, nMOS transistors are used instead of pMOS transistors.

Following the described theories and circuit design methodology for reducing the driver on-resistance, a 2- and a 3-stacked CMOS HV-drivers are designed in TSMC 65-nm low-power technology with a nominal voltage of 2.5 V for the I/O-devices. The circuits, which can be applied respectively for the maximum allowed supply voltages of 5.0 V and 7.5 V, will be presented in the next chapter.

Chapter 4

Circuits of 2- and 3-stacked CMOS HV-drivers

Regarding the theories and circuit design methodology for reducing the driver on-resistance, 2- and 3-stacked HV-drivers are designed for supply voltages in the range between 2.5 V and 5.0 V (2.5 V$<VHdd\leq$5.0 V) and 5.0 V and 7.5 V (5.0 V$<VHdd\leq$7.5 V), respectively, which are presented in this chapter. The HV-drivers are based on the minimum allowed stack number to maintain the operation of each transistor within the technology limits. The functionality of the circuits is analysed for various supply voltages and compared with the theories presented in Chapter 3 and also with a previous work [31].

4.1 Circuit Design of a 2-stacked CMOS HV-Driver

Figures 4.1a and 4.1b illustrate the circuit of a 2-stacked CMOS HV-driver and the corresponding test bench, respectively. The gate-controlling circuits $\mathrm{GC_{n2}}$ and $\mathrm{GC_{p2}}$ described in the previous chapter, are used. The HV-driver contains two pMOS transistors (Mp1 and Mp2) in the pull-up path and two nMOS transistors (Mn1 and Mn2) in the pull-down path. The input signal Vin regulates Mn1, whereas Mp1 is controlled by $Vpin$, which is level-shifted up from Vin using a circuit obtained from [30]. This level-shifter will be described in Chapter 6. The gate-controlling circuits $\mathrm{GC_{n2}}$ and $\mathrm{GC_{p2}}$ control the gates of Mn2 and Mp2 respectively, while the transistors Mn1 and Mn2 are regulated by the input signals Vin and $Vpin$. Four switches $\mathrm{SW\_VD_{n2}}$, $\mathrm{SW\_VD_{p2}}$, $\mathrm{SW\_Vp_{23}}$ and $\mathrm{SW\_Vn_{23}}$ are designed to provide the voltages VD_{n2}, VD_{p2}, Vp_{23} and Vn_{23} respectively according to the on- and off-states. Each switch consists of two transmission gates, each containing an nMOS and a pMOS transistor [61]. The parameters of the resistor and the capacitors, and the widths of transistors with a length of 280 nm are given in Table 4.1.

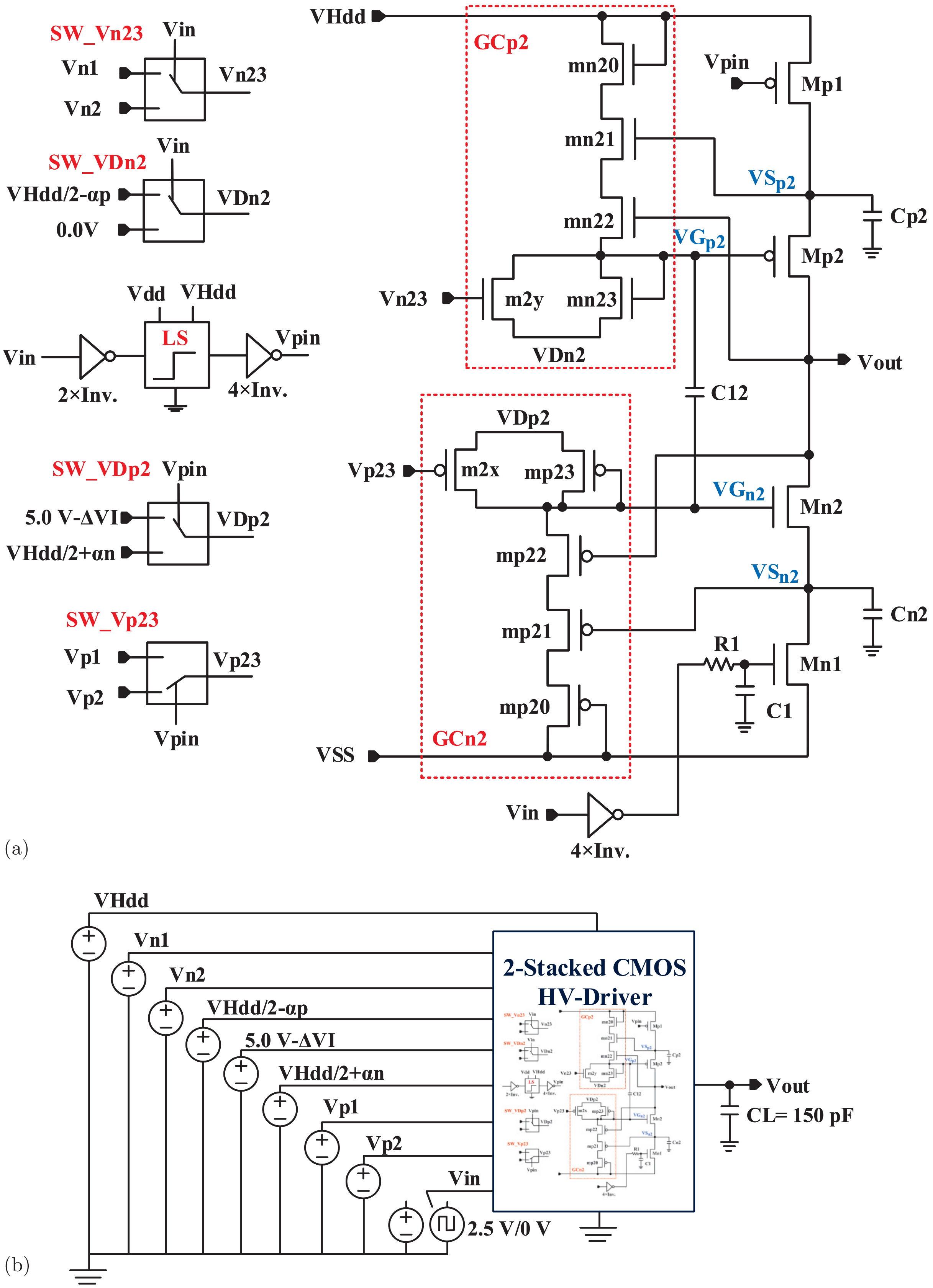


Figure 4.1: (a) Circuit design of a 2-stacked CMOS HV-driver and (b) the corresponding test bench for simulation

Table 4.1: The parameters of the transistors, capacitors and resistor of the designed 2-stacked CMOS driver

HV-driver		**GC$_{n2}$**				
Mn1, Mn2	Mp1, Mp2	mp$_{20}$	mp$_{21}$	mp$_{22}$	mp$_{23}$	m$_{2x}$
16 μm	32 μm	250 μm	250 μm	32 μm	28 μm	32 μm

inverters		**GC$_{p2}$**				
Mn_Inv	Mp_Inv	mn$_{20}$	mn$_{21}$	mn$_{22}$	mn$_{23}$	m$_{2y}$
100 μm	100 μm	75 μm	81 μm	96 μm	42 μm	78 μm

SW_Vn$_{23}$		**SW_VD$_{n2}$**		**SW_Vp$_{23}$**		**SW_VD$_{p2}$**	
nMOS	pMOS	nMOS	pMOS	nMOS	pMOS	nMOS	pMOS
64 μm	160 μm	320 μm	100 μm	320 μm	320 μm	320 μm	320 μm

passive components				
R$_1$	C$_1$	C$_{n2}$	C$_{p2}$	C$_{12}$
2 kΩ	0.2 pF	5.5 pF	10.5 pF	0.5 pF

To avoid an overvoltage, the gate-drain connected transistors mp$_{20}$ and mn$_{20}$ are added in series to the circuits GC$_{n2}$ and GC$_{p2}$, respectively. Four inverters and a low-pass filter containing a resistor R_1 and a capacitor C_1 adjust the input signal *Vin* to regulate the transistor Mn1 to prevent an overvoltage across the terminals of this transistor. Each inverter contains an nMOS (Mn_Inv) and a pMOS (Mp_Inv) transistor.

There now follows a description of the functionality of the circuit, along with a detailed analysis of the two previously considered groups of supply voltages.

4.1.1 Operational Analysis for VHdd of 5.0 V

Initially, the circuit operation is analysed for a supply voltage of 5.0 V (twice the nominal operating voltage of 2.5 V) and without using the additional transistors m$_{2x}$ and m$_{2y}$.

4.1.1.1 DC-Analysis

With respect to discharging the output voltage *Vout* from 5.0 V to 0 V, the node voltage characteristics of the 2nd-stacked nMOS transistor Mn2 are displayed in Figure 4.2 obtained from DC simulation for the on-state. Moreover, the ideal voltages VS_{n2} and VG_{n2}, which are expressed as "*Vout*/2" and "(*Vout*/2)+2.5 V" according to Equations (3.10) and (3.11), are also plotted in Figure 4.2. As can be seen, the real gate and source voltages approximately track these ideal lines.

In order to examine more closely into the accuracy of the circuit GC$_{n2}$, the difference between the real and ideal node voltages VG_{n2} and VS_{n2} and also the difference between the curves of the real VG_{n2} and "VS_{n2}+2.5 V" are illustrated in Figure 4.3a, which vary between –56 mV and 81 mV. The ideal gate and source voltages, which are equal to

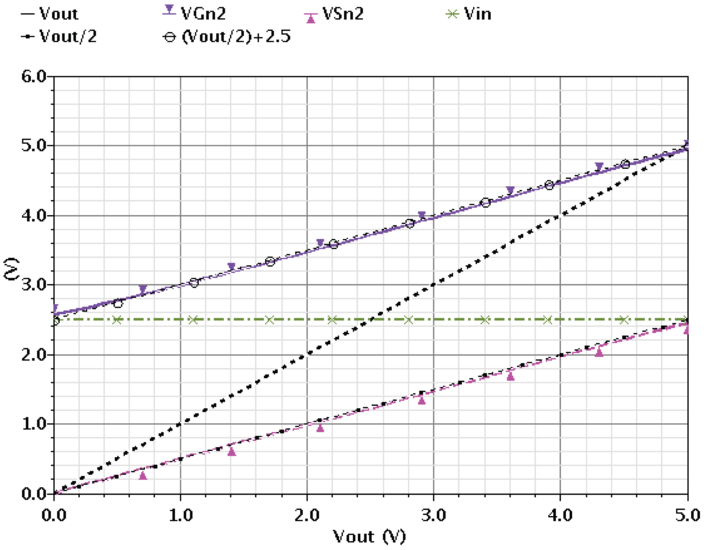
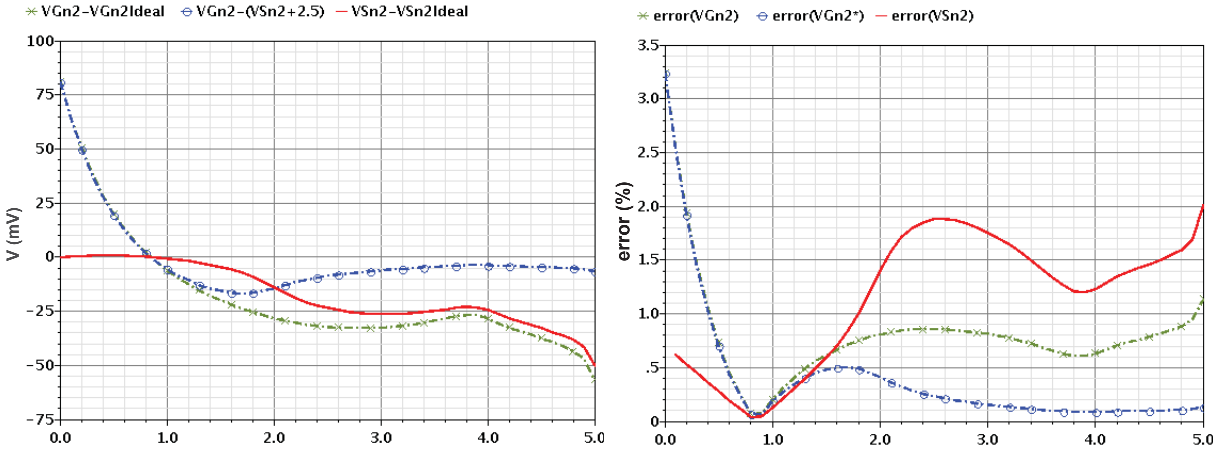


Figure 4.2: DC-characteristics of the ideal and real node voltages of Mn2 vs. *Vout* in the on-state while the output node discharges from 5.0 V to 0 V (*VHdd*=5.0 V)



(a) (b)

Figure 4.3: (a) Difference (b) errors between ideal and real node voltages of Mn2

"*Vout*/2+2.5 V" and "*Vout*/2", are termed as $VG_{n2Ideal}$ and $VS_{n2Ideal}$, respectively. The appropriate voltage errors for these variations are illustrated in Figure 4.3b and calculated as follows:

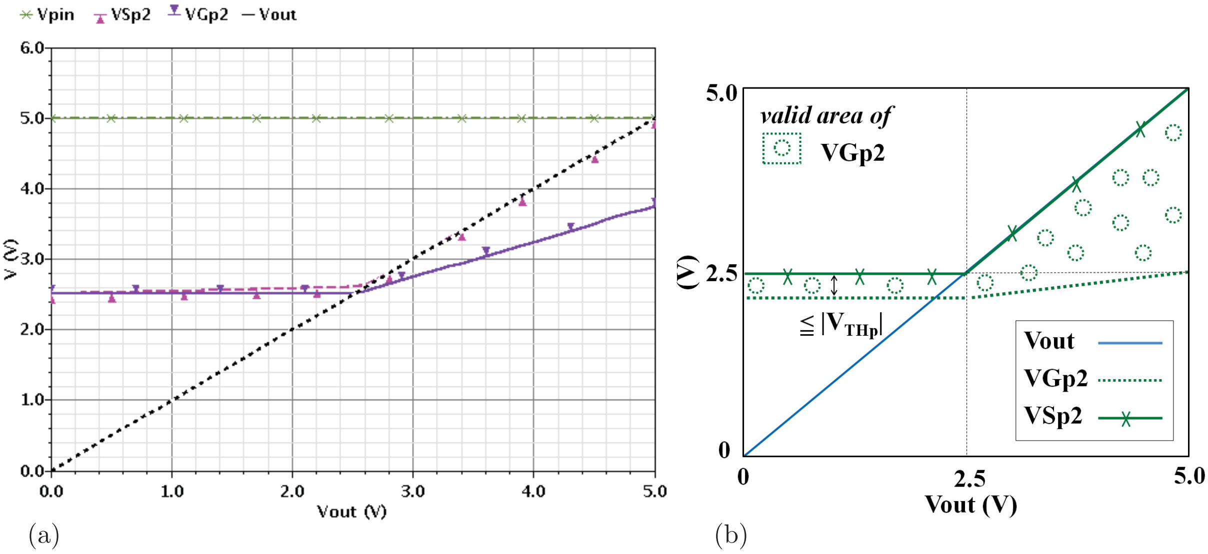
$$error(VG_{n2}) = \frac{\left|VG_{n2} - (\frac{Vout}{2} + 2.5\,V)\right|}{\frac{Vout}{2} + 2.5\,V} \times 100 \tag{4.1a}$$

$$error(VG_{n2}*) = \frac{|VG_{n2} - (VS_{n2} + 2.5\,V)|}{VS_{n2} + 2.5\,V} \times 100 \tag{4.1b}$$

$$error(VS_{n2}) = \frac{\left|VS_{n2} - \frac{Vout}{2}\right|}{\frac{Vout}{2}} \times 100 \tag{4.1c}$$

These errors are small and lower than 3.3%, indicating a high accuracy of the functionality of the circuits GC_{n2}.

Figure 4.4a depicts the voltages VG_{p2} and VS_{p2}, which resemble the desired voltages indicated in Figure 4.4b obtained from the calculation results in Chapter 3 (Figure 3.6a). The input signal *Vpin* of 5.0 V turns the pMOS transistor Mp1 off to avoid current flowing from the supply into the pull-up path; therefore, the output and source voltages (*Vout* and VS_{p2}) can be discharged from 5.0 V due to the active pull-down path. However, VS_{p2} decreases down to 2.5 V, at which voltage the provided gate voltage VG_{p2} switches the transistor Mp2 off. As a consequence, the driver output node can be further discharged to ground.



(a) (b)

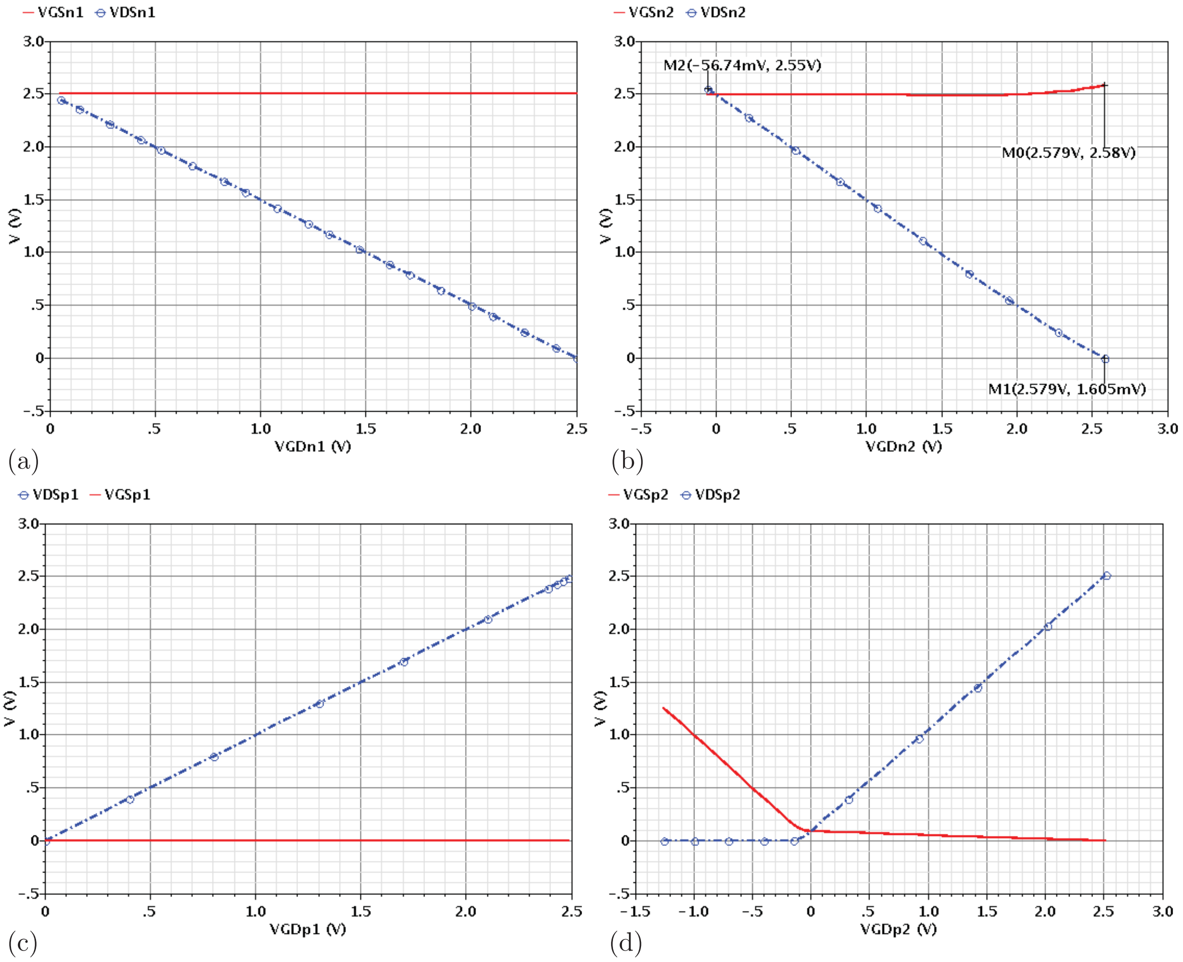
Figure 4.4: DC-characteristics of the node voltages of Mp2 vs. *Vout* obtained from the (a) simulation and (b) calculation results (on-state, *VHdd*=5.0 V)

Figures 4.5a–d show that the voltage difference across the terminals of each stacked transistor (Mn1, Mn2, Mp1 and Mp2) is within the technology limit with 5% tolerance.

The terms *VGS*, *VGD* and *VDS* represent the gate-source, gate-drain and drain-source voltages respectively of the relative nMOS or pMOS transistor. In the off-state, the input signal *Vin* of 0 V switches the transistor Mn1 off, while *Vpin* has a value of 2.5 V and turns Mp1 on since the supply voltage is 5.0 V.

As can be observed in Figure 4.6, the real gate voltage VG_{p2}, which is provided by the gate-controlling circuit GC_{p2}, and the source voltage VS_{p2} approach the ideal lines of "*Vout*/2" and "(*Vout*/2)+2.5 V" respectively, which are obtained from Equations (3.32) and (3.33).

In order to examine more closely the accuracy of the gate-controlling circuit GC_{p2},



(a) (b) (c) (d)

Figure 4.5: Voltage difference across terminals of (a) Mn1, (b) Mn2, (c) Mp1 and (d) Mp2 in the on-state (pull-down active, *VHdd*=5.0 V)

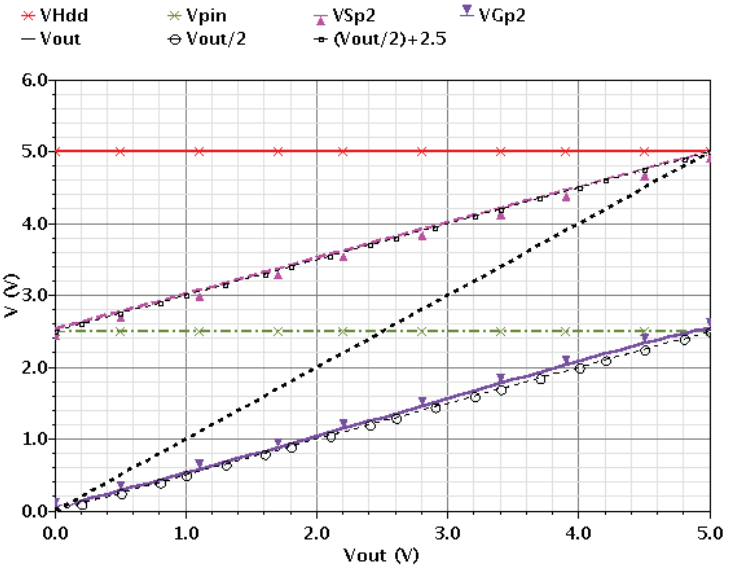


Figure 4.6: The node voltage characteristics of Mp1 and Mp2 vs. *Vout* (off-state, *VHdd*=5.0 V)

the differences between the real VG_{p2}, VS_{p2} and the ideal voltages $VG_{p2Ideal}$ and $VS_{p2Ideal}$, which are defined as:

$$VG_{p2Ideal} = \frac{Vout}{2} \tag{4.2a}$$

$$VS_{p2Ideal} = \frac{Vout}{2} + 2.5\,V, \tag{4.2b}$$

are plotted in Figure 4.7. These vary between 0.0 V and 85 mV.

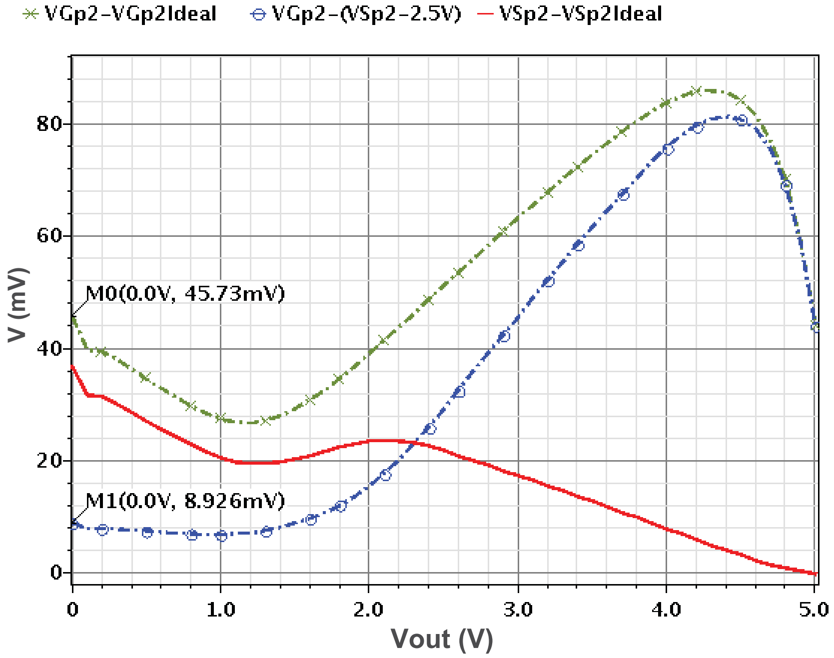
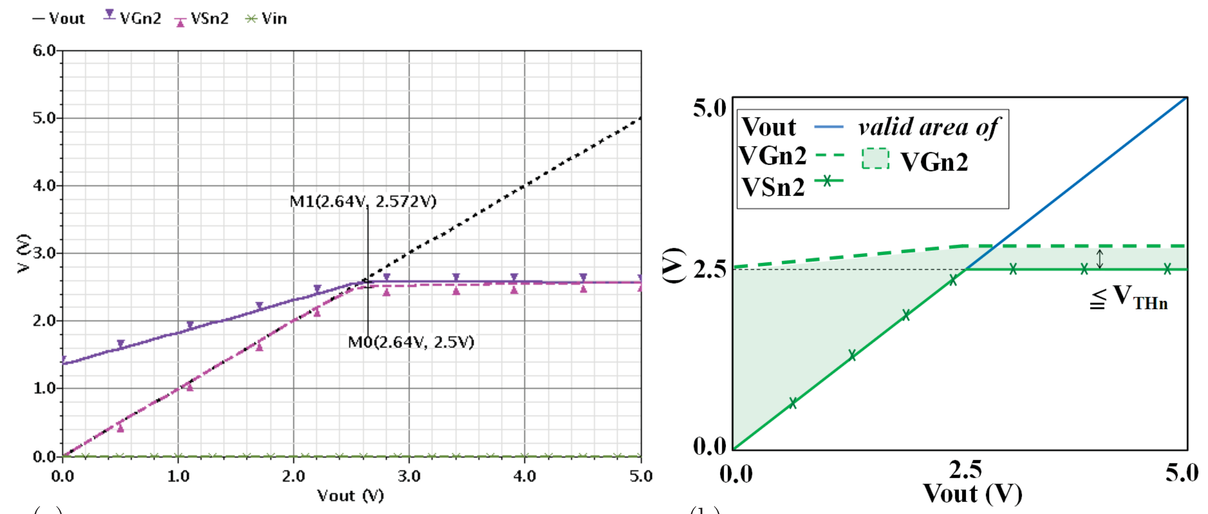


Figure 4.7: Difference between ideal and simulated node voltages of Mp2 (pull-up active with *VHdd* of 5.0 V)

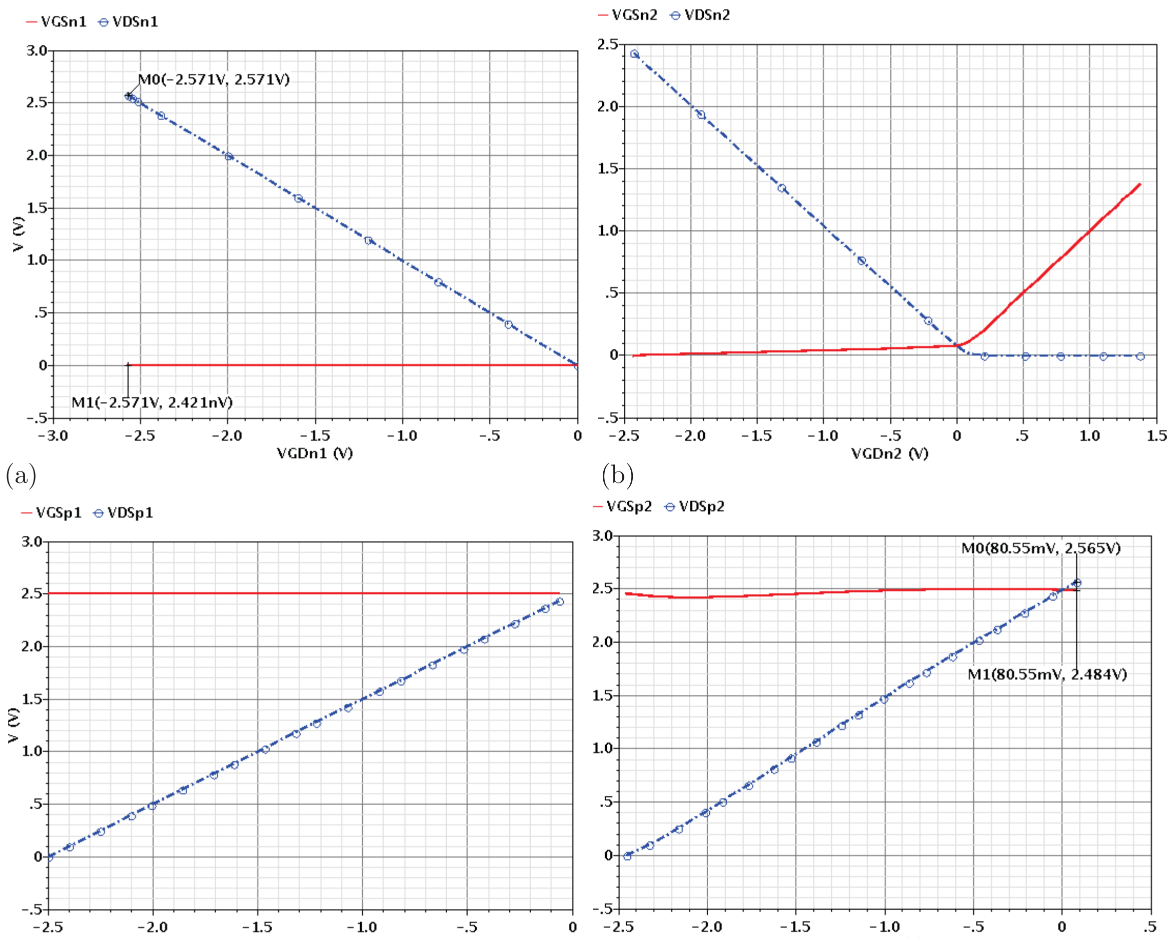
Figure 4.8a displays the node voltage characteristics ($Vout$, VG_{n2} and VS_{n2}) of Mn2 versus the output voltage in the off-state. These voltage characteristics follow the desired voltages, which are described in Section 3.4.1.2 and shown in Figure 4.8b. The input signal Vin of 0 V turns the transistor Mn1 off. Due to the active pull-up path, the node S_{n2} can charge up to 2.5 V because at this voltage, the gate-source voltage of Mn2 falls below its threshold voltage. Therefore, the transistor Mn2 turns off. As a result, the output node is charged to the supply voltage of 5.0 V.

In the off-state, the voltage between the terminals of each stacked transistor (Mn1, Mn2, Mp1 and Mp2) is proved and is plotted in Figures 4.9a–d. As can be seen, the different voltages are maintained within the technology limit of 2.5 V with a 5% tolerance.



(a) (b)

Figure 4.8: The node voltage characteristics of Mn2 vs. *Vout* in the off-state obtained from the (a) DC-simulation and (b) calculation results (*VHdd*=5.0 V)



(a) (b) (c) (d)

Figure 4.9: Voltage difference across the terminals of (a) Mn1, (b) Mn2, (c) Mp1 and (d) Mp2 in the off-state (*VHdd*=5.0 V)

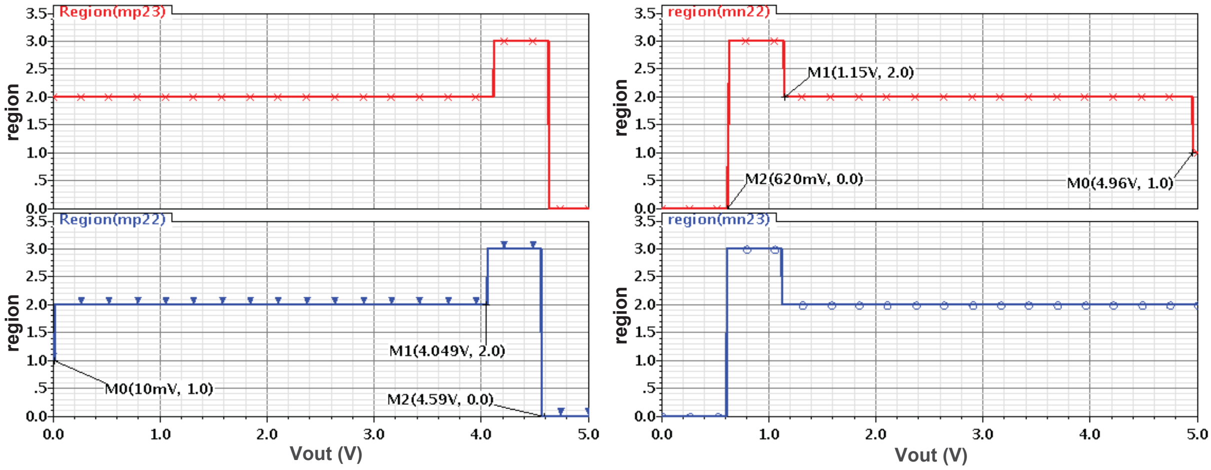
4.1.1.2 Reasons for Deviation

As previously demonstrated, there are slight deviations of the provided voltages (VG_{n2} and VG_{p2}) as simulated from the calculated values in Equations (3.11) and (3.33). There are different reasons for these inaccuracies, which are discussed below.

- Firstly, the transistors mn_{22}, mn_{23}, mp_{22} and mp_{23} of the gate-controlling circuits $\mathrm{GC}_{\mathrm{n2}}$ and $\mathrm{GC}_{\mathrm{p2}}$ not only operate in the saturation region but also enter the cut-off or sub-threshold regions, while the provided gate voltages should regulate the respective stacked transistors to drive the maximum current. Furthermore, mp_{22} and mn_{22} operate in the linear region, when the output node starts charging from ground to 10 mV and discharging for 40 mV from 5.0 V respectively as can be observed in Figures 4.10a and 4.10b. In the circuit design methodology for gate-controlling circuits presented in the last chapter in Section (3.4.2.1), it is assumed that these transistors (mn_{22}, mn_{23}, mp_{22} and mp_{23}) operate only in the saturation region. Since that is not the case, the circuits $\mathrm{GC}_{\mathrm{n2}}$ and $\mathrm{GC}_{\mathrm{p2}}$ cannot provide the exact calculated gate voltages in Equations (3.11) and (3.33).

In terms of the *BSIM4* MOSFET model used for the simulation, the numbers **0**, **1**, **2** and **3** refer to the cut-off, linear, saturation and sub-threshold regions, respectively (Figures 4.10a and 4.10b).

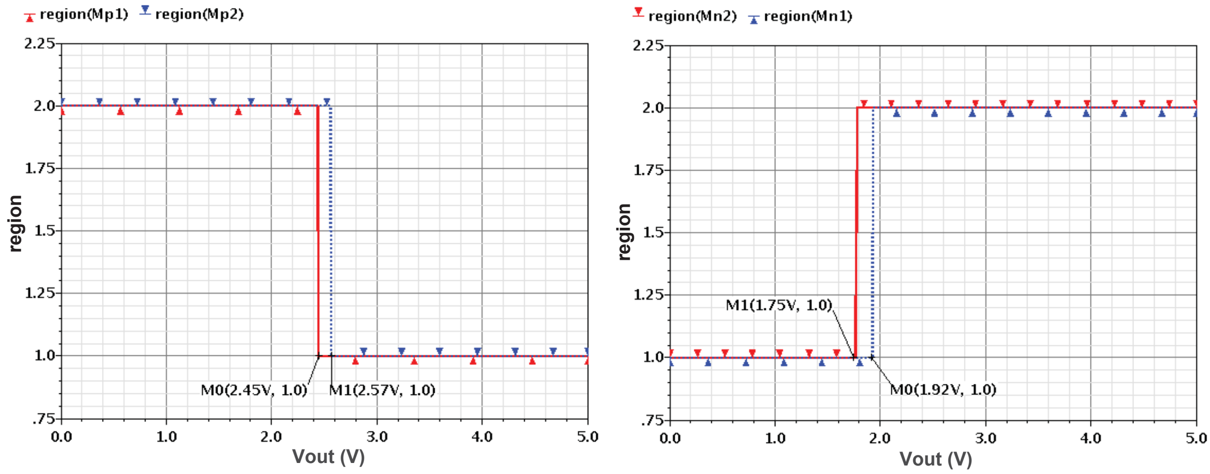
- It is also assumed that the same type of stacked transistors ("Mp1 and Mp2" / "Mn1 and Mn2") operate simultaneously in the same operational region: saturation, linear or cut-off regions, but in fact that is not the case, as shown in Figures 4.11a



(a) (b)

Figure 4.10: Operation regions of the transistors (a) mp_{22} and mp_{23} in the on-state, (b) mn_{22} and mn_{23} in the off-state of the HV-driver ($VHdd$= 5.0 V)

and 4.11b. By charging the driver output node from 0 V to 5.0 V, the pMOS transistors Mp1 and Mp2 enter into the linear region from the saturation region at *Vout* of 2.45 V and 2.57 V respectively (Figure 4.11a). While the output node discharges from 5.0 V to ground, the entering of the transistor Mn1 and Mn2 into the linear region can be detected at the output voltages of 1.92 V and 1.75 V, respectively in Figure 4.11b.



(a) (b)

Figure 4.11: Operation regions of the transistors (a) Mp1 and Mp2 in the off-state, (b) Mn1 and Mn2 in the on-state ($VHdd = 5.0$ V)

- The other reason for the deviation between generated and ideal gate voltages is that the provided rail voltages VD_{p2} and VD_{n2} for GC$_{\mathrm{p2}}$ and GC$_{\mathrm{n2}}$ due to the switches SW_VD$_{\mathrm{p2}}$ and SW_VD$_{\mathrm{n2}}$ respectively do not maintain the constant values of 5.0 V and 0 V, as required for the on- and off-state respectively. As indicated in Figure 4.12, VD_{p2} varies between 4.8 V and 5.0 V, whereas VD_{n2} varies between 0 V and 44 mV.

- For the calculated gate voltages to drive the maximum current in the driver pull-up and pull-down paths, it is also assumed that the threshold voltages of the involved transistors in each path of the driver and also of the gate-controlling circuits are identical, but in fact this is not the case. The threshold voltages of the coupled transistors (“Mn1 and Mn2”, “Mp1 and Mp2”, “mp$_{22}$ and mp$_{23}$” and also “mn$_{22}$ and mn$_{23}$”) are not equal.

In the case of the on-state, the threshold voltages of Mn1 and Mn2 (V_{th_Mn1} and V_{th_Mn2}) and also of mp$_{22}$ and mp$_{23}$ (V_{th_mp22} and V_{th_mp23}) are plotted versus *Vout* in Figures 4.13a and 4.13b, respectively. The absolute value of the diversity between both

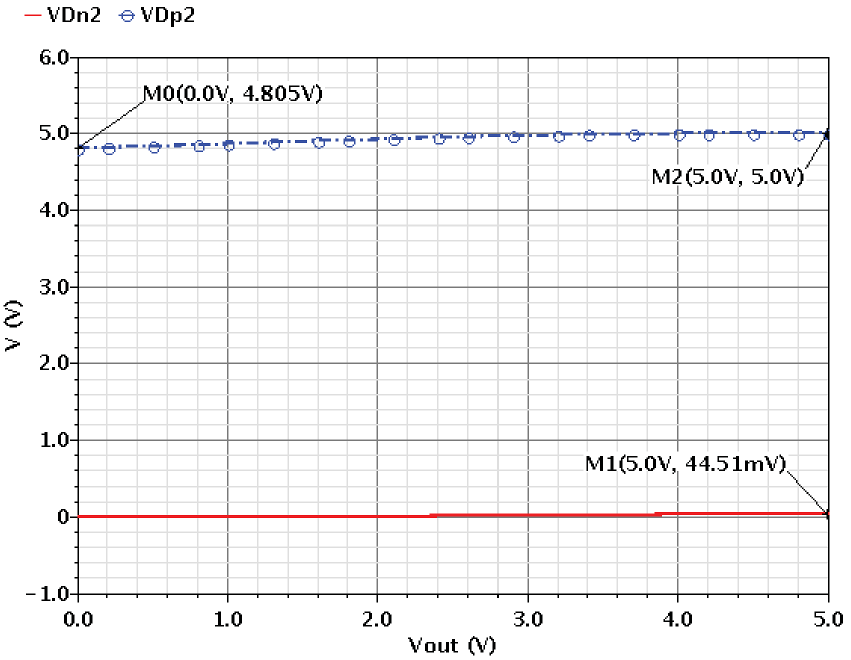
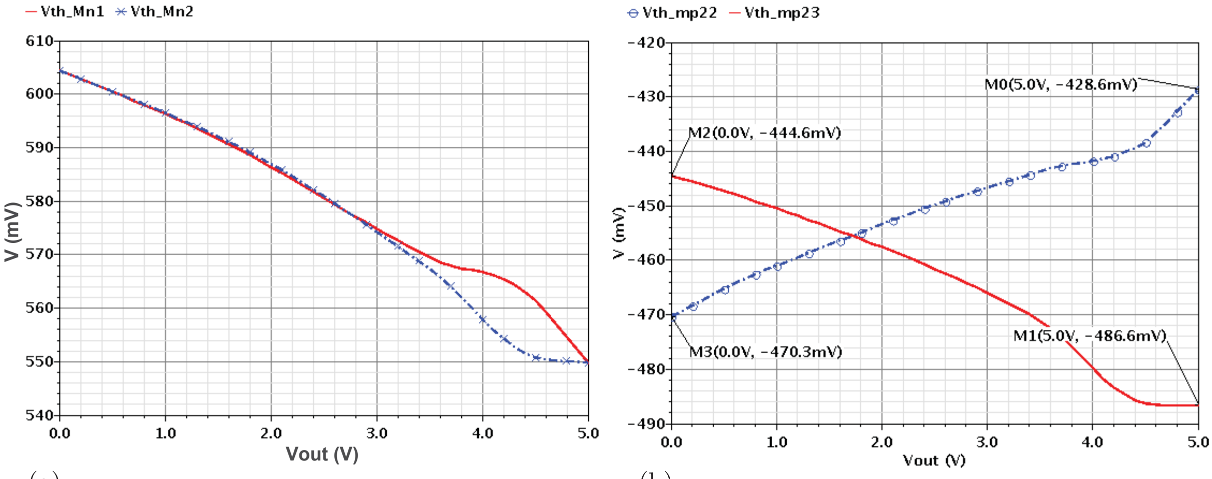


Figure 4.12: The voltage characteristics of VD_{n2} in the off-state and VD_{p2} in the on-state ($VHdd$= 5.0 V)

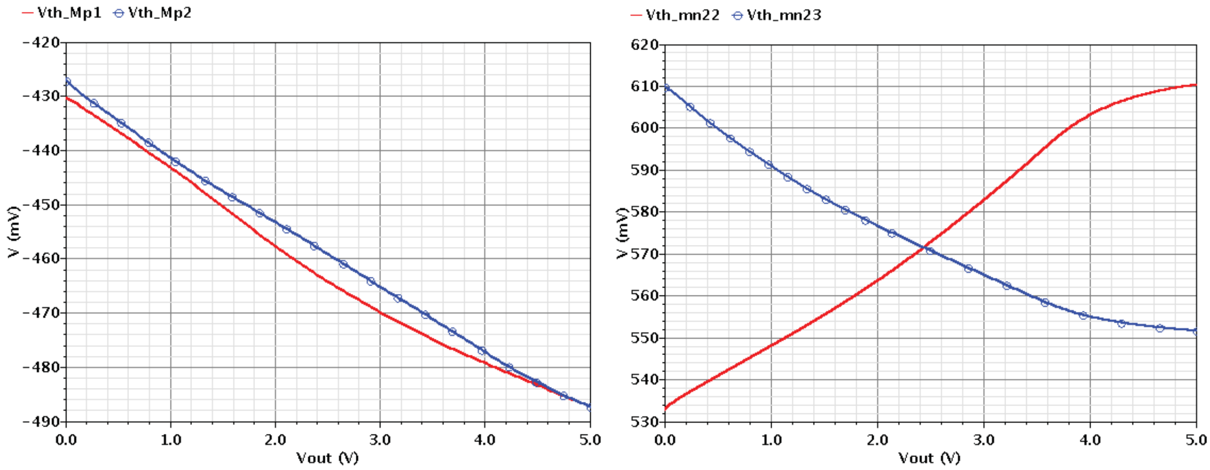


(a) (b)

Figure 4.13: (a) Threshold voltage characteristics of Mn1 and Mn2, (b) mp_{22} and mp_{23} vs. *Vout* in the on-state

V_{th} of Mn1 and Mn2 varies between 0 V and approximately 12 mV, whereas the maximum difference between these voltages of mp_{22} and mp_{23} reaches 58 mV.

The same problem appears for the threshold voltages of the coupled transistors Mp1 and Mp2 (V_{th_Mp1} and V_{th_Mp2}) and also of mn_{22} and mn_{23} (V_{th_mn22} and V_{th_mn23}), as depicted in Figures 4.14a and 4.14b in the off-state. The maximum difference between V_{th_Mp1} and V_{th_Mp2} is 5.1 mV at *Vout* of 2.4 V and that between V_{th_mn22} and V_{th_mn23} is about 77 mV, when the output node starts charging.



(a) (b)

Figure 4.14: Threshold voltage characteristics of (a) Mp1 and Mp2 and (b) mn$_{22}$ and mn$_{23}$ vs. *Vout* in the off-state

- Furthermore, to avoid an overvoltage, the widths of the transistors mn$_{22}$ and mn$_{23}$ are set differently, as can be observed from Table 4.1. Moreover, mp$_{22}$ and mp$_{23}$ do not have the same dimensions, even though for the circuit design of gate-controlling circuits GC$_{\mathrm{n2}}$ and GC$_{\mathrm{p2}}$ providing the calculated gate voltages, it is assumed that these transistors should be identical to the same type of transistor. This is one of the reasons for the deviation between the generated and ideal gate voltages.

In the next step, it is considered to verify the feasibility of the circuit by the transient analysis.

4.1.1.3 Transient Analysis

A pulse signal (*Vin*), which varies between 0 V and 2.5 V, is applied to the input of the circuit. Figure 4.15 illustrates the transient characteristic of *Vin* and its level-shifted signal *Vpin* with an offset of 2.5 V.

Using the transient analysis, it was identified that the values of the provided gate voltages VG_{n2} and VG_{p2} are limited because of the impact of the transistors' parasitic capacitances on the circuits GC$_{\mathrm{n2}}$ and GC$_{\mathrm{p2}}$ respectively, and also that the transistors mn$_{22}$ and mn$_{23}$ of GC$_{\mathrm{p2}}$ and mp$_{22}$ and mp$_{23}$ of GC$_{\mathrm{n2}}$ enter the cut-off region at the beginning of charging and discharging the output node as shown in Figures 4.10a and 4.10b.

Figure 4.16a shows the transient simulation results of *Vout*, VG_{n2} and also the provided voltage $V(R||C_{par})$ of the equivalent circuit instead of the transistor mp$_{23}$ (Figures 4.16b and 4.16c), for which a parallel connected resistor (R) of 150 kΩ and a parasitic capacitor (C_{par}) of 250 fF are used. In the on-state, when the output node has just started discharging, VG_{n2} has to be 5.0 V and follows the calculated rule of "*Vout*/2+2.5 V", but it starts with a value of ca. 4.6 V (Figure 4.16a at 1 μs). At this voltage, the pMOS transistors

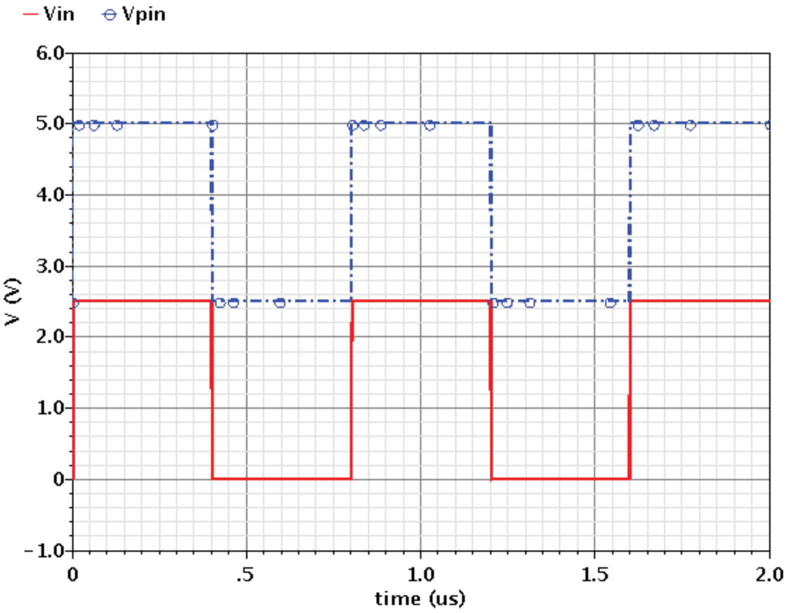
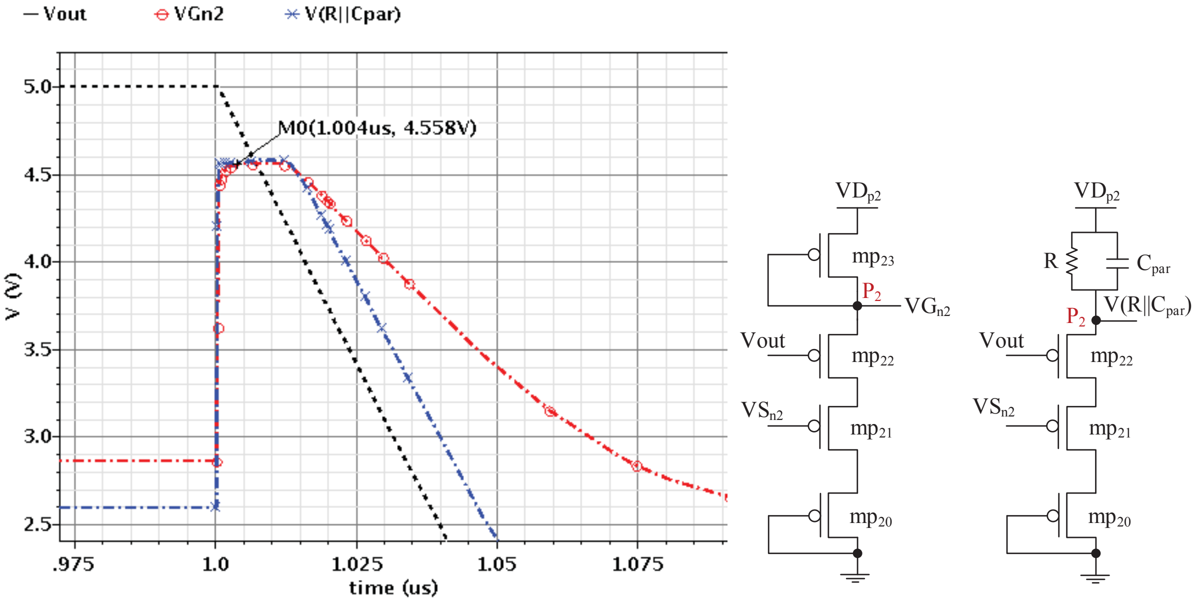


Figure 4.15: Transient voltage characteristics of the input signals *Vin* and *Vpin* (*VHdd*=5.0 V)



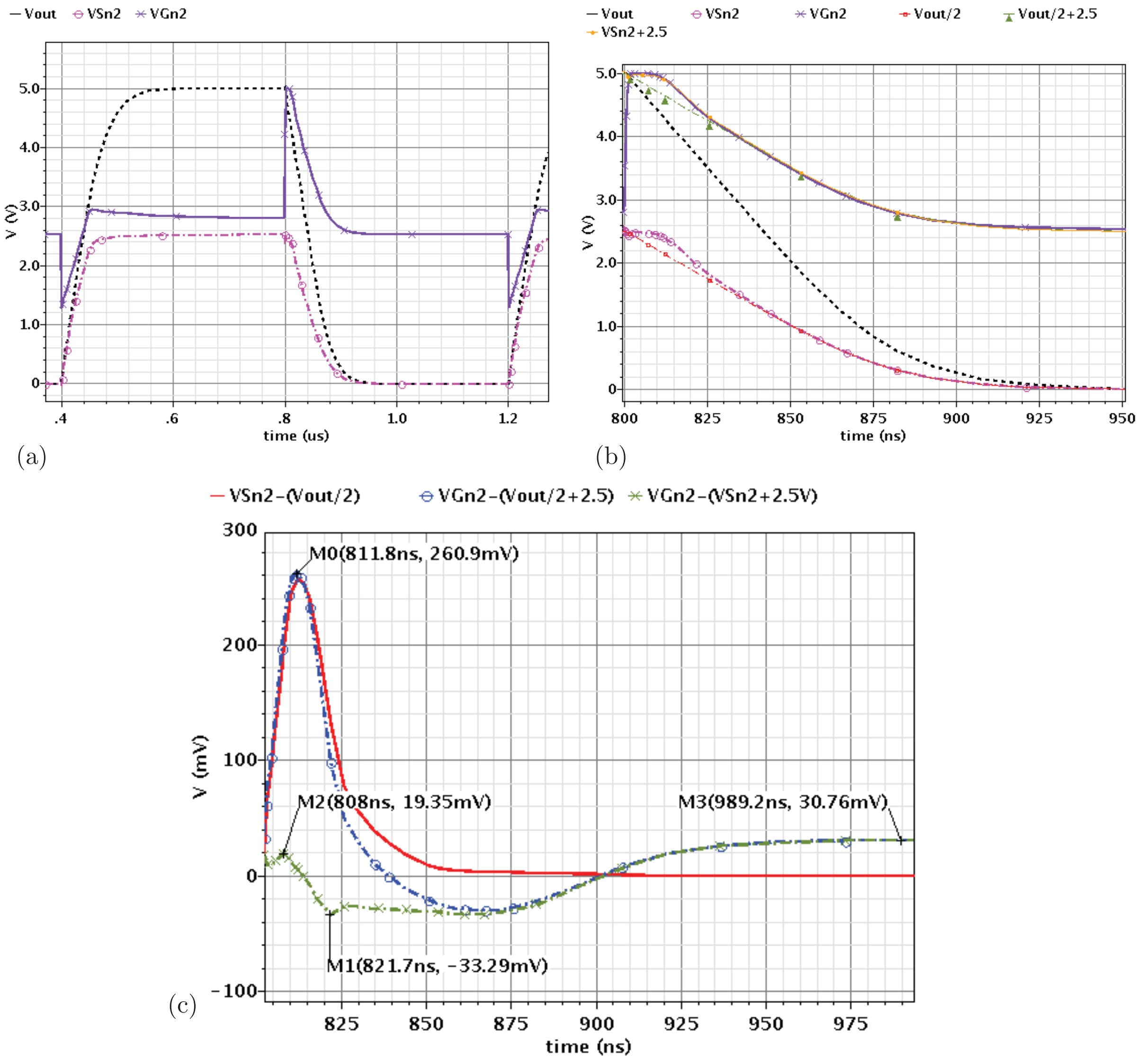
(a) (b) (c)

Figure 4.16: (a) The transient voltage characteristics of *Vout*, VG_{n2} and $V(R||C_{par})$ (*VHdd*=5.0 V), (b) the circuit $\mathrm{GC}_{\mathrm{n2}}$ of the designed 2-stacked CMOS including (c) the equivalent circuit model instead of the transistor mp_{23}

mp_{22} and mp_{23} enter into the sub-threshold region from the cut-off region. The model cannot track VG_{n2} exactly because of the constant value of the resistor R, whereas the on-resistance of mp_{23} continuously changes depending on the condition of the transistors mp_{21} and mp_{22}, which varies due to the respective gate voltages referred to as VS_{n2} and *Vout* respectively. The provided VG_{n2} maintains 4.6 V until the pMOS transistors mp$_{22}$ and mp$_{23}$ start to operate in the sub-threshold and then in the saturation regions. As previously mentioned, in order to avoid this problem, a pMOS transistor such as m$_{2x}$ is connected in parallel to mp$_{23}$, as can be seen in Figure 4.1a (Figure 3.9c). The gate of this transistor is regulated with the switch circuit SW_Vp$_{23}$ depending on the on- and off-states. On the other side, the parallelogram-shaped region ***B*** in Figure 3.4 helps to simplify the problem, since the desired voltage VG_{n2} does not need to follow exactly the line of Equation (3.11) when the transistor Mn2 operates in the saturation region.

Figure 4.17a represents a transient simulation of $Vout$, VS_{n2} and VG_{n2} of the improved circuit GC$_{n2}$ (Figure 4.1).

In the time frame between 0.4 μs and 0.8 μs, the nMOS transistor Mn1 is in the off-state due to the input signal of 0 V. The provided gate voltage VG_{n2} rises from ca. 1.3 V



(a)

(b)

(c)

Figure 4.17: (a) Transient node voltage characteristics of Mn2, (b) comparison between these and the appropriate ideal voltages and (c) their differences ($VHdd$= 5.0 V)

at 0.4 μs to 2.9 V, whereas the node VS_{n2} is charged from ground to 2.5 V. The transistor Mn2 turns off because its gate-source voltage falls below its threshold voltage. As a result, the output node (*Vout*) is charged to 5.0 V.

At 0.8 μs, the input signal of 2.5 V switches on the transistor Mn1; therefore, the node VS_{n2} is discharged. The transient voltage characteristic VS_{n2} and VG_{n2} approach the calculated curves "*Vout*/2" and "*Vout*/2+2.5 V" ("VSn2+2.5 V") respectively, as can be seen in Figure 4.17b zoomed in from Figure 4.17a. The differences between the ideal and simulated voltages are illustrated in Figure 4.17c.

The voltage difference in the time frame between 800 ns and 825 ns, with a maximum of 261 mV (deviation of 5.5% from the ideal voltage), is higher than in the other time range, but it is not considerable because of the calculated VG_{n2}, which forms region ***B*** in Figure 3.4. However, it is remarkable that the absolute maximum difference between VG_{n2} and "VS_{n2}+2.5 V" is about 33 mV (0.7%), which indicates the high accuracy of the gate-controlling circuit GC_{n2} providing the voltage VG_{n2} with an offset of 2.5 V to VS_{n2}.

The same problem as previously mentioned regarding the provided VG_{n2}, which was limited at the beginning of discharging, also occurs in the circuit GC_{p2}. Therefore, to solve this problem, an nMOS transistor such as m_{2y}, which is regulated with the switch circuit SW_Vn_{23} depending on the driver on- and off-states, is added in parallel to mn_{23}, as can be seen in Figure 4.1a (Figure 3.9d).

Figure 4.18 shows a transient simulation of *Vout*, VS_{p2} and VG_{p2} of the improved circuit GC_{p2}. In the on-state, the level-shifted input signal *Vpin* is 5.0 V, which turns the transistor Mp1 off. Therefore, the pull-up node S_{p2} can discharge from 5.0 V but only down to 2.5 V because at this value, the provided gate voltage VG_{p2}, which varies between 2.1 V and 2.3 V, turns the transistor Mp2 off. As a result, the output node discharges to ground due to the active pull-down transistors.

In the time frame between 0.4 μs and 0.8 μs in Figure 4.18, in which the driver enters the off-state, the provided VG_{p2} approximates to the rule of *Vout*/2 and also tracks the curve of "VS_{p2}–2.5 V".

As depicted in Figure 4.1a, to the original circuit based on theory for driving the maximum current, the transistors m_{2x} and m_{2y} are added. Furthermore, to avoid an overvoltage, two additional MOS diodes, mp_{20} and mn_{20}, are employed in series in the circuits GC_{n2} and GC_{p2}, respectively. Three capacitors C_{n2}, C_{p2} and C_{12} are also used for damping down an overvoltage.

In addition to the previously mentioned reasons for the slight deviation between the provided gate voltages and the calculated results, adding extra transistors and capacitors also affects the accuracy of the generated voltages VG_{n1} and VG_{p2}.

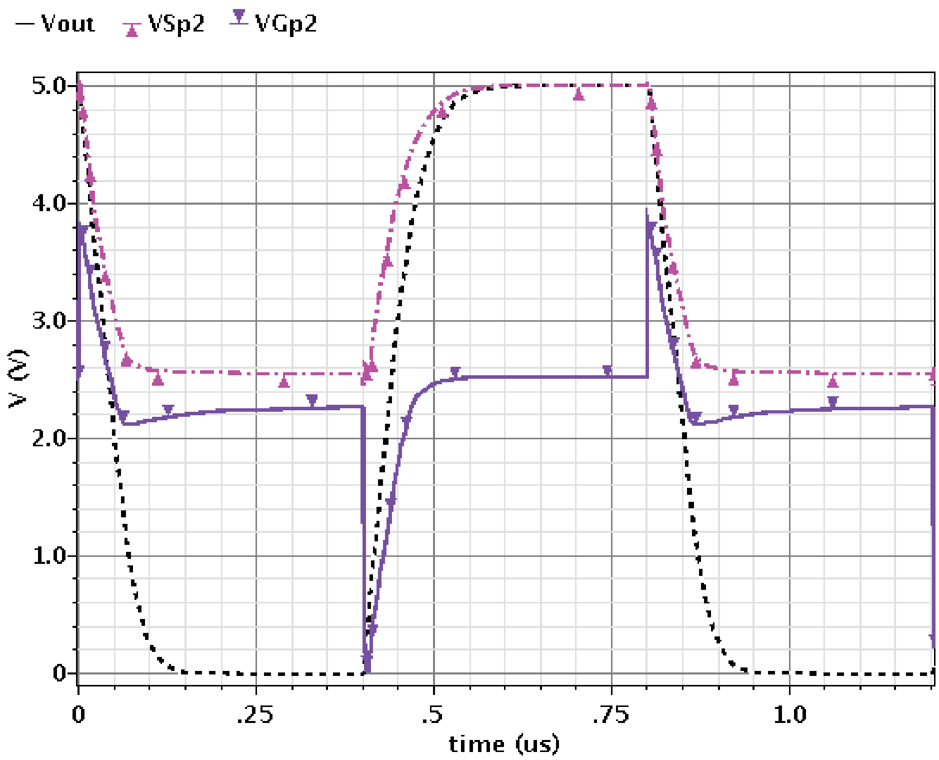
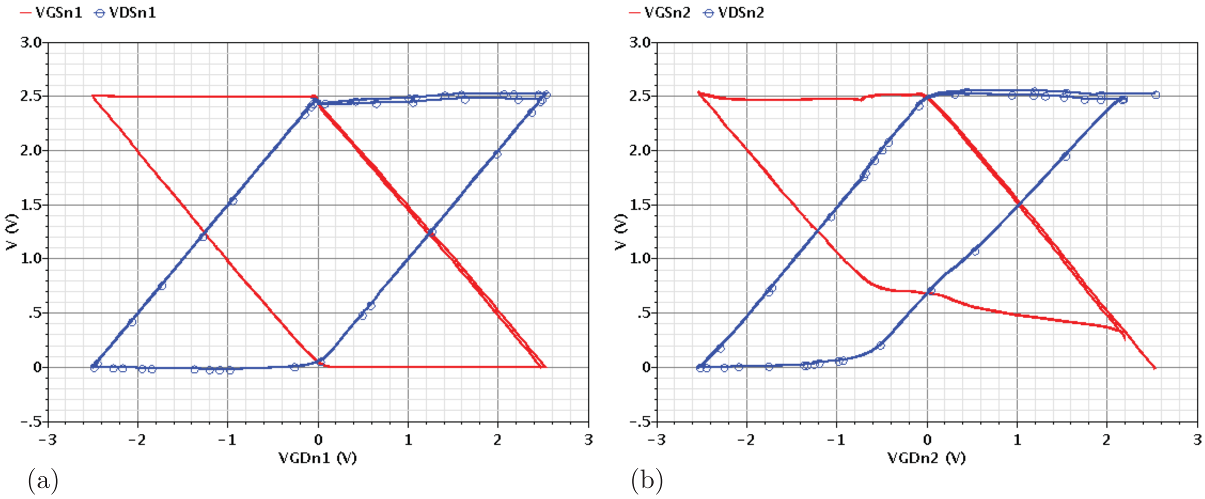


Figure 4.18: Transient voltage characteristics of the transistor nodes Mp2 ($VHdd$=5.0 V)

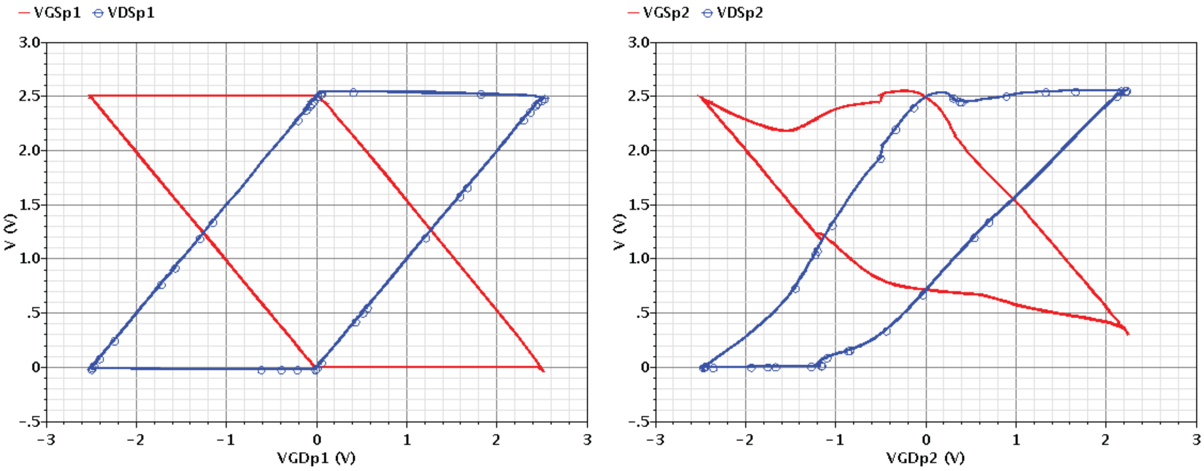
Figures 4.19a–b and 4.20a–b show the voltage difference characteristics across the transistor nodes: gate-source (VGS_{n1}, VGS_{n2}, VGS_{p1} and VGS_{p2}) and drain-source (VDS_{n1}, VDS_{n2}, VDS_{p1} and VDS_{p2}) versus gate-drain voltage (VGD_{n1}, VGD_{n2}, VGD_{p1} and VGD_{p2}) of the transistors Mn1, Mn2, Mp1 and Mp2 from the transient simulation results, which are maintained within the technology limit of 2.5 V with 5% tolerance.



(a)

(b)

Figure 4.19: Voltage difference across the terminals of (a) Mn1 and (b) Mn2 obtained from the transient simulation results (VHdd= 5.0 V)



(a) (b)

Figure 4.20: Voltage difference across the terminals of (a) Mp1 and (b) Mp2 obtained from the transient simulation results (VHdd= 5.0 V)

4.1.2 Operational Analysis for VHdd Indivisible by Vn

As mentioned in this and also the previous chapter, extra transistors (m_{2x} and m_{2y}) are employed for gate-controlling circuits of HV-drivers supplied by a voltage multiple of *Vn*. Furthermore, regarding these additional transistors, the provided gate voltages VG_{nk} and VG_{pk} are almost constant according to Equations (3.23) and (3.32) for supply voltages, which are indivisible by the nominal voltage and are between "$(N{-}1)\times Vn$" and "$N\times Vn$", while the output node discharges from *VHdd* to V_I and charges from 0 V to V_{Ip}, respectively. Depending on the supply voltage and also the on- and off-states, the gates of these transistors are regulated with extra switches SW_Vp$_{23}$ and SW_Vn$_{23}$ providing the voltages Vp_{23} and Vn_{23}, as illustrated in Figure 4.1a.

For a supply voltage indivisible by *Vn*, operation of the designed 2-stacked CMOS HV-driver (Figure 4.1a) is verified first with a supply voltage of 4.0 V. Depending on this supply voltage, the reference voltages of the circuit are respectively set at the required values to operate the gate-controlling circuits for driving the maximum current in the driver pull-up and pull-down paths while ensuring that every transistor stays within its safe operating region. The low and high levels of the input signal *Vin* are shifted from 0 V and 2.5 V up to 1.5 V and 4.0 V, respectively to form the signal *Vpin* regulating the pMOS transistor Mp1.

4.1.2.1 DC and Transient Analysis

Figure 4.21a depicts the DC-simulation results of the driver pull-down nodes (VS_{n2}, VG_{n2} and *Vout*) for driving the maximum drain current in the on-state. For comparison with the theory described by Equations (3.23) and (3.24), two curves are additionally plotted:

one is the line of "*Vout/2+2.5 V*" as the ideal gate voltage for the range of *Vout* between 0 V and 3.0 V. The other curve is "VS_{n2}*+2.5 V*", which is the task of the gate-controlling circuit GC_{n2} to shift up the source voltage VS_{n2} with an offset of 2.5 V for providing the voltage VG_{n2}. According to Table 3.3, the defined range of ΔV_I is 1.0 V for the supply voltage of 4.0 V, which means, in the output voltage range between 3.0 V and 4.0 V, the ideal gate voltage VG_{n2} remains constant at 4.0 V. However, as can be seen in Figure 4.21a, the provided VG_{n2} has this constant value, when the output node discharges from 4.0 V to 3.4 V. After this, VG_{n2} decreases and approaches linearly from 4.0 V to 2.5 V,

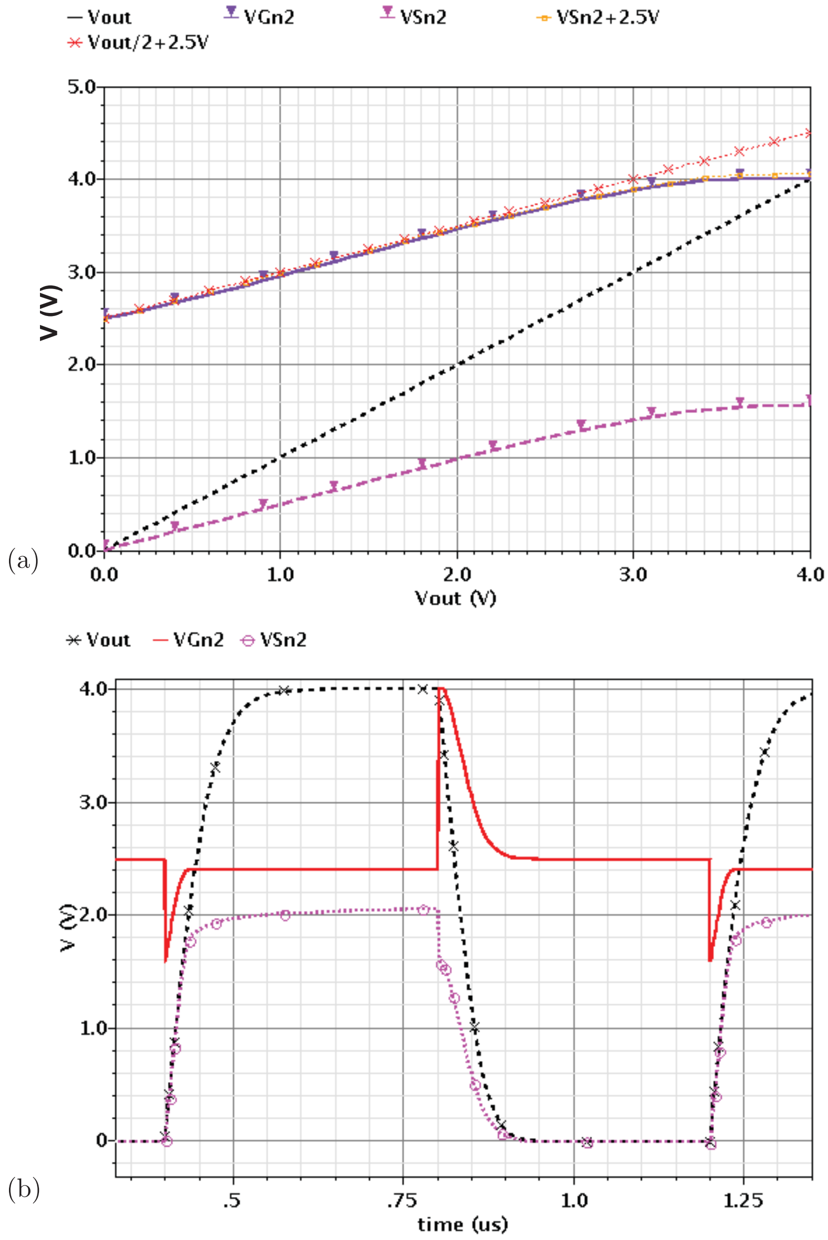


Figure 4.21: The ideal and provided node voltages of Mn2 from the (a) DC simulation results in the on-state and (b) the transient simulation results (*VHdd*= 4.0 V)

while the output voltage reduces from 3.0 V to ground. This can also be observed from the transient characteristic of VG_{n2} in Figure 4.21b, while the output node discharges from 4.0 V to ground.

Figure 4.22 shows, how the provided gate voltage VG_{n2} approaches the rule in Equations (3.23) and (3.24) with respect to the output voltage.

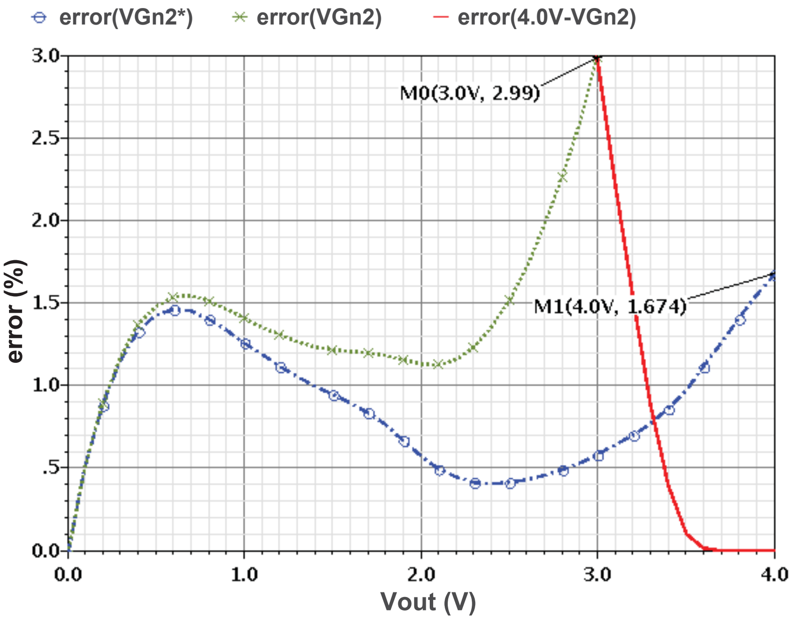


Figure 4.22: Errors between the provided and the ideal gate voltage VG_{n2} ($VHdd$=4.0V)

The curve of $error(VG_{n2})$ represents the error between the provided and ideal gate voltage VG_{n2} with a maximum of 3%, while the output load discharges from 3.0 V to ground. The curve of $error(4.0\,V{-}VG_{n2})$ depicts an error between VG_{n2} and the rule in Equation (3.23) for the output voltage in the range between 3.0 V and 4.0 V. This error increases from 0% to a maximum value of 3% during the discharging of the output load.

The term $error(VG_{n2}{*})$ expresses the error between the provided VG_{n2} and the line of "VS_{n2}+2.5 V" and has an average of about 1% for *Vout* in the range of between 0 V and 4.0 V. This indicates a high accuracy of about 99% for the functionality of the circuit $\mathrm{GC_{n2}}$ in providing the gate voltage VG_{n2} with an offset of 2.5 V to the source voltage VS_{n2}.

In the off-state, it is expected that the output voltage will be charged to the supply voltage of 4.0 V because of the active pull-up and the inactive pull-down path. The node voltage VS_{n2} can be charged to 2.0 V ($Vout/2$), when the transistor Mn2 is turned off at *Vout* of 2.0 V due to the provided gate voltage VG_{n2}. This is proved by the DC-simulation, as can be seen in Figure 4.23a.

In the transient simulation illustrated in Figure 4.21b, in the time frame between 0.4 μs and 0.8 μs the provided gate voltage VG_{n2} is about 2.4 V, which turns the transistor Mn2 off when the node S_{n2} charges to 2.0 V. As a consequence, the output voltage reaches to 4.0 V. Furthermore, an equal voltage drop of 2.0 V across each stacked transistor (Mn1 and Mn2) has been achieved, which does not impact negatively on the lifetime of the transistors.

The transient node voltage characteristics of the pMOS transistor Mp2 are displayed in Figure 4.23b. In the driver off-state (between 0.4 μs and 0.8 μs), the provided gate voltage VG_{p2} starts from 0 V to 1.5 V driving Mp2. Therefore, the current can drive from the supply to the driver output node, since the pull-down network is inactive. As a result,

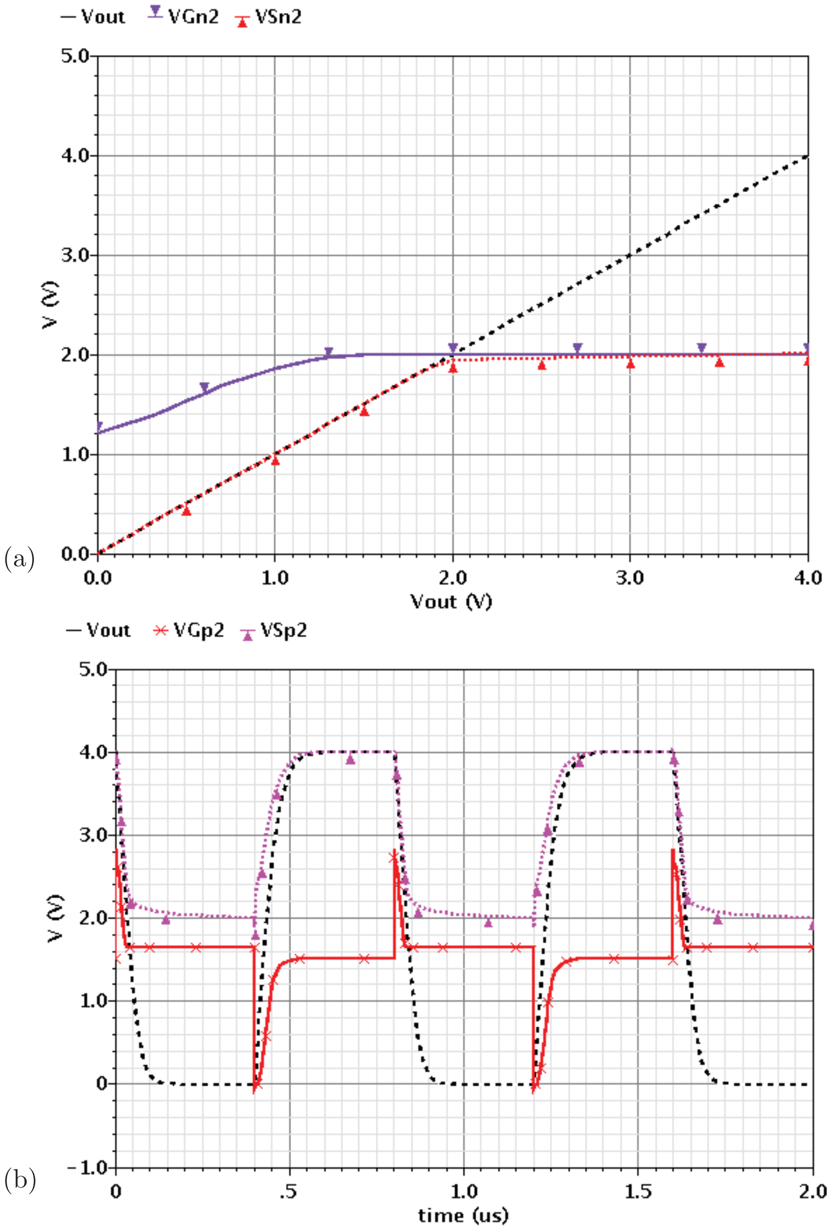


Figure 4.23: (a) The node voltage DC-characteristics of Mn2 in the off-state and (b) the transient node voltage characteristics of Mp2 ($VHdd$=4.0 V)

the node S_{p2} and the output load can charge to the supply voltage of 4.0 V (VS_{n2} and *Vout*). The offset between VG_{p2} and VS_{p2} is maintained at 2.5 V during the off-state.

In the on-state, the signal *Vpin* of 4.0 V switches the transistor Mp1 off. Due to this and the active pull-down path, the driver output node discharges to ground. Consequently, the node S_{p2} also discharges from 4.0 V but until ca. 2.0 V, since the provided gate voltage VG_{p2} of ca. 1.7 V turns Mp2 off at that point. As a result, an equal voltage drop of about 2.0 V across each stacked transistor (Mp1 and Mp2) has been achieved.

4.1.2.2 Analysing the Performance of the Circuit

Since the circuit is designed based on the theory of driving the maximum drain current for minimum on-resistance, in this section, the performance of the designed 2-stacked CMOS HV-driver will be analysed.

According to Table 3.3, the defined range of ΔV_I is 2.0 V for a 2-stacked CMOS HV-driver with a supply voltage of 3.0 V, which means, in the output voltage range between 1.0 V and 3.0 V, the ideal gate voltage VG_{n2} should be constant at 3.0 V according to Equation (3.23). However, as can be seen in Figure 4.24, the provided VG_{n2} has this constant value, when the output node discharges from 3.0 V to 2.6 V. After this, VG_{n2} decreases approximately linearly to 2.5 V, while the output voltage reduces to ground.

Because the accuracy of the gate-controlling circuits of the HV-driver with a supply voltage of 3.0 V is worse than the other higher supply voltages, the performance of the circuit is proved with this voltage (*VHdd* of 3.0 V). In terms of the calculation results,

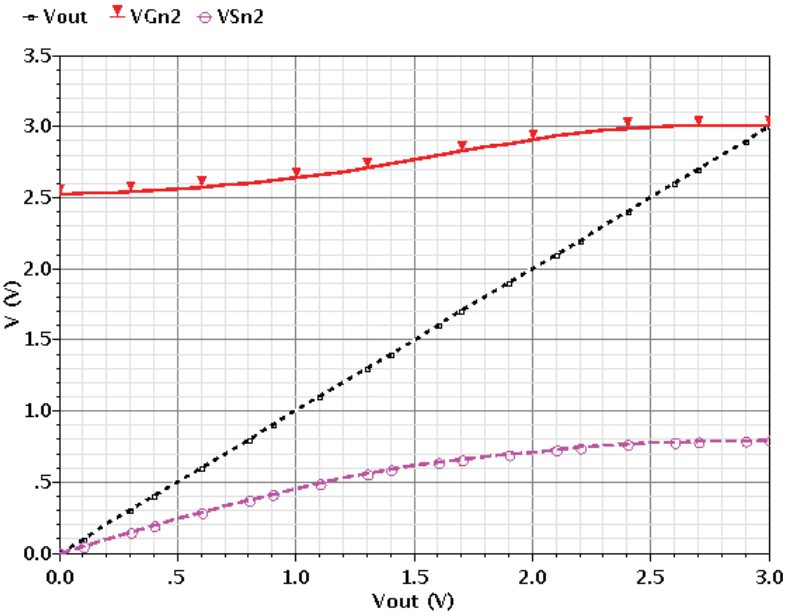
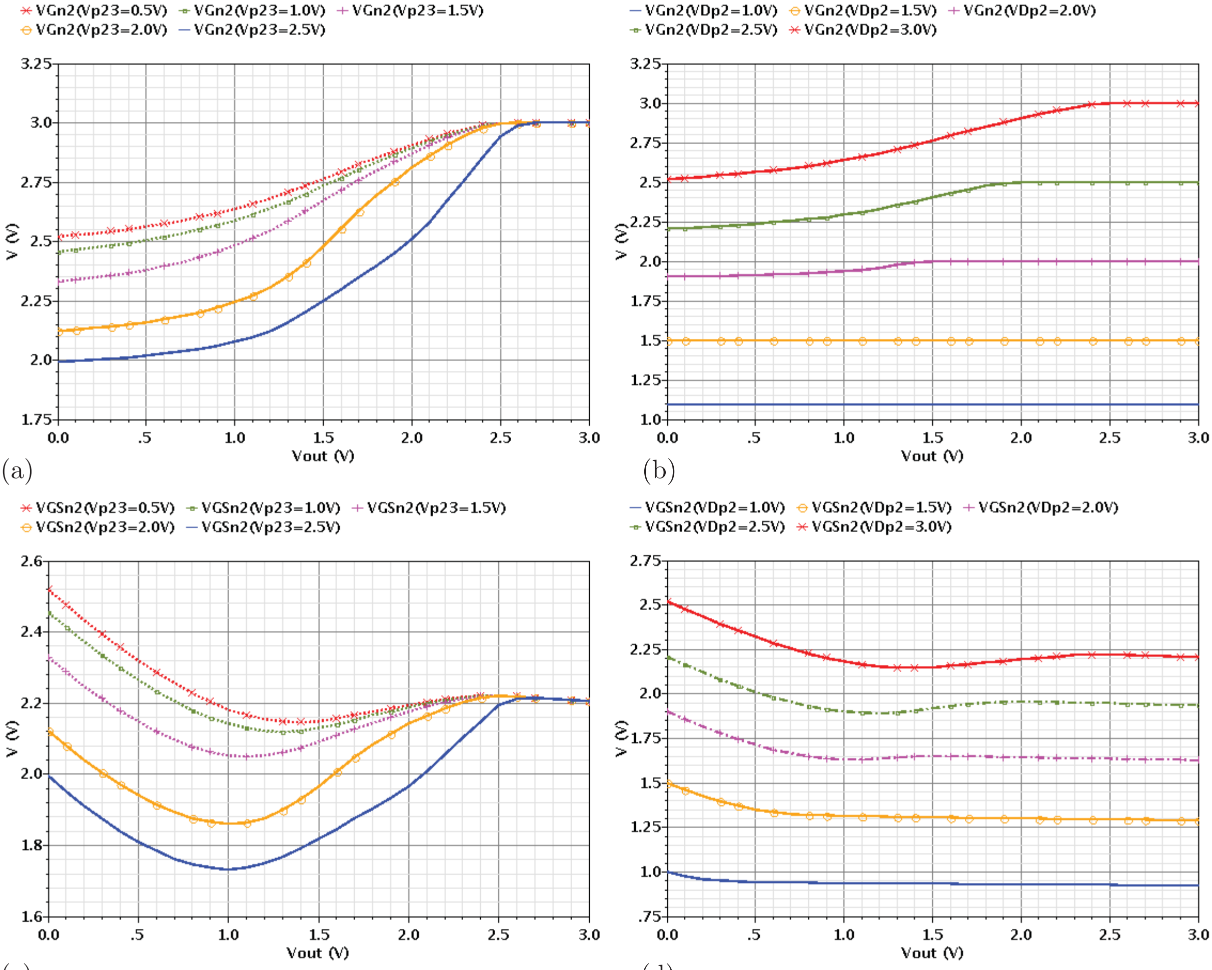


Figure 4.24: The provided node voltages of Mn2 versus *Vout* in the on-state (*VHdd*=3.0 V)

the maximum current can flow in the pull-up and as well in the pull-down path when the gate voltage of each stacked transistor has an offset of Vn (2.5 V) to the corresponding source voltage. However, the reference voltages (Vp_{23} and Vn_{23}), and the high and low supply rail voltages (VD_{p2} and VD_{n2}) of the circuits GC$_{\text{n2}}$ and GC$_{\text{p2}}$ affect the provided gate voltages VG_{n2} and VG_{p2} and consequently the current driving in the pull-down and pull-up paths. For driving the maximum current, Vp_{23}, Vn_{23}, VD_{p2} and VD_{n2} should be set at 0.5 V, 2.5 V, 3.0 V and 0 V, respectively depending on the on- or off-state. In the next step, by varying these parameters, it can be seen how the provided gate voltages VG_{n2} and VG_{p2} change and as a result the current, on-resistance, and rise and fall times are negatively affected. In the on-state (pull-down active), by increasing the gate voltage of m$_{\text{2x}}$ (Vp_{23}) from 0.5 V to 2.5 V, the provided gate voltage characteristics VG_{n2} reduce, as shown in Figure 4.25a. Furthermore, by decreasing VD_{p2} from 3.0 V to 1.0 V, VG_{n2} drops down from 3.0 V to 1.1 V (Figure 4.25b).



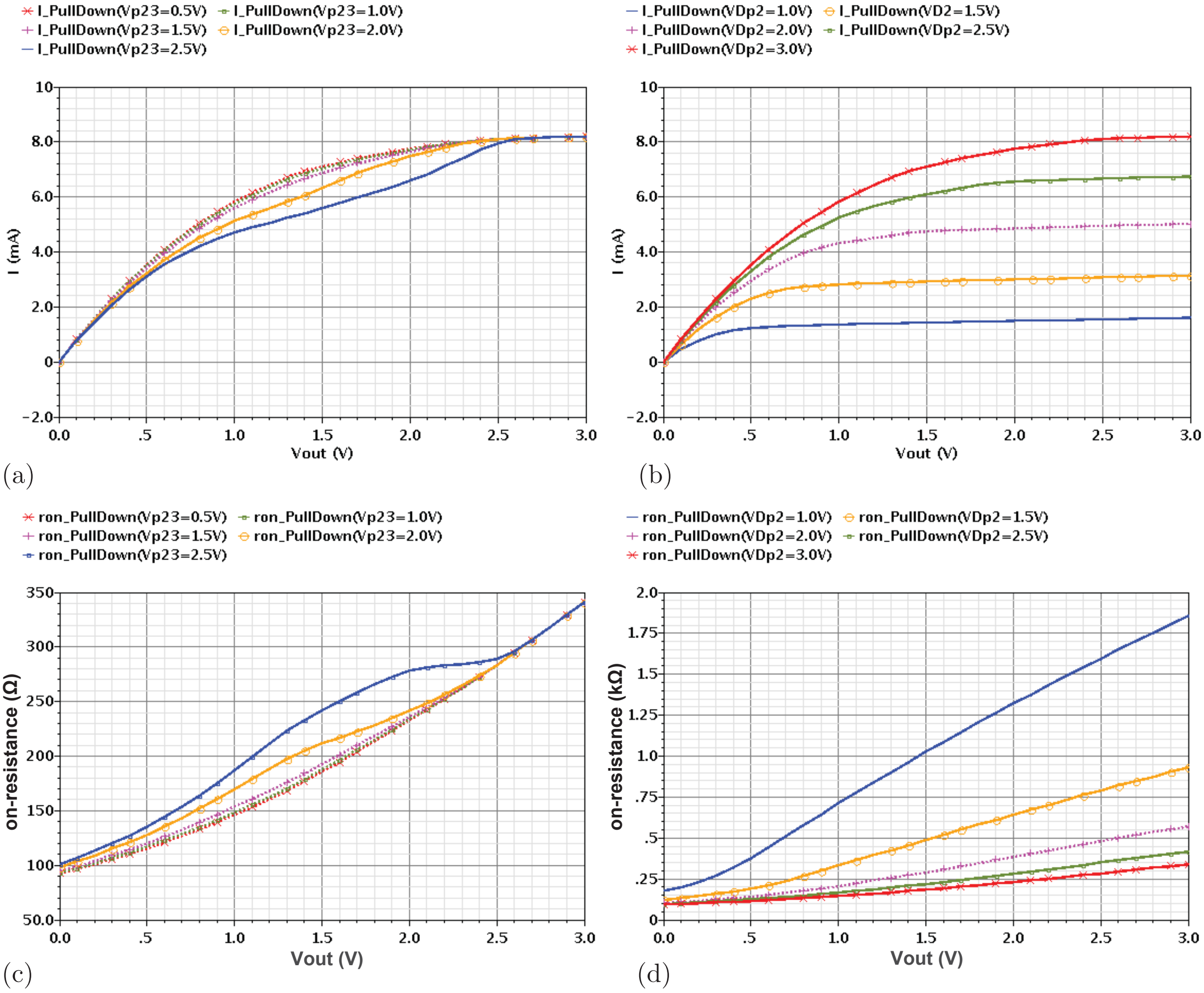
(a) (b)

(c) (d)

Figure 4.25: The DC-characteristics of (a), (b) the gate voltage VG_{n2}, (c), (d) the gate-source voltage VGS_{n2} of the transistors Mn2 according to different values of Vp_{23} and VD_{p2} ($VHdd$=3.0 V and Vin=2.5 V)

Consequently, the gate-source voltage of Mn2 (VGS_{n2}) reduces, as is evident in Figures 4.25c and 4.25d, respectively. As expected, the pull-down current is lowered (Figures 4.26a and 4.26b) and as a result, the on-resistance of the pull-down rises, as shown in Figures 4.26c and 4.26d. Consequently, the discharging of the driver output load is becoming slower, as can be seen from the fall times in Table 4.2. It is evident that the pull-down path has the lowest on-resistance due to the provided gate voltage VG_{n2} with Vp_{23} of 0.5 V and VD_{p2} of 3.0 V. Therefore the maximum current drives in the pull-down path with these parameters. The pull-down on-resistance with these ideal voltages varies from 340 Ω to 96 Ω, whereas with VD_{p2} of 1.0 V, it changes from 1.85 kΩ to 0.176 kΩ, while the output node discharges from 3.0 V to ground.

In the off-state (pull-up active), the gate voltage of m_{2y} (Vn_{23}) is decreased from the ideal setting value of 2.5 V to 0.5 V and the lower rail voltage of GC_{p2} (VD_{n2}) is increased from the ideal voltage of 0 V to 2.0 V respectively, which raises the provided gate voltage



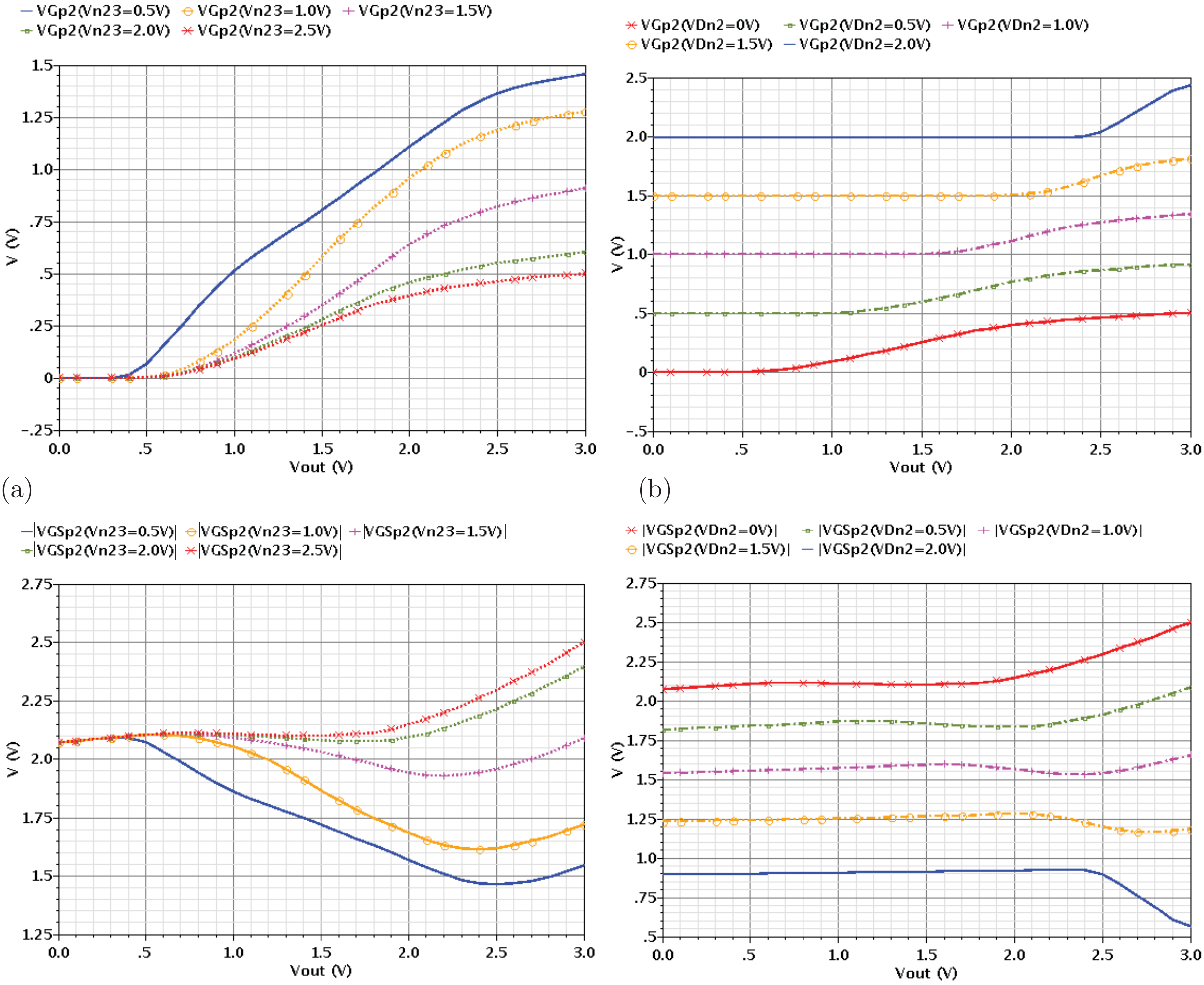
(a) (b) (c) (d)

Figure 4.26: The DC-characteristics of (a), (b) the pull-down current, (c) and (d) the pull-down on-resistance according to different values of Vp_{23} and VD_{p2} ($VHdd$=3.0 V and Vin=2.5 V)

VG_{p2}, as illustrated in Figures 4.27a and 4.27b.

Following this, the absolute value of the gate-source voltage of Mp2 (VGS_{p2}) reduces (Figures 4.27c and 4.27d) and due to that effect, the current of the pull-up path decreases, as shown in Figures 4.28a and 4.28b. Consequently, the on-resistance of the pull-up path rises (Figures 4.28c and 4.28d), leading to a longer time to charge the driver output load, as can be seen from the rise times in Table 4.2.

From these results, it can be observed that the provided VG_{p2}, after setting the parameters Vn_{23} and VD_{n2} at 2.5 V and 0 V respectively, drives the maximum current in the off-state and the pull-up path has the minimum on-resistance. As a result, the rise time of $Vout$ is minimal (Table 4.2).



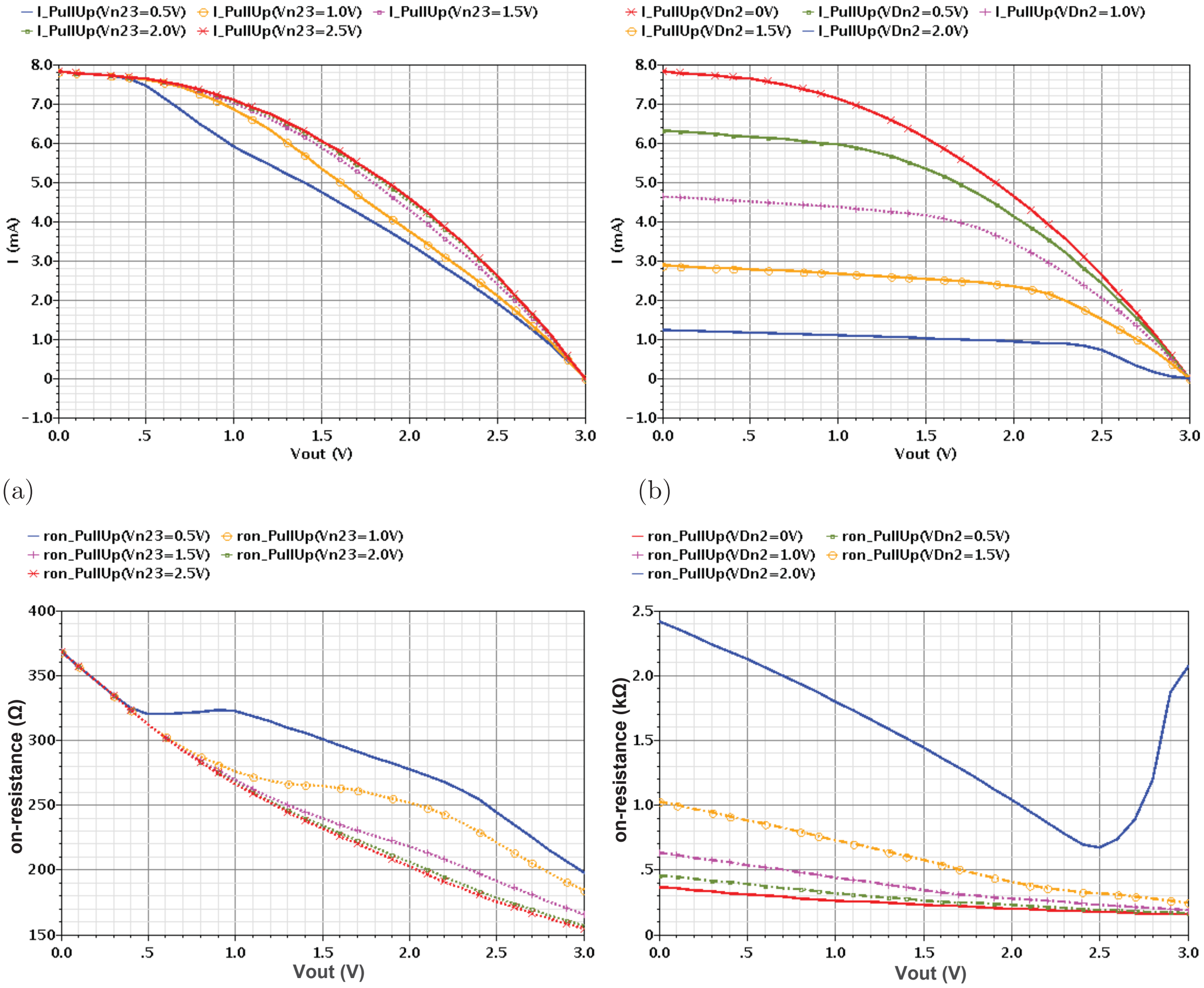
(a) (b)

(c) (d)

Figure 4.27: The DC-characteristics of (a), (b) the gate voltage VG_{p2}, (c) and (d) the gate-source voltage VGS_{p2} of Mp2 according to different values of Vn_{23} and VD_{n2} ($VHdd$= 3.0 V and Vin=0 V)

Table 4.2: Rise (RT) and fall (FT) time of the output voltage according to the different values of the influencing reference voltages (C_L=150 pF)

$Vn_{23\text{-}off}$ [V]	$VD_{n2\text{-}off}$ [V]	RT [ns]	$Vp_{23\text{-}on}$ [V]	$VD_{p2\text{-}on}$ [V]	FT [ns]
2.5	0	77.3	0.5	3.0	63.3
0.5	0	98.3	2.5	3.0	75.4
2.5	1.0	109.5	0.5	2.0	87.6
1.0	1.0	153.3	2.0	2.0	114.0



(a) (b)

(c) (d)

Figure 4.28: The DC-characteristics of (a), (b) the pull-up current, (c) and (d) the pull-up on-resistance according to different values of Vn_{23} and VD_{n2} ($VHdd$=3.0 V and Vin=0 V)

4.1.3 Comparison with Work B

In this section, the designed 2-stacked CMOS HV-driver, which is termed in this subsection as work *A*, is compared to the published work *B* described in [31], in which the gate voltages of VG_{n2} and VG_{p2} of an *N*-stacked CMOS HV-driver are set at the constant value of *Vdd*, expressing the nominal voltage of standard transistors, which is equal to 2.5 V in the process technology used in this work (Figure 4-29). The supply voltage is a multiple of the nominal voltage and defined as $N \times Vdd$. The dimensions of the stacked CMOS transistors of work *B* are set identical to those of HV-driver *A*.

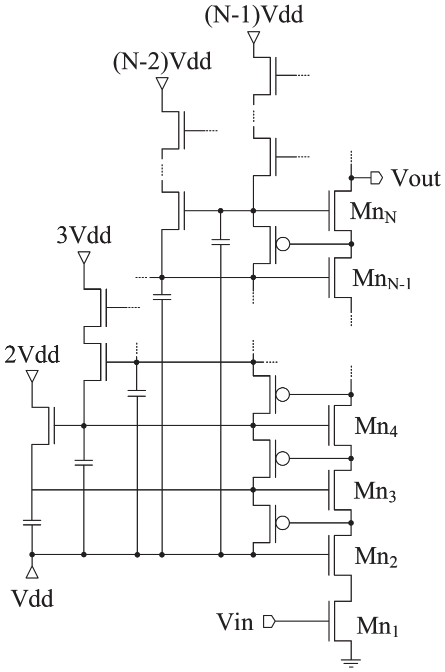
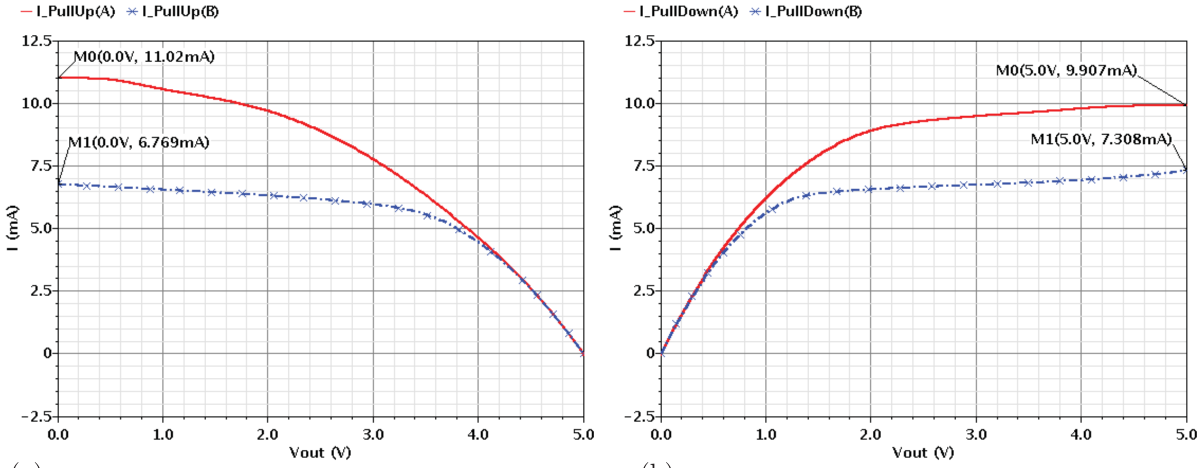


Figure 4.29: Bias circuit for the nMOS transistors of the *N*-stacked CMOS driver *B* [31]

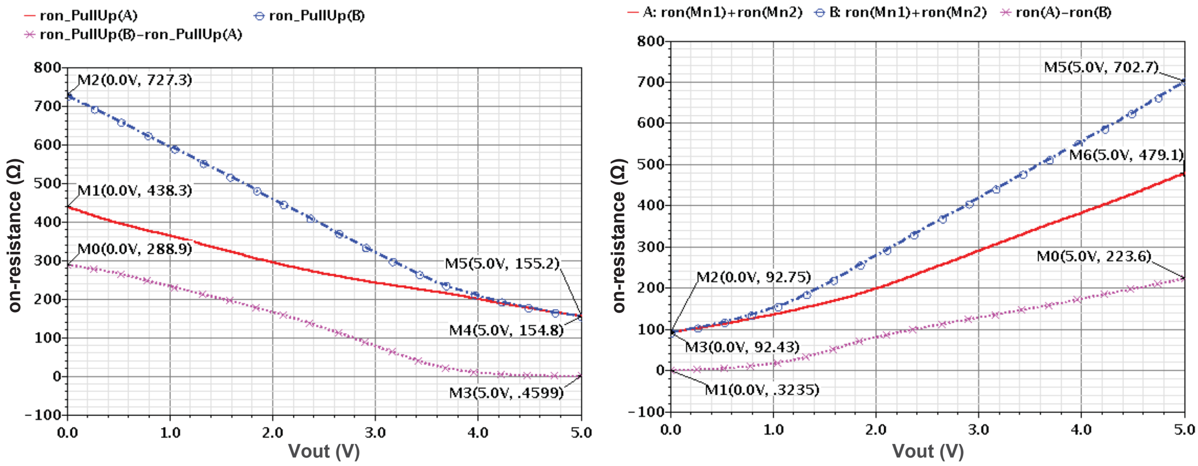
Figures 4.30a and 4.30b depict the pull-up and pull-down path current characteristics of both works (*A* and *B*) versus *Vout* in terms of charging and discharging the driver output node. As can be seen, the nMOS transistors and also pMOS transistors of this work (*A*) drive a current higher than the current of work *B*. For example, the initial currents of the pull-up and pull-down paths of work *A* are respectively around 4.3 mA (ca. 63%) and 2.6 mA (ca. 36%) higher than those of the HV-driver *B*.

Considering the fact of a higher current due to the provided gate voltages driving transistors, it was expected, that the on-resistance would be reduced. The Figures 4.31a and 4.31b, which indicate the on-resistance characteristics of the pull-up and pull-down transistors (ron_PullUp and ron_PullDown) of both circuits (*A* and *B*) and their differences, illustrate this fact.



(a) (b)

Figure 4.30: (a) Pull-up currents in the off-state and (b) pull-down currents in the on-state of the HV-driver A and B ($VHdd$=5.0 V)



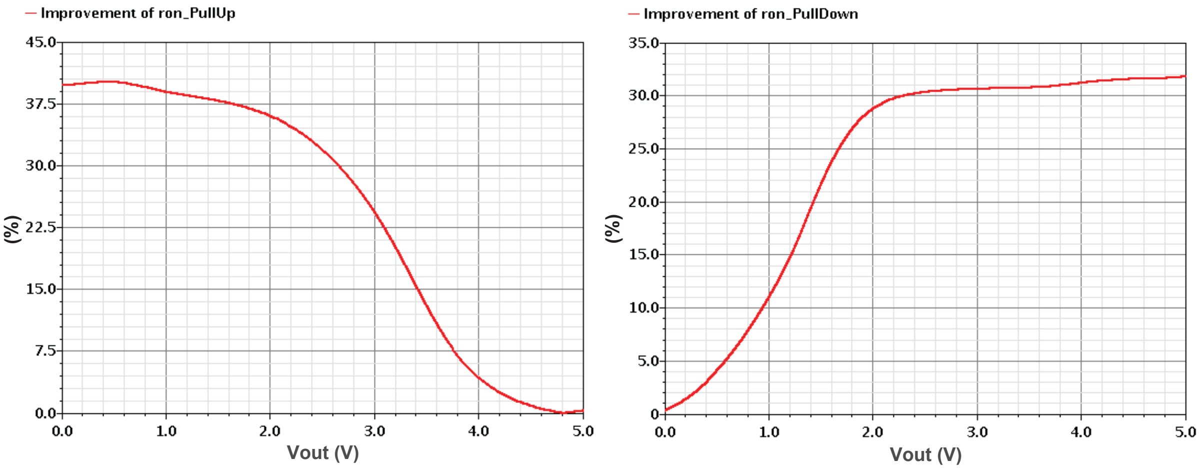
(a) (b)

Figure 4.31: On-resistances of the (a) pull-up path in the off-state and (b) pull-down path in the on-state of the HV-driver A and B ($VHdd$=5.0 V)

The initial on-resistances of the pull-up and pull-down paths are improved by about 40% and 32% respectively when compared to B, as shown in Figures 4.32a and 4.32b respectively. During charging of the output node from 0 V to about 3.2 V, the improvement of the pull-up on-resistance is over 21% (Figure 4.32a), whereas the improvement of the pull-down on-resistance is over 20%, when the output node discharges from 5.0 V to 1.4 V (Figure 4.32b).

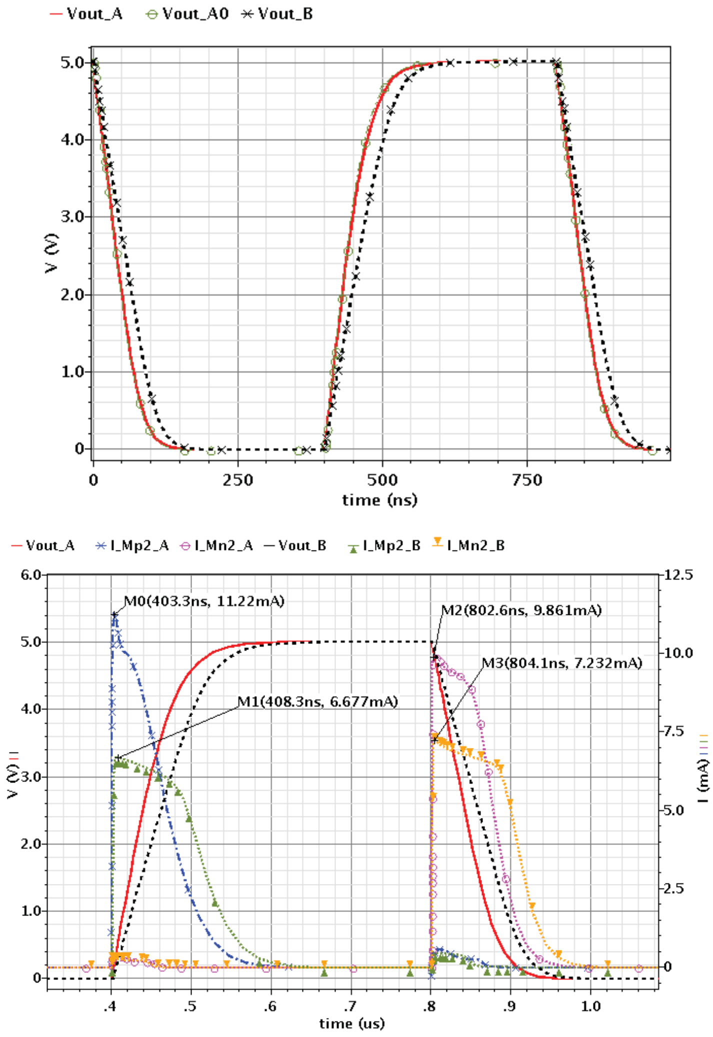
Figure 4.33a compares the output signals of the designed 2-stacked CMOS driver (A) with the published work (B). Both circuits are supplied with 5.0 V.

The output signal of the initial HV-driver (A_0) designed without the extra transistors m_{2x}, m_{2y} and capacitors is also depicted. Its delay, fall and rise times have a slight difference by about 4% in comparison to the driver's output of work A. The transient



(a) (b)

Figure 4.32: The improvement of the (a) pull-up on-resistance in the off-state and (b) pull-down on-resistance in the on-state of this work compared to work *B*



(a)

(b)

Figure 4.33: (a) Transient output voltage characteristics, (b) the pull-up and pull-down currents of the HV-drivers *A* and *B* with a load capacitance of 150 pF ($VHdd$= 5.0 V)

output voltage, and the pull-up and pull-down current characteristics of works *A* and *B* are displayed in Figure 4.33b. At the beginning of switching, a higher current flows in the pull-up and pull-down paths of work *A* during charging and discharging the output load capacitance of 150 pF. Consequently, the switching of the driver *A* is faster than that of *B*.

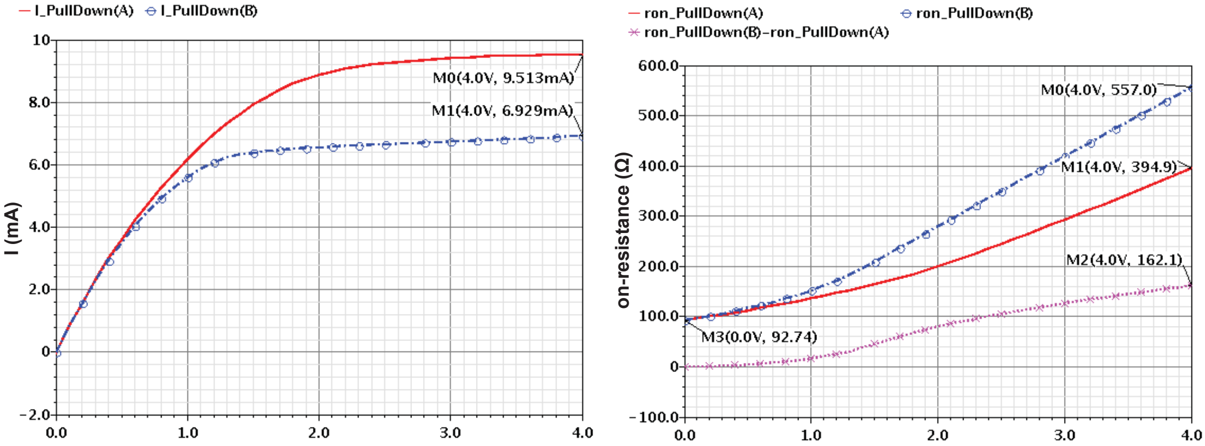
Table 4.3 gives a comparison view between rise time (*RT*), fall time (*FT*), delays (d_1, d_2 and d_m), initial pull-up and pull-down currents (I_p and I_n) and on-resistances (*ron*) of both works *A* and *B*. The term d_1 is defined for the delay between the falling edge of the output and the rising edge of the input signals. The delay between rising edge of *Vout* and falling edge of *Vin* and the average delay are expressed as d_2 and d_m, respectively. The parameters ($\mathrm{delay_m}$, rise and fall times) of circuit *A* are improved by 33%, 21% and 20% when respectively compared to driver *B*. The circuits are loaded with a capacitance of 150 pF.

Table 4.3: Rise and fall times, delays, pull-up and pull-down currents and on-resistances of the designed HV-driver (*A*) and work *B* with a load capacitance of 150 pF

VHdd	*work*	*FT[ns]*	*RT[ns]*	d_1*[ns]*	d_2*[ns]*	*pull-up*		*pull-down*	
						$I_p[mA]$	$ron[\Omega]$	$I_n[mA]$	$ron[\Omega]$
5.0 V	*A*	78.5	87.7	41.8	38.9	11.0	438	9.9	479
				$d_m = 40.3$					
	B	98.4	110.9	58.5	61.2	6.8	727	7.3	702
				$d_m = 59.9$					
improvement		20%	21%	29%	36%	61.8%	39.8%	35.6%	31.8%
				$d_m = 33\%$					

As previously mentioned, the published work *B* is designed for a supply voltage that it is a multiple of the nominal voltage. However, both drivers, *A* and *B*, are compared for lower supply voltages. The delay, rise and fall times, and the on-resistance of work (*A*) are also significantly better than these parameters of the work *B*.

Figures 4.34a and 4.34b represent comparisons between the current and on-resistance characteristics of the pull-down path of both works *A* and *B* during discharging of the driver node from 4.0 V to ground. Both HV-drivers are supplied with 4.0 V. This entails reduced delay, rise and fall times of the output signal, which are about 57%, 56% and 17% respectively. Table 4.4 shows the comparison of delay, rise and fall times, initial on-resistance, initial pull-up and pull-down currents between both drivers with a supply voltage of 4.0 V. Driving a higher current in the pull-down path of *A*, with an initial improvement of 38%, indicates a lower on-resistance with an improvement up to 30% in comparison with work *B*, as can be observed in Figure 4.35.



(a) (b)

Figure 4.34: The pull-down (a) on-resistances and (b) currents of the HV-drivers *A* and *B* in the on-state (*VHdd*=4.0 V)

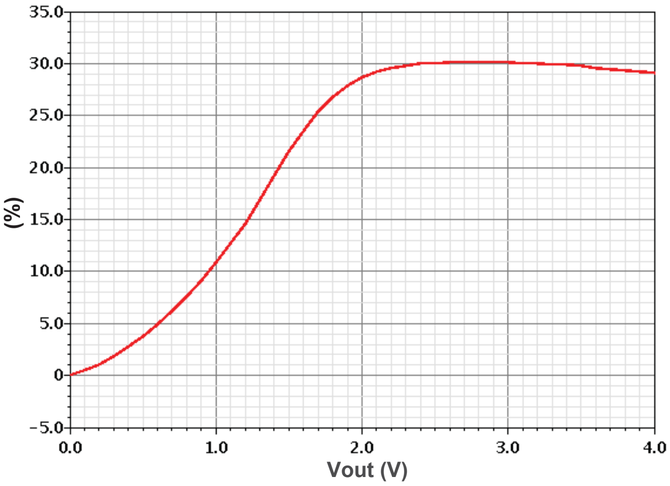


Figure 4.35: The on-resistance improvement of the HV-driver *A* over the previous one, *B*, in the on-state (*VHdd*=4.0 V)

Table 4.4: Rise and fall times, delays, pull-up and pull-down currents and on-resistances of the drivers *A* and *B* with a load capacitance of 150 pF

VHdd	*work*	*FT[ns]*	*RT[ns]*	d_1*[ns]*	d_2*[ns]*	*pull-up*		*pull-down*	
						$I_p[mA]$	$ron[\Omega]$	$I_n[mA]$	$ron[\Omega]$
4.0 V	*A*	68.2	84.4	34.0	34.0	10.1	382	9.5	395
				$d_m = 34.0$					
	B	82.3	193.4	47.2	110	3.1	1.3 k	6.9	557
				$d_m = 78.6$					
improv. [%]		17.1	56.3	28	69	226	70.5	37.6	29
				$d_m = 56.7$					

From these and previous results, it is evident that the designed 2-stacked CMOS HV-driver *A* based on the rules presented in Equations (3.11), (3.23), (3.24), (3.33), (3.34) and (3.35) has significantly higher currents driving in the pull-up and pull-down paths. As expected, it has markedly improved on-resistance and therefore switches faster than circuit *B*.

The pull-up and pull-down on-resistances of this HV-driver (*A*) can be further improved when the transistor dimensions of the gate-controlling circuits $\mathrm{GC_{n2}}$ and $\mathrm{GC_{p2}}$ are adjusted separately for each applied supply voltage. In this case, the circuit would not be suitable for a wide range of supply voltages between 2.5 V and 5.0 V, but it could be used for a small range of supply voltages.

4.2 Circuit Design of a 3-stacked CMOS HV-driver

Regarding the design of the gate-controlling circuits as described in Chapter 3, a 3-stacked CMOS HV-driver is designed for supply voltages in the range between 5.0 V–7.5 V (5.0 V < $VHdd \leq$ 7.5 V), as illustrated in Figure 4.36. The maximum applied supply voltage of 7.5 V is three times the nominal voltage (2.5 V) of transistors used in this work.

The stage HV-driver contains three pMOS transistors (Mp1, Mp2 and Mp3) in the pull-up path and three nMOS transistors (Mn1, Mn2 and Mn3) in the pull-down path. The supply high-voltage is termed as *VHdd*. The control signal *Vin* is buffered from the system input signal Vin_g due to two inverters *Inv1* and *Inv2* to drive the transistor Mn1, whereas Mp1 is controlled by *Vpin*, which is level-shifted up from *Vin* using two level-shifters *LS2* and *LS3* obtained from [30]. These circuits will be presented in Chapter 6.

The circuit of the designed HV-driver contains four different gate-controlling circuits $\mathrm{GC_{n2}}$, $\mathrm{GC_{n3}}$, $\mathrm{GC_{p2}}$ and $\mathrm{GC_{p3}}$ to provide gate voltages VG_{n2}, VG_{n3}, VG_{p2} and VG_{p3} for the transistors Mn2, Mn3, Mp2 and Mp3, respectively. According to the rules of Equations (3.11) and (3.33) and circuit design methodology presented in Chapter 3, these circuits should drive the maximum currents in the pull-up and pull-down paths for a supply voltage of 7.5 V. For lower supply voltages greater than 5.0 V, the provided gate voltages should approach the theories in Equations (3.23), (3.24), (3.34) and (3.35) to drive nearly the maximum current.

The same circuits, $\mathrm{GC_{n2}}$ and $\mathrm{GC_{p2}}$, with the corresponding switches $\mathrm{SW\_VD_{n2}}$, $\mathrm{SW\_VD_{p2}}$, $\mathrm{SW\_Vp_{23}}$ and $\mathrm{SW\_Vn_{23}}$, which are designed for the 2-stacked CMOS HV-driver in the previous chapter, are used for this driver. The gates of $\mathrm{mp_{22}}$ and $\mathrm{mn_{22}}$ are regulated by the nodes $\mathrm{S_{n3}}$ and $\mathrm{S_{p3}}$, respectively. Furthermore, the dimensions of transistors are adjusted to the operation of the circuit avoiding any overvoltage. The

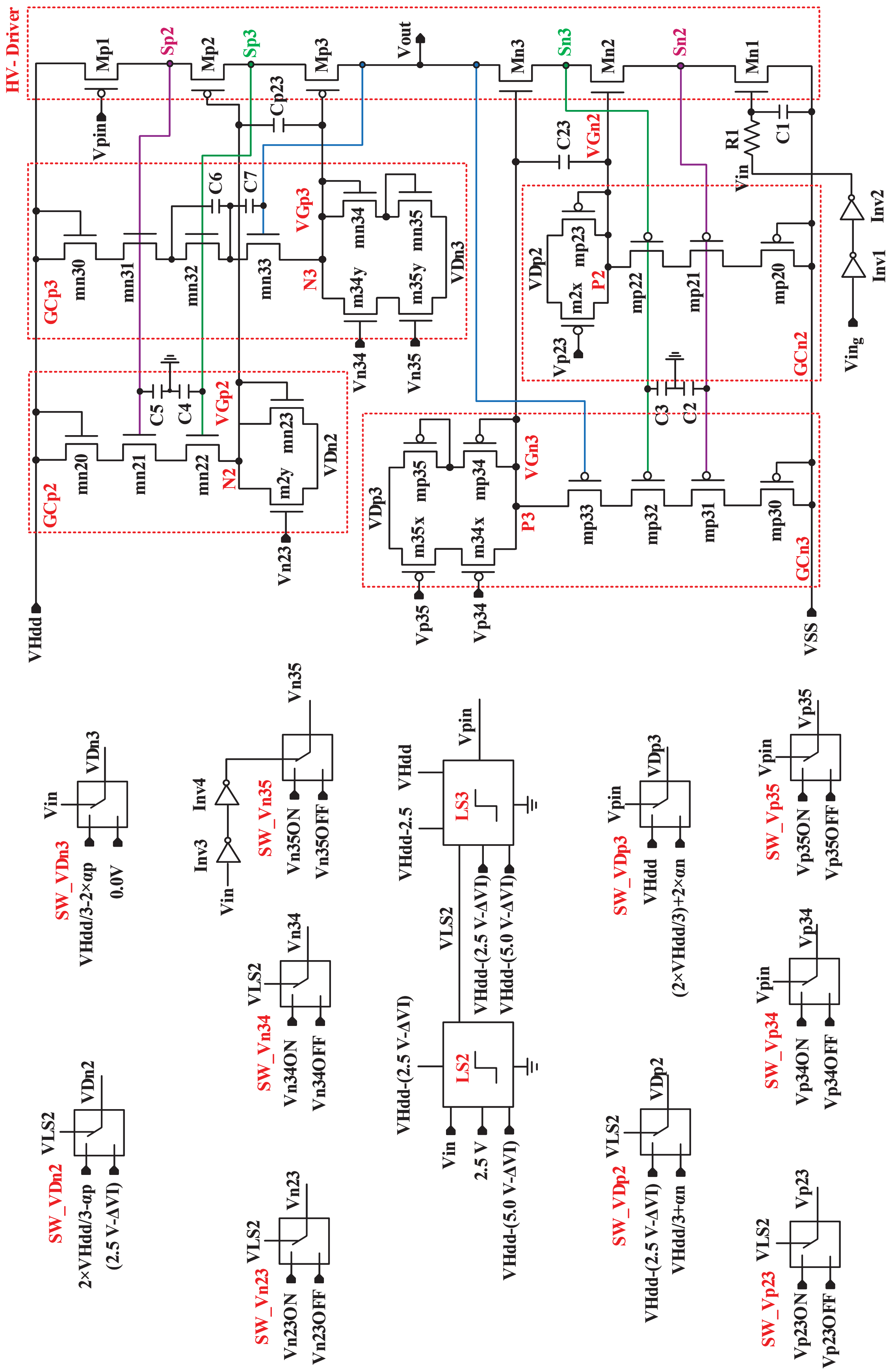


Figure 4.36: Circuit design of the designed 3-stacked CMOS HV-driver

output signal V_{LS2} of the first level-shifter ($LS2$) controls the switches SW_VD$_{\mathrm{n2}}$ and SW_VD$_{\mathrm{p2}}$. Consequently, the reference voltages "$(2\times VHdd/3)–\alpha_p$" of switch SW_VD$_{\mathrm{n2}}$ and "$VHdd–(2.5\text{ V}–\Delta V_I)$" of SW_VD$_{\mathrm{p2}}$ are delivered to the switches' outputs VD_{n2} and VD_{p2}, respectively in the on-state. In the off-states, VD_{n2} and VD_{p2} are referred to "$2.5\text{ V}–\Delta V_I$" and "$(VHdd/3)+\alpha_n$", respectively.

According to the signal levels of V_{LS2}, the reference voltages Vn_{23ON} and Vn_{23OFF} regulate the extra transistor m2y of the gate-controlling circuit GC$_{\mathrm{p2}}$ in the on- and off-state respectively, whereas m$_{\mathrm{2x}}$ of GC$_{\mathrm{n2}}$ is referred to Vp_{23ON} and Vp_{23OFF}.

To provide the low and high rail voltages VD_{n3} and VD_{p3} of GC$_{\mathrm{p3}}$ and GC$_{\mathrm{n3}}$ in terms of on- and off-states, two switches SW_VD$_{\mathrm{n3}}$ and SW_VD$_{\mathrm{p3}}$ are designed with a control signal Vin and $Vpin$, respectively. In the on-state, VD_{n3} and VD_{p3} are referred to the reference voltages "$(VHdd/3)–2\times\alpha_p$" and $VHdd$, whereas in the off-state, they are connected to the reference voltages 0 V and "$(VHdd/3)+2\times\alpha_n$", respectively.

Additionally, four switches SW_Vp$_{34}$, SW_Vp$_{35}$, SW_Vn$_{34}$ and SW_Vn$_{35}$ are designed for regulating the extra transistors m$_{\mathrm{34x}}$, m$_{\mathrm{35x}}$, m$_{\mathrm{34y}}$ and m$_{\mathrm{35y}}$, respectively. The level-shifted signal $Vpin$ controls the first two switches (SW_Vp$_{34}$ and SW_Vp$_{35}$) to operate the appropriate transistors with the respective reference voltages Vp_{34ON} and Vp_{35ON} or Vp_{34OFF} and Vp_{35OFF} in terms of on- and off-states. The last both switches, SW_Vn$_{34}$ and SW_Vn$_{35}$, are controlled respectively with V_{LS2} and Vin passing the reference voltages Vn_{34ON} and Vn_{35ON} or Vn_{34OFF} and Vn_{35OF} to regulate the transistors m$_{\mathrm{34y}}$ and m$_{\mathrm{35y}}$.

As previously mentioned, each switch is formed by two transmission gates (TG) with a control signal passing a required reference voltage as an input signal to the output. Each transmission gate contains an nMOS and a pMOS transistor [61], and each inverter contains an nMOS (*nMOS_Inv*) and a pMOS (*pMOS_Inv*) transistor. The parameters of the resistors, capacitors and widths of transistors are given in Table 4.5. The length of each transistor is determined to be 280 nm. The transmission gates of the switches are termed as TG_{on} and TG_{off}, which pass a suitable reference voltage for the on- and off-state. The widths of their transistors are also indicated in this table.

The gate-drain connected transistors mp$_{30}$ and mn$_{30}$ are added in series to the circuits GC$_{\mathrm{n3}}$ and GC$_{\mathrm{p3}}$, respectively to prevent an overvoltage. Two low-pass filters (R_{p1}/C_{p1} and R_1/C_1) adjust the input signals $Vpin$ and Vin to the pull-up and pull-down node voltages during charging and discharging to prevent an overvoltage across terminals of the transistors Mn1 and Mp1.

In the next steps, the operation of the circuit will be proven and analysed for two groups of supply voltages: one is equal to three times the nominal voltage (7.5 V) and the other is between 5.0 V and 7.5 V (indivisible by 2.5 V).

Table 4.5: Resistors, capacitors and transistors' widths of the designed 3-stacked CMOS driver

pull-down path	**pull-up path**	$\mathbf{GC_{n2}}$				
Mn1, Mn2, Mn3	*Mp1, Mp2, Mp3*	mp_{20}	mp_{21}	mp_{22}	mp_{23}	mp_{2x}
16 μm	48 μm	250 μm	250 μm	32 μm	32 μm	32 μm

$\mathbf{SW\_VD_{p2}}$			$\mathbf{SW\_VD_{n2}}$		$\mathbf{GC_{p2}}$				
TG	*nMOS*	*pMOS*	*nMOS*	*pMOS*	mn_{20}	mn_{21}	mn_{22}	mn_{23}	mn_{2y}
TG_{on}	320 μm	320 μm	10 μm	320 μm	320 μm	320 μm	28 μm	27 μm	8 μm
TG_{off}	320 μm	320 μm	320 μm	10 μm					

$\mathbf{SW\_VD_{p3}}$			$\mathbf{SW\_VD_{n3}}$		$\mathbf{SW\_Vp_{23}}$		$\mathbf{SW\_Vn_{23}}$	
TG	*nMOS*	*pMOS*	*nMOS*	*pMOS*	*nMOS*	*pMOS*	*nMOS*	*pMOS*
TG_{on}	320 μm	320 μm	1 μm	320 μm	16 μm	160 μm	16 μm	48 μm
TG_{off}	320 μm	320 μm	320 μm	1 μm	64 μm	160 μm	16 μm	48 μm

$\mathbf{SW\_Vp_{34}}$			$\mathbf{SW\_Vp_{35}}$		$\mathbf{SW\_Vn_{34}}$		$\mathbf{SW\_Vn_{35}}$	
TG	*nMOS*	*pMOS*	*nMOS*	*pMOS*	*nMOS*	*pMOS*	*nMOS*	*pMOS*
TG_{on}	16 μm	160 μm	16 μm	160 μm	16 μm	48 μm	16 μm	48 μm
TG_{off}	64 μm	160 μm	64 μm	160 μm	16 μm	48 μm	16 μm	48 μm

$\mathbf{GC_{n3}}$							
mp_{30}	mp_{31}	mp_{32}	mp_{33}	mp_{34}	mp_{35}	mp_{34x}	mp_{35x}
250 μm	250 μm	32 μm	32 μm	16 μm	16 μm	16 μm	16 μm

$\mathbf{GC_{p3}}$							
mn_{30}	mn_{31}	mn_{32}	mn_{33}	mn_{34}	mn_{35}	mn_{34y}	mn_{35y}
270 μm	270 μm	270 μm	25 μm	24 μm	24 μm	33 μm	16 μm

$\mathbf{Inv_1}$, $\mathbf{Inv_2}$, $\mathbf{Inv_3}$, $\mathbf{Inv_4}$	
nMOS_Inv	*pMOS_Inv*
100 μm	100 μm

passive components									
R_1	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_{23}	C_{p23}
7 kΩ	0.02 pF	16 pF	16 pF	5 pF	30 pF	0.2 pF	0.3 pF	0.3 pF	1 pF

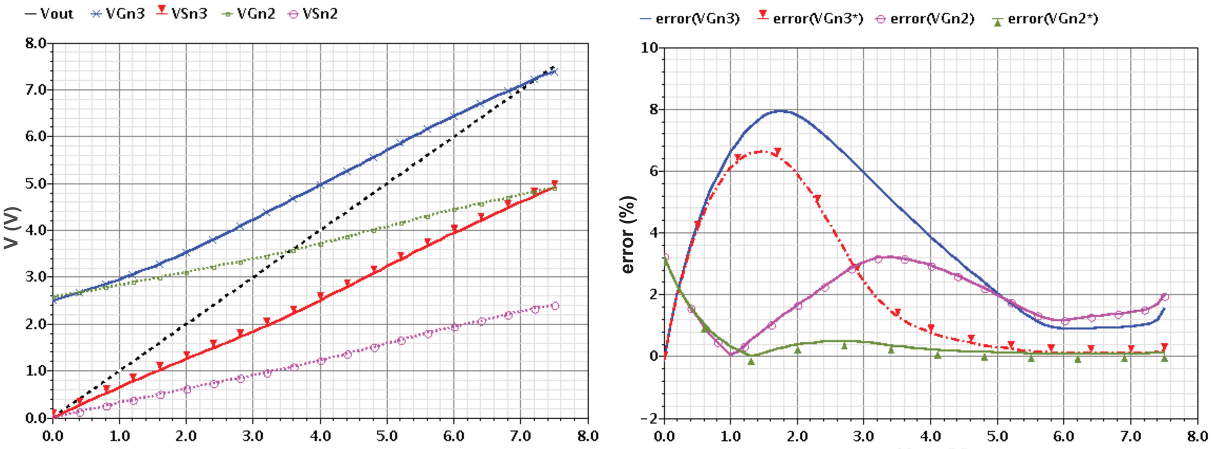
4.2.1 Operational Analysis for VHdd of 7.5 V

In this sub-section, the circuit operation is analysed due to the DC and transient simulation for a supply voltage of 7.5 V ($3\times Vn$). The provided gate voltages due to the gate-controlling circuits are compared with the theories presented in Equations (3.11) and (3.33).

4.2.1.1 DC Analysis: Active Driver-Paths

In the initial design phase, the transistors $\mathrm{m_{2x}}$, $\mathrm{m_{34x}}$, $\mathrm{m_{35x}}$, $\mathrm{m_{2y}}$, $\mathrm{m_{34y}}$ and $\mathrm{m_{35y}}$ are not considered. The designed HV-driver is controlled at first in the on-state with the input signals *Vin* of 2.5 V and *Vpin* of 7.5 V with a supply voltage of 7.5 V.

Figure 4.37a shows the pull-down node voltage characteristics VG_{n2}, VG_{n3}, *Vout*, VS_{n3} and VS_{n2} versus *Vout*, which are obtained from the DC simulation results. The output node discharges from 7.5 V to ground. The provided gate voltages of Mn2 and Mn3 and also the pull-down node voltages approximately follow the rules in Equations 3.10 and 3.11. The characteristics of *VG_{n2}* and *VG_{n3}* approach lines passing through the points (0 V, 2.5 V) and (7.5 V, 5.0 V) and the points (0 V, 2.5 V) and (7.5 V, 7.5 V), respectively. Due to these provided gate voltages, the discharging of the pull-down nodes (*VS_{n2}* and *VS_{n3}*) nearly track the lines from 5.0 V and 2.5 V to ground, respectively.



(a) (b)

Figure 4.37: (a) The DC node voltage characteristics of Mn2 and Mn3 of the designed 3-stacked CMOS driver and (b) the errors between the provided and the ideal gate-voltages vs. *Vout* (*VHdd*= 7.5 V and pull-down active)

Figure 4.37b illustrates the errors between the provided and the required gate voltages regarding Equation (3.11). They are expressed as *error(VG_{n2})* and *error(VG_{n3})* with a maximum of ca. 3% and 8%, respectively. The terms *error(VG_{n2}*)* and *error(VG_{n3}*)* express how the provided gate voltages deviate from the appropriated source voltage with an offset of 2.5 V as follows:

$$error(VG_{n2}*) = \frac{|VG_{n2} - (VS_{n2} + 2.5\,V)|}{VS_{n2} + 2.5\,V} \times 100 \tag{4.3a}$$

$$error(VG_{n3}*) = \frac{|VG_{n3} - (VS_{n3} + 2.5\,V)|}{VS_{n3} + 2.5\,V} \times 100 \tag{4.3b}$$

The term *error(VG_{n3}*)* has a maximum of ca. 6.5%, while *error(VG_{n2}*)* is small (under 0.5%) when the driver output is discharged from 7.5 V to ca. 0.8 V. However, when *Vout* is discharged to ground, this error increases to 3%.

For the off-state, with the input signals *Vin* of 0 V and *Vpin* of 5.0 V, the DC simulation of the pull-up node voltages *VG_{p2}*, *VG_{p3}*, *Vout*, *VS_{p3}* and *VS_{p2}* versus the output voltage *Vout* are plotted in Figure 4.38. During charging of the output node (*Vout*) from ground to

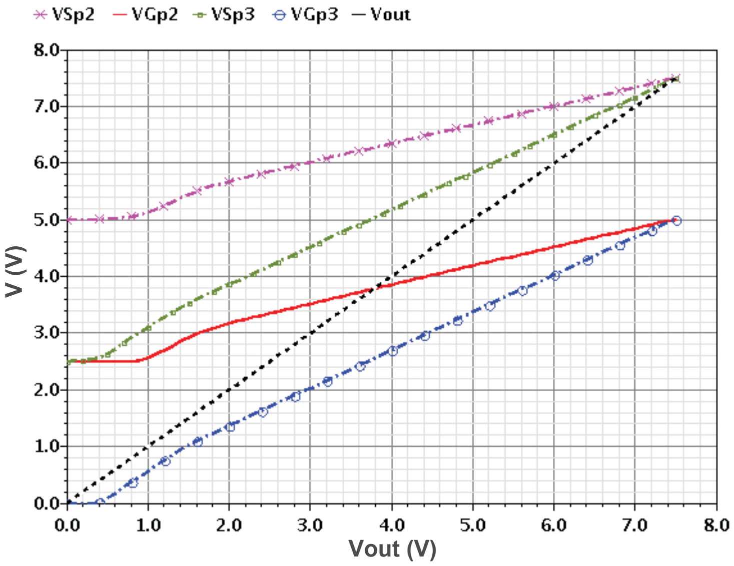


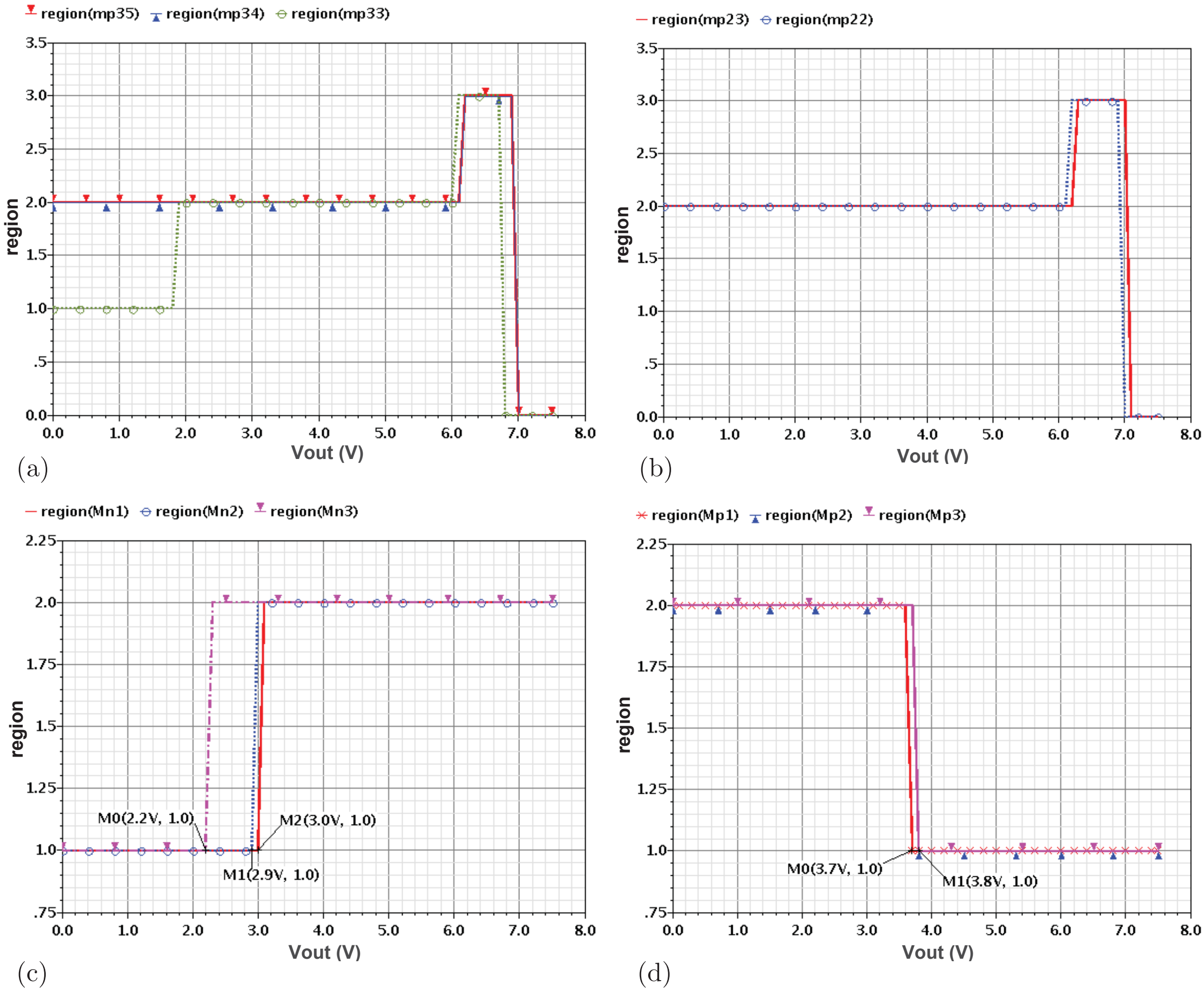
Figure 4.38: The DC node voltage characteristics of Mp2 and Mp3 of the designed 3-stacked CMOS driver vs. *Vout* (*VHdd*=7.5 V and pull-up active)

the supply voltage of 7.5 V, the provided gate voltages VG_{p3} and VG_{p2} have characteristics almost linear from 0 V and 2.5 V, respectively to 5.0 V. The appropriate pull-up nodes (S_{p3} and S_{p2}) charge roughly linearly from 2.5 V and 5.0 V, respectively, to 7.5 V, with an offset of approximately 2.5 V to the corresponding gate voltages, as can be seen from the voltages VS_{p3} and VS_{p2} in Figure 4.38.

4.2.1.2 Reasons for Deviation

As highlighted, each provided gate voltage has a slight difference to the desired voltage. The main reasons for this can be understood by considering the following points:

1. In the on-state, the transistors mp_{33}, mp_{34}, mp_{35}, mp_{22} and mp_{23} of GC_{n3} and GC_{n2}, and in the off-state, the complementary transistors mn_{33}, mn_{34}, mn_{35}, mn_{22} and mn_{23} of the circuits GC_{p3} and GC_{p2} operate not only in the saturation region but also in the cut-off, sub-threshold and, for the transistor mp_{33}, also in the linear region, whereas in the presented circuit design methodology, it is assumed that all these transistors operate only in the saturation region. Figures 4.39a and 4.39b show the operation regions of the above-mentioned transistors of the circuits GC_{n2} and GC_{n3} vs. the driver output voltage *Vout*. As can be seen, the transistor mp_{33} operates further in the linear region ("**1**") for *Vout* in the range between 0 V and 1.8 V. In the *BSIM4* MOSFET model used in Cadence for simulation, the four operation regions of cut-off, linear, saturation and sub-threshold are designated with the numbers **0**, **1**, **2** and **3**.



(a) (b) (c) (d)

Figure 4.39: Operation regions of the transistors (a) mp_{33}, mp_{34}, mp_{35}, (b) mp_{22} and mp_{23}, (c) Mn1, Mn2 and Mn3 in the on-state and (d) Mp1, Mp2 and Mp3 in the off-state ($VHdd$=7.5 V)

2. The calculation gate voltages of the stacked transistors for driving the maximum current in the driver pull-down and pull-up path indicated that the transistors of each path should operate simultaneously in the same operational region (saturation or linear), but conversely it is not the case, as shown in Figures 4.39c and 4.39d.

3. The next reason is that the provided supply voltages VD_{p2} and VD_{p3} of the circuits GC_{n2}, GC_{n3} for the on-state and the provided low supply rail voltages VD_{n2} and VD_{n3} of GC_{p2} and GC_{p3} for the off-state are not uniformly constant, as required. As shown in Figures 4.40a and 4.40b, the voltages VD_{p2}, VD_{p3}, VD_{n2} and VD_{n3}, as provided by the switches SW_VD_{p2}, SW_VD_{p3}, SW_VD_{n2} and SW_VD_{n3}, vary between 50 mV and 100 mV from the ideal constant values of 5.0 V, 7.5 V, 2.5 V and 0 V, respectively.

4. Another reason for the deviation is that the threshold voltages of the transistors in

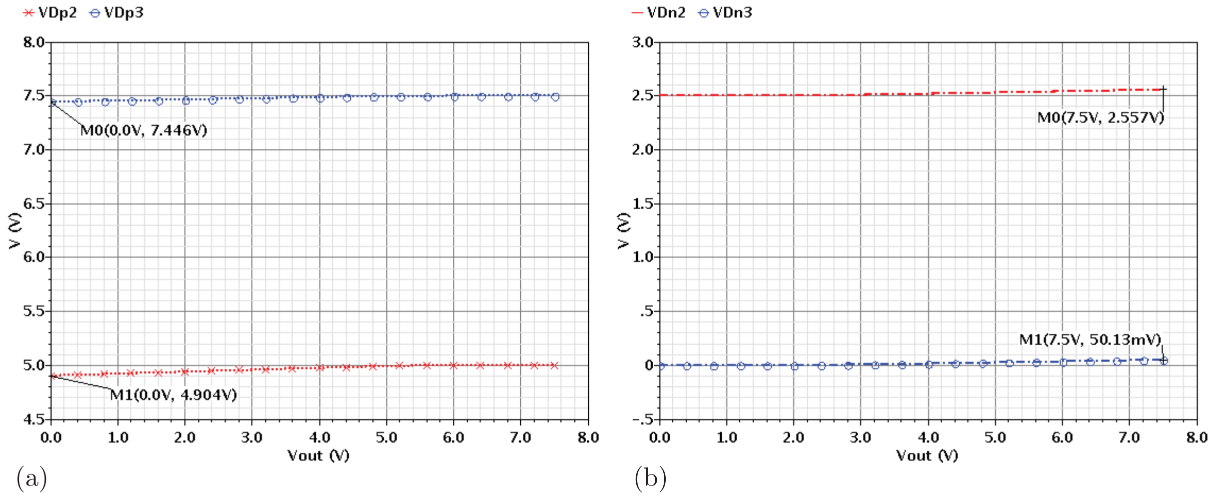


Figure 4.40: The voltage characteristics of (a) VD_{p2}, VD_{p3} in the on-state (b) VD_{n2} and VD_{n3} in the off-state ($VHdd$=7.5 V)

the pull-down path, Mn1, Mn3 and Mn2 (Figure 4.41), and also in the pull-up path, Mp1, Mp2 and Mp3 are unequal to each other. Moreover, the threshold voltages of the transistors of each gate-controlling circuit, which are involved in the calculation for providing the required gate voltages, are not identical, as can be seen from the voltage characteristics of V_{th_mp22} and V_{th_mp23}, the threshold voltages of mp_{22} and mp_{23} in Figure 4.42a and V_{th_mp33}, V_{th_mp34} and V_{th_mp35}, the threshold voltages of mp_{33}, mp_{34} and mp_{35} in Figure 4.42b, which are obtained from the simulation results based on *BSIM4* MOSFET model [66].

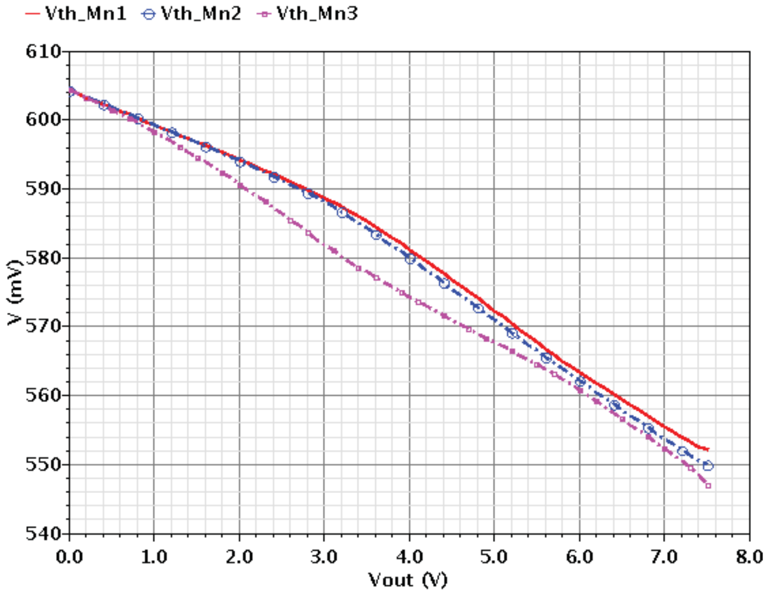
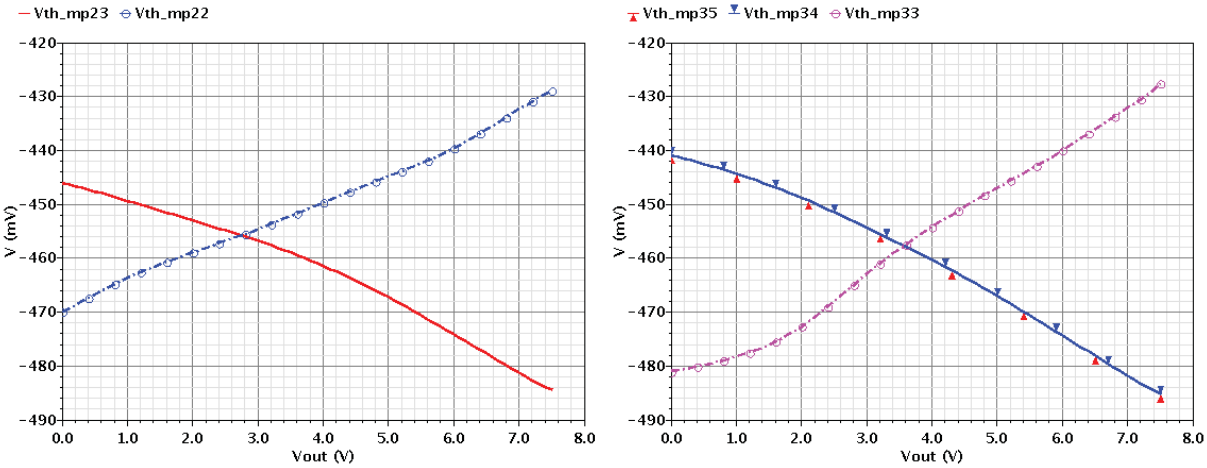


Figure 4.41: Threshold voltage characteristics of Mn1, Mn2 and Mn3 ($VHdd$=7.5 V and Vin=2.5 V)



(a) (b)

Figure 4.42: Threshold voltage characteristics of (a) mp_{22}, mp_{23}, and (b) mp_{33}, mp_{34} and mp_{35} vs. *Vout* (*VHdd*=7.5 V and *Vin*=2.5 V)

5. In the presented circuit design methodology for gate-controlling circuits, it is assumed that the widths of the transistors mn_{22} and mn_{23} of GC_{p2}, mn_{33} and mn_{34} of GC_{p3}, mp_{33} and mp_{34} of GC_{n3} should be equal to each other, but they are set differently to avoid overvoltages. Therefore, this is one of the reasons for the deviation between the generated and ideal gate voltages.

4.2.1.3 DC Analysis: Inactive Driver-Paths

According to the circuit design of the gate-controlling circuits regulating the stacked transistors, the pull-down and pull-up paths should be inactive in the off- and on-states, respectively. Consequently, the driver output node can be charged to the supply voltage or discharged to ground.

For the off-state (pull-up active), the node voltage characteristics VG_{n2}, VS_{n2}, VG_{n3}, VS_{n3} and *Vout* of stacked nMOS transistors vs. the driver output voltage *Vout* are plotted in Figure 4.43a obtained from the DC simulation. The input signal *Vin* of 0 V turns the transistor Mn1 off; therefore, the node S_{n2} can be charged up to 2.5 V because at this value the provided gate voltage VG_{n2} switches the transistor Mn2 off. Then the node S_{n3} is charged to 5.0 V, since the gate-source voltage of the transistor Mn3 falls below its threshold voltage and this turns Mn3 off. As a consequence, the driver output node can be charged to the supply voltage of 7.5 V due to the active pull-up path.

Figure 4.43b depicts the node voltage characteristics (VG_{p2}, VS_{p2}, VG_{p3}, VS_{p3} and *Vout*) of the pull-up stacked transistors vs. *Vout*, which are obtained from the DC simulation for the on-state (pull-down active).

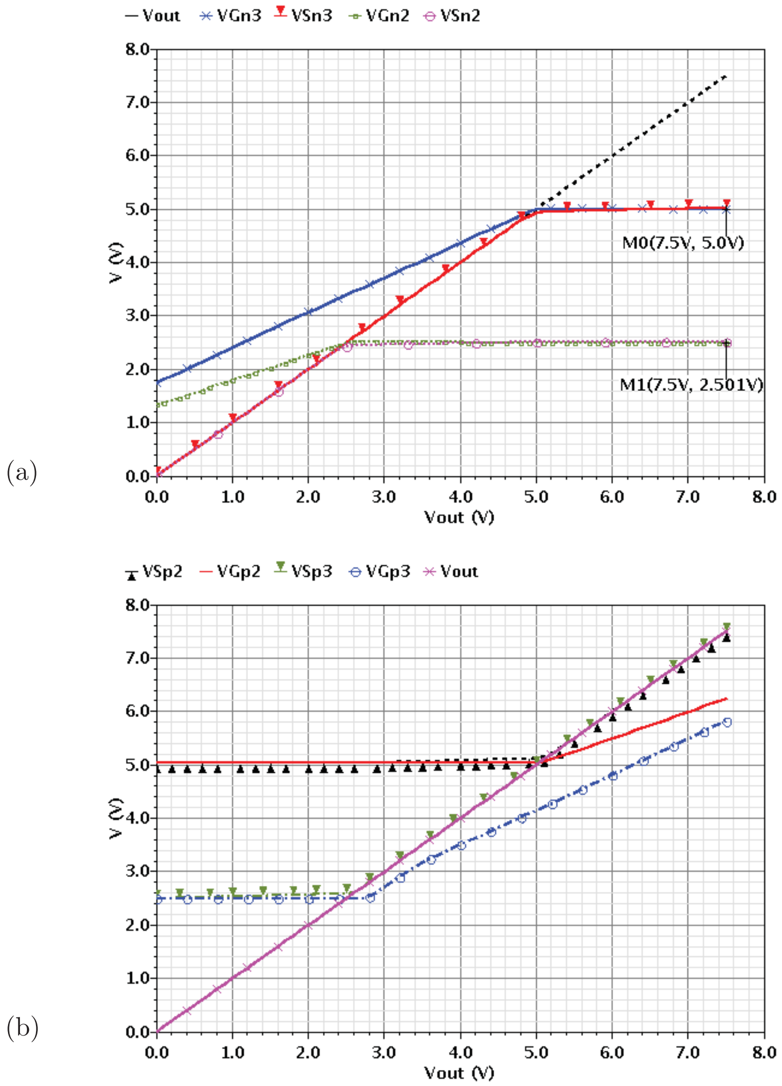


Figure 4.43: The node voltage characteristics of (a) Mn2 and Mn3 in the off-state and (b) Mp2 and Mp3 in the on-state vs. *Vout* obtained from DC simulation (*VHdd*=7.5 V)

4.2.1.4 Transient Analysis

The transient values of the provided gate-voltages VG_{n2} and VG_{n3} are illustrated in Figure 4.44. Their characteristics are limited up to 4.55 V and 6.45 V instead to 5.0 V and 7.5 V, respectively, when the driver output load starts discharging. The reason for this is because the transistors mp_{22} and mp_{23} of the gate-controlling circuit $\mathrm{GC}_{\mathrm{n2}}$ and mp_{33}, mp_{34} and mp_{35} of $\mathrm{GC}_{\mathrm{n3}}$ enter into the cut-off region, whilst the output node is discharged from 7.5 V to about 6.9 V.

In order to avoid this problem, as previously mentioned for the circuit design of a 2-stacked CMOS HV-driver, a pMOS transistor such as $\mathrm{m}_{2\mathrm{x}}$ is connected in parallel to mp_{23} so as to drive the current from VD_{p2} to the node ***P2*** providing the voltage VG_{n2}, when mp_{23} enters into the cut-off region. In-series connected pMOS transistors $\mathrm{m}_{34\mathrm{x}}$ and $\mathrm{m}_{35\mathrm{x}}$

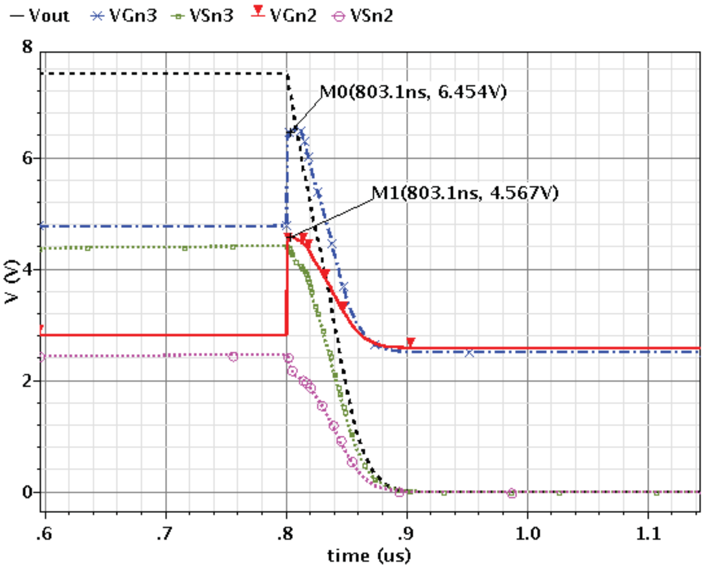


Figure 4.44: Transient node voltage characteristics of the transistors Mn2 and Mn3 based on the version design of a 3-stacked CMOS HV-driver without m_{2x}, m_{34x}, m_{35x}, m_{2y}, m_{34y} and m_{35y} ($VHdd$=7.5 V)

are added in parallel to mp_{34} and mp_{35} to drive the current from VD_{p3} to the node ***P3***. The gates of these three additional transistors are regulated by the switches SW_Vp_{23}, SW_Vp_{34} and SW_Vp_{35} according to the on- and off-states.

The complementary form of the above-described transistors such as m_{2y}, m_{34y} and m_{35y} are inserted into the circuits GC_{p2} and GC_{p3}. Furthermore, to avoid an overvoltage, the gate-drain connected transistors mp_{20}, mp_{30}, mn_{20} and mn_{30} are added to GC_{n2}, GC_{n3}, GC_{p2} and GC_{p3}, respectively and also the capacitors C_2–C_7, C_{23} and C_{p23} are inserted into the circuit of the HV-driver as indicated in Figure 4.36.

Figures 4.45a and 4.45b represent the transient node voltage characteristics of the pull-down (Mn2 and Mn3) and the pull-up (Mp2 and Mp3) stacked transistors, respectively, after optimising the circuits HV-driver with the extra transistors and capacitors. The driver has a load capacitor of 50 pF. In the time frame between 0.4 μs and 0.8 μs in Figure 4.45a, the transistor Mn1 is off due to the low input signal of 0 V. Therefore, the node S_{n2} can be charged from ground up to 2.5 V, because when VS_{n2} reaches around 2.5 V, the provided gate voltage VG_{n2} of 2.8 V turns transistor Mn2 off. Thus, the node S_{n3} can be charged further. The gate voltage VG_{n3} of 5.4 V turns transistor Mn3 off, when the source voltage VS_{n3} reaches 5.0 V. Consequently, the driver output node (*Vout*) can be charged to 7.5 V, due to the active pull-up path. In the same time period, the provided gate voltages VG_{p2} and VG_{p3} at 5.0 V turn the respective transistors Mp2 and Mp3 on. Since the pull-down path is inactive, the pull-up nodes (VS_{p2}, VS_{p3} and also *Vout*) are discharged to 7.5 V (Figure 4.45b). In the period from 0.8 μs to 1.2 μs, the HV-driver with

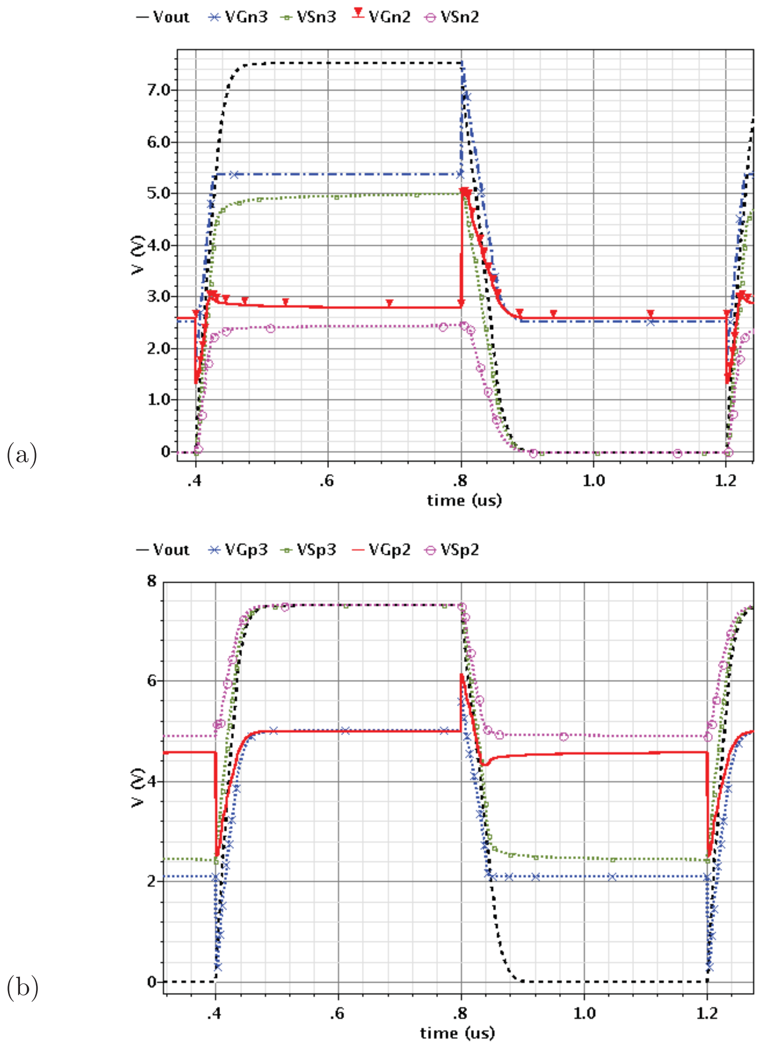


Figure 4.45: Transient node voltage characteristics of (a) Mn2 and Mn3 and (b) Mp2 and Mp3 based on the optimised design of the 3-stacked CMOS HV-driver (*VHdd*= 7.5 V)

an input signal of 2.5 V operates in the on-state. The node S_{n2} is discharged from 2.5 V to ground due to the on-state of Mn1. The node S_{n3} and the output load are also discharged from 5.0 V and 7.5 V, respectively, to ground because of the inactive pull-up path and also the provided VG_{n2} and VG_{n3}, which start from 5.0 V and 7.5 V, respectively and decrease to around 2.5 V (Figure 4.45a). In the same time frame, the level-shifted signal *Vpin* of 7.5 V turns Mp1 off and the provided gate voltages VG_{p2} of 4.6 V and VG_{p3} of ca. 2.2 V switch transistors Mp2 and Mp3 off, when the corresponding nodes S_{p2} and S_{p3} discharge to around 5.0 V and 2.5 V, respectively. As a result, no current can flow from supply to the driver output load; therefore, the output node can be discharged due to the active pull-down path from 7.5 V to ground (Figure 4.45b). According to the off-state, Figure 4.46 indicates the generated and ideal gate voltages of the stacked pMOS transistors VG_{p2}, VG_{p3}, $VG_{p2Ideal}$, $VG_{p3Ideal}$ and also their differences. The respective errors $error(VG_{p2})$ and $error(VG_{p3})$ are plotted in Figure 4.45b, where VG_{2Ideal} and VG_{3Ideal} are defined as the ideal voltages according to Equation (3.33). The provided gate voltages approach the respective ideal voltage characteristics. Figure 4.47 shows the provided and ideal gate voltages of the stacked nMOS transistors VG_{n2}, VG_{n3}, $VG_{n2Ideal}$, $VG_{n3Ideal}$ and also their differences in the on-state of the driver. The maximum errors of VG_{n2} and VG_{n3} from the ideal gate voltages are 8% (380 mV) and 6% (248 mV), respectively.

Figures 4.48a–4.48d display the transient simulation results of the gate-source and drain-source voltages of the *k*th-stacked main transistor to the corresponding gate-drain voltage characteristic. As can be observed from these figures, the voltage between terminals of each stacked transistor is within the technology limit of 2.5 V to within a 5% tolerance. In the range between –2.5 V and 0 V of the gate-drain voltage, the gate-source

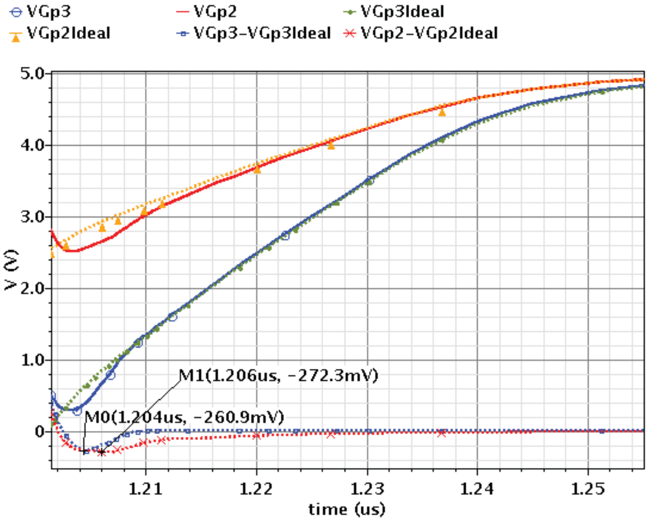


Figure 4.46: Comparison between the provided and ideal node voltage characteristics of Mp2 and Mp3 (*VHdd*=7.5 V, *Vin*=0 V)

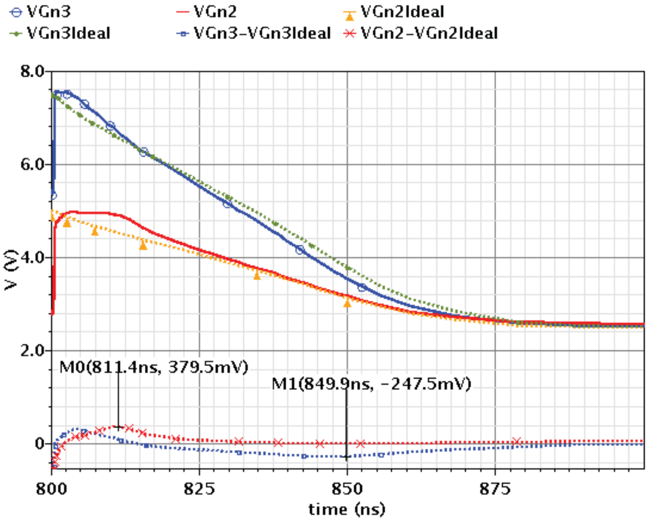
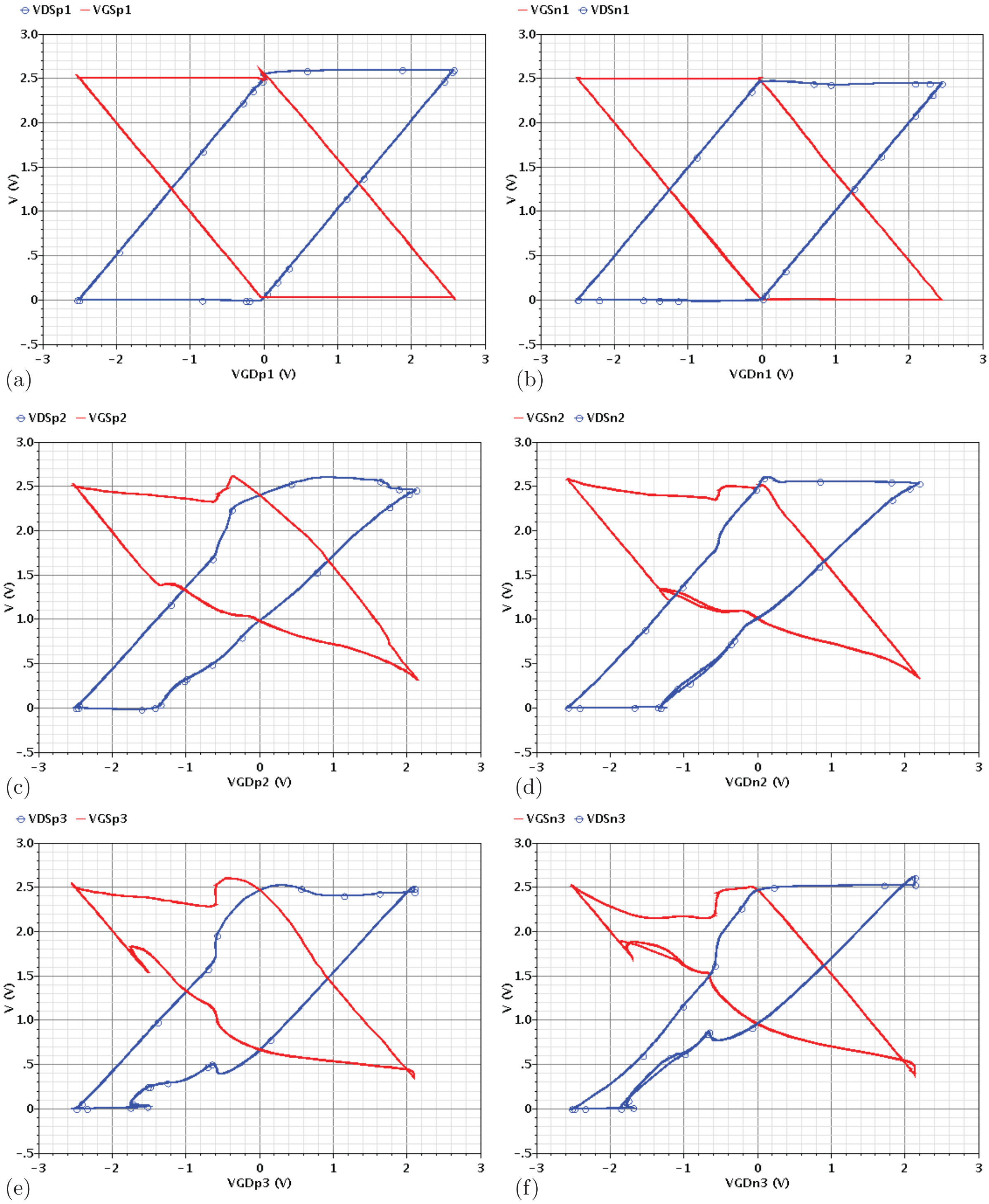


Figure 4.47: Comparison between the provided and ideal node voltage characteristics of Mn2 and Mn3 (*VHdd*=7.5 V, *Vin*=2.5 V)

voltages of Mn2 and Mn3 (VGS_{n2} and VGS_{n3}) approach the offset 2.5 V in the on-state, whereas the transient characteristics of VGS_{p2} and VGS_{p3} follow this value in the off-state. This is what is required for driving the maximum current in the pull-up and pull-down paths.



(a) (b) (c) (d) (e) (f)

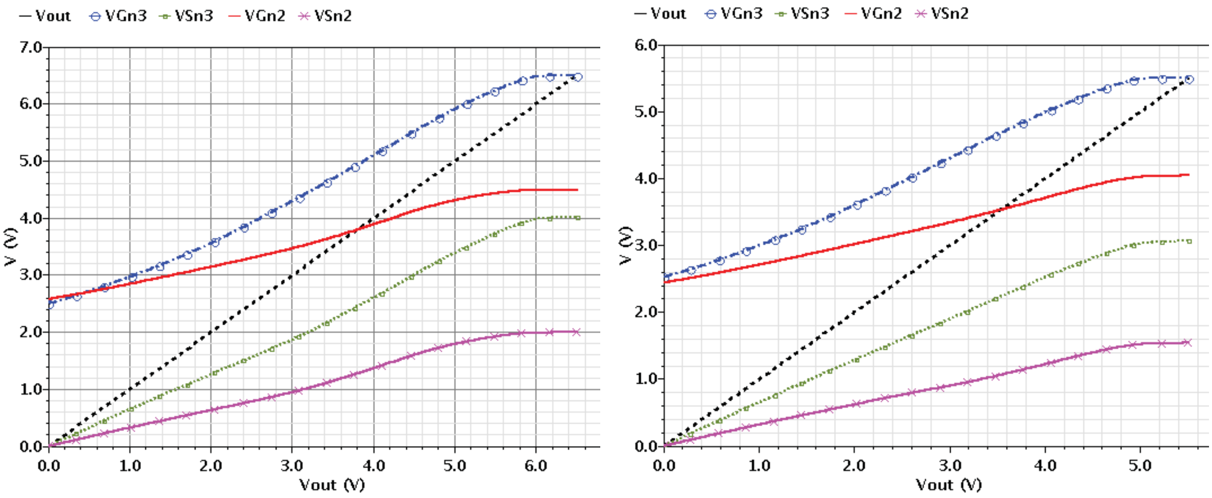
Figure 4.48: Voltage difference across terminals of (a) Mp1, (b) Mn1, (c) Mp2, (d) Mn2, (e) Mp3 and (f) Mn3 of the designed 3-stacked CMOS HV-driver (*VHdd*=7.5 V)

4.2.2 Operational Analysis for VHdd Less than 7.5 V

In this sub-section, to verify the correct operation of the designed HV-driver for lower supply voltages between 5.0 V and 7.5 V, the circuit is supplied with 6.5 V and 5.5 V.

In terms of the rule in Equation (3.23), for this range the driver output load is discharged from *VHdd* to V_I (=$VHdd$–ΔV_I), the provided gate voltages VG_{n2} have to be constant at "$VHdd$–(Vn–ΔV_I)", which is equal to 4.5 V for the supply voltage of 6.5 V and 4.0 V for 5.5 V. The expression ΔV_I is defined in Table 3.3 for a 3-stacked CMOS driver and is 0.5 V for the supply voltage of 6.5 V and 1.0 V for 5.5 V. In this range from V_I to *VHdd*, the gate voltage VG_{n3} has to be 6.5 V and 5.5 V corresponding to the applied supply voltage *VHdd* in accordance with Equation (3.23). Outside this range, when the driver output node is discharged from "$VHdd$–ΔV_I" to ground, VG_{n2} and VG_{n3} have to track the rule in Equation (3.24). Concurrently, each gate voltage has an offset of 2.5 V to the corresponding source voltage, thus allowing the maximum current to flow in the pull-down path.

In the on-state, the DC node voltage characteristics of the pull-down transistors versus *Vout* are plotted in Figures 4.49a and 4.49b for supply voltages of 6.5 V and 5.5 V, respectively.

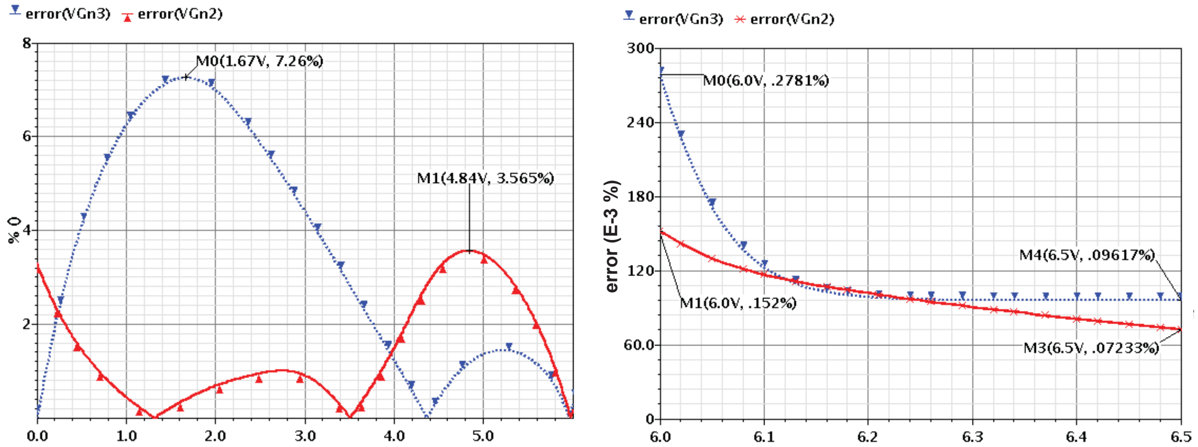


(a) (b)

Figure 4.49: The DC node voltage characteristics of Mn2 and Mn3 of the designed HV-driver vs. *Vout* in the on-state for the supply voltage of (a) 6.5 V and (b) 5.5 V

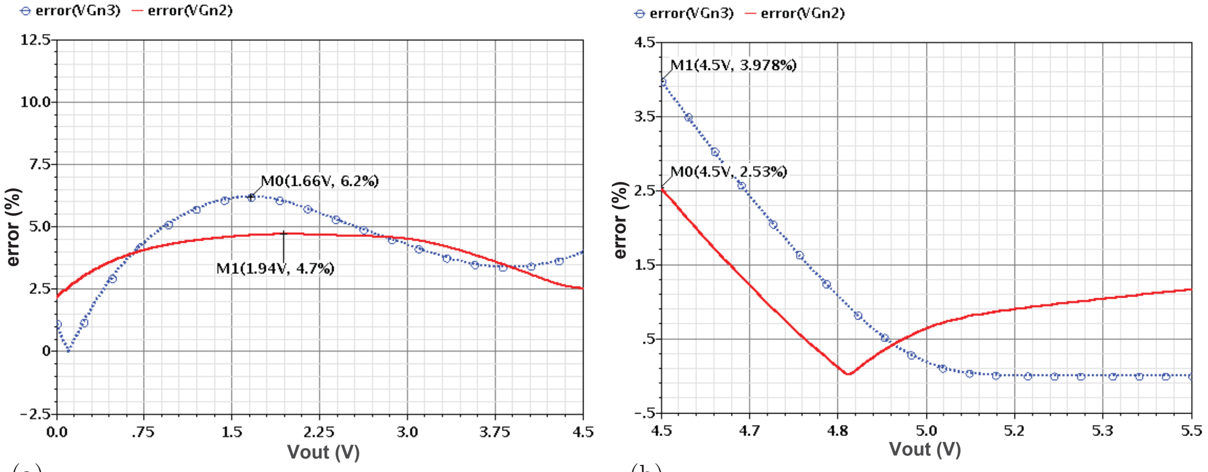
As can be seen, the provided gate voltages VG_{n2} and VG_{n3} approach the ideal lines, and have an offset of ca. 2.5 V to the respective source voltages VS_{n2} and VS_{n3}.

For the supply voltage of 6.5 V, the corresponding errors, $error(VG_{n3})$ and $error(VG_{n2})$, between the provided and calculated gate voltages are displayed in Figures 4.50a and 4.50b with respect to *Vout* in the range from 0 V to 6.0 V and from 6.0 V to 6.5 V, respectively and likewise for the supply voltage of 5.5 V in Figures 4.51a and 4.51b versus *Vout* in the range from 0 V to 4.5 V and from 4.5 V to 5.5 V, respectively. Despite the maximum values of *error*(VG_{n3}) and *error*(VG_{n2}) reaching up to 3% and 7%, respectively, the average of these errors is small and less than 3%.



(a) (b)

Figure 4.50: The errors of the provided gate voltages of Mn2 and Mn3 for the supply voltage of 6.5 V in the range of the output (a) from 0 V to 6.0 V and (b) from 6.0 V to 6.5 V



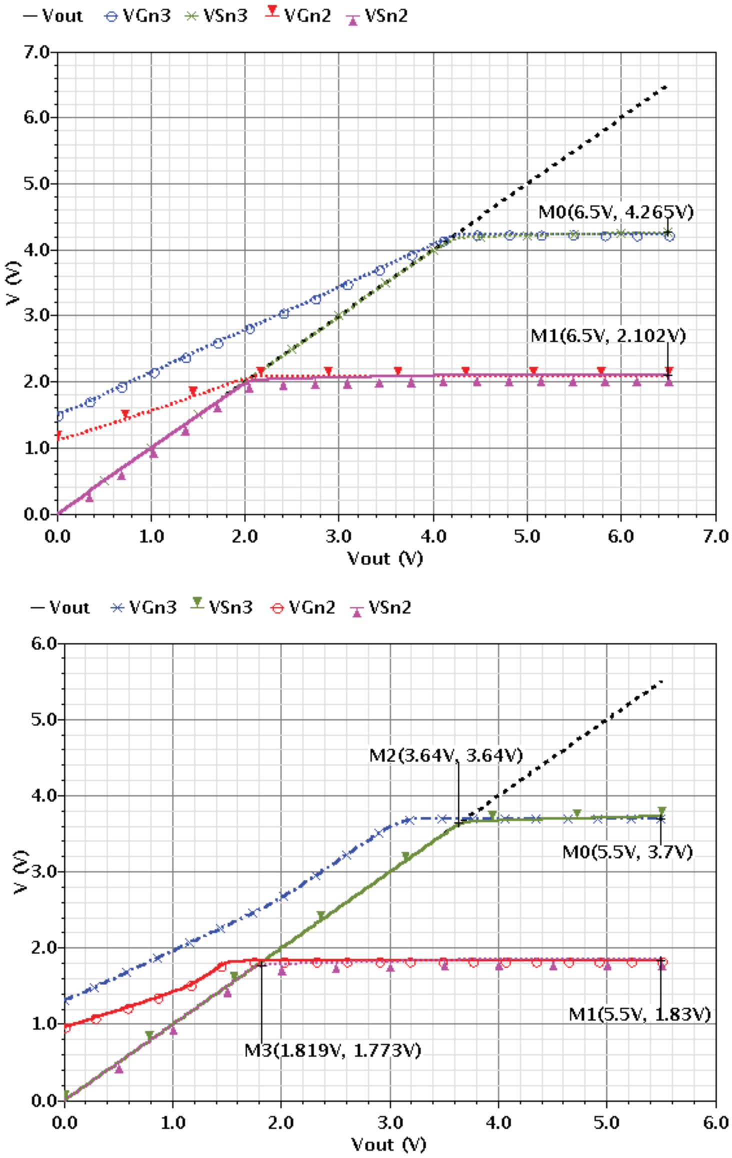
(a) (b)

Figure 4.51: The errors of the provided gate voltages of Mn2 and Mn3 for the supply voltage of 5.5 V in the range of the output (a) from 0 V to 4.5 V and (b) from 4.5 V to 5.5 V

In the off-state (pull-up active), each provided gate voltage must turn the corresponding nMOS transistor off in a timely fashion in order to maintain an equal voltage drop of $VHdd/3$ across each stacked transistor.

For a supply voltage of 6.5 V, Figure 4.52a shows the provided gate voltages VG_{n2}

and VG_{n3}, which turn Mn2 and Mn3 off when the corresponding source voltage VS_{n2} and VS_{n3} reaches up to 2.1 V and 4.3 V, respectively. For *VHdd* of 5.5 V, Figure 4.52b shows that these transistors are switched off when the corresponding source voltages (VS_{n2} and VS_{n3}) reach up to 1.77 V and 3.6 V, respectively, and further charge to 1.83 V and 3.7 V due to the leakage current. As a result, the output is charged to 5.5 V.



(a)

(b)

Figure 4.52: The node voltage characteristics of Mn2 and Mn3 of the 3-stacked CMOS HV-driver vs. *Vout* in the off-state for *VHdd* of (a) 6.5 V and (b) 5.5 V

The transient node voltage characteristics of the pull-down stacked transistors are plotted in Figure 4.53a for a supply voltage of 6.5 V. In the period between 0.4 μs and 0.8 μs, the the transistor Mn1 is off and the provided gate voltage VG_{n2} of 2.5 V turns the transistor Mn2 off, when the corresponding source node S_{n2} is charged to *VHdd*/3, which is equal to ca. 2.17 V. Consequently, the source node of Mn3 (S_{n3}) is charged up to 4.3 V ($2\times VHdd/3$), since at this point the gate voltage VG_{n3} of 4.8 V turns transistor Mn3 off. As a result, the output can be charged to 6.5 V, which is equal to the supply voltage.

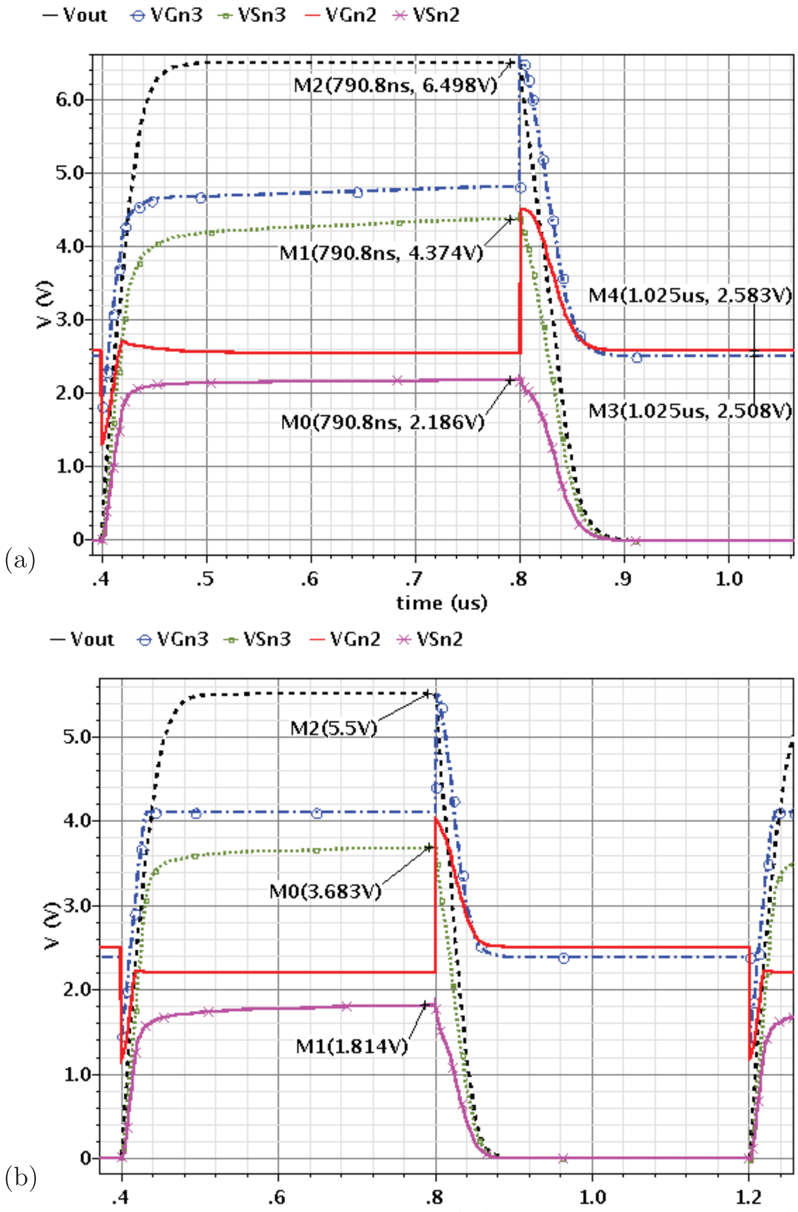


Figure 4.53: Transient node voltage characteristics of the transistors Mn2 and Mn3 of the designed 3-stacked CMOS HV-driver for a supply voltage of (a) 6.5 V and (b) 5.5 V

As can be seen in Figure 4.53b, the same procedure occurs for the stacked nMOS transistors of the driver for a supply voltage of 5.5 V, but with the difference that the source voltages VS_{n2} and VS_{n3} reach up to 1.8 V ($VHdd/3$) and 3.7 V ($2\times VHdd/3$), respectively, since the provided gate voltages VG_{n2} of 2.2 V and VG_{n3} of 4.1 V switch the corresponding transistors Mn2 and Mn3 off. As a consequence, the output can be charged to 5.5 V. From 0.8 μs to 1.2 μs, the HV-driver enters the on-state. The first transistor Mn1 switches on because of the input signal of 2.5 V; therefore, the node S_{n2} can be discharged. Due to the inactive pull-up transistors and the provided gate voltages VG_{n2} and VG_{n3}, which approach the rules in Equations (3.23) and (3.24), the source node of Mn3 and the output load are discharged to ground. The offset between the source and the corresponding gate voltages is approximately 2.5 V.

As can be seen for both supply voltages, 6.5 V and 5.5 V, the driver output load can charge and discharge between the supply voltage and ground due to the provided gate voltages according to the off- and on-states.

4.2.3 Comparison with Work B

In this sub-section, the currents and on-resistances of the pull-up and pull-down paths of the designed 3-stacked CMOS HV-driver defined here as work *A*, are compared to the published work (*B*) described in [31] pp. 124–130, as shown in Figure 4.54. The number and dimensions of stacked transistors of the HV-driver *B* are set identically to those of the driver *A*.

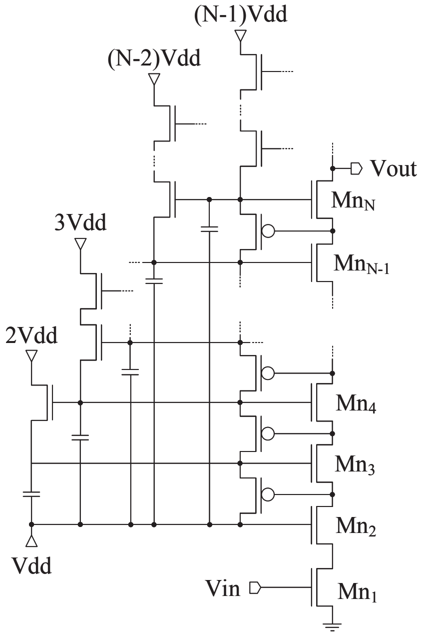
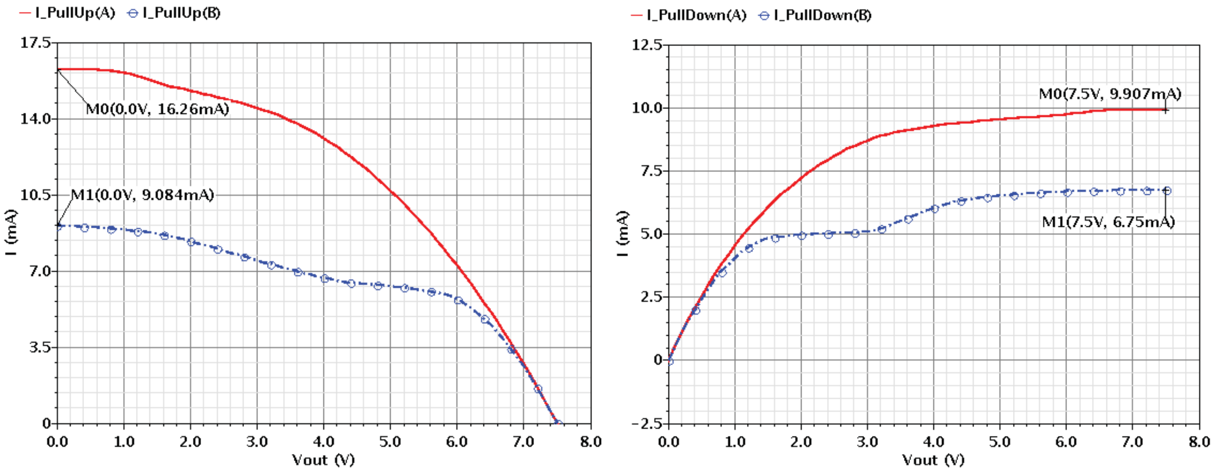


Figure 4.54: Bias circuit for the nMOS transistors of the *N*-stacked CMOS driver *B* [31]

From Figures 4.55a and 4.55b, it can be observed that the pull-up and pull-down currents of this driver (*A*) supplied with 7.5 V are significantly higher when compared with those of work *B*, while the output node is charged from 0 V to ca. 6.8 V in the



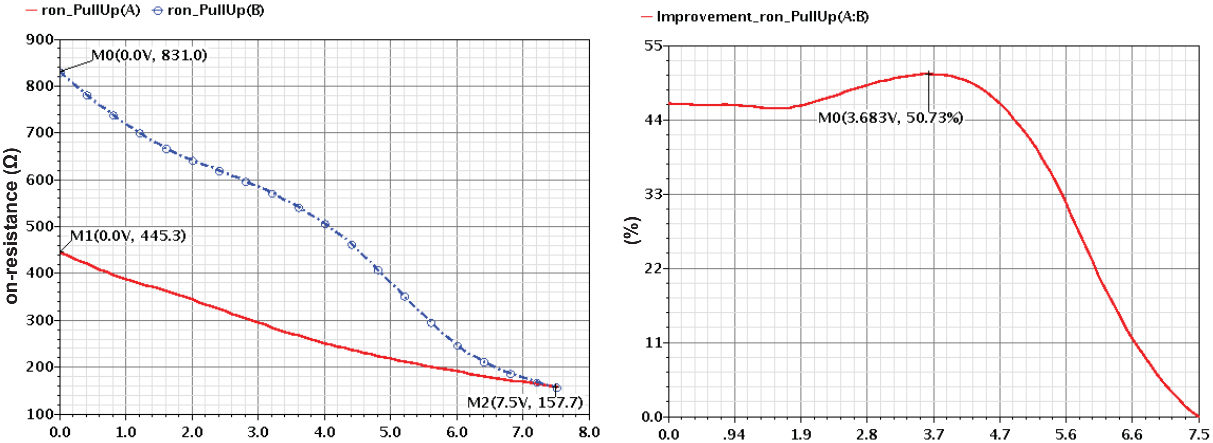
(a) (b)

Figure 4.55: A comparison between (a) the pull-up and (b) the pull-down currents of both HV-drivers *A* and *B* (*VHdd*=7.5 V)

off-state and discharged from 7.5 V to about 0.8 V in the on-state, respectively. The initial pull-up and pull-down currents of *A* are increased by about 76% (7.2 mA) and 46% (3.2 mA) respectively, when compared to the appropriate initial currents of *B*.

These results indicate that the on-resistances of both pull-up and pull down paths have been reduced, which can be discerned from Figures 4.56a and 4.57a, respectively. The improvements to the corresponding on-resistance in percent terms are presented in Figures 4.56b and 4.57b.

The initial on-resistances of the driver's (*A*) pull-up and pull-down paths are considerably improved by 46% (386 Ω) and 36% (413 Ω) respectively, when compared with the driver *B*. When the driver output node (*Vout*) is charged from 0 V to 6.5 V in the



(a) (b)

Figure 4.56: (a) The pull-up on-resistance of the HV-drivers *A* and *B*, (b) the on-resistance improvement of *A* compared to *B* (*VHdd*=7.5 V, off-state)

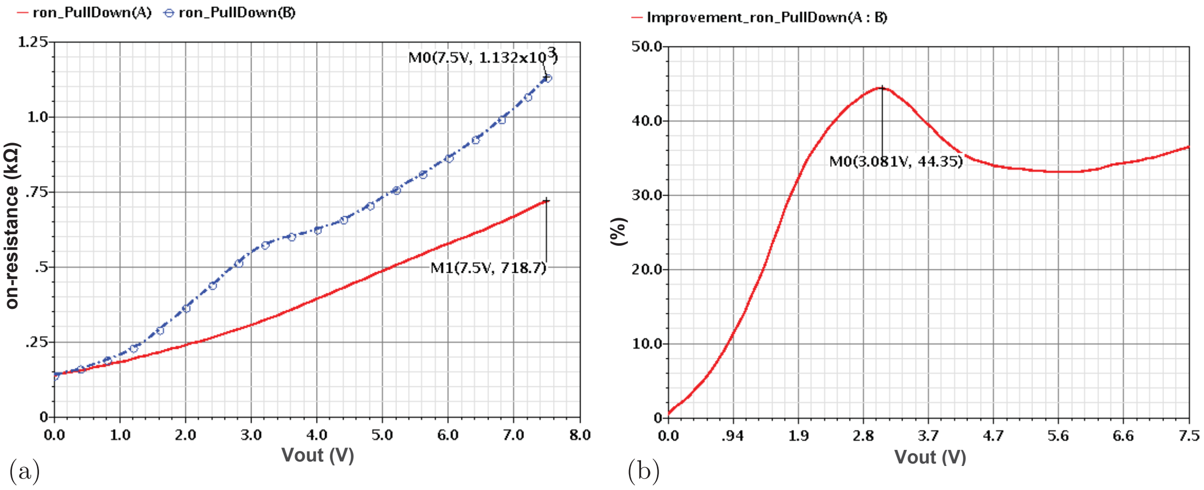


Figure 4.57: (a) The pull-down on-resistance of the HV-drivers *A* and *B*, (b) the on-resistance improvement of *A* compared to *B* (*VHdd*=7.5 V, off-state)

off-state and discharged from 7.5 V to 0.9 V in the on-state, the improvements of both on-resistances are still over 10%, which is the reason for driving more current in the pull-up and pull down paths of the driver *A* when compared with the driver *B*.

For lower supply voltages, the pull-up and pull-down currents of the driver *A* are significantly higher than those of the driver *B*, as can be seen in Figures 4.58a and 4.58b for a supply voltage of 5.5 V. The initial pull-up and pull-down currents of the driver *A* are 14.8 mA and 9.5 mA, respectively, whereas those of the work *B* are 2.3 mA and 6.6 mA.

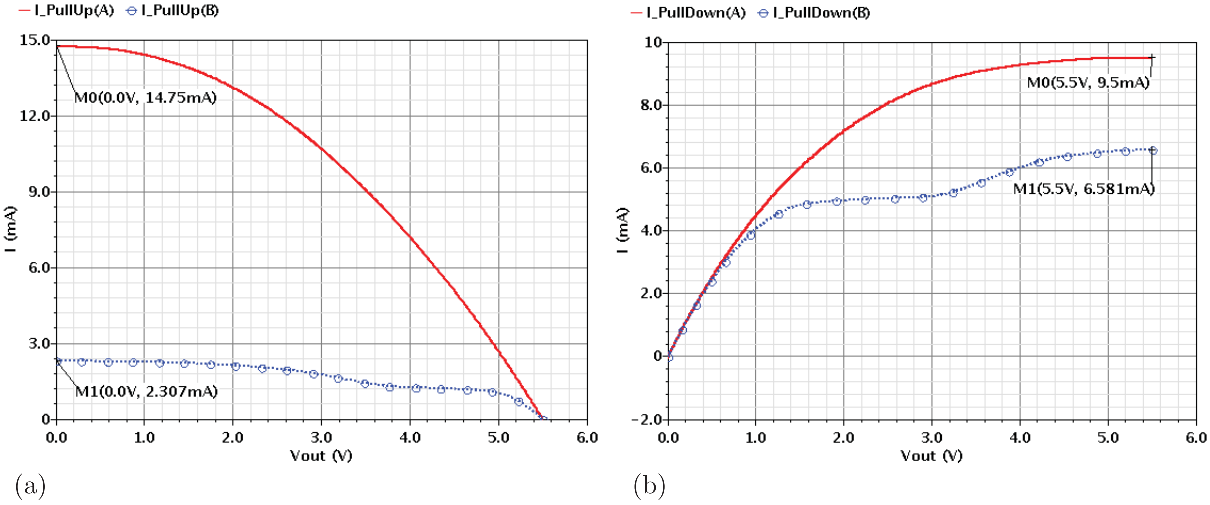
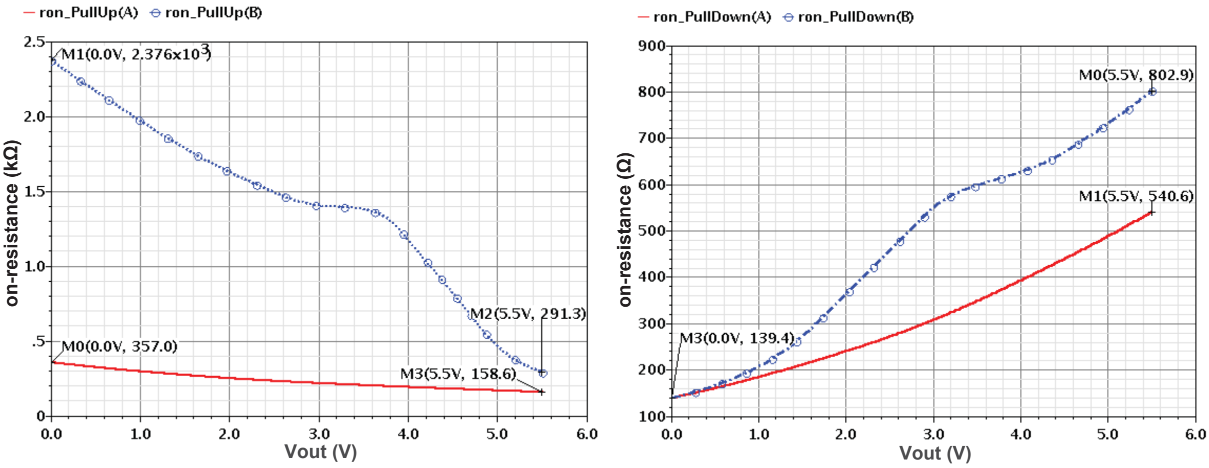


Figure 4.58: (a) The pull-up and (b) the pull-down currents of the HV-drivers *A* and *B* (*VHdd*=5.5 V)

Driving a higher current indicates a lower on-resistance, as may be observed in Figures 4.59a and 4.59b showing respectively the pull-up and pull-down on-resistances of both HV-drivers *A* and *B*. The driver *A* has an initial on-resistance of 357 Ω and 540 Ω



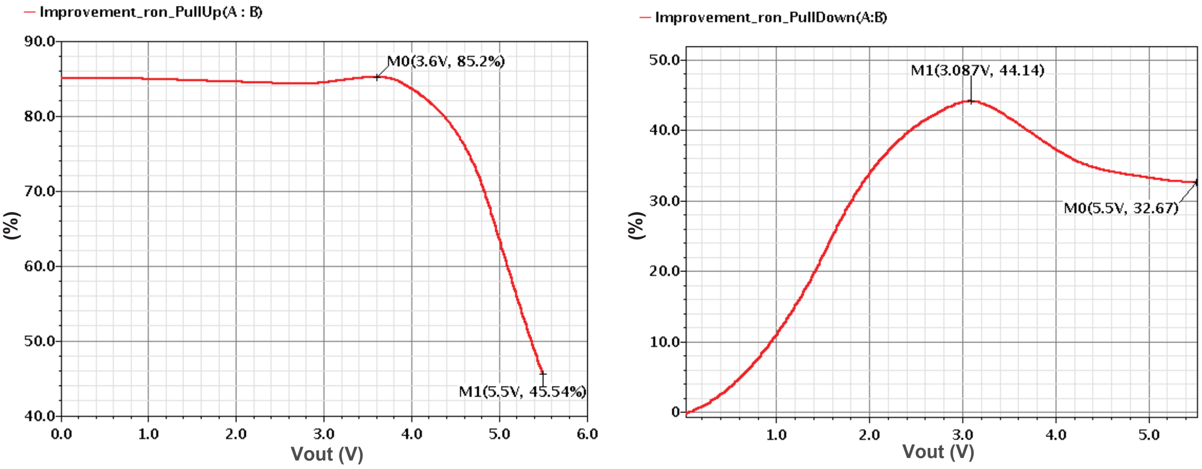
(a) (b)

Figure 4.59: (a) The pull-up and (b) the pull-down on-resistance of the HV-drivers *A* and *B* (*VHdd*=5.5 V)

respectively, whereas the work *B* has 2.4 kΩ and 803 Ω.

During discharging the output node from 5.5 V to 1.0 V, the improvement of the pull-down on-resistance is over 10% (Figure 4.60b). Furthermore, the on-resistance of the pull-up transistors is considerably improved between 45% and 85% when the output load charges from 0 V to 5.5 V (Figure 4.60a).

Table 4.6 gives the comparison between the initial pull-up and pull-down currents (I_p and I_n) and on-resistances (R_{on}) for both HV-drivers *A* and *B* with supply voltages of 5.5 V, 6.5 V and 7.5 V. In comparison to driver *B*, the simulation results for different supply voltages indicate that the gate control circuits $\mathrm{GC_{n2}}$, $\mathrm{GC_{n3}}$, $\mathrm{GC_{p2}}$ and $\mathrm{GC_{p3}}$ of the designed HV-driver *A* drive higher currents in the pull-up and pull-down paths due to the



(a) (b)

Figure 4.60: The improvement of (a) the pull-up and (b) the pull-down on-resistances of the HV-drivers *A* in comparison to the work *B* (*VHdd*=5.5 V)

Table 4.6: Initial pull-up and pull-down currents and on-resistances of both 3-stacked CMOS HV-drivers A and B for different supply voltages

VHdd	**work**	**pull-up**		**pull-down**	
		I_p *[mA]*	R_{on} *[Ω]*	I_n *[mA]*	R_{on} *[Ω]*
7.5 V	*A*	16.3	445.3	9.9	718.7
	B	9.1	831.0	6.8	1132
improv. of A		79%	46%	45%	36%
remark		*Ron-improv.* $>$ *10% with* *max. 51% for Vout* ϵ *[0 V, 6.5 V]*		*Ron-improv.* $>$ *10% with* *max. 44% for Vout* ϵ *[0.9 V, 7.5 V]*	
6.5 V	*A*	13.9	452.7	9.7	630.5
	B	6.9	934.2	6.6	965.3
improv. of A		101%	51%	47%	35%
remark		*Ron-improv.* $>$ *10% with* *max. 57% for Vout* ϵ *[0 V, 6.2 V]*		*Ron-improv.* $>$ *10% with* *max. 45% for Vout* ϵ *[1.0 V, 6.5 V]*	
5.5 V	*A*	14.8	357.0	9.5	540.6
	B	2.3	2376	6.6	802.9
improv. of A		543%	85%	44%	33%
remark		*Ron-improv.* $>$ *45% with* *max. 85% for Vout* ϵ *[0 V, 5.5 V]*		*Ron-improv.* $>$ *10% with* *max. 44% for Vout* ϵ *[1.0 V, 5.5 V]*	

provided gate voltages as anticipated. These suggest a reduced on-resistance for pull-up and pull-down paths as confirmed by the on-resistance analysis detailed in Table 4.6. An average of about 85% of *Vout* during charging or discharging between 0 V and *VHdd*, the on-resistance of driver *A* shows an improvement of over 10% when compared with driver *B*.

Chapter 5

Realisation of a HV-Driver for a Buck Converter

In this chapter, the design of the presented 3-stacked CMOS HV-driver is optimized for switching a buck converter, and implemented on chips. The chips are mounted on printed circuit boards using two package technologies: chip-in-package and chip-on-board. Both are measured with different loads and presented in this chapter.

5.1 3-Stacked CMOS HV-Driver for Switching a Buck-Converter

The main purpose of this work is to design an HV-driver switching a buck converter, as depicted in Figure 5.1. The buck converter has the task to reduce the DC high voltage of 5.5 V (*VHdd*) to the lower DC voltage of 1.2 V (V_{bc}). As mentioned in section (2.1.3), the converter contains an inductor L (4.7 μH) connected in-series with a resistor R_m (100 mΩ) and a parallel RC circuit (R_L of 12 Ω and C_L of 12 μF). The low-pass LC filter removes the high frequency switching ripple to provide a DC voltage V_{bc} to the load R_L. The designed HV-driver should switch the buck converter with a frequency of 2 MHz.

5.1.1 Circuit Parameters

The transistor dimensions of the designed 3-stacked CMOS HV-driver presented in Chapter 4 are adjusted for a load capacitor of 50 pF. By regulating the gate of each stacked transistor due to the gate-controlling circuits, a current approximating to the maximum value can flow in the pull-up and pull-down paths; however, the resulting nearly minimum on-resistance, varying between 150 Ω and 718 Ω during charging and discharging the

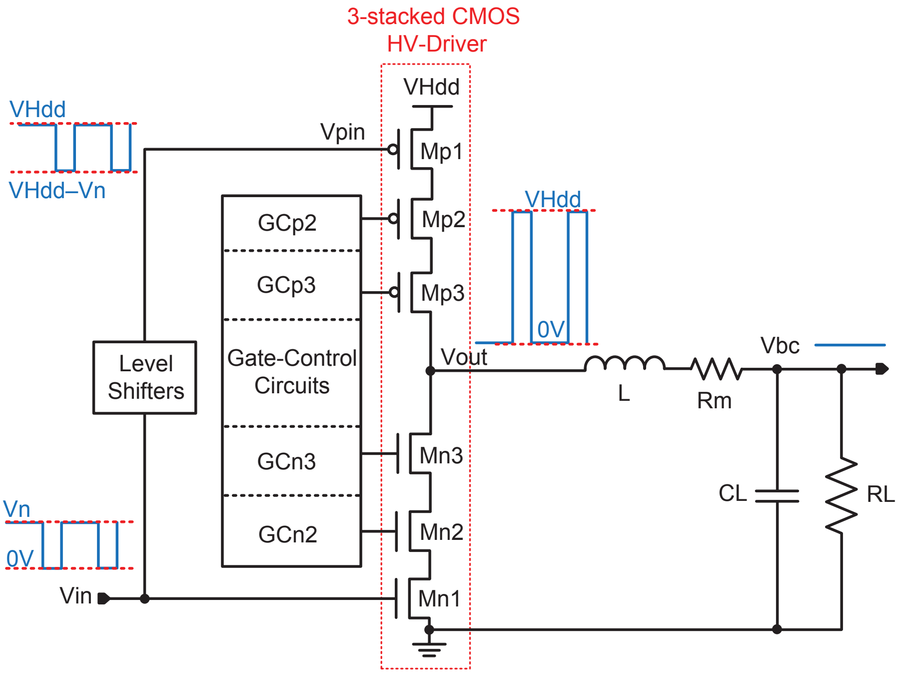


Figure 5.1: Principle of a buck converter switched by the designed 3-stacked CMOS HV-driver

driver output load for the supply voltage of 7.5 V, is still not low enough to switch the proposed buck converter; therefore, the on-resistance is reduced by scaling the transistors of the designed circuit, as described in the following sub-sections.

5.1.1.1 Scaling of Driver Transistors

By increasing the gate width and also the number of transistors, which are connected in-parallel in each stack, the driver on-resistance can be reduced. This will be shown by simulation of the varying parameters of the first stacked CMOS. It should be mentioned, to begin with circuit design, the RF CMOS transistors "*nmos_rf_25_6t*" and ‘‘*pmos_rf_25*" are selected from the 65-nm *TSMC* technology with a nominal I/O voltage of 2.5 V. The maximum total width and the minimum length of each transistor are 320 μm and 280 nm, respectively. At a drain-source voltage of 100 mV, the on-resistances of these transistors, nMOS and pMOS, with the maximum width of 320 μm, are 3.56 Ω and 9.63 Ω, respectively, which are too low for switching the proposed buck converter. An on-resistance of 45 mΩ in the pull-up and pull-down paths would be optimal for switching the buck converter. To achieve this on-resistance, the numbers of nMOS (Xn) and pMOS (Xp) transistors in each stack should be increased to 238 and 642, respectively. However, increasing the gate width to 320 μm and the numbers of nMOS and pMOS transistors to 238 and 642, respectively requires a larger chip area. Furthermore, the gate capacitance and parasitic resistance increase, which negatively impacts on the efficiency of the proposed buck converter. The provided chip area for the proposed HV-driver circuit may not exceed 500 μm×500 μm; therefore, the numbers of nMOS and pMOS transistors in each stack are set to 20 and 54, respectively. This results an on-resistance of 0.178 Ω in each stack device and a total on-resistance of 0.534 Ω in the driver's pull-down and pull-up paths. For different numbers of transistors (*Xn* and *Xp*), Figure 5.2 shows the transient gate-capacitance characteristics of an nMOS (Mn) and a pMOS (Mp) transistors forming an inverter, which is switched by a pulse signal. The length and width of each transistor are set to 280 nm and 320 μm, respectively. Increasing the number of transistors (*Xn* for Mn and *Xp* for Mp), the appropriate gate-capacitance also increases, which would negatively affect the efficiency of the buck converter.

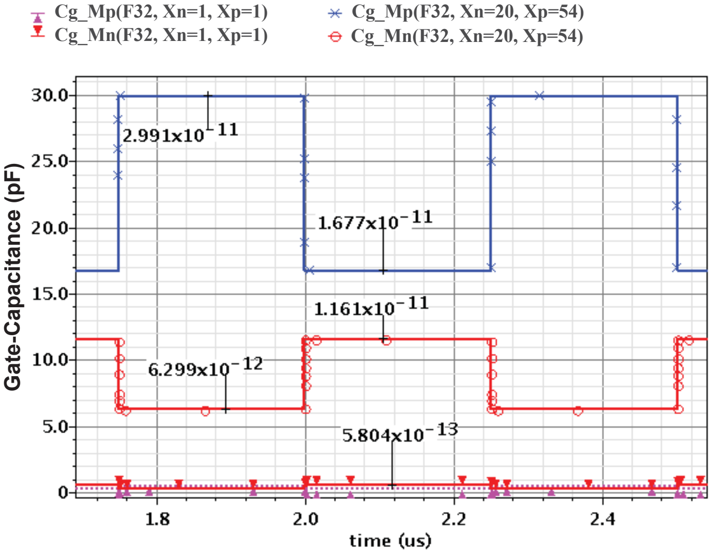


Figure 5.2: Transient gate-capacitance characteristics of an nMOS and a pMOS transistor of an inverter for different numbers of transistors

Figures 5.3a and 5.3b demonstrate the improvement of the pull-up and pull-down on-resistances, which reach up to 99% and 98%, by increasing the number of transistors (*Xn* for Mn1–Mn3 and *Xp* for Mp1–Mp3) in each stacked device when compared with the situation where *Xn* and *Xp* are both set to one ("**1**"). The improvement of the respective on-resistance ($Improv._{ron}$) is obtained from the following equations:

$$Improv._{ron\_PullUp} = \frac{ron_{PullUp}(Xp = 1) - ron_{PullUp}(Xp = 1 \ldots 56)}{ron_{PullUp}(Xp = 1)} \times 100 \tag{5.1a}$$

$$Improv._{ron\_PullDown} = \frac{ron_{PullDown}(Xn = 1) - ron_{PullDown}(Xn = 1 \ldots 23)}{ron_{PullDown}(Xn = 1)} \times 100 \tag{5.1b}$$

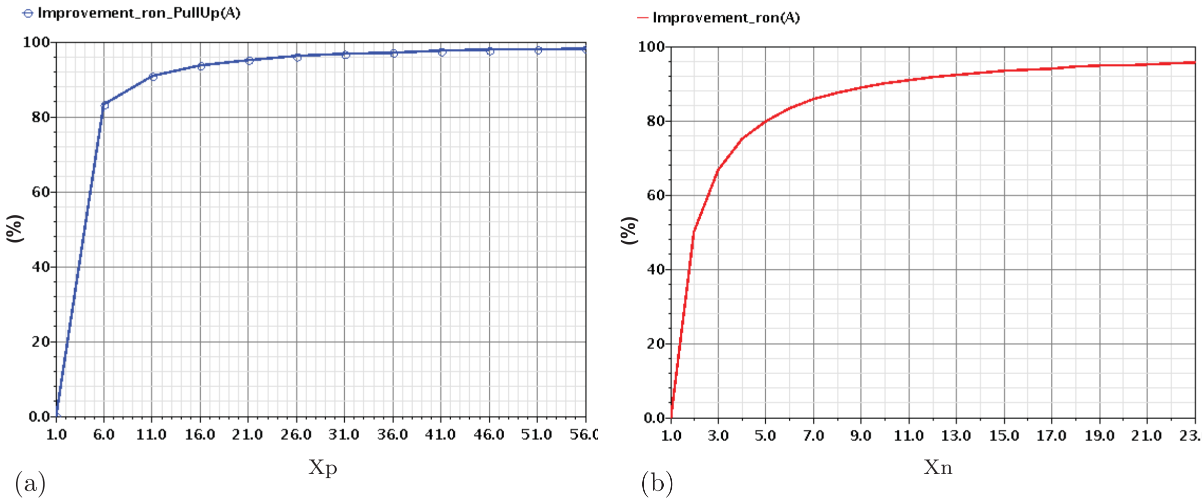


Figure 5.3: The on-resistance improvement of (a) the pull-up and (b) the pull-down transistors in comparison to the original design with respect to increasing the number of transistors in each stack of the driver

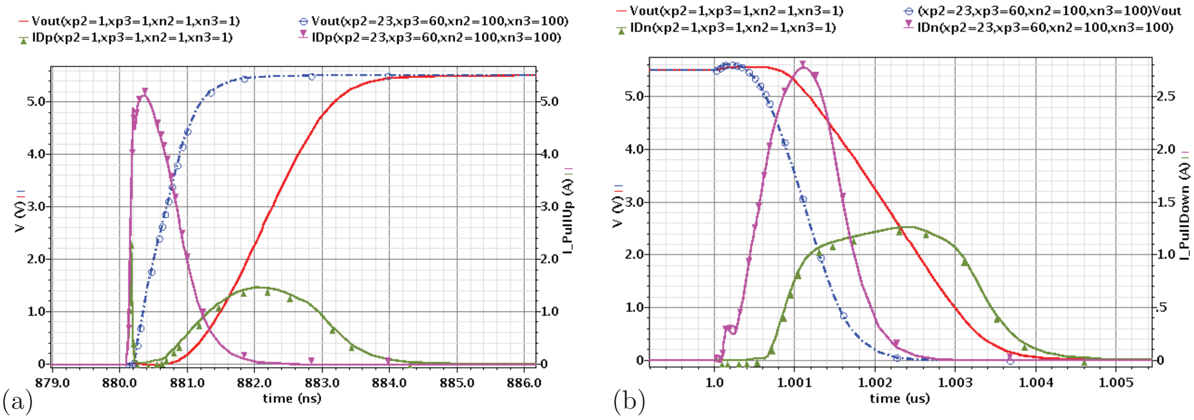
5.1.1.2 Scaling of Gate-Controlling Circuits

Increasing the total width and raising the number of transistors in each stacked device of the HV-driver, allow more current to flow. Therefore, the charging and discharging of the output load is faster. In terms of adjusting the provided gate voltages with the current and also ensuring each transistor remains in the safe operating region, the number of transistors used in the gate-controlling circuits also needs to increase: 23 for each transistor of GC_{n2}, 60 for GC_{n3}, 100 for GC_{p2} and GC_{p3}.

Figures 5.4a and 5.4b show the pull-up (ID_p) and pull-down (ID_n) currents, the rising and falling edge of $Vout$ for two cases: when the numbers of transistors of the gate-controlling circuits are still "**1**" as per the original circuit design and also when they are set to the required number, where xp_2, xp_3, xn_2 and xn_3 are defined as the number of transistors in the circuits GC_{n2}, GC_{n3}, GC_{p2} and GC_{p3} respectively.

For the second case, at the beginning of charging and discharging, more current drives in the pull-up and pull-down paths when compared with the first case. The lower rise- and fall times of 0.91 ns and 1.1 ns respectively, indicate that the driver switches faster than the first one with rise- and fall times of 1.88 ns and 2.0 ns, respectively. These results are obtained by the transient analysis of the HV-driver with a capacitive load of 500 pF.

Since with these transistors' dimensions, the switching times of each transistor is faster than those of the original parameters, the capacitors C_2–C_7, C_{23} and C_{p23} are not required to avoid overvoltages.



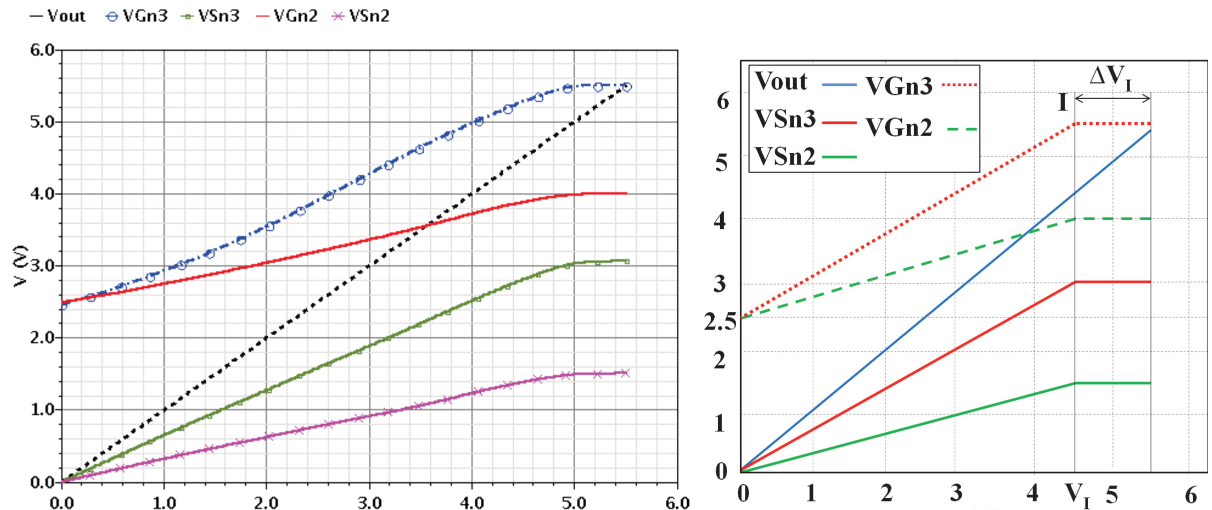
(a) (b)

Figure 5.4: Transient characteristics of (a) the pull-up currents, rising edges of *Vout* and (b) the pull-down currents and falling edges of *Vout* of the designed driver with the original and the optimised numbers of transistors of GC-circuits (C_L=500 pF).

5.1.2 Circuit Analysis

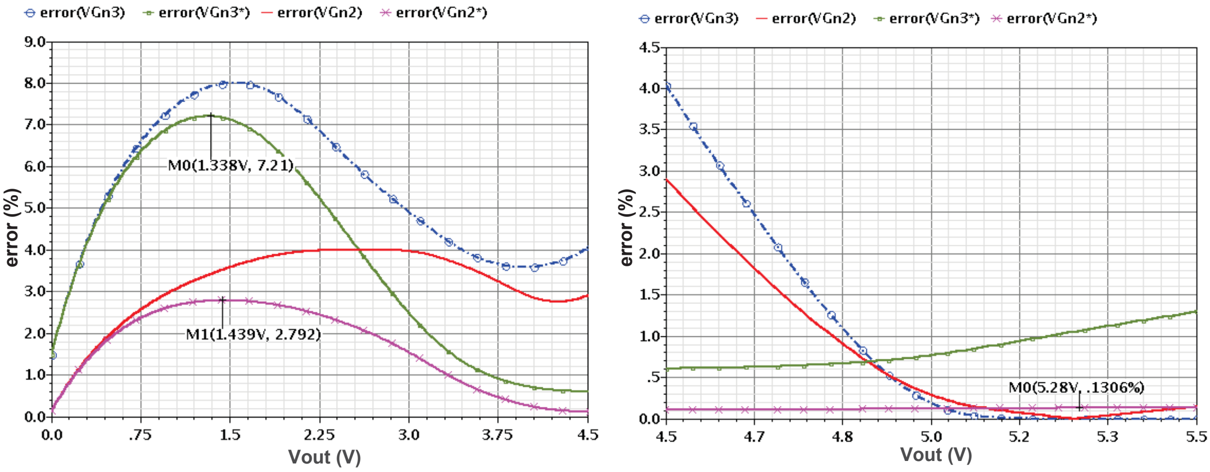
After setting and adjusting the transistors' dimensions for the HV-driver and the gate-controlling circuits, the DC node voltage characteristics of the pull-down transistors Mn2 and Mn3 vs. *Vout* are plotted in Figure 5.5a for the on-condition (pull-down active). The circuit is supplied with 5.5 V. Due to the active pull-down and inactive pull-up transistors, the driver output and the pull-down nodes can be discharged from 5.5 V, 3.0 V and 1.5 V to ground, respectively. The gate voltages VG_{n3} and VG_{n2}, which start with 5.5 V and 4.0 V for operating the transistors Mn3 and Mn2 in the on-state, have an offset of approximately 2.5 V to the appropriate source voltages VS_{n3} and VS_{n2}. The node voltage characteristics approach the ideal voltages plotted in Figure 5.5b, as previously presented in Figure 3.5.

When the driver output node is discharged from 4.5 V to ground, the error between the provided and calculated gate voltages $error(VG_{n2})$ and $error(VG_{n3})$, have maximum values of 4% and 8%, respectively, as shown in Figure 5.6a. In the range of *Vout* between 4.5 V and 5.5 V, VG_{n2} and VG_{n3} have to be constant at 4.0 V and 5.5 V, respectively according to the rule in Equation (3.23). However, the provided gate voltages have a slight deviation from the corresponding ideal values (Figure 5.6b). At the beginning of discharging, both errors $error(VG_{n2})$ and $error(VG_{n3})$ are very low at less than 0.2%, but they raise to 2.9% and 4% when *Vout* is reduced down to 4.5 V. The curves with expressions $error(VG_{nk}*)$ show the errors between the provided gate voltages (VG_{n2} and VG_{n3}) and the respective source voltages with an offset of 2.5 V. These errors $error(VG_{nk}*)$ are lower than the appropriate error($\mathrm{VG_{nk}}$), especially in the range of *Vout* between 4.5 V and 5.5 V, where they are under 1.3% for $error(VG_{n3}*)$ and under 0.1% for $error(VG_{n2}*)$. This indicates a high accuracy of operating the gate-controlling circuits $\mathrm{GC_{n2}}$ and $\mathrm{GC_{n3}}$, which provide the gate voltages with an offset of 2.5 V to the respective source voltages.



(a) (b)

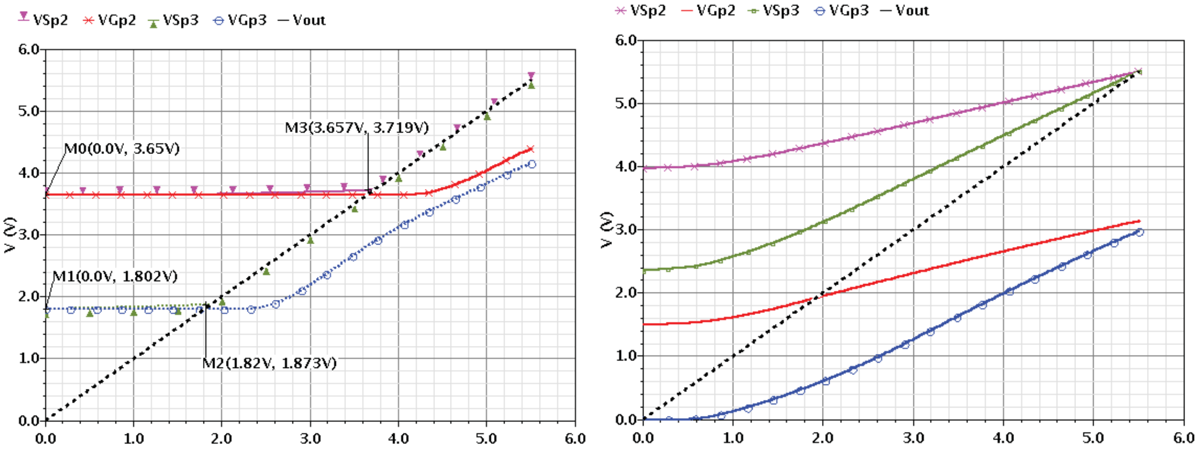
Figure 5.5: (a) The DC simulated node voltage characteristics of Mn2 and Mn3 of the designed 3-stacked CMOS driver vs. *Vout* and (b) the respective ideal characteristics described in Chapter 3 (*VHdd*=5.5 V, pull-down active)



(a) (b)

Figure 5.6: The errors of the provided gate voltages for Mn2 and Mn3 of the designed 3-stacked CMOS HV-driver in the range of the output (a) from 0 V to 4.5 V and (b) from 4.5 V to 5.5 V (*VHdd*=5.5 V)

In addition to the on-state of the pull-down transistors, in order that the driver output and also pull-down nodes S_{n2} and S_{n3} can be discharged to ground, the pull-up pMOS transistors must be off to avoid driving current from supply to the output node. Figure 5.7a depicts the provided gate and source voltages of Mp2 and Mp3 versus *Vout* in the on-state. At the beginning of discharging the output node, VG_{p2} and VG_{p3} are low enough to discharge the appropriate source nodes from 5.5 V down to 3.7 V and 1.8 V, respectively, since at these voltages the corresponding pMOS transistor switches off. Figure 5.7b displays the provided gate and the appropriate source voltages of the pull-up transistors for the off-state, whereas the pull-down network is inactive. As can be seen, VG_{p3} and VG_{P2} start with 0 V and 1.5 V, respectively for driving current from supply to the driver output node. The corresponding source voltages, which have an offset of 2.5 V to the appropriate gate voltages, rise from 2.4 V and 4.0 V respectively to 5.5 V. The provided gate voltages approach the rules in Equations (3.34) and (3.35).



(a) (b)

Figure 5.7: The DC node voltage characteristics of Mp2 and Mp3 in the (a) off- and (b) on-state ($VHdd$=5.5 V)

5.1.3 Comparison with Work B

In this sub-section, the designed circuit defined here as work A, is compared to the published work (B) described in [31] pp. 124–130 (Figure 5.8), and the transistor dimensions of work B are adjusted accordingly to work A. However, the involved capacitors are neglected, since they increase the switching times of the driver B.

The comparison between the pull-up currents of HV-drivers A and B are plotted in Figure 5.9a, and the pull-down currents in Figure 5.9b. The currents of the driver A are significantly higher than those of driver B. Their initial pull-up and pull-down currents are improved 288% (3.89 A) and 48% (1.35 A), respectively.

The simulation results demonstrate that raising the width and the number of transistors increases the driving current, which portends reducing the pull-up and pull-down on-resistances (*ron_PullUp* and *ron_PullDown*), as displayed respectively in Figures 5.10a and 5.10b. Their initial values for circuit A are 986 mΩ and 1.2 Ω respectively, whereas those of the original circuit described in the previous chapter (Figures 4.59a and 4.59b) are 357 Ω and 540 Ω. The figures also show the comparison of this circuit A with the driver B containing the same transistor dimensions as used in driver A. However, the on-

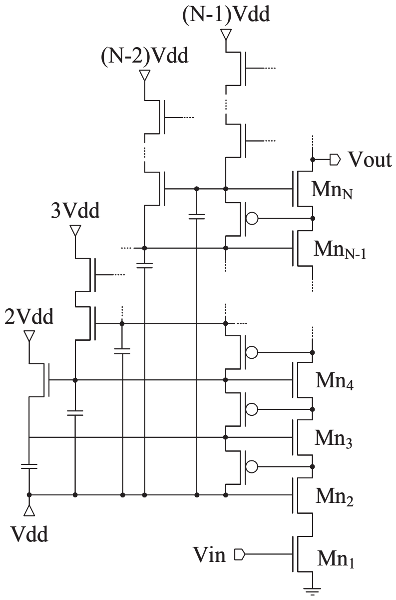
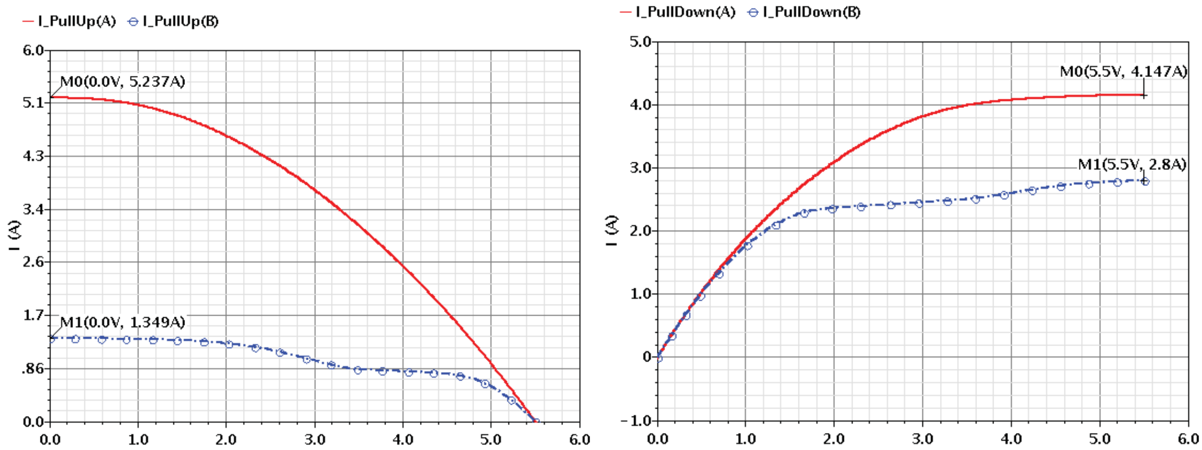


Figure 5.8: Bias circuit for the nMOS transistors of the N-stacked CMOS driver B [31]

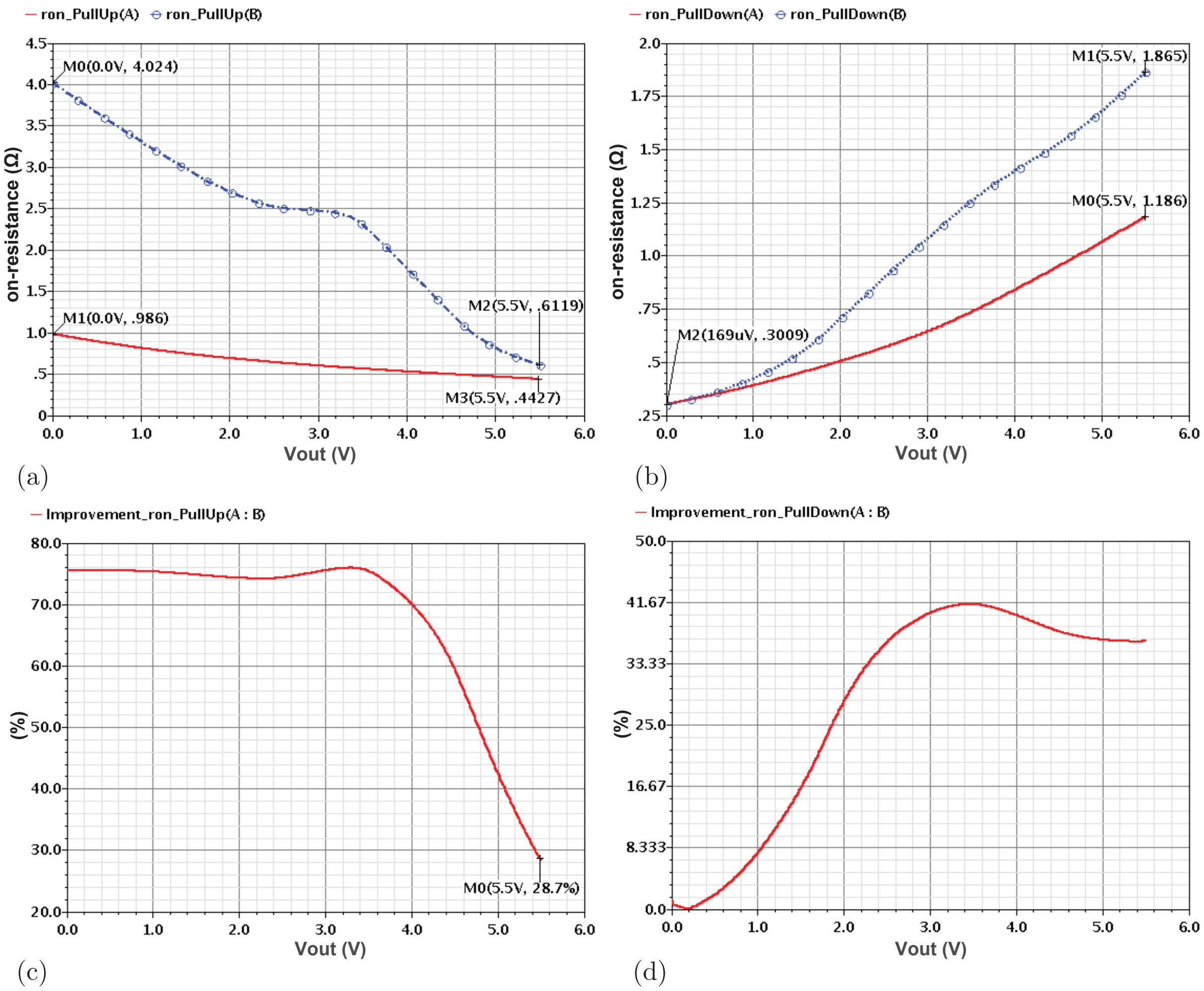


(a) (b)

Figure 5.9: (a) The pull-up and (b) the pull-down currents of the HV-drivers A and B ($VHdd$=5.5 V)

resistance of A also has a considerable improvement in comparison to the circuit B, which reaches up to 75% for the pull-up and 41% for the pull-down path, as can be observed in Figures 5.10c and 5.10d, respectively. These give evidence, which in turn shows that the provided gate voltages of A drive a higher current as shown in Figures 5.9a and 5.9b.

Figure 5.11 shows the improvement in the rise- and fall times of the driver output (A) when compared with $Vout$ of B. With increasing the load capacitance from 100 pF to 5 nF the rise time of the driver A output voltage shows a reduction of between 11% and 70%. The improvement in the fall time reaches up to 28%, whereas for a capacitance lower than 0.41 nF it worsens, as can be observed from the results in Figure 5.11.



(a) (b) (c) (d)

Figure 5.10: (a) The pull-up and (b) pull-down on-resistance of the HV-drivers *A* and *B*, (c) and (b) the respective on-resistance improvement of driver *A* relative to *B*

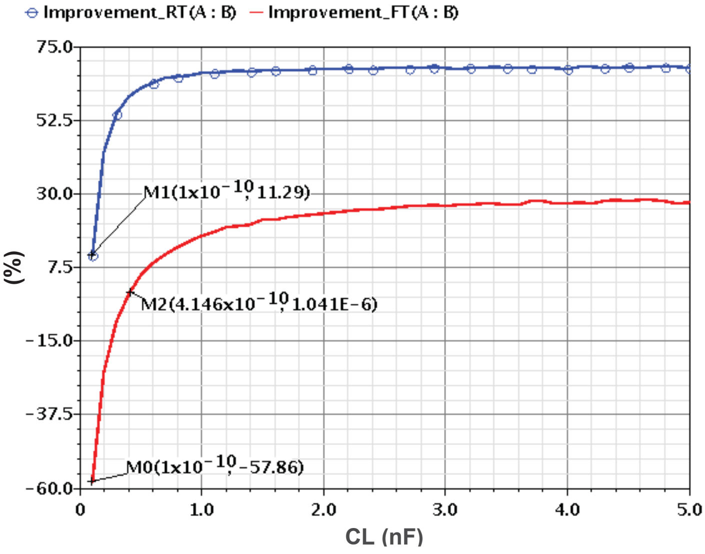


Figure 5.11: Improvement of the rise- and fall times of the driver output voltage (*A*)

Lower on-resistance, rise- and fall times of HV-driver *A* lead to lower conduction and switching loss. Therefore, the buck converter switching by driver *A* has higher efficiency if switched by driver *B*.

5.2 HV-Driver 3HVDv1

As previously shown, increasing the total width and raising the number of transistors in each stacked device of the HV-driver allows more current to flow. Therefore, the charging and discharging of the output load is faster, but on the other hand, the number of transistors used in the gate-controlling circuits also needs to increase: 23 for each transistor of $\mathrm{GC_{n2}}$, 60 for $\mathrm{GC_{n3}}$, 100 for $\mathrm{GC_{p2}}$ and $\mathrm{GC_{p3}}$ in terms of adjusting the provided gate voltages with the pull-up and pull down currents of the driver and avoiding any overvoltages.

This requires a larger chip area. The layout of the circuit would be far greater than the envisaged chip area of around 450 μm×450 μm. Therefore, the circuit area needs to be reduced.

In this sub-section, the final circuit design and layout of a 3-stacked CMOS driver implemented on chips are introduced. The circuit is defined as **3HVDv1**. The pre- and post-layout simulation and measurement results are also presented. The chips are manufactured for testing on printed circuit boards using two methods of packaging technologies. One is that the chips are bonded into a **CQFP64** package, and the other is that the chips are mounted directly on PCBs, which is defined chip-on-board (**COB**). These technologies and the measurement results of both with or without overvoltage protections are also introduced in this section.

5.2.1 Circuit Design

For shrinking the circuit area, the number of transistors used in each stack of the gate-controlling circuits have been reduced, but irregularly to control currents driving in the entire circuit for avoiding an overvoltage.

Furthermore, instead of using the RF-transistors, "*nmos_rf_25_6t*" and "*pmos_rf_25*", whose layouts are available fully constructed in the 65-nm TSMC technology, the basic I/O nMOS and pMOS transistors "*nch_25*" and "*pch_25*" have been used. These transistors also have a nominal I/O voltage of 2.5 V and a wider range for setting the transistor width, but their layouts need to be completed manually regarding the ideal layouts of the RF-transistors. For example, to construct the layout of a deep n-well (DNW) nMOS transistor, a deep n-well layer is inserted as a rectangle covering the transistor and additionally an n-well layer is placed around the structure as a sidewall. In terms of connecting the DNW-terminal to the deep n-well layer, conductors are set on the n-well layer . When the finger of a transistor is greater than one, the source and drain regions contain detached layers, which are respectively manually connected together. The surface area of connecting layer is set according to the current flowing through these transistor terminals. By reducing the number of transistors of the gate-controlling circuits and employing the basic transistors, a significantly smaller circuit area of about 0.187 mm^2 (435×431 μm^2) has been achieved. The values of resistors [Ω], capacitors [fF], widths [μm] and the number (n) of transistors with a length of 280 nm of the implemented 3-stacked CMOS HV-driver are given in Table 5.1.

In this version of circuit (*3HVDv1*), as illustrated in Figure 5.12, the switch SW_VD$_{p2}$ shown in Figure 4.36 has been removed for reducing the number of reference voltages. The voltage *VD$_{p2}$* is provided by the first level-shifter *LS2*, whereby the output signal of this circuit is buffered two times due to two inverters *Inv_VD$_{p2}$* containing a pMOS and an nMOS transistor as detailed in Table 5.1.

Table 5.1: Resistors, capacitors, widths [μm] and numbers (n) of transistors of *3HVDv1*

pull-down path	**pull-up path**	**GC$_{n2}$**				
Mn1, Mn2, Mn3	*Mp1, Mp2, Mp3*	mp_{20}	mp_{21}	mp_{22}	mp_{23}	mp_{2x}
899.91 (20)	899.91 (8)	50 (5)	50 (5)	1 (19)	1 (26)	1 (16)

SW_VD$_{p2}$			**SW_VD$_{n2}$**		**GC$_{p2}$**				
TG	*nMOS*	*pMOS*	*nMOS*	*pMOS*	mn_{20}	mn_{21}	mn_{22}	mn_{23}	mn_{2y}
TG$_{on}$	none	none	90 (2)	10 (1)	10 (1)	4 (2)	1 (20)	1 (30)	30 (30)
TG$_{off}$	none	none	90 (2)	10 (1)					

SW_VD$_{p3}$			**SW_VD$_{n3}$**		**SW_Vp$_{23}$**		**SW_Vn$_{23}$**	
TG	*nMOS*	*pMOS*	*nMOS*	*pMOS*	*nMOS*	*pMOS*	*nMOS*	*pMOS*
TG$_{on}$	4 (1)	40 (1)	140 (2)	320 (2)	8 (1)	12 (1)	20 (1)	20 (1)
TG$_{off}$	4 (1)	40 (1)	140 (2)	320 (2)	8 (1)	12 (1)	20 (1)	20 (1)

SW_Vp$_{34}$			**SW_Vp$_{35}$**		**SW_Vn$_{34}$**		**SW_Vn$_{35}$**	
TG	*nMOS*	*pMOS*	*nMOS*	*pMOS*	*nMOS*	*pMOS*	*nMOS*	*pMOS*
TG$_{on}$	10 (4)	10 (1)	4 (1)	10 (1)	10 (1)	20 (2)	7 (1)	10 (1)
TG$_{off}$	10 (4)	10 (1)	4 (1)	10 (1)	10 (1)	20 (2)	7 (1)	10 (1)

GC$_{n3}$							
mp_{30}	mp_{31}	mp_{32}	mp_{33}	mp_{34}	mp_{35}	mp_{34x}	mp_{35x}
30 (1)	30 (1)	30 (2)	1 (11)	1 (23)	1 (23)	480 (28)	135 (1)

GC$_{p3}$							
mn_{30}	mn_{31}	mn_{32}	mn_{33}	mn_{34}	mn$_{35}$	mn_{34y}	mn_{35y}
250 (1)	250 (1)	4 (11)	1 (4)	1 (1)	1 (1)	110 (24)	320 (34)

Inv$_1$, Inv$_2$, Inv$_4$		**Inv$_3$**		**Inv$_5$, Inv$_6$**		**Inv_VD$_{p2}$**	
nMOS	*pMOS*	*nMOS*	*pMOS*	*nMOS*	*pMOS*	*nMOS*	*pMOS*
110 (1)	170 (1)	150 (1)	110 (1)	100 (1)	50 (1)	40 (1)	300 (1)

passive components			
R_1	R_{p1}	C_1	C_{p1}
101.1 Ω	1.0 Ω	35.1 pF	20.3 pF

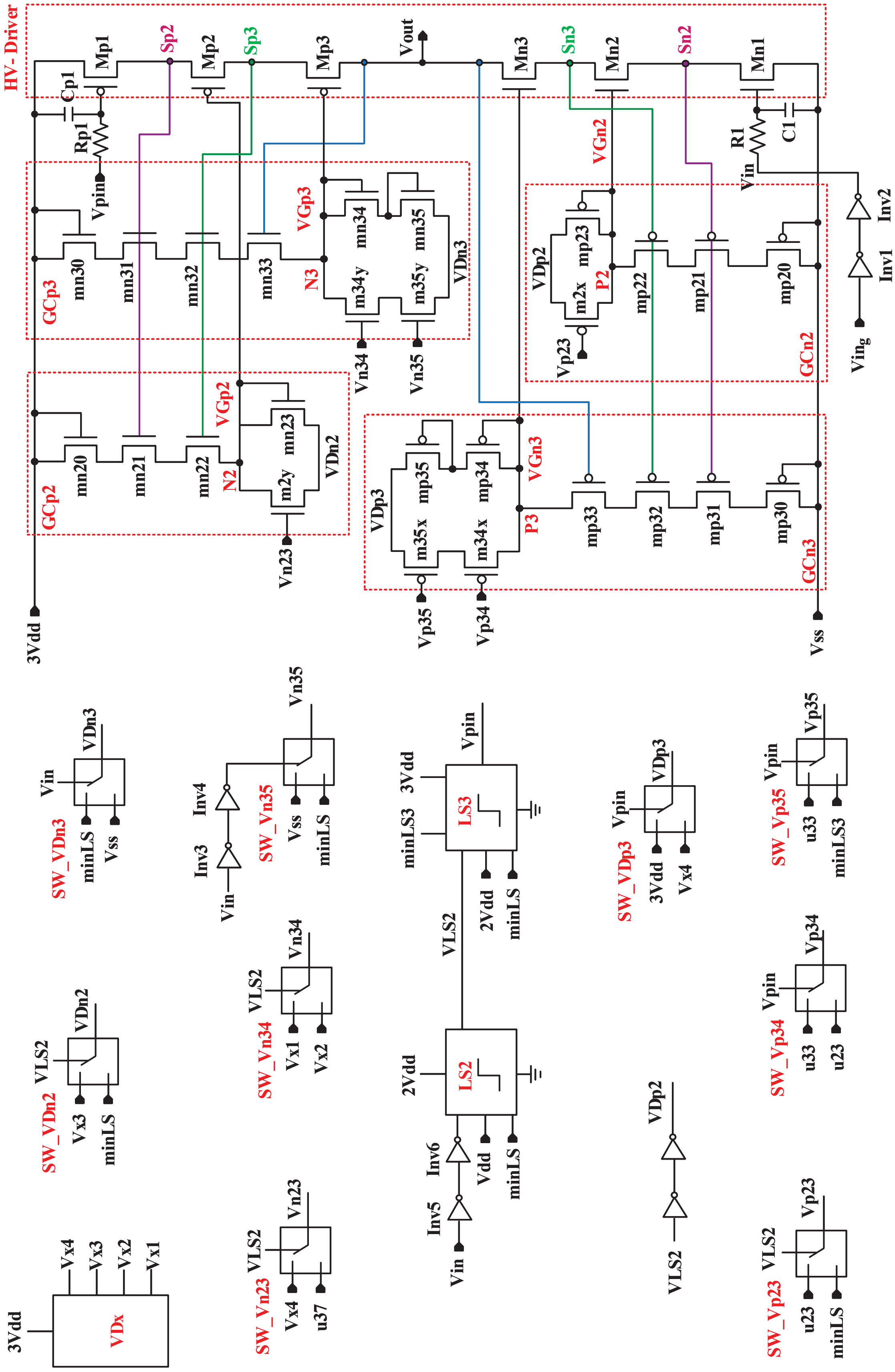


Figure 5.12: Circuit design of the designed 3-stacked CMOS HV-driver *3HVDv1*

The capacitors C_2–C_7, C_{23} and C_{p23} indicated in Figure 4.36 are not required for this circuit, which is a great advantage for saving the chip area. For adjustment, the input signals *Vin* and *Vpin* to the voltages of the pull-down and also pull-up nodes to avoid an overvoltage, two low-pass filters (R_1C_1 and $R_{p1}C_{p1}$) are integrated in the circuit passing input signals for regulating the first CMOS transistors Mn1 and Mp1. A voltage divider (*VDx*) is included in the circuit intended to provide four reference voltages, V_{x1}, V_{x2}, V_{x3} and V_{x4}, which are 5.0 V, 4.7 V, 2.7 V and 0.5 V at a supply voltage of 5.5 V.

The layout and microphotograph of the circuit are presented in Figures 5.13 and 5.14 respectively. Since the number of transistors of the gate-controlling circuits should be reduced for the purpose of saving the chip area, some transistors of the circuit HV-driver cannot operate in the safe region. Therefore, in this case, the circuit is designed for a supply voltage of 5.5 V. Since the number of transistors in each stack of the gate-controlling circuits has been reduced and also some reference voltages, which are close to each other, are considered to have one value, the circuit operation is analysed in the following steps, showing how far the provided gate voltages are from ideal values.

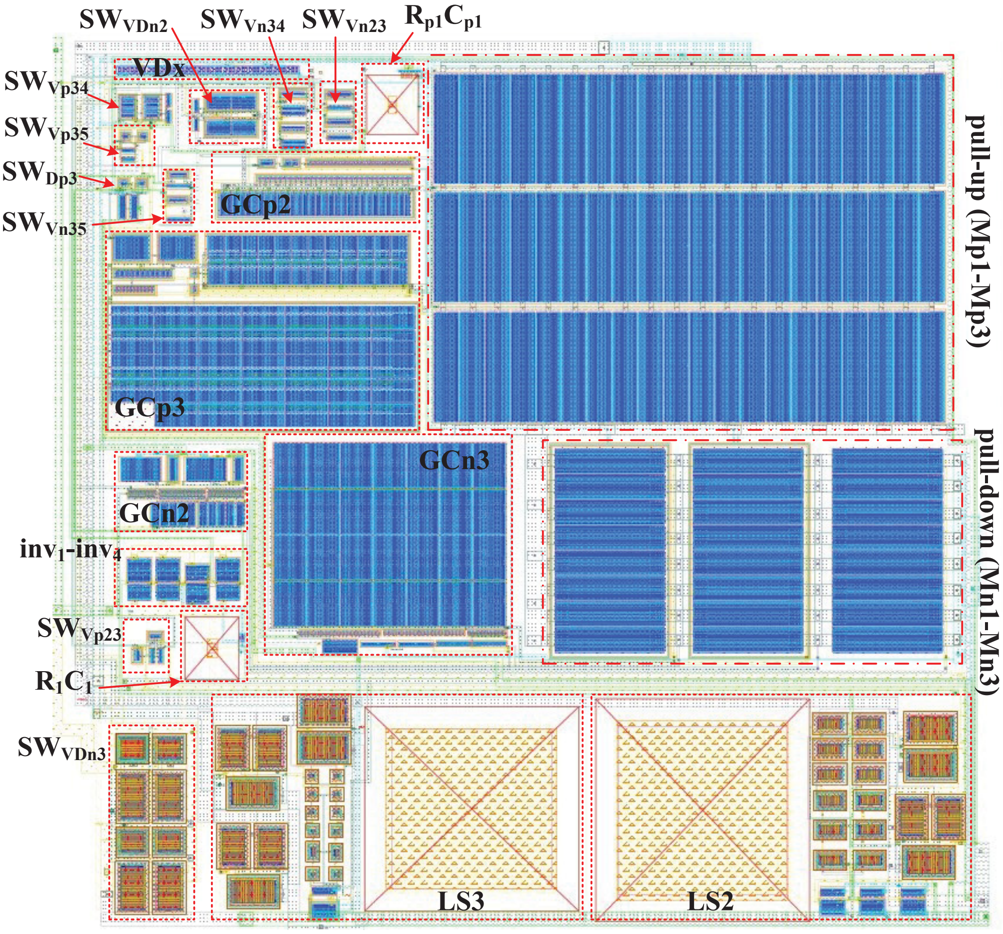


Figure 5.13: The layout and of the HV-driver *3HVDv1*

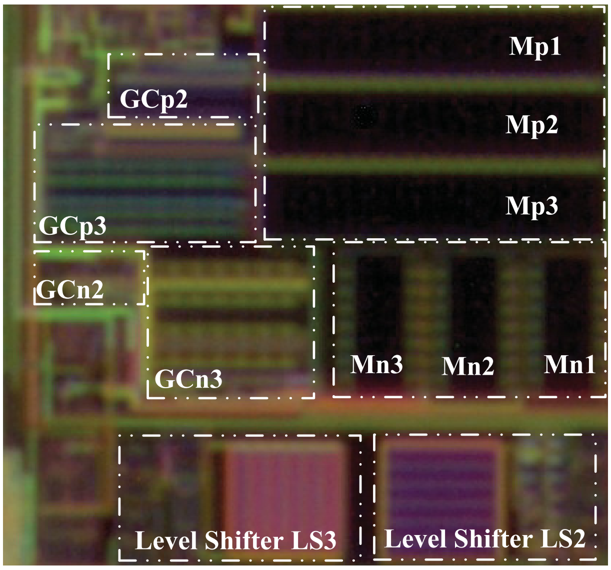


Figure 5.14: The microphotograph of the HV-driver *3HVDv1*

5.2.2 Circuit Analysis

For the on-state (pull-down active), the provided gate voltages of the pull-down transistors, as illustrated in Figure 5.15, approximately follow the rules in Equations (3.23) and (3.24), but their deviations from the calculated voltages are higher than the gate voltages of the previous circuit presented in Section 4.2. The deviations of the generated VG_{n2} and VG_{n3} of this circuit (*3HVDv1*) from the calculated values are plotted versus *Vout* in Figure 5.16a between 0 V to 4.5 V and in Figure 5.16b between 4.5 V to 5.5 V. These errors *error(*VG_{n2}*)* and *error(*VG_{n3}*)* have a maximum value of 10% and 13%, respectively.

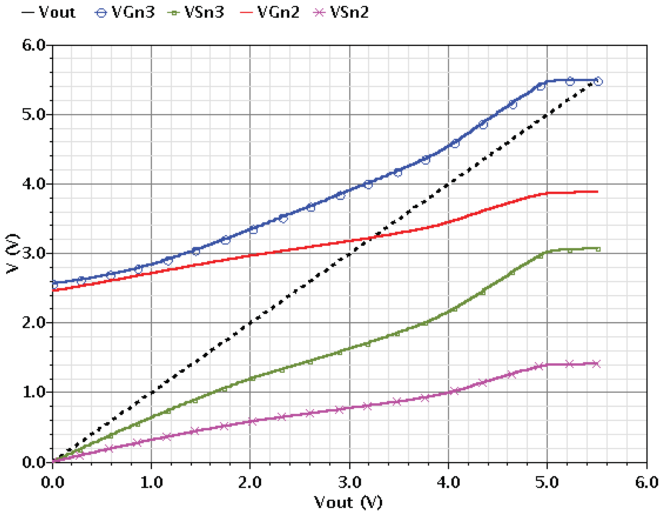
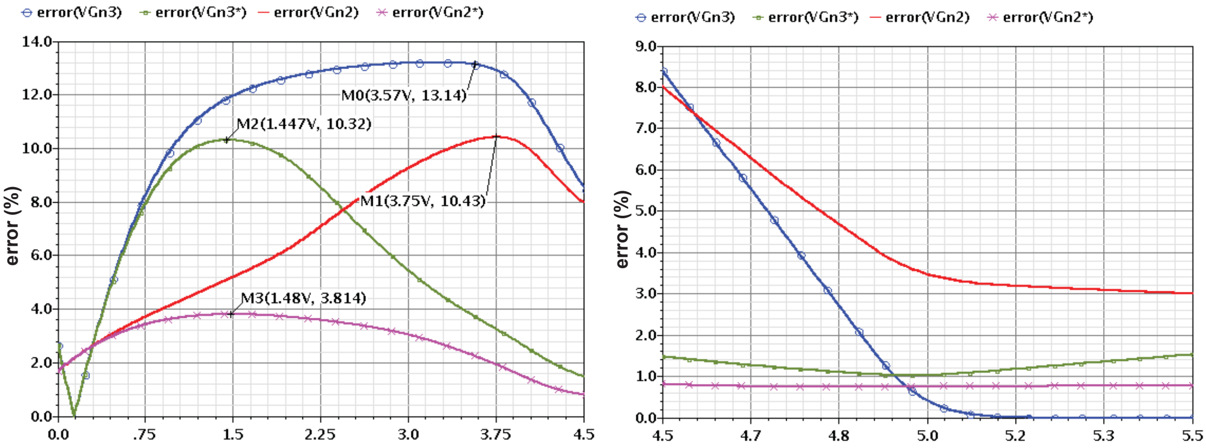


Figure 5.15: The node voltage characteristics of Mn2 and Mn3 of the driver *3HVDv1* vs. *Vout* (on-state, *VHdd*=5.5 V

From the characteristics of *error(VG_{n2}*)* and *error(VG_{n3}*)*, it can be observed that the circuit GC_{n2} has with over 96%, a higher accuracy than GC_{n3} for maintaining an offset of 2.5 V with the corresponding source voltage.



(a)

(b)

Figure 5.16: The errors of the provided gate voltages of *3HVDv1* in the range of the output voltage (a) from 0 V to 4.5 V and (b) from 4.5 V to 5.5 V (*VHdd*=5.5 V, on-state)

Figure 5.17 depicts the node voltages of the pull-down transistors (Mn2 and Mn3) for the off-state. As can be seen, these transistors are turned off by the provided gate voltages VG_{n2} and VG_{n3} when their source nodes S_{n2} and S_{n3} are charged to 1.83 V and 3.67 V, respectively. Consequently, the driver output node can be charged to 5.5 V. As a result, there is an equal voltage drop of 1.83 V (5.5 V/3) across each stacked transistor.

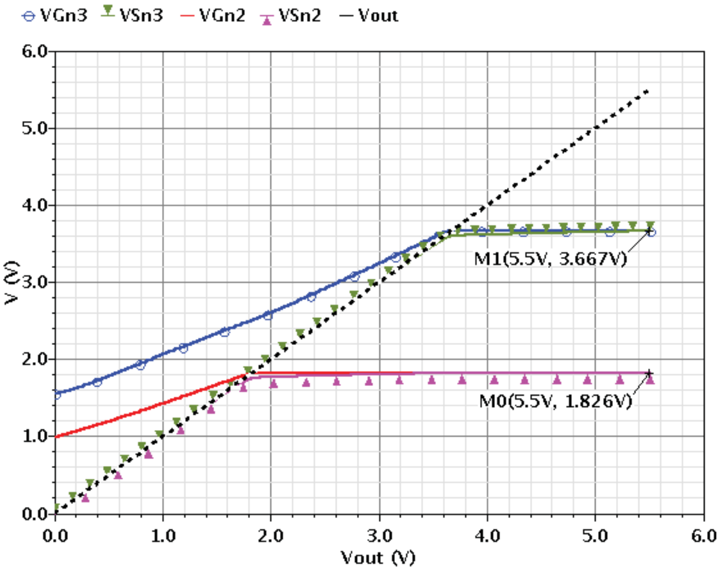


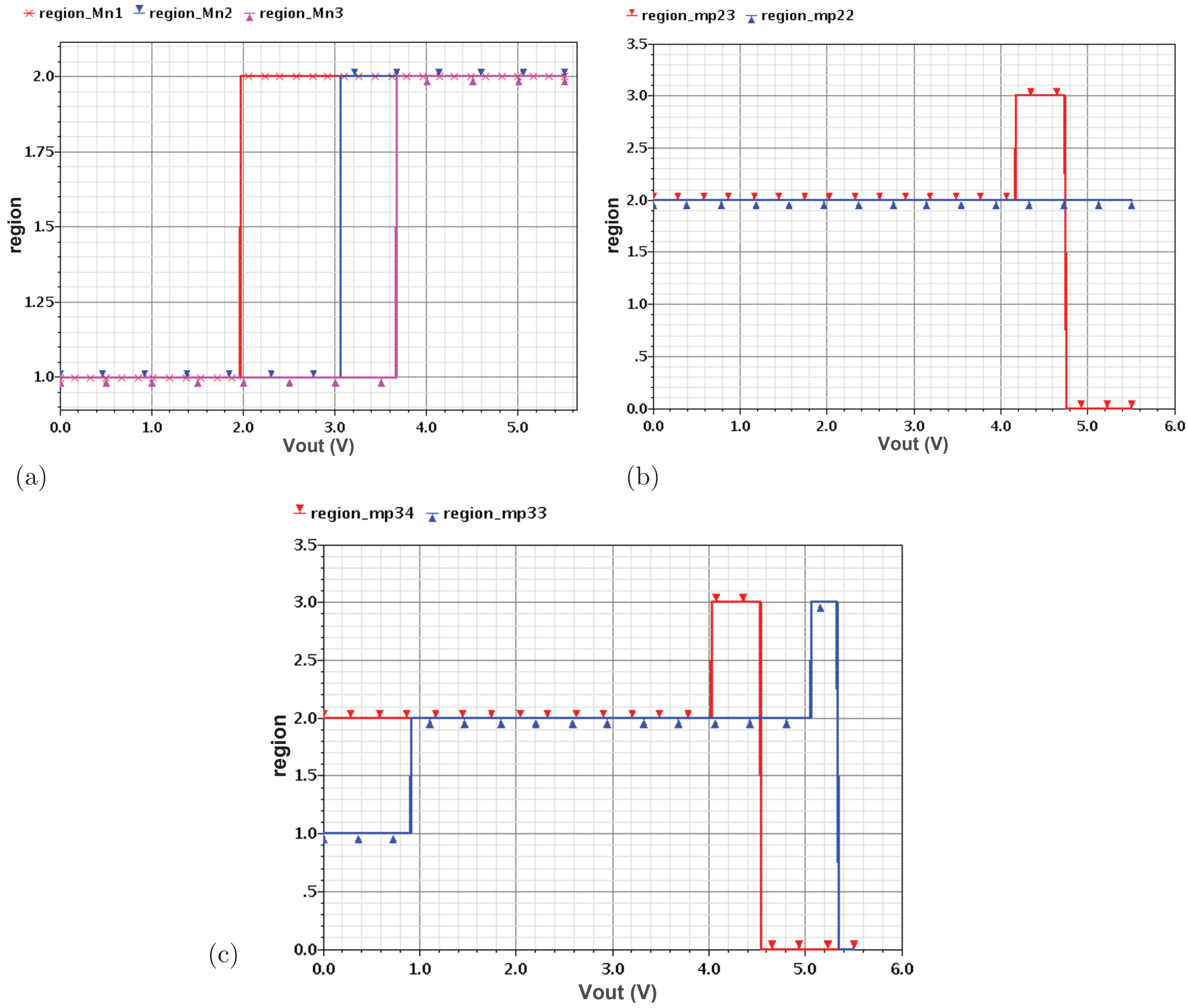
Figure 5.17: The DC node voltage characteristics of Mn2 and Mn3 of the implemented HV-driver (*3HVDv1*) vs. *Vout* (*VHdd*=5.5 V, off-state)

5.2.3 Reasons for Inaccuracy

The main reasons for the difference between the provided and calculated gate voltages are described in detail here.

1) Unequal operational regions of transistors

The rules presented in Equations (3.23) and (3.24) state that all the stacked driver transistors operate in the same region – linear or saturation –; but unfortunately, it is not the case. Figure 5.18a shows that the 3-stacked nMOS transistors Mn3, Mn2 and Mn1 of this HV-driver initially operate in the saturation region at the beginning of discharging the driver output node, thereafter they enter irregularly in the linear region, when *Vout* drops down to 3.7 V, 3.1 V and 2.0 V, respectively.



(a)

(b)

(c)

Operation regions: 0 = cut-off, 1 = linear, 2 = saturation, 3 = sub-threshold

Figure 5.18: Operation regions of the transistors (a) Mn1, Mn2, Mn3, (b) mp_{22} and mp_{23}, (c) mp_{33} and mp_{34} of *3HVDv1* in the on-state (*VHdd*=5.5 V)

The same problem is evident in the circuit $\mathrm{GC_{n2}}$ for transistors $\mathrm{mp_{22}}$ and $\mathrm{mp_{23}}$ and also in $\mathrm{GC_{n3}}$ for $\mathrm{mp_{33}}$, $\mathrm{mp_{34}}$ and $\mathrm{mp_{35}}$. For the circuit design methodology of gate-controlling circuits presented in Chapter 3, it has been assumed that the above-mentioned transistors operate steady in the saturation region. However, as can be seen in Figure 5.18b and 5.18c, transistor $\mathrm{mp_{22}}$ operates incessantly in saturation region, whereas mp23 enters in the cut-off, sub-threshold and finally into the saturation region whilst the output node discharges from 5.5 V to ground.

For *Vout* between 0.9 V and 4.0 V, transistors $\mathrm{mp_{33}}$ and $\mathrm{mp_{34}}$ of the circuit $\mathrm{GC_{n3}}$ operate together in the saturation region. Out of this range, they are not in the same operating region. Furthermore, the transistor $\mathrm{mp_{33}}$ enters into the linear region while the driver output node discharges from 0.9 V to ground.

2) Unequal threshold voltages

The next reason for the presented slight inaccuracy of the provided gate voltages is the unequal threshold voltages (V_{th}) of the stacked nMOS transistors Mn1, Mn3 and Mn2, as displayed vs. *Vout* in Figure 5.19a. Their initial values are 551 mV, 573 mV and 580 mV, respectively at *Vout* of 5.5 V.

Furthermore, the threshold voltages of $\mathrm{mp_{22}}$ and $\mathrm{mp_{23}}$ of the circuit $\mathrm{GC_{n2}}$ are not equal, as depicted in Figure 5.19b. Additionally, the threshold voltages of transistors $\mathrm{mp_{33}}$ and $\mathrm{mp_{34}}$ of the circuit $\mathrm{GC_{n3}}$ are also not identical (Figure 5.19c). These transistors are involved in the calculation to provide the required gate voltages; therefore, their threshold voltages should be identical, as assumed in the calculation for driving the same current.

3) Variable high and low rail voltages

Another reason for the diversity is that the high and low rail voltages VD_{p2}, VD_{p3}, VD_{n2} and VD_{n3} of the gate-controlling circuits, $\mathrm{GC_{n2}}$, $\mathrm{GC_{n3}}$, $\mathrm{GC_{p2}}$ and $\mathrm{GC_{p3}}$, are not uniformly constant. Figure 5.20 shows the voltage characteristics of VD_{p2} and VD_{p3}, which should have constant values of 4.0 V and 5.5 V, respectively as required for the on-state, but they have uniform characteristics with a maximum difference of 60 mV and 205 mV respectively from the desired values.

4) Modifying the reference voltages

Since for both on- and off-states, the gate-controlling circuits require different high and low-rail supply voltages (VD_{p2}, VD_{p3}, VD_{n2} and VD_{n3}) and also voltages for regulating the ancillary transistors ($\mathrm{m_{2x}}$, $\mathrm{m_{2y}}$, $\mathrm{m_{34x}}$, $\mathrm{m_{35x}}$, $\mathrm{m_{34y}}$ and $\mathrm{m_{35y}}$), the entire circuit of the designed HV-driver demands more pads than are available on the chip. Therefore, to minimise this problem, some voltages which are close to each other are considered to have one value, but this negatively affects the inaccuracy of the provided gate voltages.

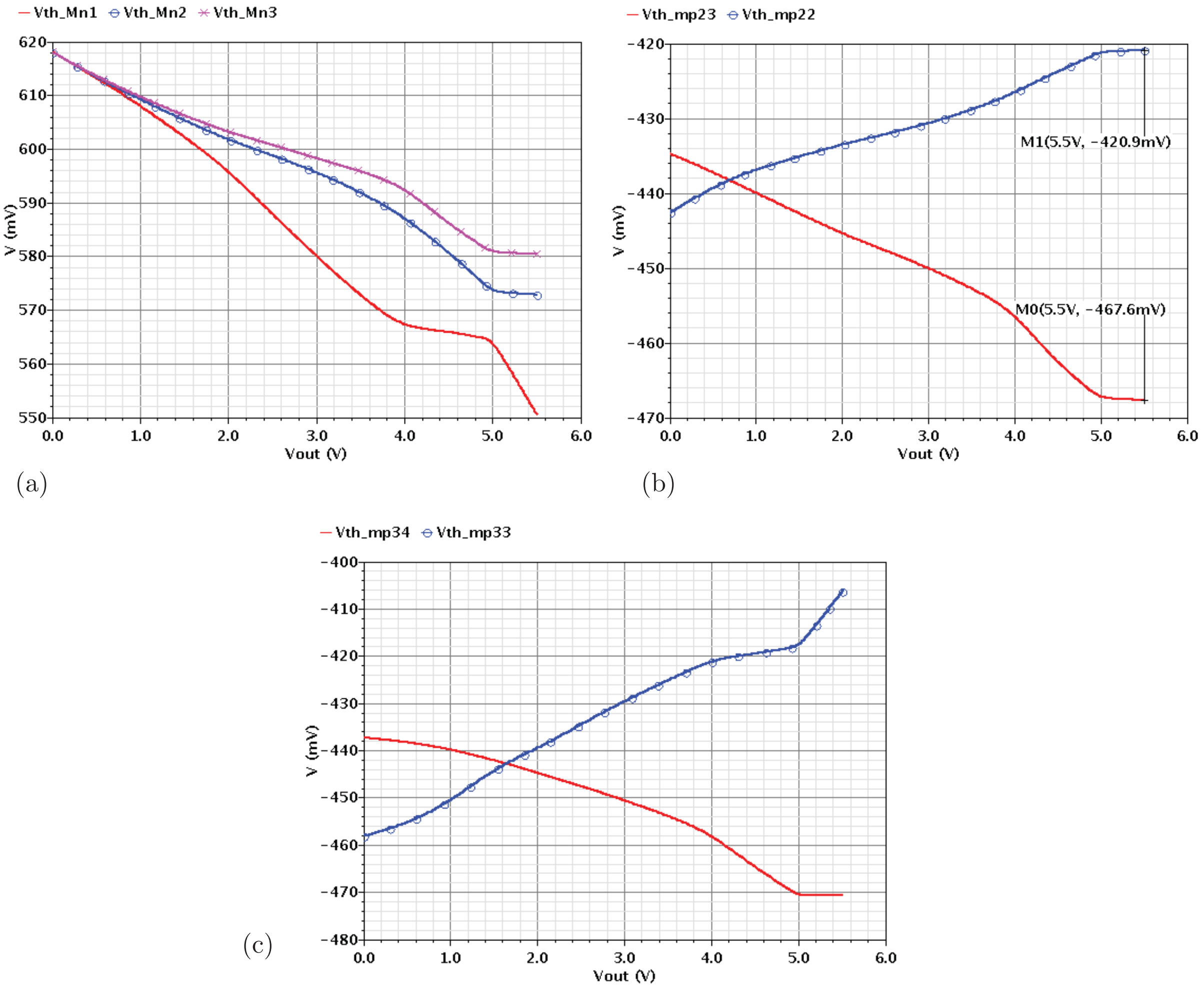


Figure 5.19: Threshold voltage characteristics of (a) Mn1, Mn2 and Mn3, (b) mp_{22}, mp_{22}, (c) mp_{33} and mp_{34} of *3HVDv1* (*VHdd*=5.5 V, on-state)

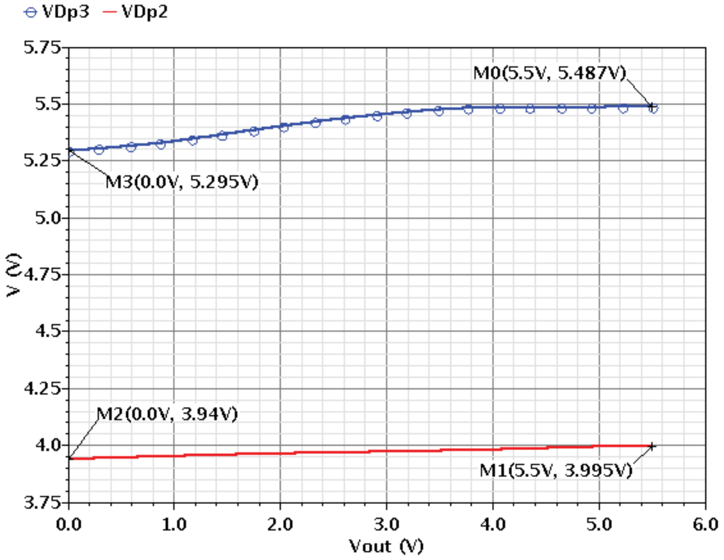


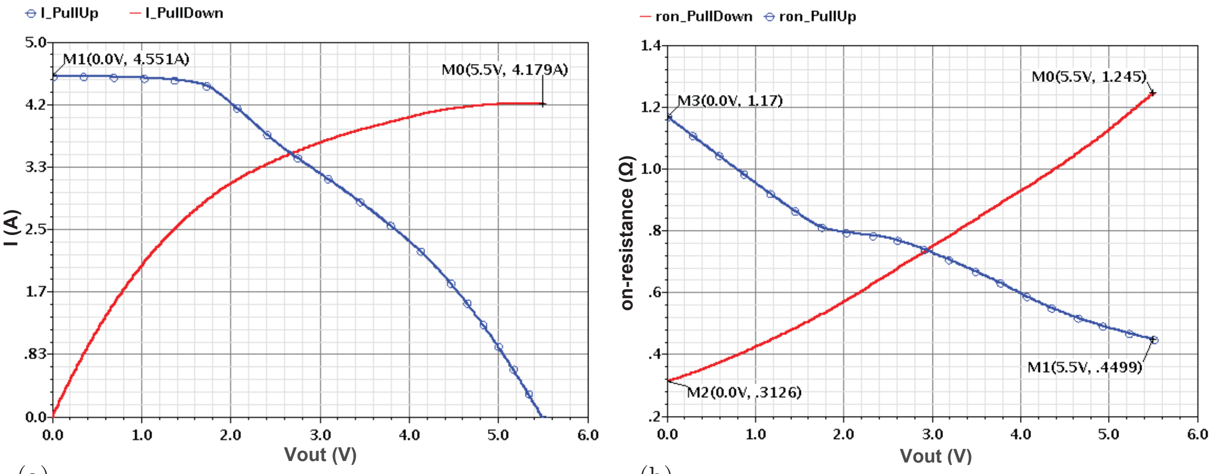
Figure 5.20: The voltage characteristics of VD_{p2} and VD_{p3} of the HV-driver *3HVDv1* in the on-state (*VHdd*=5.5 V)

5) Unequal numbers of transistors

As can be observed from Table 5.1, the numbers of transistors mn_{22} and mn_{23} of $\mathrm{GC}_{\mathrm{p2}}$, mn_{33} and mn_{34} of $\mathrm{GC}_{\mathrm{p3}}$, mp_{22} and mp_{23} of $\mathrm{GC}_{\mathrm{n2}}$, mp_{33} and mp_{34} of $\mathrm{GC}_{\mathrm{n3}}$ (see Figure 5.12) should be equal, but they are set differently from each other to avoid overvoltages. Therefore, this is one of the reasons for the deviation between generated and ideal gate voltages.

5.2.4 Comparison with Work B

Figures 5.21a and 5.21b show respectively the currents and on-resistances of the pull-up and pull-down paths. In comparison to the previously presented 3-stacked CMOS HV-driver in Section (4.2), the initial pull-up current of this driver is 0.68 A (13%) lower, and its initial pull-up and pull-down on-resistances are 18% and 5%, respectively higher. However, there are still significant advantages when compared to those of the HV-driver *B* in Figures 5.9a, 5.9b, 5.10a and 5.10b. For example, the HV-driver *3HVDv1* has initial pull-up and pull-down currents of 4.6 A and 4.2 A, whereas those of the driver *B* are 1.3 A and 2.8 A, respectively. The initial pull-up and pull-down on-resistances of 1.17 Ω and 1.245 Ω of the driver *3HVDv1* are improved by 71% and 33% respectively when compared to those of HV-driver *B*.



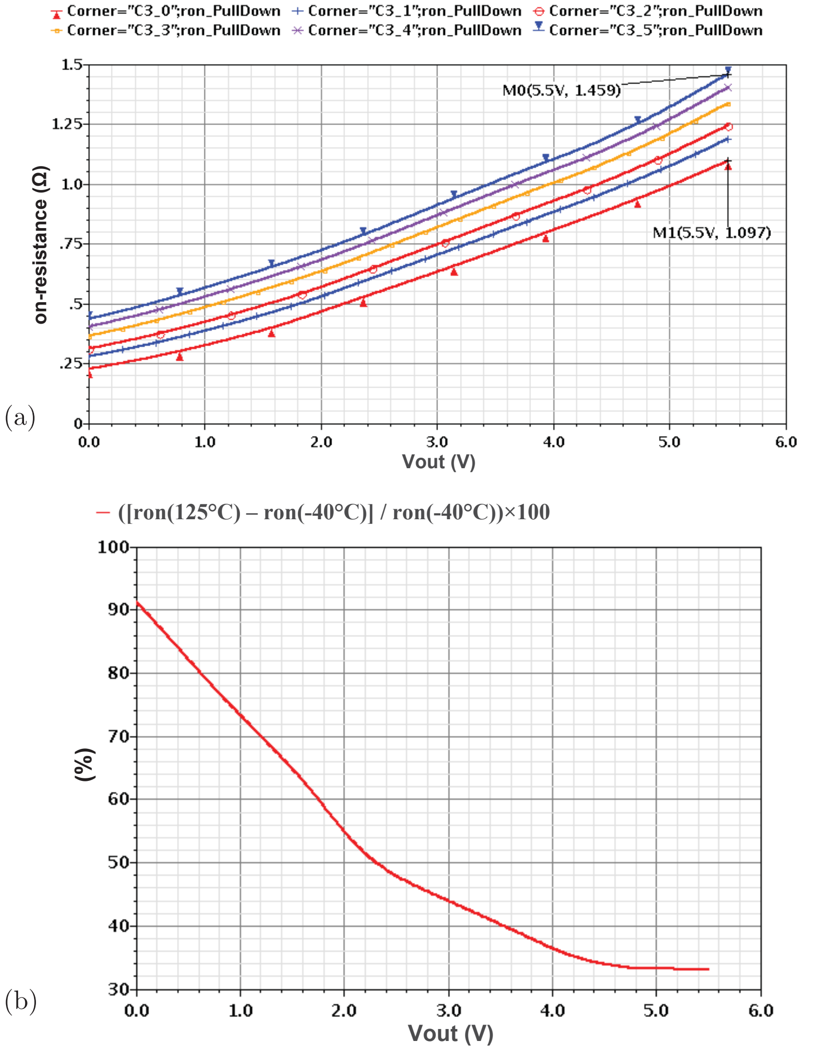
(a) (b)

Figure 5.21: The pull-up and the pull-down (a) currents and (b) on-resistances of *3HVDv1*

5.2.5 Corner Simulation

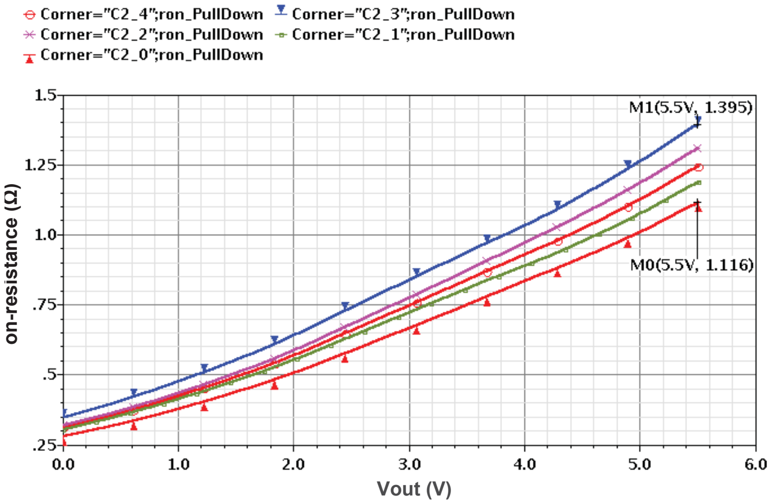
The circuit is simulated for different process variations and temperatures. Figure 5.22a shows the pull-down on-resistance versus the driver output voltage for various temperatures from –40 °C to 125 °C using the typical process "*tt*". As expected, the on-resistance increases when raising the temperature because a higher temperature leads to lower carrier mobility. With respect to the output voltage, the pull-down on-resistance at 125 °C is between 33% and 91% higher than that at the lowest temperature of –40 °C, as depicted in Figure 5.22b.

Figure 5.23 plots the pull-down on-resistance versus the driver output voltage for different process variations "*ff*", "*fs*", "*sf*", "*ss*" and "*tt*". At the corners C2_3 and C2_0, which express the slow "*ss*" and the fast process "*ff*", the on-resistance is the highest and the lowest, respectively. At the process corner "*sf*", *ron_PullDown* is higher than that at "*tt*" and this itself is greater than the result at the corner "*fs*". The deviation of the pull-down on-resistance at the corner "*ss*" from that at "*ff*" varies between 23% and 26%.



$C_{3\_0} = -40\,°\mathrm{C}$, $C_{3\_1} = 0\,°\mathrm{C}$, $C_{3\_2} = 27\,°\mathrm{C}$, $C_{3\_3} = 70\,°\mathrm{C}$, $C_{3\_4} = 100\,°\mathrm{C}$, $C_{3\_5} = 125\,°\mathrm{C}$

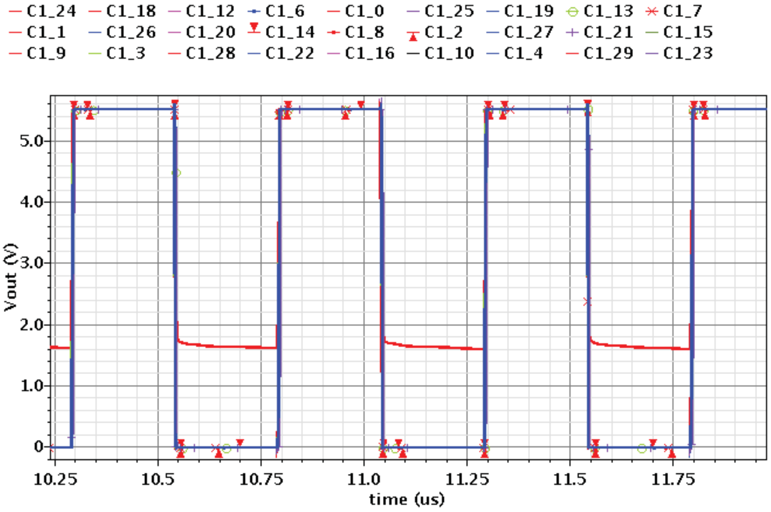
Figure 5.22: (a) The pull-down on-resistance obtained from corner simulation and (b) the worsening of the on-resistance for the temperature of 125 °C in comparison for –40 °C (typical process "*tt*")



C_{2_0} = "ff", C_{2_1} = "fs", C_{2_2} = "sf", C_{2_3} = "ss", C_{2_4} = "tt"

Figure 5.23: The pull-down on-resistance obtained from corner simulation ($T = 27°\text{C}$)

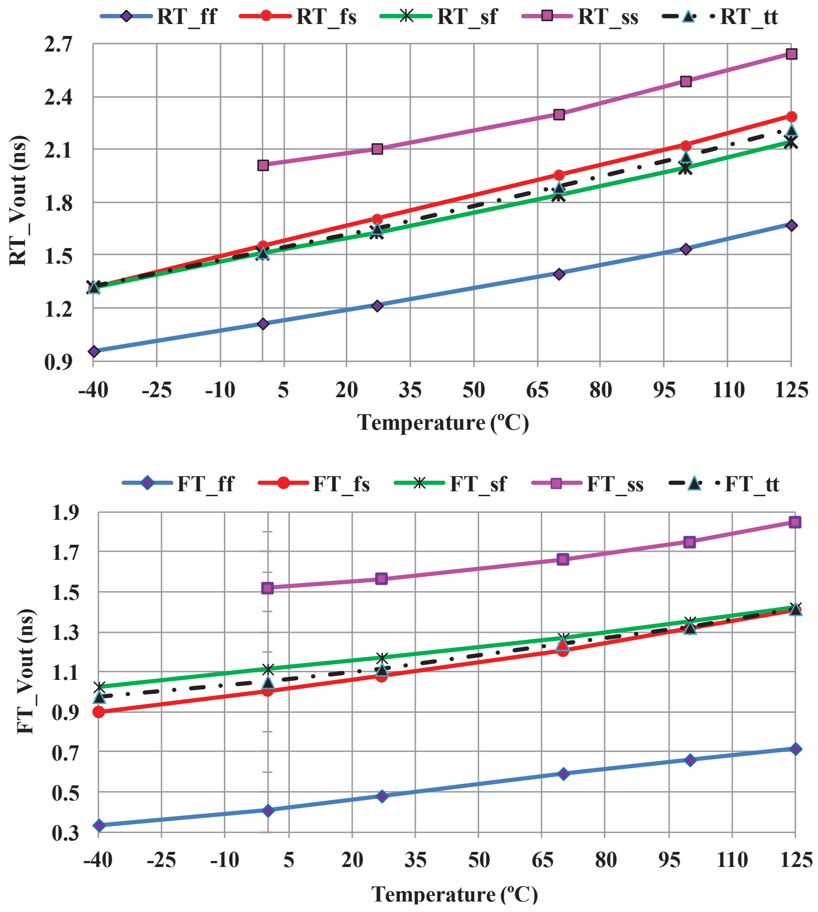
The circuit is also simulated for different combinations of process variations and temperatures (PT). The transient simulation results of the driver output signal indicate that the circuit at the corner C1_18 ("ss", –40 °C), cannot operate correctly. As shown in Figure 5.24, in the on-state (pull-down active), the driver output node discharges from 5.5 V up to 1.6 V instead to ground, since the pull-up path is still active.



C_{1_0} = -40 °C; ff	C_{1_1} = 0 °C; ff	C_{1_2} = 27 °C; ff	C_{1_3} = 70 °C; ff	C_{1_4} = 100 °C; ff
C_{1_5} = 125 °C; ff	C_{1_6} = -40 °C; fs	C_{1_7} = 0 °C; fs	C_{1_8} = 27 °C; fs	C_{1_9} = 70 °C; fs
C_{1_10}= 100 °C; fs	C_{1_11}= 125 °C; fs	C_{1_12}= -40 °C; sf	C_{1_13}= 0 °C; sf	C_{1_14}= 27 °C; sf
C_{1_15}= 70 °C; sf	C_{1_16}= 100 °C; sf	C_{1_17}= 125 °C; sf	C_{1_18}= -40 °C; ss	C_{1_19}= 0 °C; ss
C_{1_20}= 27 °C; ss	C_{1_21}= 70 °C; ss	C_{1_22}= 100 °C; ss	C_{1_23}= 125 °C; ss	C_{1_24}= -40 °C; tt
C_{1_25}= 0 °C; tt	C_{1_26}= 27 °C; tt	C_{1_27}= 70 °C; tt	C_{1_28}= 100 °C; tt	C_{1_29}= 125 °C; tt

Figure 5.24: The output voltage characteristic obtained from corner simulation

The rise times (*RT*) and fall times (*FT*) of the output voltages are plotted in Figures 5.25a and 5.25b, respectively versus the temperature. The HV-driver is in an open-load condition. As expected, these parameters are at the slow corner "*ss*" higher than those at the other process variations and at the fast corner "*ff*", they are the lowest. However, at only one corner, a desirable output voltage has not be achieved. Furthermore, at the corners for the temperatures above 70 °C and also for the fast process variation "*ff*", overvoltages up to 11% of 2.5 V occur between the terminals of each of some transistors.



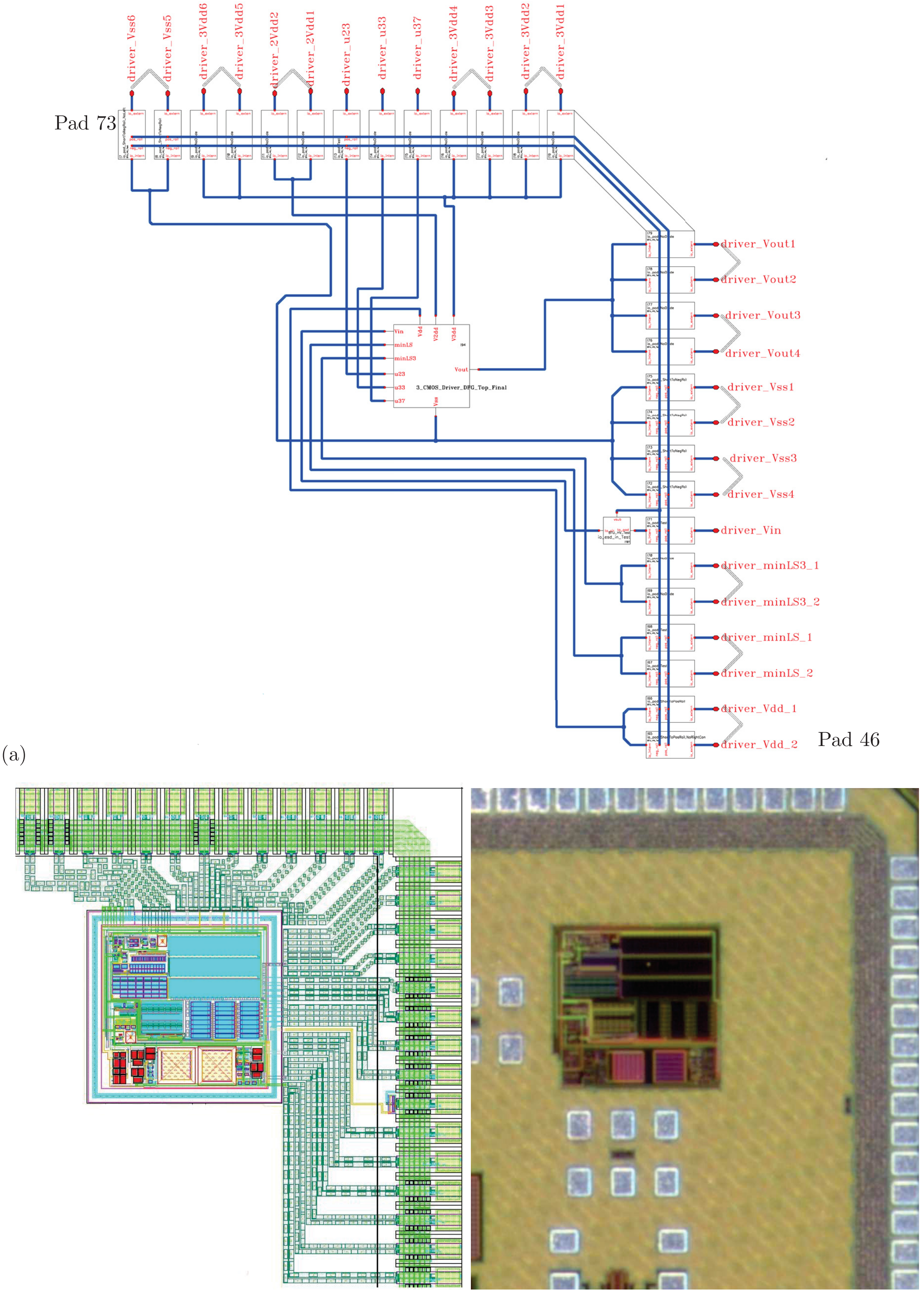
(a)

(b)

Figure 5.25: (a) Rise (*RT*) and (b) fall (*FT*) times of *Vout* obtained from corner simulation

5.2.6 Implementation on Chips

The HV-driver *3HVDv1* is implemented on a chip including 80 pads, which is designed and fabricated using CLN65LP, 65-nm CMOS TSMC technology. The chip area is 2mm×2mm. For the HV-driver, 28 pads have been determined to deliver the desired signals, as listed in Table 5.2. Figures 5.26a, 5.26b and 5.26c present the top-level schematic, the layout and a micro-photograph of the circuit on a chip, respectively.



(a)

(b)

(c)

Figure 5.26: (a) Top-level, (b) layout and (c) micro-photograph of the circuit on the chip including the pads

Table 5.2: The pads of the designed chip for the HV-driver *3HVDv1*

Pad No.	**Pad Name**	**Description**
46, 47	Vdd	2.5 V (equal to the nominal I/O voltage)
48, 49	minLS	low rail-voltage for the 1st level-shifter (=1.5 V for VHdd of 5.5 V)
50, 51	minLS3	low rail-voltage for the 2nd level-shifter (=3.0 V for VHdd of 5.5 V)
52	Vin	input signal of the HV-driver
53, 54, 55 56, 72,73	Vss	ground (0 V)
57, 58, 59, 60	Vout	driver's output signal
61, 62, 63 64, 70, 71	3Vdd	supply high-voltage (VHdd with max. value of 5.5 V)
65	u37	reference voltage (=3.7 V for VHdd of 5.5 V)
66	u33	reference voltage (=3.3 V for VHdd of 5.5 V)
67	u23	reference voltage (=2.3 V for VHdd of 5.5 V)
68, 69	2Vdd	supply voltage for the 2nd level-shifter (=4.0 V for VHdd of 5.5 V)

5.2.7 Measurement

In this work, two packaging technologies are used: chip-in-package (CIP) and chip-on-board (COB), which are tested on the printed circuit board (PCB) presented in Figures 5.27a and 5.27b. In the next sections, the measurement results of both technologies with and without overvoltage protections are presented, discussed and compared to each other. The descriptions of the chips are given in Table 5.3.

Table 5.3: Descriptions of the measured chips

Chip	**Description**
C2, C3, C4, C5, C6	chips in-package without overvoltage protection while switching the proposed buck converter
C3x, C4x, C5x, C6x	chips in-package with a capacitive load as an overvoltage protection
C5OVP	chip *C5* in-package using a resistor and Schottky diode as an overvoltage protection (OVP) while switching the buck converter
COB2, COB5	chips on-board (I) with OVP while switching the buck converter and (II) without OVP while operating in an open-load condition
COBx	chip-on-board without using OVP while switching the buck converter

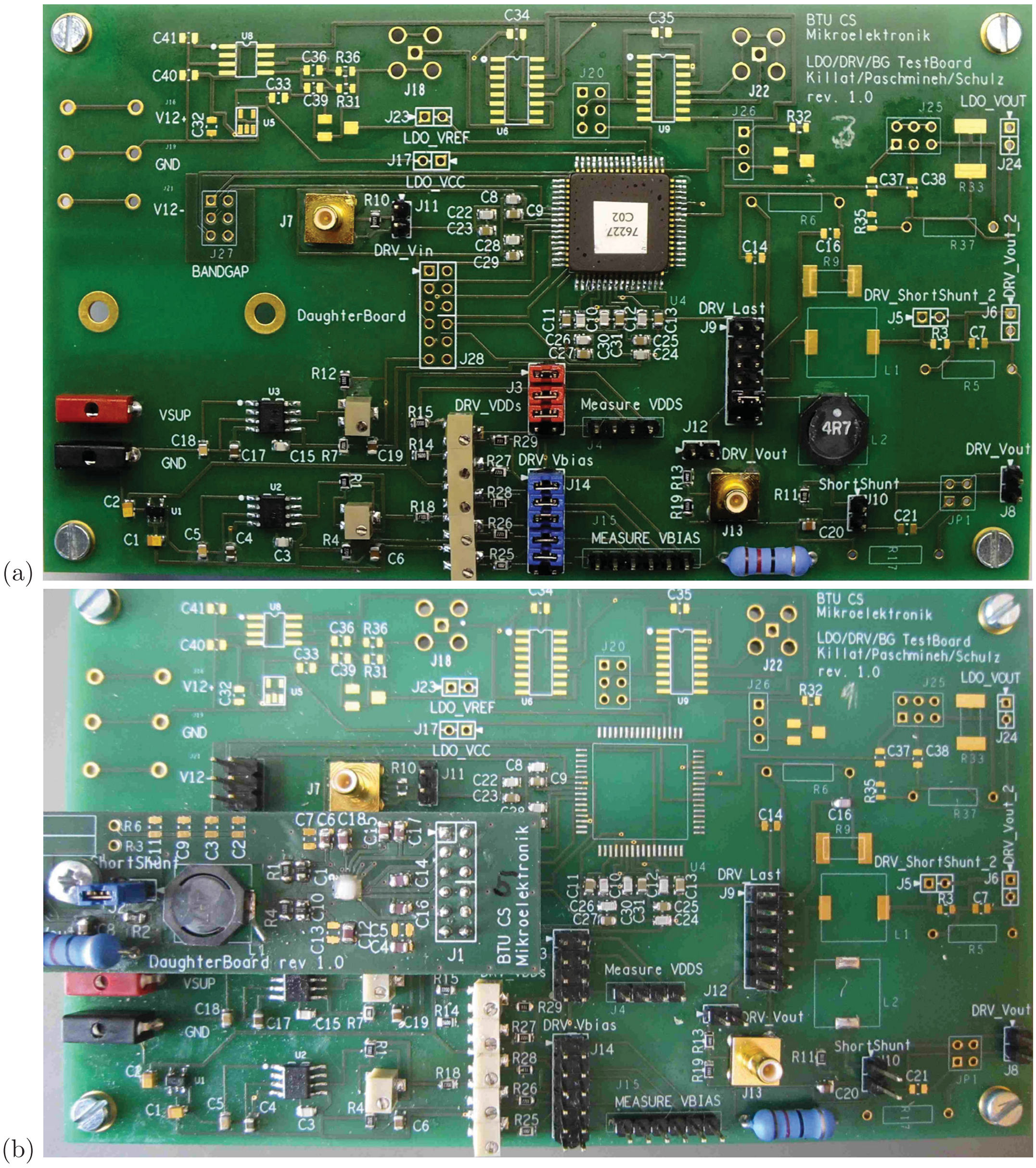


Figure 5.27: (a) Chip-in-package mounted on *PCB 3* and (b) chip-on-board attached on the daughter board 5 (*PCB 1*)

5.2.7.1 Chip-in-Package (CIP)

Regarding the technology "Chip-in-Package", the manufactured chip is bonded into a **CQFP64** package, which is defined for a **C**eramic **Q**uad **F**lat **P**ackage consisting of **64** pins (16 pins on each side). The package is mounted on the test board presented in Figure 5.27a.

Various measurements have been accomplished for proving the stability and correct functionality of the circuit in the open-, capacitive and resistive-load conditions and also by switching the proposed buck-converter, as shown in Figure 5.28, where Vin_g is the input signal provided by the voltage generator. The pull-up and pull-down driver on-resistances have been also investigated. Some undesirable parasitic effects occur during the measurement process; accordingly, different methods are employed to reduce these, which are discussed in detail here.

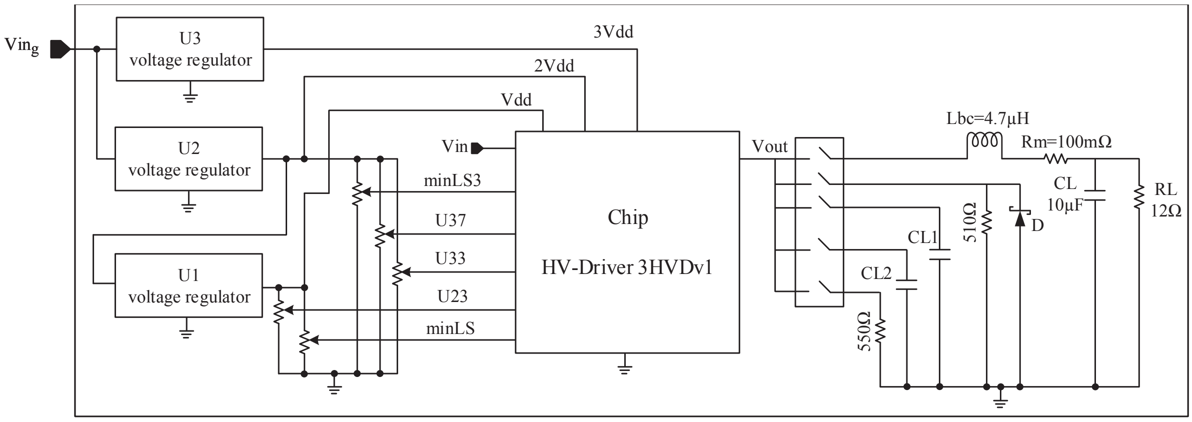


Figure 5.28: The principle of the test bench for the driver *3HVDv1* implemented on a chip

5.2.7.2 Chip-in-Package: Driver On-Resistance

To obtain the pull-down and pull-up on-resistance of the proposed HV-driver, an external current (I_{out}) varying from 0 mA to 100 mA is fed into or pulled from the chip output node, while the driver is operating in the on- or off-state. The appropriate output voltages ($Vout$) have been measured and from these the on-resistances (Ron) are calculated.

It is notable that the measurement for determining on-resistance is carried out for the steady condition. In this case, the output node had already been charged to the supply voltage or discharged to ground according to the off- and on-states.

The voltages and the respective on-resistances obtained from the post-layout simulation including the layout-induced parasitic effects are also presented here for the circuit *3HVDv1*.

A. Pull-Down On-Resistance

In the driver on-state, the output node is discharged to 0 V. By feeding current (I_{out}) into the chip output node, which flows through the active pull-down path to ground, the output voltage increases. Table 5.4 gives the measurement and simulation results of $Vout$ ($Vout_M$ and $Vout_S$) and the corresponding calculated pull-down on-resistance (Ron_S and Ron_M) according to the feeding-in currents (I_{out}).

The suffixes "*_S*" and "*_M*" of the terms *Vout* and *Ron* express results from post-layout **S**imulation and **M**easurement. The initial measured and simulated *Vout* for a current of 0 mA are 1.735 mV and 2.168 mV respectively. These values are subtracted from the measured and simulated *Vout* ($Vout_{M0}$ and $Vout_{S0}$) for different I_{out} as follows:

$$Vout_S(I_{out}) = Vout_{S0}(I_{out}) - Vout_{S0}(0\,mA) \tag{5.2a}$$

$$Vout_M(I_{out}) = Vout_{M0}(I_{out}) - Vout_{M0}(0\,mA) \tag{5.2b}$$

The on-resistance of the pull-down path is calculated by dividing $Vout_M(I_{out})$ and $Vout_S(I_{out})$ by the corresponding current (I_{out}).

Table 5.4: Pull-down on-resistance calculated from the measured and simulated *Vout*

I_{out}[mA]	$Vout_{S0}$[mV]	$Vout_S$[mV]	Ron_S[Ω]	$Vout_{M0}$[mV]	$Vout_M$[mV]	$\mathrm{Ron_M}$[Ω]	ΔRon[Ω]
0	2.4	–	–	1.7	–	–	–
1	7.3	4.9	4.91	7.3	5.6	5.59	0.69
2	12.2	9.8	4.92	12.9	11.2	5.60	0.68
3	17.1	14.7	4.92	18.5	16.8	5.60	0.68
5	27.0	24.6	4.92	29.7	28.0	5.60	0.68
10	51.7	49.3	4.93	57.7	56.0	5.60	0.67
20	101.4	99.0	4.95	113.9	112.2	5.61	0.66
30	151.6	149.2	4.97	170.3	168.6	5.62	0.65
40	202.2	199.8	4.99	227.1	225.4	5.64	0.64
50	253.2	250.8	5.02	284.5	282.7	5.65	0.64
60	304.7	302.3	5.04	342.4	340.6	5.68	0.64
70	356.6	354.2	5.06	400.9	399.1	5.70	0.64
80	409.0	406.6	5.08	460.4	458.6	5.73	0.65
90	461.8	459.4	5.11	521.2	519.4	5.77	0.67
100	518.0	515.6	5.16	582.7	580.9	5.81	0.65

As can be observed from Table 5.4 for different currents, the calculated on-resistances are not exactly equal to each other. The difference between the on-resistances obtained from the simulation and also measurement results reaches up to 0.248 Ω and 0.215 Ω for the minimum and maximum feeding currents (1 mA and 100 mA), respectively. The reason for this is that the variation of *Vout* affects the provided gate voltage VG_{n3}, since the gate of transistor mp_{33} of the gate-controlling circuit $\mathrm{GC_{n3}}$ is regulated by the driver output voltage. Therefore, the on-resistance of the stacked nMOS transistor Mn3 is modified. As a result of this, the pull-down on-resistance cannot be constant during varying the feeding current. There are also differences with an average of about 0.66 Ω between the calculated on-resistances Ron_S and Ron_M obtained from the simulation and measurement results. This results from the resistance of the measurement device, cables, contacts, bonding wires, lead frame of the package and also wires and jumper on the circuit board. The comparison between Ron_S and Ron_M versus I_{out} is shown in Figure 5.29.

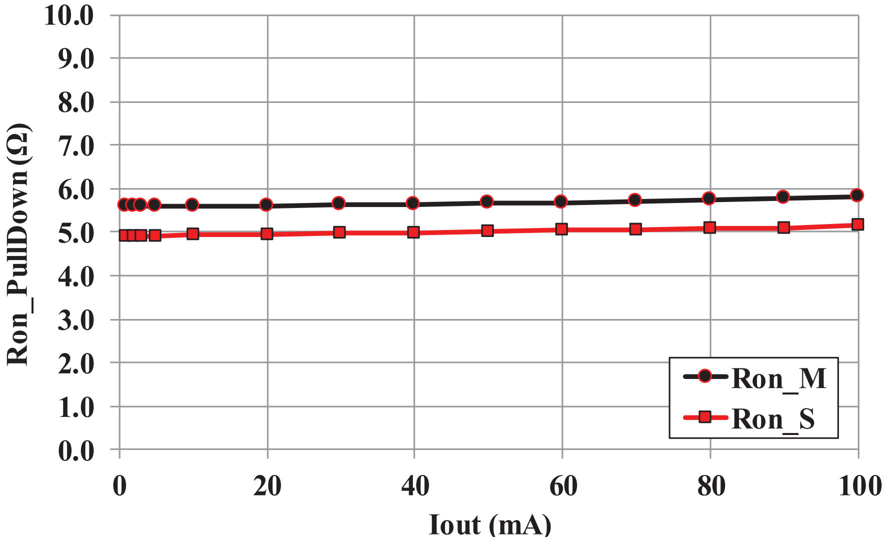


Figure 5.29: The pull-down on-resistance vs. the feeding current from measured and simulated results

B. Pull-Up On-Resistance

With an input signal of 0 V, the driver operates in the off-state and its output settles to the supply voltage (*VHdd*). By drawing current (I_{out}) from the output node with a current source, the output voltage *Vout* is reduced. The pull-up on-resistance can be calculated by dividing the voltage drop $\Delta Vout$ by the current I_{out}.

The voltage drop $\Delta Vout$ is indicated as "*VHdd–Vout*", the difference between the supply voltage of the driver (*VHdd*) and the output voltage (*Vout*) obtained from the measurement and post-layout simulation results.

With respect to the drawing currents (I_{out}), the measured and simulated output voltages ($Vout_M$ and $Vout_S$), the corresponding calculated voltage drops ($\Delta Vout_M$ and $\Delta Vout_S$) and the pull-up on-resistances (Ron_M and Ron_S) are given in Table 5.5.

The initial simulated and also measured voltage drops at current of 0 mA are 2 mV and 1.3 mV, respectively. These initial values are subtracted from the voltage drops for different pulling currents (I_{out}). The pull-up on-resistance has been calculated as follows:

$$Ron_S(I_{out}) = [VHdd_{S0}(I_{out}) - Vout_{S0}(I_{out}) - \Delta V_{dropS}(0\,mA)]/I_{out} \tag{5.3a}$$

$$Ron_M(I_{out}) = [VHdd_{M0}(I_{out}) - Vout_{M0}(I_{out}) - \Delta V_{dropM}(0\,mA)]/I_{out} \tag{5.3b}$$

where $VHdd_{M0/S0}(I_{out})$ and $Vout_{M0/S0}$ express the measured/simulated supply and output voltages. The term $\Delta V_{\mathrm{drop}}(0\,\mathrm{mA})$ is defined as:

$$\Delta V_{dropM}(0\,mA) = VHdd_{M0}(0\,mA) - Vout_{M0}(0\,mA) \tag{5.4}$$

Table 5.5: Pull-up on-resistance calculated from the measured and simulated output voltages

I_{out} [mA]	$VHdd_S$ [V]	$Vout_{S0}$ [V]	ΔV_{dropS} [V]	Ron_S [Ω]	$VHdd_M$ [V]	$Vout_{M0}$ [V]	ΔV_{dropM} [V]	$\mathrm{Ron_M}$ [Ω]	ΔRon [Ω]
0	5.4870	5.485	0.0020	–	5.5003	5.4990	0.0013	–	–
1	5.4735	5.4490	0.0045	4.50	5.5001	5.4945	0.0043	4.30	0.20
2	5.4722	5.4431	0.0091	4.55	5.4998	5.4899	0.0086	4.30	0.25
3	5.4709	5.4375	0.0134	4.47	5.4996	5.4854	0.0129	4.30	0.17
5	5.4684	5.4260	0.0224	4.48	5.4992	5.4764	0.0215	4.30	0.18
10	5.4620	5.3970	0.0450	4.50	5.4983	5.4539	0.0431	4.31	0.19
20	5.4496	5.3390	0.0906	4.53	5.4968	5.4090	0.0865	4.33	0.20
30	5.4373	5.2830	0.1343	4.48	5.4954	5.3643	0.1298	4.33	0.15
40	5.4252	5.2260	0.1792	4.48	5.4942	5.3193	0.1736	4.34	0.14
50	5.4131	5.1680	0.2251	4.50	5.4930	5.2743	0.2174	4.35	0.15
60	5.4012	5.1110	0.2702	4.50	5.4919	5.2288	0.2618	4.36	0.14
70	5.3892	5.0540	0.3152	4.50	5.4909	5.1830	0.3066	4.38	0.12
80	5.3774	4.9960	0.3614	4.52	5.4899	5.1368	0.3518	4.40	0.12
90	5.3655	4.9380	0.4075	4.53	5.4889	5.0903	0.3973	4.41	0.11
100	5.3537	4.8800	0.4537	4.54	5.4879	5.0425	0.4441	4.44	0.10

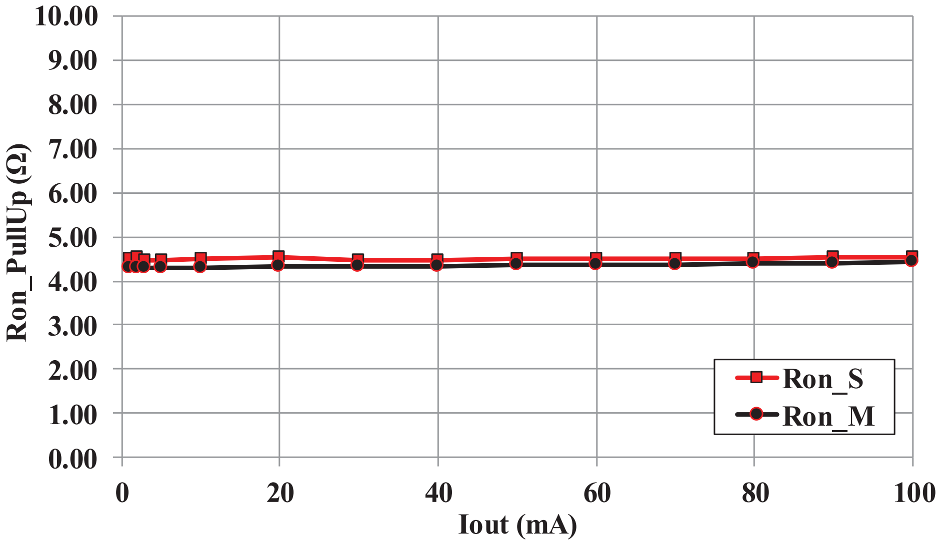


Figure 5.30: The pull-up on-resistance vs. the drawing current from measured and simulated results

The characteristics of Ron_S and Ron_M versus I_{out} are plotted in Figure 5.30. The on-resistance $\mathrm{Ron_M}$ obtained from the measurement results increases by raising the drawing current. The difference between the on-resistances at I_{out} of 1 mA and 100 mA is 140 mΩ. The reason for this is the same as described for the pull-down path. The gate of the transistor $\mathrm{mn_{33}}$ of the gate-controlling circuit $\mathrm{GC_{p3}}$ is regulated by the driver output voltage. Therefore, by changing $Vout$, the provided gate voltage VG_{p3} also varies. As a result, this affects the on-resistance of the stacked pMOS transistor Mp3. Consequently, the pull-up on-resistance cannot remain constant by varying the pulling current.

Because of the resistance of the previously mentioned objects such as cables, bonding wires and lead frame of the package, the on-resistance of the measured results is larger than that of the simulated results, but this is not the case, as measured and simulated. The reason is that the voltage supplying the main stage of the HV-driver cannot be measured. The voltage of *VHdd*, which can be measured and simulated, is not only the supply voltages of the main stage but also of the some sub-circuits such as the gate-controlling circuits, second level-shifter *LS3* and voltage divider *VDx*; therefore, the given $VHdd_M$ and $VHdd_S$ in the Table 5.5 are not the exact values as required.

5.2.7.3 Chip-in-Package: Dynamic Operation

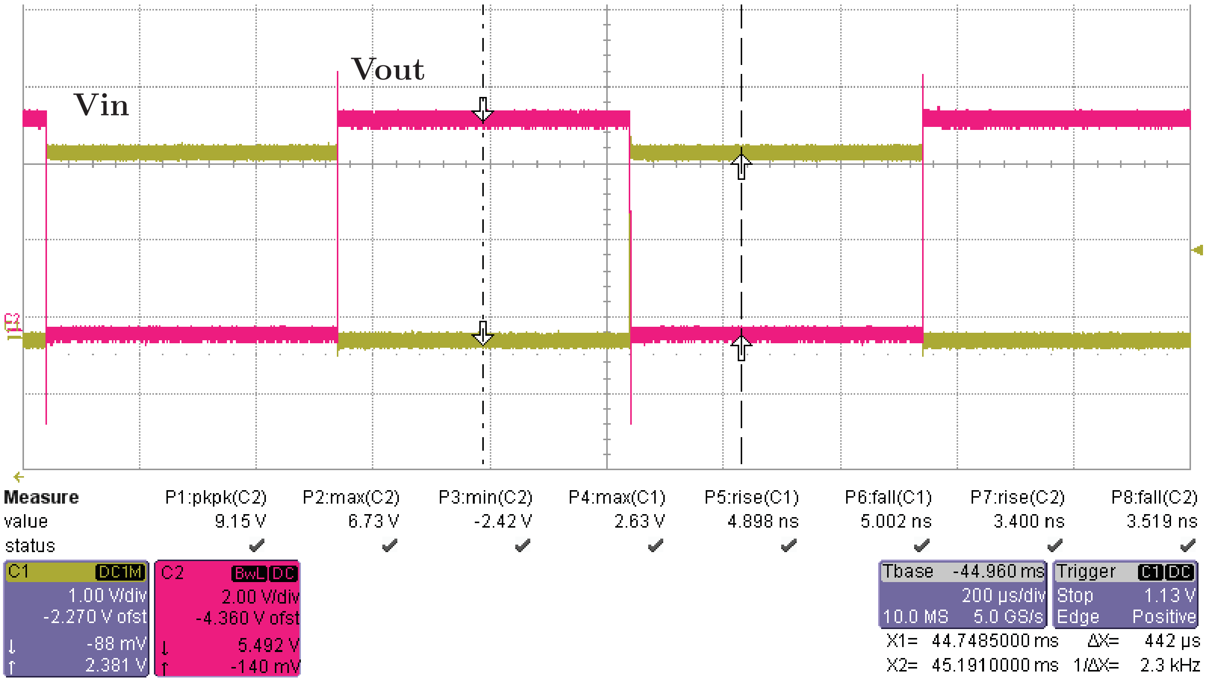
In order to verify and study the performance of the HV-driver *3HVDv1* in transient analysis, the circuit is fed with a rectangular-pulse input signal with two levels of 0 V and 2.4 V and a period of 1 ms (f= 1 kHz). Because of a high peak-to-peak amplitude, its high level is set to 2.4 V instead of 2.5 V. The circuit is supplied with 5.5 V and is tested at first in an open-load condition.

The measured waveforms of the input *Vin* (on the channel C1) and the output voltages *Vout* (on the channel C2) are displayed in Figure 5.31, and are coloured in yellow-green (lime) and red-violet, respectively. As expected, with a high level of the input signal, the output voltage is on the ground level (because of noise and ground shift, the cursor is at about –140 mV). The output voltage is high at ca. 5.5 V like the supply voltage when the input signal is low.

These high and low levels of *Vout* indicate that the driver output node discharges and charges between ground and the supply voltage. This, in turn, means that with the high level of the input signal, all pull-down transistors enter the on-state, whereas the pMOS transistors of the pull-up path are inactive; therefore, the output node can be discharged to ground. With a low input signal, the procedure is reversed; consequently, the output node can be charged to the supply voltage. As indicated in this figure, the output voltage has a high peak of 6.73 V and a low peak of –2.42 V, which are caused by the parasitic effects and will be discussed later.

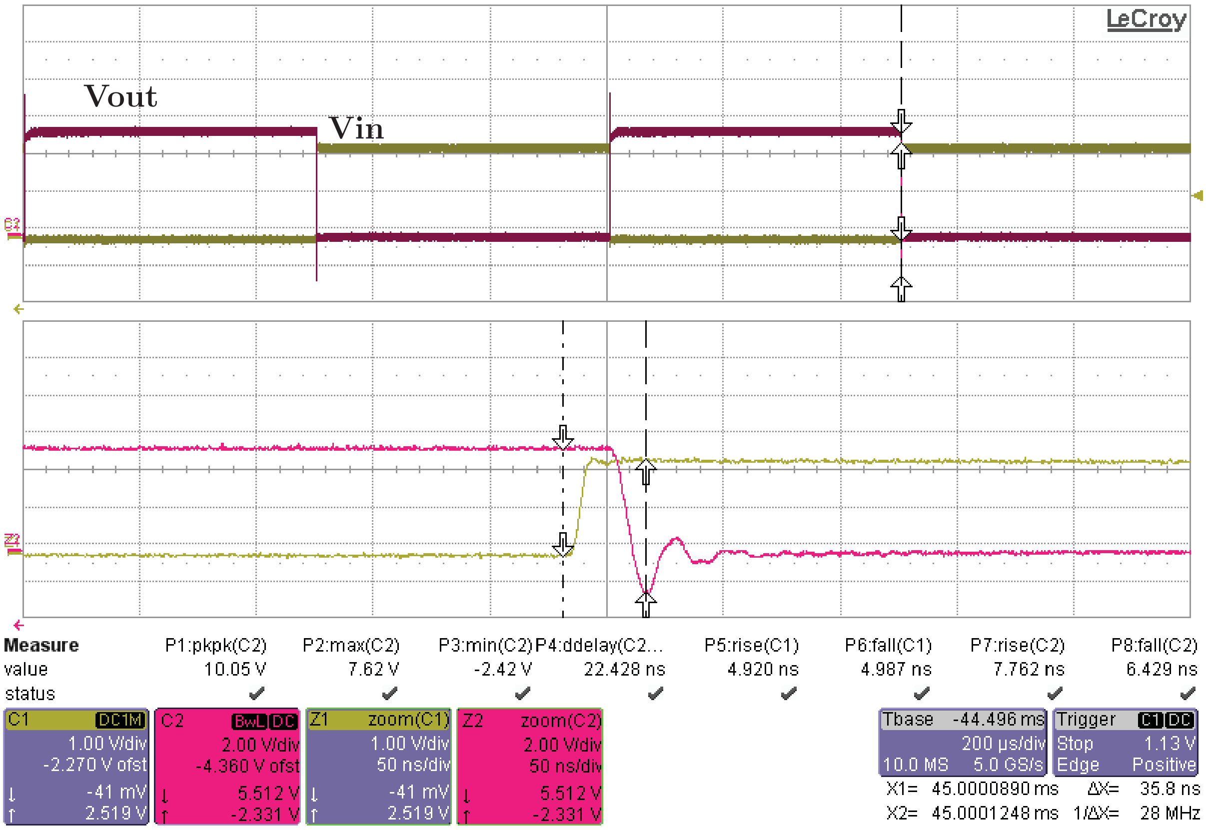
The HV-driver is proved with various loads: a resistance of 550 Ω, capacitors with values of 47 pF, 100 pF, 147 pF, 180 pF and 280 pF. In each condition of the capacitive and resistive load, the measured waveform of the output signal indicates that the HV-driver functions properly, as can be seen in Figure 5.32 with a load capacitor of 280 pF. The rise and fall times of *Vout* in comparison with the open-load condition, increase from 3.4 ns and 3.5 ns, respectively to 7.8 ns and 6.4 ns.

For various loads, Table 5.6 gives the rise times (RT), fall times (FT) and delays of the measured and also simulated *Vout* of the HV-circuit supplied with 5.5 V. It must be



```
Measure    P1:pkpk(C2)   P2:max(C2)   P3:min(C2)   P4:max(C1)   P5:rise(C1)   P6:fall(C1)   P7:rise(C2)   P8:fall(C2)
value          9.15 V       6.73 V      -2.42 V       2.63 V      4.898 ns      5.002 ns      3.400 ns      3.519 ns
status            ✓            ✓            ✓            ✓             ✓             ✓             ✓             ✓
C1        DC1M   C2       BwL DC                                         Tbase   -44.960 ms   Trigger     C1 DC
      1.00 V/div        2.00 V/div                                              200 µs/div   Stop        1.13 V
  -2.270 V ofst    -4.360 V ofst                                         10.0 MS   5.0 GS/s   Edge      Positive
↓        -88 mV   ↓      5.492 V                                         X1=  44.7485000 ms      ΔX=    442 µs
↑       2.381 V   ↑      -140 mV                                         X2=  45.1910000 ms    1/ΔX=   2.3 kHz
```

Figure 5.31: The measured waveforms of the input (C1) and output (C2) voltages ($VHdd$=5.5 V, open-load)



```
Measure    P1:pkpk(C2)   P2:max(C2)   P3:min(C2)P4:ddelay(C2...   P5:rise(C1)   P6:fall(C1)   P7:rise(C2)   P8:fall(C2)
value         10.05 V       7.62 V      -2.42 V     22.428 ns      4.920 ns      4.987 ns      7.762 ns      6.429 ns
status            ✓            ✓            ✓            ✓             ✓             ✓             ✓             ✓
C1        DC1M   C2       BwL DC   Z1     zoom(C1)   Z2     zoom(C2)     Tbase   -44.496 ms   Trigger     C1 DC
      1.00 V/div        2.00 V/div        1.00 V/div        2.00 V/div         200 µs/div   Stop        1.13 V
  -2.270 V ofst    -4.360 V ofst         50 ns/div         50 ns/div   10.0 MS   5.0 GS/s   Edge      Positive
↓        -41 mV   ↓      5.512 V   ↓       -41 mV   ↓      5.512 V   X1=  45.0000890 ms      ΔX=    35.8 ns
↑       2.519 V   ↑     -2.331 V   ↑      2.519 V   ↑     -2.331 V   X2=  45.0001248 ms    1/ΔX=    28 MHz
```

Figure 5.32: The measured waveforms of the input (C1) and output (C2) voltages ($VHdd$=5.5 V, C_L=280 pF)

considered that the simulation of the circuit is accomplished with respect to the parasitic effects created by the layout.

The reason for the difference between the simulated and measured rise- and fall times, which is significant as highlighted in Figure 5.33, is the impact of the package, PCB and also some reference voltages, which could not be set exactly as in the simulation. The suffixes "**_M**" and "**_S**" are used here to indicate the results obtained from **M**easurements and post-layout **S**imulations included impact of parasitic effects, respectively.

Table 5.6: Simulated and measured rise-, fall times and delays of *Vout* with different load-conditions (*VHdd*=5.5 V)

C_L [pF]	RT_S [ns]	FT_S [ns]	$delay_S$ [ns]	RT_M [ns]	FT_M [ns]	$delay_M$ [ns]
0	3.328	1.557	4.258	3.40	3.50	18.38
47	3.420	1.797	4.511	4.16	3.89	19.20
100	3.580	2.160	4.772	4.60	4.70	20.15
147	3.722	2.530	5.051	4.97	4.68	20.30
180	3.940	2.790	5.096	6.37	6.70	21.03
280	4.488	3.623	5.478	7.76	6.43	22.42
R_L [Ω]						
550	3.3	1.6	4.3	3.40	3.60	18.10

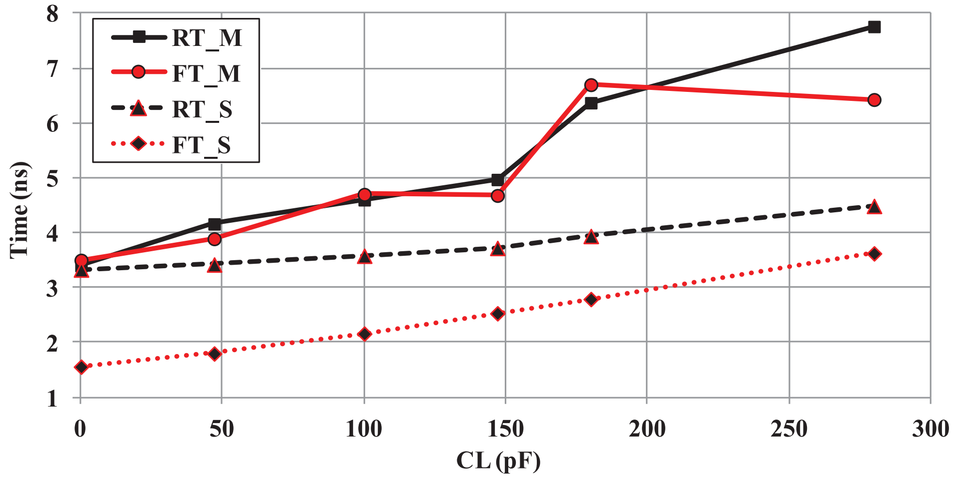


Figure 5.33: Rise- and fall times of the measured and simulated output voltage (*VHdd*=5.5 V)

The current I_{VHdd}, which flows from the source (*VHdd*) into the chip, can be measured but cannot be considered as the driver pull-up current (I_{DR}). This is because other sub-circuits, like the voltage divider *VDx*, the gate-controlling circuits $\mathrm{GC_{p2}}$, $\mathrm{GC_{p3}}$ and $\mathrm{GC_{n3}}$ and the second level shifter *LS3*, are also supplied with *VHdd* and each of these consumes part of the current I_{VHdd}.

Consequently, the pull-up current of the driver (I_{DR_M}) is estimated by multiplying the current from the simulation results (I_{DR_Sx}) with the ratio (α_{DR}). This ratio is obtained by dividing the measured current consumption by its simulated value as the equation: $\alpha_{\mathrm{DR}}=\mathrm{I}_{\mathrm{VHdd\_M}}/I_{VHdd\_Sx}$.

Table 5.7 gives details about the simulated and the measured current and dynamic power consumption for various load-conditions: open, capacitive (280 pF) and resistive (550 Ω) load conditions. The terms I_{DR} and P_{DR} express the current and the dynamic power consumption of the driver main stage, respectively. The flowing current through the load-resistor (I_{RL_M}) is measured to be 4.91 mA. It should be noted that the average of the current is considered, since the current I_{DR} can draw from the supply when the pull-up path is active. The power consumption of the chip (P_{Chip}) is obtained from the measurement results as follows:

$$P_{Chip} = I_{VHdd} \times VHdd + I_{2Vdd} \times 2Vdd + I_{Vdd} \times Vdd \tag{5.5}$$

In Table 5.7, the suffix "_Sx" indicates the results obtained from pre-layout simulations.

Table 5.7: Current and power consumption of the HV-driver and its main stage (*VHdd*=5.5 V)

Condition	I_{VHdd_M} *[mA]*	I_{VHdd_Sx} *[mA]*	I_{DR_Sx} *[mA]*	α_{DR}	I_{DR_M} *[mA]*	P_{DR} *[mW]*	P_{Chip} *[mW]*
Open-load	13.90	19.38	6.20	0.72	4.447	24.5	84.7
C_L=280 pF	13.93	20.36	7.21	0.68	4.937	27.2	84.7
R_L=550 Ω	18.851	24.21	11.06	0.72	9.338	51.4	111.4

5.2.7.4 Chip-in-Package: Stability of HV-Driver

For proving the stability of the HV-driver, the output voltage of the chip has been closely observed with repeatedly connecting and abruptly disconnecting a load resistance (R_L) of 550 Ω for two conditions:

I) The input signal is a rectangular pulse with levels of 0 V and 2.5 V

II) The input signal is 0 V (off-state)

In both cases, the transient waveforms and also the mean value of *Vout* have been kept under observation during connecting and after disconnecting the load resistance (R_L) of 550 Ω. It is considered, that the external supply voltage (Vin_g) must be set to at least 6.5 V regarding the data sheet of the voltage regulators, U1, U2 and U3, which are mounted on the PCB (Figures 5.27a and 5.28) to provide stable voltages such of *VHdd* of 5.5 V.

After disconnecting with R_L, the form and value of the transient characteristic of *Vout* have remained unchanged without the appearance of any peaks, if compared with those before disconnection. This confirms the stability of the circuit. The results of *Vout*, *VHdd*, the supply current I_{VHdd} and the current driving through the load resistance I_{RL} are given in Table 5.8 regarding the test steps. I_{VHdd} is the average current with the 50% duty cycle of *Vin*. Therefore, the theoretical shift of I_{VHdd} with R_L of 550 Ω should be 5.0 mA, which is close to the measured 4.8 mA.

Table 5.8: Measured values of *Vout*, *VHdd*, I_{VHdd} and I_{RL} in connection with proving the stability of the HV-driver *3HVDv1*

<table>
<tr><th colspan="5">I. Vin: rectangular pulse form (0 V/2.5 V), Vin_g=6.5 V (stable area)</th></tr>
<tr><td><i>step</i></td><td><i>load condition</i></td><td><i>VHdd [V]</i></td><td>I_{VHdd} <i>[mA]</i></td><td>$Vout_{mean}$ <i>[V]</i></td></tr>
<tr><td>1.</td><td><i>open load</i></td><td>5.5003</td><td>13.94</td><td>2.7328</td></tr>
<tr><td>2.</td><td><i>connecting with</i> R_L</td><td>5.4983</td><td>18.73
(I_{RL}= 4.79)</td><td>2.7110</td></tr>
<tr><td>3.</td><td><i>disconnecting from</i> R_L</td><td>5.5003</td><td>13.94</td><td>2.7328</td></tr>
<tr><th colspan="5">II. Vin=0 V (off-state), Vin_g=6.5 V (stable area)</th></tr>
<tr><td><i>step</i></td><td><i>load condition</i></td><td><i>VHdd [V]</i></td><td>I_{RL} <i>[mA]</i></td><td><i>Vout [V]</i></td></tr>
<tr><td>1.</td><td><i>open load</i></td><td>5.5012</td><td>–</td><td>5.4998</td></tr>
<tr><td>2.</td><td><i>connecting with</i> R_L</td><td>5.4991</td><td>9.88</td><td>5.4559</td></tr>
<tr><td>3.</td><td><i>disconnecting from</i> R_L</td><td>5.5012</td><td>–</td><td>5.4998</td></tr>
</table>

5.2.7.5 Chip-in-Package: Lower Supply Voltages

As previously mentioned, the circuit is designed based upon the theories described in Equations (3.11), (3.23), (3.24), (3.33), (3.34) and (3.35), but for reducing the circuit area, the number of transistors in each stack of the gate-controlling circuit has been reduced and some reference voltages have been unified. Therefore, in terms of maintaining each transistor in the safe operation region, the circuit *3HVDv1* is suitable only for the supply voltage of 5.5 V in order to follow the theories. However, this circuit (*3HVDv1*) has been also proved for lower supply voltages.

Two voltage generators *U2* and *U3*, which are mounted on the circuit board, as can be seen in Figure 5.34, provide the supply voltages "*VHdd*", "*2Vdd*", "*Vdd*" and also the supply voltage of the voltage dividers assembled on the PCB, which generate reference voltages such as "*minLS*" and "*minLS3*". A DC input voltage (Vin_g) operate both generators. Regarding the data sheets, this input voltage should be in the range between 6.5 V and 15 V to provide stable voltages. Based on this range, the voltage generators *U2*

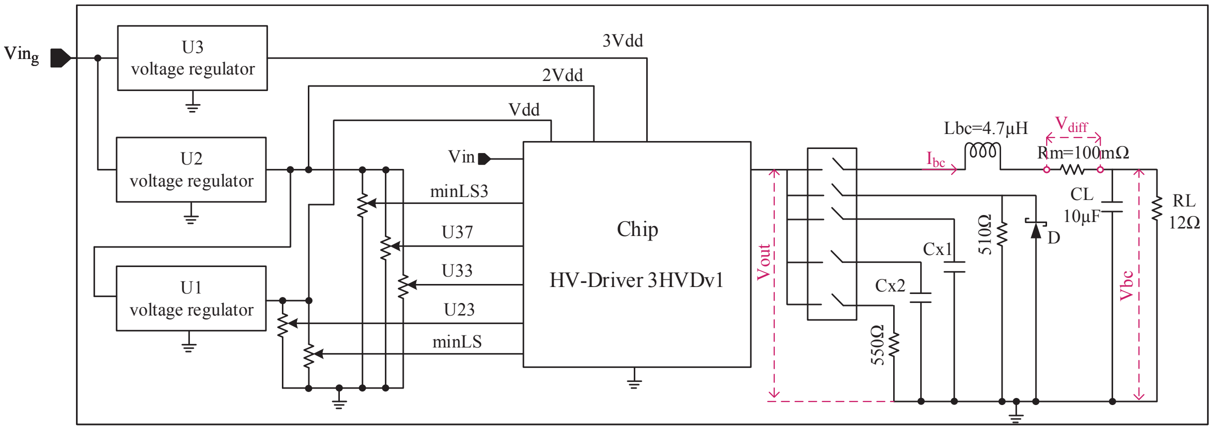


Figure 5.34: The principle of the PCB for testing the driver *3HVDv1*

and *U3* are adjustable for applications in the ranges from 4.4 V to 5.5 V and from 3.4 V to 4.2 V, respectively.

However, with decreasing the DC input voltage of the generator, stable supply and reference voltages have been achieved, which have been permanently proved by controlling their values using a measurement device and monitoring their transient waveforms on an oscilloscope.

With provided stable supply and reference voltages, the HV-driver is proved at lower supply voltages (*VHdd*) between 2.6 V and 5.5 V with a pulse input signal (0 V / 2.4 V) in an open-load condition. As can be seen in Figure 5.35a, with a supply voltage of 2.7 V, the circuit has an approximately rectangular pulse form signal at its output node. The level-shifted voltage *Vpin* of about 1.95 V is not low enough for a faster flowing current from the supply to the pull-up nodes, whereas the gate-source of the pMOS transistor Mp3 of about 1.85 V is high enough to quickly drive the current from its source node (S_{p3}) to the output node. In contrast, the falling edge of *Vout* with a fall time of 2.2 ns indicates that the driver switches much faster in the on-state, when the input signal is high.

The measurement results show that the circuit with a supply voltage over 2.8 V switches faster and has a rectangular form as desirable. As can be seen in Figure 5.35b, the output of the circuit supplied with 2.8 V has a rectangular pulse shape with nearly sharp edges. The rise- and fall times of the flanks are about 3.3 μs and 2.2 ns, respectively.

For various supply voltages from 2.6 V to 5.5 V, the output waveforms of three different chips *C2*, *C4* and *C5* have been observed on the oscilloscope. The chips *C2* and *C4* are mounted one after the other on the printed circuit board **PCB 2** and *C5* on **PCB 3**. From the displayed output pulse, the rise- and fall times have been obtained. The measured rise times (RT_{C2}, RT_{C4} and RT_{C5}) decrease rapidly from ca. 100 μs to about 7.3 ns when increasing the supply voltage from 2.6 V to 3.5 V. For *VHdd* over 3.8 V, rise times for the output voltage of all three chips vary between 3.0 ns and 3.5 ns (Figure 5.36a).

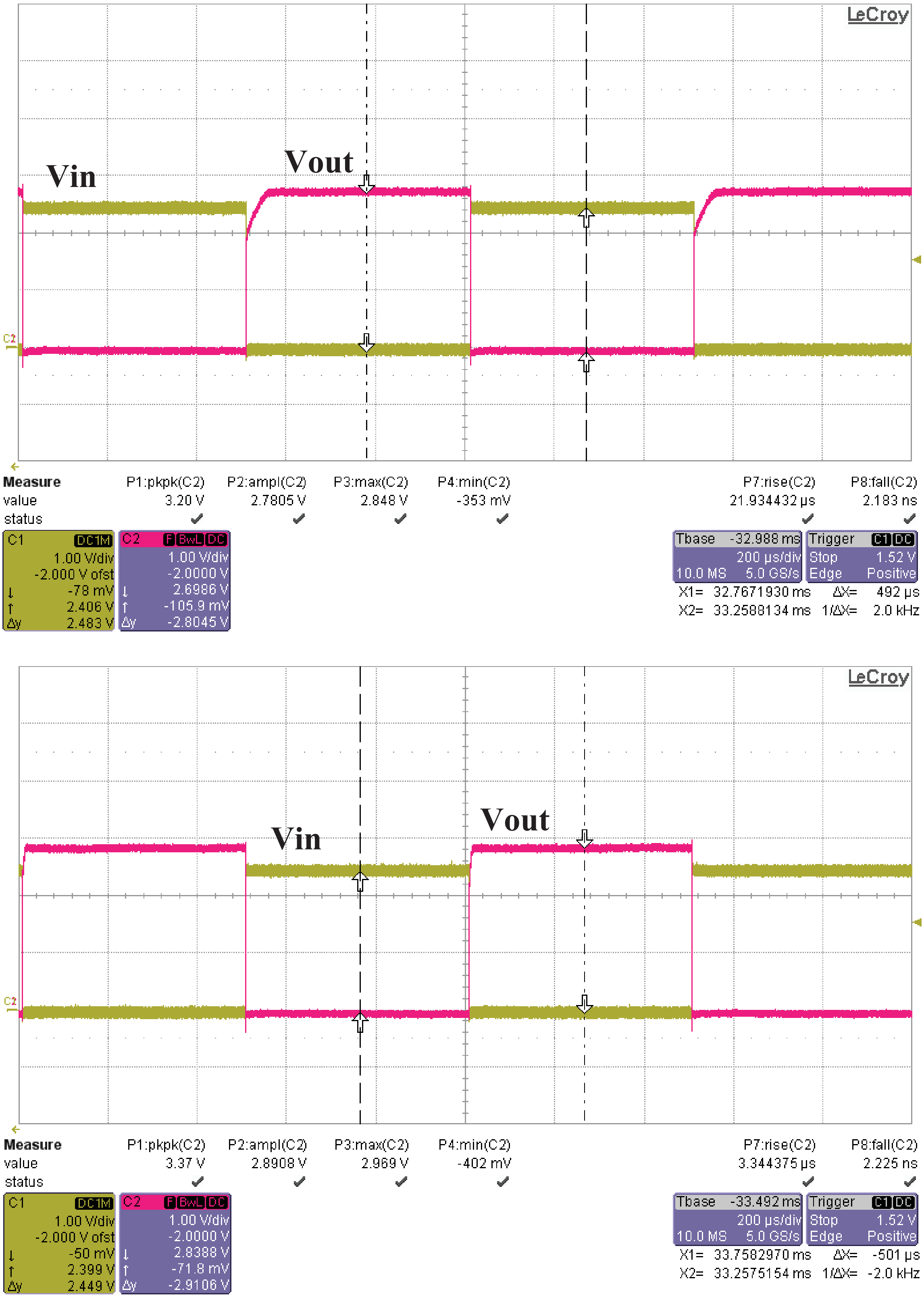
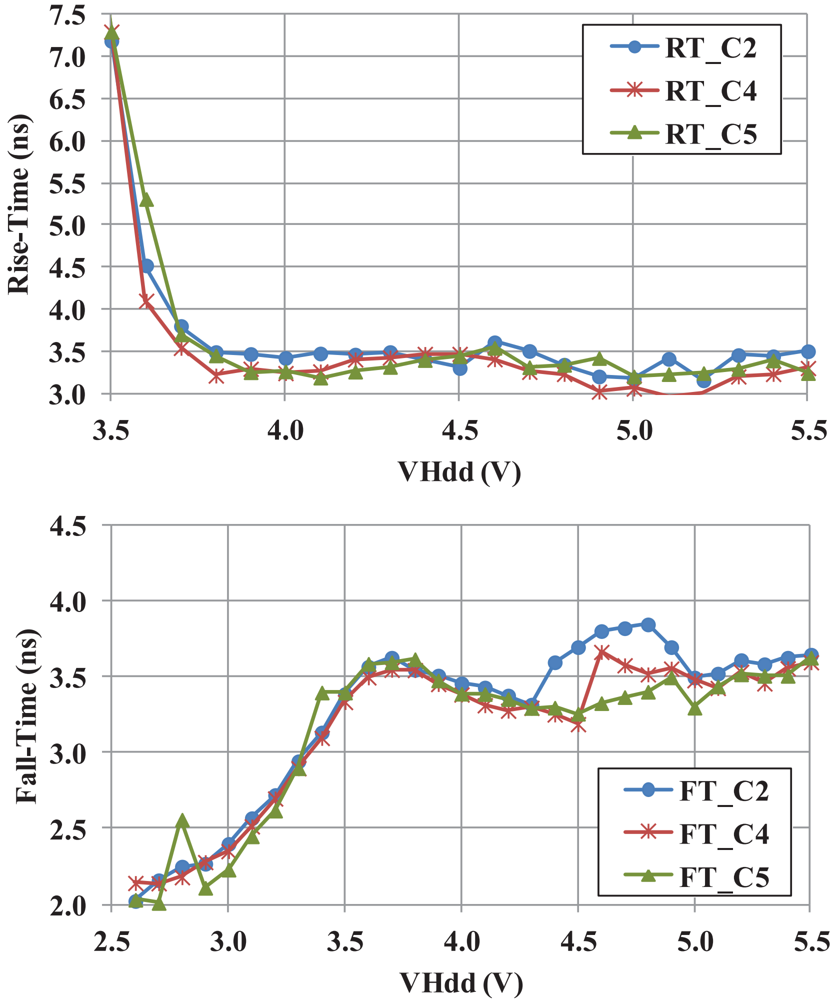


Figure 5.35: The measured waveforms of the input (channel C1) and output (channel C2) voltages of 3HVDv1 with *VHdd* of (a) 2.7 V and (b) 2.8 V (open-load)

In contrast, for all supply voltages between 2.6 V and 5.5 V, the outputs have fall times (FT_{C2}, FT_{C4} and FT_{C5}) in the range of a few nanoseconds, which are lower than 3.8 ns. By raising the supply high-voltage (*VHdd*) from 2.6 V to 3.6 V, the fall times increase from about 2.0 ns to ca. 3.5 ns and after that they swing between 3.2 ns and 3.8 ns as shown in Figure 5.36b.



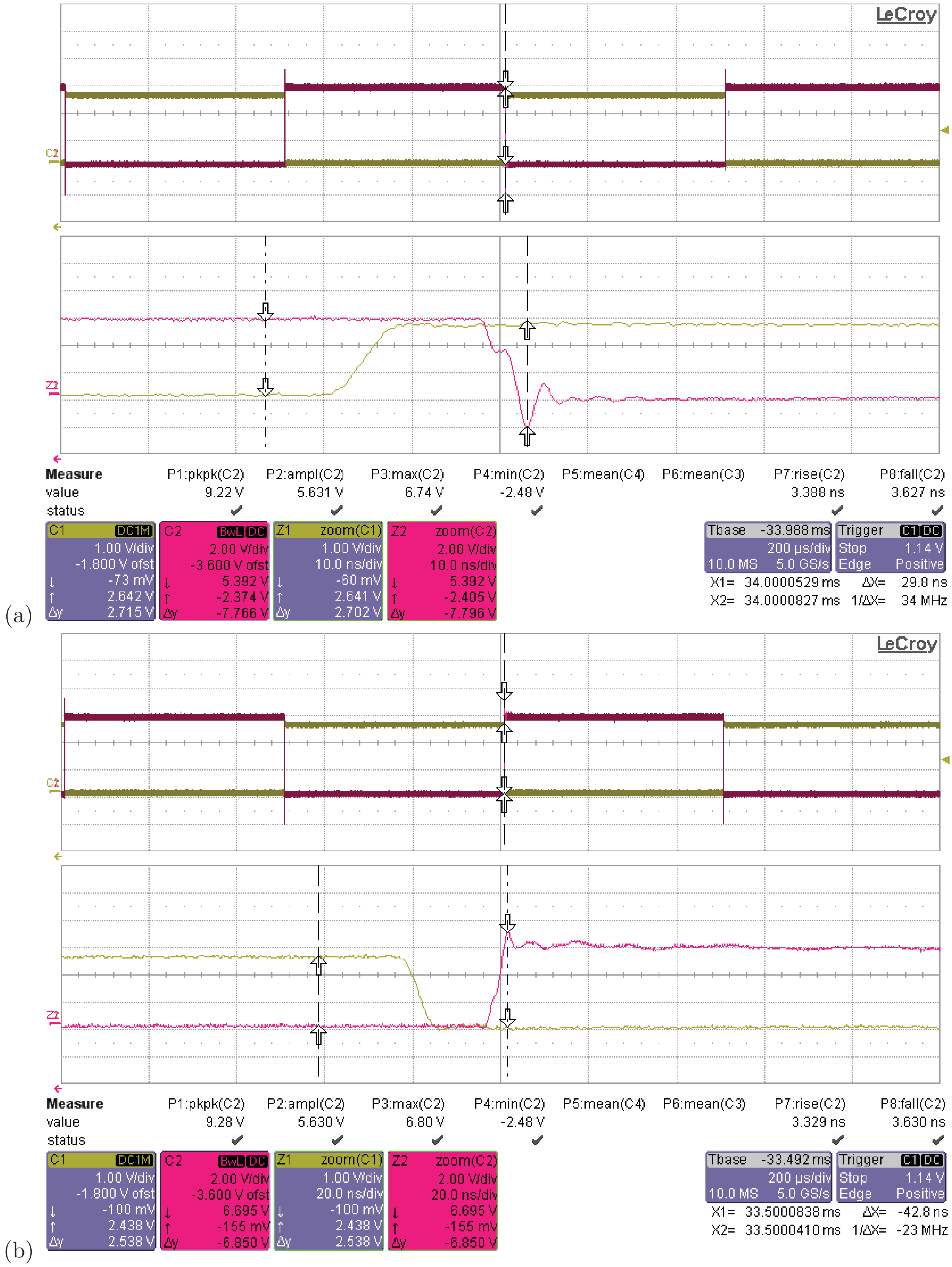
(a)

(b)

Figure 5.36: The measured (a) rise- and (b) fall times of the output voltage of the chips *C2*, *C4* and *C5* with respect to the high supply voltage *VHdd*

5.2.7.6 Chip-in-Package: Output Peaks

The output waveform of the chip manifests positive and negative peaks, which increase with raising the supply voltage. Figures 5.37a and 5.37b shows the positive and negative peaks (1.3 V and –2.5 V) of the output waveform for the Chip *C4* with a supply voltage of 5.5 V. These overvoltages are caused due to the parasitic effects, which will be discussed later.



(a)

Measure	P1:pkpk(C2)	P2:ampl(C2)	P3:max(C2)	P4:min(C2)	P5:mean(C4)	P6:mean(C3)	P7:rise(C2)	P8:fall(C2)
value	9.22 V	5.631 V	6.74 V	-2.48 V			3.388 ns	3.627 ns
status	✓	✓	✓	✓			✓	✓

C1 DC1M 1.00 V/div -1.800 V ofst ↓ -73 mV ↑ 2.642 V Δy 2.715 V
C2 BwL DC 2.00 V/div -3.600 V ofst ↓ 5.392 V ↑ -2.374 V Δy -7.766 V
Z1 zoom(C1) 1.00 V/div 10.0 ns/div ↓ -60 mV ↑ 2.641 V Δy 2.702 V
Z2 zoom(C2) 2.00 V/div 10.0 ns/div ↓ 5.392 V ↑ -2.405 V Δy -7.796 V
Tbase -33.988 ms 200 µs/div 10.0 MS 5.0 GS/s
Trigger C1 DC Stop 1.14 V Edge Positive
X1= 34.0000529 ms ΔX= 29.8 ns
X2= 34.0000827 ms 1/ΔX= 34 MHz

(b)

Measure	P1:pkpk(C2)	P2:ampl(C2)	P3:max(C2)	P4:min(C2)	P5:mean(C4)	P6:mean(C3)	P7:rise(C2)	P8:fall(C2)
value	9.28 V	5.630 V	6.80 V	-2.48 V			3.329 ns	3.630 ns
status	✓	✓	✓	✓			✓	✓

C1 DC1M 1.00 V/div -1.800 V ofst ↓ -100 mV ↑ 2.438 V Δy 2.538 V
C2 BwL DC 2.00 V/div -3.600 V ofst ↓ 6.695 V ↑ -155 mV Δy -6.850 V
Z1 zoom(C1) 1.00 V/div 20.0 ns/div ↓ -100 mV ↑ 2.438 V Δy 2.538 V
Z2 zoom(C2) 2.00 V/div 20.0 ns/div ↓ 6.695 V ↑ -155 mV Δy -6.850 V
Tbase -33.492 ms 200 µs/div 10.0 MS 5.0 GS/s
Trigger C1 DC Stop 1.14 V Edge Positive
X1= 33.5000838 ms ΔX= -42.8 ns
X2= 33.5000410 ms 1/ΔX= -23 MHz

Figure 5.37: The measured waveforms of the input (channel C1) and output (channel C2) voltages of Chip *C4* with the respective (a) falling edge and (b) rising edge of *Vout* (*VHdd*=5.5 V and pen-load)

Figure 5.38a illustrates the differences between the maximum and the amplitude of the output voltages of the chips *C2*, *C3*, *C4* and *C5*, which are defined here as high peaks and termed as *HP_C2*, *HP_C3*, *HP_C4* and *HP_C5*. The chip *C5* is replaced on **PCB 3** after completing the measurement of the chip *C3*.

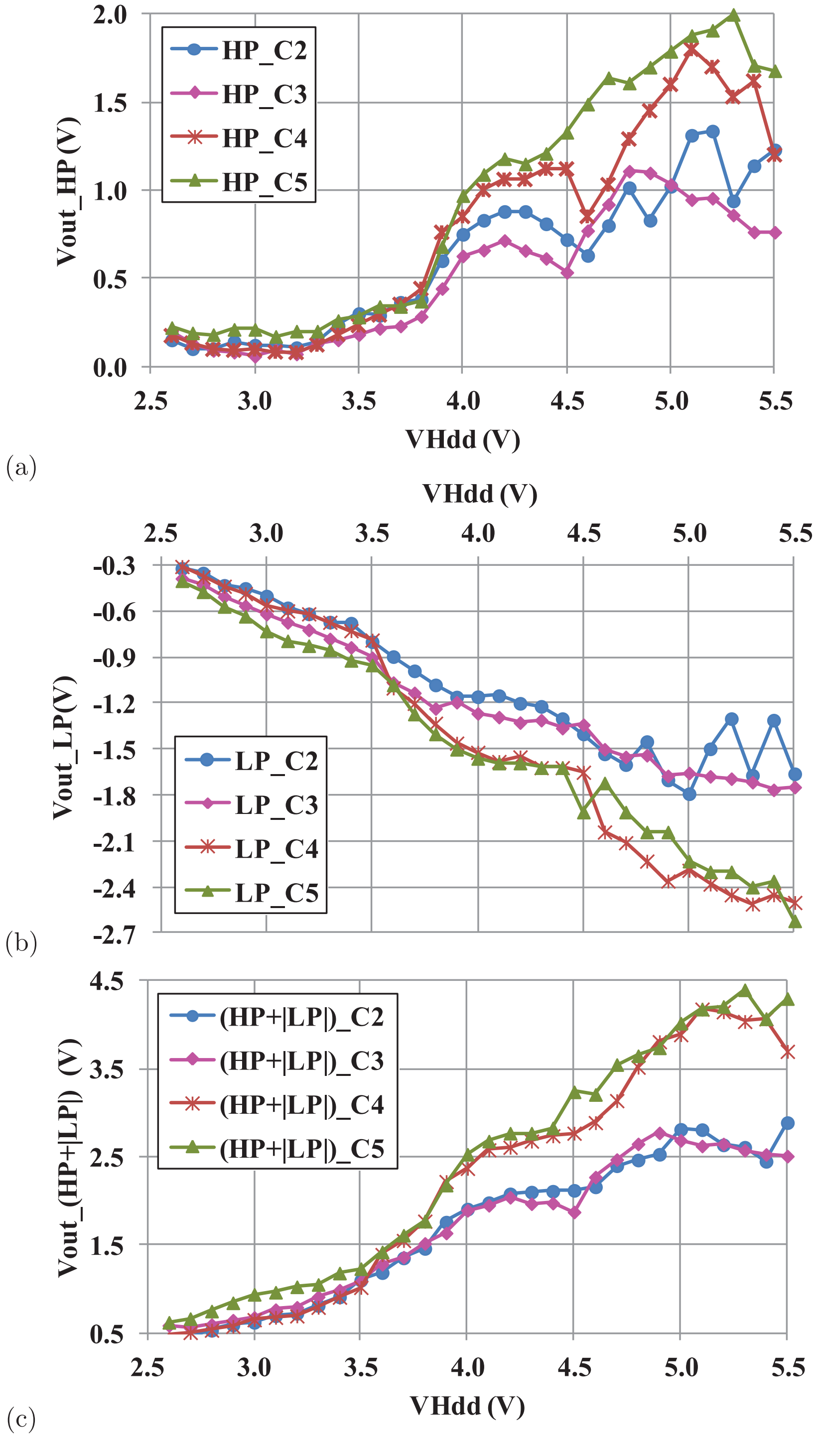


Figure 5.38: The measured (a) high, (b) low and (c) the sum of the high and absolute value of the low overvoltages of the output voltage vs. *VHdd*

As can be seen, these overvoltages (HP) heighten by increasing *VHdd* to 5.5 V, especially HP_C5, which reaches up to 2.0 V and has higher overvoltages than those of the other chips.

The same problem occurs for negative peaks of the output voltages, which are defined here as low peaks (*Vout_LP*) and termed as *LP_C2*, *LP_C3*, *LP_C4* and *LP_C5* for the chips *C2*, *C3*, *C4* and *C5* respectively. Their absolute values increase from ca. 0.4 V to about 1.8 V for the chips *C2* and *C3* and to about 2.6 V for *C4* and *C5*, as shown in Figure 5.38b.

The sums of *Vout_HP* and the absolute value of *Vout_LP* for all four chips are plotted in Figure 5.38c. The output overvoltages of chips *C4* and *C5*, which rise from 0.5 V up to 4.2 V and 4.4 V, respectively, are significantly higher than those of *C2* and *C3* with maximums of 2.8 V.

At a supply voltage of 5.5 V, the positive (HP) and negative (LP) overvoltages of the output waveforms of two different chips *C6* and *C5*, mounted respectively on **PCB 2** and **PCB 3**, have been measured whilst increasing the frequency from 1 kHz to 2 MHz. The measurement results presented in Figure 5.39 are nearly constant, which indicates that the parasitic effects are frequency-independent for frequencies between 1 kHz and 2 MHz.

In the next section, the parasitic effects causing overvoltages on the output voltage will be discussed and investigated due to the theory and the circuit simulation.

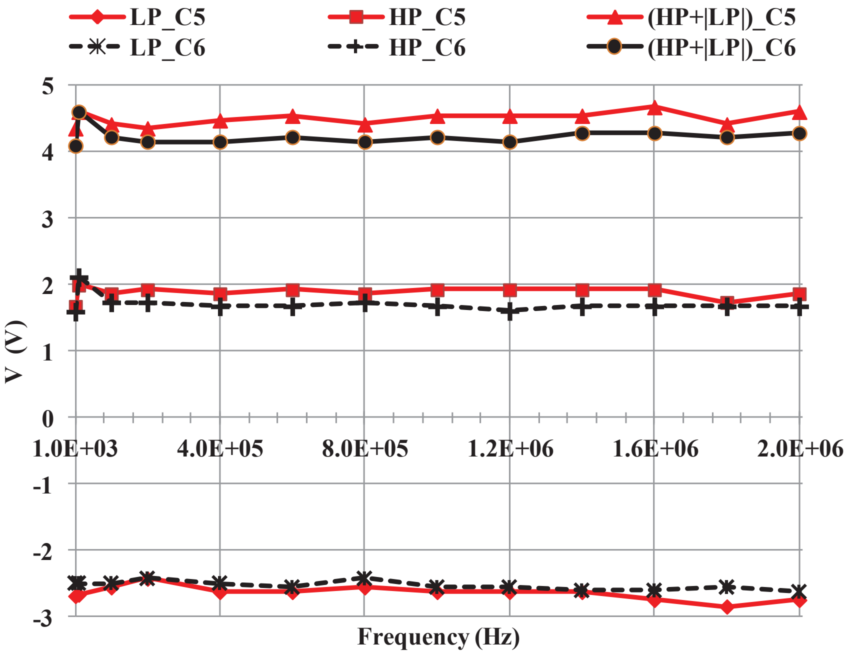


Figure 5.39: The measured high-, low-peaks of the output voltages of chips *C5* and *C6* and the sum of the absolute values of both peaks vs. the frequency

5.2.7.7 Chip-in-Package: Parasitic Effects

The bond wires, lead frames of the IC packages, interconnecting wires on the chips and also conductors used for transmission lines on the PCBs have capacitive, resistive and inductive parasitic effects, when electrons flow through them. These impact negatively on the circuit performance, such as occurrence of the output peaks. The parasitic effects of bond wires and the lead frame of a IC package are discussed here in detail. Figure 5.40 shows the equivalent circuit of a wire.

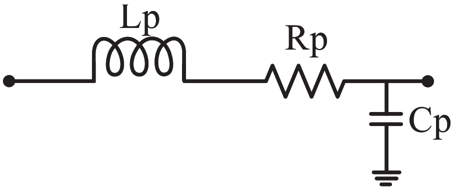


Figure 5.40: The equivalent circuit of a wire

A) Resistive effects

The type **CQFP 64**, **C**eramic **Q**uad **F**lat **P**ackage with **64** pins, is used for packaging the designed IC chip in this work. The material of the lead frame is *Alloy–42*, which is defined for a binary nickel-iron alloy containing 42% nickel and has an electrical resistivity of 70× 10^{-8} Ω×m [18].

At low frequencies, it is reasonable to take DC losses into account. Whereas at high frequencies, skin effects should be considered because the alternating electric current (AC) crowding is mainly toward the surface of the conductor at the so-called “skin”. This impacts frequency-dependent on the resistance and the inductance of the conductor [19].

The bond wires of the IC packages manufactured in this work are gold and have a diameter (D_b) of 25 μm and a length (l_b) of 2 mm. The DC resistor R_b of a bond wire is calculated as 90 mΩ using the Pouillet’s law:

$$R_b = \rho_b \frac{l_b}{A_b} , \tag{5.6}$$

where ρ_b expresses the electrical resistivity (2.214×10^{-8} Ω×m for gold) and A_b is the cross-sectional area ($\pi \times r_b{}^2$) of a bond wire.

At high frequencies, the current is restricted to a layer at the conductor’s surface with a thickness of so-called skin depth (δ) and is defined approximately as [19–20]:

$$\delta \approx \sqrt{\frac{2\rho}{\omega\mu}} = \sqrt{\frac{\rho}{\pi f \mu}} \quad [\mathrm{m}] \tag{5.7}$$

The skin depth (δ) for a gold conductor is plotted versus frequency in Figure 5.41. At a frequency of 36 MHz, the thickness δ with 12.48 μm falls below the radius of the cross section (r_b) of the bond wire used in this work, which is 12.5 μm. As a consequence, the current flowing through the bond wire is confined in the skin depth caused by skin effect, whereby with increasing frequencies to 2 GHz, the skin depth reduces by up to 1.67 μm.

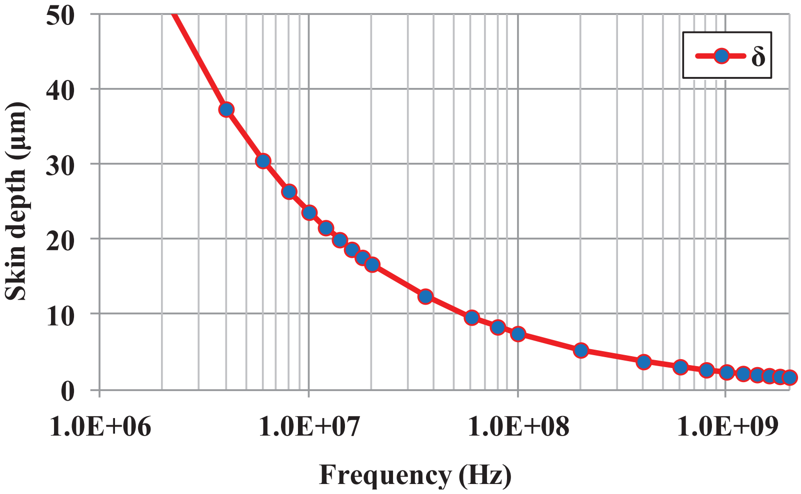


Figure 5.41: The skin depth characteristic of a bond wire used in the package CQFP64 of this work vs. frequency

The AC resistance of the wire, $R_b(\delta)$, caused by the skin effect approaches the following equation using Pouillet's law:

$$R_b(\delta) \approx \rho_b \frac{l_b}{A_{SE}} = \rho_b \frac{l_b}{\pi(r_b^2 - (r_b - \delta)^2)} \tag{5.8}$$

where A_{SE} is the cross-sectional area of the skin layer.

As shown in Figure 5.42, the DC and AC resistances of a bond wire are plotted for frequencies up to 2 GHz. The wire has a skin effect for higher frequencies over 36 MHz. With increasing frequencies from 36 MH to 2 GHz, the AC resistance ($R_b\delta$) raises from 90 mΩ to 361 mΩ.

To simplify the calculation the parasitic parameters, the skin effect is neglected in this work. However, the bond wires have the DC resistance of 90 mΩ. Additional to the bond wires, the lead frame of the package must also be considered for occurring the parasitic effects. A finger of the lead frame used in the package **CQFP64** has a length of approx. 9.0 mm and a cross-section area of 0.0525 mm^2, which is obtained from its thickness of 0.15 mm and width of 0.35 mm. Due to the skin effect, the estimated effective resistance ($R_{f\_Alloy42}(\delta)/l$) of the lead finger raises from from 120 mΩ to ca. 695 mΩ when increasing the frequency from 31 MHz to 2 GHz (Figure 5.43).

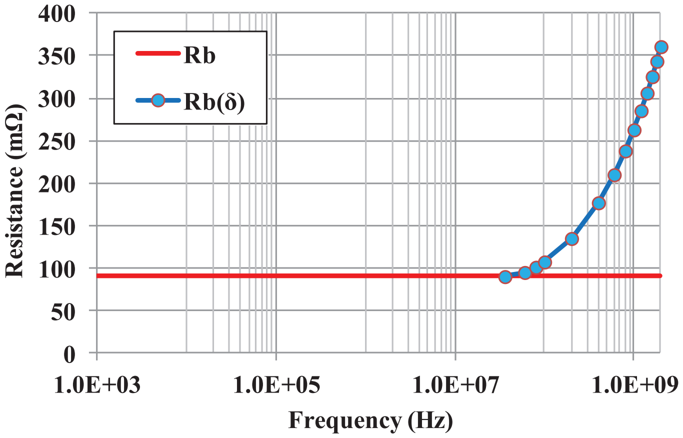


Figure 5.42: The DC and AC resistance-characteristics of a bond wire used in the package CQFP64 of this work vs. frequency

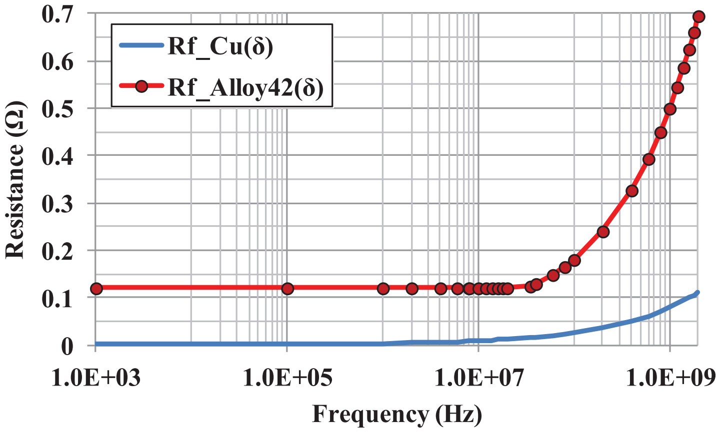


Figure 5.43: The DC and AC resistance-characteristics of a frame finger used in the package CQFP64 of this work vs. frequency in comparison with the material copper

Figure 5.43 compares the resistance characteristics $R_{f\_Alloy42}(\delta)$ and $R_{f\_Cu}(\delta)$ of lead fingers made from two different materials: *Alloy-42* used for manufacturing the lead frames in this work and copper (*Cu*), which is significantly more conductive because *Cu* has a lower electrical resistivity of 1.72×10^{-8} Ω×m than *Alloy-42* (70×10^{-8} Ω×m). Since the parasitic elements are considered in this work without the skin effect, each lead finger has only a DC resistance of 120 mΩ.

B) Inductive effects

In addition to the described resistive effect, the wires also have an inductive impact in view of the internal (L_{int}) and external (L_{ext}) inductances of a wire. The total inductance is defined as:

$$L_{tot} = L_{ext} + L_{int} \tag{5.9}$$

In comparison to the external inductance, the internal inductance is substantially smaller and therefore, it is often neglected. It is frequency-dependent and at higher frequencies, it decreases because of the skin effect. The internal inductance can be calculated as [24–26]:

$$L_{int} = \begin{cases} \frac{R_{dc}}{2\pi f_{(2\delta=t)}} & \text{for } \delta \geq \text{t} \\ \\ \frac{R(\delta)}{2\pi f} & \text{for } 2\delta < \text{t} \end{cases} \tag{5.10}$$

For the range of low frequencies, the DC resistance and the frequency, at which the skin effect occurs, should be used for calculation of the internal inductance. The estimated external inductance of a single (L_{b_ext}) and double bond wires (L_{2b_ext}) and also of a lead finger (L_f) can be calculated as expressed in the following Equations (5.11) and (5.12) using approximate analytical formulae from [20–24]:

$$L_{b\_ext} \approx \frac{\mu_0 l_b}{2\pi}\left[ln(\frac{2l_b}{r_b}) - 0.75\right] \tag{5.11}$$

$$L_{2b\_ext} = L_{b1} + L_{b2} - 2 \times M_{1,2}\ , \tag{5.12}$$

where μ_0 is the permeability of free space and $M_{1,2}$ the mutual inductance of the two conductors:

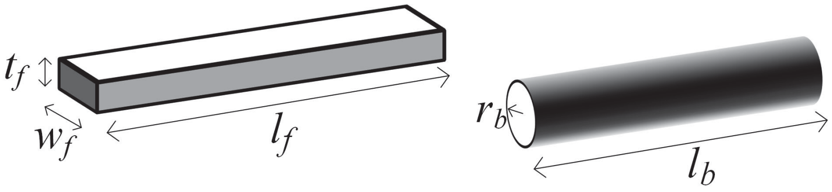
$$M_{1,2} \approx \frac{\mu_0 l_b}{2\pi}\left[ln(\frac{2l_b}{d_b}) - 1 + \frac{d_b}{l_b}\right] \tag{5.13}$$

For a single and double bond wires with a length (l_b) of 2 mm, radius (r_b) of 12.5 μm and a pitch (d_b) of ca. 76 μm, these equations yield the inductances L_{b_ext} of 2.01 nH and L_{2b_ext} of 1.61 nH. For simplification purposes, the calculation of bond wire inductance assumes that the wires are straight lines (Figure 5.44b). However, for a more precise calculation of their self- and mutual-inductances, their actual model should be split into several smaller lines, e.g. where a kink is present, and their coordination should be taken into account [22][26]. The estimated external inductance (L_{f_ext}) of a lead finger with a rectangular cross-section, as shown in Figure 5.44a, can be calculated using the self-inductance formulae from [22] and [27]:

$$L_{fext} = \frac{\mu_0 l_f}{2\pi}\left[ln(\frac{2l_f}{w_f + t_f}) + 0.5 + 0.2235 \times \frac{w_f + t_f}{l_f}\right]\ , \tag{5.14}$$

where w_f, t_f and l_f are the width, thickness and length of a lead finger respectively.

Regarding the mutual inductance in Equation (5.13), the estimated inductance of a lead finger is calculated as 2.93 nH based on the following finger dimensions: length (l_f) of approx. 9 mm, width (w_f) of 0.35 mm, depth (t_f) of 0.15 mm and pitch (d_b) of about 0.6 mm (0.4 mm–0.8 mm).



(a) (b)

Figure 5.44: The simplified structures of (a) a lead finger and (b) a bond wire

The estimated total and external inductances of bond wires (single and double) and a lead finger are illustrated in Figures 5.45 and 5.46. As can be seen, at high frequencies, each total inductance will decrease and approach the relative external inductance, because the internal inductance reduces with increasing high frequencies due to the skin effect. In the schematic of the designed chip of the HV-driver *3HVDv1*, the bond wires and the lead fingers are modeled with their equivalent circuits containing parasitic resistors, R_f and R_b, inductors L_f, L_{2b} and L_b, and capacitors of 50 fF.

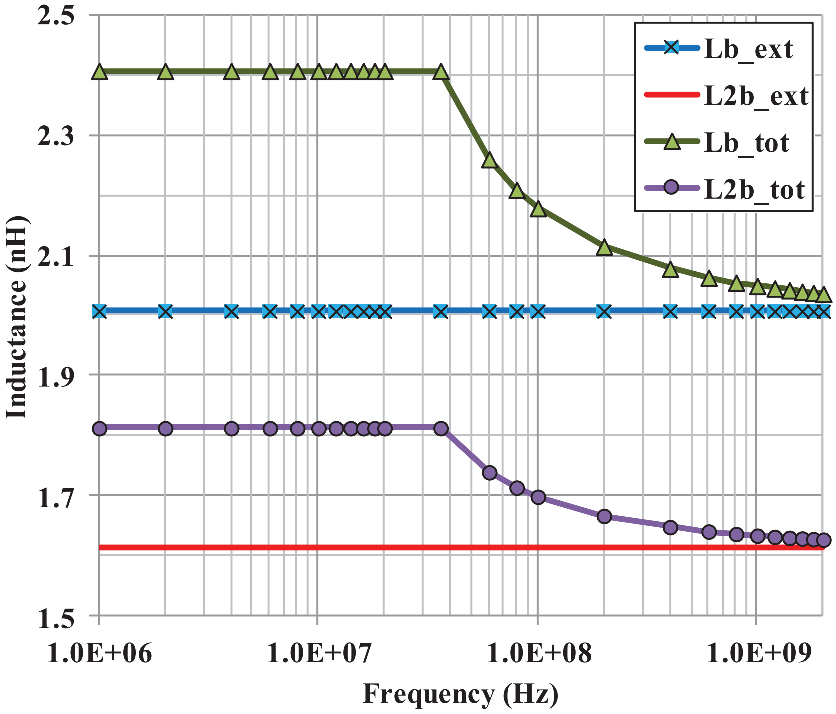


Figure 5.45: The estimated external and total inductances of a single and double bond wires of CQFP64

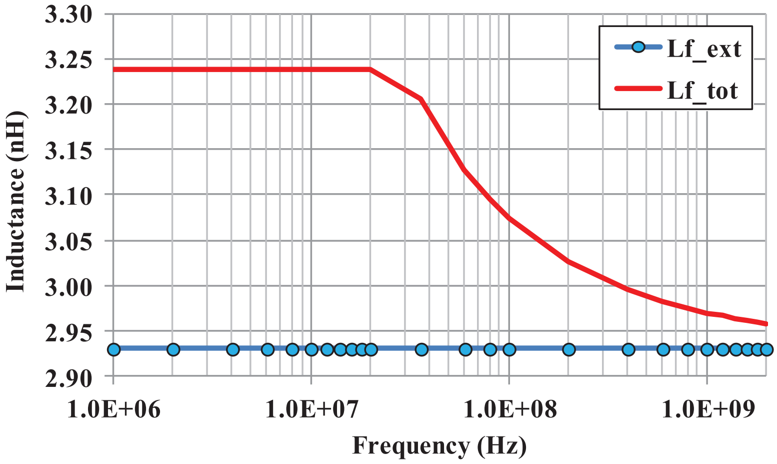


Figure 5.46: The estimated external and total inductances of a lead finger of the package CQFP64

The parameters are set with the estimated calculated parasitic values without skin effect: L_f=3.24 nH, L_{2b}=1.8 nH, L_b=2.4 nH, R_f= 90 mΩ and R_b= 120 mΩ where the suffix "*f*" express parameters of the lead fingers and "*b*" is for those of the bond wires.

Figure 5.47 shows the equivalent circuit of a bond wire and a lead finger. The schematic of the chip included the equivalent circuits of the bond wires and lead fingers is transient simulated with a supply voltage of 5.5 V. In this simulation, the parasitic effects of interconnected wires on the chip and also on the circuit board are not included since this would lead to intricate and lengthy computation for simulation of the chip.

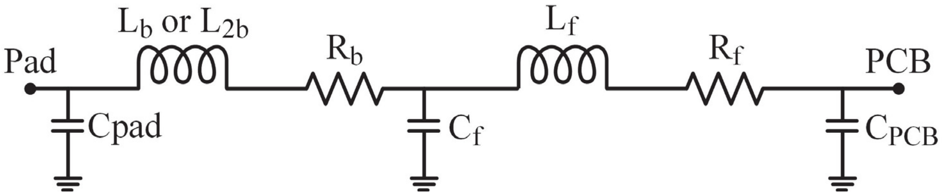


Figure 5.47: The equivalent circuit of a bond wire and a lead finger

From the simulation result, the transient output voltage characteristic *Vout*, the voltage at the pin connector of the package to the PCB, is displayed in Figure 5.48. As can be seen, the output voltage has a negative peak (LP) of –1.97 V and a positive (HP) overvoltage of 0.88 V (=6.38 V–5.5 V). These values are in the range of measured high (HP) and low (LP) peaks of *Vout* as shown previously in Figures 5.38a and 5.38b for a supply voltage of 5.5 V.

The impact of the wire bond and lead finger inductances on the peaks of the out-

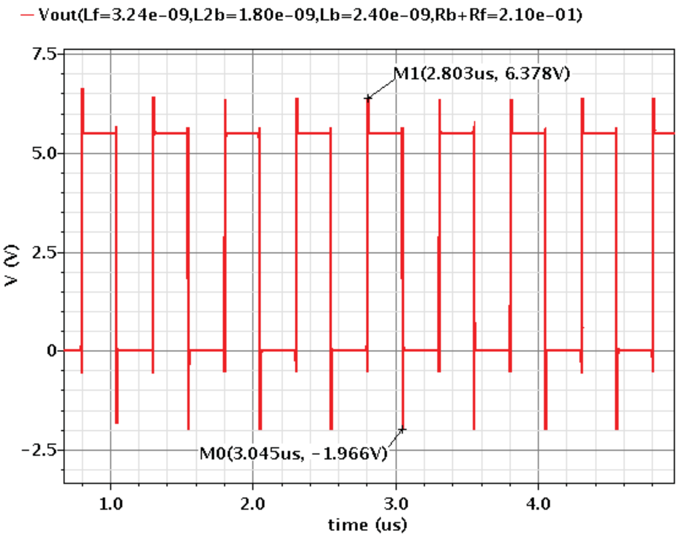


Figure 5.48: The simulated characteristic of *Vout*, the voltage at the pin connector of the package to the PCB, with considering parasitic effects

put characteristic are analysed due to the transient simulation by varying the relevant parameters for the following two steps. In both cases, the circuit is supplied with 5.5 V.

Firstly, the inductance of each lead finger (L_f) is set to zero. With varying the inductance ($L_{2b}/2$) of each double wire from 0.4 nH to 1.0 nH, the high peak (M6, M7, M5 and M0 shown in Figure 5.49) of the output characteristics increases from 5.66 V to 5.96 V and the low peaks (M4, M3, M2 and M1 depicted in Figure 5.49) fall deeper from –218 mV to –834 mV. As a result, the positive and negative overvoltages rise by increasing the inductance of each double wire.

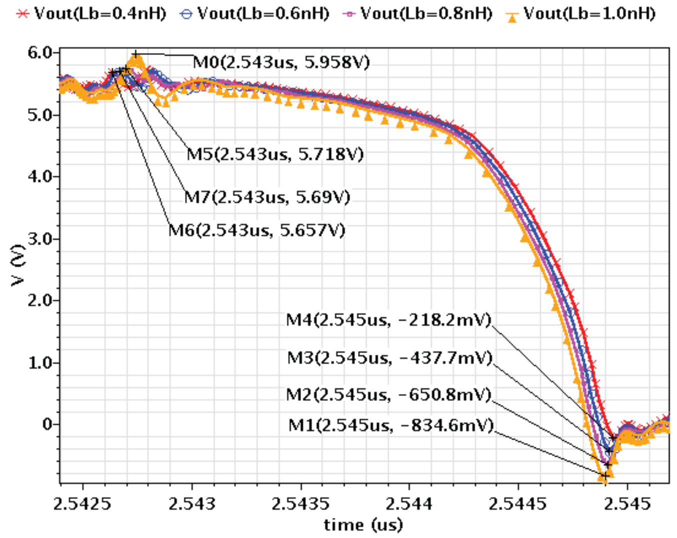


Figure 5.49: The simulated output voltage characteristics of the designed chip for different inductors of each double bond wire

Next, all parasitic parameters are set as calculated. By varying the inductance of each lead finger from 2.0 nH to 5.0 nH, the maximum value of the output voltage ($Vout_{max}$) rises from 6.3 V to 7.9 V, which are significantly higher than the amplitude of 5.5 V. Table 5.9 gives the details of the positive (HP) and negative (LP) overvoltages of the output signal for different inductors of each lead finger. The absolute value of the negative overvoltage (LP) increases also from 1.2 V to 2.3 V.

Table 5.9: The maximum ($Vout_{max}$), positive (HP) and negative (LP) overvoltages [V] of the output voltage for different L_{f_ext} *[nH]*

$\mathbf{L_{f\_ext}}$	**2.0**	**3.0**	**4.0**	**5.0**
$\mathbf{Vout_{max}}$	6.30	6.48	6.9	7.91
HP	0.9	1.0	1.4	2.4
LP	–1.2	–2.0	–2.2	–2.3

5.2.7.8 Driver 3HVDv1 Switching Buck Converter

As shown by using equivalent circuits consisting of parasitic resistors, inductors and capacitors with estimated values obtained from the calculations, it has been evidenced that packaging and also conductors on the chip and on the printed circuit board negatively impact on the circuit performance such as occurrence of peaks on the output voltage. Furthermore, these peaks increase with connection to the inductor of the proposed buck converter used in this work; therefore, the circuit on the chip can be broken down.

For reducing the output spikes (overvoltages), the following three methods have been used, while the respective chip switches the proposed buck converter.

1. Connecting a capacitor across the chip output node and ground
2. Adding a resistor connected in parallel to a Schottky diode on the PCB between the chip output node and ground
3. Using the technology Chip-On-Board (COB) with and without adding the parallel-connected resistor and Schottky diode

5.2.7.9 Chip-in-Package: Using Capacitor

From the simulation analysis, a capacitor (C_x) with a value of between 1 nF and 2.5 nF has been determined for reducing peaks during switching the buck converter, when it is connected across the chip output node and ground. This approach resembles the method using a Snubber capacitor [67]–[69].

In practice, the circuit is firstly supplied with 3.6 V and after that connected to the proposed buck converter. Subsequently, the supply voltage is raised to 5.5 V. The peaks of the chip output voltage have been observed with and without a capacitor of 1 nF, 1.5 nF and 2.5 nF. For supply voltages higher than 4.5 V, the output overvoltages are so high that switching the buck converter with a capacitor lower than 2.5 nF is incredible.

The impact of the capacitor (C_x) on high and low peaks (HP and LP) of the output voltage for different supply voltages from 3.6 V to 5.5 V is given in Table 5.10 for the chip *C3*. The duty cycle (D) of the input signal is determined for generating a voltage of 1.2 V (V_{bc}) at the buck converter's output. The term **P:P** (peak-to-peak) represents the difference between the maximum and minimum measured values of *Vout*.

For supply voltages of up to 4.0 V, switching the buck converter with and without capacitor C_x has been accomplished. When using a capacitor of 2.5 nF, the overvoltages LP and HP for the supply voltage of 4.0 V improved respectively from –2.73 V and 0.9 V to –1.37 V and 0.33 V. For higher supply voltages, switching the buck converter without the capacitor C_x is a hazard that could break down the circuit on the chip. For example, for *VHdd* of 5.0 V and 5.5 V, only the capacitor of 2.5 nF is employed. The low and high peaks of |–1.5 V| and 0.4 V for a supply voltage of 5.5 V can be imagined to be significantly lower than without using the capacitor.

Table 5.10: The measured output over voltages and the relative duty-cycle providing V_{bc} of 1.2 V for different capacitors and supply voltages for the chip *C3*

VHdd [V]	C_x [nF]	P:P [V]	LP [V]	HP [V]	D [%]	T [°C]
3.6	–	7.10	–2.67	0.83	47.8	29.5
	1.0	5.80	–1.67	0.53	47.1	
	1.5	5.40	–1.42	0.38	46.8	
	2.5	4.90	–1.26	0.05	45.5	
4.0	–	7.63	–2.73	0.90	55.6	29.5
	1.0	6.67	–1.80	0.87	55.0	
	1.5	6.19	–1.60	0.59	54.3	
	2.5	5.68	–1.37	0.33	54.1	
4.5	**1.0**	7.63	–2.08	1.05	59.0	30
	1.5	7.00	–1.67	0.83	58.0	
	2.5	6.40	–1.44	0.55	57.4	
5.0	**2.5**	7.50	–1.52	0.22	63.9	30.5
5.5	**2.5**	7.88	–1.54	0.42	66.5	31.5

Figure 5.50 shows a comparison between the output voltage low- (LP) and high-peaks (HP) of the chip *C4* with and without using the capacitor C_x of 2.5 nF versus the duty-cycle of *Vin* in the range from 40% to 80%. The low- (LP) and high-peaks (HP) respectively indicate the negative and positive output overvoltages. The circuit is supplied

with 4.0 V and switches the proposed buck converter. The peaks are termed as $Vout_{LP\_C4x}$ and $Vout_{HP\_C4x}$ for using C_x and as $Vout_{LP\_C4}$ and $Vout_{HP\_C4}$ for without C_x.

As can be seen, the absolute values of the output low peaks ($Vout_{LP\_C4}$) without using the capacitor C_x vary between 2.1 V and 3.5 V, which are too high and would damage the chip. With connecting the chip output to the capacitor C_x of 2.5 nF, these values reduce in the range between 0.9 V and 1.5 V. However, the high-peaks ($Vout_{HP\_C4}$), which are in the range from 0 V to 0.7 V without C_x, are not as improved as the low-peaks. With using the proposed capacitor, the peaks $Vout_{HP\_C4x}$ vary from 0.3 V to 0.5 V.

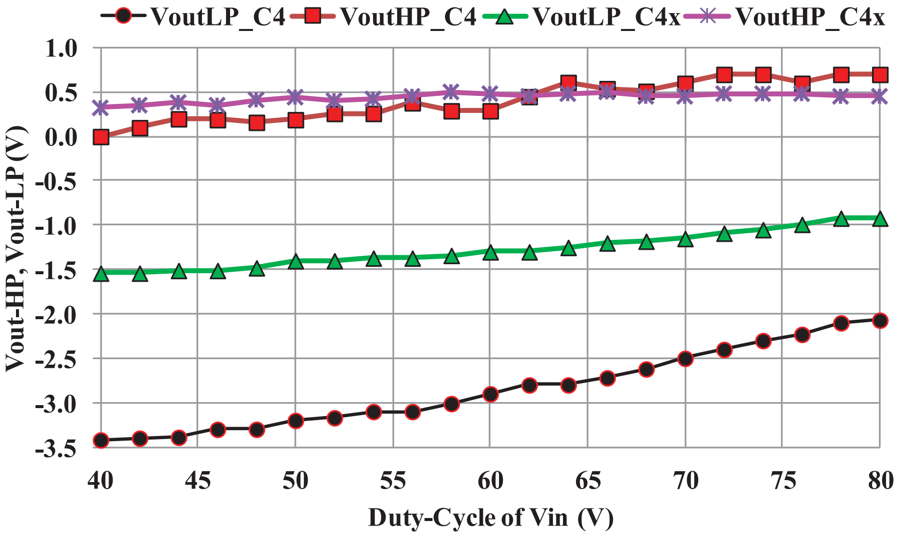


Figure 5.50: The measured output over voltages of the chip *C4* with and without using the capacitor of 2.5 nF with respect to duty-cycle of the input signal *Vin* (*VHdd*=4.0 V, V_{bc}=1.2 V)

One major problem of this method for reducing the output overvoltages is that the rise- and fall times of the output voltage increase to about 30 ns–40 ns, which indicates slower switching of the buck converter when compared against the circuit without using the capacitor. The other drawback is that when increasing the value of the capacitor, for achieving the same voltage (V_{bc}) at the output of the buck converter, the duty-cycle of the input signal decreases, which means the time off-state increases. Subsequently more current drives from supply into the output load; therefore, the power consumption increases.

Table 5.11 provides details about duty-cycle (D) of the input signal *Vin* and the current consumption (I_g) of the whole system (PCB included the chip *C4*) for different capacitors (C_x) and output voltages (V_{bc}) of the buck converter. The circuit is supplied with 4.0 V. As can be seen, in terms of increasing the value of the capacitor C_x, the duty-cycle reduces, whereas the current consumption rises.

Table 5.11: The measured duty-cycle of *Vin* to obtain different output voltages V_{bc} for various capacitors (C_x) and the respective current consumption

$\mathbf{V_{bc}}$	**1.1 V**		**1.2 V**		**1.3 V**		**1.4 V**	
C_x [nF]	D [%]	I_g [mA]	D [%]	I_g [mA]	D [%]	I_g [mA]	D [%]	I_g [mA]
–	58.0	69	54.4	76	50.8	84	47.5	92
1	57.2	75	53.9	82	50.3	90	46.9	98
1.5	57.0	77	53.8	84	49.2	93	46.8	101
2.5	56.6	83	53.5	91	49.9	98	46.5	106

Figure 5.51 shows the respective current consumptions I_{VHdd_C4} and I_{VHdd_C4x} from the supply versus the duty-cycle of *Vin*. Both current characteristics respectively decrease from 94 mA and 104 mA to 17 mA and 32 mA when raising the duty-cycle from 40% to 80%, because the time that the driver pull-up path is active reduces. However, the result shows that with using the capacitor C_x, the consumption current I_{VHdd_C4x} is higher than without C_x. The difference characteristic between both currents ΔI_{VHdd} is also plotted in Figure 5.51, which varies between 10 mA and 15 mA.

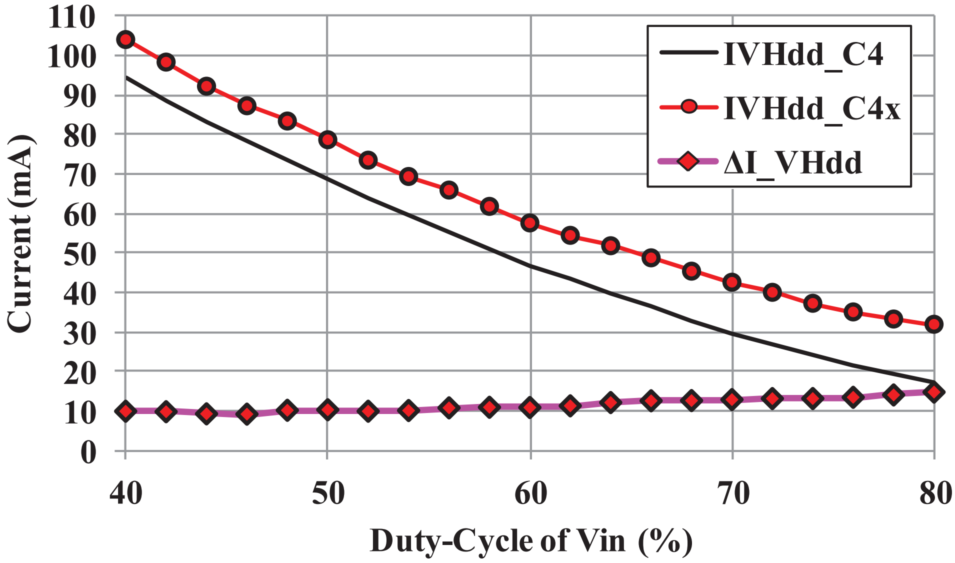


Figure 5.51: The measured current consumption characteristics, while the circuit switches the buck converter with and without C_x and their difference (*VHdd*=4.0 V)

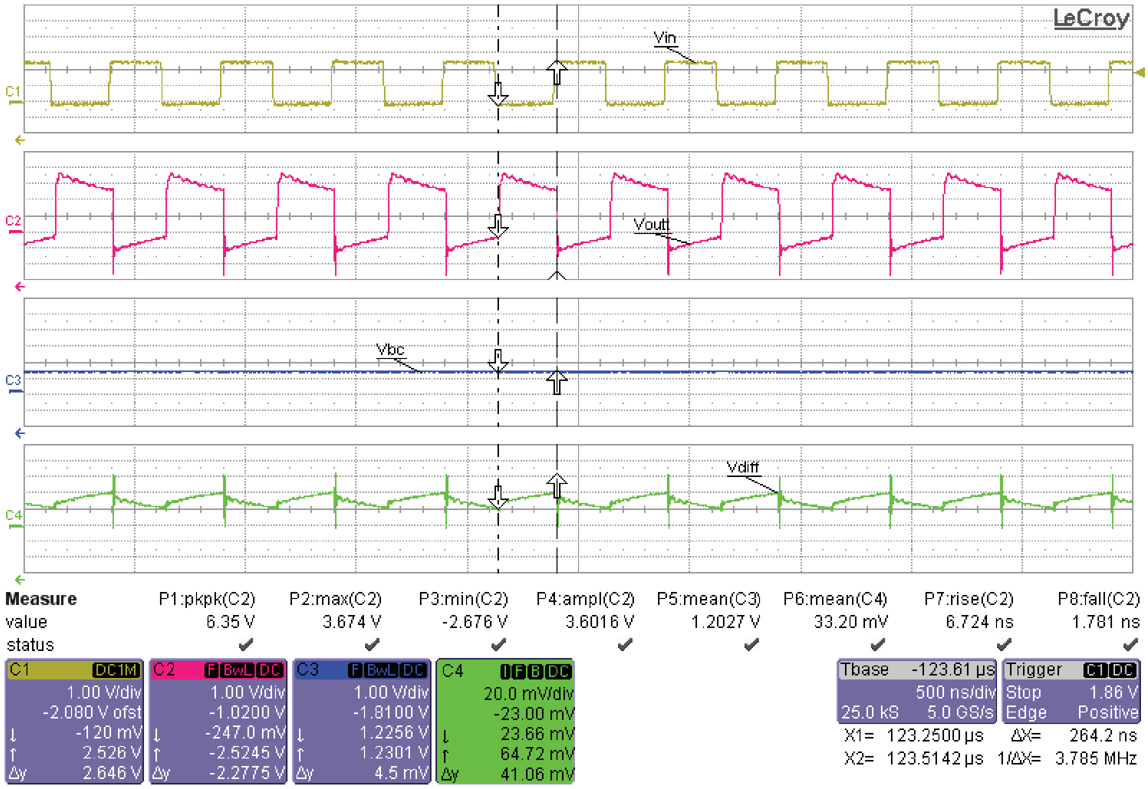
For supply voltage of 4.0 V, to achieve the initial voltage V_{bc}, the duty-cycle of *Vin* must be reduced by about 1%–2%, when the capacitor C_x is employed for reducing spikes on the output waveform. However, this increases the current consumption. It can be assumed that for higher supply voltages, the current consumption increases significantly more than for the initial condition (without connecting the chip output to C_x), but this comparison has not been performed to prevent any damaging impact on the chip.

The waveform characteristics of the buck converter, which is switched by the chip *C4*, are shown in Figures 5.52a and 5.52b for the supply voltage of 3.6 V and in Figures 5.53a and 5.53b for 5.5 V. The waveforms comprise the input signal *Vin*, the output voltage of the chip *Vout* and of the buck converter V_{bc} and the differential voltage V_{diff} across the resistor R_m, which are respectively connected to the oscilloscope channels C1, C2, C3 and C4.

With a duty-cycle of 47.7%, a buck converter output voltage (V_{bc}) of 1.2 V has been achieved for a supply voltage of 3.6 V without using the capacitor C_x. The differential voltage V_{diff} of 33.2 mV across R_m, indicates an extra resistive parasitic effect of at least 232 mΩ due to the differential probe used to measure the voltage drop across R_m. However, the waveform shows that V_{diff}, which is proportional to the current flowing through the inductor (L) and the resistor R_m of the buck converter, rises and decreases linearly according to the off- and on-states. With inserting the capacitor of 2.5 nF, the rise- and fall times increase as well (Figure 5.52b); therefore, as expected, the duty-cycle of *Vin* decreases to 45.7%. Due to the capacitor C_x, the absolute values of the low peaks, indicated as *min(C2)* in the figure, reduces from 2.68 V to 1.30 V. The maximum output voltage termed as *max(C2)* of this chip *C4* increases slightly from 3.67 V to 3.82 V, whereas that of the chip *C3* decreases as given HP in Table 5.10 for supply voltage 3.6 V. As previously mentioned, the high peaks HP is the difference between the maximum and the desired high level of the output voltage.

For supply voltage of 5.5 V, the capacitor C_x of 2.5 nF has to be used to avoid breaking down the circuit on the chip because of high output overvoltages, which increase by connecting to the inductor of the buck converter. As displayed in Figure 5.53a, *Vout* has a high-peak (HP) of 0.36 V and a low-peak (LP) of –1.57 V. The output voltage V_{bc} of 1.2 V has been achieved by setting the duty-cycle of *Vin* at 65.6%. Figure 5.53b shows that a voltage of 0.7 V has been achieved at the output of the buck converter by setting the duty-cycle at 80%. The circuit is supplied by 5.5 V.

The output high- and low peaks (HP and LP) of two chips *C3* and *C4*, which separately switch the proposed buck converter on the **PCB 3** and **PCB 2** respectively, have been measured for various supply voltages from 3.6 V to 5.5 V with connecting the capacitor of 2.5 nF across the chip output node and ground. For every supply voltage, the duty-cycle of the input signal has been adjusted to achieve the voltage V_{bc} of 1.2 V at the converter output. The results are presented in Figures 5.54a and 5.54b. The difference between peaks of both chips are slightly low. The high peaks (HP) reach up to about 0.55 V (Figure 5.54a) and the low peaks (LP) vary from ca. –1.3 V to approximately –1.6 V (Figure 5.54b). The output voltage drop across *VHdd* from 4.5 V to 4.6 V occurs as a result of adjusting reference voltages by increasing the supply voltage.



Measure	P1:pkpk(C2)	P2:max(C2)	P3:min(C2)	P4:ampl(C2)	P5:mean(C3)	P6:mean(C4)	P7:rise(C2)	P8:fall(C2)
value	6.35 V	3.674 V	-2.676 V	3.6016 V	1.2027 V	33.20 mV	6.724 ns	1.781 ns
status	✓	✓	✓	✓	✓	✓	✓	✓

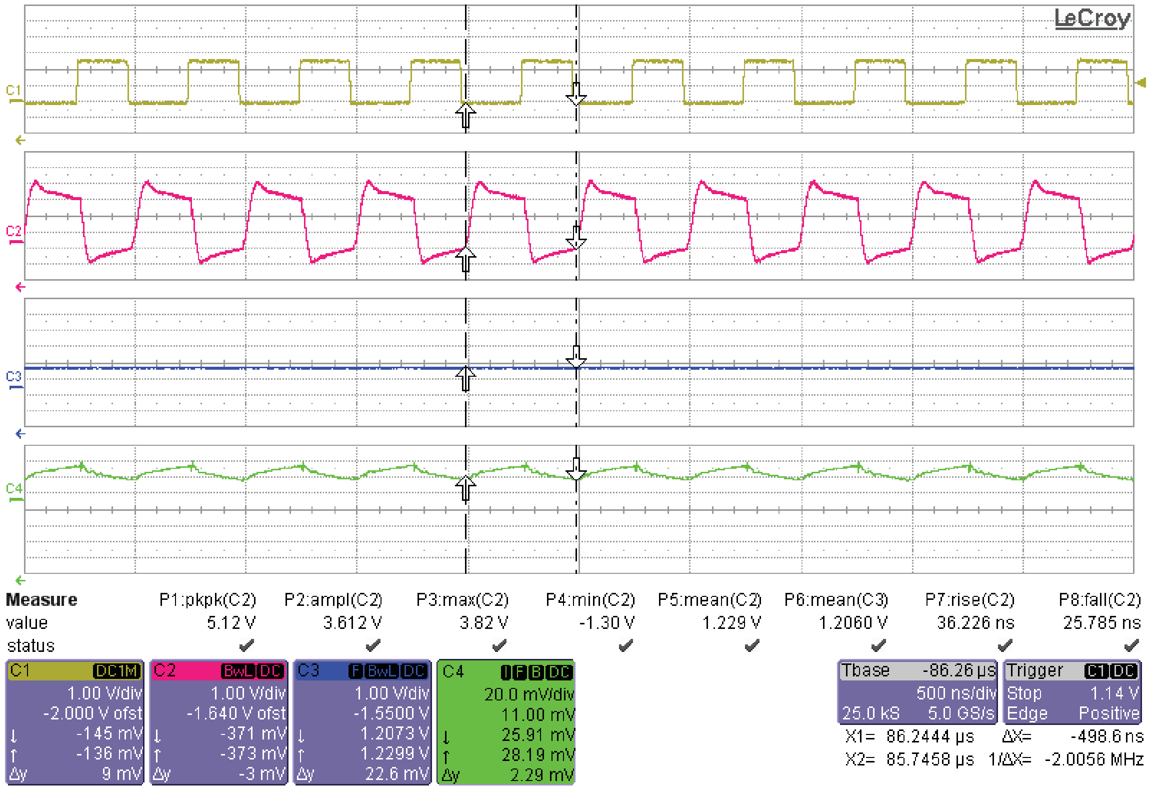
C1 DC1M	C2 F BwL DC	C3 F BwL DC	C4 I F B DC
1.00 V/div	1.00 V/div	1.00 V/div	20.0 mV/div
-2.080 V ofst	-1.0200 V	-1.8100 V	-23.00 mV
↓ -120 mV	↓ -247.0 mV	↓ 1.2256 V	↓ 23.66 mV
↑ 2.526 V	↑ -2.5245 V	↑ 1.2301 V	↑ 64.72 mV
Δy 2.646 V	Δy -2.2775 V	Δy 4.5 mV	Δy 41.06 mV

Tbase -123.61 µs
500 ns/div
25.0 kS 5.0 GS/s

Trigger C1 DC
Stop 1.86 V
Edge Positive

X1= 123.2500 µs ΔX= 264.2 ns
X2= 123.5142 µs 1/ΔX= 3.785 MHz

(a)



Measure	P1:pkpk(C2)	P2:ampl(C2)	P3:max(C2)	P4:min(C2)	P5:mean(C2)	P6:mean(C3)	P7:rise(C2)	P8:fall(C2)
value	5.12 V	3.612 V	3.82 V	-1.30 V	1.229 V	1.2060 V	36.226 ns	25.785 ns
status	✓	✓	✓	✓	✓	✓	✓	✓

C1 DC1M	C2 BwL DC	C3 F BwL DC	C4 I F B DC
1.00 V/div	1.00 V/div	1.00 V/div	20.0 mV/div
-2.000 V ofst	-1.640 V ofst	-1.5500 V	11.00 mV
↓ -145 mV	↓ -371 mV	↓ 1.2073 V	↓ 25.91 mV
↑ -136 mV	↑ -373 mV	↑ 1.2299 V	↑ 28.19 mV
Δy 9 mV	Δy -3 mV	Δy 22.6 mV	Δy 2.29 mV

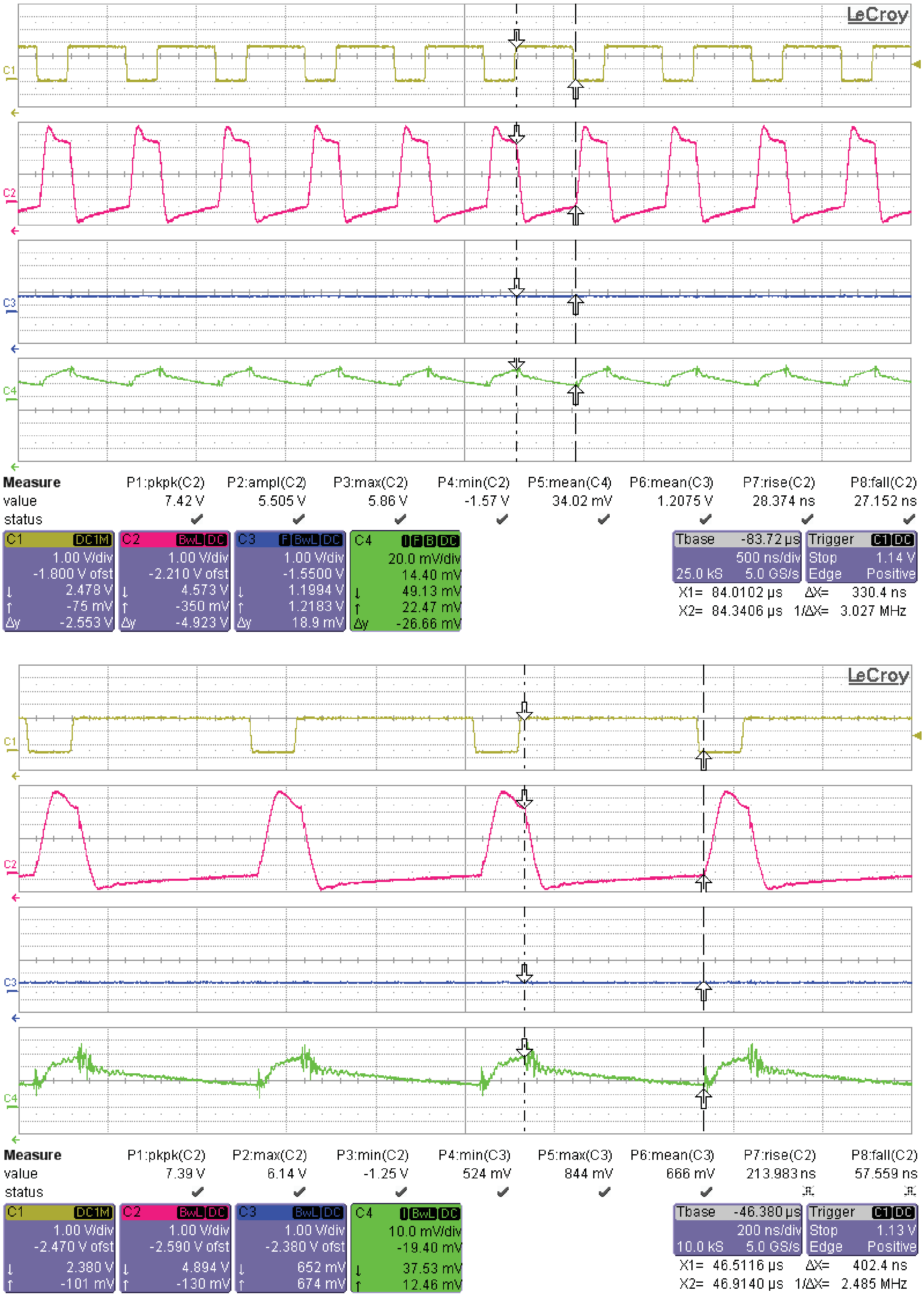
Tbase -86.26 µs
500 ns/div
25.0 kS 5.0 GS/s

Trigger C1 DC
Stop 1.14 V
Edge Positive

X1= 86.2444 µs ΔX= -498.6 ns
X2= 85.7458 µs 1/ΔX= -2.0056 MHz

(b)

Figure 5.52: The measured waveforms of *Vin* (channel C1), *Vout* (C2), V_{bc} (C3) and V_{diff} (C4) of the buck converter switched with the circuit *3HVDv1* on the chip *C4* (a) without and (b) with C_x of 2.5 nF (*VHdd*=3.6 V)



(a)

Measure	P1:pkpk(C2)	P2:ampl(C2)	P3:max(C2)	P4:min(C2)	P5:mean(C4)	P6:mean(C3)	P7:rise(C2)	P8:fall(C2)
value	7.42 V	5.505 V	5.86 V	-1.57 V	34.02 mV	1.2075 V	28.374 ns	27.152 ns
status	✓	✓	✓	✓	✓	✓	✓	✓

C1 DC1M	C2 BwL DC	C3 F BwL DC	C4 I F B DC
1.00 V/div	1.00 V/div	1.00 V/div	20.0 mV/div
-1.800 V ofst	-2.210 V ofst	-1.5500 V	14.40 mV
↓ 2.478 V	↓ 4.573 V	↓ 1.1994 V	↓ 49.13 mV
↑ -75 mV	↑ -350 mV	↑ 1.2183 V	↑ 22.47 mV
Δy -2.553 V	Δy -4.923 V	Δy 18.9 mV	Δy -26.66 mV

Tbase -83.72 µs
500 ns/div
25.0 kS 5.0 GS/s
Trigger C1 DC
Stop 1.14 V
Edge Positive
X1= 84.0102 µs ΔX= 330.4 ns
X2= 84.3406 µs 1/ΔX= 3.027 MHz

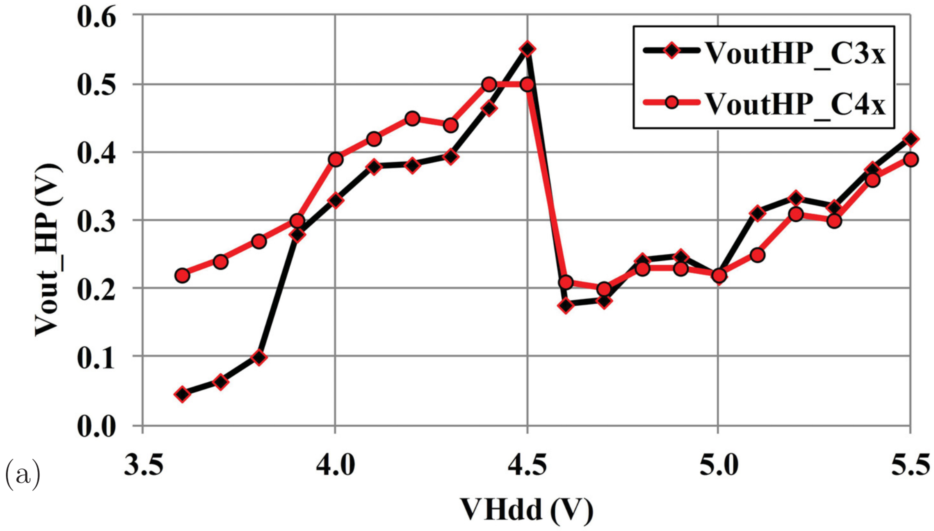
(b)

Measure	P1:pkpk(C2)	P2:max(C2)	P3:min(C2)	P4:min(C3)	P5:max(C3)	P6:mean(C3)	P7:rise(C2)	P8:fall(C2)
value	7.39 V	6.14 V	-1.25 V	524 mV	844 mV	666 mV	213.983 ns	57.559 ns
status	✓	✓	✓	✓	✓	✓	⎍	⎍

C1 DC1M	C2 BwL DC	C3 BwL DC	C4 I BwL DC
1.00 V/div	1.00 V/div	1.00 V/div	10.0 mV/div
-2.470 V ofst	-2.590 V ofst	-2.380 V ofst	-19.40 mV
↓ 2.380 V	↓ 4.894 V	↓ 652 mV	↓ 37.53 mV
↑ -101 mV	↑ -130 mV	↑ 674 mV	↑ 12.46 mV

Tbase -46.380 µs
200 ns/div
10.0 kS 5.0 GS/s
Trigger C1 DC
Stop 1.13 V
Edge Positive
X1= 46.5116 µs ΔX= 402.4 ns
X2= 46.9140 µs 1/ΔX= 2.485 MHz

Figure 5.53: The measured waveforms of *Vin* (C1), *Vout* (C2), V_{bc} (C3) and V_{diff} (C4) of the buck converter with V_{bc} of (a) 1.2 V and (b) 0.7 V (*VHdd*=5.5 V, chip *C4x*)



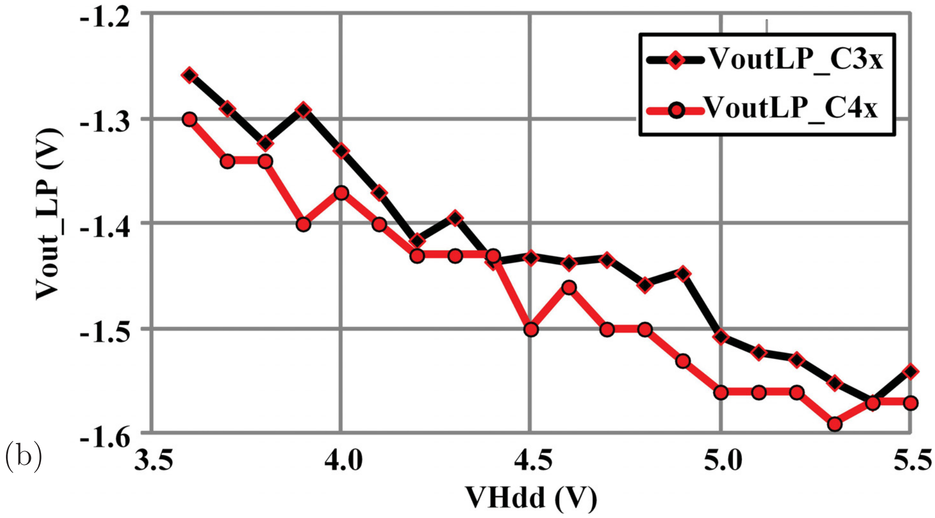


Figure 5.54: The measured (a) high- (HP) and (b) low-peaks (LP) of the output voltage of the chip *C3x* and *C4x* switching the proposed buck-converter using the capacitor of 2.5 nF vs. the supply voltage (V_{bc}=1.2 V)

With increasing the duty-cycle of *Vin* from 40% to 80%, the output voltage V_{bc} of a buck converter switched by the chip *C3* is measured for different supply voltages of 4.0 V, 4.5 V, 5.0 V and 5.5 V. The results are plotted in Figure 5.55. The capacitor of 2.5 nF has been used for reducing the output spikes. The voltage characteristics of V_{bc} are nearly linear and generated due to the buck converter from the supply voltages 4.0 V, 4.5 V, 5.0 V and 5.5 V respectively to 0.5 V, 0.59 V, 0.6 V and 0.7 V for a duty-cycle of 80%. For a duty-cycle of 40%, these *VHdd* (4.0 V, 4.5 V, 5.0 V and 5.5 V) are stepped down respectively to 1.5 V, 1.8 V, 2.0 V and 2.2 V.

It has to be taken into account that by a duty-cycle of 40%, the current consumption of PCB reaches up to 150 mA. To avoid damage to the chips, the measurement has been accomplished for different duty-cycle from 40% upwards.

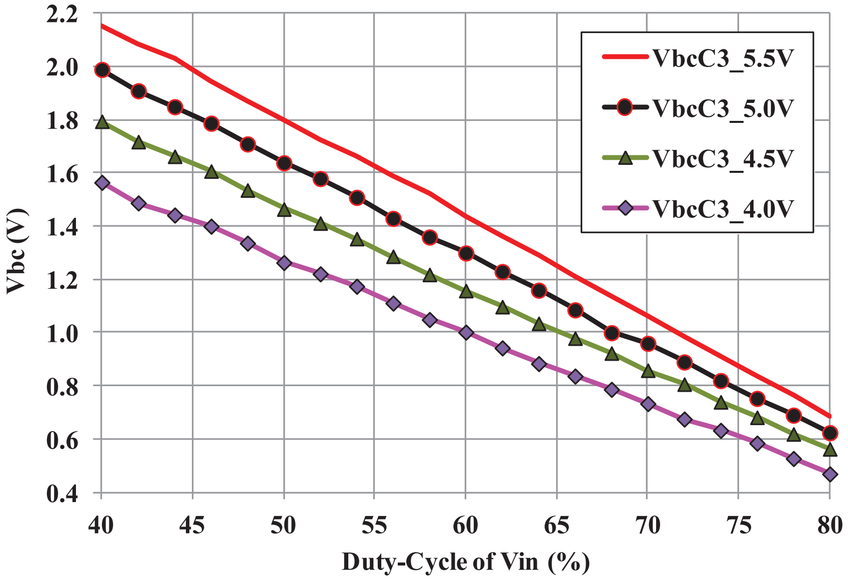


Figure 5.55: The measured output voltage (V_{bc}) of the buck converter switched by the chip *C3x* vs. the duty-cycle of *Vin*

In this section, to reduce output overvoltages and avoid damage to the circuit, a capacitor of 2.5 nF is connected across the chip output and ground. However, the switching time of the buck converter rises more than 10 times and more current is consumed for charging the capacitor. In the next steps, the other methods are presented in order to avoid high overvoltages during switching the proposed buck converter with the designed HV-driver circuit on the chip.

5.2.7.10 Chip-in-Package: Using Schottky Diode (OVP)

In order to protect the output from overvoltage, a parallel-connected resistor of 510 Ω and Schottky diode ([70]–[73]) is inserted across the chip output node and ground (Figure 5.56).

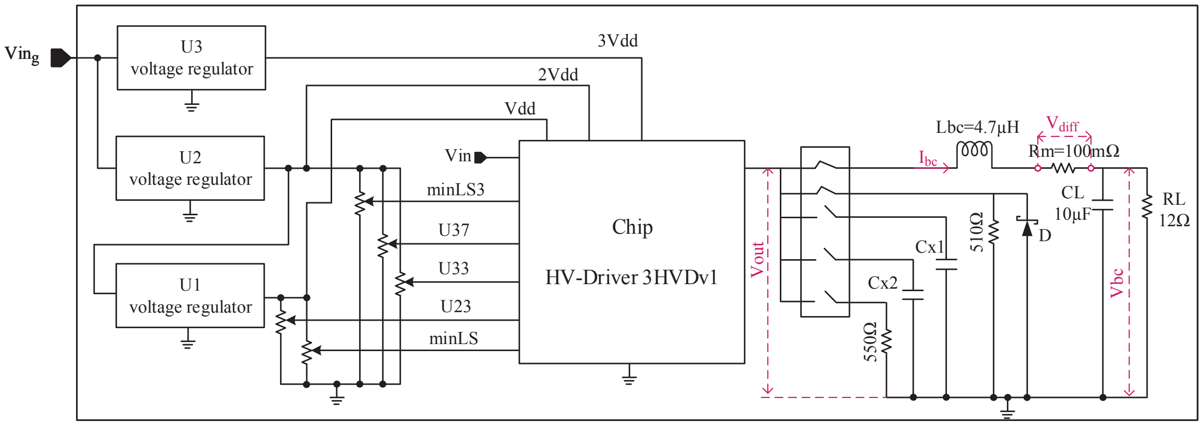


Figure 5.56: The principle of the PCB for switching the buck converter using an OVP (Schottky diode and resistor)

This reduces the absolute value of low peaks. For reducing high peaks, the same combination of these components should be connected between the output node and the supply voltage rail of *VHdd*. Therefore, the driver output voltage (*Vout*) at the output node of chips, can be limited to a maximum of $VHdd+V_F$, and a minimum of $-V_F$, where V_F is defined for the forward voltage of the Schottky diode. However, a place for mounting an OVP across the output node of a chip and the supply voltage rail is not envisaged on the PCB draft, since the appearance of large peaks on the output signal was not expected. The device containing a parallel-connected resistor and Schottky diode is defined in this work as OVP (**O**ver**v**oltage **P**rotection). The electrical characteristics of the used Schottky diode *AVX SD0805S020S1R0* are given in Table 5.12.

Table 5.12: Electrical characteristics of the used Schottky diode *AVX SD0805S020S1R0*

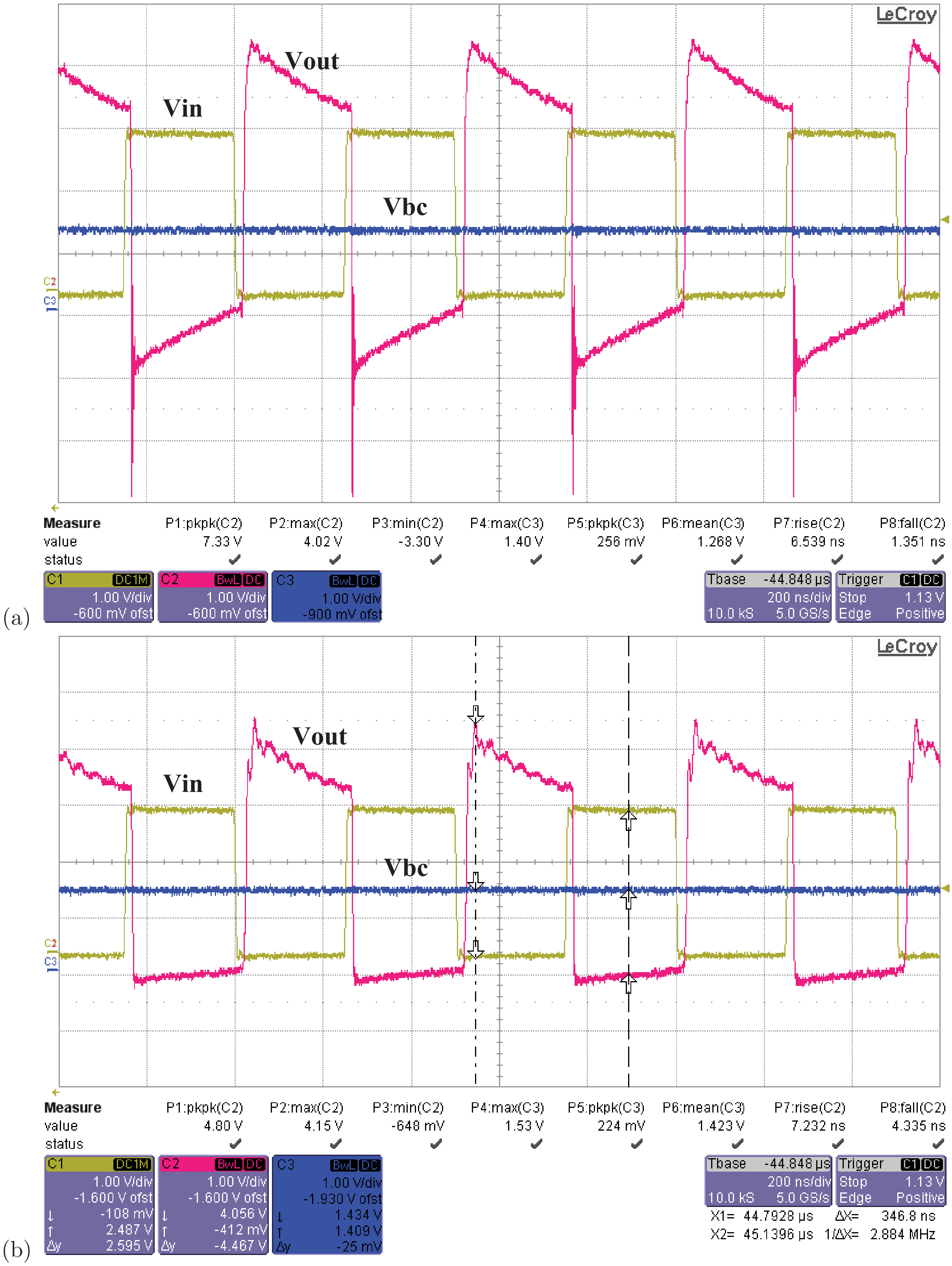
Max. Reverse Voltage	**Max. Forward Current**	**Max. Peak Forward Surge Current**	**Reverse Current**	**Forward Voltage**
20.0 V	1.0 A	10.0	0.028 mA/Max. 0.2 mA	0.42 V/Max. 0.45 V

The measured output voltage waveforms of the chip *C5* and the buck converter with and without OVP are presented in Figures 5.57a and 5.57b, respectively, where the channels C2 and C3 present the output voltage waveforms of the chip (*Vout*) and the buck converter (V_{bc}) and are respectively coloured red and blue. In both conditions, the circuit is supplied with 4.0 V and switches the proposed buck converter (BC) with a duty-cycle of 50%. The comparison between both results indicates that the negative peaks on the driver output voltage (*Vout*) is improved significantly when the proposed OVP is connected across the chip output and ground.

Without OVP, the chip output voltage has a high-peak (HP) of 0.02 V and a low-peak (LP) of –3.3 V, whereas with using OVP, the HP increases slightly to 0.15 V but the absolute values of low-peak (LP) reduces significantly from 3.3 V to 0.65 V. The stepped-down output voltage V_{bc} increases by about 12% from 1.27 V to 1.42 V and the current consumption I_{VHdd} decreases from 81.5 mA to 74.5 mA, as detailed in Table 5.13. The peak-to-peak ripple voltage of V_{bc} (ΔV_{bc}) has been also improved by about 12.5%.

Table 5.13: Comparison between signal waveforms of the buck converter with and without OVP; in both cases without C_x of 2.5 nF (D=50%)

load condition	*VHdd*	V_{bc}	ΔV_{bc}	$Vout_{max}$	$Vout_{min}$	I_{VHdd}
BC without OVP and C_x	4.0 V	1.268 V	0.256 V	4.02 V	–3.300 V	81.5 mA
BC with Schottky diode	4.0 V	1.423 V	0.224 V	4.15 V	–0.648 V	74.5 mA



(a)

Measure	P1:pkpk(C2)	P2:max(C2)	P3:min(C2)	P4:max(C3)	P5:pkpk(C3)	P6:mean(C3)	P7:rise(C2)	P8:fall(C2)
value	7.33 V	4.02 V	-3.30 V	1.40 V	256 mV	1.268 V	6.539 ns	1.351 ns
status	✓	✓	✓	✓	✓	✓	✓	✓

C1 DC1M 1.00 V/div -600 mV ofst
C2 BwL DC 1.00 V/div -600 mV ofst
C3 BwL DC 1.00 V/div -900 mV ofst
Tbase -44.848 µs 200 ns/div 10.0 kS 5.0 GS/s
Trigger C1 DC Stop 1.13 V Edge Positive

(b)

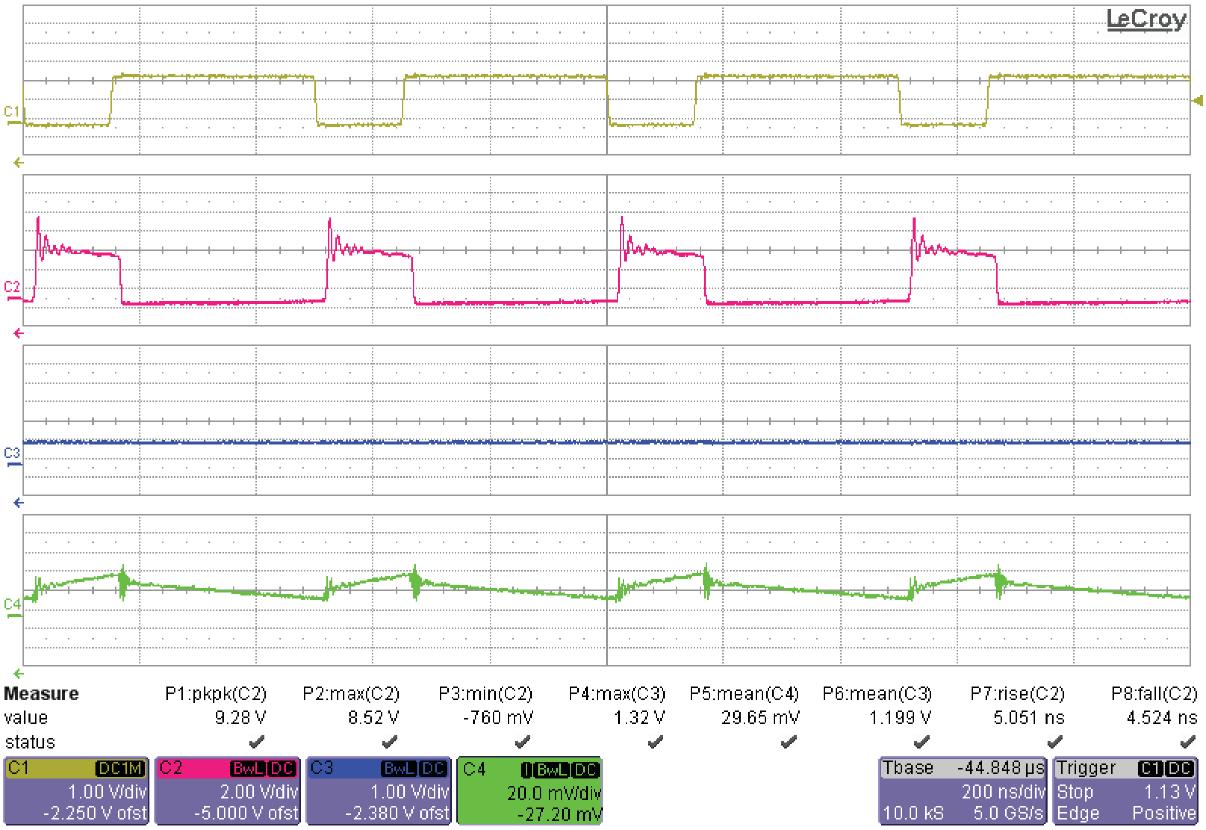
Measure	P1:pkpk(C2)	P2:max(C2)	P3:min(C2)	P4:max(C3)	P5:pkpk(C3)	P6:mean(C3)	P7:rise(C2)	P8:fall(C2)
value	4.80 V	4.15 V	-648 mV	1.53 V	224 mV	1.423 V	7.232 ns	4.335 ns
status	✓	✓	✓	✓	✓	✓	✓	✓

C1 DC1M 1.00 V/div -1.600 V ofst ↓ -108 mV ↑ 2.487 V Δy 2.595 V
C2 BwL DC 1.00 V/div -1.600 V ofst ↓ 4.056 V ↑ -412 mV Δy -4.467 V
C3 BwL DC 1.00 V/div -1.930 V ofst ↓ 1.434 V ↑ 1.409 V Δy -25 mV
Tbase -44.848 µs 200 ns/div 10.0 kS 5.0 GS/s
Trigger C1 DC Stop 1.13 V Edge Positive
X1= 44.7928 µs ΔX= 346.8 ns
X2= 45.1396 µs 1/ΔX= 2.884 MHz

Figure 5.57: The measured waveforms of *Vin* (C1, yellow), *Vout* (C2, red) and V_{bc} (C3, blue) of the proposed buck converter switched by the circuit on the chip *C5* (a) without and (b) with connecting to OVP (*VHdd*=4.0 V)

A comparison between output voltages with and without using the proposed protection (OVP) has not been performed for higher supply voltages, since they would cause damage to the HV-circuit.

Figure 5.58 displays the measured waveforms of *Vin*, *Vout*, V_{bc} and V_{diff}, which are connected to the oscilloscope channels C1, C2, C3 and C4 and coloured yellow, red, blue and green, respectively. The circuit is supplied with 5.5 V, which is stepped down to 1.2 V at a duty-cycle of 70.3%. This is improved by around 7.2%, if compared to the duty-cycle of the previous application using the capacitor C_x of 2.5 nF as overvoltage protection. The minimum value of *Vout* is –0.76 V, which is also improved when compared with the previous value of –1.57 V, as presented in Figure 5.53a. However, the high-peak of *Vout* has become worse with a value of 3.0 V. This high overvoltage could be reduced by connecting the same OVP between the chip output node and the supply voltage rail of *VHdd*. The waveform V_{diff}, which is proportional to the current flowing through the inductor of the buck converter, increases linearly when the input signal is low and *Vout* is high, and then also decreases linearly in the opposite state.



Measure	P1:pkpk(C2)	P2:max(C2)	P3:min(C2)	P4:max(C3)	P5:mean(C4)	P6:mean(C3)	P7:rise(C2)	P8:fall(C2)
value	9.28 V	8.52 V	-760 mV	1.32 V	29.65 mV	1.199 V	5.051 ns	4.524 ns
status	✓	✓	✓	✓	✓	✓	✓	✓

Figure 5.58: The measured waveforms of *Vin* (C1, yellow), *Vout* (C2, red) and V_{bc} (C3, blue) of the proposed buck converter switched by the chip *C5OVP* providing V_{bc} of 1.2 V (*VHdd*=5.5 V, with OVP)

The high- ($\mathrm{HP_{C5OVP}}$) and low-peaks ($\mathrm{LP_{C5OVP}}$) of the output signal of the chip *C5OVP* switching the buck converter have been measured, as plotted in Figure 5.59. The chip *C5OVP* is defined for the chip *C5*, which is assembled with the Schottky diode and resistor. The measurement is accomplished for various supply voltages in the range from 3.9 V to 5.5 V, which are stepped down to 1.2 V at the output of the buck converter by adjusting the duty-cycle of *Vin*.

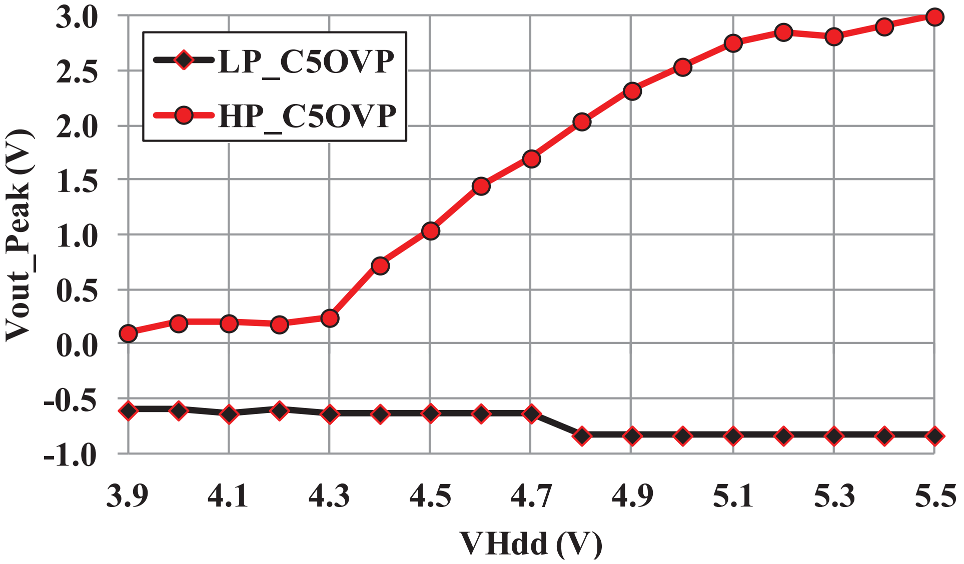


Figure 5.59: The measured high- (HP) and low-peaks (LP) of the output voltage of the chip C5OVP switching the proposed buck-converter vs. the supply voltage (V_{bc}= 1.2 V, with OVP)

Due to the overvoltage protection (OVP), the output waveforms have smaller negative peaks ($\mathrm{LP_{C5OVP}}$) which vary between –0.8 V and –0.6 V, when compared with those ($VoutLP_{C3x}$ and $VoutLP_{C4x}$) of the chips *C3x* and *C4x* using the capacitor C_x, which vary between –1.6 V and –1.2 V as presented in Figure 5.54b. In contrast, the high-peaks rise significantly from 0.1 V to 3.0 V, which is too high and would critically damage the circuit. The voltage drop of low peaks (LP) across *VHdd* from 4.6 V to 4.7 V occurs as a result of adjusting reference voltages by increasing the supply voltage.

In the next step, in terms of verifying the operation of the system, the DC voltage at the converter output (V_{bc}) is investigated with different supply voltages (4.0 V, 4.5 V, 5.0 V and 5.5 V) and a varying duty-cycle of *Vin* in the range of 40% to 80%. In order to prevent driving current higher than 150 mA into the chip - since this would damage the circuit - the buck converter has been switched for a duty-cycle not lower than 40% (42% for the supply voltage 5.5 V). The measured converter output voltage termed as Vbc_{C5OVP} are plotted in Figure 5.60. The applied supply voltages could be stepped down in the range of between 0.45 V to 2.35 V according to the adjusted duty-cycle.

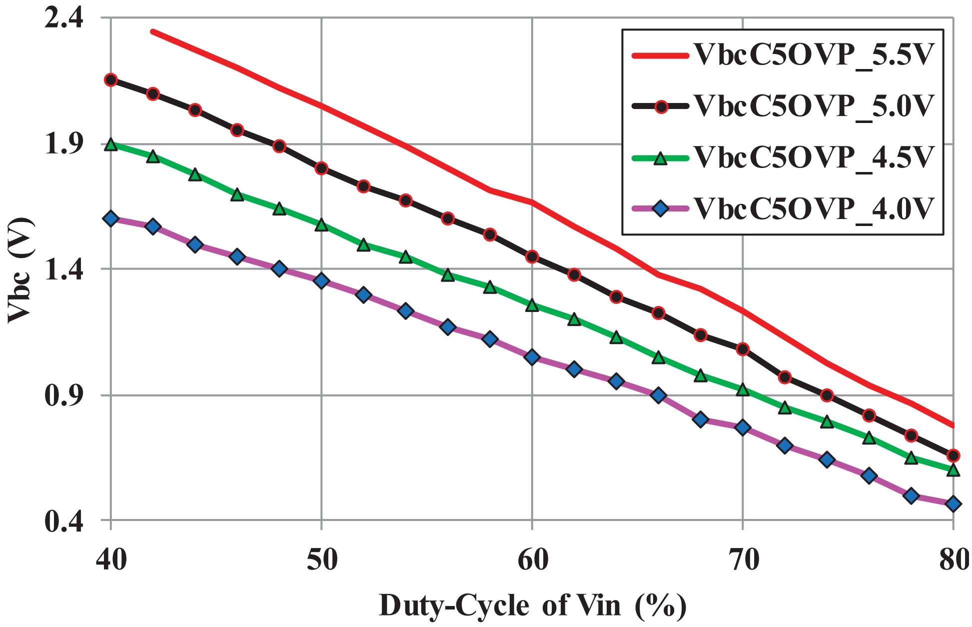


Figure 5.60: The measured output voltage (V_{bc}) of the buck converter switched by the chip *C5OVP* for various supply voltages

The third method used to reduce overvoltages of the driver output signal is described in the next step.

5.2.7.11 Chip-on-Board (COB)

Regarding theories discussed in the section concerning parasitic effects (5.2.7.7) and also simulation and measurement results, it has been shown that bonding wires and lead fingers can impact negatively on circuit performance. These effects become apparent as high and low peaks on the output voltage waveform.

In this work, another technology has been used to eliminate the parasitic effects of package. The chip is directly attached to a so-called daughter circuit board (Figure 5.61a), which is assembled to the main PCB (Figure 5.61b). This technology is defined as "chip-on-board" (COB). Due to the aluminum wire bonding, the pads on the chip are connected to the nickel-gold plated bond pads on the daughter board, as shown in Figure 5.62. The chip bond wires are encapsulated using the glob-top technology to cover them [28][29].

The other advantages of COB as compared to packaging is saving space on the PCB and eliminating the cost of packaging [28][29]. The technology is simpler; however, reworking and changing the chip are difficult or often impossible because the bond wires are not easily removable, which is the major disadvantage of COB.

The major parasitic effects of this technology occur due to the bond wires containing parasitic resistance and inductance. The bond wires are made of aluminum and each of them occupies a resistance of about 0.108 Ω regarding Equation (5.8) and its specific pa-

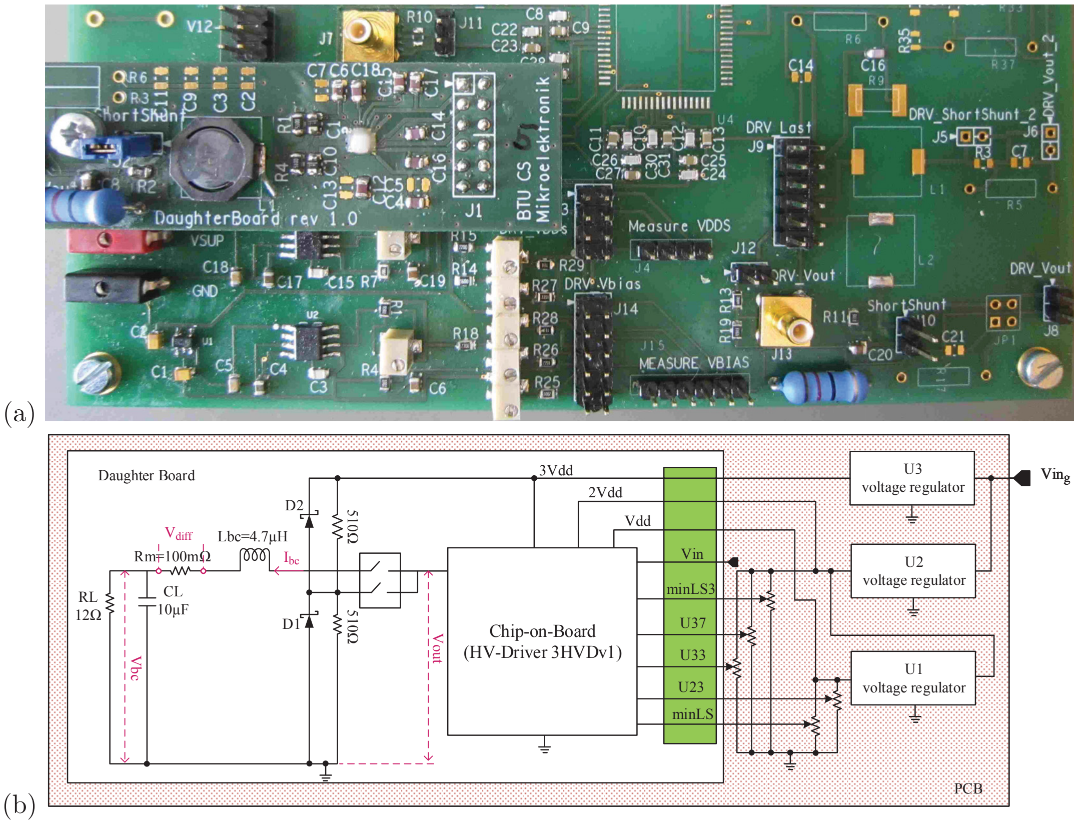


Figure 5.61: (a) Chip-on-board and (b) the principle of the daughter circuit board

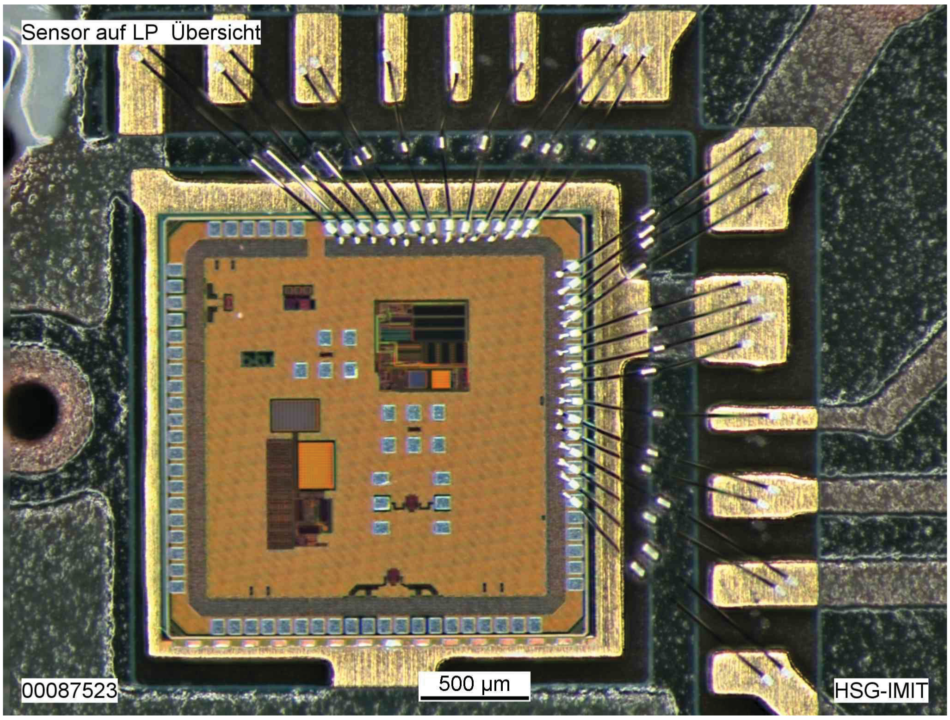


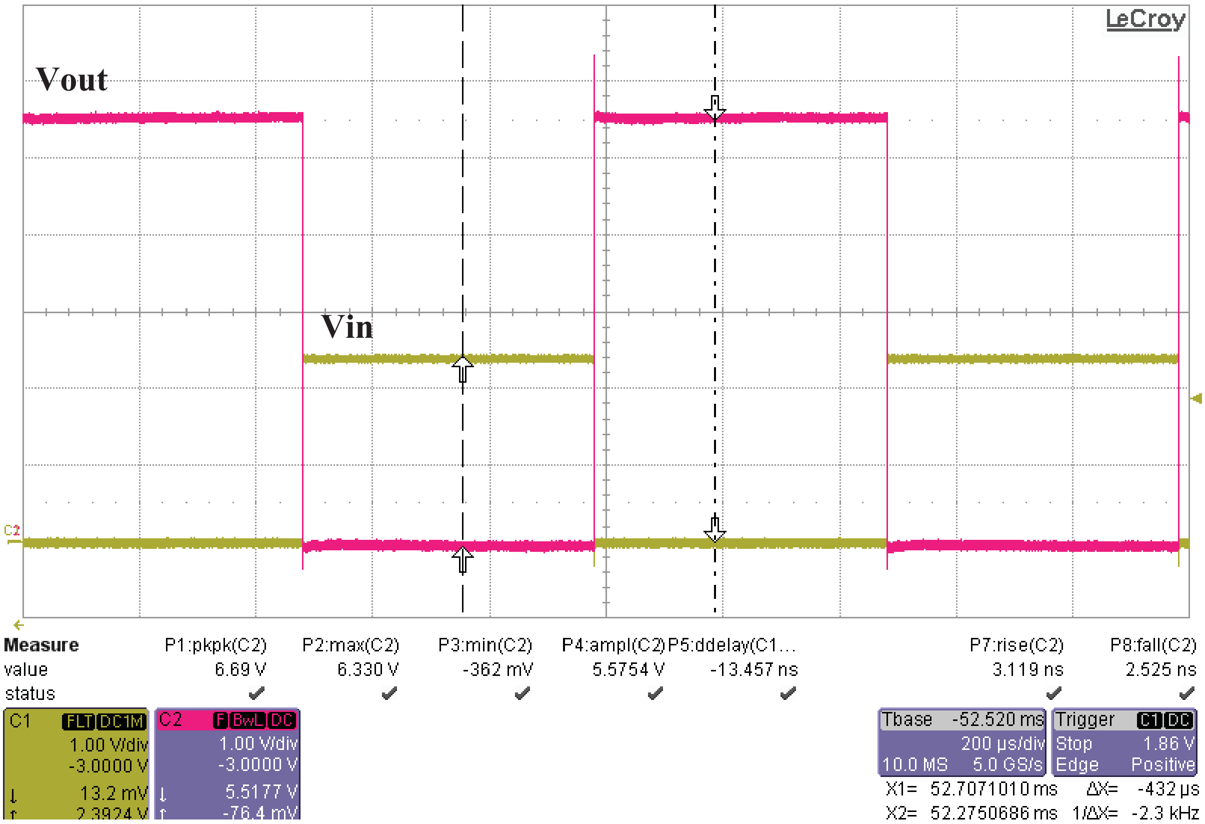
Figure 5.62: Microphotograph of the chip-on-board (assembled and photographed by Mr. H. Schottmann from Hahn-Schickard company)

rameters, electrical resistivity of 2.82×10^{-8} $\Omega\times$m, diameter of 20 μm and a length of about 1.2 mm. In terms of Equations (5.10) and (5.11), the external and internal inductances of a single bond wire are ca. 1.1 nH and 0.06 nH, respectively. It is important to note that the implemented COB has 28 bond wires, of which only four are single. The rest are in a group of two or four wires and parallel to each other; therefore, the inductance of each of them is lower than for a single one because of the mutual inductance effect. Consequently, it can be expected that the peaks of the output voltage of this COB are lower than those of the chip-in-package, especially since the technology is excluded from lead frame fingers.

In this work, the circuit on the chip COB is proved for two conditions: open-load and switching the proposed buck converter that are present below.

5.2.7.12 Chip-on-Board: Dynamic Operation in Open-Load

For the same measurement procedure as applied to previous chips, the same rectangular-pulse signal with a frequency of 1 kHz is fed to the input of the COB in the open-load condition. Figures 5.63, 5.64a and 5.64b show the waveforms of the input (*Vin*) and output (*Vout*) signals on the channels C1 (yellow-green) and C2 (red-violet), respectively.



Measure	P1:pkpk(C2)	P2:max(C2)	P3:min(C2)	P4:ampl(C2)	P5:ddelay(C1...	P7:rise(C2)	P8:fall(C2)
value	6.69 V	6.330 V	-362 mV	5.5754 V	-13.457 ns	3.119 ns	2.525 ns
status	✓	✓	✓	✓	✓	✓	✓

C1 FLT DC1M
1.00 V/div
-3.0000 V
↓ 13.2 mV
↑ 2.3924 V

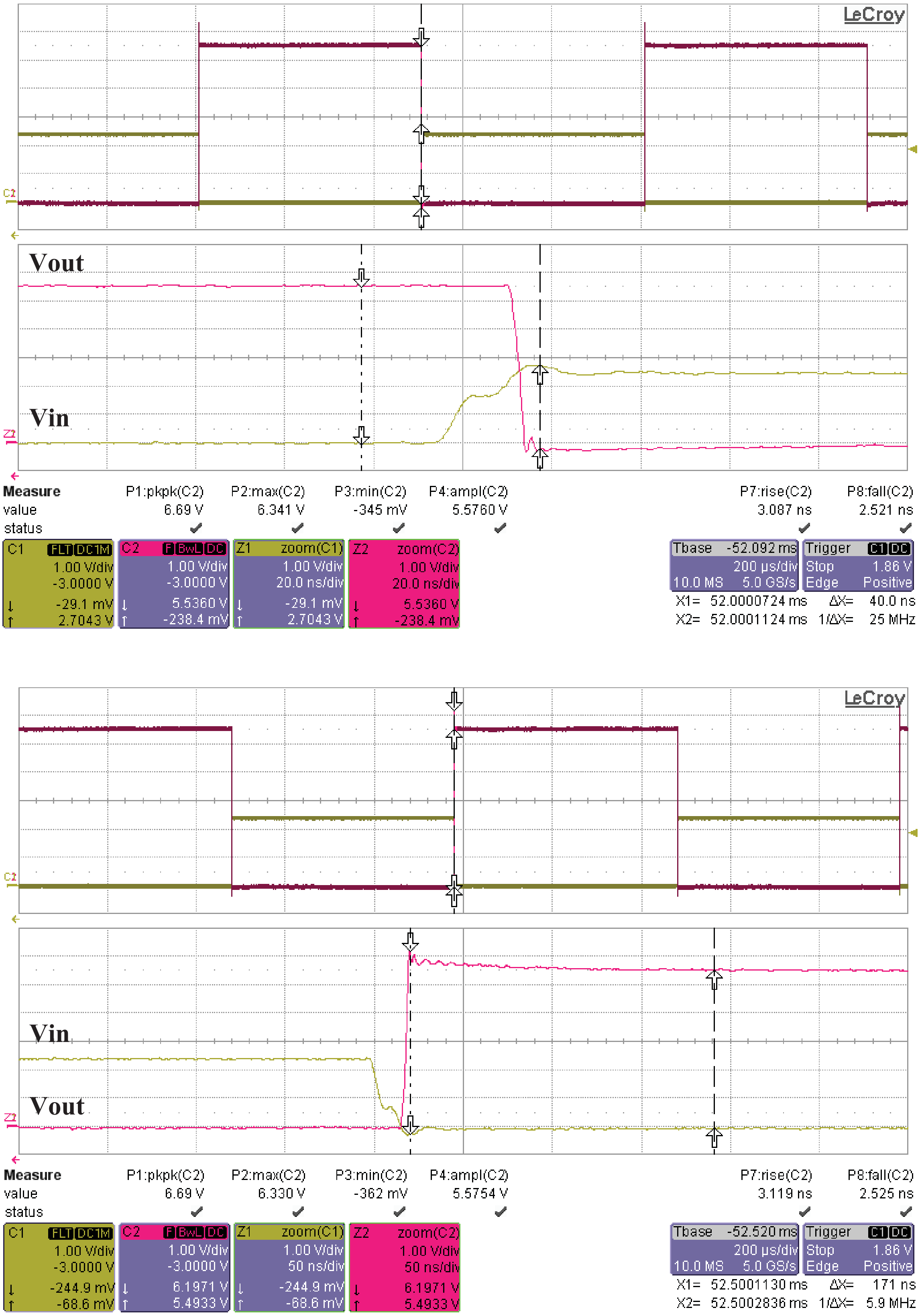
C2 F BwL DC
1.00 V/div
-3.0000 V
↓ 5.5177 V
↑ -76.4 mV

Tbase -52.520 ms
200 µs/div
10.0 MS 5.0 GS/s

Trigger C1 DC
Stop 1.86 V
Edge Positive

X1= 52.7071010 ms ΔX= -432 µs
X2= 52.2750686 ms 1/ΔX= -2.3 kHz

Figure 5.63: The measured waveforms of the input and output voltages of *COB2* (*VHdd*=5.5 V, open-load)



Measure	P1:pkpk(C2)	P2:max(C2)	P3:min(C2)	P4:ampl(C2)	P7:rise(C2)	P8:fall(C2)
value	6.69 V	6.341 V	-345 mV	5.5760 V	3.087 ns	2.521 ns
status	✓	✓	✓	✓	✓	✓

C1 FLT DC1M 1.00 V/div -3.0000 V ↓ -29.1 mV ↑ 2.7043 V
C2 F BwL DC 1.00 V/div -3.0000 V ↓ 5.5360 V ↑ -238.4 mV
Z1 zoom(C1) 1.00 V/div 20.0 ns/div ↓ -29.1 mV ↑ 2.7043 V
Z2 zoom(C2) 1.00 V/div 20.0 ns/div ↓ 5.5360 V ↑ -238.4 mV
Tbase -52.092 ms 200 µs/div 10.0 MS 5.0 GS/s
Trigger C1 DC Stop 1.86 V Edge Positive
X1= 52.0000724 ms ΔX= 40.0 ns
X2= 52.0001124 ms 1/ΔX= 25 MHz

(a)

Measure	P1:pkpk(C2)	P2:max(C2)	P3:min(C2)	P4:ampl(C2)	P7:rise(C2)	P8:fall(C2)
value	6.69 V	6.330 V	-362 mV	5.5754 V	3.119 ns	2.525 ns
status	✓	✓	✓	✓	✓	✓

C1 FLT DC1M 1.00 V/div -3.0000 V ↓ -244.9 mV ↑ -68.6 mV
C2 F BwL DC 1.00 V/div -3.0000 V ↓ 6.1971 V ↑ 5.4933 V
Z1 zoom(C1) 1.00 V/div 50 ns/div ↓ -244.9 mV ↑ -68.6 mV
Z2 zoom(C2) 1.00 V/div 50 ns/div ↓ 6.1971 V ↑ 5.4933 V
Tbase -52.520 ms 200 µs/div 10.0 MS 5.0 GS/s
Trigger C1 DC Stop 1.86 V Edge Positive
X1= 52.5001130 ms ΔX= 171 ns
X2= 52.5002836 ms 1/ΔX= 5.9 MHz

(b)

Figure 5.64: A closer view of the output (b) falling- and (c) rising edges of the measured waveform of the output voltage($VHdd$=5.5 V, open-load)

The circuit is supplied with a high voltage of 5.5 V. The rectangular-pulse signal of the waveform *Vout* shows that the HV-driver circuit on the chip works correctly. As can be seen in these figure, the levels of the output voltage waveform settle to *Vss* and *Vout* according to the high and low levels of the input signal, for which the circuit enters the on- and off-states respectively.

Figures 5.64a and 5.64b give a closer view of the output falling- and rising edges, respectively, according to the input signal. Furthermore, it has to be observed that the output voltages have a positive (HP) and a negative (LP) overvoltage of 0.8 V and –0.3 V respectively, much less than for the chips in package (*C2*, *C3*, *C4* and *C5*), which have maximum absolute values of 1.6 V (HP) and 2.7 V (|LP|), respectively, when compared with the results presented in Figures 5.38a and 5.38b for a supply voltage of 5.5 V.

The fall time of 2.5 ns is about 1.1 ns lower than for the previously measured output voltages, as shown in Figure 5.36b, which are higher than 3.6 ns. The rise time of 3.1 ns is slightly lower (about 0.2 ns) than the measured RTs of other chips, as plotted in Figure 5.36a.

To observe the improvement of overvoltages due to this technology, the high- and low peaks of the driver output voltage are measured for other supply voltages and compared to those of the chips using package technologies. For this reason, two different chips on-board *COB2* and *COB5* have been tested in the open-load condition for various supply voltages in the range from 2.6 V to 5.5 V. Figures 5.65a and 5.65b illustrate the measured high- (HP) and low- (LP) peaks, respectively.

As previously mentioned, the high peaks (HP) are the difference between the maximum and the expected output voltage, which represents the positive output overvoltage. In comparison with the output overvoltages (LP and HP) of the chips *C2*, *C3*, *C4* and *C5*, illustrated in Figures 5.38a and 5.38b, the absolute value of LP of both COBs are substantially lower and vary between 0.2 V and 0.7 V, whereas those of the chips in-package increase from 0.3 V to 1.7 V for *C2* and *C3* and to 2.6 V for *C4* and *C5*. With increasing the supply voltage from 2.6 V to 5.5 V, $Vout_{(LP+HP)}$ of COBs vary between 0.4 V and 1.4 V, whereas $Vout_{(LP+HP)}$ of chips in-package have a value up to 4.5 V.

The results of *COB5* are little worse than those of *COB2*. For example, the differences between LPs of both reach up to 0.3 V. The reason could depend on different daughter boards, bond wiring or the COB technology process.

Figure 5.66 shows the measured rise- (RT) and fall- (FT) times of both COBs' outputs. In comparison with the results of the chips in package (Figure 5.36b), the fall times of COBs remain constant at about 2.5 ns, whereas the rise times of the chips-in-package are ca. 3.5 ns, when the supply voltage is increased over 4.0 V.

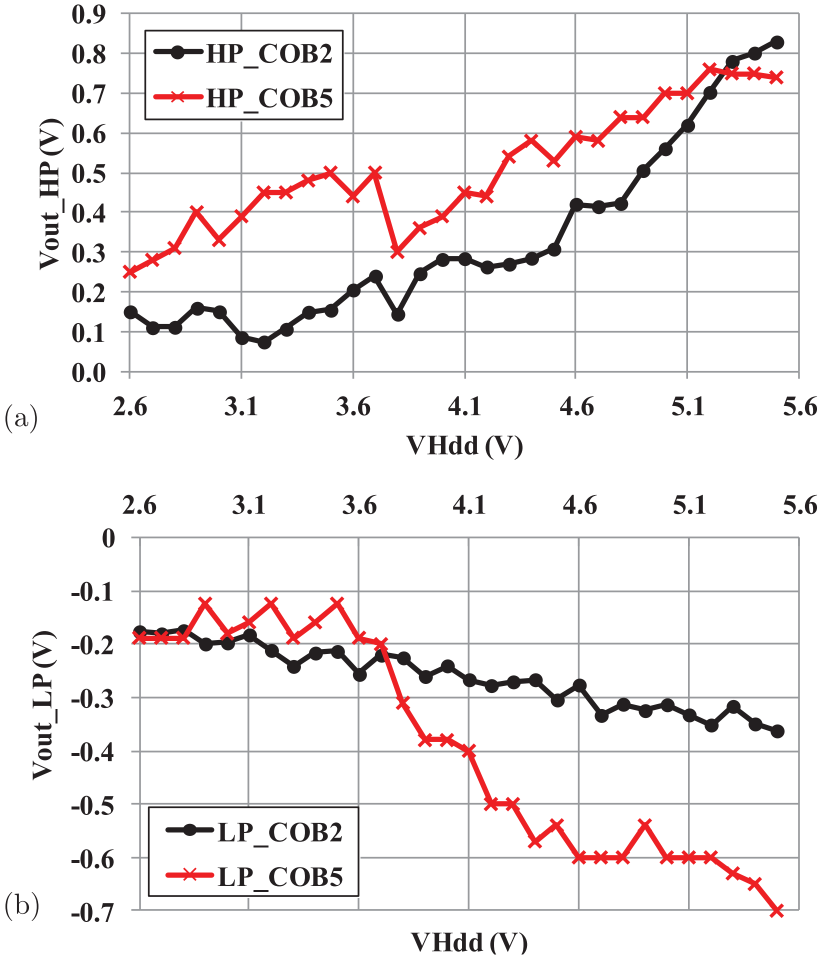


Figure 5.65: The measured output (a) positive- and (b) negative over voltages of *COB2* and *COB5* vs. *VHdd* (open-load)

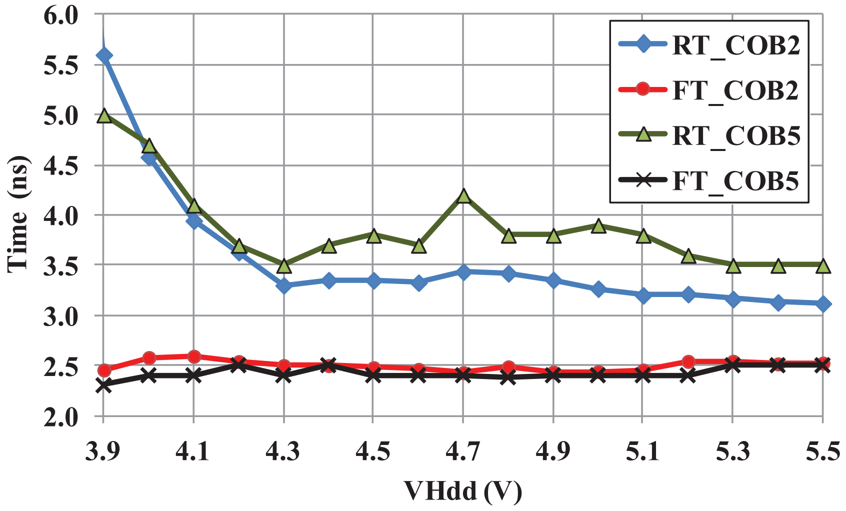


Figure 5.66: The measured rise- (*RT*) and fall- (*FT*) times of the output voltages of the chips-on-board *COB2* and *COB5* vs. *VHdd* (open-load)

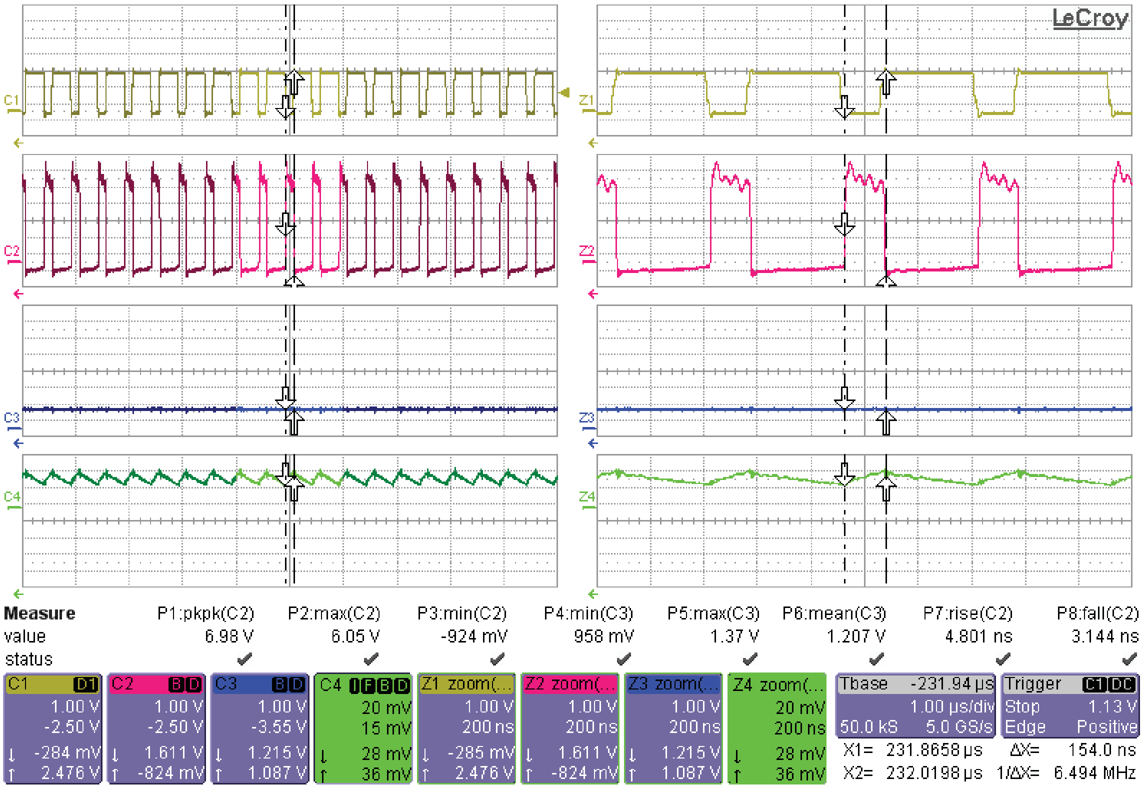
5.2.7.13 Chip-on-Board: Switching Buck Converter

Despite applying the technology COB to avoid high output overvoltages, two overvoltage protection (OVP) devices are also connected, one across the chip output and ground and other one between the chip output and the supply rail of *VHdd*. As previously mentioned, each of these OVP devices comprise a resistor of 510 Ω and a Schottky diode connected in parallel. These devices are intended to protect the circuit from the extra higher overvoltages during switching the buck converter.

Initially, the circuit is supplied with 5.5 V for switching the proposed buck converter, which is also mounted on the daughter board. By adjusting the duty-cycle of the input signal to 70.7%, the supply voltage is stepped down to 1.2 V, as can be seen in Figure 5.67.

The waveforms comprise the input signal *Vin*, the output voltage of the COB (*Vout*), the output voltage of the buck converter V_{bc} and the differential voltage V_{diff} across the resistor R_m. They are connected to the oscilloscope channels C1 (lemon), C2 (red), C3 (blue) and C4 (green), respectively.

The minimum output voltage of COB is –0.9 V, whereas that of the output of the chip-in-package using the capacitor C_x of 2.5 nF with the same supply voltage (5.5 V) is



Measure	P1:pkpk(C2)	P2:max(C2)	P3:min(C2)	P4:min(C3)	P5:max(C3)	P6:mean(C3)	P7:rise(C2)	P8:fall(C2)
value	6.98 V	6.05 V	-924 mV	958 mV	1.37 V	1.207 V	4.801 ns	3.144 ns
status	✓	✓	✓	✓	✓	✓	✓	✓

Figure 5.67: The measured waveforms of *Vin* (channel C1), *Vout* (C2) and V_{bc} (C3) of the buck converter switched by the chip-on-board *COB5* providing V_{bc} of 1.2 V (*VHdd*=5.5 V, with OVP)

–1.6 V, as can be compared with the results in Figure 5.53a. In comparison with chip-in-package *C5OVP* (chip *C5* with OVP connected across the chip output and ground) the positive output overvoltage (HP) of COB reaches up to 0.55 V, whereas that of *C5OVP* is ca. 3.0 V. As can be seen in Figure 5.67, the waveform of the differential voltage V_{diff} is proportional to the current flowing through the inductor (L) of the buck converter, rises and decreases linearly, while the driver output load charges and discharges according to the off- and on-states.

For various supply voltages of 4.0 V, 4.5 V, 5.0 V and 5.5 V, the output voltage V_{bc} of the buck converter has been measured by varying the duty-cycle from 40% to 80%, as plotted in Figure 5.68a. For the supply voltage of 5.5 V, the duty-cycle is set at least at 44%, because for a lower duty-cycle a current of more than 150 mA would drive from the supply into the chip and would damage the circuit.

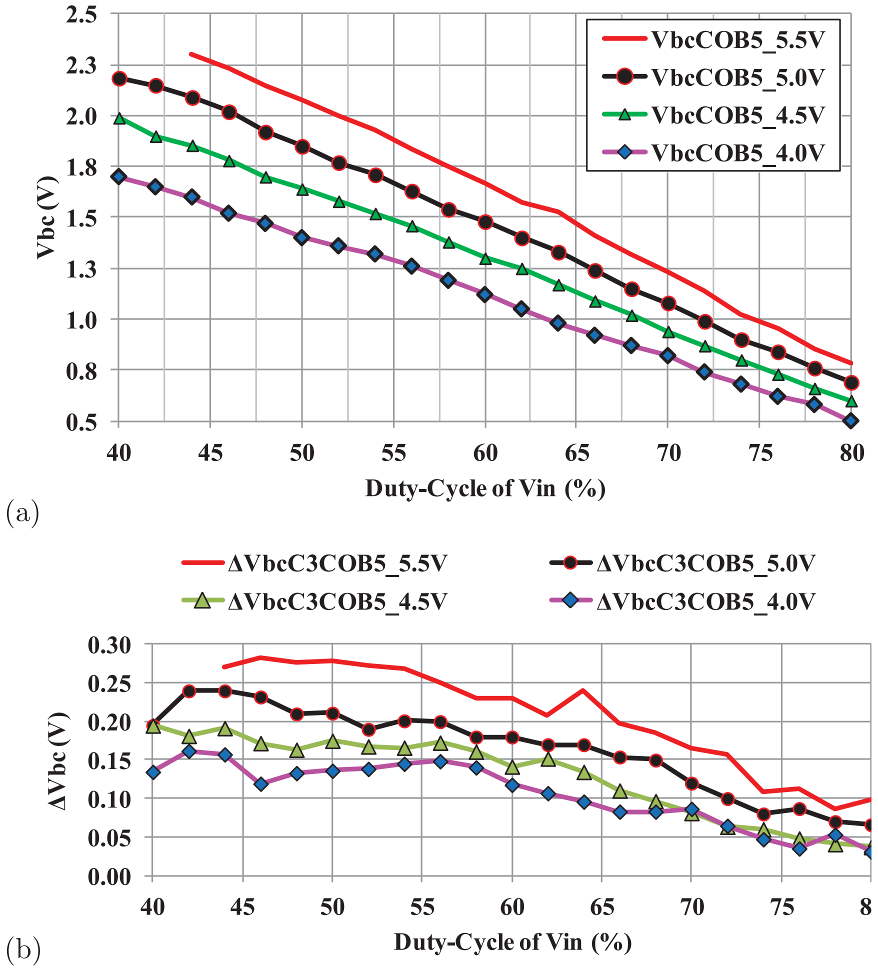
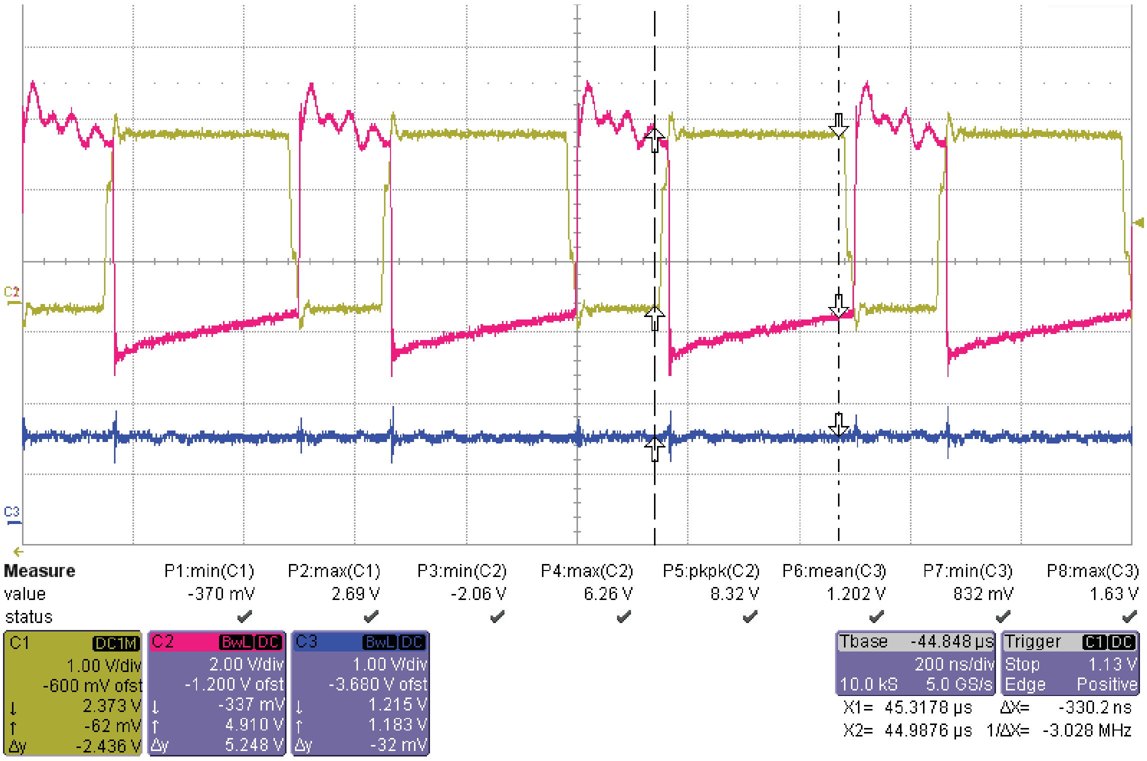


Figure 5.68: (a) The measured output voltage of the buck converter (BC) switched by the chip-on-board *COB5* for various *VHdd*, (b) the difference between these results and V_{bc} for BC switched by the chip-in-package *C3* using C_x of 2.5 nF

The voltage characteristics of V_{bc} are nearly linear. Regarding the applied supply voltages of 4.0 V, 4.5 V, 5.0 V and 5.5 V, they vary in the ranges between 0.5 V–1.7 V, 0.6 V–2.0 V, 0.7 V–2.3 V and 0.8 V–2.3 V, respectively, due to switching the converter with different duty-cycles of *Vin*. The measured voltages V_{bc} of *COB5* are higher than those of the chip in-package *C3* using the capacitor C_x of 2.5 nF at the same duty-cycles. The differences between both voltages (ΔV_{bc}) reach up to about 0.3 V, as plotted in Figure 5.68b. This means that the efficiency of *COB5* is higher than for the chip *C3* using the capacitor C_x of 2.5 nF.

To determine the impact of two overvoltage protection (OVP) circuits on the performance of the chip-on-board, the switching of the buck converter has also been accomplished without these protecting circuits. The measured values are here termed with the suffix "*COBx*". Figure 5.69 shows the waveforms of the input signal *Vin* (green-yellow), output of *COBx* (red-violet) and the buck converter V_{bc} (blue), which are connected to the oscilloscope channels C1, C2 and C3, respectively. The chip is supplied with 5.5 V and the voltage V_{bc} of 1.2 V has been achieved by setting the duty-cycle at 66.6% with a ripple of 0.8 V.

As expected, the low-peaks of the COB output ($VoutLP_{COBx}$) of –2.1 V are significantly lower than those of *COB5* with a value of –0.9 V, as shown in Figure 5.67. Fur-



Measure	P1:min(C1)	P2:max(C1)	P3:min(C2)	P4:max(C2)	P5:pkpk(C2)	P6:mean(C3)	P7:min(C3)	P8:max(C3)
value	-370 mV	2.69 V	-2.06 V	6.26 V	8.32 V	1.202 V	832 mV	1.63 V
status	✓	✓	✓	✓	✓	✓	✓	✓

C1 DC1M	C2 BwL DC	C3 BwL DC
1.00 V/div	2.00 V/div	1.00 V/div
-600 mV ofst	-1.200 V ofst	-3.680 V ofst
↓ 2.373 V	↓ -337 mV	↓ 1.215 V
↑ -62 mV	↑ 4.910 V	↑ 1.183 V
Δy -2.436 V	Δy 5.248 V	Δy -32 mV

Tbase -44.848 µs
200 ns/div
10.0 kS 5.0 GS/s

Trigger C1 DC
Stop 1.13 V
Edge Positive

X1= 45.3178 µs ΔX= -330.2 ns
X2= 44.9876 µs 1/ΔX= -3.028 MHz

Figure 5.69: The measured waveforms of *Vin* (channel C1), *Vout* (C2) and V_{bc} (C3) of BC switched by *COBx* (*COB5* without OVP, *VHdd*=5.5 V)

thermore, the output voltage V_{bc} of the buck converter switched by *COB5* with OVP has been achieved at 1.2 V by a duty-cycle of 70.7% with a ripple of 0.4 V.

5.2.8 Comparison between Different Methods

The performances of the systems, in which the proposed buck converter switches by different chips with and without various types of overvoltage protections, are compared to each other in the following sub-sections.

The suffixes "_*C3*", "_*C4*", "_*C5*" and "_*C6*" are termed for the results of chips *C3*, *C4*, *C5* and *C6* using the capacitor *Cx* of 2.5 nF, "_*C5OVP*" is for the chip *C5* using the presented Schottky diode (OVP) across the chip output and ground, "_*COB2*" and "_*COB5*" for the chips-on-board with two OVPs, one between the chip output and ground and the other across the supply voltage rail of *VHdd* and the chip output, and the suffix "_*COBx*" for the chip-on-board *COB2* without OVPs and *Cx*, as described in Table 5.14.

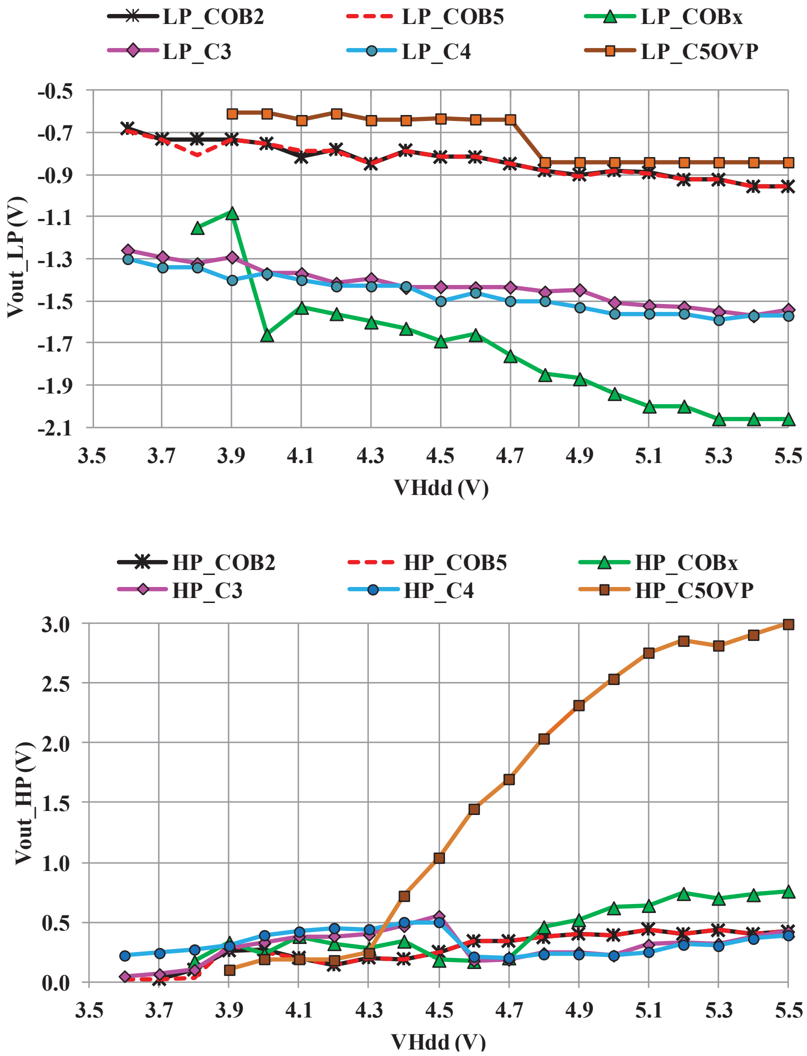
Table 5.14: Descriptions of the suffixes for the measured results

Suffix	**Description**
_*C3*, _*C4*, _*C5*, _*C6*	for chips in-package with a capacitive load *Cx* of 2.5 nF
_*C5OVP*	for chips in-package with Schottky diode (OVP)
_*COB2*, _COB5	for chips on-board with Schottky diode (OVP)
_*COBx*	for chips on-board without Schottky diode (OVP) and *Cx*

5.2.8.1 Output Overvoltages

Figures 5.70a and 5.70b indicate, respectively, a comparison between output low- (LP) and high- (HP) peaks of the chips *C3*, *C4*, *C5OVP*, *COB2*, *COB5* and *COBx* with different technologies, with and without overvoltage protections, which switch the proposed buck converter.

The switching of the buck converter due to the respective method has been accomplished for different supply voltages in the range from 3.6 V/3.9 V to 5.5 V. The duty-cycle of the input cycle is adjusted in terms of achieving a voltage of 1.2 V at the buck converter output. As can be compared in Figure 5.70a, the absolute values of the output low-peaks ($\mathrm{LP_{COBx}}$) of the COB without using OVP raised from 1.1 V to 2.1 V with increasing the supply voltage from 3.6 V to 5.5 V. These values (LP) are higher than those of other chips: *COB2*, *COB5*, *C3*, *C4* and *C5OVP*. The output of the chip *C5* with the overvoltage protection OVP has the smallest low-peaks ($\mathrm{LP_{C5OVP}}$), which vary in the range between –0.6 V and –0.8 V. With increasing the supply voltage, the high-peaks ($\mathrm{HP_{C5OVP}}$) of the chip *C5* with OVP rise rapidly from 0.2 V to 3.0 V, because there is no overvoltage pro-



(a)

(b)

Figure 5.70: The measured output (a) low- and (b) high-peaks of different chips with and without different overvoltage protections vs. *VHdd* (V_{bc}=1.2 V)

tection to reduce the positive high peaks. A Schottky diode is connected between the chip output node and the ground, which reduces the negative spikes on the output voltage. The high-peaks $\mathrm{HP_{C5OVP}}$ are significantly higher than those of other chips, which remain under 0.8 V, as shown in Figure 5.70b. The *COB2* and *COB5* have almost identical high- and low-peaks.

5.2.8.2 Duty-Cycle

Figure 5.71 shows the comparison between the duty-cycle, at which the voltage V_{bc} of 1.2 V has been achieved at the output the buck converter switched by the chips: *COB2*, *COB5*, *COBx*, *C3*, *C4* and *C5OVP* versus the supply voltage varying from 3.6 V/3.9 V to 5.5 V. The duty-cycle (D) characteristic for *COBx* is lower than those for *COB2*, *COB5* and also for *C5OVP*. It approaches to D-characteristics of chips *C3* and *C4*, which indicates that the overvoltage protection containing the resistor and Schottky diode positively impact on the performance of the system.

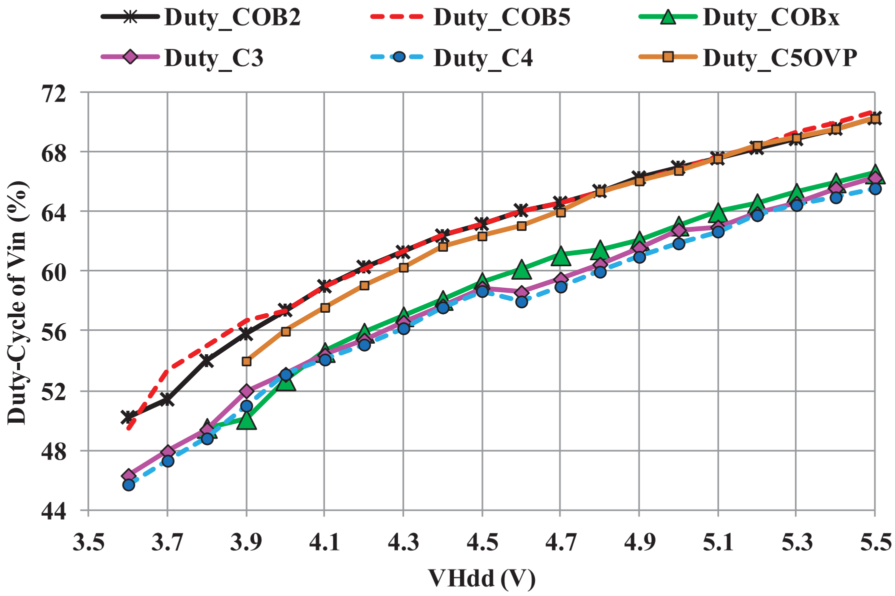


Figure 5.71: The duty-cycles for switching the buck converter by different chips with or without various overvoltage protections achieving V_{bc} of 1.2 V

5.2.8.3 Efficiency

From the measured output voltage (V_{bc}) of the buck converter, the efficiencies of the chips *C3*, *C4*, *C5*, *C6*, *C5OVP* and the chips on board *COB2*, *COB5* and *COBx* are calculated for various duty-cycles (D) of *Vin* with a supply voltage of 5.5 V, according to Equation (2.2) [11] defined in Chapter 2. The results are plotted in Figure 5.72.

The efficiencies of *COB5* and *C5OVP* reach appr. 75%, which is about 10% higher than the efficiencies of other buck converters switched by the chips *COBx* (without OVP and *Cx*), *C3*, *C4*, *C5* and *C6* using *Cx*. From the measured duty-cycle achieving a voltage of 1.2 V (V_{bc}) at the output of the buck converter for each supply voltage (*VHdd*) in the range between 3.6 V and 5.5 V, as previously presented in Figure 5.71, the efficiencies of *C3*, *C4*, *C5OVP*, *COB2*, *COB5* and *COBx* are also calculated according to Equation (2.2). The results are plotted in Figure 5.73. As can be seen, *COB2*, *COB5* and *C5OVP* have the highest efficiencies, varying between 66% and 74.5% in comparison to other chips, whereas the efficiencies of both COBs, *COB2* and *COB5*, are higher than that of *C5OVP* for supply voltages lower than 4.8 V. Their difference reaches up to 3%. The efficiencies of other chips *C3*, *C4* and *COBx* vary between 61.5% and 65%; however, *COBx* has a higher efficiency than *C3* and *C4* for a supply voltage over 4.1 V.

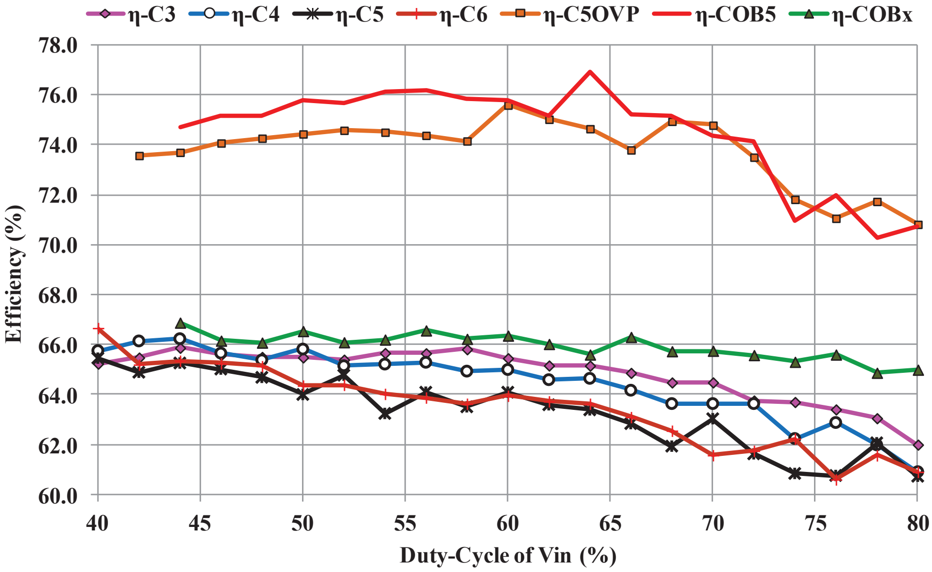


Figure 5.72: Efficiency of the buck converter for different duty-cycle of the input signal with a supply voltage of 5.5 V obtained from measured results

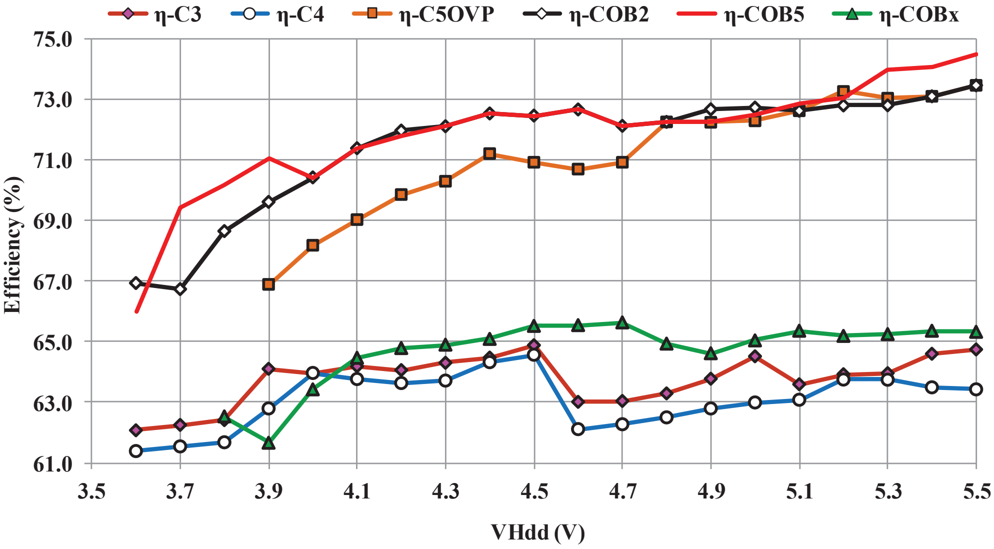


Figure 5.73: Efficiency of the buck converter with an output voltage (V_{bc}) of 1.2 V for different supply voltages obtained from measured results

5.2.8.4 On-Resistance of The Driver Pull-Up Path

In the off-state, the driver pull-up path connects the supply power to the inductor of the buck converter, as shown in Figure 5.74.

The pull-up on-resistance (Ron_{PullUp}) of the designed HV-driver can be calculated from the measured results using the following equation, when **it is assumed that the buck converter has only conduction loss** [5][13][14]:

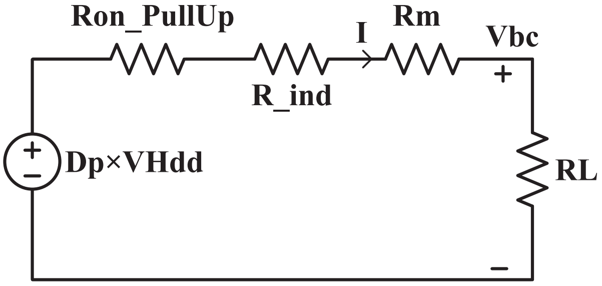


Figure 5.74: The buck converter in the off-state

$$\frac{D_p \times VHdd}{V_{bc}} = \frac{R_L + R_m + R_{ind} + Ron_{PullUp}}{R_L} \tag{5.15a}$$

$$Ron_{PullUp} = \frac{D_p \times VHdd \times R_L}{V_{bc}} - (R_L + R_m + R_{ind}), \tag{5.15b}$$

where R_{ind} is the resistance of the real inductor (L) and has a value of 20 mΩ, as discussed in Chapter 2.

The results of Ron_{PullUp} for different duty-cycle (D) of Vin with a supply voltage of 5.5 V are displayed in Figure 5.75 for the chips in package *C3*, *C4*, *C5*, *C6*, *C5OVP* and the chips on board *COB2*, *COB5* and *COBx*.

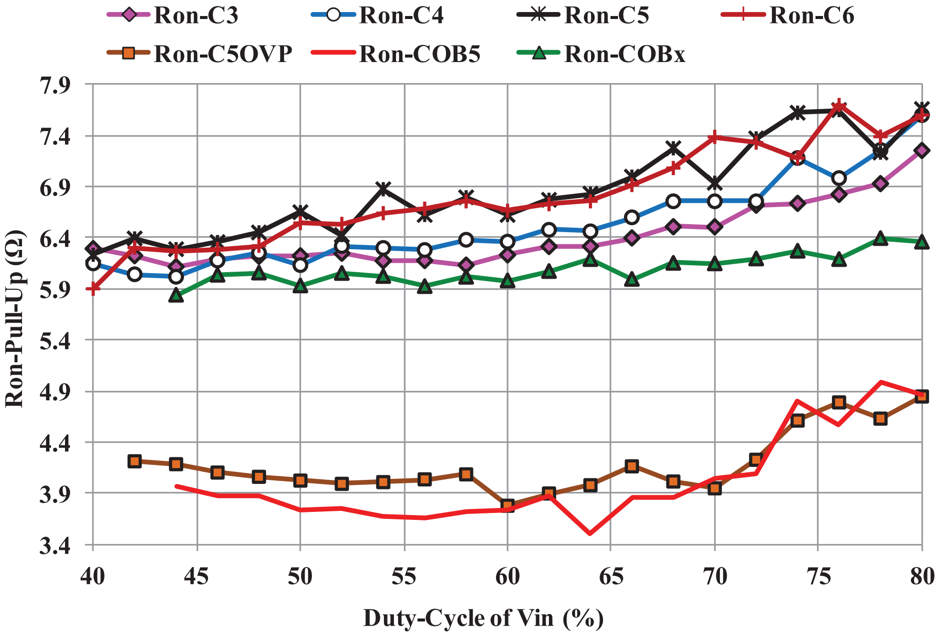


Figure 5.75: The driver pull-up on-resistance of different chips switching the buck converter with a supply voltage of 5.5 V for different duty-cycle of *Vin* obtained from the measured results

The driver pull-up on-resistances of *COB5* and *C5OVP* vary between 3.5 Ω and 4.9 Ω by increasing the duty-cycle D, which approach the value of 4.3 Ω obtained from the measurement results for the chip *C5* as presented in Section (5.2.7.2). In comparison with these results, the calculated on-resistances of other devices (*C3*, *C4*, *C5*, *C6* and *COB*x) varying between 5.9 Ω and 7.7 Ω are much higher with minimum and maximum differences of 1.5 Ω and 2.8 Ω. However, these results are not the real on-resistance of the driver pull-up path, since the chips *C3*, *C4*, *C5*, *C6* and *COB*x have higher power loss and the respective on-resistance can not be obtained correctly from Equation (5.15b).

Chapter 6

Improved Drivers and Level-Shifters

In this chapter, two concepts for HV-drivers are presented, which have been designed in view of the drawbacks identified during the design, simulations, fabrication and measurements of the 3-stacked CMOS HV-driver *3HVDv1* [Pub3] and [Pub4]. The drivers are defined as **3HVDv2** and **4HVDv3**, incorporating versions **2** and **3**, which are based on **3**- and **4**-stacked CMOS transistors respectively; whereby the second design (*4HVDv3*) is an improved form of the first one (*3HVDv2*). Additionally, the level-shifter used in the circuit design of *3HVDv1* is introduced in this chapter. Furthermore, three different pre-input stage circuits are presented for switching an HV-differential-amplifier [Pub7]. The circuits shift down the high-voltage input levels (up to 5.0 V) to low-voltage signals (up to 2.5 V) and they are here defined as **H**igh to **L**ow **V**oltage **L**evel-**S**hifters with the abbreviations **HLV**-level shifter or **HLV-LS**. These HV-circuits are also designed in 65-nm TSMC technology with a nominal I/O voltage of 2.5 V.

6.1 Improved HV-Drivers

The main disadvantage of the presented circuit design methodology and also other common HV-drivers is that the voltage between the terminals of each stacked transistor is exactly on the technology limit for the maximum allowed supply voltage, since the number of stacked CMOS transistors is determined as being equal to the rounded-up integer (N) of the division of the supply voltage $VHdd$ by the nominal voltage Vn [31]–[36]. In this case, unexpected overvoltages caused by parasitic effects would damage the circuit on the chip.

The following major points have been considered in designing the two HV-driver circuits [Pub3][Pub4]:

1. Designing without capacitors because they occupy more space on the chip and if connected to the driver nodes, the switching times increase.

2. Designing without resistors (R) because they have different current load characteristics to transistors and can cause an overvoltage. Furthermore, the threshold voltage of a transistor varies with its effective length and can not be matched with R.

3. Designing the HV-driver based on *N+1*-stacked CMOS or higher to avoid an overvoltage between the terminals of each transistor, where N is the rounded-up quotient of the division of *VHdd* by *Vn*.

   As shown in the last chapter, due to the inductive parasitic effects of the bond wires, lead frames, interconnecting wires on the chip and also on the PCB, maintaining the voltage between each of the transistor terminals within the technology limit cannot be 100% guaranteed. Therefore, adding one stacked CMOS is more reliable for avoiding an overvoltage; however, this increases the on-resistance of the driver leading to longer switching times and negatively impacts on the efficiency of the switched buck converter.

4. By adding an extra CMOS, the range of the applied supply voltages can be extended for a more flexible application

5. Designing without including RC-circuits, which are integrated in the previously design *3HVDv1* at the gates of the input CMOS transistors for adjusting the input signals to the driver node voltages. Consequently, these circuits limit the flexibility of the applied supply voltage.

6. Preferably with a minimal number of, or without any reference voltages, since this requires extra circuits such as voltage dividers containing additional passive and/or active elements which would increase the likelihood of overvoltages.

6.1.1 High-Voltage Driver 3HVDv2

Regarding the above points, a HV-driver defined as **3HVDv2** is designed based on 3-stacked CMOS transistors for switching a buck converter. The circuit is optimised for arbitrary supply voltages from 2.6 V to 6.0 V. This range of 3.4 V is extended by 40% when compared with common drivers being suitable for a supply voltage range of 2.4 V. For controlling the gates of the stacked transistors, a method is used as described in the next step [Pub3].

6.1.1.1 Method of Design

Figure 6.1a presents the background idea of the method to regulate the gate terminals of a kth–stacked nMOS transistor (Mn) of the HV-driver. Two resistors, R_{z1} and R_{z2}, form a voltage divider and the pMOS transistor M_x regulates the main transistor Mn in off- and on-states. The gate and source nodes of the transistor M_x are connected to the source and gate nodes of Mn, respectively.

In the off-state, since the input signal is low (0 V), the pull-down nodes of the main stage start to charge. Regarding the provided gate voltage V_{g_off}, the transistor Mn turns off when its gate-source voltage reaches its threshold voltage V_{thn}; therefore, its source voltage is charged to "$V_{g\_off} - V_{thn}$" and then rises to nearly V_{g_off} due to the sub-threshold current.

In the on-state, the input signal of the HV-driver is high and turns the first nMOS transistor on; therefore, the pull-down nodes discharge to ground. In this condition, the gate voltage of Mn defined as V_{g_on} follows its source voltage due to the pMOS transistor M_x, which turns on because its gate-source voltage increases since the gate node of M_x is connected to the driver pull-down path. As a result, the transistor M_x pulls the gate voltage of Mn down. By determining suitable transistor dimensions of M_x, the gate-source voltage of Mn can be kept equal to or lower than Vn (2.5 V).

As previously mentioned, resistors have different current load characteristics to transistors. Therefore, to avoid an overvoltage, in-series connected transistors (M_{z1}–M_{zk}) containing MOS-diodes (gate-drain connected transistors) and/or transistors controlled by reference voltages are used rather than R_{z1} and R_{z2} (Figure 6.1b).

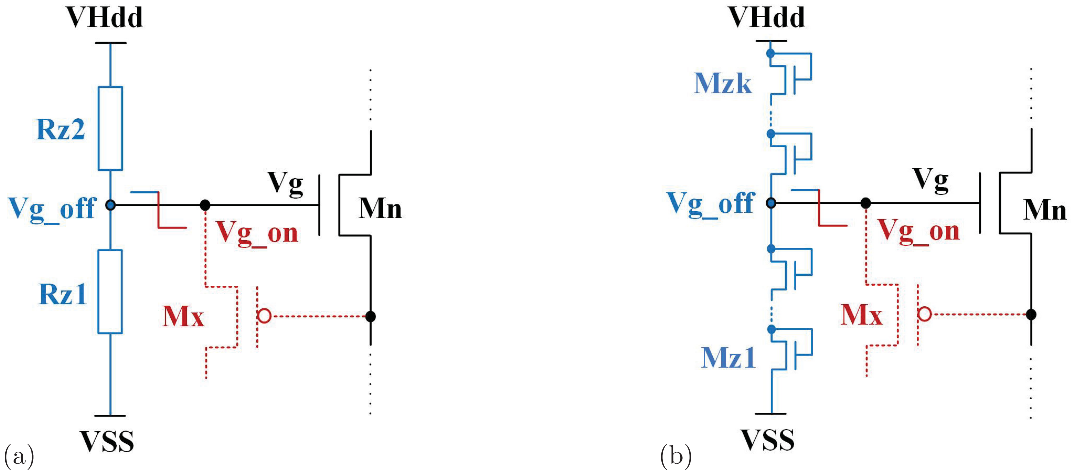


Figure 6.1: Regulating the gate-voltage of a stacked nMOS transistor due to a voltage divider consisting of (a) resistors or (b) transistors

For regulating “*N+1*”-stacked nMOS transistors of a HV-driver according to on- and off-states, a pre-circuit comprising two stages is employed. This is also defined as a gate-controlling circuit. One stage consists of stacked pMOS transistors, whose gates are connected to the respective pull-down nodes, and the second stage operates as a voltage divider containing transistors M_{z1}–M_{zk} (gate-drain connected transistors with or without transistors biased by reference voltages). For regulating the pMOS transistors, the complementary form of the described design is used. In the next section, the circuit design of *3HVDv1* is described.

6.1.1.2 Circuit Design

Based on the described method and considering the previously mentioned points for circuit design, a 3-stacked CMOS HV-driver defined as *3HVDv2* is designed as illustrated in Figure 6.2. The circuit is supplied with a high voltage termed as *VHdd* and consists of four stages. The first stage contains the main stacked transistors, Mn1, Mn2, Mn3, Mp1, Mp2 and Mp3, and is switched with the input signals *Vin* and *Vpin*.

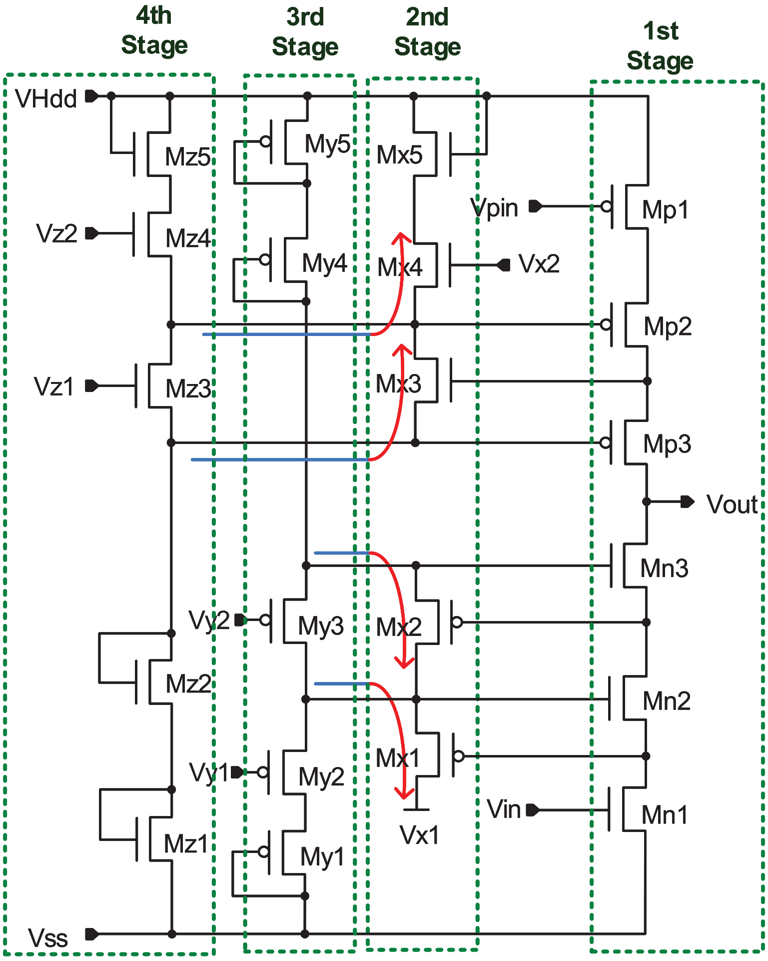


Figure 6.2: The circuit of the 3-stacked CMOS HV-driver *3HVDv2*

The second stage containing the transistors M_{x1}–M_{x5} is based on two separated parts providing the gate-voltages in the on-state. The first part of the 2nd stage comprises the two series-connected pMOS transistors M_{x1} and M_{x2}, which regulate the gates of the nMOS transistors Mn2 and Mn3 by pulling current from their gate nodes to the low voltage rail of V_{x1}. As a result, the gate-voltages follow the corresponding source voltages.

The second part of the 2nd stage includes three series-connected nMOS transistors M_{x3}, M_{x4} and M_{x5}, which drive current from supply to the gates of Mp2 and Mp3 in order to pull up their voltages. As a consequence, the pMOS transistors turn off. It should be noted that the gate of M_{x4} is biased by a reference voltage of V_{x2} to make the driver flexible for different *VHdd*, and the gate-drain connected transistor M_{x5} is employed to avoid an overvoltage.

The third stage contains five in-series connected pMOS transistors M_{y1}–M_{y5} and operates as a voltage divider regulating the gates of the 2nd- and 3rd-stacked nMOS transistors (Mn2 and Mn3) in the off-state. M_{y1}, M_{y4} and M_{y5} are gate-drain connected transistors. In order to make the driver flexible for different supply voltages, the gates of M_{y2} and M_{y3} are biased by reference voltages V_{y1} and V_{y2}.

The fourth stage operates also as a voltage divider providing gate voltages for the pMOS transistors Mp2 and Mp3 in terms to turn the pMOS transistors on in the driver off-condition. This stage comprising five nMOS transistors (M_{z1}–M_{z5}) is the complementary form of the third stage.

The major advantage of this driver is that it can be applied for a supply voltage in the range of 2.6 V to 6.0 V.

6.1.1.3 Simulation Results

Figure 6.3 shows the transient simulation results of the output voltages of the designed HV-driver *3HVDv2* for various supply voltages in the range from 2.6 V to 6.0 V. As expected, regarding the on- and off-states, the driver output is discharged and charged between ground and the supply voltage *VHdd*, which build a pulse-shaped form signal. This indicates the correct functionality of the HV-driver. This circuit is proved also by switching the previously described buck converter, containing an inductor L of 4.7 nH, a capacitor C_L of 12 μF, resistors R_m of 100 mΩ and R_L of 12 Ω. In Figure 6.4, the output voltages of the HV-driver (*Vout*) and the buck converter (V_{bc}) are plotted regarding to the input signals *Vin* and *Vpin* with 2 MHz frequency. The input signal *Vpin* with levels of 3.5 V and 6.0 V are shifted up, respectively from the levels 0 V and 2.5 V of the input signal *Vin* due to an adapted level-shifter. With an input duty cycle of about 79% (D_{bc}=21%), a voltage (V_{bc}) of 1.2 V can be obtained from the supply voltage of 6.0 V at the output of the buck converter.

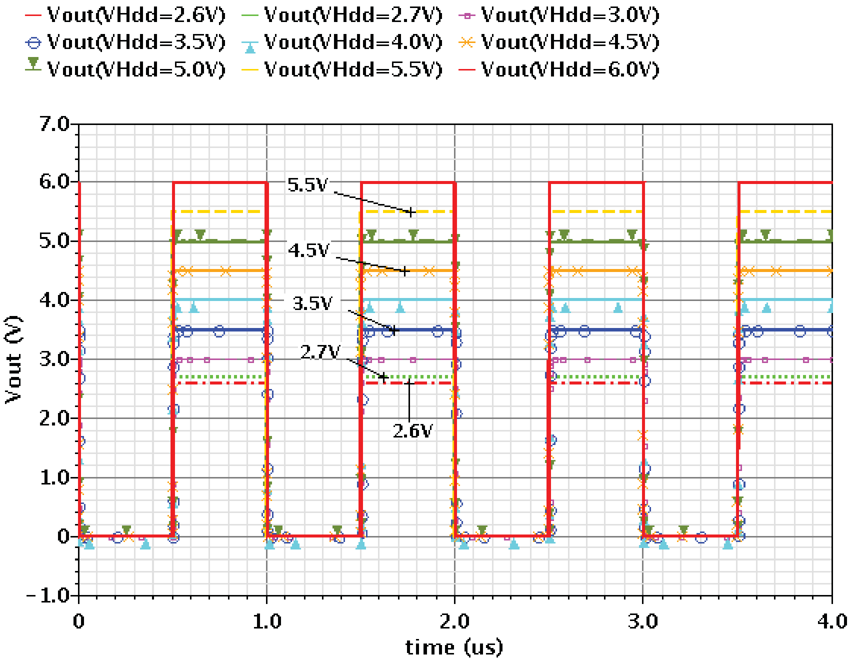


Figure 6.3: Output signals of the HV-driver *3HVDv2* for different supply voltages

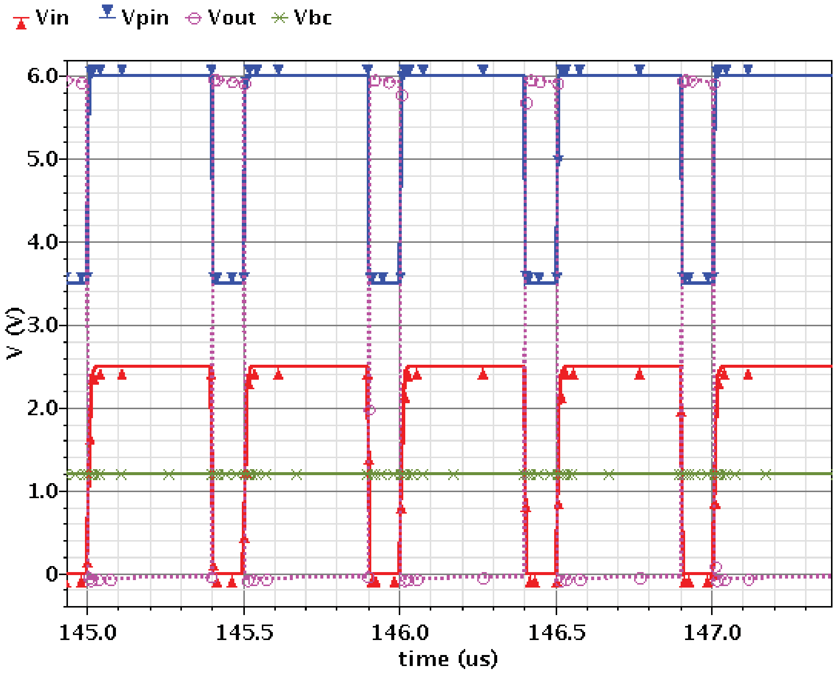


Figure 6.4: Input and output voltage characteristics of the driver and the buck converter switched by *3HVDv2* with *VHdd* of 6.0 V

6.1.1.4 Comparison with HV-Driver 3HVDv1

Table 6.1 gives a comparison of the dynamic power consumptions (P), the rise- (RT) and fall (FT) times of the output voltages of this work (*3HVDv2*) with the previous work (*3HVDv1*) for different supply voltages in the open-load condition.

The driver *3HVDv2* has a lower dynamic power consumption and better rise times in comparison with the driver *3HVDv1*. It should be noted that these results are obtained from simulation without considering the parasitic effects. The range of the applied supply voltages of the HV-driver *3HVDv2* is wider than that for *3HVDv1*.

Table 6.1: Rise-, fall times and power consumption of the HV-drivers *3HVDv1* and *3HVDv2* (open-load)

VHdd [V]	**HV-Driver 3HVDv2**			**HV-Driver 3HVDv1**		
	RT [ns]	*FT [ns]*	*P [mW]*	*RT [ns]*	*FT [ns]*	*P [mW]*
6.0	1.22	1.15	66.1	–	–	–
5.5	0.99	1.25	46.7	1.36	0.85	59.2
4.5	1.51	1.35	29.4	1.8	0.60	42.9
3.5	0.54	1.36	8.5	1.78	0.41	24.9
2.6	0.66	1.54	7.4	–	–	–

6.1.2 High-Voltage Driver 4HVDv3

Based on the method described in Section 6.2.1, a 4-stacked CMOS HV-driver defined as **4HVDv3** is designed, which is an improved circuit model of the previous HV-driver *3HVDv2*. The driver is optimised for arbitrary supply voltages from 3.5 V to 7.5 V. This range is extended by 66% when compared to common HV-drivers being suitable for a supply voltage range of 2.4 V. The control voltages to regulate the stacked transistors of the HV-driver are achieved by using a self-biasing method; therefore, reference voltages are not required. The circuit is stable for temperatures between –40 °C and 125 °C.

6.1.2.1 Circuit Design

The gate-controlling circuit of the HV-circuit *3HVDv2* is regulated by six different reference voltages, V_{x1}, V_{x2}, V_{y1}, V_{y2}, V_{z1} and V_{z2} (Figure 6.2) and these require extra circuits such as voltage dividers containing passive and/or additional transistors. These make the design of the HV-circuit more complicated and increase the circuit area.

Figure 6.5 presents the circuit design of the HV-driver *4HVDv3*, which is based on 4-stacked nMOS transistors (Mn1–Mn4) in the pull-down and 4-stacked pMOS transistors (Mp1–Mp4) in the pull-up path. Regarding the on- (pull-down active) and off-state (pull-up active), the node voltages of the driver's transistors are depicted in this figure.

The stacked transistors are regulated by a pre-circuit supplied with the same high-voltage *VHdd*, which is applied for the main stage of the HV-driver. The pre-circuit is

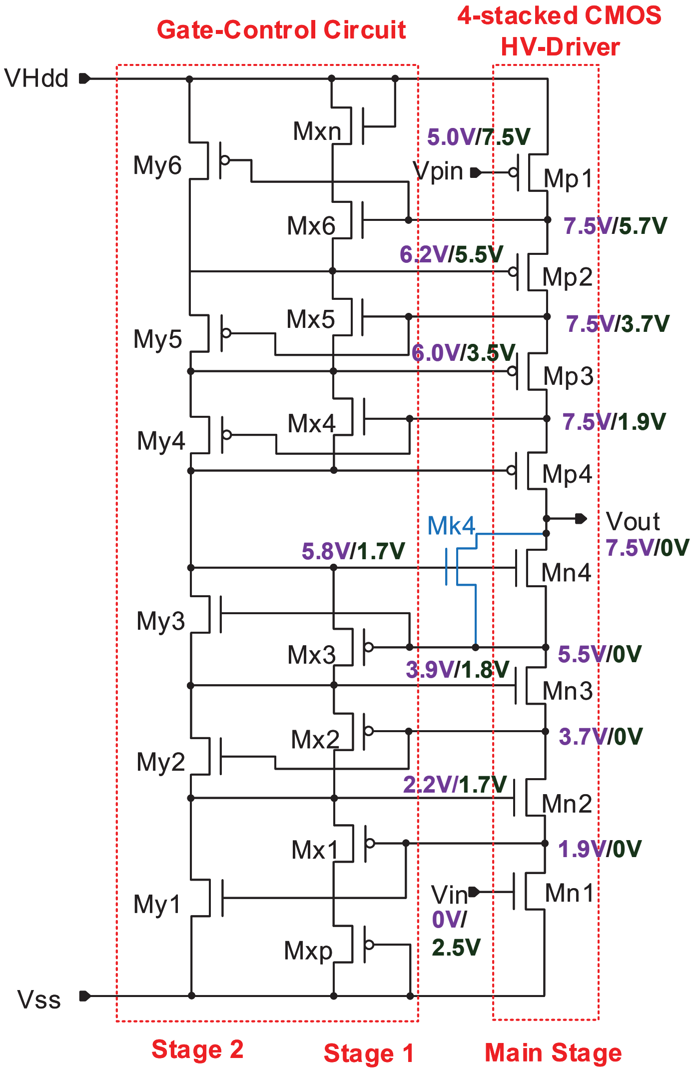


Figure 6.5: The circuit design of the 4-stacked CMOS HV-driver *4HVDv3*

defined as a gate-controlling circuit and based on two stages. The first stage contains two parts: upper and lower parts.

The upper part comprises in-series connected nMOS transistors (M_{x4}–M_{x6} and M_{xn}) controlling the gates of the driver pull-up transistors in the off-state, whereas the lower part is formed by in-series connected pMOS transistors M_{x1}, M_{x2} and M_{x3}, which respectively regulate the gate nodes of Mn2, Mn3 and Mn4 in the on-state. The gates of M_{x1}–M_{x6} are connected to the pull-down and pull-up nodes, respectively. The transistors M_{xn} and M_{xp} are added to avoid an overvoltage.

The second stage comprises six in-series connected transistors: three nMOS transistors M_{y1}, M_{y2} and M_{y3} operate as a voltage divider for regulating the gates of Mn2, Mn3 and Mn4 in the off-state, whereas the three pMOS transistors M_{y4}, M_{y5} and M_{y6} control Mp2, Mp3 and Mp4 in the on-state.

The function of the pre-circuit is as follows:

- In the off-state, the input signal of 0 V turns Mn1 off, the source node of Mn2 starts charging until the difference between this voltage and the gate voltage (VG_{n2}) of Mn2, which is provided by the voltage divider of the second stage (M_{y1}–M_{y3}) reaches down to the absolute value of the threshold voltage of M_{x1}. As a consequence, M_{x1} and Mn2 turn off because both gate-source voltages of Mn2 and M_{x1} fall below their threshold voltages. In the same process, the other stacked nMOS transistors Mn3 and Mn4 turn off according to the provided gate voltages by the voltage divider and off-condition of the control transistors M_{x2} and M_{x3}.

  Since the transistors M_{y1}, M_{y2} and M_{y3} are on, the source voltages of M_{x4}–M_{x6} and M_{xn} are reduced in terms of keeping the pMOS transistors Mp2, Mp3 and Mp4 on. Consequently, the nodes of the pull-up path and the driver output are charged to the supply voltage *VHdd*. By adjusting the dimensions of M_{x4}, M_{x5} and M_{x6}, the voltage difference across the terminals of each transistor remains within the technology limit of 2.5 V.

- In the on-state, since the nMOS transistor Mn1 is on, the pull-down path of the driver starts to discharge. Therefore, the pMOS transistors M_{x1}, M_{x2} and M_{x3} turn on. As a consequence, the gate voltages VG_{n2}, VG_{n3} and VG_{n4} are pulled down in order to maintain the voltage differences across the terminals of each corresponding transistor within the technology limit of 2.5 V in the on-state. However, the transistor dimensions of M_{x1}, M_{x2}, M_{x3} and M_{xp} are also adjusted to achieve this considerable point. In this on-state, the stacked pMOS transistors in the driver pull-up path are turned off because of the provided high voltages due to the pMOS transistors M_{y4}, M_{y5} and M_{y6}.

Because of the different transistor characteristics of the pull-down and pull-up paths, the node between both is critical, which causes an overvoltage across drain and source nodes of Mn4. Therefore, an nMOS transistor M_{k4} is added in parallel to M_{n4} to avoid this problem.

6.1.2.2 Simulation Results

The transient waveforms of the pull-down and pull-up node voltages of the designed HV-driver can be observed according to the input signals *Vin* and *Vpin* in Figures 6.6 and 6.7, respectively. The circuit is supplied with the maximum proposed applied supply voltage of 7.5 V. In the off-state (pull-up active), when the input signals *Vin* and *Vpin* are 0 V and 5.0 V respectively, the source nodes of Mn2, Mn3, Mn4 and the output node are charged to about 1.9 V, 3.7 V, 5.5 V and 7.5 V respectively, whereas the source nodes of Mp2, Mp3 and Mp4 are charged to 7.5 V, as shown in Figure 6.7.

In the on-state (pull-down active), the input signals *Vin* and *Vpin* are 2.5 V and 7.5 V, respectively. The driver pull-down and also output nodes discharge to ground. Since the transistor Mp1 is off and the pull-up path is active, the source nodes of Mp2, Mp3 and Mp4

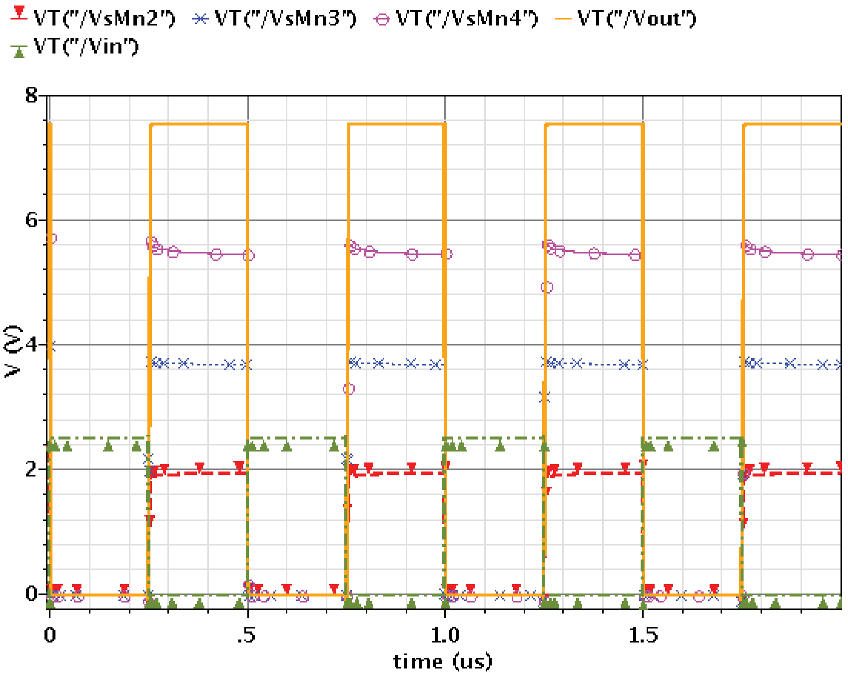


Figure 6.6: Voltage characteristics of the driver pull-down nodes and *Vin*

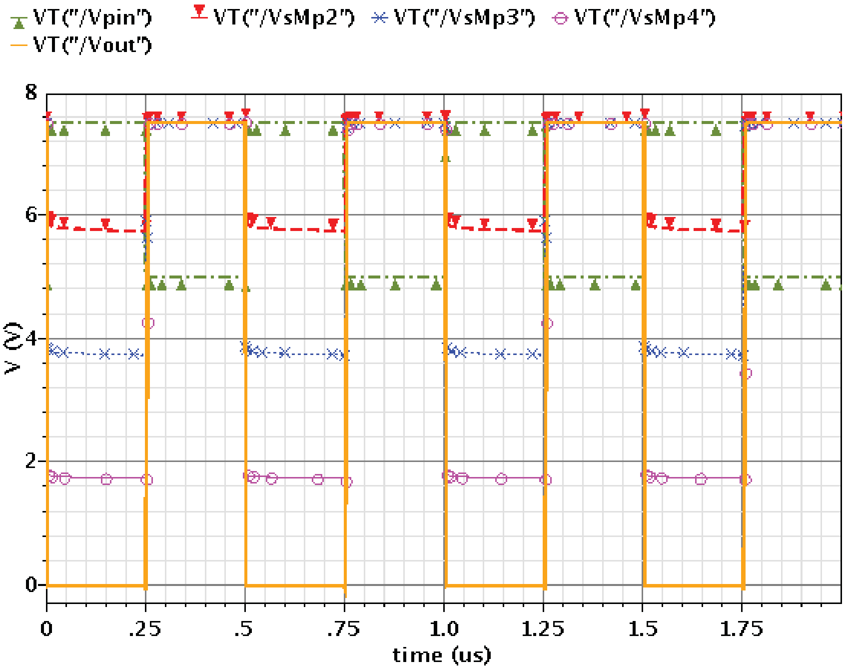


Figure 6.7: Voltage characteristics of the driver pull-up nodes and *Vpin*

discharge also from the supply voltage of 7.5 V, but to 5.7 V, 3.7 V and 1.9 V, respectively, according to the appropriate gate voltages.

The transient simulation output voltage *Vout* of the proposed 4-stacked CMOS HV-driver is plotted in Figure 6.8 for different supply voltages in the range from 3.5 V to 7.5 V. The driver is in an open-load condition. The output voltage is a rectangular-pulse form with low and high levels of 0 V and *VHdd*, which indicates the output node is charged and discharged between *VHdd* and ground according to the off- and on-state. This verifies the correct operation of the HV-driver.

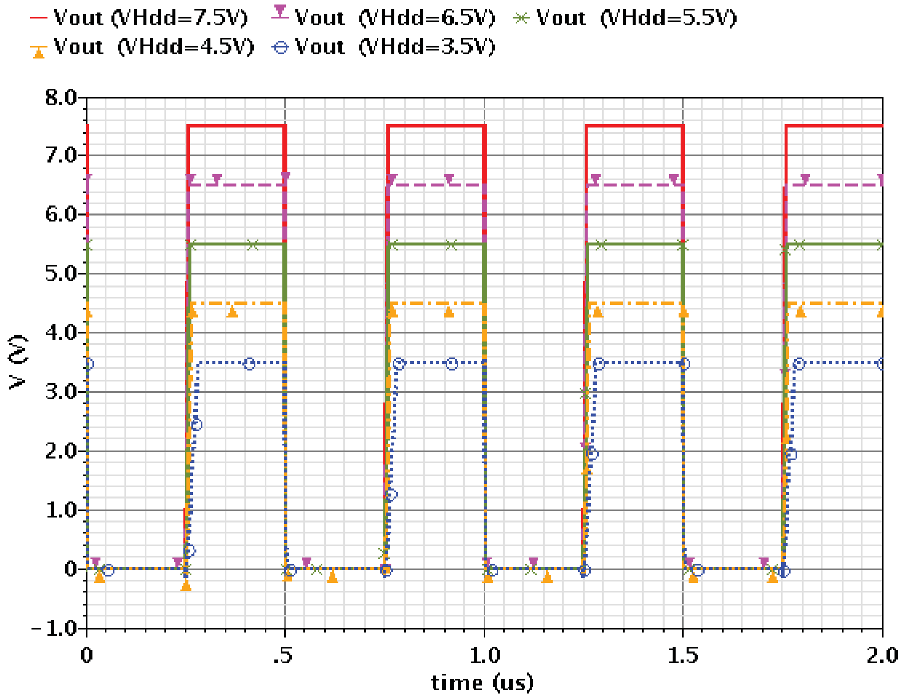


Figure 6.8: Output signals of the HV-driver *4HVDv3* for different *VHdd* (open-load)

In order to switch the proposed buck converter, the number of parallel connected transistors in each stack is adjusted. Figure 6.9 shows the simulated transient characteristics of the output voltage of the driver *Vout*, of the buck converter V_{bc} and the current I_{bc} according to the input signals *Vin* and *Vpin*. A voltage of 1.2 V at the converter output has been achieved from the supply voltage of 5.5 V with a duty-cycle (D_{Vin}) of 76.0%, which is equal to D_{bc} of 24.0%.

Under an open-load condition, the HV-driver circuit is simulated with the maximal applied supply voltage of 7.5 V for different process variations and temperatures between – 40 °C and 125 °C. The provided rectangular output signals, which vary between two levels 0 V and 7.5 V, indicate that the circuit operates correctly at every corner (Figure 6.10). Furthermore, at each corner, there is no overvoltage between terminals of each transistor.

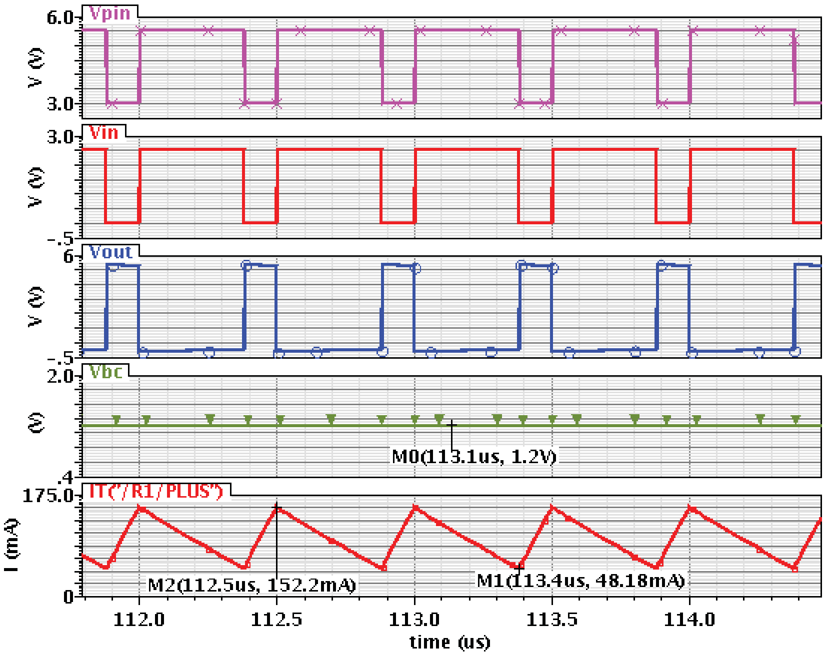


Figure 6.9: Voltage characteristics of the input signals, the outputs of the driver and the buck converter switching by *4HVDv3* with *VHdd* of 5.5 V

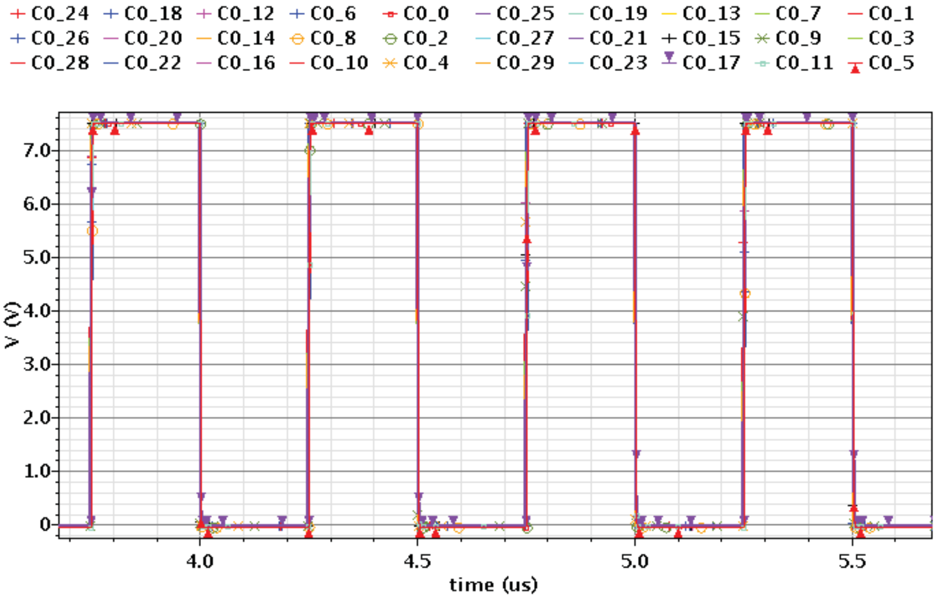
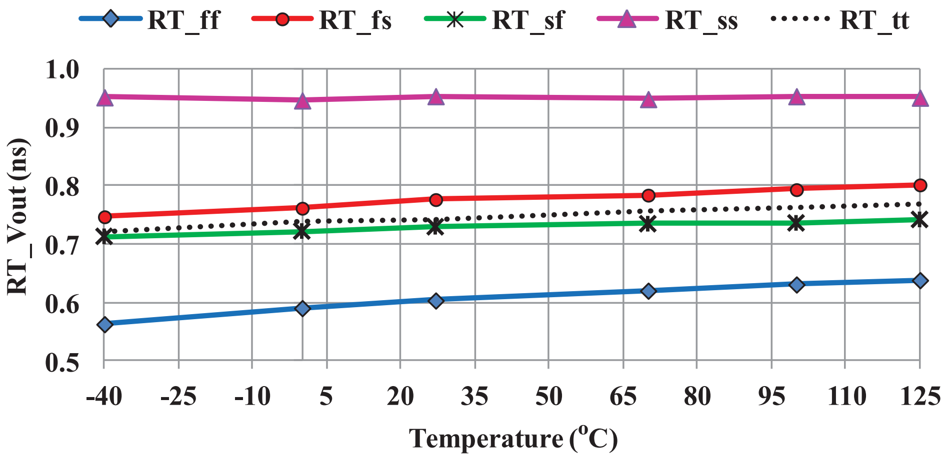


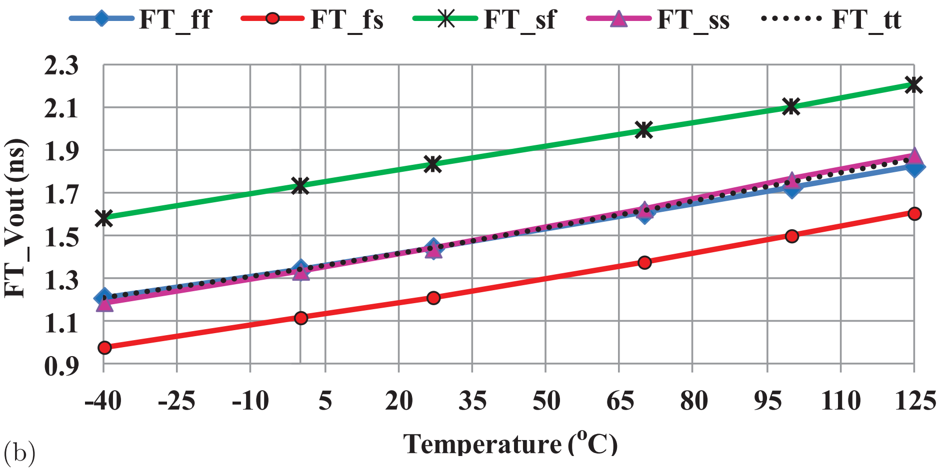
Figure 6.10: The output voltage characteristics of *4HVDv3* obtained from the corner simulation (*VHdd*=7.5 V)

The rise times (*RT*) of the output voltages are plotted in Figure 6.11a for different process variations with respect to the temperature corners. At the slow corner "*ss*", these values are higher than others, and at the fast corner "*ff*", they are the lowest.

The fall-times (*FT*) are depicted in Figure 6.11b. At the process corners "*sf*" and "*fs*", these values are, respectively the greatest and the least.



(a)



(b)

Figure 6.11: (a) Rise- (RT) and (b) fall- (FT) times of the output voltage obtained from the corner simulation

6.1.2.3 Comparison with HV-Driver 3HVDv1

The major advantages of this design can be summarised as follows:

1. the gate-controlling circuit is supplied by the same high voltage $VHdd$, which is also applied for the main stage of the HV-driver
2. no passive elements are required
3. due to the self-biasing method, no reference voltages are required, which;
4. simplifies the circuit design and the operation of the HV-driver and, also;
5. extends the range of applied supply voltage, which is equal to 4.0 V (i.e. from 3.5 V to 7.5 V). This range is 66% wider than the range of common HV-drivers.

This circuit (*4HVDv3*) has two additional advantages when compared with the HV-driver *3HVDv1*:

- In an open-load condition and with a supply voltage of 5.5 V, the delay between the driver input and output signals of 0.8 ns is shorter than that of the HV-driver *3HVDv1*, which is about 3.0 ns. It should be mentioned that these values and other parameters, as detailed in Table 6.2, are obtained from simulation results without considering parasitic effects.

  The term $delay_1$ is defined for the delay between the falling edge of the output and the rising edge of the input signals. The delay between rising edge of *Vout* and falling edge of *Vin* and the average delay are expressed as $delay_2$ and $delay_m$, respectively.

- The other advantage is that the circuit can withstand over a greater temperature range, since the voltage difference across the terminals of each transistor is maintained within the technology limit for different temperatures between –40 °C to 125 °C and also for different process variations, whereas circuit *3HVDv1* is only suitable for a temperature between 0 °C and 70 °C and at the corner for the fast process "*ff*", overvoltages also occur between the terminals of each of some transistors of this circuit.

Table 6.2: Rise-, fall-times and delays [ns] of the HV-drivers *3HVDv1* and *4HVDv3*

Load	**4HVDv3**				**3HVDv1**			
	FT	*RT*	*delay*		*FT*	*RT*	*delay*	
			$delay_1$	$delay_2$			$delay_1$	$delay_2$
Open-load	1.53	1.71	0.91	0.69	0.84	1.36	3.89	2.2
			$delay_m$=0.80				$delay_m$=3.04	
C_L=280 pF	3.92	3.97	2.30	1.59	1.25	1.82	4.40	2.50
			$delay_m$=1.95				$delay_m$=3.45	

Despite these advantages, this HV-driver has a few drawbacks, which will be discussed hereinafter.

The pull-up (*ron_PullUp*) and pull-down (*ron_PullDown*) on-resistances of this HV-driver are plotted in Figures 6.12a and 6.12b with respect to the output voltage (*Vout*), which charge and discharge between ground and the supply voltage of 5.5 V.

During charging, the pull-up on-resistance (*ron_PullUp*) rises from 5.2 Ω to 8.4 Ω and then decreases to 1.1 Ω. In the on-state, while the output discharges from 5.5 V to ground, the on-resistance characteristic of the pull-down path increases from 2.8 Ω to 5.6 Ω, and after that reduces to 0.7 Ω. In contrast, the pull-up and pull-down on-resistances of the HV-driver *3HVDv1*, as shown in Figure 5.21b, decrease evenly from 1.2 Ω to 0.4 Ω and 0.3 Ω, respectively.

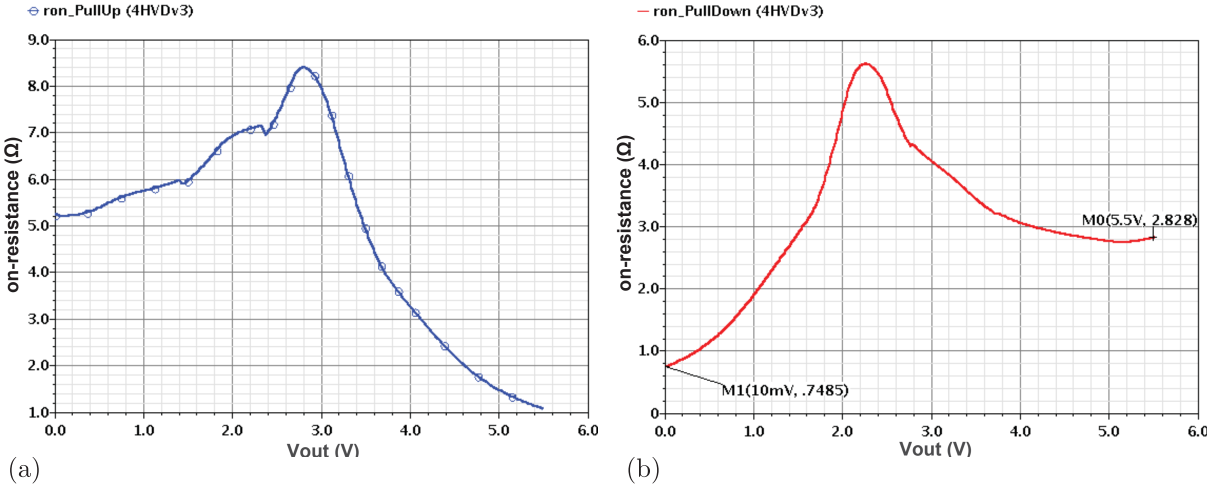


Figure 6.12: The on-resistance characteristics of the (a) pull-up and (b) pull-down path of *4HVDv3* vs. the driver output voltage (*VHdd*=5.5 V)

There are two main reasons for these higher on-resistances. The first is that the HV-driver *4HVDv3* has one more stack CMOS in comparison to the other HV-driver. The second is that the gate voltages of the stacked transistors of the HV-driver *3HVDv1* are provided by different gate-controlling circuits according to the presented theory for driving the maximum current.

However, the on-resistance of *4HVDv1* can be reduced in two ways: one is to increase the number of transistors connected in parallel in each stack, but this leads to more power consumption. The other approach is to optimise the dimensions of the pre-circuit transistors in order to maintain the gate-source voltage of each main stacked transistor at a maximum value, when the respective transistor should operate in the on-condition. The safe operating region of the transistor must also be taken into account.

A higher on-resistance has a consequence of increasing the switching times. A comparison between the rise- (RT) and fall- (FT) times of both HV-drivers are given in Table 6.2. The results are obtained from simulation results without considering parasitic effects with a supply voltage of 5.5 V.

6.2 Level Shifters

6.2.1 Low-to-High Level-Shifters

According to the levels, *Vn* and 0 V, of the input signal, which regulates the first nMOS transistor of the HV-driver pull-down path, the first pMOS transistor of the pull-up path needs to be switched with a signal containing two levels: *VHdd* and "*VHdd–Vn*", where *Vn* and *VHdd* are the nominal and the high supply voltage, respectively. This signal is provided by a high-voltage circuit defined as a level-shifter, which shifts the levels of the input signal to the required levels. This circuit is not only essential for switching the pull-up network of a HV-driver, but also for interconnecting or switching the HV sub-circuits. In the circuit design of the 3-stacked CMOS HV-driver presented in Figure 5.12, level-shifted signals are also required for controlling the switches according to the on- and off-state.

In the circuit of the HV-driver *3HVDv1*, two level-shifters *LS2* and *LS3* are designed. They have the same circuit design but different transistors' dimensions and values of reference, high and low rail voltages. Each of these consists of two stages, which are respectively based on 3-stacked CMOS. The circuit design is optimised from a level-shifter described in [30] by adding an extra stacked-CMOS (*MLS3*, *MLS4*, *MLS9* and *MLS10*) on each stage to avoid an overvoltage, as can be seen in Figure 6.13. The capacitor C_2 and transistors' widths of the circuits *LS2* and *LS3* are given in Table 6.3a. The length of each transistor is 280 nm. The corresponding supply voltage of *Inv1*, reference voltage (*Vmin*), high (*LS_VHdd*) and low rail voltages (*Vss*) are detailed as in Table 6.3b.

The described circuit in [30] is supplied with a high-voltage of twice *Vdd* (*2Vdd*). The term *Vdd* is defined as the nominal operating voltage of the used transistor. The nMOS transistors *MLS1* and *MLS2*, respectively on the left and right stage, are differentially switched by the input signal *Vin* and its inverted signal, which vary between two levels, ground and *Vdd*. The circuit has an offset of *Vdd* and shifts up the levels 0 V and *Vdd* of the input signal, respectively to *Vdd* and *2Vdd* using a capacitor C_2, which couples the gate of the pMOS transistor *MLS12* with the gate of the nMOS transistor *MLS2*. A second inverter, *Inv2*, is used between the gates of the pMOS transistors *MLS11* and *MLS12* to improve the switching speed of the level-shifter.

The level-shifters *LS2* and *LS3* have been designed based on the described circuit to switch the first pMOS of the HV-driver *3HVDv1* and also to operate the gate-control circuits $\mathrm{GC_{n2}}$, $\mathrm{GC_{n3}}$, $\mathrm{GC_{p2}}$ and $\mathrm{GC_{p3}}$. Both level-shifters have an offset voltage (*Vos*) of 2.5 V.

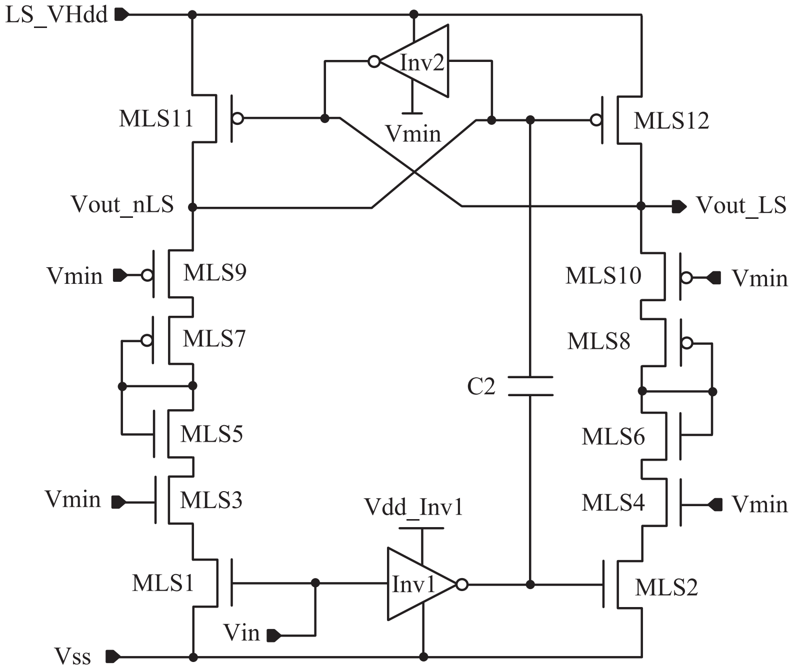


Figure 6.13: The optimised design of a level-shifter described in [30]

Table 6.3: (a) Capacitor and transistors' widths of *LS2* and *LS3*; (b) Reference, high and low rail voltages of the level-shifters

(a)

Level-shifter LS2					
MLS1–MLS12	C_2	*Inv1*		*Inv2*	
		Mn	Mp	Mn	Mp
64 μm	12.3095 pF	50 μm	100 μm	320 μm	320 μm

Level-shifter LS3						
MLS1, MLS2 *MLS5–MLS12*	*MLS3, MLS4*	C_2	*Inv1*		*Inv2*	
			Mn	Mp	Mn	Mp
1 μm	3 μm	11 pF	50 μm	100 μm	320 μm	320 μm

(b)

Voltages	**work [30]**	**LS2**	**LS3**
LS_VHdd	2×*Vn*	3.0 V	5.5 V
Vmin	*Vn*	1.5 V	3.0 V
Vdd_Inv1	*Vn*	2.5 V	4.0 V
Vss	0	0.0 V	1.5 V

In terms of the applied high supply voltage of 5.5 V and according to the theory of calculated gate voltages to drive the maximum currents, the circuit *LS2* is supplied with 4.0 V and the gates of its transistors *MLS3*, *MLS4*, *MLS9*, *MLS10* and the lower rail voltage of the second inverter *Inv2* in Figure 6.13 are set at 1.5 V (*Vmin*=4.0 V−*Vos*), whereas those of the level-shifter *LS3* are determined at 3.0 V (*Vmin*=5.5 V−*Vos*). These voltages 1.5 V (=4.0 V−*Vos*) and 3.0 V (=5.5 V−*Vos*) are termed as *minLS* and *minLS3*, respectively. As a consequence, the circuit *LS2* shifts up the levels 0 V and 2.5 V of *Vin* to 1.5 V and 4.0 V, respectively. This output signal ($Vout_{\_LS2}$) is applied as an input signal for the level-shifter *LS3*. The circuit *LS3* is supplied with *VHdd* of 5.5 V. The levels of its input signals 1.5 V and 4.0 V are shifted to 3.0 V and 5.5 V, respectively. The transient waveforms of $Vout_{LS2}$ and $Vout_{LS3}$ are plotted in Figure 6.14 according to the input pulse signal *Vin*. During the measurement process, the circuit HV-driver is applied with supply voltages lower than 5.5 V. According to the applied supply voltage (*VHdd*), the level-shifter *LS2* is supplied to a voltage equal to the expression of "5.0 V–(7.5–*VHdd*)/2"; therefore, for the supply voltages of 3.5 V, 4.0 V, 4.5 V, 5.0 V and 5.5 V, the circuit *LS2* is supplied with 3.0 V, 3.25 V, 3.50 V, 3.75 V and 4.0 V, respectively.

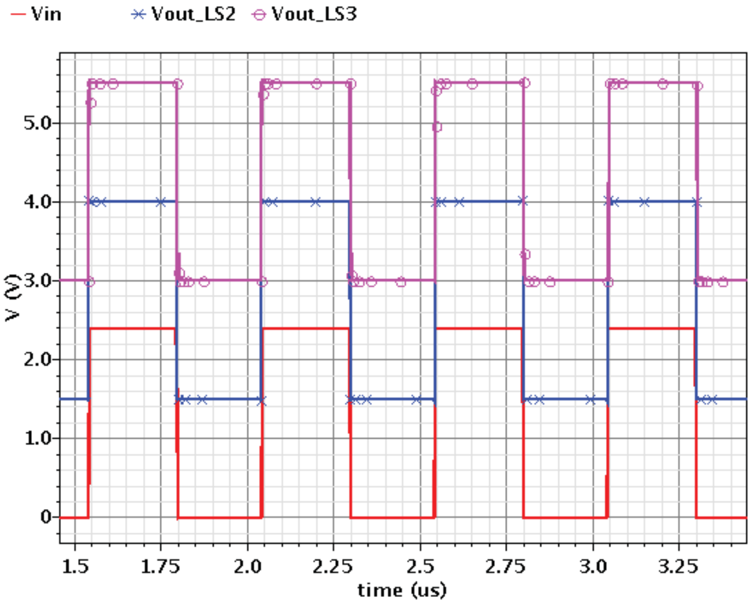


Figure 6.14: Transient voltage characteristics of the input *Vin* and the output signals of the level-shifters *LS2* and *LS3* designed for the HV-driver *3HVDv1* (VHdd=5.5 V)

6.2.1.1 Problems of Circuit Design

During the design, layout and measurement of the proposed HV-driver *3HVDv1*, three major problems of these level-shifters have been identified, which are described in the following steps:

1. Each level-shifter requires an extensive area on the chip due to the utilised capacitor C_2, as can be seen in Figures 5.13 and 5.14 showing the layout and the microphotograph of the designed HV-driver *3HVDv1*. The total area of the circuit is about 435×431 μm^2 whereas the level-shifters *LS2* and *LS3* consume an area of approx. 350×113 μm^2, which is 21% of the total circuit area.

2. The next notable problem is that, due to the inverter *Inv2* between the gates of the uppermost pMOS transistors on both stages of each level-shifter, the circuit is not suited for DC operation and can be applied only for clock operation.

   For different supply voltages, the dc output voltage characteristics of *LS2* versus the input signal *Vin* are plotted in Figure 6.15a. The level-shifter is supplied with 4.0 V, as the required value in this work, and 5.0 V. According to these supply voltages of 4.0 V and 5.0 V, the voltage V_{min}, which is the gate voltages of *MLS3*, *MLS4*, *MLS9*, *MLS10* and also the lower rail voltage of the inverter *Inv2*, as denoted in Figure 6.13, has been set at 1.5 V and 2.5 V, respectively.

   According to the supply voltages of 4.0 V and 5.0 V, it is expected that at the low range of the input signal (*Vin*), the level-shifter output voltage $Vout_{LS2}$ should be 1.5 V and 2.5 V, respectively, which is the case, and for higher values of *Vin*, it should be 4.0 V and 5.5 V. However, in contrast to these, $Vout_{LS2}$ remains constant at 1.5 V and 2.5 V, respectively. The reason is that for an input signal (*Vin*) higher than ca. 0.95 V, as shown in Figure 6.15a, the generated inverted voltage $Vout_{nLS2}$ at the drain node of *MLS11* is not low enough to switch off the inverter *Inv2*. Therefore, the output node of *Inv2* cannot be pulled up to the supply voltage of *LS2*. Consequently the output of the inverter, which is determined as the output of *LS2* ($Vout_{LS2}$), remains low.

3. The other main problem identified during measuring is that the circuit on the chip cannot operate correctly by setting the supply voltage of this level-shifter *LS2* at 4.0 V. The values of the coupler capacitor C_2 have been set at 12.3 pF and 11.0 pF, respectively for the level-shifters *LS2* and *LS3*. The simulation results in Figure 6.15b show that the level-shifter *LS2* breaks down with a load capacitor C_{L2} higher than 32.3 pF. It can be assumed that the function of the level-shifter *LS2* has a capacitive load above this value, which is caused by parasitic capacitances on the chip. Therefore, in practice, the HV-driver cannot operate when the supply voltage of *LS2* is set exactly at 4.0 V.

   In this work, this problem could be avoided by reducing the supply voltage of *LS2* from 4.0 V to 3.8 V, which indicates the level-shifter *LS2* has capacitive parasitic effects of over 50 pF at the output, as determined from simulation results.

6.2.1.2 Problem Solutions

As previously mentioned, both level-shifters *LS2* and *LS3* are not suitable for dc operation. The problem can be solved by removing the inverter *Inv2* between the gates of *MLS11* and *MLS12* [38][74].

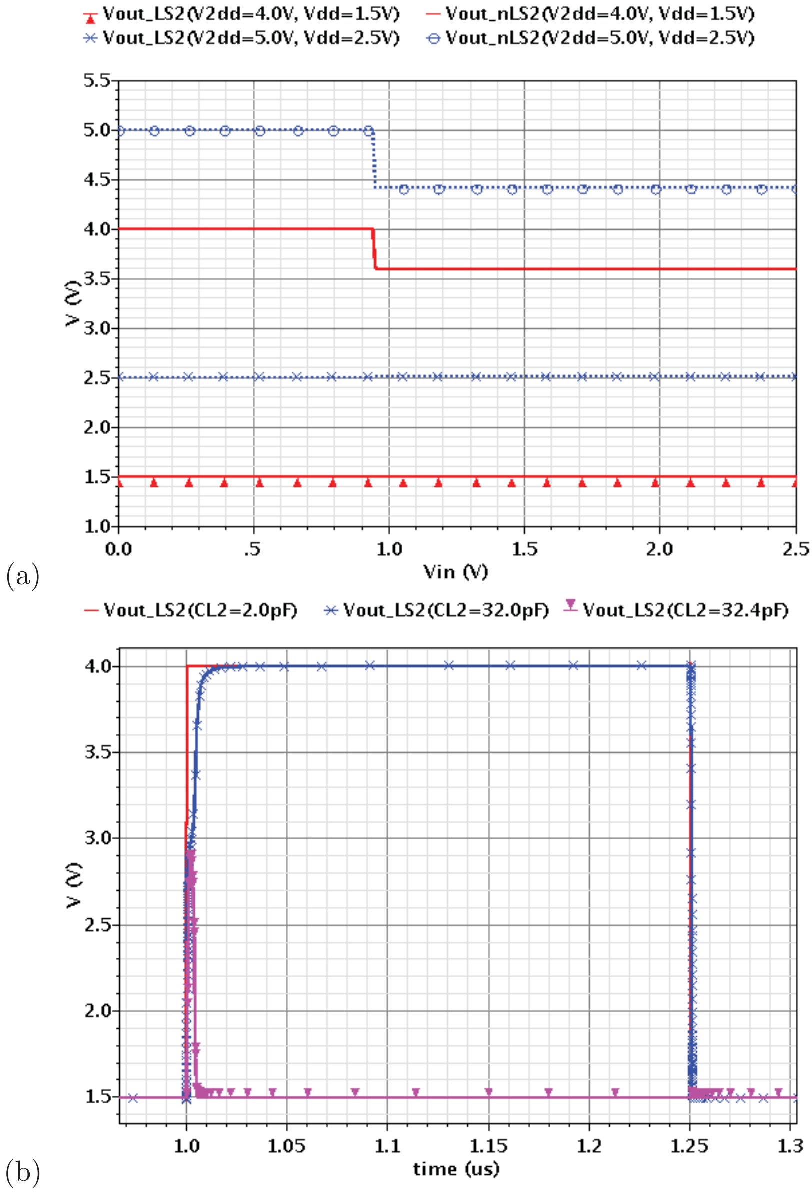


Figure 6.15: (a) DC output voltage characteristics of level-shifter *LS2* vs. the input signal *Vin*, (b) the transient output voltage of *LS2* for different load capacitors (C_{L2})

Figure 6.16 shows the dc voltage characteristics of the level-shifter's input (Vin_{LS2}), the output ($Vout_{LS2}$) and the differential output signal on the left side ($Vout_{nLS2}$) versus the input voltage (*Vin*) after removing the second inverter (*Inv2*). As can be seen, the low (0 V) and high (2.5 V) levels of Vin_{LS2} are shifted up, respectively to 1.5 V and 4.0 V ($Vout_{LS2}$).

The second problem, which relates to the level-shifter *LS2*, is that the function of the circuit breaks down for the desired supply voltage of 4.0 V. This problem can be solved in the circuit design by increasing the capacitor *C2* and also adding two inverters as buffers at the output, which has been employed at the output of the level-shifter *LS3*. The next

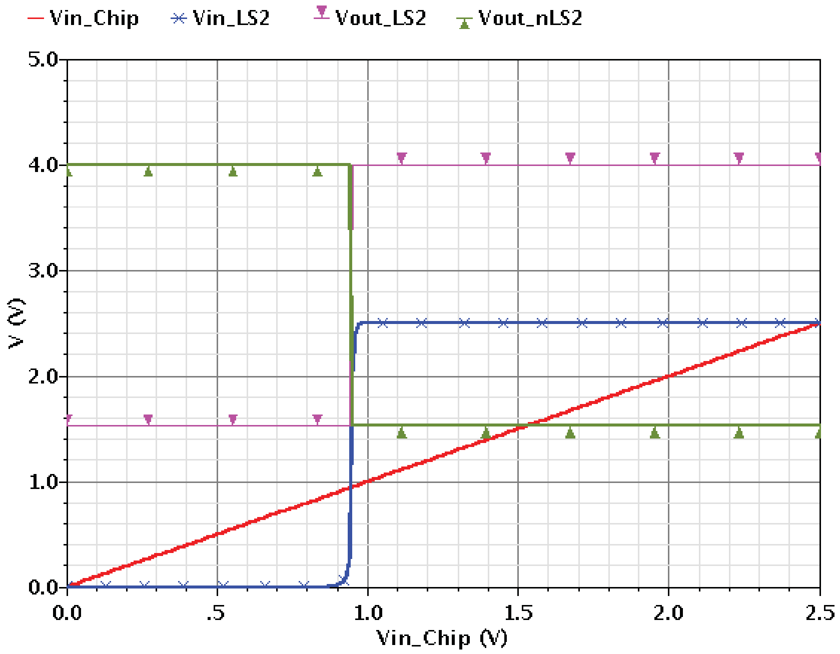


Figure 6.16: The dc voltage characteristics of the input (Vin_{LS2}), the output ($Vout_{LS2}$) and the differential output signal ($Vout_{nLS2}$) of the level-shifters *LS2* without *Inv2*

approach for reducing the problem is to design each level-shifter independently to each other.

After realising the problems of the designed level-shifters used in the circuit of *3HVDv1* and the above suggested solutions, different concepts for designing level-shifters have been published in [Pub3],[Pub4] and [Pub5]. In common with other level-shifters [30], [38], [39], [41], [42], the circuits are only suitable for a short range of different supply voltages. These circuits shift up the levels (0 V/ *Vn*) of the input signal to "*VHdd*–2.5 V" and *VHdd* respectively, where *VHdd* is here defined as the supply voltage of the level-shifter. The difference between the maximum and minimum feasible applied supply voltages is at most 2.4 V.

In view of the previously mentioned disadvantages, different concepts for designing a level-shifter have been published in [Pub3],[Pub4] and [Pub5]. The following major points are considered in the design of new high-voltage level-shifters with an extended range of applied supply voltages:

- In order to save chip area, the level-shifters are designed without capacitors such as C_2 used in the level-shifters *LS2* and *LS3* of the HV-driver *3VHDv1* since these occupy about 60% of the level-shifter's area.
- Adding extra stacked transistors and/or MOS-diodes to prevent an overvoltage between the terminals of each transistor and also to extend the range of applied supply voltages to make the circuit more flexible for different applications.

6.2.2 High-to-Low Level-Shifters

To simplify the design of HV-circuits or for interconnecting between HV- and LV-circuits, there is a requirement for pre-input stage circuits, which step down the high-voltage levels of a signal into low levels. These level-down shifters are here defined as a **H**igh to **L**ow **V**oltage **L**evel-**S**hifter with the abbreviations **HLV**-level shifter or **HLV-LS**.

In this work, three different pre-input stage circuits are designed for switching a HV-differential-amplifier [Pub7]. The circuits shift down the high-voltage input levels (up to 5.0 V) to low-voltage signals (up to 2.5 V). The circuits are compared to each other and also with the common HLV-level shifter in terms of their circuit description, drawbacks, and advantages due to the simulation results.

6.2.2.1 Common HLV-Level Shifter X

Figure 6.17 shows the inputs to a differential amplifier using resistive dividers, Rx/Ry and Rx^*/Ry^*, in each input path [46][47]. Low-voltage signals Vin_L and $Vin_L{}^*$ are provided from the high-voltage input signals Vin_H and $Vin_H{}^*$.

These resistive dividers are defined in this work as *HLV-LS X*. However, this method has a major disadvantage that the voltage divider draws a current from the input to ground.

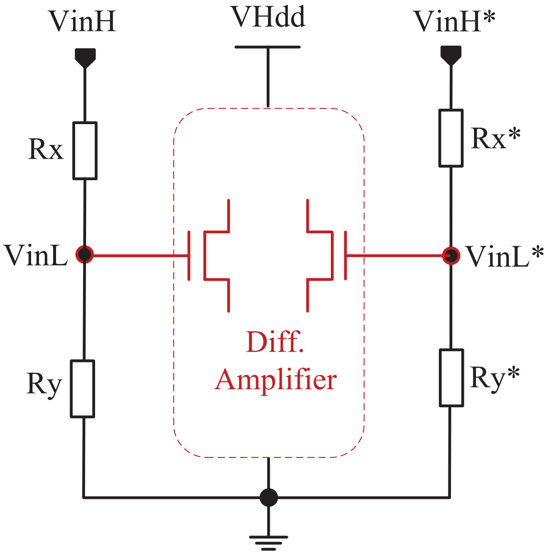


Figure 6.17: Resistive dividers defined as HLV-level shifter (*HLV-LS X*) controlling the input transistors of a HV-differential amplifier

6.2.2.2 HLV-Level Shifter A

The first design is defined as *HLV-level shifter A*, which is a common-drain stage containing an nMOS transistor *Mn* and a resistor *R*, as presented in Figure 6.18. The suffix " * " indicates the components of the pre-stage on the right side of the differential input transistor.

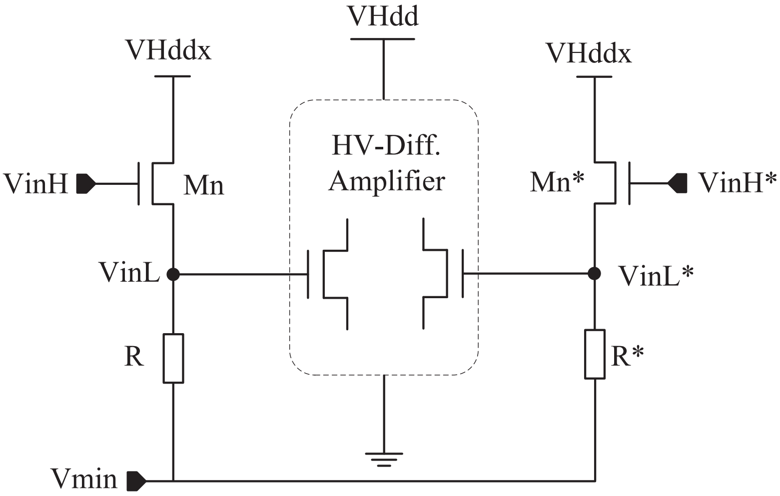


Figure 6.18: Circuit design of the *HLV-level shifter A*

The high-voltage input signal Vin_H, which can be up to 5.0 V, regulates the gate of the nMOS transistor *Mn*. The pre-stage is supplied with $VHdd_x$ of 2.5 V. When the gate-source voltage of the nMOS exceeds the threshold voltage, the node between the transistor *Mn* and the resistor starts to charge from 0 V up to 2.5 V. The disadvantage of this pre-stage is that, when the low voltage rail (V_{min}) of the stage is set at ground, a high-voltage input signal over 5.0 V cannot be applied, otherwise an overvoltage would occur between the transistor's nodes. For input signals higher than 5.0 V, only a limited range of Vin_H can be applied at the gate node of *Mn* as given in Table 6.4, whereby the low voltage rail V_{min} has to be set at the minimum value of the input signal range.

Table 6.4: The voltage range of the *HLV-Level Shifter A*

VHdd	**V_{min}**	**Vin_H**		**$VHdd_x$**	**Vin_L**	
		min.	**max.**		**min.**	**max.**
5.0 V	0.0 V	0.0 V	5.0 V	2.5 V	0.0 V	2.5 V
7.5 V	2.5 V	2.5 V	7.5 V	5.0 V	2.5 V	5.0 V
10 V	5.0 V	5.0 V	10.0 V	7.5 V	5.0 V	7.5 V
N×Vn	$VHdd–2\times Vn$	$(N–2)\times Vn$	$N\times Vn$	$(N–1)\times Vn$	$(N–2)\times Vn$	$(N–1)\times Vn$

6.2.2.3 HLV-Level Shifter B

Figure 6.19 shows the second HLV-level shifter defined as *HLV-LS B*, which is based on the previous pre-stage circuit (*HLV-LS A*). To avoid an overvoltage, two extra nMOS transistors *Mn0* and *Mn1* are added in series between the input transistor *Mn2* and the supply voltage rail of *VHdd*. The high input signal Vin_H is applied to the input of the source-follower formed by *Mn0*, *Mn1* and *Mn2*. The required low-voltage signal Vin_L is provided from the source potential of the source follower by the resistive divider *Rx*, *Ry* and *Rz*.

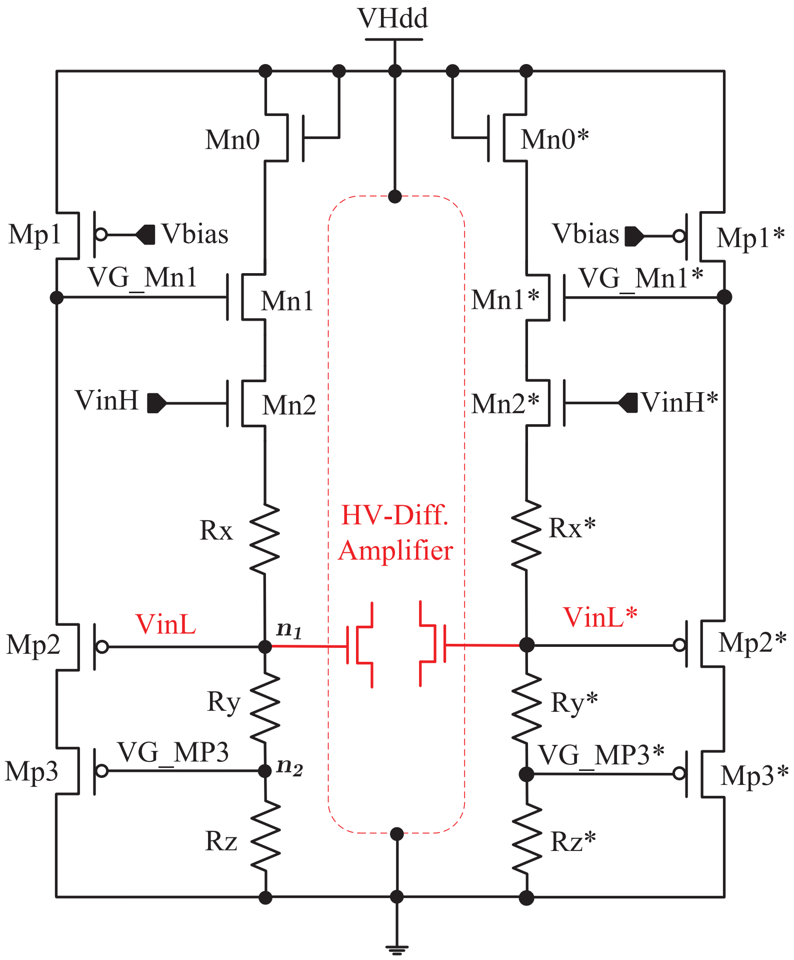


Figure 6.19: Circuit design of the *HLV-level shifter B*

A second stage containing series-connected pMOS transistors *Mp1*, *Mp2* and *Mp3* is designed with the same supply voltage *VHdd* of 5.0 V to control the transistor *Mn1* in the safe operating area. The gates of *Mp2* and *Mp3* are connected to the nodes of the first stage, n_1 and n_2, which is divided by the resistors *Rx*, *Ry* and *Rz*.

The gate of *Mp1* is biased by a reference voltage of 2.5 V to maintain the gate-source voltage of *Mp2* in the range of 2.5 V, as can be described as follows:

$$I_{Mp1} = \frac{\beta}{2}(|VGS_{Mp1}| - |V_{thp}|)^2 = I_{Mp2} \tag{6.1}$$

$$VGS_{Mp1} = 2.5\,V \approx VGS_{Mp2} = VG_{Mn1} - Vin_L \tag{6.2}$$

where I_{Mp}, VG_{Mn}, VGS_{Mp} and VGS_{Mn} express respectively the current, gate voltage and gate-source voltage of the respective transistor (*Mp1*, *Mp2* or *Mn1*), and V_{thp} is the threshold voltage of the pMOS transistors.

Therefore, the voltage of the gate *Mp2* (Vin_L), which varies between 0 V and 2.5 V, is shifted up about 2.5 V, at the gate of *Mn1* (VG_{Mn1}), as can be seen in Figure 6.20, where the term Vin_{L_B} is defined for the required low-voltage signal (Vin_{L_B}) provided by the circuit *HLV-LS B*.

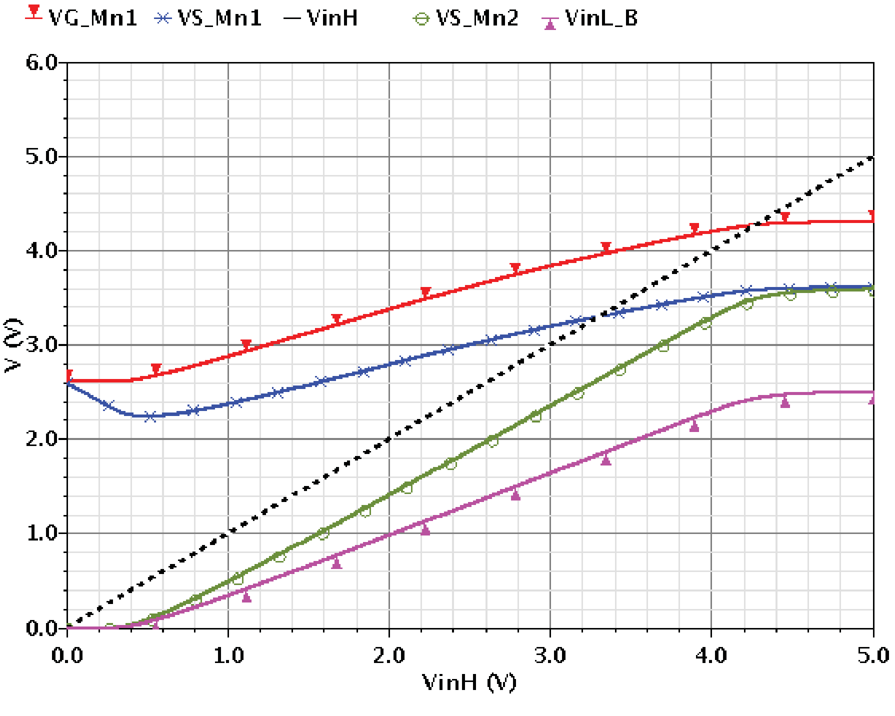
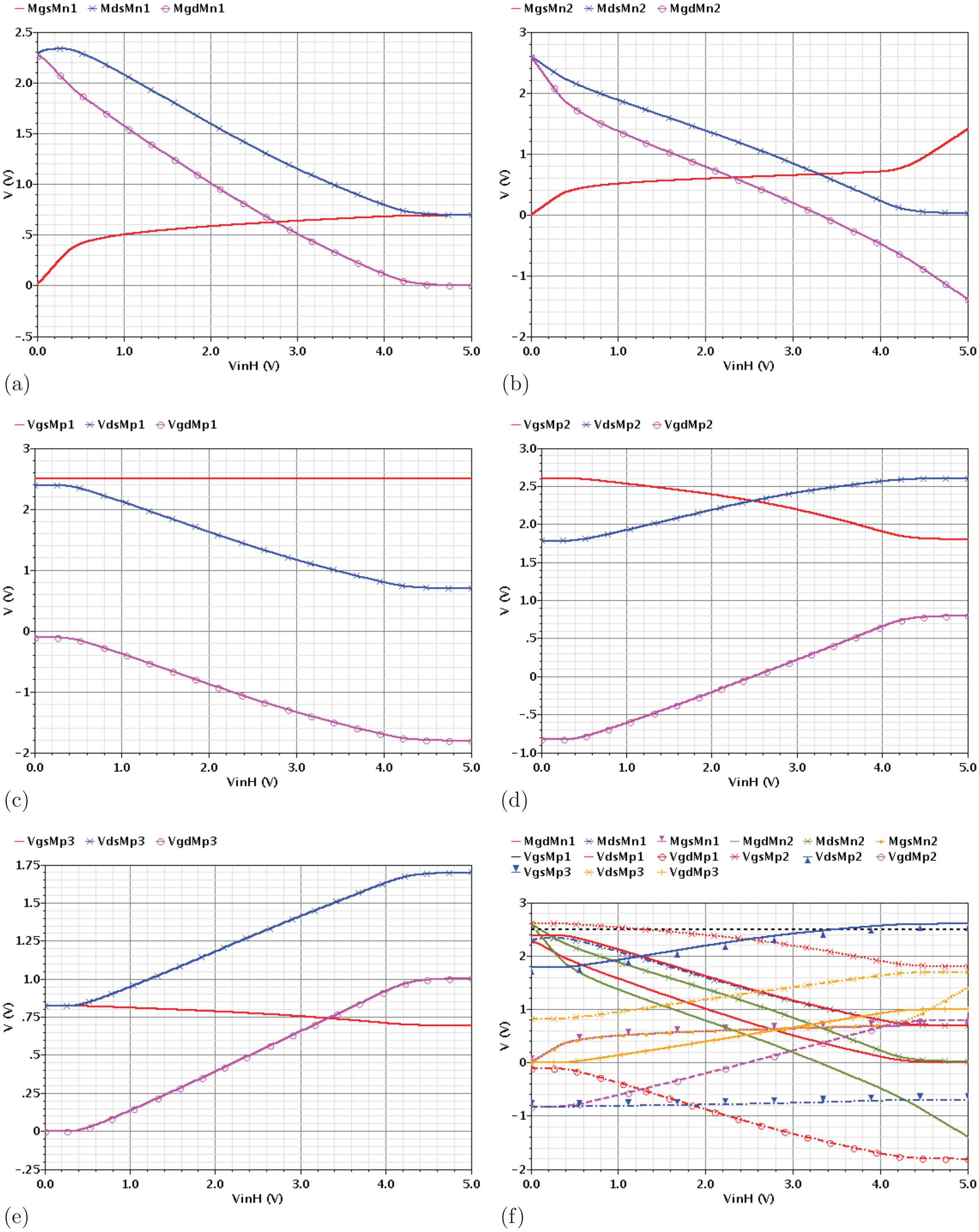


Figure 6.20: The dc characteristics of the output signal (Vin_{L_B}), gate and source voltages of *Mn1* and *Mn2* of the *HLV-LS B*

For a higher input voltage being equal to "$N \times Vn$", "***N*–1**" nMOS transistors are needed to be connected in series between the input nMOS transistor *Mn2* and the high supply voltage rail. To avoid an overvoltage, a gate-drain connected MOS transistor such as *Mn0* in Figure 6.19 should be also added between the group of the "*N*–1" nMOS transistors and the supply voltage rail.

With respect to the high-voltage input signal Vin_H, the simulation results in Figures 6.21a–f show that the voltage between the terminals of each transistor for *HLV-level shifter B* is within the technology limit with 5% tolerance.



(a) (b) (c) (d) (e) (f)

Figure 6.21: Voltage difference across terminals of (a) *Mn1*, (b) *Mn2*, (c) *Mp1*, (d) *Mp2*, (e) *Mp3* and (f) all voltage differences in a view (*HLV-LS B*)

6.2.2.4 HLV-Level Shifter C

The weakness of the circuit HLV-LS B is the required matching between resistors and threshold voltage of transistors. Therefore, an optimised circuit is designed using two series-connected nMOS transistors *Mn4* and *Mn3*, instead of the resistors, as can be seen in Figure 6.22. The circuit is defined as *HLV-level shifter C*.

The provided voltage at the node between both transistors (*Mn3* and *Mn4*) is not low enough to drive the pMOS transistor *Mp3* of the second stage. Therefore, the third stage containing two series-connected nMOS transistors (*Mn5* and *Mn6*) forming a current mirror with *Mn4* and the gate-drain connected *Mn3*, is added to the circuit. According to the high-voltage input signal, the voltage provided at the node between the transistors *Mn5* and *Mn6* can regulate the transistor *Mp3* of the second stage.

The simulation results in Figure 6.23 shows that the voltage between the terminals of each transistor is within the technology limit with 5% tolerance.

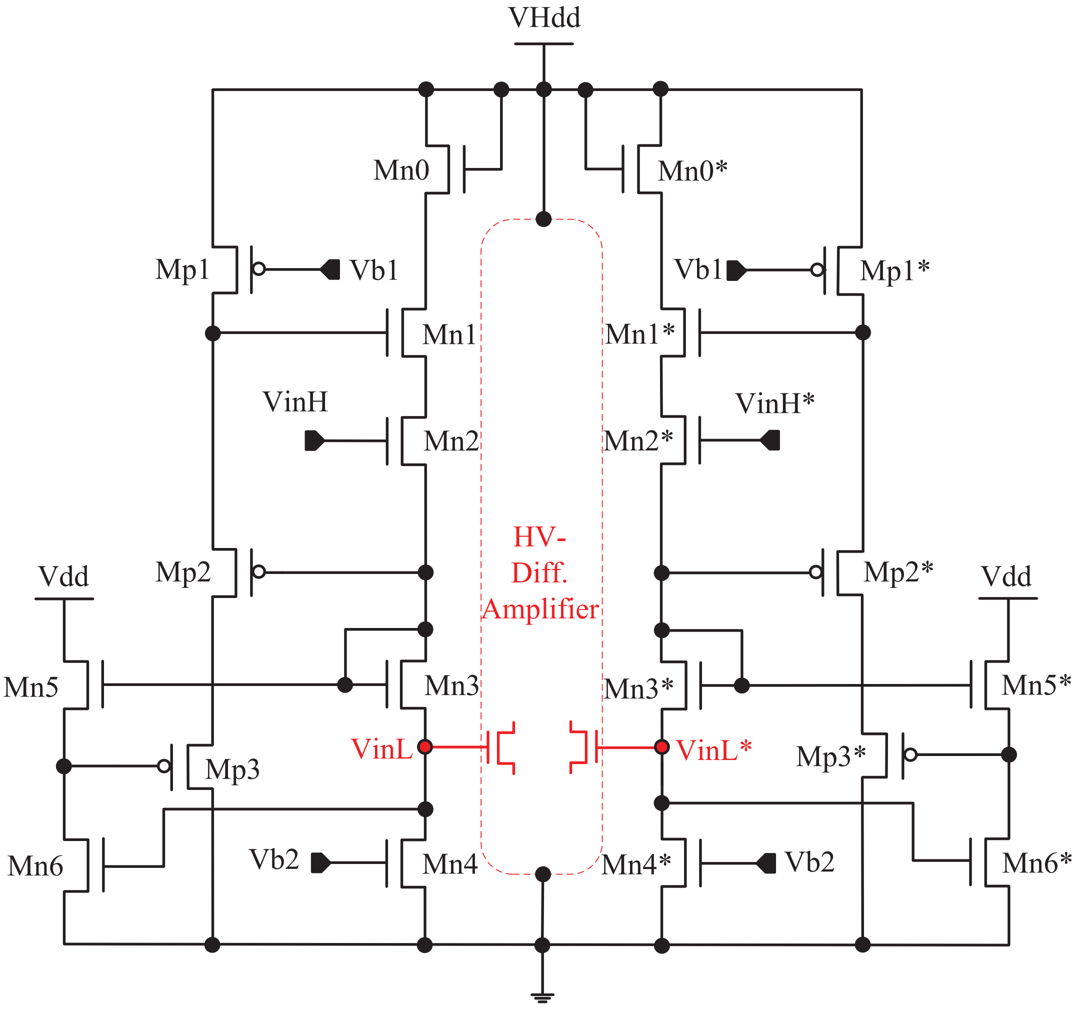


Figure 6.22: Circuit design of the *HLV-level shifter C*

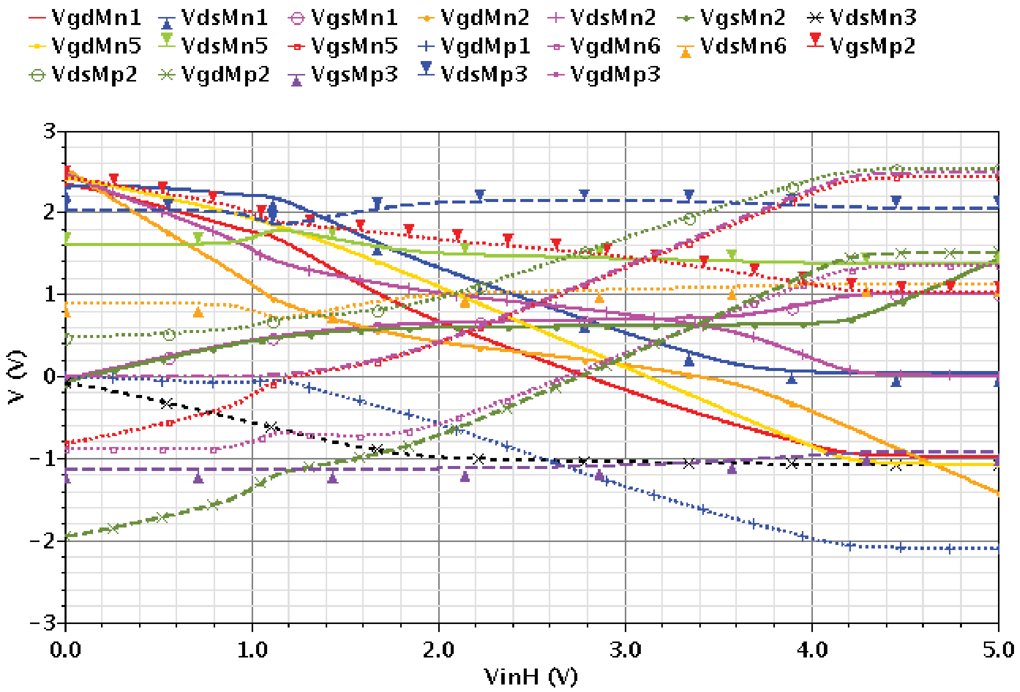


Figure 6.23: Voltage difference across terminals of each transistor of *HLV-LS C* versus the input signal Vin_H

In the next section, the voltage difference across terminals of each transistor of *HLV-LS B* and *HLV-LS C* is proved and the output voltages of the designed circuits are compared to each other.

6.2.2.5 Simulation Results and Comparison

According to the HV-input signal Vin_H, which is a square-wave with levels 0 V and 5.0 V, the transient output voltage characteristics (Vin_L) of the *HLV-level shifters X*, *A*, *B* and *C* with levels 0 V and ca. 2.5 V are demonstrated in Figure 6.24.

Table 6.5 gives a comparison between delays, rise (RT) and fall (FT) times of the output voltages Vin_L of the presented *HLV-level shifters X*, *A*, *B* and *C*. The simulation results are obtained for the application regulating the input transistors of a high-voltage differential amplifier [Pub7]. With *HLV-LS C*, the output voltage Vin_L has the lowest delay and fall time and a satisfied rise time in comparison to the other level shifters. The major advantage of the designed *HLV-LSs* (*A*, *B* and *C*) is that the input signal dissipates no current; however, the level-shifter *HLV-LS C* is the most favourable due to the circuit design without the need for resistors. Figure 6.25 displays a comparison between the dc output voltage characteristics of the HLV-level-shifters. The output signal of *HLV-LS B* has a wider linear output range when compared with circuits *A* and *C*. However, *HLV-LS B* and *HLV-LS C* should be optimised to approach the ideal operation of *HLV-LS X*.

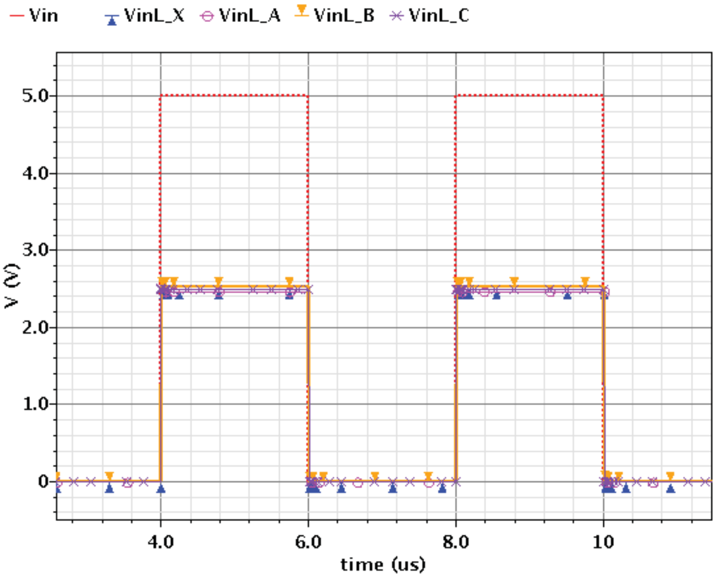


Figure 6.24: Transient input and output voltages of the *HLV-level shifters* X, A, B and C

Table 6.5: Comparison results between the rise- (RT), fall times (FT) and delays of the output signals of the *HLV-level shifters* X, A, B and C

HLV-LS	**RT ([ns]**	**FT [ns]**	**delay [ns]**
X	6.50	5.70	1.90
A	0.07	2.12	4.70
B	2.96	5.96	1.20
C	0.33	0.48	0.12

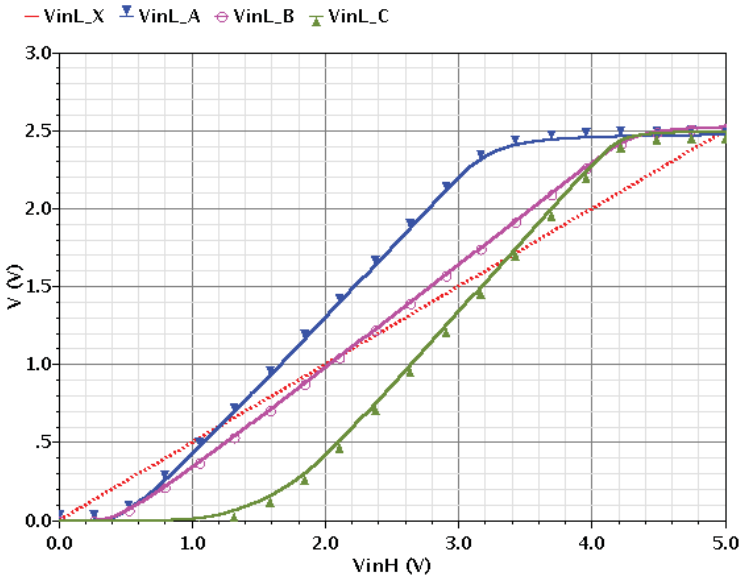


Figure 6.25: The dc output voltage characteristics of the *HLV-level shifters* X, A, B and C versus the high-voltage input signal Vin_H

Transistor dimensions and resistor values of the designed pre-stage circuits (*A*, *B* and *C*) regulating the proposed differential amplifier are given in Table 6.6. However, for other applications, these parameters may need to be adjusted.

Table 6.6: Transistor dimensions width/ length [μm/μm] and resistor values [kΩ] of the designed *HLV-LSs A*, *B* and *C*

HLV-LS A	
Mn	*R*
1/0.280	80

HLV-LS B					
Mn0, Mn1, Mn2	*Mp1, Mp2*	*Mp3*	*Rx*	*Ry*	*Rz*
1/0.280	1/0.280	20/0.280	80	110	74

HLV-LS C						
Mn0	*Mn1*	*Mn2*	*Mn3*	*Mn4, Mn5, Mn6, Mp1*	*Mp2*	*Mp3*
0.4/0.500	3.4/0.280	8/0.280	0.4/0.280	0.4/0.280	1/0.280	9/0.500

Since the presented HLV-level shifters are designed based on stacked standard transistors, the circuits are technology-independent and can be implemented on every technology.

Chapter 7

Discussion and Conclusion

The aim of this work is to design an N-stack CMOS HV-driver with a minimum on-resistance for the fastest possible switching. To achieve this goal, firstly, the required gate voltage of each stacked CMOS transistor is calculated using the computer algebra system "**MAXIMA**" to drive the maximum current into the drivers' active path and obtain an equal voltage drop across each transistor in the inactive path. In both conditions, the voltage difference across the terminals of each transistor is maintained within the technology limited range. Driving the maximum current indicates that the driver path has a minimum on-resistance.

The calculation is accomplished for two different groups of supply voltages, divisible and indivisible by the nominal voltage of the standard transistors involved in the circuit design. The results are presented as a theory in mathematical formulae yielding the gate voltages of N-stacked CMOS transistors for various supply voltages. Based on these results, a circuit design methodology to generate the respective gate voltages is introduced. In pursuance of the theory and circuit methodology, a 2- and a 3-stacked CMOS HV-driver were designed for the maximum allowed supply voltages of 5.0 V and 7.5 V, respectively in *TSMC* 65-nm technology using I/O-transistors with a nominal voltage of 2.5 V.

Due to DC and transient simulation results, it has been shown that the provided gate voltages track approximately the ideal values with slight deviations for various supply voltages. The main reasons for these inaccuracies are listed as follows, and are discussed in detail in this work:

- unequal transistor threshold voltages
- separately entering the main stacked transistors into the operational regions
- operating the transistors of the gate-controlling circuits not only in saturation but also in the cut-off, sub-threshold and/or linear regions.

- variable low and high rail voltages of the designed gate-controlling circuits
- setting unequal transistor widths for gate-controlling circuits to avoid an overvoltage
- the additional transistors and capacitors

The accuracy can be improved by optimising the respective switches to provide steady constant low- and high rail voltages according to the on- and off-states and also by designing gate-controlling circuits individually for an HV-driver supplied with a fixed voltage.

To prove that the maximum currents flow in the driver's pull-up and pull-down paths, the reference, high and low supply rail voltages of the controlled circuits, which provide gate voltages for the 2-stacked CMOS HV-driver, are changed from the ideal determined values. The simulation results show that the provided gate voltages are affected and as a result the currents are decreased. Consequently, the respective on-resistances are reduced.

Furthermore, the designed circuits of this work (A) are compared with the published work (B) described in [31]. The dimensions of the stacked CMOS transistors of the work B are set identically to those of A. The simulation results show, in the case that the supply voltages for the 2- and 3-stacked CMOS HV-drivers are 5.0 V and 7.5 V, respectively, the pull-down on-resistance of the driver A is improved by app. 36%, and the pull-up on-resistance by 40% and 46%, respectively, when compared to the HV-driver B. For lower supply voltages, the improvement of the pull-up on-resistance of A is significantly increased, since the pull-up on-resistance of B is worsened due to the constant gate voltage of the second pMOS transistor.

The next goal of this work is to optimise the designed 3-stacked CMOS HV-driver for switching a buck converter.

A HV-circuit defined as *3HVDv1* is realised in an area of $0.187\,\text{mm}^2$ and implemented on a chip with a size of 2mm×2mm. Two different technologies of packaging are used: chip-in-package (CIP) and chip-on-board (COB). The performance of both chips are verified for various high supply voltages (*VHdd*) in the range from 2.7 V to 5.5 V. At the output node, a rectangular signal with levels of ca. 0 V and *VHdd* is generated, which indicates charging and discharging of the output load between the ground and the supply voltage. This shows the correct operation of the circuit and that the pull-up and pull-down transistors switch on time according to the on- and off-states. However, overvoltages occur as positive and negative peaks on the output waveform, and these are measured and compared for different chips according to various output loads and supply voltages. With respect to the discussion in Chapter 5, it has been shown that the bond wires and lead fingers of a package have parasitic effects. The simulation results confirm that these effects cause overvoltages on the output voltage. It should be noted, that the interconnecting wires and contactors on chips and PCBs also have parasitic effects which negatively impact on the circuit's performance.

Furthermore, these peaks would increase on connection to the inductor of a buck converter used in this work; therefore, the circuit on the chip can be broken down. For reducing the output overvoltages, three methods have been used:

1. Connecting a capacitor across the chip output node and ground
2. Adding a resistor connected in parallel to a Schottky diode on the PCB between the chip output node and ground. This overvoltage protection is defined as OVP in this work.
3. Using the technology COB with and without two OVPs. The first is set as described above and the second is connected between the chip output node and the supply rail.

To prove the correctness of the circuit's functionality and also to compare the different methods of switching the buck converter, various measurements have been accomplished for different supply voltages and duty-cycles.

The measurement shows the chips-on-board have smaller overvoltages in the open-load condition, when compared with the chips-in-packages. By switching the buck converter, the negative output overvoltages COB and CIP using OVP are significantly lower than other chips without this overvoltage protection. Additionally, they have a lower switching loss because of the smaller rise and fall times. With increasing the supply voltage from 3.6 V to 5.5 V, the measurement results show the chips using OVP have about 8%–10% higher efficiencies in comparison to those of other chips. However, during the design and measurement of this circuit, the following major problems were identified:

- Regarding the ideal layout of the RF transistors, completion of the layout of the basic transistors used in the circuit *3HVDv1* was attempted by connecting the drain and source nodes respectively together, when the finger of a transistor was greater than one. Furthermore, to build a deep n-well (DNW) nMOS transistor, a DNW layer is integrated into a basic nMOS transistor and additionally an n-well layer is placed around the structure as a sidewall. In terms of connecting the DNW-terminal to the deep n-well layer, conductors are set on this n-well layer.
- The dimensions of the surface of each transistor's terminals were set approximately according to the currents flowing through these terminals; however, the deep n-wells could not be constructed as precisely they should have been because of the lack of

DNW layer and parasitic diodes between this and besides layers in the model of the nMOS transistor; therefore, the current flowing through this node cannot be simulated in the schematic of the circuit. The estimated equivalent circuit model, which is designed according to the measurement results of a DNW nMOS transistor also implemented on the chip, was not precise and suited enough to design the circuit *3HVDv1*. As a result, the implemented circuit on the chip could not be precisely simulated as required.

- By measuring the DNW transistor implemented on the chip, it has been identified that the dimensions of the DNW layer, n-well ring and the distance between these and surrounding layers have not being met satisfactorily.
- For reducing the circuit area, the number of transistors used in each stack of the gate-controlling circuits was decreased, which meant that the provided gate voltages could not track exactly the ideal values.
- The designed circuit on the chip is suitable only for supply voltages up to 5.5 V but not higher, because to save extra pads, four reference voltages are provided by a voltage divider and cannot be set for higher voltages as required.
- Since for both on- and off-states, the gate-controlling circuits require different high- and low-rail voltages and also reference voltages for regulating the transistors of the gate-controlling circuits, the entire circuit demands more pads than are available on the chip. Therefore, some voltages close to each other are considered as one value, but this increases the inaccuracy of the provided gate voltages compared to the ideal values.
- As shown in this work, bonding wires, packaging, interconnecting wires, conductors etc. negatively impact on the circuit performance, especially causing the appearance of high peaks on the output voltage. The common HV-drivers are based on N-stacked CMOS. The number N depends on *VHdd*, which is N times greater than the nominal voltage. Because of this, the voltage between terminals of each transistor is exactly on the limit. Due to parasitic effects, maintaining the transistors in their safe operation area cannot be obtained with 100% satisfaction. To reduce the overvoltage, it is helpful to use capacitors, but they lead to longer charging times and discharging. As a result, the switching time of the HV-driver would increase. Therefore, biasing of "*N+1*" stacked CMOS is a more effective method to avoid overvoltages.
- Two level-shifters used in this circuit are optimised from the level-shifter described in [30]. Both level-shifters require an extensive area on the chip due to the utilised

capacitors. They consume an area of approx. $350{\times}113\,\mu\text{m}^2$, which is 21% of the total circuit area.

- Because of the circuit design of the level-shifters, the *3HVDv1* circuit is not suited for DC operation and can be operated only dynamically.

In view of the drawbacks identified during the design, implementation, simulation and measurement, the following concepts of HV-circuits were presented in addition to the main goals of this work:

- Two HV-drivers with different circuit design methodologies
- Three low- to high-voltage level-shifters published in [Pub3],[Pub4] and [Pub5]
- Three high- to low-voltage level-shifters

For the improved HV-drivers, which are defined as *3HVDv2* and *4HVDv3*, a method is described to control the gate of the main stacked transistors, which simplifies the circuit design. The HV-drivers are optimised for arbitrary supply voltages from 2.6 V/3.5 V to 6.0 V/7.5 V. According to the on- and off-states, the regulation of the stacked main transistors of *4HVDv3* is achieved by using a self-biasing method. Therefore, no reference voltages are required. The circuit is stable for temperatures between –40 °C and 125 °C.

In this work, three pre-circuits are designed to reduce the levels of a high-input signal up to 5.0 V to lower levels between 0 V and 2.5 V. The circuits are defined as high-to-low level-shifters *HLV-LS A*, *HLV-LS B* and *HLV-LS C*. The major advantage of these circuits is that the input signal dissipates no current. The *HLV-LS C* is the most favourable due to the circuit design without the need for resistors; however, it should be optimised to achieve a wider linear output range.

The major advance of the circuits designed in this work is that they are technology-independent and compatible with scaled CMOS devices.

Publications

- 2016

[Pub1] S. Pashmineh; S. Bramburger and D. Killat, “Design of a High-Voltage Rail-to-Rail Error Amplifier based on Standard CMOS used in an LDO”, *29th EEE Canadian Conference on Electrical and Computer Engineering* (*CCECE 2016*), Vancouver, IEEE, May 2016

[Pub2] S. Pashmineh and D. Killat, “A High-Voltage Driver Based on Stacked Low-Voltage Transistors with Minimized On-Resistance for a Buck Converter in 65 nm CMOS”, *29th EEE Canadian Conference on Electrical and Computer Engineering* (*CCECE 2016*), Vancouver, IEEE, May 2016

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[Pub3] S. Pashmineh and D. Killat, “Design of a High-Voltage Driver Based on Low-Voltage CMOS with an Adapted Level Shifter Optimized for a Wide Range of Supply Voltage”, *IEEE 22nd International Conference on Electronics, Circuits, and Systems* (*ICECS 2015*), Cairo, IEEE, Dec. 2015, pp. 5–8

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