# **Extraction of Transmission Line Parameters and Effect of Conductive Substrates on their Characteristics**

Saurabh Chaturvedi, Mladen Božanić, Saurabh Sinha

Department of Electrical and Electronic Engineering Science
Faculty of Engineering and the Built Environment
University of Johannesburg, Auckland Park Kingsway Campus
Johannesburg, South Africa

E-mail: chaturvedi.s.in@ieee.org, mbozanic@ieee.org, ssinha@uj.ac.za

**Abstract.** The paper presents the effect of conductive or lossy silicon (Si) substrates on the frequency-dependent distributed series impedance transmission line (TL) parameters,  $R(\omega)$  and  $L(\omega)$ . The frequency variations of these parameters of the microstrip line for four different conductivities of Si substrate are observed and compared. Keysight Technologies (formerly Agilent's Electronic Measurement Group) Advanced Design System is used for the electromagnetic simulations of the microstrip line structures. Scattering parameters (S-parameters) based equations are used to plot the variations of series impedance parameters as a function of frequency. Furthermore, this paper explains a complete method to extract various parameters related to a TL. The work extracts the parameters of a microstrip TL model provided with the GlobalFoundries 0.13  $\mu$ m SiGe BiCMOS8HP process design kit up to 100 GHz.

**Keywords:** Conductive substrate, microstrip line, transmission line (TL) model, *S*-parameters, skin effect, SiGe BiCMOS, process design kit (PDK).

#### 1. Introduction

With the extensive scaling of metal oxide semiconductor (MOS) transistors, complementary MOS (CMOS) process technology has had the advantage of the integration of digital, analog, and multi-gigahertz (GHz) radio frequency (RF) modules to implement a system on chip (SOC). However, owing to the low resistivity of silicon (Si) substrate, the on-chip passive components show low quality factors (*Q*-factors) in CMOS technology. The performance of RF circuits is mainly limited by the low quality on-chip passives in typical CMOS technology [1], [2].

With the increase in operating frequency, the electrical property of onchip interconnects has emerged as a dominating factor in the overall performance of Si based RF integrated circuits (ICs). In recent years, much research has been done to learn the frequency-dependent behavior of on-chip interconnects and passive elements fabricated on lossy Si substrates [3], [4]. The transmission characteristics of interconnects on lossy substrates have been presented by a full-wave electromagnetic (EM) approach [5], [6] and quasi-static EM methods [7] with equivalent circuit modeling [8], [9]. The closed-form formulae to determine the frequency dependence of distributed parameters of IC interconnects on conductive Si substrates are reported in [3], [4].

This paper compares EM simulation results using the Keysight Technologies Advanced Design System (ADS) for the variations of frequency-dependent impedance parameters of the microstrip interconnect for four Si substrate conductivities, including  $10^4$ ,  $10^3$ ,  $10^2$ , and 10 S/m. The paper also discusses a generic equation based method to extract various parameters associated with a transmission line (TL). The parameters of a microstrip TL model available with the GlobalFoundries 0.13  $\mu$ m SiGe BiCMOS8HP process design kit (PDK) are extracted up to 100 GHz.

The paper is organized as follows: Section 2 depicts the structure of a microstrip line on a lossy Si substrate and lists the specifications of parameters. This section also presents the distributed *RLGC* TL model, scattering parameters (*S*-parameters) based equations, and the EM simulation setup. Section 3 explores a method to extract the TL parameters and exhibits the circuit schematic for EM simulations. The simulation results are demonstrated and discussed in Section 4, and Section 5 concludes this paper.

#### 2. On-Chip Interconnect

#### 2.1. Structure Specifications

The structure of a microstrip-type on-chip interconnect on a lossy Si substrate is shown in Fig. 1. A microstrip line is the most common TL used in planar circuits at high frequencies. The cross-section consists of a substrate between a conductor and a ground plane.

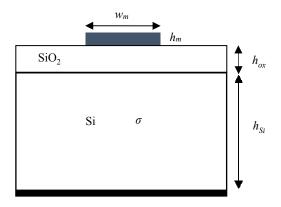


Fig. 1. Microstrip line on a lossy Si substrate.

The specifications of parameters of the on-chip interconnect structure of Fig. 1 are tabulated in Table 1.

**Table 1.** List of parameters

Parameter	Value
Substrate (Si) thickness, $h_{Si}$	450 μm
Substrate dielectric constant	11.9
Oxide (SiO <sub>2</sub> ) thickness, $h_{ox}$	2.5 μm
Oxide dielectric constant	3.9
Metal thickness, $h_m$	1 μm
Metal width, $w_m$	5 μm
Metal length, $l_m$	1 mm
Substrate conductivity, $\sigma$	$10^4$ , $10^3$ , $10^2$ , $10$ S/m
Metal conductivity, $\sigma_m$	$5.99 \times 10^7  \text{S/m}$

#### 2.2. Distributed RLGC Model

Fig. 2 illustrates an RLGC section of a distributed TL. A TL can be partitioned into many similar RLGC sections using the Telegrapher's equations. The parameters  $R(\omega)$ ,  $L(\omega)$ ,  $G(\omega)$ , and  $C(\omega)$  are the frequency-dependent distributed line resistance, inductance, conductance, and capacitance per unit length (PUL), respectively. The length of the section is dx. The series impedance interconnect parameters are  $R(\omega)$  and  $L(\omega)$ , while the shunt admittance parameters are  $G(\omega)$  and  $C(\omega)$ .

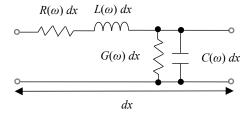


Fig. 2. Distributed *RLGC* section.

The characteristic impedance  $Z_c$  and the propagation constant  $\gamma$  are associated with these frequency-dependent line parameters [10]. The relations are given by (1) and (2), respectively.

$$Z_{c} = \sqrt{\frac{R(\omega) + j\omega L(\omega)}{G(\omega) + j\omega C(\omega)}}$$
(1)

$$\gamma = \sqrt{[R(\omega) + j\omega L(\omega)][G(\omega) + j\omega C(\omega)]}$$
 (2)

The expressions of  $Z_c$  and  $\gamma$  are represented in terms of the S-parameters [10] as:

$$Z_c = \sqrt{Z_0^2 \frac{(1+S_{11})^2 - S_{21}^2}{(1-S_{11})^2 - S_{21}^2}}$$
 (3)

$$e^{-\gamma l} = \left\{ \frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}} \pm K \right\}^{-1} \tag{4}$$

where

$$K = \sqrt{\frac{(S_{11}^2 - S_{21}^2 + 1)^2 - (2S_{11})^2}{(2S_{21})^2}} \,. \tag{5}$$

The distributed parameters of a TL are determined by using (6)-(9) [10]:

$$R(\omega) = \operatorname{Re}(\gamma Z_c) \tag{6}$$

$$L(\omega) = \frac{\operatorname{Im}(\gamma Z_c)}{\omega} \tag{7}$$

and

$$G(\omega) = \text{Re}\left(\frac{\gamma}{Z_c}\right) \tag{8}$$

$$C(\omega) = \frac{\operatorname{Im}\left(\frac{\gamma}{Z_c}\right)}{\omega}.$$
 (9)

#### 2.3. Simulation Setup

The layouts of microstrip interconnect structures for different conductivities ( $10^4$ ,  $10^3$ ,  $10^2$ , and 10 S/m) of Si substrate are drawn in the ADS layout editor, and the S-parameters based EM simulations are performed using Momentum simulator. Fig. 3 shows the layout of the microstrip line structure. The schematic representation of this structure is demonstrated in Fig. 4. The structures are simulated for the frequency range of 0.1 GHz to 20 GHz [11]. The variations of distributed impedance parameters  $R(\omega)$  and  $L(\omega)$  as a function of frequency are plotted in ADS by using (3)-(7).

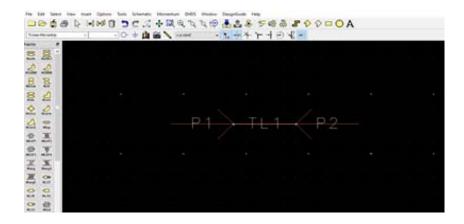


Fig. 3. Microstrip line layout.

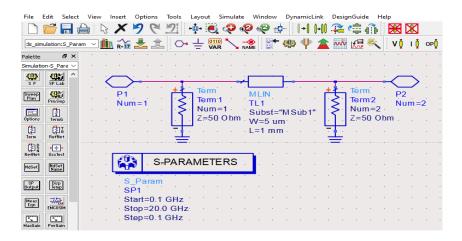


Fig. 4. Schematic diagram.

#### 3. Extraction of Millimeter-Wave Transmission Line Parameters

In Section 2, the parameter extraction has been limited to the series impedance TL parameters and up to 20 GHz. Section 3 expands on the discussion by introducing a method to extract various parameters associated with a TL up to millimeter-wave (mm-wave) frequencies. The parameters of a microstrip TL model provided with the GlobalFoundries 0.13  $\mu$ m SiGe BiCMOS8HP PDK are extracted. In the BiCMOS8HP PDK, the model singlewire is a microstrip TL structure that incorporates one signal line, a metal ground plane, and optional side shields. The back end of line metal levels for the signal line and ground plane are chosen by the designer. In this work, the metal layers, AM and M1, are used as signal line and ground plane, respectively [12].

### 3.1. Parameter Extraction Method

The parameters of the singlewire microstrip TL model are extracted by using the set of equations [13] given in Fig. 5, where equations are written in the format and syntax that ADS uses. In this method, first of all, the *S*-parameters are obtained by ADS EM simulations, and then the *S*-parameters are converted into the *Z*- and *Y*-parameters.

Therefore, this line parameters extraction method can be classified as *Z*- and *Y*-parameters based method. After the simulation, these equations are written in the ADS Data Display window to plot the parameters as a function of frequency.

Fig. 5. Equations for parameter extraction.

#### 3.2. Simulation Setup

Fig. 6 shows the ADS schematic for EM simulations. The width and length of the signal line are chosen as 5  $\mu$ m and 180  $\mu$ m, respectively. The schematic is simulated for the frequency range of 1 GHz to 100 GHz.

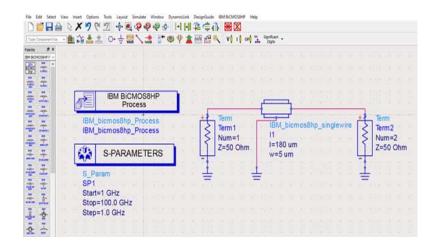
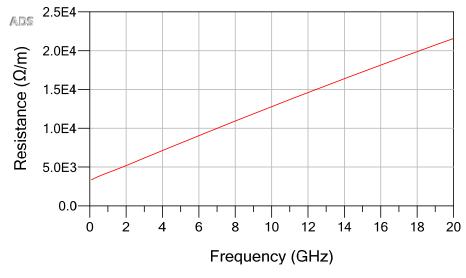


Fig. 6. Schematic diagram.

## 4. Results and Discussion

#### 4.1. Results for the Transmission Line of Section 2

The ADS frequency response graphs of distributed resistance and distributed inductance PUL of the microstrip line for a Si substrate with the conductivity of  $10^4$  S/m are presented in Fig. 7 and Fig. 8, respectively. The units of resistance and inductance PUL are  $\Omega$ /m and H/m, respectively.



**Fig. 7.** Frequency variation of distributed resistance PUL  $(\Omega/m)$ .

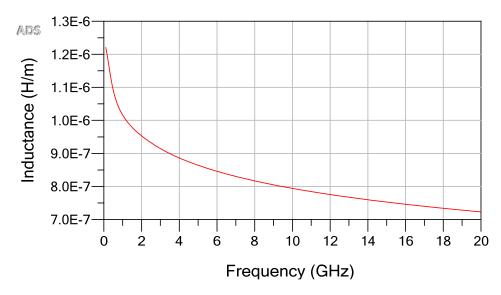
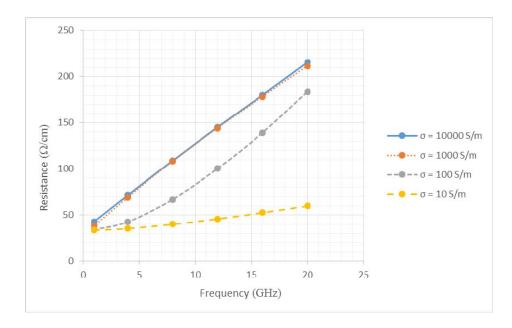


Fig. 8. Frequency variation of distributed inductance PUL (H/m).

Similarly, the frequency response graphs for other conductivities of Si substrate are obtained using ADS. Fig. 9 and Fig. 10 compare the frequency response of distributed resistance and distributed inductance PUL, respectively, for four different conductivities of Si substrate.



**Fig. 9.** Frequency response of resistance PUL ( $\Omega$ /cm) for different substrate conductivities.

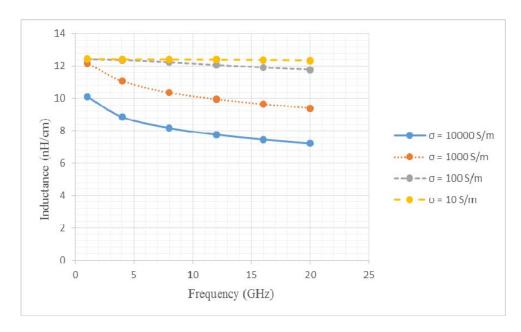
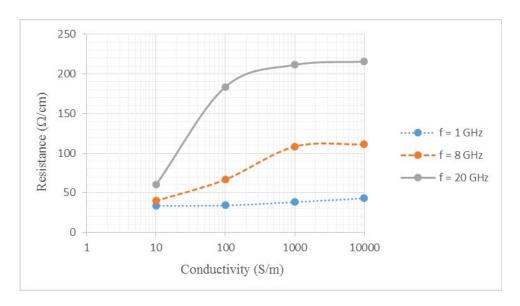


Fig. 10. Frequency response of inductance PUL (nH/cm) for different substrate conductivities.

The lossy behavior of Si substrate increases the dependence of on-chip interconnect parameters on frequency. In Si based technologies, including CMOS and BiCMOS, owing to the higher conductivity of the substrates, the distributed inductance of an interconnect shows the frequency-dependent nature, which is because of the substrate skin effect. Similarly, in addition to the metal skin effect, the substrate skin effect enhances the frequency dependence of the distributed line resistance. The variations of distributed impedance parameters with frequency depend mainly on the conductivity and thickness of the substrate [8].

Fig. 7 shows the linear increment of the distributed resistance PUL with frequency, while Fig. 8 demonstrates the decrease in the distributed inductance PUL of the microstrip line for the substrate conductivity of 10<sup>4</sup> S/m. As displayed in Fig. 9, on decreasing the substrate conductivity, the distributed resistance PUL shows a relatively slow increment with frequency. Similarly, Fig. 10 exhibits that on decreasing the substrate conductivity, the decrease in the distributed inductance PUL with frequency becomes much slower. These EM simulation results support the fact that the frequency-dependent distributed series impedance parameters of the on-chip interconnects show more variations with a higher substrate conductivity. The substrate skin effect becomes more significant with the increase in substrate conductivity.

The variations in distributed resistance and distributed inductance PUL with substrate conductivity for three frequencies are also shown in Fig. 11 and Fig. 12, respectively.



**Fig. 11.** Change in the distributed resistance PUL ( $\Omega$ /cm) with substrate conductivity.

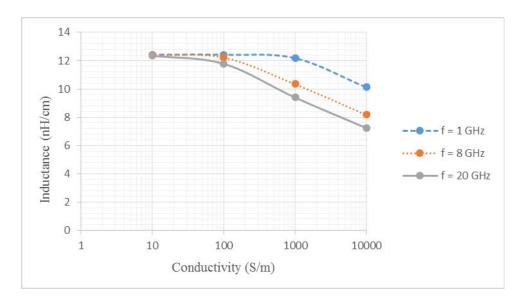


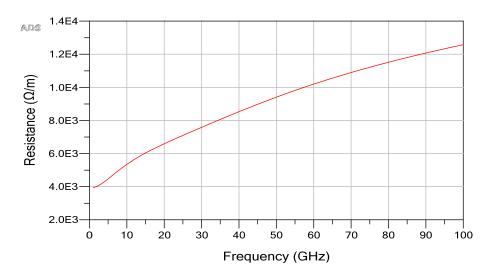
Fig. 12. Change in the distributed inductance PUL (nH/cm) with substrate conductivity.

## 4.2. Results for the Transmission Line of Section 3

The schematic of Fig. 6 is simulated and the frequency response plots are obtained up to 100 GHz by using the equations given in Fig. 5.

## **4.2.1.** Series Impedance Parameters

Fig. 13 and Fig. 14 depict the frequency variation of series impedance parameters of the TL.



**Fig. 13.** Resistance PUL  $(\Omega/m)$  vs frequency plot.

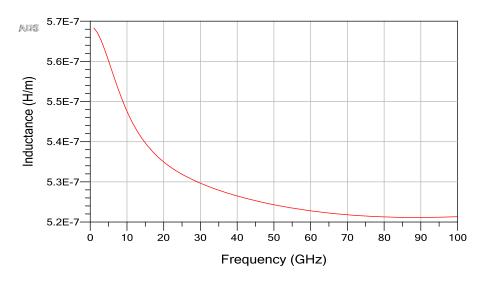
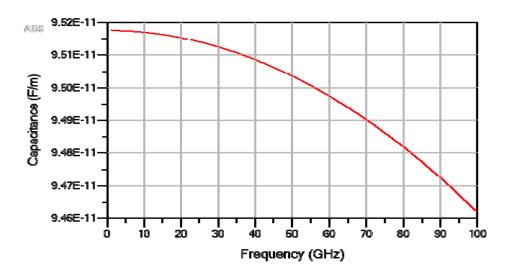


Fig. 14. Inductance PUL (H/m) vs frequency plot.

# **4.2.2.** Shunt Admittance Parameters

Fig. 15 and Fig. 16 present the variation of shunt admittance parameters with frequency.



**Fig. 15.** Capacitance PUL (F/m) vs frequency plot.

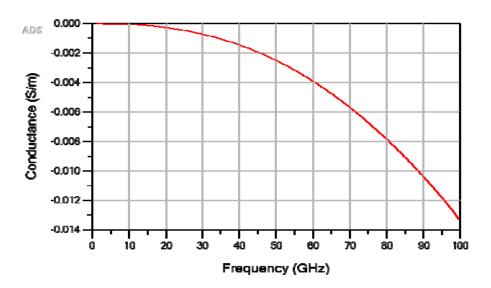
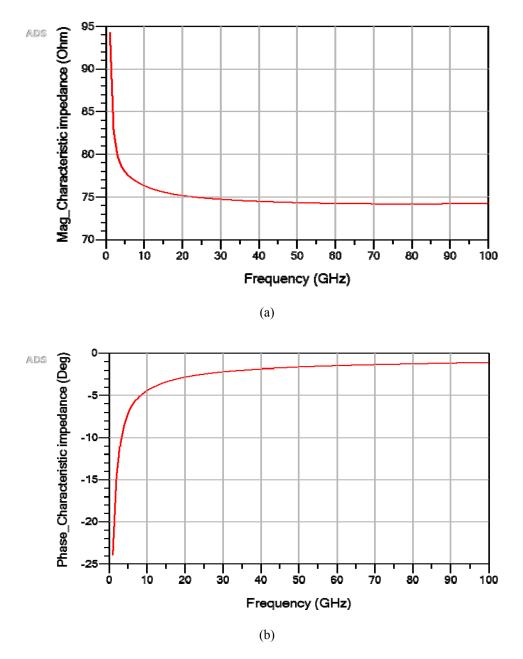


Fig. 16. Conductance PUL (S/m) vs frequency plot.

# 4.2.3. Characteristic Impedance

The magnitude and phase responses of the TL characteristic impedance are illustrated in Figs. 17 (a, b).



**Fig. 17.** Characteristic impedance vs frequency plots.

## **4.2.4.** Propagation Parameters

The magnitude of the propagation constant as a function of frequency is plotted in Fig. 18(a). The attenuation constant and phase constant graphs are demonstrated in Fig. 18(b) and Fig. 18(c), respectively.

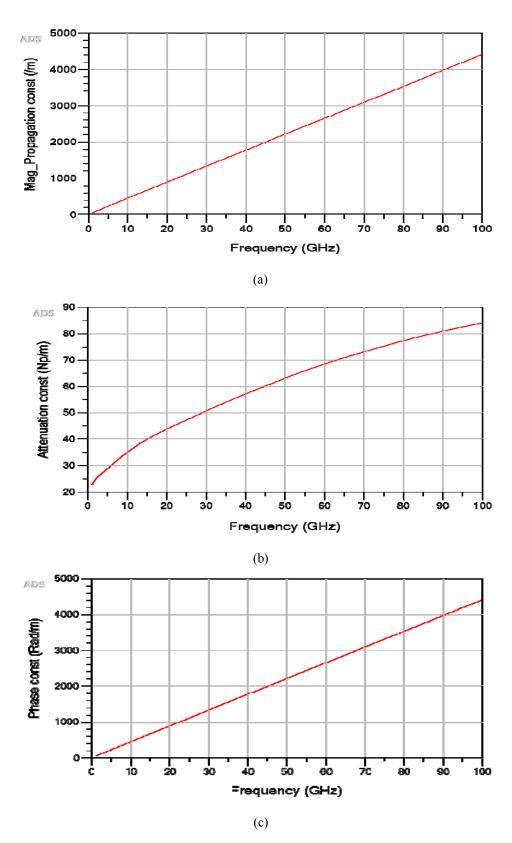
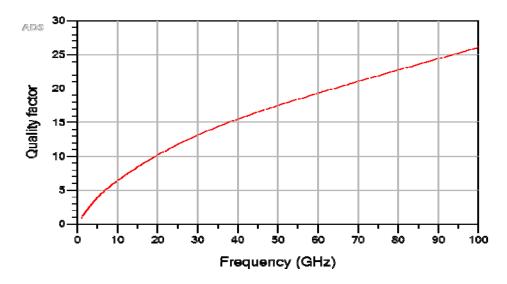


Fig. 18. Propagation parameters vs frequency plots.

#### 4.2.5. Quality Factor

The quality factor variation of the TL with frequency is shown in Fig. 19.



**Fig. 19.** Quality factor vs frequency plot.

#### 5. Conclusion

In this paper, the frequency responses of distributed series impedance parameters of the microstrip TL are compared for four different conductivities of Si substrate. The S-parameters based EM simulation results exhibit the impact of substrate and conductor losses on the variations of series impedance line parameters with frequency. The substrate skin effect shows a significant influence on the frequency characteristics of these parameters. The paper further discusses the Z- and Y-parameters based method for the extraction of TL parameters and plots the frequency variations of parameters in the mm-wave regime.

#### References

- [1] D. Yang, Y. Ding, and S. Huang, "A 65-nm high-frequency low-noise CMOS-based RF SoC technology," *IEEE Trans. Electron Devices*, vol. 57, no. 1, pp. 328-335, Jan. 2010.
- [2] T. Kim, X. Li, and D. J. Allstot, "Compact model generation for on-chip transmission lines," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 3, pp. 459-470, Mar. 2004.
- [3] A. Weisshaar, H. Lan, and A. Luoh, "Accurate closed-form expressions for the frequency-dependent line parameters of on-chip interconnects on lossy silicon substrate," *IEEE Trans. Adv. Packag.*, vol. 25, no. 2, pp. 288-296, May 2002.
- [4] A. Weisshaar and A. Luoh, "Closed-form expressions for the series impedance parameters of on-chip interconnects on multilayer silicon substrates," *IEEE Trans. Adv. Packag.*, vol. 27, no. 1, pp. 126-134, Feb. 2004.
- [5] W. Shu, S. Shichijo, and R. M. Henderson, "Investigation of propagation characteristics of CPWs on a lossy substrate with a novel equivalent circuit," in *Proc. IEEE Texas Symp. Wireless Microw. Circuits Syst.*, 2014, pp. 1-4.

- [6] E. Grotelüschen, L. S. Dutta, and S. Zaage, "Full-wave analysis and analytical formulas for the line parameters of transmission lines on semiconductor substrates," *Integration, VLSI J.*, vol. 16, no. 1, pp. 33-58, Nov. 1993.
- [7] A. Tripathi, Y.-C. Hahm, A. Weisshaar, and V. K. Tripathi, "A quasi-TEM spectral domain approach for calculating distributed inductance and resistance of microstrip on Si-SiO<sub>2</sub> substrate," *IET Electron. Lett.*, vol. 34, no. 13, pp. 1330-1331, Jun. 1998.
- [8] J. Zheng, Y.-C. Hahm, V. K. Tripathi, and A. Weisshaar, "CAD-oriented equivalent-circuit modeling of on-chip interconnects on lossy silicon substrate," *IEEE Trans. Microw. Theory Tech.*, vol. 48, no. 9, pp. 1443-1451, Sep. 2000.
- [9] J. Zheng, V. K. Tripathi, and A. Weisshaar, "Characterization and modeling of multiple coupled onchip interconnects on silicon substrate," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 10, pp. 1733-1739, Oct. 2001.
- [10] W. R. Eisenstadt and Y. Eo, "S-parameter-based IC interconnect transmission line characterization," *IEEE Trans. Compon., Hybrids, Manuf. Technol.*, vol. 15, no. 4, pp. 483-490, Aug. 1992.
- [11] S. Chaturvedi, M. Božanić, and S. Sinha, "Effect of lossy substrates on series impedance parameters of interconnects," in *Proc. IEEE 2016 Int. Semiconductor Conf. (CAS)*, 2016, pp. 55-58.
- [12] MOSIS Integrated Circuit Fabrication Service. [Online]. Available: https://www.mosis.com
- [13] Keysight Technologies. [Online]. Available: http://www.keysight.com