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Analysis and modeling methods for predicting functional robustness of integrated circuits during fast transient events

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Introduction

Integrated circuits miniaturization is still ongoing nowadays allowing increasingly massive integration of electronic functions. An integrated technology is the definition of the dimensions and processes required to manufacture an integrated circuit and its fundamental conception bricks. The main characteristic of a technology is the feature size called λ that represents the smallest dimension for a transistor gate. Size reduction of integrated circuit is mainly accomplished by decreasing this feature size. All other dimensions of the technology are defined as an integer multiplication factor of λ. The value of λ determines the size, power consumption, switching speed, performance and many other properties of a chip. So far, Moore's law successfully predicted that technology dimensions will be reduced by a factor of two every 18 months. The automotive world follows this trend as well, moving recently to 16 nm technology nodes (see Fig. 1) [1] that are normally employed in less demanding applications.

Reduction of λ results in more massive integration on a given silicon surface. The area occupied by a function on silicon is the main cost factor. Reducing this area allows to diminish the unit manufacturing cost resulting in increased profits and margins. For the same area, integrated circuits in more recent technologies can pack more functionalities with higher performances. Weight reduction of electronic modules in automotive or aerospace lowers fuel consumption, and reduces the impact on the environment.

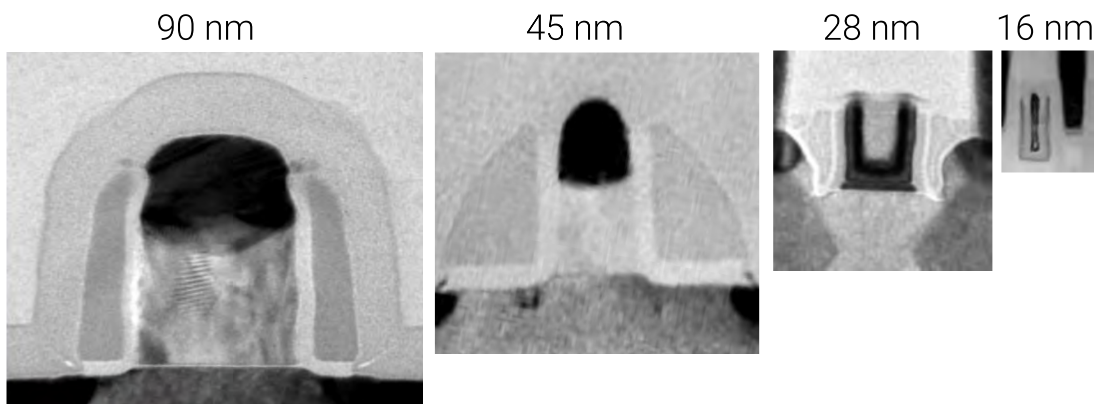

Figure 1: Recent evolution of NXP's automotive technology nodes [1]

The decrease of λ results in reduction of insulating material's thickness. Transistor gate oxide becomes thinner, tolerating lower electrical fields before breakdown. After breakdown, the oxide starts leaking significant amount of currents and the transistor becomes unusable. As a result, the technology provides more sensitive conception bricks and a larger silicon area must be dedicated to protecting the core circuitry [1].

New major trends are also emerging in the automotive field. The development of fully autonomous driving is seeing tremendous progress. This class of functionalities take decisions and perform critical actions such as braking or steering the wheel. Those features are developed to offer increased safety for the user. A side consequence is that electronic modules now have very high responsibilities. The real-time constraint is particularly important, meaning that electronic circuits must perform their duties without delay and operate correctly all the time. For instance, an airbag system must always be ready to trigger in case of car accident without any delay. Electric cars raise new challenges for safety as well, such as battery management. Those features require more computing power, more sensing capabilities and more data to exchange. As a consequence, the amount of Engine Control Unit (ECU)s and electronic modules in a car is growing quickly. Communication buses like the Controller Area Network (CAN) [2] or Local Interconnect Network (LIN) [3] are shared by multiple systems and new standards appear for supporting higher bandwidths. The CAN bus with Flexible Data rate (CAN-FD) is an example of this trend.

The automotive environment is quite harsh for electronic devices and equipments are exposed to a wide range of stresses. A running engine generates plenty of vibrations and mechanical stress. A lot of heat and thermal cycling is produced when the engine is on, and a vehicle is exposed to large temperature variations during its lifetime. Electrical contacts, solder joints and connections suffer from these stresses, and must be designed to withstand them. Electronic system are also exposed to a wide range of electrical stresses especially in the automotive field. Transient disturbances can be generated by natural phenomena or by the vehicle itself. When the engine is turned on, the battery voltage can drop very low due to the amount of current drawn by the ignition. This voltage drop can affect electronic systems and damage them. Another major source of electrical stress is called the Electro-Static Discharge (ESD).

An electrostatic discharge is the sudden flow of electricity between two objects of different charge. It is the result of a local accumulation of electrostatic potential. When a large enough potential difference is reached, a very rapid and large discharge occurs. It is common to record amplitudes in the range of thousands of volts and tens of amperes. A study by Renault car manufacturer [4] estimates that electronic devices are exposed 10000 times to ESDs during their lifetime. It has always been considered a very serious threat for electronic systems.

In terms of architecture, a vehicle is constituted by a multitude of electronic modules interconnected by cables. Interconnected electronic systems need to share a good ground reference for them to communicate and work properly. The car's metallic body is the ground reference for all electronic modules, because a good connection to Earth is impossible inside a vehicle. Electronic modules and the battery are all linked to the car's

body using wires and cables. In D.C. and at low frequencies, this ground connection is good because the vehicle's body is a very large chunk of metal with a very low resistance. At high-frequencies though, those cables have an inductive behavior. They oppose to variations of currents and exhibit large potential differences. Local disturbances can shift the ground reference between one module an another. Electrostatic discharges are high frequency events of very large amplitude and can cause disturbances like this. Inside a vehicle, the discharges can propagate inside cables by conduction, or by coupling between cables through radiated emission. Electronic modules are designed to be robust but the complex architecture and the very harsh nature of ESD makes challenging to guarantee immunity.

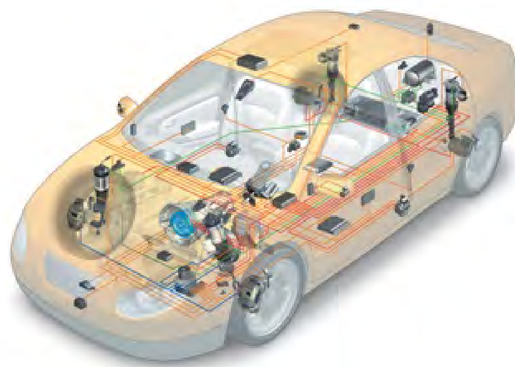

Figure 2: Architecture of electronic systems in a vehicle [5]

In summary, electronic devices must operate in severe automotive environment while using more sensitive conception bricks. Despite the robustness of modules, disturbances such as electrostatic discharges can cause failures. In the ESD field, there are two kinds of failures to consider. The hardware failure, or hard-failure, is when an electronic device is permanently damaged [6]. Destruction can occur through oxide breakdown, when a too large voltage is applied on an insulating material. It can also occur through thermal breakdown, when current through a structure is too high and causes a meltdown. Recently, a new class of failures is being studied. Soft-failure, or functional failure, is when an electronic device fails temporarily to perform its function, because of an electrical disturbance. Different levels of severity can be identified depending on the impact of the failure on the rest of the system. A module that is momentarily disturbed by a discharge but recovers immediately is less severe than a module that requires user intervention. Also, failures on the airbag system are much more severe than on the entertainment system, because user safety is put at risk in the first case. A first article on the topic was published by F. Caignet and N. Lacrampe in 2007 [7]. A large amount of research at the system level was published in EOS/ESD symposium 2012 [8, 9, 10] and 2013 [11, 12]. The draft standard IEC 62433-6 [13] aims to provide a base framework for soft-failures analysis and prediction. Analysis of the literature reveals that most

studies are currently focused on system-level soft-failure analysis. There is currently no real work at the component level or studies performed inside the design of an integrated circuit.

Beyond studying failures inside integrated circuits, it is important to keep in mind how chips are designed and developed. This is important to propose solutions that are actually implementable. This entire process from the specification to the manufacturing of a product is called the design flow (see Fig. 3). During this process, there are many teams and people involved. Modeling team creates electrical model of technology components. Design team assembles component together to create integrated functions that conform to the specification. Layout team translates the electrical schematic into the series of masks and layers required by manufacturing. The laboratory tests manufactured parts and runs investigations in case of failures. The ESD and Electro-Magnetic Compatibility (EMC) team has the particularity to interact will all teams because issues and solutions can be found in any step of the design flow. The main source of delay in this process is the manufacturing time which can be of several months. Designs are put on silicon but the parts are tested only after manufacturing, several months later. To gain time to market and be competitive, it is essential to reduce the number of design-manufacturing-testing cycles. Each additional manufacturing is very expensive, and increases further the development time of the product. This is why any simulation tool able to predict early any kind of failure (and functional failures among them) is very valuable for silicon design companies.

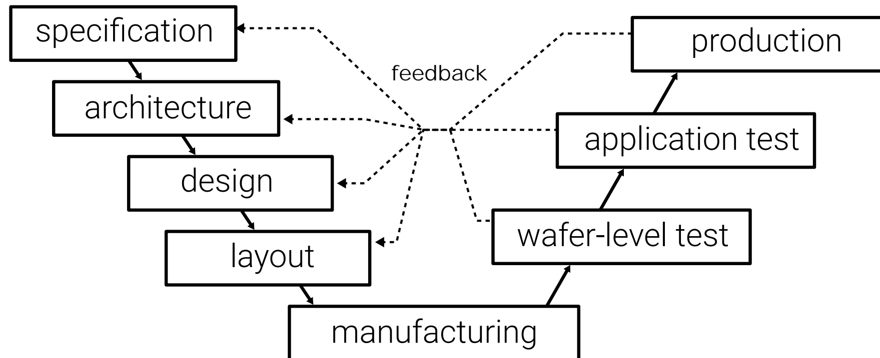

Figure 3: Simplified integrated circuit design flow

It was demonstrated that real-time electronic circuits have higher responsibilities yet they can be disturbed by disturbances such as electrostatic discharges. It is essential to understand how failures appear in order to fix them and prevent them prior to manufacturing. For this purpose, many approaches and methods were explored and detailed in this document. Fig. 4 shows the different paths taken during the research, all studied in parallel with the ultimate goal to develop and validate integrated circuit models for soft-failures. Among all proposed approaches, a modeling method of electronic systems exposed to electrostatic discharge is developed, improving prior work on the topic [14, 15]. It helps determining what fraction of an incoming discharge reaches

the integrated circuit. Then, on-chip measurement methods have been designed and manufactured, in order to acquire more data inside the chip. Those methods comprise monitoring devices such as an on-chip current sensor, overvoltage and undervoltage detectors, and a communication chain for fast prototyping. Finally, modeling methods were experimented using simulation tools. The first method models each block function individually, then offer to chain and combine models together to deduce the robustness of a complete top-level function. The second method aims to build an electrical equivalent model of the integrated circuit, for system-level simulations. Black box modeling that abstract the internal design using only the external behavior is used. Finally, a concept of an assertion system is detailed, to identify quickly and efficiently during preliminary design phase the potential weakness of an integrated circuit.

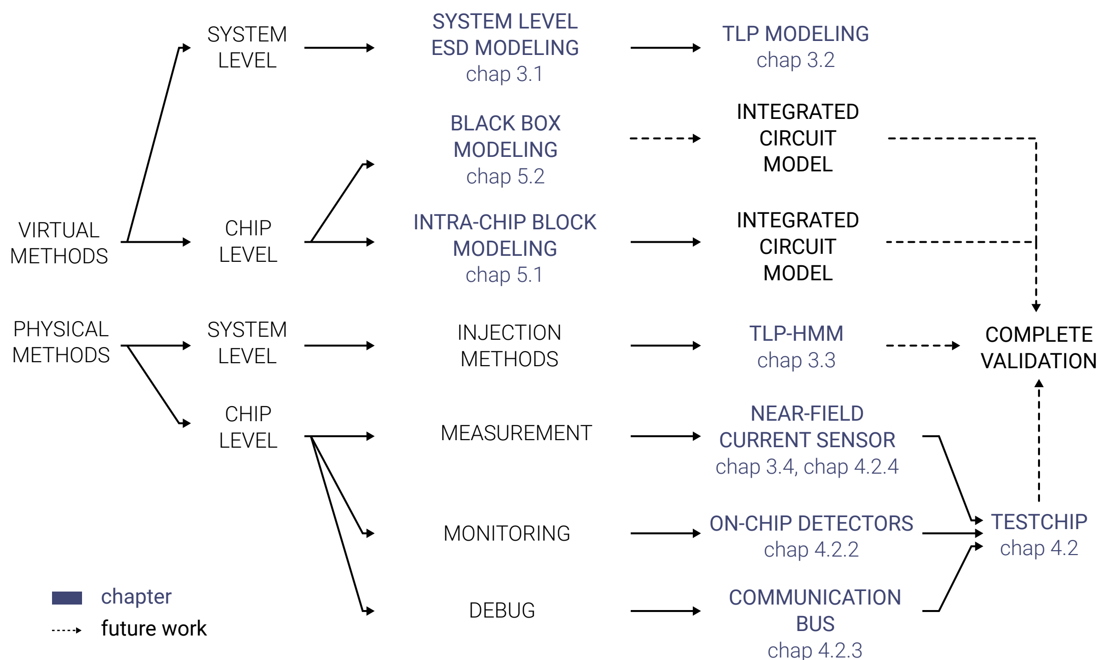

Figure 4: Explored research paths for soft-failure investigation and prediction

Chapter 1 details what is an electrostatic discharge and how to reproduce it in laboratory conditions. This preliminary work highlights how functional failures appear and how they impact electronic devices. The literature about ESD-induced soft-failures is reviewed . It is demonstrated that so far that most of the studies are focused at the system level, and that it remains very challenging to identify failure root cause without access to the chip design.

Chapter 2 presents a modeling method for simulating ESD waveforms up to the integrated circuit inputs. The first challenge for understanding soft-failures at silicon-level is to determine what fraction of an incoming ESD actually reaches the integrated circuit. Between the injection point of a stress and the disturbed circuit, many devices are connected such as cables, discrete devices, etc. Each element interacts with the

discharge, absorbs a part of its current or changes the waveform. A model library of common electrical elements found in ESD testing environment has been constructed and is detailed. The modeling method is applied to a complex pulse generator, and yields a highly accurate model. Finally, a new test generator was developed to overcome some issues met during the debug of silicon-level failures using system level ESD testers [16, 17]. The principle of operation and architecture of the generator is described. It produces the same compliant waveform than those standards, with some advantages such as increased testing reproducibility and zero radiated emission.

A case of soft-failure in an integrated circuit is explained in chapter 3. In a first phase, measurement data is obtained at the application board level and the failure is explained. Simulations are run to understand how failures appear, and more specifically how a short electrical event can disturb an integrated circuit for a long period of time. In a second phase, the integrated function is placed onto a custom testchip. Specific on-silicon structures were designed to gather measurement data on electrical nets that are not physically accessible. All these measurements are performed for the purpose of estimating the accuracy of integrated circuit ESD simulations. There are two main potential sources of error that are checked. Silicon technology device models are not designed to function for extremely fast transient transient disturbances. Also, standard simulations do not take parasitic devices into account, such as metal track resistances and parasitic couplings. Measurement data is confronted to simulations in order to verify the validity of models. Analysis of the failure led to the development of a testchip, to put on silicon the same failing function but with a more convenient environment for measurement and investigation.

When issues are discovered late in the testing lab, analysis is performed manually, by trial and error, searching inside the design why the function is failing. It is a complex and time-consuming process. The core research of this work focuses on proposing new analysis methods and tools for electrical simulations. It is detailed in chapter 4. The first method offers to study and model block functions individually, then connect the models together to deduce the robustness of a top-level function. The second method targets system-level simulations comprising integrated circuit. It focuses on modeling an integrated function with a behavioral model that is not aware of the internal design, in order to run powered ESD simulations. Finally, a concept is presented for easing the search of soft-failures during integrated circuit development. It is based on using a assertions inside the blocks to efficiently and quickly find which function or net is being disturbed due to an ESD.

The final conclusion summarizes the work achieved during the PhD, highlights the most notable discoveries, and identifies follow-up work and research topics that could be worth pursuing.

Chapter 1

Review of ESD testing and functional analysis

1.1 Context

1.1.1 Electrostatic discharge

An electrostatic discharge (ESD) is the result of the accumulation of electrostatic potential. It is a very sudden current flow that propagates through metallic or non-metallic materials, electrical systems and sometimes even through the air. It is a very short electrical event, involving large currents, extremely high voltages, and durations in the range of a few hundred nanoseconds. Currents can reach tens of amperes and voltage levels several thousand of volts. The total discharge energy is small, somewhere near the millijoule (mJ). The power on the other hand is extremely high because the waveforms are changing extremely rapidly.

Objects can accumulate electrostatic potential by tribocharging or electrostatic induction. In the case of tribocharging, electrons are transferred from one object to the other when they are put into contact and then separated. One object becomes positively charged and the other negatively depending on the kind of material constituting each one. Nature of common materials in that regard is given in Table 1.1

Field induction, also called electrostatic induction, works differently but also results in accumulation of electrostatic potential. When a piece of material is placed inside an electric field, positive and negative charges of the material become spatially separated, at a macroscopic scale. If the object is temporarily grounded in one point, charges near that location are evacuated, in majority positive or negative. Similarly to tribocharging, electrostatic induction causes the material to loose its electrical neutrality.

Tribocharging happens constantly when a vehicle is in motion [19]. It occurs because of the friction of the tires on the road surface, which is a constant contact followed by separation mechanism. Therefore, static electricity accumulates constantly inside a vehicle, until a discharge happens.

Triboelectrification may also happen between a human body with clothing and the

↑ Positive	Rabbit fur
	Glass
	Mica
	Human Hair
	Nylon
	Wool
	Fur
	Lead
	Silk
	Aluminum
	Paper
	Cotton
	Steel
	Wood
	Amber
	Sealing Wax
	Nickel, copper brass, silver
	Gold, platinum
	Sulfur
	Acetate rayon
	Polyester
	Celluloid
	Silicon
↓ Negative	Teflon

Table 1.1: Typical Triboelectric Series (Credit: ESDA [18])

seat fabric, eventually leading to an electrostatic discharge. The probability of discharge is rather low [19] and the phenomenon can be only be observed in rare situations when the human body leaves the vehicle.

Similarly, triboelectrification can also occur between the vehicle's body and the airflow generated by the motion. More specifically, it is not the air itself but the dirt particles carried in it that induce the contact and separation process. The ESDA indicates that virtually all materials can be triboelectrically charged [18] as long as the contact and separation process exists.

1.1.2 Impact of ESD on electronic devices

As detailed in the introduction, electrostatic discharges constitute a large threat for electronic devices. Failures can occur during manufacturing or normal operation. The manipulation of parts by manufacturing machines involves repeated contact and separation. Ultimately, triboelectrification and discharges happen and devices can get de-

stroyed. Several standards exist to guarantee that devices can survive this manufacturing step.

The Human Body Model (HBM) reproduces the discharge of a human body into a device. It is standardized in Method 3015.9 of MIL-STD-883 [20] and JEDEC JS-001-2014 [21]. The charged human body is modeled by a 100 pF capacitor and a discharge resistor of 1.5 kΩ. Charging voltages reach a maximum of 8 kV, although nowadays customers tend to ask for less than that.

The Charged Device Model (CDM) is a field-induced ESD test. The component under test is placed between two charging plates that generate an electric field. At some point, a grounded pin is brought near any of the pins of the component, forcing the charges to evacuate suddenly. This test is standardized in [22].

The Machine Model (MM) used to be another ESD testing specification that is now considered deprecated. The JEDEC committee recommended discontinuing use of this standard [23], because it is the result of a misunderstanding of real-world events in manufacturing environments. It does not help improving the reliability of devices against electrostatic discharges.

Those three tests (HBM, CDM, MM) aim to guarantee that the devices can survive their manufacturing environment qualified as Electrostatic Protected Area (EPA). An EPA area involves special hardware such as anti-static wrist wraps or special carpet materials to avoid the accumulation of electrostatic potential and electrostatic discharges.

Over the years, manufacturing processes and standards have been improved, reducing the requirements of discharge levels to sustain. In parallel, the factory environment has been studied extensively to identify actual levels devices are exposed to. Machine Model deprecation is the perfect illustration of increased community knowledge and experience. Those efforts aim to reduce the pressure on semiconductor manufacturers that are facing growing challenges to protect devices, because of the shrink of technologies and robustness.

After manufacturing, failures can happen with the device in its operating environment. Manipulation by electrically-charged humans is a major source of danger for commercial products like cellphones and cameras. The automotive environment is even harsher, with vehicles being a major source of electrostatic discharges.

The electrical destruction of a device is called a hard-failure. A hard-failure corresponds to changes in the material structure or properties of a device to the point where it no longer fulfills at least part of its specification. ESD induce those failures because of the extremely large current densities, high voltages, and power levels involved. Different kinds of failure signatures can be observed. Pictures of destroyed devices, obtained with an electronic microscope, are provided in Fig. 1.1.

A first kind of common failure for integrated devices is the oxide breakdown. Oxide breakdown happens when an insulating material is exposed to a larger electric field than it can tolerate. A picture of the oxide of a device destroyed because of an electrostatic discharge is provided in Fig. 1.1. During an ESD, large voltage variations in a short amount of time result in very large electric fields. Oxide breakdown happens usually with the insulator constituting the gate of a Metal-Oxide Semiconductor (MOS) transistor.

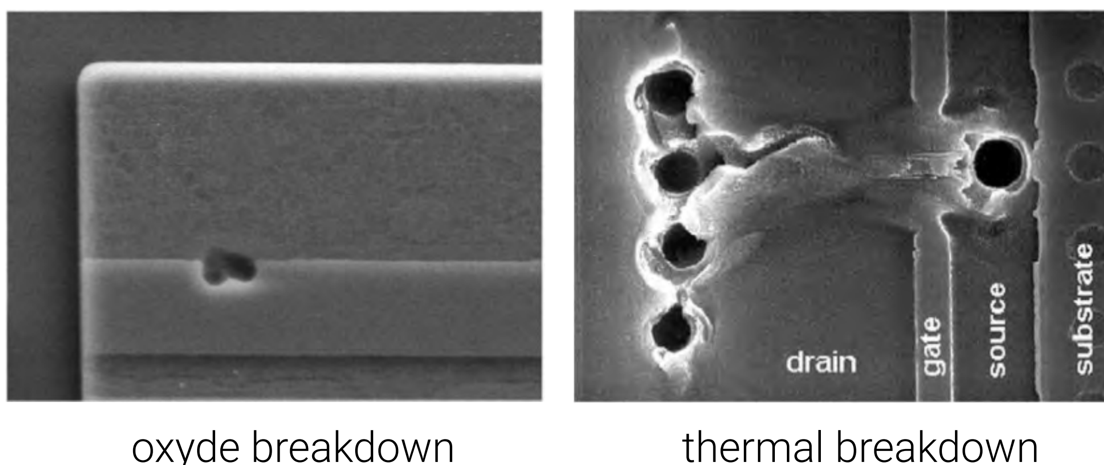

Figure 1.1: Example of ESD induced failures at silicon-level (From [24])

As technologies shrink, so does transistor gate oxide thickness. After the failure, the gate that is normally insulated from the rest of the device leaks significant amount of current. The transistor can no longer operate and is considered destroyed.

Thermal breakdown is another kind of ESD induced failure. It is the result of an elevation of temperature inside the silicon, above its melting point. It is caused for long discharges that can induce significant and very localized device heating. It results in a significant increase of leakage current or apparition of short-circuits.

Finally, metal melting is the last kind of failures observed after a discharge. Inside an integrated circuit, metal tracks are rather resistive because of their form factor. Resistivity sits in the range of $10\,\mathrm{m}\Omega\,\square^{-1}$ to $100\,\mathrm{m}\Omega\,\square^{-1}$. When large currents are flowing, metal tracks and vias dissipate power and heat up. The elevation of temperature, if large enough, can melt the metal track and turn it into an open-circuit.

Integrated circuits are studied and protected against hard-failure since a few decades. Despite this experience of the ESD community, it remains challenging to perfectly protect an electronic system against hard-failures. Nowadays, a new class of failures appears. Instead of studying permanent failures, devices are studied for temporary failures affecting their functionality. These are called soft-failures or functional failures. ESD can cause them to happen, with diverse consequences. In less severe situations, functionality of a chip is disturbed just for the duration of the ESD and recovers immediately without noticeable consequence. The failure remains located inside the integrated circuit and does not impact the application above. Sometimes, the discharge is harmful enough to cause a circuit to restart because the ESD disturbed some critical nets or parameters. This is common when supply voltages go out of specification for instance. Startups or power-on reset functions can interpret overvoltage or undervoltage caused by disturbances as the signal for a regular power-up sequence. The device can also perform restarts to try a recovery because proper operations cannot be guaranteed, due to unexpected values on some nets. Most microcontrollers for instance monitor supply

voltages of digital gates. If the voltage is too low, the noise margins of the gates cannot be guaranteed and proper operation either. At this point, the microcontroller restarts in an attempt to recover normal operation. Restarts are slow processes compared to the operation of a chip. For critical applications, this delay is highly unwanted because it impacts human safety. The availability of the chip that triggers airbags in a car is vital for instance. In a more severe scenario, the system gets completely frozen or stuck into an unwanted state because of the ESD. The only way to recover normal operation requires a user-intervention. User intervention can take the form of turning the key to shut down and restart the vehicle's engine. Finally, hard-failure can be seen as the next step immediately after the most severe soft-failure. The device is in a non-recoverable state and must be replaced. Hard-failures are not considered for functional robustness analysis.

In this context, soft-failures represent a risk just as important as hardware failures. To limit risks and costs inherent to upgrading a device after it was deployed in the field, these failures must be taken care of as early as possible. Ideally, the robustness of an electronic product should be studied, characterized or simulated during its design phase. The research conducted and presented in this document aims to develop new tools and techniques for studying and predicting functional failures.

To protect sensitive electronics against discharges, several options are available. The most common solution, presented in the next section, is the ESD protection.

1.1.3 ESD protection

ESD protections divert discharge current before it reaches sensitive circuitry. By offering a low impedance path to ground, they clamp input voltages to avoid crossing the maximum accepted levels. Fig. 1.2 gives a simple example of ESD protection strategy. Current is routed into the ground before reaching the core circuitry. Protections have very low on-resistance, usually in the order of a few ohms. Even with a few amperes of current, voltage remains low. ESD protections can absorb significant amounts of current for very short periods of time, but they are not designed to sustain DC currents.

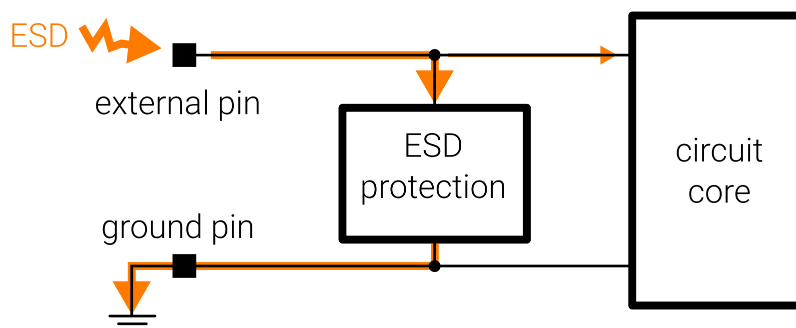

Figure 1.2: Classic ESD protection strategy

Inside an electronic circuit, ESD protections are found in two different locations. On-chip protections are integrated directly into silicon. External protections are discrete devices connected to inputs or outputs of integrated circuits. Historically, on-chip protections were designed for stresses generated during manufacturing. They were not aimed to protect against system-level discharges, i.e. discharges happening in the field during the normal product life. This task was fulfilled by external protections, such as transient voltage suppressors, diodes, capacitors, filters. Over the years, design techniques and simulations tools have improved, and more robust integrated protections could be designed. On the other hand, equipment manufacturer were always looking for means of reducing the bill of materials (BOM) or the cost of electronic systems. This led to a shift of responsibilities toward on-chip ESD protections for handling system-level stresses. The shrink of integrated technologies makes this tasks even more challenging. External protections are still very relevant, where an integrated solution would occupy too much silicon area, or when very harsh requirements are demanded.

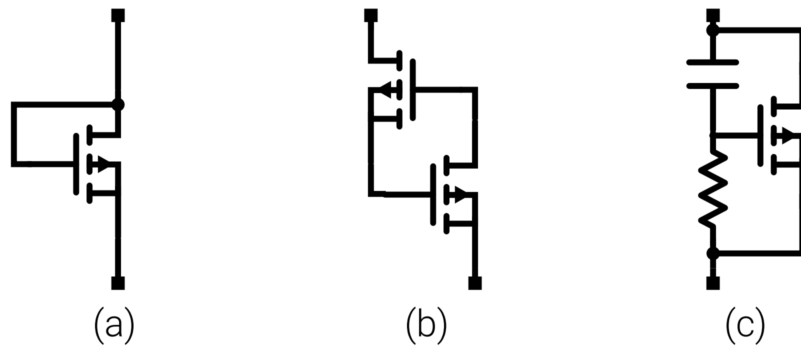

Figure 1.3: common ESD protections architectures - (a) Diode (b) Thyristor (c) RC-triggered MOS

ESD protections can be designed in various ways (see Fig. 1.3). Diodes or thyristors are two main architectures used for designing a protection. Thyristors have typical snapback characteristics as shown in Fig. 1.4. RC-triggered MOS are frequently found for protecting low-voltage Input and/or Output (I/O) of Complementary Metal Oxide Semiconductor (CMOS) circuits. Basically, it is a power transistor activated during the discharge by a resistor-capacitor network. During a transient event, the capacitor acts as a short-circuit, rising the gate potential. The MOS switches on and absorbs current, deviating it into the ground.

A few key values are important for describing a protection. V_{t1} refers to the triggering voltage of the protection. I_{t1} corresponds the current absorbed by the protection immediately after triggering. V_{t2} and I_{t2} describe the coordinates where the protection is destroyed. A sudden increase of the leakage current (Fig. 1.4) is a good indicator of a damaged protection.

To design an efficient ESD protection, several requirements are to be fulfilled. This is called the conception window, illustrated in Fig. 1.5. In the absence of a discharge,

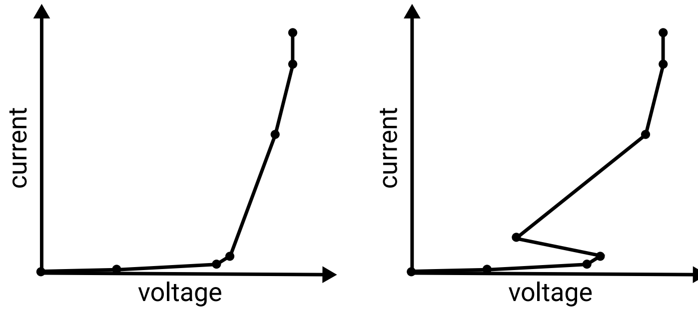

Figure 1.4: I(V) curves of typical ESD protections with snapback and no-snapback

protections must be transparent to the rest of the device. It corresponds to the area in green in Fig. 1.5. The protection must trigger above the operating voltage of the circuitry. For instance, if an input operates between 0 V and 5 V, and the protection switches on at 4 V, it will trigger during normal operation and be immediately destroyed. On the other hand, protections must clamp voltage (by absorbing current) before reaching the maximum voltage tolerated by the silicon gate oxide. It corresponds to the red area on Fig. 1.5. When absorbing large currents, the protection heats up very high locally. If the temperature exceeds the melting of silicon (1414 °C), the protection device gets destroyed through thermal breakdown, corresponding to the area in orange in Fig. 1.5. For demanding applications, protections must trigger at a given voltage accurately, independently of manufacturing process, mismatches and temperature variation. This reduces the conception window substantially and makes the design more challenging.

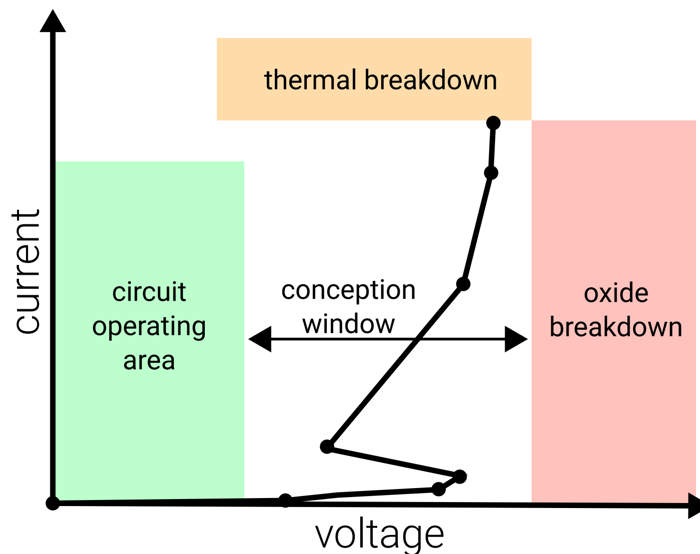

Figure 1.5: Conception window of an ESD protection

To design and validate protections, tools like Synopsys TCAD (Technology Computer Aided Design) [25] are employed to simulate semiconductor physics. Afterwards, an electrical model is constructed, to verify that the protection and the circuit cooperate as expected. Simulation is ran in a Simulation Program with Integrated Circuit Emphasis (SPICE) environment. Modeling of ESD protections for SPICE simulations is presented later in chapter 2.1.3.

1.2 Review of ESD testing

Electronic hardware robustness is tested against electrostatic discharges using different test methods and standards. Each method reproduces a specific discharge event in laboratory conditions. In this chapter, relevant ESD generators for this research work are detailed.

In ESD testing, a distinction is often made between so-called system-level level tests and Integrated Circuit (IC) level tests. System-level tests reproduce discharge events encountered by a system deployed in the field. Silicon-level tests target ESD events happening during IC manufacturing.

System-level tests involve higher voltage and current amplitudes, and are more harmful for electronic devices than IC level tests.

1.2.1 Transmission Line Pulsing (TLP)

The transmission line pulsing generator is an extremely popular tool in the ESD field. Over the years, it was employed in a variety of applications, from characterization of devices [26, 27], investigation of failures [28, 29] and correlation of failure levels with other generators [30]. It is a versatile tool, that was often modified to address larger testing conditions [31] or non-rectangular pulse waveforms [32, 33]. The technique was invented by T. Maloney and N. Nakamura [34]. It is standardized as part of ANSI/ESD STM 5.5.1-2016 [35] through the effort of the ESD Association (ESDA) [36]. It was extensively studied during the PhD thesis of N. Monnereau [15] and N. Lacrampe [14].

Transmission Line Pulsing (TLP) systems produce a short rectangular pulse, through the discharge of a coaxial cable (Fig. 1.6). The cable is initially charged with an high-voltage voltage supply through a high value resistor. This keeps the current small and avoids oscillations on the cable. When the voltage of the cable reaches the desired amplitude, a relay can be switched to trigger the discharge. The coaxial cable has usually a characteristic impedance of 50 Ω and a length of 10 m, corresponding to a 50 ns propagation delay. The generated pulse is twice that delay.

TLP systems constitute very well-controlled test generators. The pulse is generated inside a shielded environment. It is isolated from external radiated emissions and does not emit electromagnetic disturbances. The characteristic impedance of 50 Ω can be controlled up to the load, by using appropriate 50 Ω cables and hardware. Those properties result in clean and repeatable pulse waveforms without reflections. The main features of the generated pulse are given in figure 1.7.

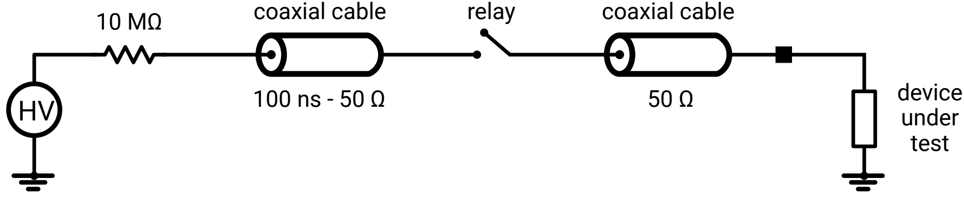

Figure 1.6: Minimal example of a TLP system

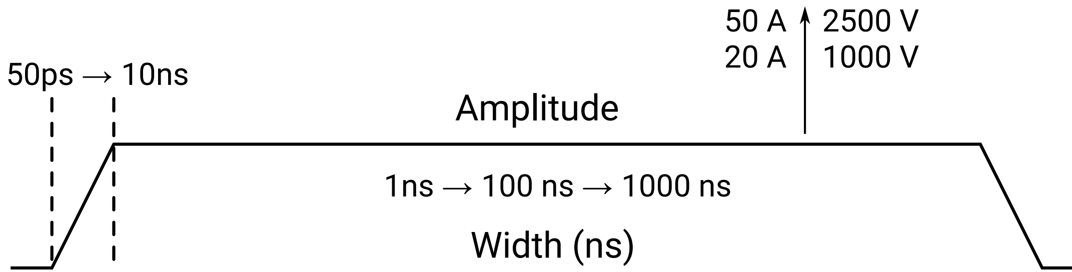

Figure 1.7: Main characteristics of a TLP pulse on a resistive load

The waveform parameters are completely controlled and easily tunable. The charging voltage is set by the high-voltage source. The pulse width can be increased or decreased by changing the length of the coaxial cable. The risetime can be enforced with a $50\,\Omega$ matched risetime filter [37, 38]. Unlike most filters, they are specifically designed to work by absorption and not by reflection. They do not pollute the system with reflected waves.

TLP generators can also be employed as a measurement tool. Some configurations use Time-Domain Reflectometry (TDR) and others rely on more standard techniques for measuring electrical properties of a load.

Time-domain reflectometry is a measurement technique with a wide range of applications. With TDR, it is possible to determine electrical properties of a device by observing reflected waveforms. Application of time-domain reflectometry to TLP is described in the ANSI ANSI/ESD STM 5.5.1-2016 standard [35]. In this configuration, voltage and current measured at the output of the generator are equal to voltage and current waveforms inside the load.

This is due to the superposition of the incident and reflected pulses during the discharge (see Fig. 1.8). When the relay is closed, an incident wave appears that propagates toward the load. The impedance mismatch between the load and the connection cable forces a part of the incident power to reflect back. The rest is absorbed and dissipated by the load. This reflected wave corresponds to the difference between the incident power and the absorbed power, but with a negative sign. At the measurement point, the incident wave and the reflected wave add up. Eq. 1.1 explains how this sum is equal

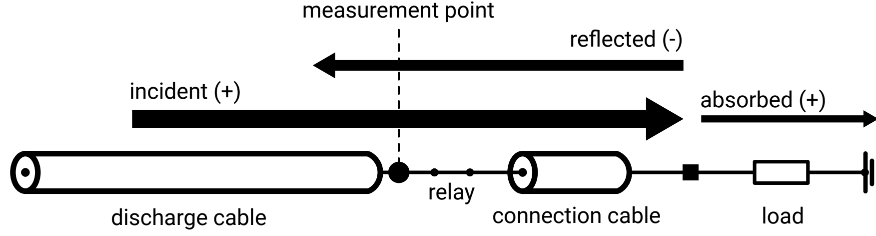

Figure 1.8: TDR measurement with incident and reflected waves superposition

to the value absorbed by the load, for the voltage.

$$V_{measured} = V_{incident} + V_{reflected} = V_{incident} + (-(V_{incident} - V_{absorbed})) = V_{absorbed} \quad (1.1)$$

The same equation applies for computing the current value. In summary, the measured voltage and currents at the output of the TLP are equal to the voltage and current inside the load, when incident and reflected waves are superimposed. An extensive analysis of Time-Domain Reflectometry (TDR) TLP is provided in [15].

Fig. 1.9 provides an example of a typical waveform generated by a TLP injecting in an ESD protection. The recording is done in a TDR configuration. Voltage and current waveforms usually exhibit two steps. The first step is due to the connection cable that links the TLP to the load (see previously Fig. 1.6). Delay Δt_1 corresponds to the delay of the connection cable. The ratio V_1/I_1 is equal to the characteristic impedance of the connection cable, usually $50\,\Omega$. The second step is the response of the tested load. The value V_2/I_2 is the quasi-static resistance of the load. V_2/I_2 is a function of the TLP charging voltage. By averaging each waveform during a few tens of nanosecond, the current and voltage value of the load can be accurately sampled.

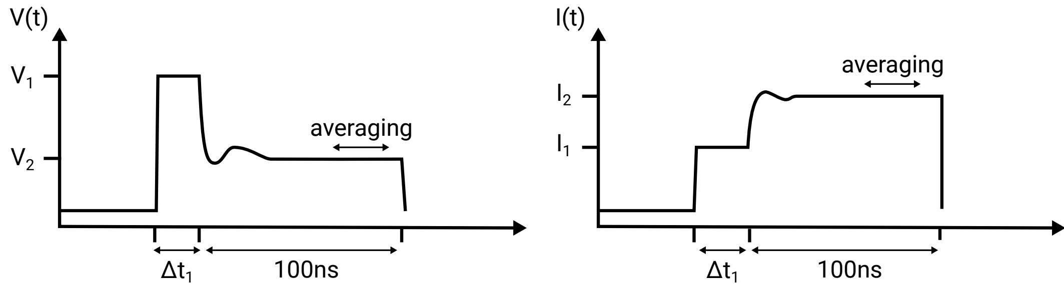

Figure 1.9: TLP V(t) and I(t) example

The pulse ends when the main coaxial cable is fully discharged. The pulse lasts twice the delay of the discharge cable. At 0 ns the relay is closed. The cable starts discharging from the end closer to the relay. The other end starts discharging only 50 ns later because of the propagation delay. It takes another 50 ns delay for the discharge to completely

propagate back to the relay side. This explain why the pulse length is twice the coaxial cable delay.

A very popular application of transmission line pulsers is the extraction of an $I(V)$ curve 1.10 from a set of pulses and measurements. An $I(V)$ represents the current versus voltage response of a device. They are called quasi-static because values are sampled during a short amount of time and cannot be entirely assimilated to a DC characterization. They are extracted at much larger levels than the device can withstand in DC. Quasi-static $I(V)$ curves are particularly useful for characterization of ESD protections [26], that by nature work in transient regime and cannot be studied in DC.

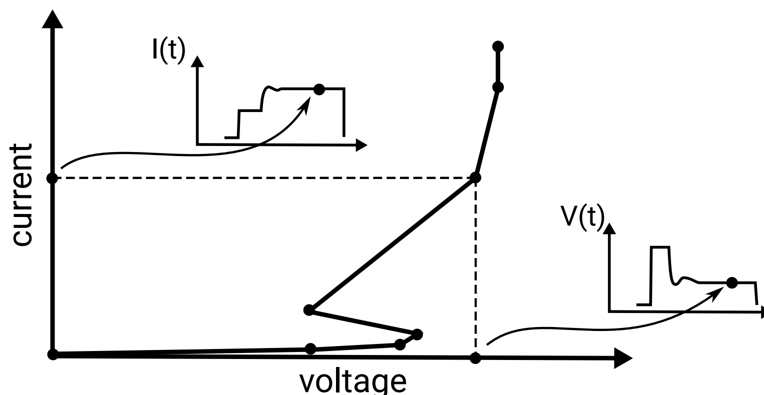

Figure 1.10: TLP-extracted I(V) characteristic example

The $I(V)$ curve is extracted point after point. Each point corresponds to a voltage and current measured by averaging the transient waveforms during the second step. A first pulse is injected, current and voltage are measured, and the coordinates of a first point are extracted. Then the process is repeated and the charging voltage is incremented after each new point (Fig. 1.10). Depending on the kind of tested device, snapback responses can sometimes be measured. A snapback response is a non-monotonous curve, where a single x-axis value (voltage) can correspond to multiple y-axis values (current). An example is provided in Fig. 1.10. Snapbacks are observed for devices with at least two different states of operation. In the off-state, it acts as a high-value resistance and current increases very slowly when voltage gets higher. When the device turns on, its resistance drops abruptly and becomes very small. Current suddenly increases and voltage falls. This transition corresponds to the discontinuity visible on the curve.

TLPs are also commonly used for testing the robustness of systems and devices [27, 7]. It is great for troubleshooting because the pulse is well repeatable. A rectangular waveform is also more desirable for investigation, it simplifies the analysis. However in some cases, it can be an issue for reproducing a failure observed with more time-varying waveforms like IEC 61000-4-2 [16] described after.

A few variations of the TLP exist to cover edge cases and specific characterization requirements. The very-fast TLP (vf-TLP) is one of them. It was designed by H. Gieser

[39] to reproduce gate oxide breakdown. Basically, it is a TLP with a shorter pulse width, usually in the range of 1 ns to 10 ns.

vf-TLP requires more advanced calibration techniques for measuring load current and voltage, and stronger constraints on the quality and bandwidth of test elements and measurement systems. In this configuration, incident and reflected waves never superimpose and by default time-domain reflectometry cannot be employed as-is. However, E. Grund adapted the technique to vf-TLP in [40]. With this method, it is possible to analyze and calculate the impedance of all elements between the generator and the load.

To sum up, Transmission Line Pulsing is an extremely versatile and useful technique for the ESD field. It is not considered a qualification tester though because it does not reproduce any real-world electrostatic discharge events. Standards and other techniques dedicated to this task are described hereafter.

1.2.2 ESD Gun (IEC 61000-4-2 / ISO 10605)

IEC 61000-4-2 [16] and ISO 10605 [17] standards define a system-level test waveform and test generator to reproduce the discharge of a human body through an electronic device. This test is used very extensively for qualification of products. Fig. 1.11 provides a picture of an ESD gun. The gun is composed of a metallic discharge tip to inject the pulse. The ground return is a long metallic ribbon a couple of meters long. Depending on the test configuration, it is connected to the product ground or the earth. Its shape impacts a lot recorded failure levels. Historically, ESD gun were famous for lacking some reproducibility on test results [41]. They have largely improved since then although radiated emissions and shape of the ground return still remain a very large factor of variation and uncertainty [42].

Figure 1.11: Picture of an ESD gun IEC 61000-4-2 compliant

Fig. 1.12 presents the main properties of the generated stress. The standard defines this waveform for a 2 Ω load. The pulse starts by a fast peak with a 1 ns risetime. It is followed by a slower slope of smaller amplitude but longer duration of about 200 ns. Voltage levels can reach 15 kV peak and 30 A of current.

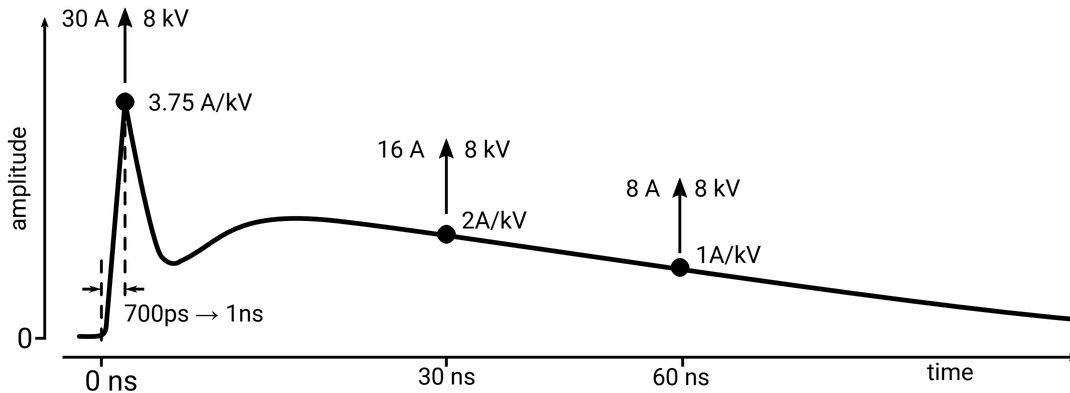

Figure 1.12: Main properties of an IEC 61000-4-2 pulse on a 2 Ω resistive load

The generation of the ESD pulse is done with a 330 Ω resistor and 150 pF capacitor discharge network. The RC network alone though does not suffice to reproduce the waveform. Parasitic devices play an important part in shaping the waveform. Fig. 1.13 provides a physically-based ESD Gun model that helps understand the impact of parasitic devices. This model was originally written by Chiu [43] and is referenced in the PhD thesis of N. Monnereau [15]. It adds an RLC network to model the ground return. A series parasitic capacitance inductance model imperfections in the direct injection path.

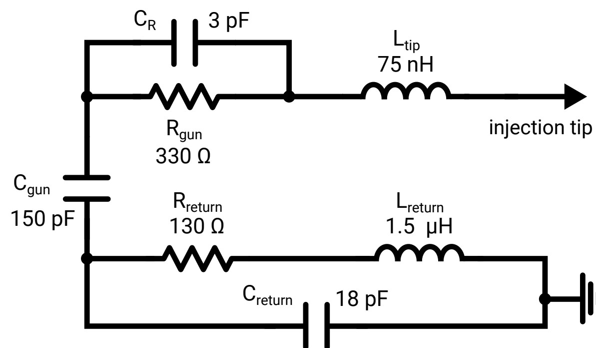

Figure 1.13: ESD Gun model (from Chiu [43])

IEC 61000-4-2 [16] and ISO 10605 [17] are system-level standards, targeting different fields of application. IEC 61000-4-2[16] standard targets consumer electronics. ISO 10605[17] standard is intended for automotive equipment. It defines additional pulse

waveforms to cover a wider range of ESD events (See fig 1.14). Each pulse is generated with a different discharge network. Instead of the usual 150 pF and 330 Ω values, all combinations with 330 pF and 2 kΩ are also possible.

The Human Metal Model (HMM) [44] specification aims to adapt those system-level standards for component-level testing. The pulse waveform remains identical, but a few modifications concerning the injection setup are proposed. Most notably, the ground return of the gun is connected directly to the ground of the device, rather than the Earth. The specification is standardized under ANSI/ESD SP5.6-2009 [44].

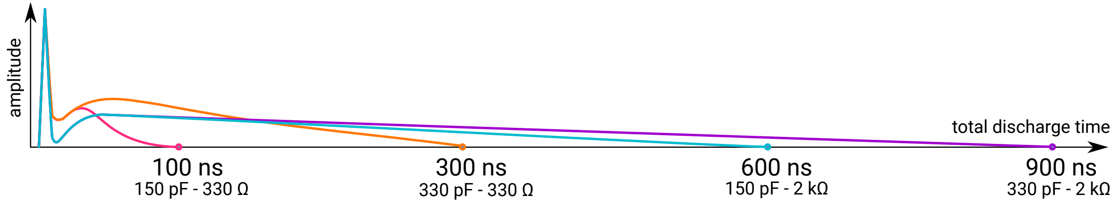

Figure 1.14: Waveforms defined in ISO 10605 standard on a 2 Ω resistive load

ISO 10605 introduces the concept of performance classes for categorizing the robustness of powered-on electronic systems in operation against electrical disturbances. Classes are defined from A to E, with A describing systems that are the more immune to the test. Class E corresponds to the worst severity, where the electronic device did not survive the test. Table 1.2 details the conditions specified for each class.

1.2.3 ISO 7637-2

ISO 7637-2[45] is an automotive standard for testing immunity of electronic devices against transient electrical disturbances. It reproduces disturbances applied on supply lines, when the battery of a car is disconnected for instance. This standard defines several waveforms. Among them, pulses 2A and 3B are the closest to an electrostatic discharge.

Pulse 2A simulates the sudden disconnection of a load placed in parallel with the device under test. In a car, it reproduces the switching of devices separated by inductive wiring harnesses. When a load is abruptly switched off, the inductance opposes to the sudden interruption of current. Instead of flowing through the load, the current is maintained and reported onto the Device Under Test (DUT) which can be damaged or disturbed in the process. These events can be quite harmful with peak voltages above 50 V during 50 µs. This pulse can be an interesting testing waveform in the context of this entire document. The characteristics of pulse 2A are given in fig. 1.15.

The ISO 7637-2 standard does not enforce how stress generators must be constructed or modeled. A compliant generator can be implemented with a resistor-capacitor discharge network. By tuning both values, it is rather straightforward to produce the standardized waveform. It should be noted though that the behavior of an RC network is quite different from an actual inductive load disconnection. However, as long as the

Immunity class	Definition
A	All functions of a device or system perform as designed during and after exposure to interference.
B	All functions of a device/system perform as designed during exposure; however, one or more of them may go beyond the specified tolerance. All functions return automatically to within normal limits after exposure is removed. Memory functions shall remain class A.
C	One or more functions of a device or system do not perform as designed during exposure but return automatically to normal operation after exposure is removed.
D	One or more functions of a device or system do not perform as designed during exposure and do not return to normal operation until exposure is removed and the device or system is reset by a simple "operator/use" action.
E	One or more functions of a device or system do not perform as designed during and after exposure and cannot be returned to proper operation without repairing or replacing the device or system.

Table 1.2: Electronic systems performance classes from ISO10605

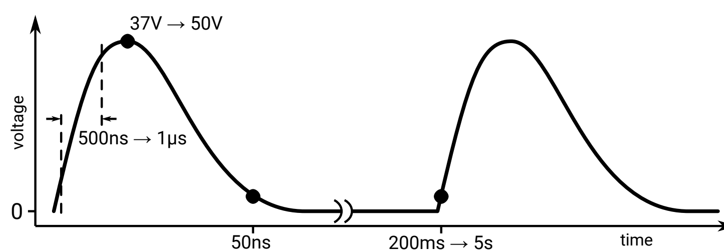

Figure 1.15: Waveform 2A defined in ISO 7637-2 standard on a $2\,\Omega$ resistive load

generated waveform follows the amplitude criteria defined in the standard the generator is considered compliant.

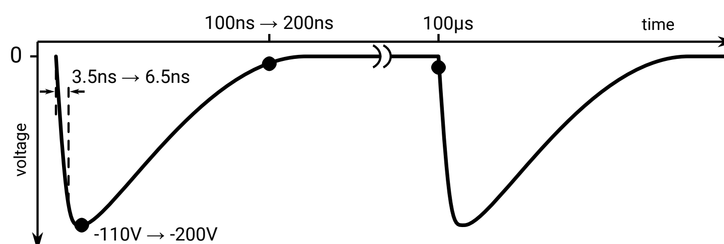

Figure 1.16: Waveform 3B defined in ISO 7637-2 standard on a $50\,\Omega$ resistive load

Pulse 3B simulates the result of a switching process on a wiring harness, causing negative spikes on a DUT. Its waveform is given in fig. 1.16. Compared to pulse 2a, this waveform has a shorter duration and risetime and a higher amplitude. Interestingly, it is one of the rare ESD waveforms to be defined on a 50 Ω load.

A few papers [46, 47, 48] studied the impact of those waveforms on integrated ESD protections. Automotive equipment manufacturer are required to qualify products against ISO 7637-2, to guarantee they can survive the vicinity of other electrical modules in the car such as ignition systems. Therefore, it is relevant to test functional robustness of devices against this standard.

The VDA FAT-AK30 working group on simulation of mixed-systems with VHDL-AMS [49] has worked on modeling all ISO 7637-2 generators. They have provided open-source models of all pulses defined in the standard, as part of the *vdalib* library [50]. For instance, VHDL-AMS model of pulse 3B is provided in Listing 1.1.

```
architecture IDEAL of ISO_7637_PULSE3B is
  constant UA0 : REAL := 0.0;
  constant D2 : REAL := LOG(10.0)/(TD-TR);
  type   STATE_TYP is (S0, S1, S2, S3);
  signal STATE  : STATE_TYP := S0;
  signal TSTART : REAL      := 0.0;
  signal ACTIVE : BOOLEAN   := FALSE;
  signal ACTIVE_CTRL : BOOLEAN;
  quantity VSW across ISW through EL_1 to EL_2;
  quantity V   across I   through EL_1 to EL_2;

begin
  process is
  begin
      STATE  <= S0;
      TSTART <= NOW;
      wait for INIT_DELAY;
      loop
        for I in 0 to INTEGER(T4/T1) loop
          STATE  <= S1;
          TSTART <= NOW;
          wait for TR/0.8;
          STATE  <= S2;
        TSTART <= NOW;
          wait for T1-TR/0.8;
      end loop;
      STATE  <= S3;
      TSTART <= NOW;
      wait for T5;
      end loop;
```

```
  end process;

  if ACTIVE use
     case STATE use
       when S0 => V == UA0+RI*I;
       when S1 => V == US*REALMAX(0.8/TR*(NOW-TSTART),1.0)+UA0+RI*I;
       when S2 => V == US*EXP(-D2*(NOW-TSTART))+UA0+RI*I;
       when S3 => V == UA0+RI*I;
       when others => V == UA0+RI*I;
     end case;
  else
     I == 0.0;
  end use;

  process (S_IN, STATE) is
  begin
     if (S_IN = '1' or S_IN = 'H')
         and (STATE = S0 or STATE = S3)
         and ACTIVE = FALSE then
         ACTIVE <= TRUE;
     end if;
     if not (S_IN = '1' or S_IN = 'H')
         and (STATE = S0 or STATE = S3)
         and ACTIVE = TRUE then
         ACTIVE <= FALSE;
     end if;
  end process;

  ACTIVE_CTRL <= not ACTIVE_CTRL when ACTIVE and STATE'event;

  if ACTIVE use
     ISW == 0.0;
  else
     VSW == 0.0;
  end use;

  break on ACTIVE, ACTIVE_CTRL;
end architecture IDEAL;
```

Listing 1.1: Open-source VHDL-AMS model of ISO7637 pulse 3B - Copyright VDA/FAT

1.2.4 IEC 61000-4-4

The IEC 61000-4-4 standard [51], also called burst test, defines an electrical fast transient for ESD testing. It defines a test waveform, generator and procedures for assessing susceptibility of electronic devices subjected to transient disturbances such as interruption of inductive loads and relay contact bounce. It concerns all kinds of inputs such as supply, signal and control lines. This standard applies to any field of application and is not specific to one.

The defined waveform is a double exponential pulse 1.17 with a width of 50 ns at 50 % of the peak amplitude. Risetime is comprised between 3.5 ns and 6.5 ns. It is defined for a 50 Ω load, with a pulse period of 15 ms and a burst period of 300 ms.

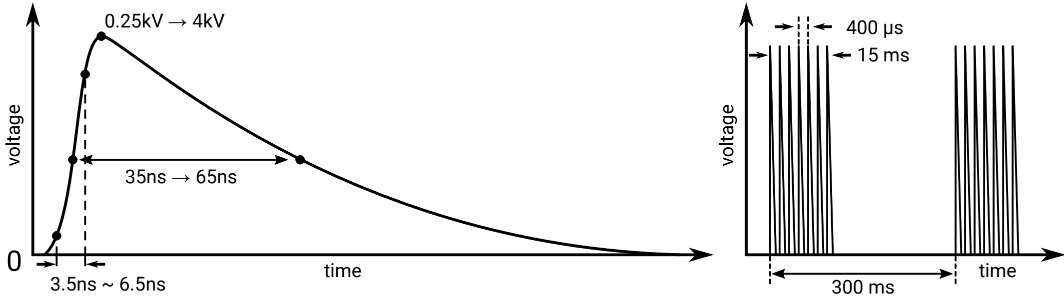

Figure 1.17: IEC 61000-4-4 waveform on a 50 Ω resistive load

The standard defines a circuit diagram for the generator (Fig 1.18). The discharge is produced by a resistor-capacitor R_C-C_C network and initiated by a spark-gap. A spark-gap consists in two conductive tips separated by a gap. When voltage across the gap becomes superior to the breakdown voltage, a spark appears and resistance of the spark gap suddenly drops, allowing discharge current to flow through. In Fig. 1.18, R_s, R_m and C_d shape the waveform. R_s defines the duration of the pulse, R_m performs an impedance matching and C_d act as a D.C. block. The generator's output is a coaxial plug to prevent radiated emission during the discharge.

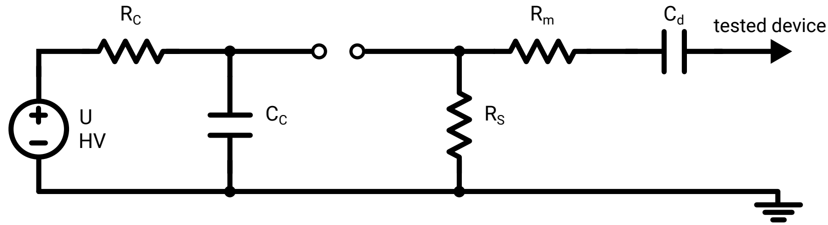

Figure 1.18: IEC 61000-4-4 generator circuit diagram

A particular injection method for powered lines called a *capacitive coupling clamp* (Fig. 1.19) is defined in this standard. This injection system is interesting for performing repeatable injection into powered supply lines. The clamp is constituted of two large

metallic plates. The upper plate has the shape of a tunnel, where the wires receiving go through. The discharge is injected in the upper plates. The bottom plate is connected to the ground of the discharge generator. Thanks to this design, the shape of the wires and the entire setup is well controlled. Although originally designed to work with the IEC 61000-4-4 waveform, the capacitive coupling clamp accepts coaxial cables and any kind of stress generator can be employed instead.

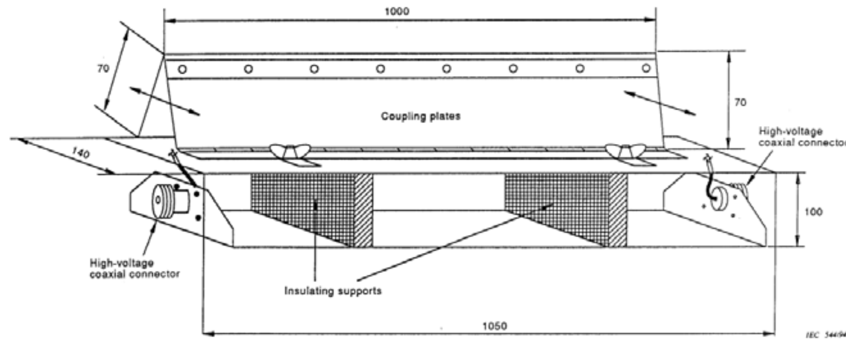

Figure 1.19: IEC 61000-4-4 capacitive coupling clamp

1.2.5 IEC 62215 standard

The IEC 62215 standard [52] defines a method for measuring the immunity of an integrated circuit to conducted electrical transient disturbances. It specifically targets testing of integrated circuits in operation. Instead of specifying test pulses, this standard defines a way to inject stresses suitable for integrated circuits. For automotive devices, the standard specifies the use of waveforms from ISO 7637-2 [45]. IEC 61000-4-4 [51] or IEC 61000-4-5 are required for industrial and consumer applications. Ultimately, the goal is to understand and classify interactions between a conducted disturbance and performance degradation induced in integrated circuits. The test method resembles the Direct radio-frequency Power Injection (DPI) technique defined in IEC 62132-4 [53]. The DPI standard focuses on frequency domain immunity, while this standard tests time-domain immunity.

Disturbances are applied to the IC pins via a coupling network, that isolates the stress generator and the D.C. supply from one another. A typical pin injection setup is given in Fig. 1.20.

Beyond test setup and waveforms, the standard defines immunity classes (see Table 1.3) to categorize the behavior of integrated circuits exposed to disturbances. It is a direct adaptation of performance classes defined in Annex B of ISO10605 and presented previously in Table 1.2. Classes range from A to E. A describes devices that are completely unaffected by the testing procedure and maintain their entire functionality. B describes a short time degradation of internal signals. It is not applicable for integrated circuits, where internal signals are most of the time not accessible. C is identical to

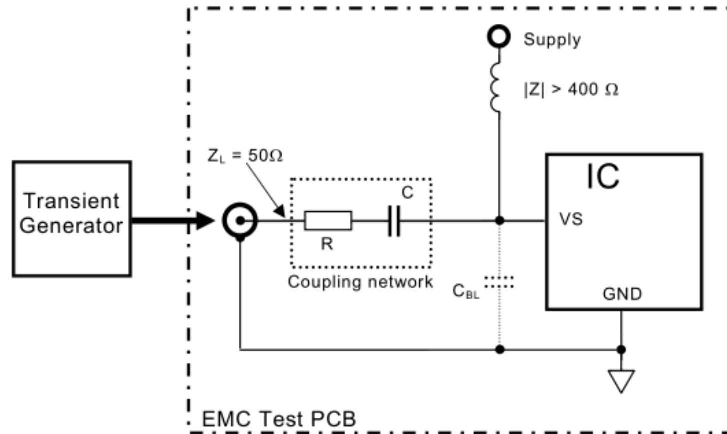

Figure 1.20: Typical injection setup via a coupling network

A, with the difference that failures can occur internally inside the chip, as long as they remain internal to the circuit and do not affect the final application. Finally, D and E describe actual cases of failure, with E representing a hard-failure.

Immunity class	Definition
A_{IC}	All monitored functions of the IC perform within the defined tolerances during and after exposure to disturbance.
B_{IC}	Short time degradation of one or more monitored signals during exposure to disturbance is not evaluable for IC only. Therefore this classification is not applicable for ICs.
C_{IC}	All monitored functions of the IC are within the defined tolerances before and after exposure to disturbance.
D_{IC}	At least one monitored function of the IC does not perform within the defined tolerances during exposure and does not return to normal operation by itself. The IC returns to normal operation by simple action (e.g. reset).
E_{IC}	At least one monitored function of the IC does not perform within the defined tolerances after exposure and can not be returned to proper operation.

Table 1.3: IC performance classes from IEC62215

1.3 Review of soft-failure silicon-level investigation

In previous sections, major ESD standards used in laboratories were presented. The impact of electrostatic discharges on electronic devices has been detailed, highlighting two classes of failures. Hard-failures are well known and multiple protection strategies exists, from external devices and ESD protections, to distributed protection architectures and much more. Soft-failures are the kind of issue caused by electrical fast transients. When discharges propagate inside electronic equipments and reach integrated circuits, they can cause them to malfunction. For multiple reasons described in previous sections, it is essential to detect early functional weaknesses. This section is a review the literature of the current state of the art on ESD induced soft-failure analysis. Study cases, observation methods and modeling approaches are presented.

1.3.1 Case studies

N. Lacrampe presents a functional failure case in [7]. Very-fast TLP is injected on an 0.18 µm CMOS technology (1.8 V supply voltage) testchip. The chip contains 6 instances on the same logic core, differing only by their power-rails architecture. The injection on power rails is performed using a D.C. block 1 nF capacitor, similarly to the DPI standard [53]. An output signal of the logic core is monitored. The susceptibility criteria is the amplitude crossing a 20 % threshold from the established logic level. Above this threshold, the core is supposed to no longer work reliably. It is proven that modeling the output buffer of the core logic is enough for reproducing with less than 20 % error the waveform on the output. It is less accurate than a full-netlist simulation, but faster to simulate. VHDL-AMS and SPICE modeling are performed in this analysis.

In [9], soft-failures are studied on a SDRAM memory in operation. The injection setup consists of a modified compact Transverse Electro-Magnetic (TEM) cell 1.21 with a reduced septum height. Reduced dimensions result in increased field strengths, to reach levels normally produced by an ESD gun. The discharge waveform, injected inside the cell, is generated by a filtered TLP and is similar in shape to IEC 61000-4-2 [16]. The SDRAM chip is mounted on a board. Data is written and read on the memory by a Field Programmable Gate Array (FPGA). Differences between incoming and outgoing data signifies a functional failure of the memory. Only the memory is exposed to the disturbance, the rest of the board's devices are located outside of the TEM cell, on the other side of the board. The main defect of this method is to only provide a global failure level. It does not allow to identify which particular net or pin is the most sensitive to disturbances.

B. Orr reports in [11] errors caused by electrostatic discharges on two different camera communication buses. Events of different severities are observed, depending on the discharge parameters. It is attempted to determine whether the sensor or the application processor is causing the error. The magnetic emission map is recorded with a near-field magnetic scanner to try to observe local variations in the emission spectrum because of the degradation of functionality. It was envisioned that soft-failure can induce significant variations in the emission spectrum of a disturbed component, and thus those variations

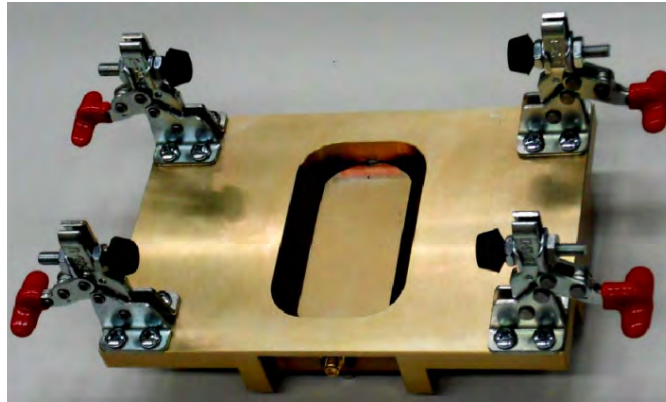

Figure 1.21: Modified TEM cell from [9]

could help localize them. In this particular case, the root cause of failures could not be determined.

An LCD display is studied in [54]. The device is tested with an IEC 61000-4-2 [16] generator, and non-destructive problems are observed due to the discharge. Electromagnetic disturbances cause stripes to appear on the display, optical parameters changes and black-lighting malfunctions. System-level testing waveforms were found too complex for identifying the root cause. A near-field injection is performed to identify which trace of the LCD's flex connector claims the lowest immunity. The lack of resolution of the near-field probe caused multiple traces to be disturbed at once, preventing this second approach to work. Finally, the individual track stressing was repeated with a capacitively-coupled TLP on each individual metal track. However, results were once more inconclusive and no metal trace could categorically be identified as more sensitive than the others. The conclusion for this paper is that silicon level soft-error models are required for standard investigation.

An investigation method is presented in [55] to search for discharge propagation paths responsible for soft-failures on a mobile phone. The IEC 61000-4-2 standard is chosen as testing waveform. Metallic parts are assumed to be the main propagation paths. To confirm this hypothesis, time-domain electromagnetic field 3D simulations of almost the entire phone are ran (see Fig. 1.22) After the failure location was determined, RC-networks are used as countermeasures to protect physical inputs and outputs, like buttons, LCD inputs and connectors.

K. Abouda details in [56] a case of soft-failure on an integrated automotive regulator IC. The failure signature is a loss of the regulated voltage when exposed to Bulk Current Injection (BCI) ISO11452-4 [57]. The test setup is provided in Fig. 1.23. The product is investigated manually, by searching inside the design for coupling and propagation paths, and performing multiple simulations. Eventually, it was proven that a residue of the disturbance was coupling through the substrate on a current mirror inside the bandgap reference. During the disturbance, bandgap voltage was shifting from its nominal value. After some delay, the bandgap output was reaching an undervoltage threshold, causing

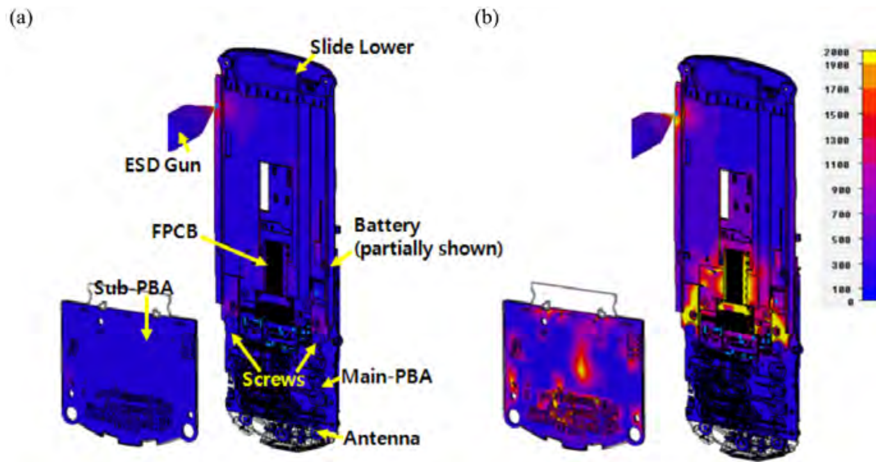

Figure 1.22: ESD Current Distribution on Mobile Phone and Backside sub-battery pack at (a) 1.0 ns and (b) 1.8 ns (Credit: [55])

the entire system to restart. To avoid it, a design fix was proposed by filtering at the appropriate spot inside the design to avoid the amplification of the disturbance.

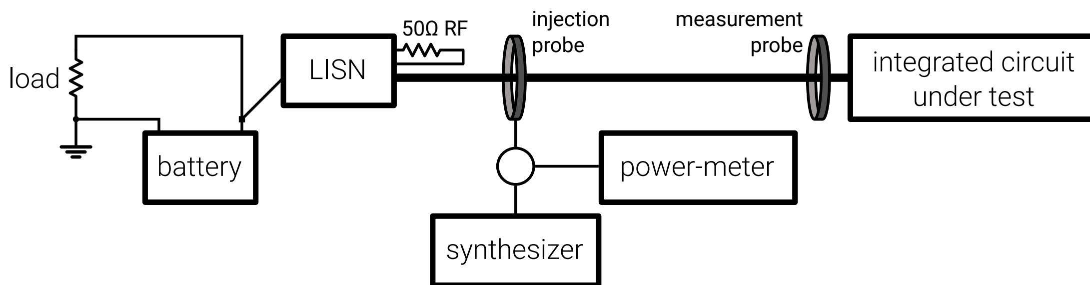

Figure 1.23: Bulk Current Injection setup

In summary of the case studies, multiple soft-failures of integrated circuits were studied. They involved core CMOS logic, SDRAM memories, video processors or multimedia devices failing to work temporarily, detected by raising a flag, display issues and communication errors. Overall, it was demonstrated that it remains highly difficult to identify the root cause of the failure, especially without access to the design of the chip. A multitude of tools has been employed throughout the studies, such as near-field injection and scan, modified TEM cells, SPICE and electromagnetic simulations and modeling languages such as VHDL-AMS. Ultimately, it seems that access to the silicon design is essential to debug the problem and fix, as was shown successfully in [56]. All these conclusions call for new investigation methods at silicon level, and modeling method for enabling system level simulations without disclosing intellectual property. The new methods and tools presented in this document aim to solve exactly this kind of issues.

1.3.2 Observation methods

F. Caignet proposes in [58] an on-chip measurement technique capable of recording ESD waveforms with a 20 GHz bandwidth. It relies on equivalent-time sampling for measuring waveforms with a much larger bandwidth that real-time oscilloscopes. Equivalent time-sampling works exclusively with repeatable or periodic signals. A real-time oscilloscope takes a complete waveform constituted of N samples in a single shot. On the other hand, a time-equivalent sampler measures waveforms point by point, and require N repetitions of the waveform to acquire the N samples. The process for acquiring the data is the following. A first waveform is shot, and the sampler only records its value at $t = 0$. A second waveform is shot, and the sampler records the value at $t = \Delta t$. At the third waveform, the recording is at $t = 2\Delta t$. The process is repeated while increasing the sampling delay by Δt at each step until enough points were acquired. This approach is interesting because it reduces a lot the constraints on the measurement system, while offering a huge bandwidth. The main disadvantage is that it requires as many measurements as the amount of points needed. In [58], the sampler was designed using a CMOS 65 nm technology and embedded into a testchip. Architecture is given in Fig. 1.24.

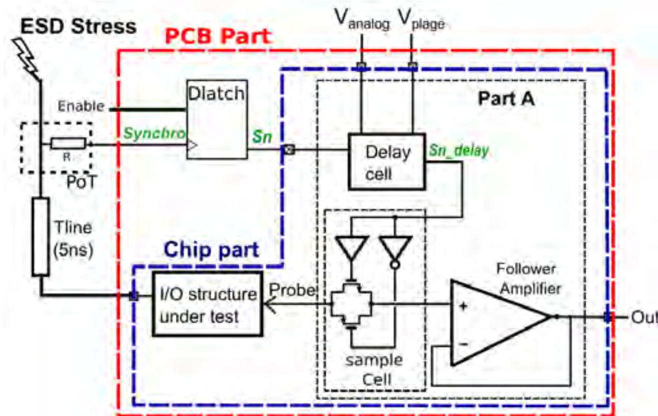

Figure 1.24: Equivalent time-sampler architecture from [58]

Other techniques exist in similar fields that could prove useful for ESD investigation. M. Nagata details in [59] an on-chip measurement technique for recording substrate noise waveforms at silicon level. Injection and measurement structures are directly integrated into a 0.4 µm CMOS technology test vehicle. The injection structures consists in a controllable noise source. The amount of logic elements, transition directions and delays can be selected to generate different noise waveforms. By coupling, the substrate receives a part of this disturbance. The sensor consists in a latch comparator 1.25. With a few synchronization signals, it is sufficient to record waveforms with a 100 ps time resolution. For ESD, this sampling frequency is almost ideal.

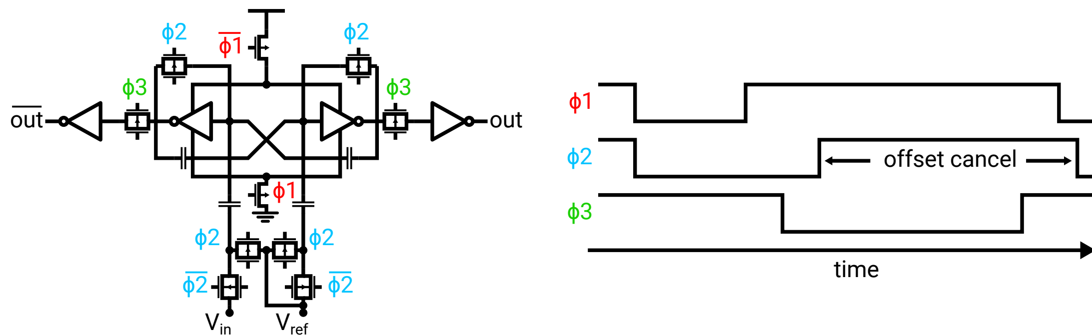

Figure 1.25: Latch comparator and timings for substrate noise detection from []

Emission Microscopy (EMMI)

Emission Microscopy (EMMI) is an observation technique where a camera registers photon emission above semiconductor devices. A device is placed in the field of view of the camera. The entire system is placed inside an enclosure to block out all ambient light. Semiconductor junctions and defects emit photons when electrically excited. By letting the camera shutter open for a long time, between a few hundred milliseconds to tens of seconds, photons generated by this process are detected by the image sensor. As photons accumulate, some sections of the image become brighter than others. Defects can be isolated from normal junctions by comparing recordings performed on tested devices with a reference device. The architecture of an EMMI system is provided in Fig. 1.26.

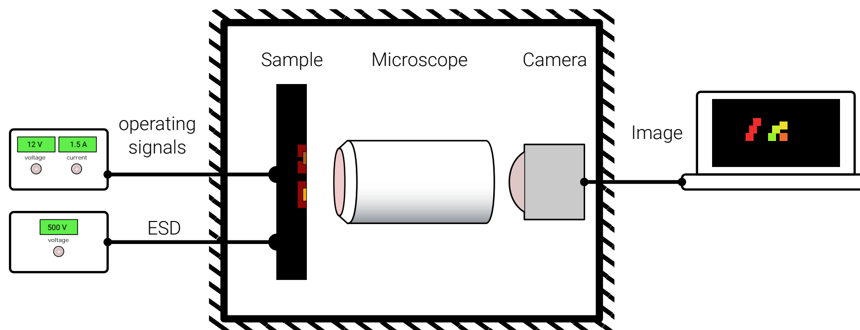

Figure 1.26: Architecture of an emission microscopy testbench

Originally, the combination of EMMI with a TLP discharge was proposed by T. Maloney and N. Khurana in the original TLP paper [34]. Afterwards, EMMI was employed for debugging hard-failures of ESD protections in 3D CMOS technologies [60] or high-voltage silicon technologies [61]. In US patent 6469536 [60], Kessler describes a method to synchronize the ESD injection with the shutter of the EMMI. Finally, EMMI was employed successfully by Besse and Abouda [62, 63, 64] for debugging and tracking down a functional failure inside an integrated automotive product exposed to ESD. In

those last papers, the integrated circuit is powered-on and in normal operation, and the EMMI helps localize soft-failures.

Fig. 1.27 shows two different images recorded with an EMMI bench. The image on the left is the reference image and the one on the right is the signature after a failure.

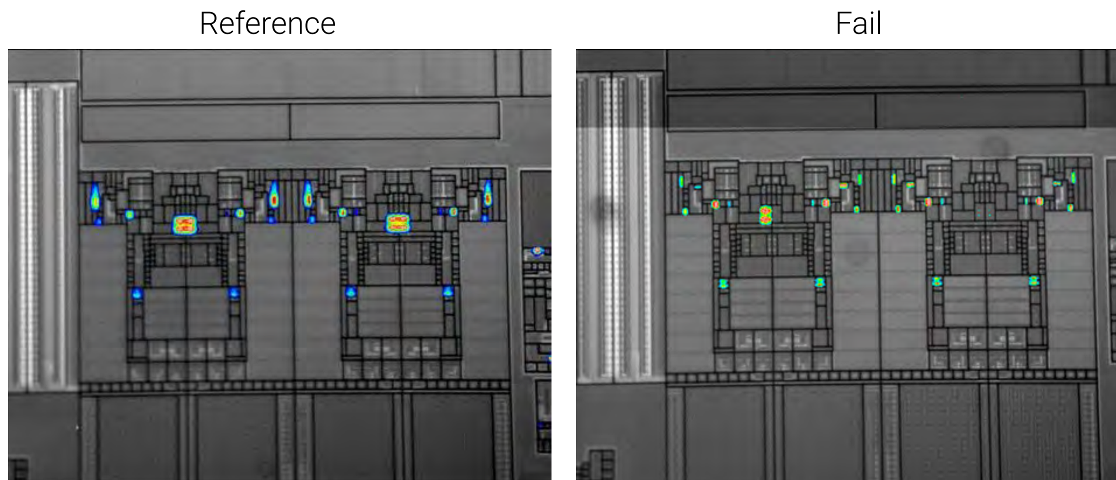

Figure 1.27: Reference and fail EMMI measurement of an integrated function

Near-field scanner

Electromagnetic near-field scanner allows creating maps of electric and magnetic field. An electric or magnetic probe is swept closely above a device to record the emitted field in near-field conditions. Measurements may be carried out in the frequency domain or in the time domain. This tool was initially intended for architectural analysis such as floor-planning and power distribution analysis. For ESD, spatial information provided by the recorded map is very useful to locate failures and malfunctions. A comprehensive and detailed analysis of near-field antennas is done by A.D. Yaghjian in [65]. More recent work details the principle of operation, data processing and hardware requirements in [66, 67, 68, 69]. Finally, measurement of electromagnetic emissions with surface scan method is standardized in IEC TS 61967-3 [70]. The architecture of a near-field scanner is given in Fig. 1.28.

In a near-field scan, the amplitude recorded by the probe depends on many factors. The amplitude measured from the sensor is the result of coupling between the source of emission and the sensor itself. In the case of a magnetic sensor constituted of a loop, the size of the loop, the diameter of the wire, the orientation of the loop and the amount of turns all impact strongly the measured waveform. Those characteristics can be estimated or measured. However, the waveform also depends on other factors harder or impossible to determine. For instance, the height between the emission source (usually a metal track) and the probe and the width of the track affect the coupling ratio. For realistic integrated circuits, there can be a dense network of metal tracks that

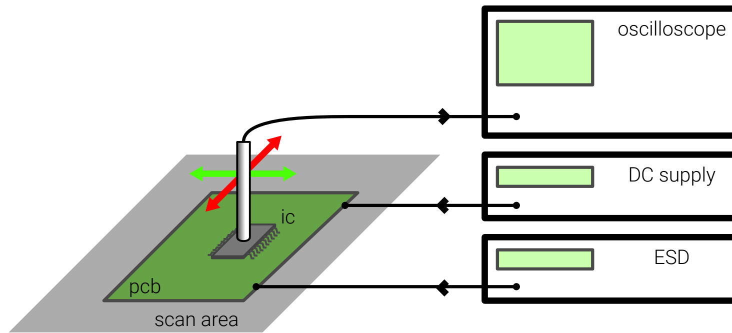

Figure 1.28: Architecture of a near-field scanning testbench

all will emit electromagnetic radiations and couple to the sensor. It is impossible to measure each track independently. Ultimately, determining absolute values of current or voltage inside a particular portion of an integrated circuit is nearly impossible. This is why near-field scanners are more interesting for obtaining relative values between different sections of the circuit. For instance, knowing that the magnetic field above a given structure is ten times greater than another structure is a precious information for understanding ESD propagation.

So far, near-field scans are performed mostly at the PCB level. A new trend is to use scanners for integrated circuits. In current silicon technologies, transistors are a few micrometers long, and metal tracks without power a few micrometers wide as well. This range of dimensions is to compare with the capabilities of current near-field scanners. Spatial resolution of a near-field scanner is not bounded by the 3-axis that moves the probe, but by the probe itself. 3-axis machines can easily be found with a positional accuracy of a micrometer, less than the typical observable structure dimensions on silicon. However, spatial resolution of current near-field probes is more in the range of 100 µm. This value depends mainly on the size of the loop, its diameter and the distance between sensor and source. For integrated circuits, this is not sufficient to isolate and identify structures. In the future, improvements can be expected on the spatial resolution, but it will raise new kinds of challenges. In the case of a probe with a resolution near 1 µm, the amount of points to record to build the map becomes huge. For a 5 mm by 5 mm silicon circuit sampled every micrometer, scanning the entire area requires 2.5 million ESD pulse injection and recordings. No integrated circuit can sustain such an amount of repeated stressing, and the device will be destroyed before the end of the scan. Also, the test time for this brute force approach is going to be very important. If the entire process is automated and a delay of 2 seconds is left between each point, the test campaign will still take 1388 hours, approximately 2 months. With smarter sampling strategies or new measurement methods, near-field scanning could be a valuable tool for silicon-level investigation.

So far, near-field scan has been presented as a measurement tool, but it can also serve as a localized stress injection system. Instead of sensing voltage or current in

the near-field probe, a pulse is injected in it. In [71], a near-field scanner is combined with a very fast TLP. A stress is injected, and the device under test is monitored for faults. A susceptibility map is obtained 1.29, that highlights the most sensitive areas of a board. The paper demonstrates that it is possible to map quantitatively and with good resolution the ESD susceptibility of a board with this method. In a similar approach, ESD sensitive metal tracks and IC pins are identified in [72] using a near-field scanner as an injection system.

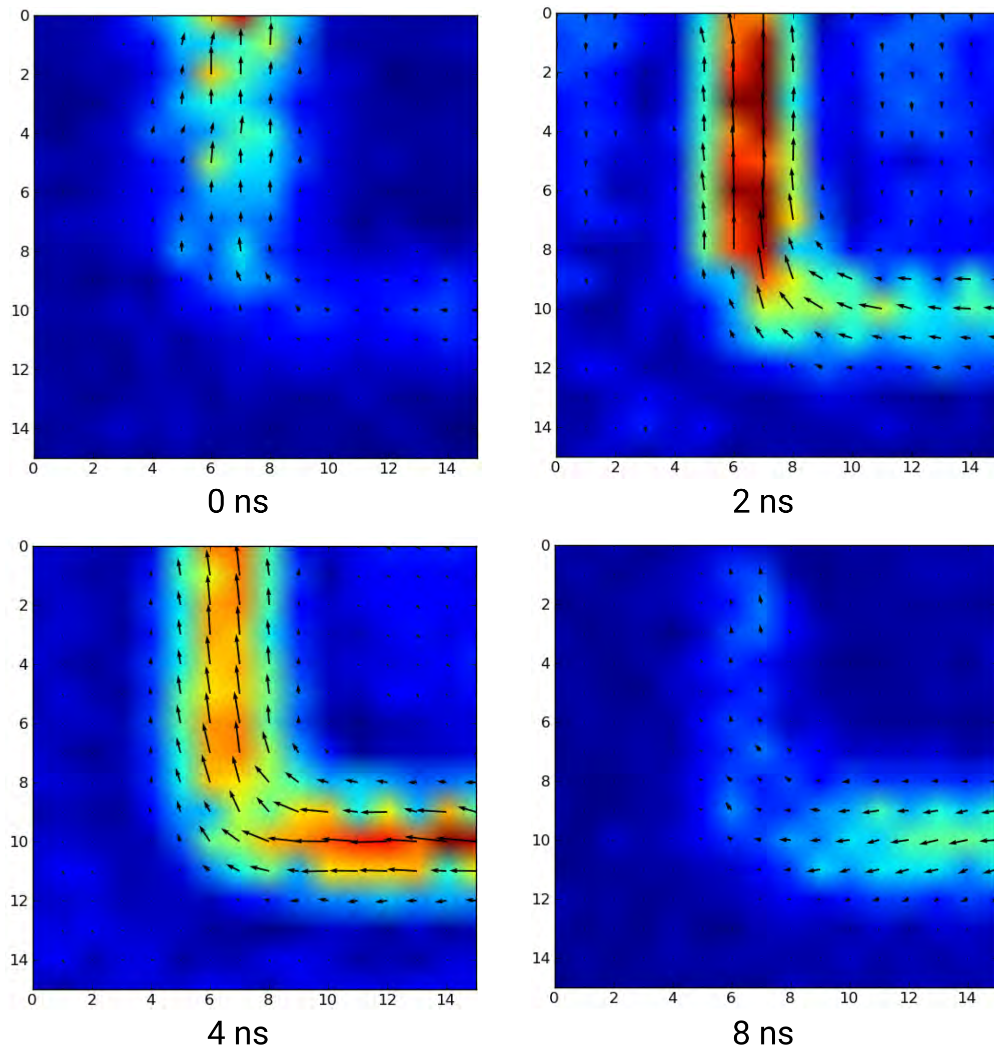

Figure 1.29: Near-field injection susceptibility map [15]

1.3.3 Modeling methods of soft-failures for integrated circuits

In the literature, various ESD modeling methods can be found. They comprise a wide range of techniques such as 3D electromagnetic and semiconductor physics simulations,

compact, behavioral, physically-based and non-linear modeling. The methods described hereafter could be used for soft-failure investigation.

M. Scholz details a mixed-mode ESD simulation approach in [10]. It is a combination of SPICE and Technology Computer-Aided Design (TCAD) models, simulated in SPICE environment. The author indicates that the combination of physical device models and standard simulations provides higher accuracy and more realistic simulations than behavioral SPICE models. Using this complex simulation tool, on-chip and off-chip device interactions are studied, in powered and unpowered conditions.

In [73], TLP characterizations serves as an I(V) model for both external protections and an IC pin. The PCB S-parameters are extracted from the board layout, using Momentum software (Agilent Technology). It is electrically model with lumped R,L,C,G elements. The modeling approach proved successful for simulation interactions between external devices and on-chip structures. This method is interesting for soft-failure analysis because it is thorough and complete and enables accurate ESD simulation.

The Input Output Buffer Information Specification (IBIS) [74] is a behavioral, black-box model for performing signal integrity simulation on digital circuits. It is widespread in the digital Application Specific Integrated Circuit (ASIC) world because it enables accurate simulations without disclosing circuit or process information. It was envisioned that IBIS models could also be used or extended for ESD. It is demonstrated in [75] that the model lacks some parameters for EMC and ESD simulations. It comprises a current versus voltage characteristic of I/Os, similar to what can be extracted by a TLP, however the IBIS model is not defined for fast pulses and high injection.

N. Lacrampe proposes in [7] to perform 3D electromagnetic simulations at silicon level, using the integrated circuit layout, to deduce the amount of capacitive couplings between Vdd and Vss rails. The extraction is performed with HFSS software (Ansoft). The goal of this analysis is to predict the susceptibility of integrated circuits against electrostatic discharges. PCB tracks are modeled by a distributed RLC network. The package data from the IBIS model [74] was used in the simulations. Finally, a TLP stress generator is modeled using a lookup table I(V) component, in series with a $50\,\Omega$ resistor.

Once again, electromagnetic full-wave simulations are conducted in powered-on ESD analysis in [55]. System-level components are simulated, such as PCB, metallic casing and battery pack. 3D EM simulations helps identify the main discharge paths and locate the failure.

Chapter 2

Development of investigation tools

2.1 System-level ESD modeling method

The electronic design world is highly competitive, and especially the automotive field. Companies need to design products as fast as possible, with lowest possible costs, while guaranteeing high levels of quality. On the other hand, electronics systems are complex to design and it is almost impossible to get the design right at the first manufacturing pass. As the project moves forward in the design cycle and reaches new milestones, every redesign and modification becomes exponentially more costly. For instance, modifying properties of a few transistors inside an integrated circuit during the early design phase comes almost for free. It takes a few minutes for a designer to make the changes, and the time required to run the validation simulations. However, if this change is done after a first tape-out, many more steps must be executed. In addition of the modification and simulation time, the top layout of the product must be updated, a new tapeout prepared and a new set of lithographic photo-masks manufactured. After a few months of manufacturing time, and testing time of the new part, the modification is landed. In the process, it has cost a lot of time and manpower to the company. Therefore, to remain competitive, the amount of design-manufacturing phases must be kept to a bare minimum, ideally to a single pass. In this context, any tool capable of detecting early issues, enabling to prevent them before manufacturing, is highly valuable.

Electrical simulations are the corner-stone of modern, computer-aided electronic design. They constitute a fundamental tool used massively in integrated circuit and system development. Silicon-manufacturing companies put a lot of effort to develop highly accurate models of their integrated technologies. In those environments, accuracy of standard analog simulations is rightfully taken for granted. For electrostatic and electromagnetic simulations though, the situation is different. By nature, electrostatic discharges are very fast and highly non-linear signals. Those events occupy a much larger frequency spectrum than waveforms usually met in standard analog simulations. It is essential to verify the accuracy of models and simulations. Models must be validated against

actual measurement data, and in many different test conditions, including powered and unpowered conditions.

In this chapter, a methodology for building electrical ESD models is proposed. It enables simulation of waveforms from the ESD source to an integrated circuit pin. This is a preliminary step for enabling simulation of soft-failures inside the chip. The proposed methodology is modular and offers to reuse models between common devices found in ESD laboratories. A typical ESD test setup comprises equipments such as DC sources, oscilloscopes, and stress generators. Equipments are connected together with wires, coaxial cables, twisted wire pairs, etc. The integrated circuit under test is often soldered onto a printed circuit board. PCBs usually host multiple kind of discrete devices, such as passive devices, ESD protections, common-mode chokes, relays, etc. Components are connected together by metal tracks. The goal of the proposed methodology is to build a library of all those elements, from lab equipments down to tiny discrete components. Each model of the library will be qualified independently with individual characterization and comparison with its model.

After the library is constructed, models can be connected together to simulate the entire system. The topology of the system serves as a blueprint for connecting models.

2.1.1 Transmission line

Cables are critical elements in any ESD test setup. They introduce significant propagation delays in regard of the duration of an electrostatic discharge. A $50\,\Omega$ coaxial cable has a propagation ratio of approximately $5\,\mathrm{ns\,m^{-1}}$. In a laboratory, it is common to find cables of tens of centimeters to a couple of meters long, resulting in delays between 1 ns to 10 ns. As a comparison, the scale of an electrostatic discharge is a few hundred nanoseconds. Both values are near the same order of magnitude and a large impact from cables on the simulation can logically be expected. Cables, microstrip lines, wires and electrical propagation media behave as transmission lines. Transmission lines were originally analyzed by J. Maxwell, L. Kelvin and O. Heaviside and a huge amount of studies on the topic are available in the literature [76, 77, 78, 79].

Cables can also be a source of ringing oscillations if the circuit contains impedance mismatches, which is often the case. Oscillation period is directly related to the cable length. In this situation, a delay even less than 1 ns can have a strong impact on waveforms. Therefore, coaxial cables, long PCB traces and any element that generates a significant delay superior to the nanosecond should be modeled.

Transmission line pulsing was used extensively during this study. As a remainder, it consists primarily in the discharge of a coaxial cable. Thus, proper modeling of coaxial cables is useful in that regard as well.

Transmission lines are characterized by their characteristic impedance, supposedly constant on the entire line. It is determined by its cross-sectional dimensions and constituting materials. For coaxial cables, common characteristic impedances are $50\,\Omega$ or $75\,\Omega$. This value is equivalent to the resistance that could be measured statically between outer and inner conductors for an **infinitely long** transmission line. All transmission lines are lossy, meaning that some part of the incoming power traversing it is dissipated.

In most cases though, losses are very small and negligible, and the line is considered lossless. The behavior of the line is also frequency-dependent. Losses, characteristic impedance and other properties can change above certain frequencies. For frequencies below a GHz, most cables and metal strips can be correctly approximated by a lossless and non frequency-dependent line.

Physically, a transmission line can be seen as a succession of infinitely small unit elements. Each element is modeled by an inductance L, a capacitance C and sometimes a leakage resistance or conductance. Those unit values are directly related to the characteristic impedance Z_c as described in Eq. 2.1. This characteristic impedance is also expressed as the ratio of voltage and current of a single wave propagating along the line.

$$Z_c = \sqrt{\frac{L}{C}} \tag{2.1}$$

Distributed model

The most popular line model in the ESD field is based on lumped capacitance and inductance. The model is a series of lumped L-C networks as illustrated in Fig. 2.1. Values for the element can be computed from the characteristic impedance characteristic impedance with Eq. 2.1.

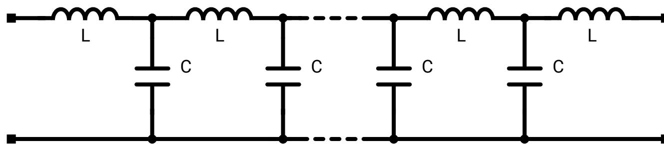

Figure 2.1: Electrical distributed LC ladder model of a lossless transmission line

$$\delta t = \sqrt{L.C} \tag{2.2}$$

Each element induces a propagation delay δt, whose values can be computed from the unit inductance and capacitance with Eq. 2.2. In a string of connected unit elements, the individual delays add up. With enough elements, the delay and behavior of the complete cable is reproduced.

During modeling, it is tempting to take large values for δL and δC, to get a large unit delay. Doing so reduces the amount of unit elements, and speeds up the simulation. However, there is a trade-off between the delay of the unit element and the accuracy of the simulation. A smaller unit delay increases accuracy of the model at large frequencies, but more elements are required for the total cable, resulting in longer simulation times. On the other hand, a larger unit delay reduces the bandwidth of the model, which may be unsuitable for accuracy, even if simulation times are improved.

By resolving the equation system constituted 2.1 and 2.2, it is possible to extract formula for L (Eq. 2.3) and C (Eq. 2.4). Values depend on the characteristic impedance

Z_C, the total cable delay Δt and the amount N of lumped elements in the model.

$$L = \frac{Z_C.\delta t}{N} \tag{2.3}$$

$$C = \frac{\delta t}{N.Z_C} \tag{2.4}$$

The distributed model supports easily lossy transmission lines by adding a unit resistance or conductance between signal and ground, or in series with the signal. On the other hand, this model does not scale well as cables get longer. To keep the same bandwidth with a longer cable, the only solution is to increase the element count, resulting in longer simulation time. Also, this model will always be bandwidth limited, otherwise it would require an infinite amount of infinitely small elements.

Two-port network model

The two-port network model described by H. Branin [76] is a much better alternative to the distributed model. It can describe efficiently and with great accuracy the behavior of uniform lossless transmission lines. The model is constituted of two voltage-controlled voltage sources and two resistors (Fig. 2.2). Compared to the distributed model, the behavioral model has by design an infinite bandwidth, and is extremely fast to simulate. It also is constant in complexity, because the simulation time is independent of the cable's delay or required bandwidth

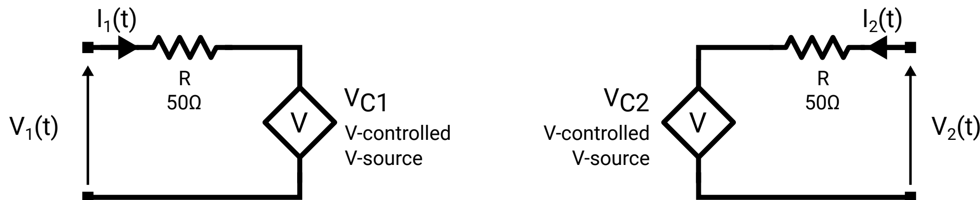

Figure 2.2: Electrical behavioral model of a lossless transmission line

Equations 2.5 and 2.6 describe the behavior of the voltage-controlled voltage sources.

$$V_{C1}(t) = V_2(t - \Delta t) + Z_C.I_2(t - \Delta t) \tag{2.5}$$

$$V_{C2}(t) = V_1(t - \Delta t) + Z_C.I_1(t - \Delta t) \tag{2.6}$$

Z_C is the characteristic impedance of the line and Δt the propagation delay between both ports. Overall, the equations describe a system where voltage and current at both ports are defined by the combination of a forward traveling wave and a backward traveling wave. An example of implementation in VHDL-AMS is provided in Listing 2.1.

```vhdl
library IEEE;
use IEEE.ELECTRICAL_SYSTEMS.all;

-- Entity
entity TLINE is
  generic (
    Z0 : REAL;
    TD : REAL := REAL'LOW;
    IC_V1 : REAL := 0.0;
    IC_I1 : REAL := REAL'LOW;
    IC_V2 : REAL := 0.0;
    IC_I2 : REAL := REAL'LOW
  );

  port (
    terminal N1 : ELECTRICAL;
    terminal N2 : ELECTRICAL;
    terminal N3 : ELECTRICAL;
    terminal N4 : ELECTRICAL
  );

begin
  assert TD > 0.0 or TD = REAL'LOW
    report "TD > 0.0 required."
    severity error;
end entity TLINE;

-- Architecture
architecture behavioral of TLINE is
  -- Voltages and currents at each port
  quantity V1 := IC_V1 across I1 through N1 to N2;
  quantity V2 := IC_V2 across I2 through N3 to N4;

  quantity ES, ER : REAL;

  -- Delayed quantities
  quantity V1_DEL, V2_DEL : REAL;
  quantity ER_DEL, ES_DEL : REAL;

begin
  -- DC conditions
  if DOMAIN = QUIESCENT_DOMAIN use
```

```
    V1 == V2;
    I1 == -I2;
    ER == Z0*I1 + 2.0*V2 - V1;
    ES == Z0*I2 + 2.0*V1 - V2;

    V1_DEL == V1;
    V2_DEL == V2;
    ER_DEL == ER;
    ES_DEL == ES;
  -- TRAN conditions
  else
    V1 == Z0*I1 + 2.0*V2_DEL - ER_DEL;
    V2 == Z0*I2 + 2.0*V1_DEL - ES_DEL;
    ES == 2.0*V2_DEL - ER_DEL;
    ER == 2.0*V1_DEL - ES_DEL;

    V1_DEL == V1'DELAYED(TD);
    V2_DEL == V2'DELAYED(TD);
    ER_DEL == ER'DELAYED(TD);
    ES_DEL == ES'DELAYED(TD);
  end use;
end architecture behavioral;
```

Listing 2.1: Transmission line behavioral VHDL-AMS model

Comparison

Simulations are run to compare both models. The expected theoretical response is a perfectly rectangular waveform measured at the load, because the transmission line is ideal and the load purely resistive. The setup is given in Fig. 2.3 and consists in injecting a rectangular pulse with a risetime of 1 ps into a load through the modeled transmission line. Different load values are employed to observe the performance and accuracy of each model. The transmission line to model has been chosen to a delay of 100 ns and a characteristic impedance of 50 Ω. Both values correspond to the cable usually employed in a transmission line pulsing generator and are thus very realistic.

Overall, the behavioral model outperforms the distributed model for representing a perfect transmission line. It reproduces exactly the 1 ps risetime on the load in all configurations (Fig. 2.4). The distributed model is either not as accurate or much slower to simulate.

For good accuracy, individual delay must be 2 or 10 times smaller than the shortest rise time. Also, simulators with variable timestep have trouble reproducing properly oscillating events. Simulated period is often wrong compared to what is mathematically expected. Oscillations also force the simulators to fall back to the smallest timestep,

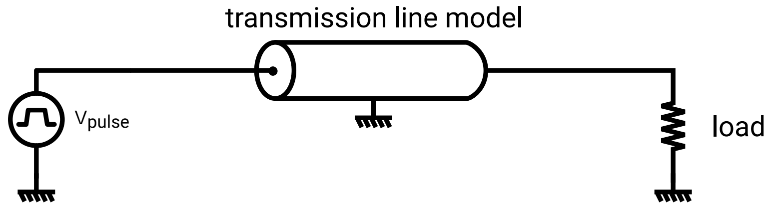

Figure 2.3: Line model validation testbench

amount N	10	100	1000	10000
simulation time	15 ms	170 ms	7.5 s	135 s
increase ratio	-	x10	x44	x18

Table 2.1: Impact of the amount of unit elements on the simulation times (the 2 port model has a constant simulation time of about 20 ms)

considerably increasing simulation times. To simulate a 100 ns TLP with a 100 ps rise-time using the distributed model, it would require unit elements with a delay of 10 ps. It means that 10000 elements are required to model the line, which is rather important and increases simulation time. Even with such a large amount, oscillations are still visible at high frequency in the simulation as shown in Fig. 2.4 and the risetime is not accurate.

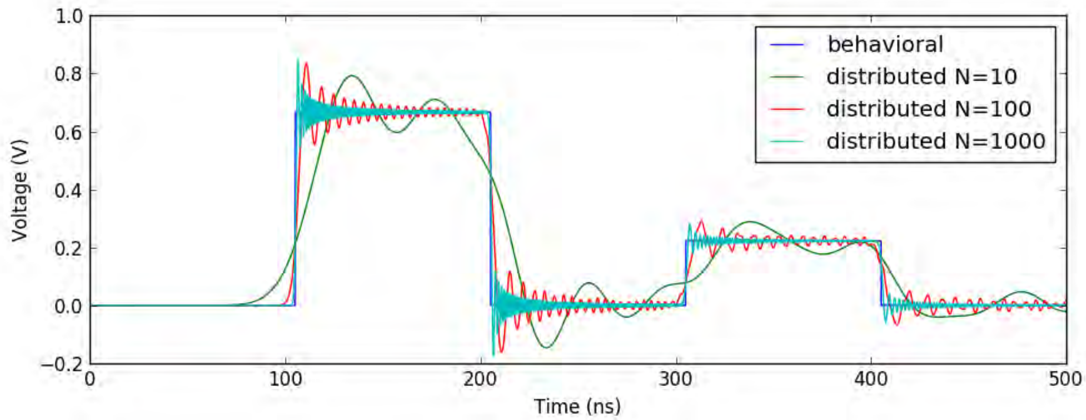

Figure 2.4: Lumped versus two-port models comparison in simulation (charging voltage 1 V)

In conclusion, the two-port model should always be preferred over the lumped model. This is obviously the approach used for all transmission line modeling presented in this document.

2.1.2 Passive devices

Discrete passive devices are the most common kind of devices found on PCB. Capacitors, inductors and resistors logically impact ESD waveforms. Their properties change at high frequencies and high-power levels of electrostatic discharges [80]. Nominal values easily vary by an order of magnitude. At frequencies above a few MHz, parasitic devices of any discrete component cause a degradation of performance. For sufficiently large frequencies, the parasitic device can prevail over the nominal function. This is how a capacitor can exhibit an inductive behavior above its resonance frequency.

The frequency content of an electrostatic discharges was characterized in [81]. The study focused on air discharges and non-shielded discharges that radiate heavily. In particular, the spectrum of the IEC 61000-4-2 standard [16] was recorded. It is shown that the majority of the frequency content is below 1 GHz, with important magnitude until tens of MHz. This corresponds to the frequency range where parasitic behavior becomes important. Therefore for ESD simulations, passive devices require models that take those parasitic devices into account.

In practice, it was found that only some passive devices in a system have a notable impact on the waveform at high-frequencies. For others, using a regular electrical model is sufficient. Decoupling capacitors were noticed to require parasitic device modeling. Since they are connected between a voltage reference (supply voltage) and a reference (ground), they have a strong impact on the disturbance waveforms that an IC pin is exposed to. Passive device models working at frequencies below 1 GHz are given in Fig. 2.5 for inductors, resistors and capacitors. The parasitic devices are represented in orange.

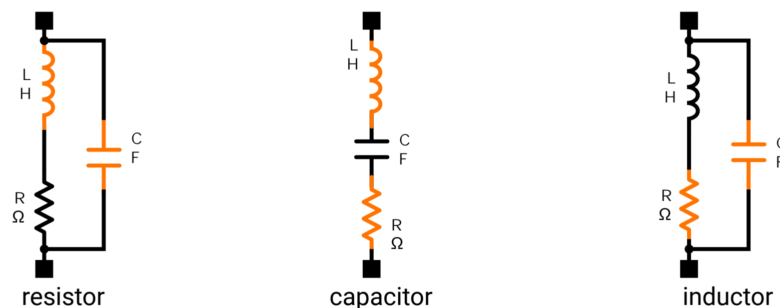

Figure 2.5: High-frequency (up to 1 GHz) models for resistor, capacitor and inductor

Those models are easily parameterized. Values can be extracted with an impedance meter capable of measuring impedances to at least 100 MHz. The extraction is performed in small-signal conditions, which can be an issue as will be later detailed. Fig. 2.6 displays the magnitude and phase versus frequency of a 6.8 nF Surface Mount Device (SMD) capacitor. The capacitor exhibits a perfect behavior up to 45 MHz. The slope of the curve below 45 MHz is negative and is a function of frequency and the capacitor value. The capacitor value can be computed with Eq. 2.7 obtained from capacitor

theory. Below 45 MHz, the phase has a value of −90°, corresponding to the theory.

$$C = \frac{1}{2\pi.f.|Z|} \tag{2.7}$$

At the resonant frequency, the capacitor is equivalent to a non-ideal short-circuit, basically a low-value resistor. This resistor, also called Equivalent Series Resistor (ESR), is both a parasitic device and the series resistance in the high-frequency model presented earlier. Beyond 45 MHz, the capacitor behaves as an inductor. The phase shift is the one of an inductor at 90°. This second slope is positive and a function of frequency and inductor value. The inductor value can be computed with Eq. 2.8. In conclusion, the values for parasitic inductor and resistor can be computed very easily from a measurement.

$$L = \frac{|Z|}{2\pi.f} \tag{2.8}$$

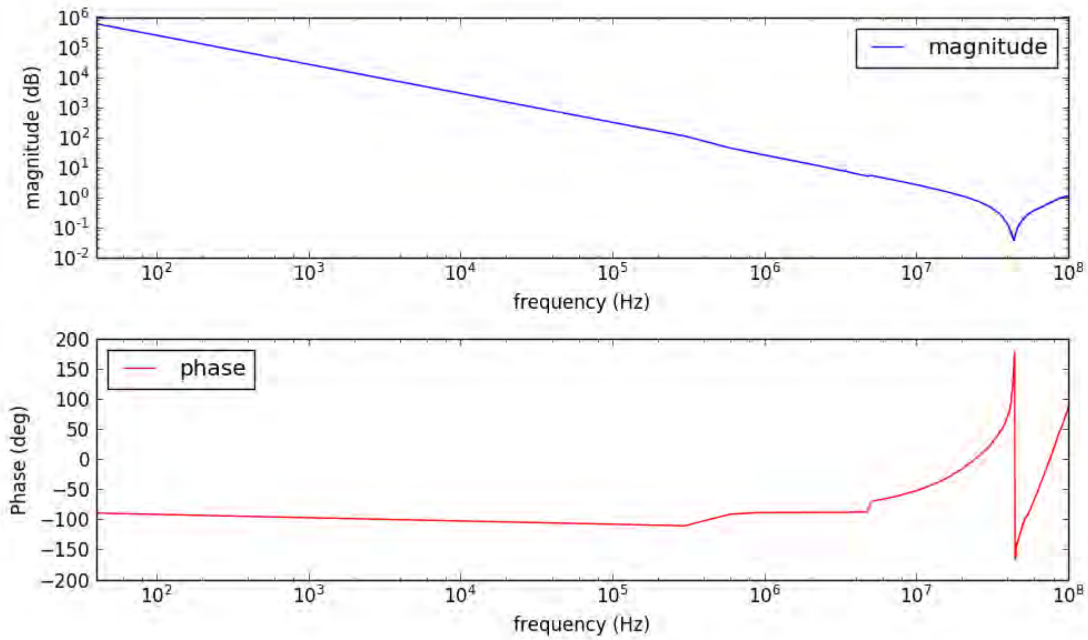

Figure 2.6: Magnitude and phase frequency response of a 6.8 nF capacitor

So far, only the frequency-related behavior was detailed. For high power and amplitudes, most passive devices also suffer of nominal ratings variations. Multi-Layers Ceramic Capacitors (MLCC) are concerned about this phenomenon [80], where the capacitance decreases at high voltages. On the contrary, capacitors built with the X7R technology are much most resilient in high regime conditions and exhibit little variations [82].

Parasitic device modeling for passive devices is a pretty common technique in high-frequency, EMC and ESD simulations. For ESD, using parasitic models is not systematically required, but it is an important tool to remember when building a system model. There is still room for model improvement, with MLCC capacitors at high-regime regime for instance.

2.1.3 ESD protections

ESD protection is the most extensively studied device in the ESD field. ESD protections designate a class of devices rather than a particular electronic component. ESD protections can be realized in multiple ways, with diodes, thyristors, Transient Voltage Suppressor (TVS), silicon-controlled rectifiers, etc. Overall, ESD protection are devices in high-impedance below a triggering voltage, low-impedance above it and capable of absorbing significant amount of currents temporarily. Overall, there are two kinds of modeling methods with physically-based models and behavioral models.

Physical modeling is often referred as TCAD modeling, for Technology Computer-Aided Design. TCAD modeling is performed by ESD designers to evaluate performance and robustness of their devices before manufacturing. In TCAD, devices can be represented as 2 or 3 dimensional meshes as shown in Fig. 2.7. The model is represented by a mesh, composed of triangle primitives. A TCAD model generally requires extensive preparation before being ready for simulation. Each manufacturing step is first described. A very broad amount of parameters must be described, such as concentration of doping materials, temperature, etc. Afterwards, the 2D or 3D shape of the lithographic photo-masks are defined with sets of coordinates. Finally, all this information is provided to the TCAD program that simulates the manufacturing process. This step consists in computing for each triangle primitive of the mesh several parameters, such as the concentration of doping materials. This step is computationally intensive and can take days to complete. Afterwards, the model is ready for electrical simulation. 2D meshes are faster to prepare and simulate than 3D meshes. However, 2D meshes do not reproduce 3D corner of device. In those areas, the the rectangular shape of a corner creates higher electric fields than the sides, and can be a major failing area. As a result, the robustness of a device estimated by a 2D TCAD simulation can actually be lower than the reality. However, experimented TCAD designers with sufficient know-how are capable of performing very accurate simulations.

Behavioral modeling is widely used for studying interactions between the protection and a circuit. The I(V) curve extracted from a TCAD simulation or a TLP measurement is reproduced by an equivalent model [84, 85, 86]. By nature, ESD protections switch from a high-impedance for the off-state to a low-impedance state after turn-on. In the case of snapback devices, the impedance change is very abrupt, leading to discontinuities of the slope of the I(V) curve. Snapback devices have non-monotonous curves, where multiple values of current can be found for a given voltage, depending on the state of the device. Large and sudden discontinuities are very challenging for classic SPICE simulations, where convergence issues rise and prevent the simulator to complete. To overcome those difficulties, modeling languages like VHDL-AMS or Verilog-A

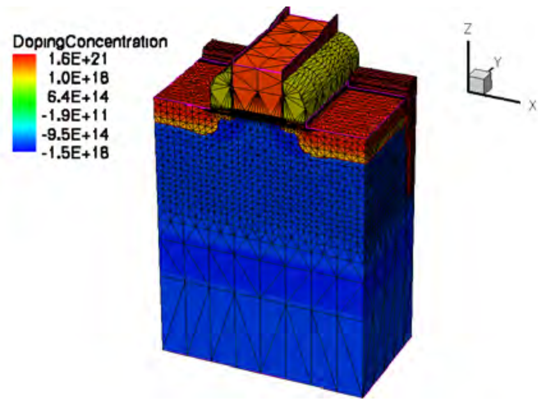

Figure 2.7: 3D mesh representation of TCAD model (Credit: M Johnson and Wikipedia [83])

are extremely helpful. They enable to describe models with very useful primitives such as equation formulation, direct support for signal integration and derivative, combined digital and analog solvers for improved convergence. Using VHDL-AMS for modeling ESD protections was proposed by N. Monnereau in [15]. The original solution proposed to handle snapback devices was to describe their behavior using a state machine. To each state of the machine is associated a slope value on the I(V) curve response 2.8.

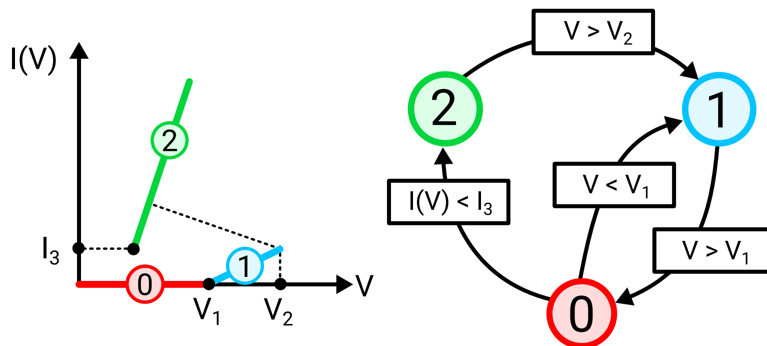

Figure 2.8: ESD protection state machine and corresponding I(V) curve

A possible implementation in VHDL-AMS is given in Listing 2.2. The active machine state is stored in a digital variable called *flag*. Initially, it is at the value 0 representing the off state. When voltage becomes superior to the triggering voltage *v_1*, *flag* takes the value of 1 and the protection turns on. For the protection to return to the off state, current flowing through the protection must become smaller than a very low value. It is generally the physical behavior observed with thyristors for instance, and incidentally helps the simulator converge and avoid oscillations between the on-state and the off-state.

```
--Single snapback structure
--BEGES REMI, 13/05/2013
```

```
--Based off work from MONNEREAU Nicolas
--LAAS/CNRS

library IEEE;
    use IEEE.electrical_systems.all;
    use IEEE.math_real.all;
    use IEEE.std_logic_1164.all;
    use IEEE.numeric_std.all;
    use work.all;

entity simple_snapback is
   generic  (
      v_1 : real:=12.0;
      v_2 : real:=13.0;
      v_3 : real:=2.0;
      v_4 : real:=3.0;
      i_1 : real:=0.0;
      i_2 : real:=0.2;
      i_3 : real:=0.2;
      i_4 : real:=1.1);

   port     (
      terminal P,N : ELECTRICAL
      );
end entity simple_snapback;

architecture behav of simple_snapback is
         quantity Vscr across Iscr through P to N;
    signal flag: integer range 2 downto 0:=0;
    signal previous_state: integer range 2 downto 0:=0;
begin
-- digital state machine
-- Defines in which state is the protection (on, off)
process
        variable state: integer range 2 downto 0 := 0;
begin
        flag <= state;
        case state is
                when 0 => wait until Vscr'Above(v_1);
                                    state:=1;
                                    previous_state<=0;
                when 1 => wait until ((not Vscr'Above(v_1)) or
                 ↪  Vscr'Above(v_2));
```

```
                                        if (Vscr'Above(v_2)) then
                                        ↪  state:= 2;
                                        else state:=0;
                                        end if;
                                        previous_state<=1;
                when 2 => wait until not Vscr'Above(v_3);
                                        state:=0;
                                        previous_state<=2;
                when others => null;
        end case;
end process;
-- Synchronisation between analog and digital simulator cores
-- When protection changes of state
process (flag) is
begin
        case flag is
                when 0 =>       if (previous_state = 1) then break
                ↪  Vscr=>v_1 , Iscr =>i_1;
                                        else break Vscr=>v_3 , Iscr
                                        ↪  =>i_3;
                                        end if;
                when 1 =>       break Vscr => v_1 , Iscr => i_1;
                when 2 =>       break Vscr => v_2 , Iscr => i_2 ;
                when others => null;
        end case;
end process;

-- Analog part
-- Defines the operating slope of the protection depending on its state
if (flag = 2)    use Iscr == ((i_4 - i_3) / (v_4-v_3)) * Vscr + (i_4 -
↪  v_4 * ((i_4 - i_3) / (v_4 - v_3))) ;
elsif (flag = 1) use Iscr == ((i_2 - i_1) / (v_2-v_1)) * Vscr + (i_2 -
↪  v_2 * ((i_2 - i_1) / (v_2 - v_1))) ;
else                    Iscr == 0.0;
end use;

end architecture behav;
```

Listing 2.2: Single snapback behavioral device model

The two main kinds of methods for modeling ESD protections have been presented. They enable accurate simulations of interactions between a circuit and a protection. Future improvements of these methods could focus on triggering delay and overshoot modeling.

2.1.4 Common mode filter

Common mode chokes (CMC) or common mode filters (CMF) allow differential currents to flow while blocking common-mode currents. They are composed of two coils wound around a single core. CMC offer a very low impedance to differential currents, and a large impedance to common-mode currents. They are frequently encountered in electronic systems to protect differential inputs and supply inputs [87, 88, 89]. Unlike regular RC-network filtering, CMC isolate from common mode disturbances where both signal and ground voltages shift. They are effective to protect differential inputs from common noise while preserving integrity of a differential signal. Chokes are frequently used for reducing emission in EMC tests, and increasing immunity of a system to conducted disturbances.

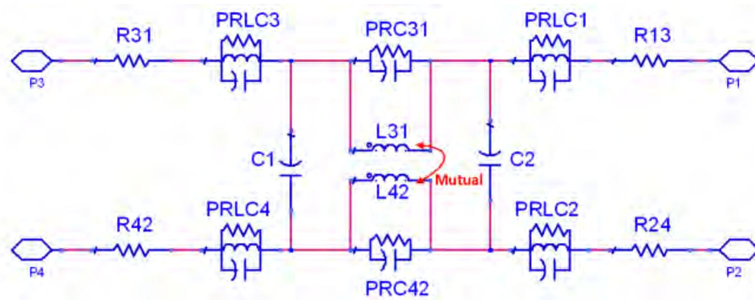

Figure 2.9: CMF linear model - from [73]

CMF were studied and modeled for ESD in [73]. Fig. 2.9 gives an example of a linear model. L31 and L42 represent the mutual inductances of the CMC. C1 and C2 model the parasitic coupling between the two coils, and all the other elements account for parasitic behavior of the coil wires. The device is tuned from a small-signal characterization. However, electrostatic discharges put devices in highly non-linear behavior. It is recommended in [90] that ferrite-based devices should be modeled with a non-linear model. Thus, L31 and L42 are represented in the model using a non-linear equation. Using this method, it is possible to build accurate common-mode filter models suitable for electrostatic discharge simulations.

2.1.5 Ferrite beads

Ferrite bead are passive filtering devices, often found in IC decoupling networks. They remove high-frequency noise in supply lines, which is why they are very often met on power cables for consumer equipments such as laptop supplies for instance. They behave as a second-order low-pass filter. In the ESD field, multiple filtering strategies with second and third order filters involving ferrites were studied in [91]. Some configurations claimed a very positive impact on the latchup immunity of the chip under test.

Ferrite beads are modeled for ESD in [10] with a resistor-capacitor-inductor network given in 2.10. The main coil is represented by an inductance L, a parasitic resistance

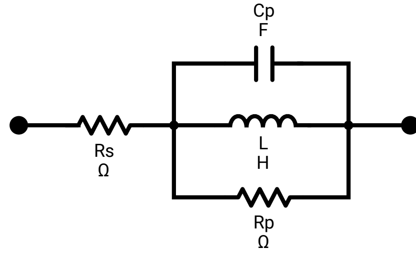

Figure 2.10: Ferrite bead model

R_p and capacitance C_p and a series resistance R_s. Those parameters can be extracted using an impedance meter, or by performing an S-parameters characterization.

2.2 Modeling method application to a TLP generator

The methodology previously described in section 2.1 is applied to the TLP bench at NXP laboratory in Toulouse. It is a good illustration on how to use the library of models for simulating a complete system. Also, this particular testbench is widely used in NXP for characterizing and testing products. The model described hereafter is used for instance to validate non-linear frequency model of passive devices.

To demonstrate its accuracy, the bench model is verified with an extensive simulation versus measurement comparison flow. First, its behavior is measured under different loads and at different charging amplitudes. The setup is identical for each simulation and measurement and is given Fig. 2.11.

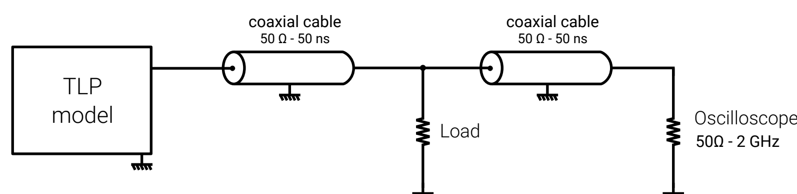

Figure 2.11: Characterization setup of the TLP

All the recorded time-domain waveforms serve as a reference for the modeling. The list of test loads is constituted of resistors, capacitors and inductors of different values. A first version of the testbench model is built, taking into account elements that physically exists. It is tested with a first SPICE simulation for a resistive load and charging voltage, and waveforms are compared against measurements. If results correlate, the validation is continued with another load or another amplitude. If results do not correlate, the model needs corrections. Usually, some part of the curve will match the measurement, but others will not and call for improvements. It can be convenient to try improving a single part of the waveform at a time. Properties of time-domain reflectometry are helpful for locating where the model needs adjustments. Indeed, with TDR, a portion of the curve in time corresponds to a physical location inside the system. If the fall time of the pulse is wrong for instance, then it can mean that some device that smooths the discharge is missing at the far end of the discharge cable. It is also very convenient to observe pictures of the system taken during testing while building the model, because some small elements might easily be missed out or forgotten from the preliminary observation, yet they might impact waveforms a lot. If some minor sections of the curves really cannot be matched using the system schematic as reference, then parasitic devices can be added. All of these steps should quickly converge on an accurate ESD model.

The complete model is detailed in Fig. 2.12. Similarly to all TLPs, the principle of operation is rather straightforward. Initially, the relay is left open while the 50 ns coaxial cable on the left is being charged by the high voltage D.C. supply. The 10 MΩ resistor ensures that the cable charges slowly to avoid oscillations, and isolates the high voltage

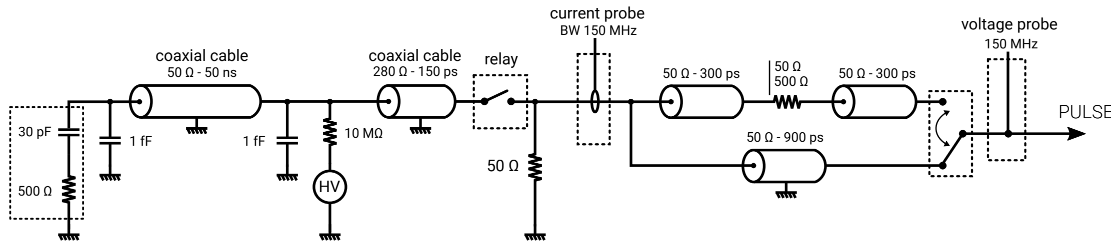

Figure 2.12: Complete model of NXP laboratory's TLP generator

supply from the pulse. The two 1 fF capacitors placed at each end of the discharge cable help the simulator respect the initial condition for the charging voltage. The cable is pre-charged to accelerate the simulation. After the relay, a 50 Ω resistor can be found, intended as an attenuator. Despite having a value of 50 Ω like the coaxial cables, this resistor creates an impedance mismatch. It is the perfect illustration of a small element that is easily missed out but impacts waveforms a lot. A current probe is connected immediately after the attenuator, and a voltage probe is connected at the output of the generator. Position of the probes are important as well, to reproduce the timeshift between them. The short transmission line represented by a 150 ps coaxial cable is a piece of bare wire. It creates impedance mismatches because it has an estimated characteristic impedance of 280 Ω. Finally, two discharge paths are possible inside the generator depending on the configuration of the switch on the output. The direct path is at the bottom, where the pulse goes straight out from the generator. The top path provides a series resistance that limits the discharge current.

A first comparison between measurement and simulation is given in Fig. 2.13. With a 25 Ω resistor and a charging voltage of 500 V, a current of 4.5 A (I_{TLP}) and a voltage of 125 mV (V_{TLP}) are recorded. The ratio of V_{TLP}/I_{TLP} between 40 ns to 100 ns is equal to 25 Ω as expected. The small difference in the second step is due to a small mismatch between the defined charging voltage on the actual TLP bench and the value really applied onto the line. It can be easily corrected in simulation by adding a small offset to the charging voltage. Until 220 ns, both curves match closely. After this time, some differences appear due to small modeling errors. Because of the reflected waves, the errors accumulate and become significant, but only after the main part of the pulse. Indeed, most ESD investigations focus on the part of the discharge below 120 ns which is the more relevant for the analysis because it actually represents voltage and current inside the device under test.

Same comparison is performed on a short circuit in Fig. 2.14. The goal is to test the extreme conditions where the model is going to be used. As expected the voltage is null and the current is close to the maximum 10 A supplied by the TLP (500 V through 50 Ω). At 120 ns, a large difference is observed between the two curves. It is actually a measurement issue due to the oscilloscope clamping amplitude outside the observation window. Because this is a limitation of the equipment, it is not modeled inside the simulation.

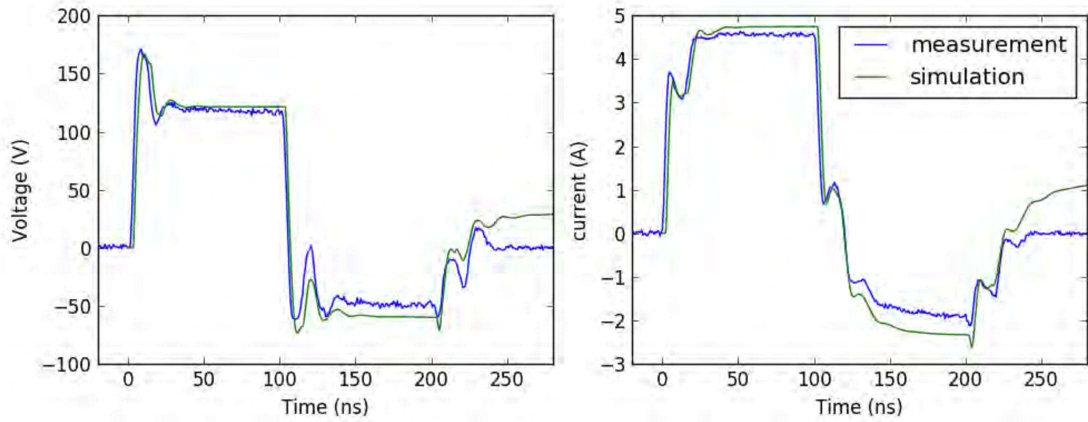

Figure 2.13: Voltage and current waveforms comparison : 500 V charging voltage on 25 Ω

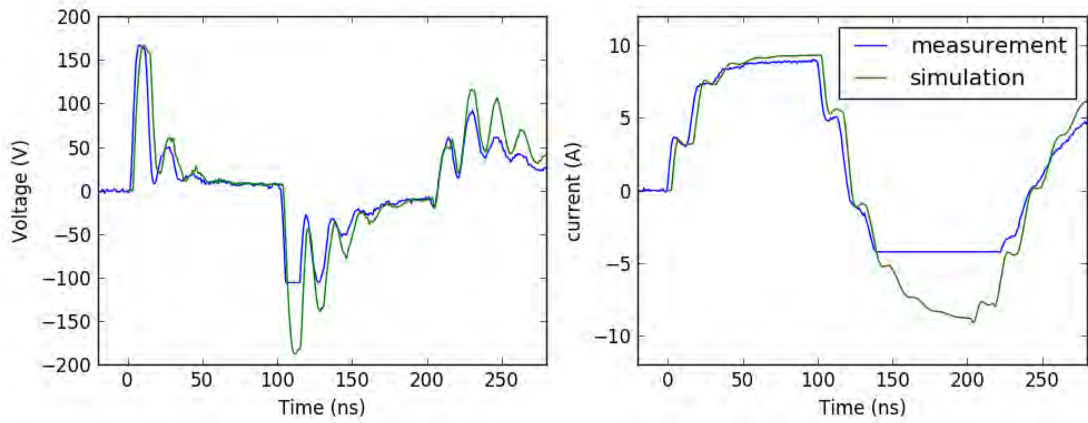

Figure 2.14: Voltage and current waveforms comparison : 500 V charging voltage on a short circuit

Finally, the process is repeated on an open circuit in Fig. 2.15. Observations are similar to the previous figures. The voltage is recorded at 220 V, corresponding to a bit less than half the TLP charging voltage. For an ideal TLP, the value would be exactly 250 V. Due to the 50 Ω resistor between signal and ground inside this TLP bench, the voltage is slightly lower. The current is close to 0 A because the load is an open circuit and does absorb current. Between 100 ns and 120 ns, the same clamped measurement issue than previously is observed on the current waveform.

So far, only resistive loads were tested. Capacitors are interesting to validate models with non real impedance. The response of the generator on a 1 nF capacitor is given in Fig. 2.16. Between 40 ns and 100 ns, voltage and current are not stable, however measurement and simulation correlate well. This is very interesting because it validates

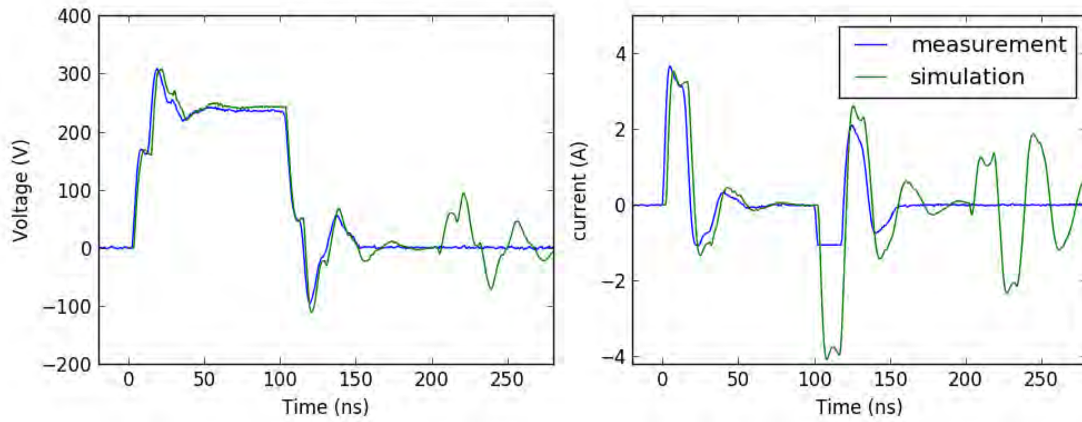

Figure 2.15: Voltage and current waveforms comparison : 500 V charging voltage on open circuit

the behavior of the generator in dynamic regime, with large varying signals. The near-linear voltage curve is due to the capacitor being charged at nearly constant current by the TLP. The slope of this linear curve is directly related to the capacitor value.

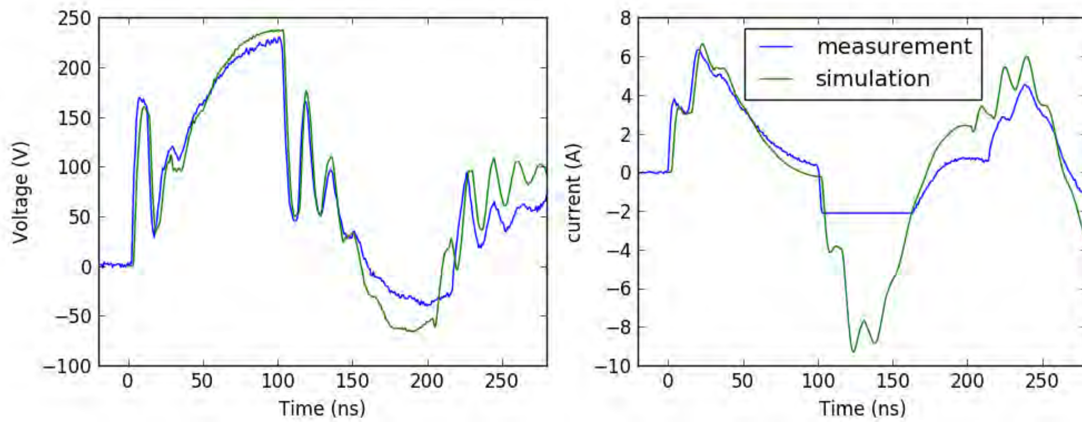

Figure 2.16: Voltage and current waveforms comparison : 500 V charging voltage on a 1 nF capacitor

More simulation and validation curves are provided in Annex A.1, for different loads and amplitudes. The goal of all those validations is to verify the model at both nominal and boundary conditions. Overall, the model is good and fits very well the measurements, demonstrating the validity of the modeling method.

2.3 Development of a new injection tool

2.3.1 Motivation

Throughout this document and in the ESD field in general, the TLP generator is used extensively as a characterization and testing tool. Among its many advantages, it generates very clean and controllable pulses in a shielded environment. It has also proven to be a great tool for studying, among other things, the behavior of silicon-level devices.

Nevertheless, ESD gun testing remains the mandatory requirement defined by customers for product qualification. Several ESD gun standards exist, targeting qualification of devices against electro-static discharges. The HMM specification [44], the IEC 61000-4-2 standard [16] and the ISO 10605 standard [17] define the same ESD testing waveform, using the same discharge device, but with different application conditions. Together, they cover a very large amount of tested devices from equipment, boards, and integrated circuit, in automotive and consumer fields. The waveform common to those three standards (Fig. 2.17) is virtually the most widely used pulse for ESD qualification.

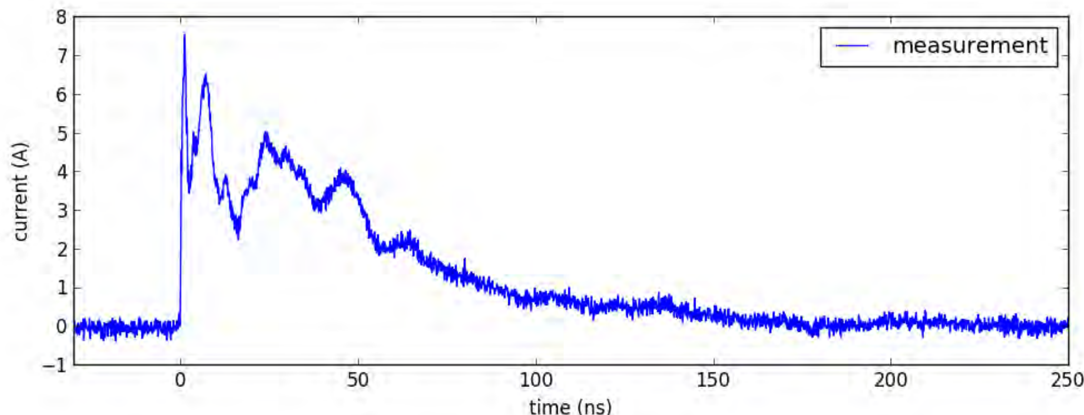

Figure 2.17: HMM pulse current waveform : 2 kV charging voltage on a 2 Ω resistive load

By design, the ESD gun has certain requirements to generate a realistic ESD discharge. Incidentally, those requirements make investigation harder because the injected waveform and test conditions are less reproducible [92]. For instance, injection is performed through a metallic tip a few centimeters long. The tip is a large source of electromagnetic radiated noise during the discharge up to several gigahertz [93]. Also, the ground return is a metallic ribbon a few meters long. It models the equivalent ground connection of a human body. However, it is also very inductive, and its value changes considerably in function of its shape. Finally, for integrated circuits in particular, the ESD gun waveform is a lot more complex than the rectangular TLP shape. In case of failure, the investigation can be quite tedious to conduct.

Unlike the ESD gun, TLP generators are extremely well controlled. The discharge

propagates entirely inside coaxial cables and does not generate any Radio-frequency (RF) radiation. In some few cases, failures can be correlated between a TLP and ESD gun [30]. However, there is generally no clear link between failures induced by each generator [94]. The lack of correlation is proven further in [30], with 2 kΩ ESD gun discharge modules. [30] demonstrates that some ESD structures in analog high-voltage technology have completely uncorrelated failure levels between TLP and HMM. Failure analysis shows that the failure mechanisms are different.

Therefore, TLP cannot be used as a drop-in replacement to ESD gun for qualification. A compromise can be found by modifying a TLP generator to produce the gun waveform, but in a shielded, well-controlled, and reproducible environment. This approach has been explored in the past by E. Grund [95] and Y. Cao [32].

In [95], Grund modifies a TLP generator by placing an impedance mismatch between two coaxial lines. The architecture of the device is given in Fig. 2.18. With this setup, the initial peak of the waveform is produced by a 4 ns cable. The second part of the waveform is produced by the combination of the 30 ns cable and a large series resistance R_{ML}, that lowers the current compared to the first peak. A risetime filter connected after the switch enforces a maximum risetime of 700 ps to 1 ns, to match the value defined in the standards. Overall, the generated waveforms has less dynamic than the standardized waveform and exhibits two flat steps. It is also widely unmatched because of the series resistor. It is suspected that this impedance mismatch placed between two delays makes this generator very likely to generate oscillations. The mismatch causes traveling waves to bounce back and forth between the load and R_{ML}, and this kind of behavior is quite far from an original gun generator. It does comply to the standards though since the required values for risetime, current at 30 ns and 60 ns are comprised in the tolerance margins.

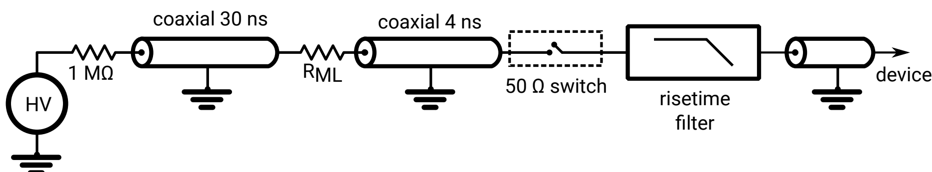

Figure 2.18: Grund's modified TLP for HMM pulse generation

The approach proposed by Cao in [32] consists in employing a capacitive discharge through a short coaxial cable to generate an HMM-compliant pulse. The architecture of the device is given in Fig. 2.19. The generator cannot be really classified as a TLP generator, since the discharge is mostly supported by the RLC network. The 1 ns coaxial cable acts as a distributed capacitor to provide the high current of the first peak. Overall, the generated waveform looks good on a 50 Ω load. However, the system is always verified with a 50 Ω termination. It is never tested in mismatched output conditions, with a true pure 2 Ω resistive load as defined in the standard. It is suspected that with an impedance mismatch at the output, the system enters in ringing oscillation. The oscillation is likely

generated by an energy exchange between the load and the RLC network, separated by the delay of the injection cable. Ultimately, this generator is probably not compliant with the standard.

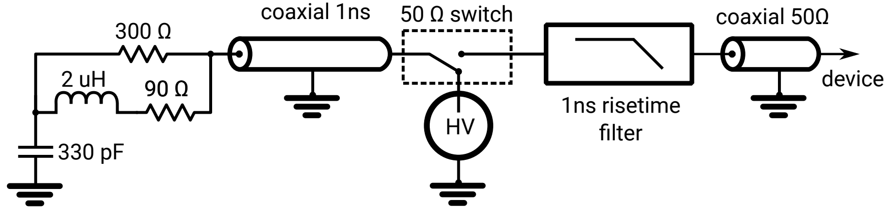

Figure 2.19: Cao's TLP-based HMM generator

In this chapter, a new and different setup is proposed. It is based on using propagation delays to shape the pulse with high flexibility. Compared to those two previous approaches, the design proposed in this document works with a classic 100 ns TLP, without requiring internal modifications. It will be demonstrated later that the proposed architecture is quite flexible, and can be tuned to match any gun pulse configuration. It is also possible to tune the output impedance, while still keeping the same waveform. Ultimately, this generator is able to generate an HMM waveform inside a shielded environment, but with a large output impedance similarly to true HMM generators. This generator was published in [33].

2.3.2 Principle of operation of the TLP-HMM

Later in this document, the new generator is referred as TLP-HMM. The TLP-HMM requires two additional modules to be connected at each extremity of a classic 100 ns TLP. These modules are simply referred hereafter as the *absorber* and the *shaping filter* (Fig. 2.20). The principle of the TLP-HMM is to re-route parts of an incoming rectangular pulse into the ground. The remaining current is injected on a 2 Ω calibration resistor, resulting in the same waveform than expected by the standards. The role of each module is detailed in the following sections.

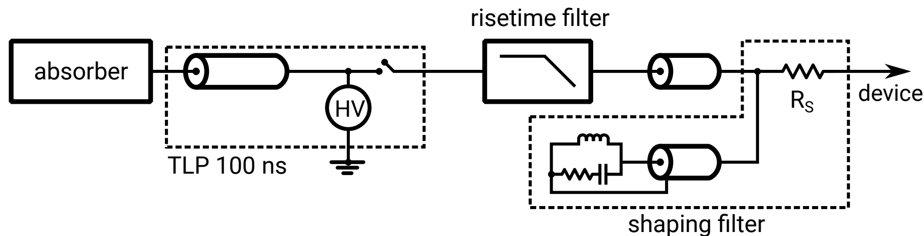

Figure 2.20: TLP-HMM architecture

Shaping filter

The shaping filter (see Fig. 2.21) deviates a part of the incoming rectangular pulse into the grounded coaxial shielding. It is constituted of five different elements, an RLC network, a delay cable and an injection resistor. The capacitor C is separated from the main propagation path by a small transmission line of delay Δt. The inductor L is neglected in this first part of the analysis. It behaves as an open circuit at the beginning of the pulse. The short coaxial cable creates a delay Δt between the main line and the RLC network. The injection resistor R_S serves to increase the output impedance, in order to get closer to the behavior of an actual HMM generator.

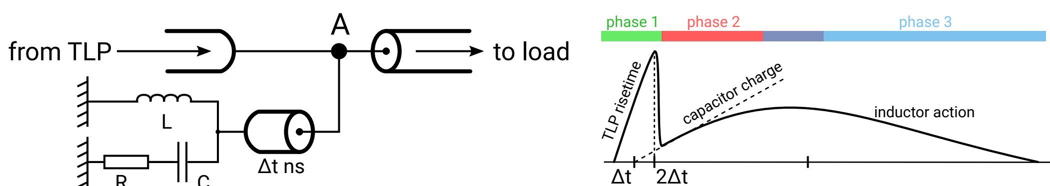

Figure 2.21: Shaping filter architecture and operation

An example case is given to detail the behavior of the generator, with a focus on the shaping filter. In phase 1 (graph on the right in Fig. 2.21), a TLP is injected on the main line. It reaches point A at $t = 0$ and the voltage at A rises from 0 V. The capacitor is still not visible from A and does not see the TLP rising edge yet. At $t = \Delta t$, the pulse reaches the capacitor, which begins to charge. This change in voltage and current in the capacitor branch is not visible immediately from point A until it propagates back. Point A keeps rising with the TLP impulse until $t = 2\Delta t$. At this moment, potential at point A falls almost immediately to 0 V, because the capacitor is drawing all the current, and its potential is low. This results in the generation of the first peak. The peak width is approximately $2\Delta t$.

In phase 2, the capacitor keeps charging, the potential at point A rises and the current drawn by the capacitor decreases. Slowly, the inductor L connected in parallel starts drawing some current. At some point between phase 2 and 3, the inductor current becomes equal to the capacitor current, and the capacitor ceases to charge. The capacitor starts discharging through the inductor. During phase 3, the inductor draws all the current and brings the voltage at A down to 0 V. The result of this combined action generates the characteristic slow slope of the HMM waveform.

The resistor R creates a voltage offset at $t = 2\Delta t$. It is used to match better the standardized waveform, which also has a superior to zero value after the first peak.

The peak width can be tuned by increasing or decreasing the length of the delay cable $t = \Delta t$. The peak width is approximately equal to $t = 2\Delta t$.

The peak risetime is enforced by the TLP risetime filter. A 1 ns risetime filter provides the correct risetime to be compliant with the standards. Several risetime filters implementations suitable for TLP generators have been described in [38, 37]. Matched risetime filters have the particularity to work by absorption, rather than rejection. Most

filters prevent high-frequency signals to propagate further into a system by reflecting them back. Risetime filters on the other hand route high-frequencies into the ground of the system, which leaves the main signal line free of noise.

The exact schematic of the shaping filter is given in Fig. 2.22. Capacitances are distributed to reduce parasitic inductances. The inductances have also been distributed to increase the maximum total current that can be absorbed. The PCB (Fig. 2.23) has a ground plane, and the central line is $50\,\Omega$ matched. Overall, its dimensions must be kept as small as possible to reduce the impact of delays.

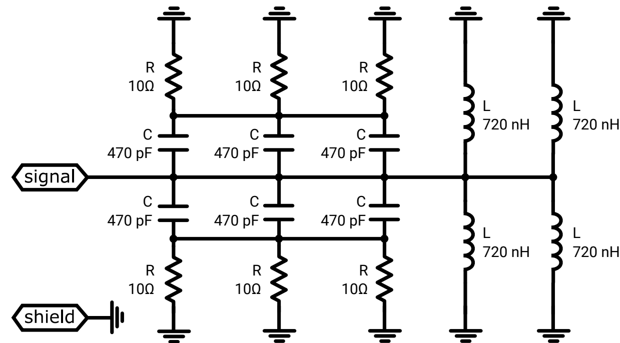

Figure 2.22: Shaping-filter schematic

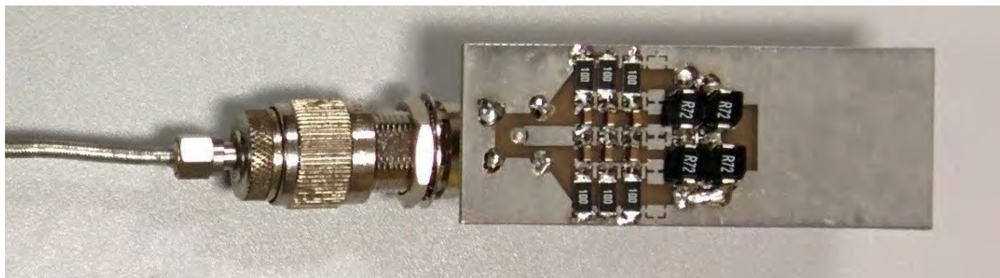

Figure 2.23: Assembled shaping-filter

Absorber

Near the end of the HMM waveform, the inductor is drawing almost all the incoming TLP current. After 100 ns, the current injected by the TLP into the shaping filter and the DUT becomes null because the cable is completely discharged. However, the current inside the inductor cannot be stopped instantly. Without the absorber, the inductor would keep absorbing a non-zero current after the TLP pulse, drawing a negative potential at point A. To avoid this phenomenon, the absorber completely filters the TLP falling edge at the end of the pulse. This way, the current through the inductor is softly brought back to 0 by the absorber, effectively eliminating the negative voltage issue.

It also acts as a matched termination for transient events, which is great to eliminate reflections and prevent ringing oscillations.

The schematic of the absorber is given Fig. 2.24 and a picture of the assembled device is given in Fig. 2.25. The device is constituted of a 50 Ω resistor, in series with a 6.6 nF capacitor.

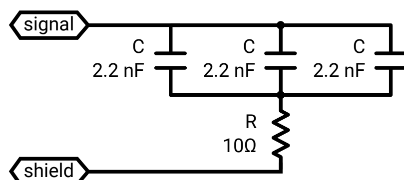

Figure 2.24: Absorber schematic

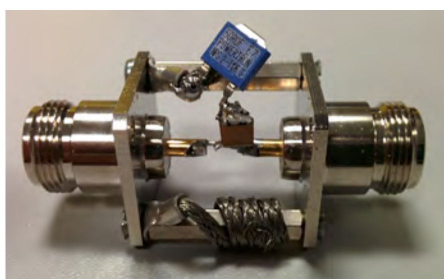

Figure 2.25: Assembled absorber

2.3.3 Validation of TLP-HMM models and standard compliance

Model validation

The response of the generator is tested in conditions as close as possible to the ISO 10605 standard [17]. The generator is connected to a 2 Ω load, itself connected to a 12 GHz (10 ps S^{-1}) oscilloscope with a 50 Ω input impedance. The setup (Fig. 2.26) has the same loading impedance than the standard measurement "target" [17, 16].

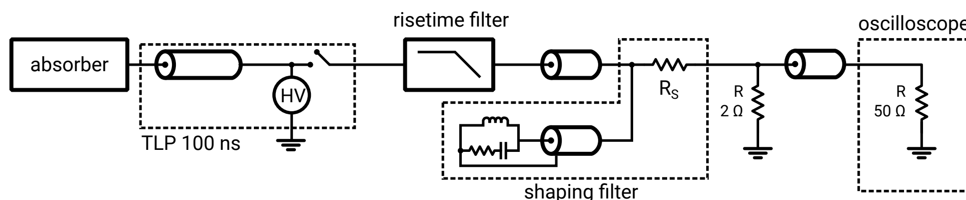

Figure 2.26: Injection setup for validating the generator

The measured and simulated waveforms are given in Fig. 2.27. Measured currents

at 30 ns and 60 ns are within the 30 % tolerance of the standard (see Table 2.2). The measured peak current is a bit lower (110 mA short of minimum margin) than standard value. This is easily corrected on the TLP by adding a small positive offset to the charging voltage.

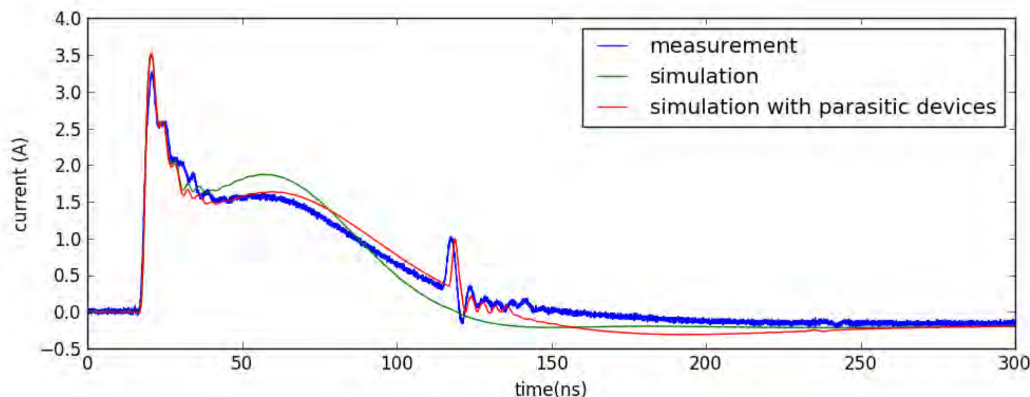

Figure 2.27: Measurement versus simulation of a 250 V TLP-HMM (equivalent 1 kV HMM) on 2 Ω

	Standard (A)	Measured (A)	Simulated (A)
peak	3.75 ±0.375	3.26	3.52
30 ns	2 ±0.6	1.54	1.8
60 ns	1 ±0.3	1.18	1.32

Table 2.2: Measured and simulated currents versus standardized values

Overall, simulation and measurement correlate quite well. There is a small difference for the slopes between 40 ns and 150 ns. Investigation showed this difference comes from the shaping filter, and its inductances in particular. Their frequency behavior is not as good as expected, and having four inductances in parallel increases further this issue. Indeed, in this configuration parasitic capacitance of inductors are connected in parallel. They add up together, leading to a large total parasitic value and degraded frequency behavior. For the next iteration of the shaping filter, a single RF inductor should be used instead. The shaping filter model can be corrected by connecting in parallel a total parasitic capacitance of 2 nF in series with a 15 Ω parasitic resistor, like shown in Fig. 2.28.

In Fig. 2.27, the glitch visible at approximately 120 ns is due to the absorber, because of two different parasitic devices. At the beginning of the TLP pulse, the parasitic capacitance between signal and ground is charged. Using the simulation, it is estimated at 20 pF. Its sudden discharge at the end of the TLP pulse causes the short voltage and current increase observed at 120 ns. The parasitic series inductance of the three

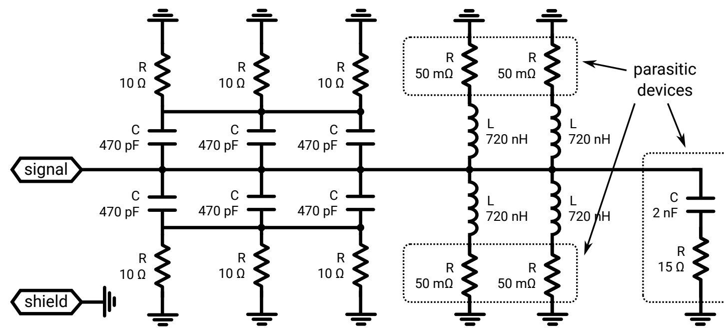

Figure 2.28: Shaping-filter schematic with parasitics

2.2 nF capacitors and the 50 Ω resistor (Fig. 2.29) is responsible afterward for the small oscillation observed between 120 ns and 150 ns. This issue should be fixed in the next iteration of the absorber by building the absorber on a dedicated PCB with 50 Ω lines. Guarantying matching along the path should eliminate this ringing oscillation.

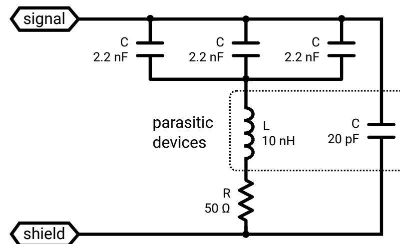

Figure 2.29: Absorber schematic with parasitics

Comparison with an ESD Gun

A generally adopted procedure to compare two ESD generators is to destroy ESD protections with each one of them and compare the failure levels. Therefore, the TLP-HMM is compared to a real standardized HMM generator following this procedure. The failure criteria is a sudden increase in the leakage current of the ESD protection under test after a pulse injection.

A set of ten different ESD protections, of different size, on-resistance, structure and failure levels are stressed with both generators. Five samples are tested for each structure and generator, to ensure the failure levels do not exhibit large variations. Table 2.3 gives the on-resistance for each tested device. These values are important later on for building a failure correlation method.

Testing results are summarized in Table 2.4. Unfortunately, the result set is too small to draw a clear conclusion. It was discovered that the TLP-HMM is not able to deliver enough current to break structure E and above. The TLP-HMM relies on a regular TLP, whose high-voltage DC supply is limited to 1 kV. On a true HMM

Structure	A	B	C	D	E	F	G	H	I	J
R_{ON} (Ω)	6.2	2.85	9.7	13.3	2.7	3.25	2.4	4.7	1.7	1.85

Table 2.3: Tested ESD protection set

generator, high-voltage D.C. supplies are generally able to reach 15 kV charging voltage and beyond. A TLP rarely requires DC supplies able to reach above 1 kV, because the output impedance is lower than HMM. For a given charging voltage, a TLP will deliver a much larger amount of current than an HMM generator. However, in the TLP-HMM configuration, the equivalent impedance of the generator is higher than the one of a TLP. As a result, the injected current is smaller. Ultimately, the TLP DC supply fails to charge high enough in order to produce large amounts of current. This defect should be fixed in a new version by building a custom TLP with a much more powerful supply.

Structure	A	B	C	D	E	F	G	H	I	J
TLP-HMM (V)	640	700	890	860	-	-	-	-	-	-
HMM (V)	1250	1250	1500	1500	6500	5000	13000	9500	20000	145000

Table 2.4: Testing results - failure levels per ESD protection

Correlation between TLP and HMM

Based on those preliminary results, a correlation method is built between TLP failure levels and HMM failure levels. It exploits the fact that the TLP-HMM is at its core a TLP, yet has a similar behavior to an HMM generator. The analysis was published in [33]. It requires a very simple characterization step for each generator, to extract the most simple equivalent circuit composed of a resistor and a DC voltage source. The DC voltage source takes the value defined by the user on the generator before a pulse. The resistor is extracted from the characterization. Finally, the ESD protection is modeled by its on-resistance. The complete equivalent circuit is just a DC source with two resistors in series (Fig 2.30). The circuit is extremely simple, however it is shown later on that it is sufficient to build a seemingly good correlation method. The key part of this approach is to consider the interaction between the on-resistance of the ESD protection and the equivalent resistance of the generator.

Different equivalent DC voltages and resistances are found between TLP and HMM. The TLP used in the NXP lab has an equivalent output resistance of 83 Ω. Interestingly, a 50 Ω value was expected, but it turns out that this particular TLP has a mismatched attenuator in it, increasing slightly its equivalent output resistance. A more classic TLP at the LAAS laboratory was also characterized and exhibits an output resistance of about 53 Ω. The HMM generator has a much larger output resistance, estimated at about 600 Ω. The TLP-HMM was also characterized, and situates somewhere in the middle with an output resistance of about 300 Ω.

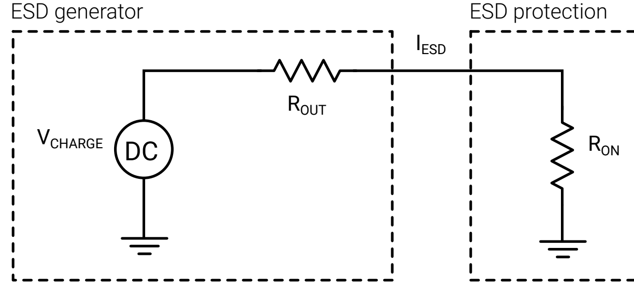

Figure 2.30: Equivalent circuit for failure correlation

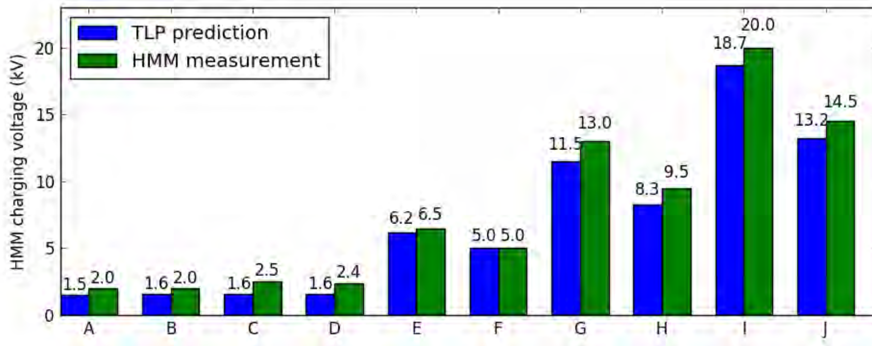

Figure 2.31: TLP prediction versus HMM measurement of failure levels

Despite different charging voltages and equivalent resistances, using this simple method yields almost identical failure currents between TLP and TLP-HMM. I_{ESD} (from Fig. 2.30) was calculated with each generator, for each of the 10 tested structures. This result indicates that this simplified circuit could link failure levels between generators. To try this hypothesis further, it is attempted to predict the HMM failure levels, directly from TLP results. The prediction method requires the TLP failure voltage and the ESD-on resistance, to predict the HMM failing voltage. Both values are easily obtained from a TLP characterization. Eq. 2.9 provides the formula, directly extracted from the equivalent circuit, to link HMM charging voltage to the TLP failure current. In this formula, I_{ESD} is measured with the TLP.

$$V_{HMM} = I_{ESD} * (R_{HMM} + R_{ON}) \tag{2.9}$$

Fig. 2.31 shows the results of this prediction method on the set of 10 ESD protections. Good correlation is achieved and indicates this method could effectively be used to establish correlation between ESD generators.

2.3.4 Conclusion, limitations and future improvements

In this section, a new alternative for generating HMM compliant waveforms using a TLP was presented. The generator works correctly and has proven quite robust against ringing oscillations and parasitic disturbances. The generated waveform passes HMM, IEC 61000-4-2 and ISO-10605 requirements.

A prototype has been constructed to enable initial testing and evaluation of the system. The design must be improved to reduce the impact of parasitic devices. Also, higher charging voltages must be supported for the generator to inject larger amount of currents. It is currently not enough to break ESD protections that withstand above 4 A of transient current. There are many challenges to be solved in order to build a TLP able to charge at 8 kV and beyond. For instance, the risetime filters are not able to sustain such high voltages and custom filters are probably required.

The insights gained during this research work led to the development of a correlation method between ESD generators. It was discovered that it is possible to link a TLP failure level to an HMM failure voltage, using a preliminary characterization method. This approach was validated on a set of 10 different ESD protections with good success so far. Future work will involve testing the method on a larger set of ESD protection and studying the triggered failure modes.

2.4 Near-field sensor post-processing

Near-field scan has been presented previously in 1.3.2. Using this technique it is possible to measure maps of electric or magnetic field above a device. While those maps already provide interesting information, to locate sources of RF noise for instance, it is interesting to post-process them in order to get voltages and currents inside the measured circuit. In this section, two different methods are described for reconstructing the original current from a near-field magnetic measurement. Each method requires a preliminary characterization of the probe. Near-field scanners were extensively studied in [66, 15].

2.4.1 Time-domain integration method

It is shown in [66] that the measured voltage of near-field magnetic probe is proportional to the time derivative of the measured and coupled current. In the next part of this analysis, the sensor voltage is denoted V_{sensor} and the original current I_{TLP}. The relationship between the two is expressed by Eq. 2.10. G is the gain of the sensor.

$$V_{sensor}(t) = G.\frac{dI_{TLP}(t)}{dt} \tag{2.10}$$

By integrating Eq. 2.10, it is possible to express I_{TLP} as a function of the measured sensor voltage V_{sensor}. This is expressed in Eq. 2.11. The offset A is the result of the

integration.

$$I_{TLP}(t) = \frac{1}{G} \int V_{sensor}(t)\mathrm{d}t + A \tag{2.11}$$

Both constants $1/G$ and A are determined experimentally with a preliminary calibration. Once calculated, both factors are estimated to remain constant and can be reused in other measurements.

On silicon, one of the sensors is dedicated to the calibration phase. The setup is given in Fig. 2.32. The input of the sensor is represented by ports S1 and S2. A square impulse of 1 V amplitude generated by a 100 ns wide TLP with a risetime of 8 ns is injected between the two input pins. The response V_{sensor} is measured with a 2 GHz bandwidth 10 GS s^{-1} oscilloscope in differential input connected between C1 and C2.

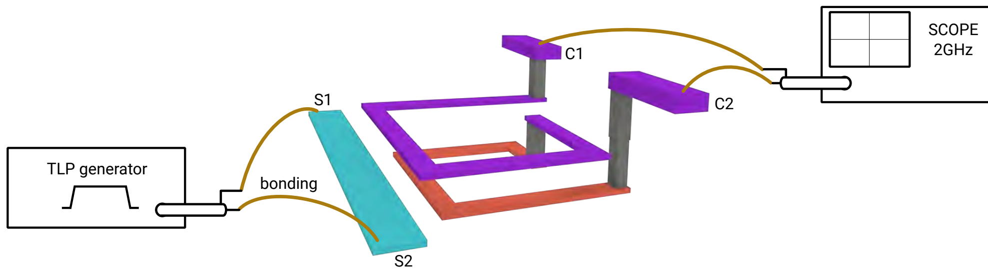

Figure 2.32: Calibration sensor setup for time-domain method

I_{TLP} and V_{sensor} waveforms are recorded during calibration (see Fig. 2.33). The top curve represents the input (I_{TLP}) and the bottom curve the output (V_{sensor}).

With those measurements, $1/G$ and A were estimated respectively equal to 8.10^8 and 0.0 .

The reconstructed curve is compared to the original in Fig. 2.34. The main step of 180 mA amplitude is properly reconstituted. Differences can be seen on the rising and falling edges of the pulse. The original curve has a first step of about 10 ns wide, with an amplitude of 80 mA. This step is due to the connection cable between the load and the generator, and is fundamentally a measurement artifact. So the difference between the two curves at 10 ns and 110 ns are expected. After 110 ns, a large difference is visible on the reflected part. In most TLP analysis, the area of interest is during the pulse between 10 ns and 110 ns. Therefore, those discrepancies are ignored, and the reconstitution method is considered accurate enough.

The time-domain method is simple to compute and produces good results. So far, it was tested with a rectangular pulse, and in the future more cross checks should be done to ensure it works with dynamic signal such as sine waves. The time-domain method also makes several approximations regarding the sensor's characteristics and its behavior. It assumes that the gain of the sensor is constant for all frequencies, which is not true. The frequency response is provided in the next section. It should be noted that the bonding

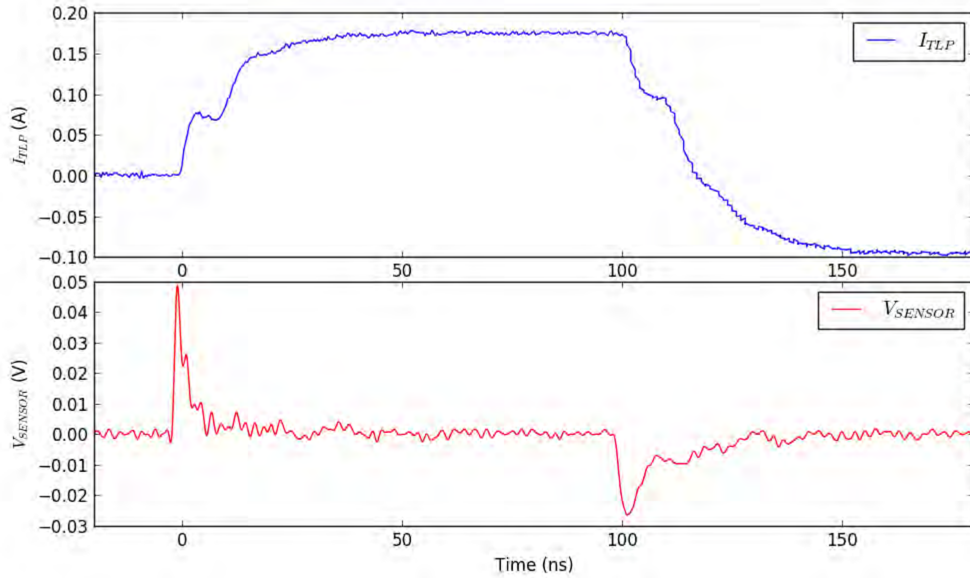

Figure 2.33: Measured voltage waveform

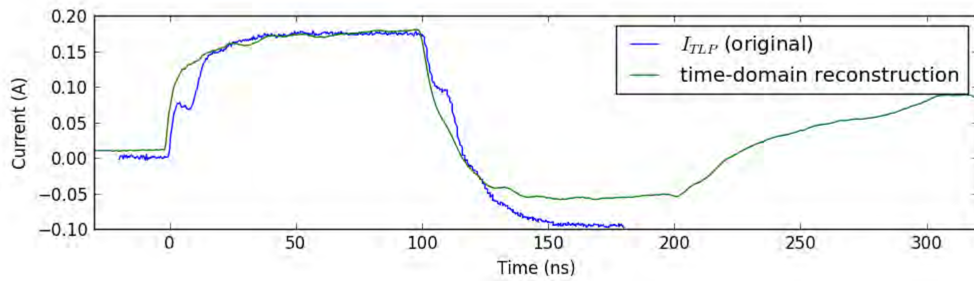

Figure 2.34: Reference current waveform versus time-domain reconstruction

pads are also part of the calibration, but they may limit the sensor performance at high frequency.

2.4.2 Frequency-domain reconstruction method

The frequency-domain method post-processes the V_{sensor} waveform using the sensor's frequency response. The characterization is conducted with the calibration sensor, using a Vector Network Analyzer. The calibration setup is similar to the time-domain method. It is given in Fig. 2.35.

The S-parameters measurements of the sensor are given in Fig. 2.36. $S11$ is the reflected power at port 1. $S21$ is the transmitted power between port 1 and port 2, and $S12$ is the transmitted power between port 2 to 1. In theory, $S12$ is identical to $S21$ for symmetrical 2-port devices. $S22$ is the reflected power from the output, which is not

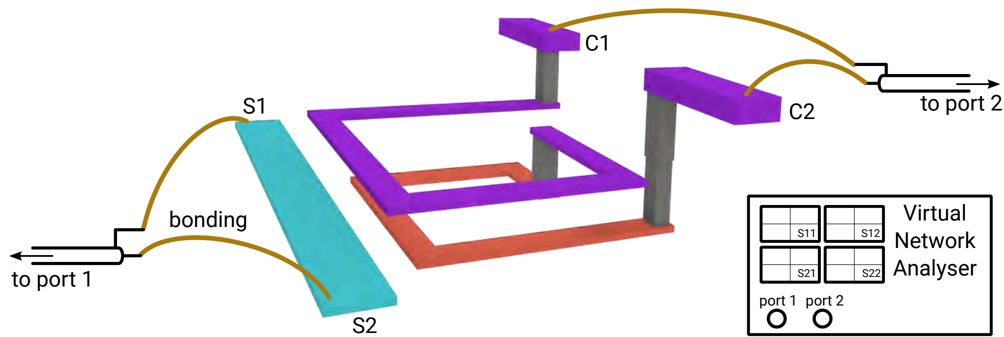

Figure 2.35: Calibration sensor setup for frequency-domain method

relevant for this study.

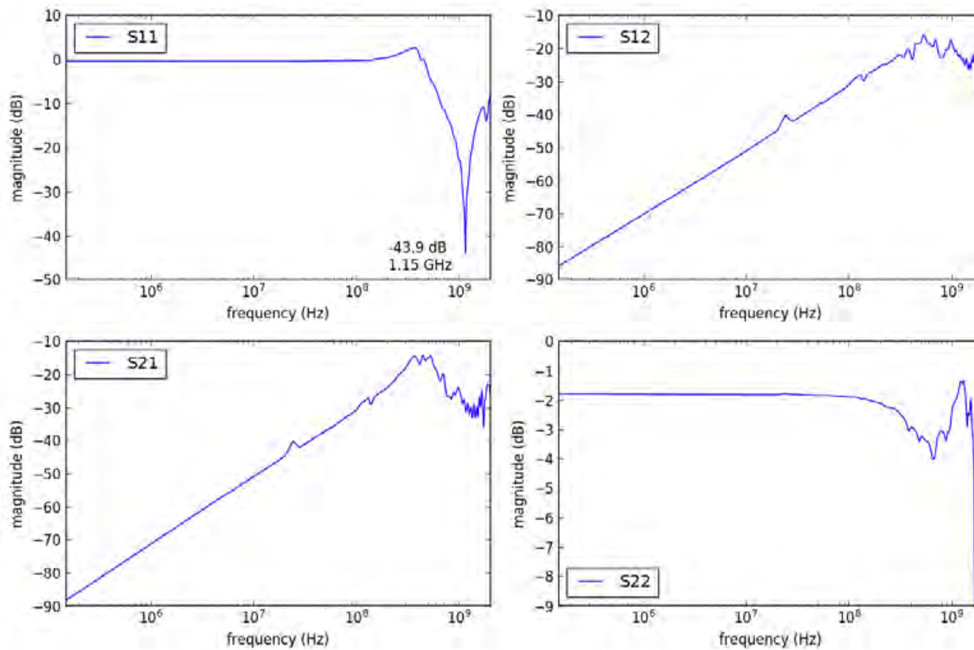

Figure 2.36: Sensor frequency response

It was suspected previously that the sensor's response is not constant versus frequency. The S-parameters measurement confirms it, showing a sensor bandwidth of about 300 MHz. S11 shows a resonance of −43.9 dB at 1.15 GHz. It corresponds to a frequency where insertion losses become very small. However, this peak is not visible on the transmitted coefficient $S12$ or $S21$. It probably means that at this frequency, a part of the input power is dissipated by the device, either by the bonding or the sensor itself.

S21 is the only scattering parameter used in the post-processing method. It represents the transfer function between the input current and the sensed voltage. Previously, only the magnitude measurements were displayed in Fig. 2.36. Another S-parameters measurement has been performed, configured to obtain both magnitude and phase information (Fig. 2.37). Phase information is very helpful to improve the quality of the post-processing, as will be detailed later on.

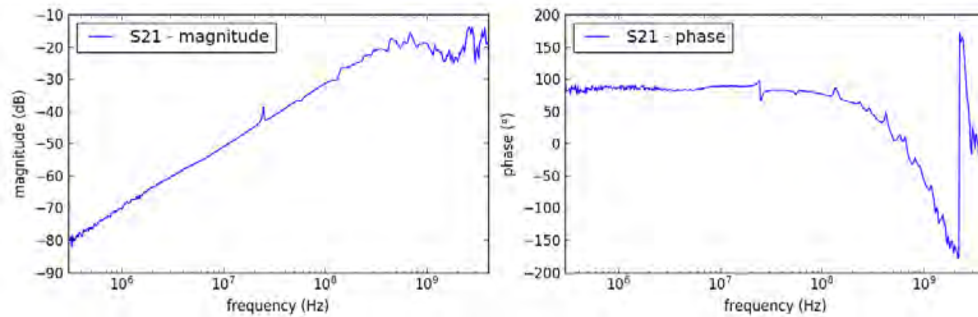

Figure 2.37: Sensor frequency response - complex S21 (magnitude and phase)

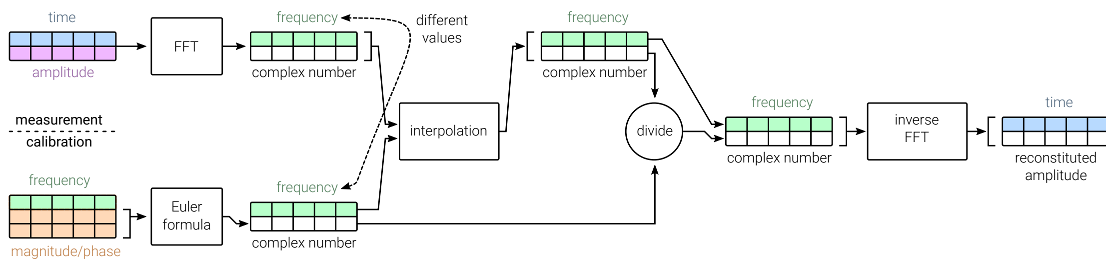

Figure 2.38: Post-processing pipeline

The post-processing method is detailed in Fig. 2.38. The measurement data in the time-domain is converted to the frequency domain using Fast Fourier Transform. The output array associates a complex number to each frequency point. An example is given in Table 2.5.

frequencies (Hz)	complex value
1.0*10^6	0.33 + i0.2
2.0*10^6	0.46 - i1.2
etc.	etc.

Table 2.5: Structure for the result of (complex) FFT

On the other hand, the S21 calibration data associates a phase and magnitude to

each frequency point. An example is given with Table 2.6. Using Euler formula (Eq. 2.12), magnitude and phase are converted to a complex number.

frequencies (Hz)	magnitude (dB)	phase (rad)
$1.5*10^6$	-10	1.23
$2.5*10^6$	-12	0.12
etc.	etc.	etc

Table 2.6: Structure for the S-parameter measurement

$$S21_{complex} = 10^{\frac{magnitude}{20}} * (\cos(phase) + i * \sin(phase)) \tag{2.12}$$

After these two operations, both data are in the frequency domain. Before moving forward in the processing, an interpolation step is required. Indeed, the frequency points between the measurement and the calibration do not match. For the next part of the algorithm, they need to be identical. In this case study, a linear interpolation is employed on the measurement data to align it on the characterization. It is possible that this kind of interpolation is not ideal. The impact of the interpolation on the results has not been studied yet but it should be done in a future work.

Afterwards, the measurement data is compensated by the characterization data of the sensor. This is done by dividing each complex value of the measurement by the complex value of the sensor.

Finally, the inverse Fast Fourier Transform of the compensated data is calculated to bring back the waveform into the time-domain. The resulting waveform is compared to the original and the integration method in Fig. 2.39. Overall, the results are similar between the time-domain and frequency-domain reconstitutions. The frequency domain seems reproduce better the rising and falling edges better. The measurement has two short steps at the beginning and the end of the pulse, because it is performed with TDR. It was expected that those steps would not show up on the reconstituted waveform that should be perfectly rectangular. There is a lot of room for improvement for each method, such as increasing the measurement frequency, and using techniques like zero-padding before performing Fast Fourier Transform and taking dissipated power into account. Those improvements will be evaluated and implemented as follow-up work.

2.4.3 Conclusion on near-field post-processing

In conclusion, both methods so far produce acceptable results. The frequency method is closer to the physical properties of the device. Ultimately, it is believed that it should behave better than the time-domain method. It is the method chosen for processing measurement data later-on in section 3.2.7

As follow-up work, both techniques should be verified with sine-waves and other time varying signals. Different integration methods and improvements to the post-processing pipeline should be tested and evaluated.

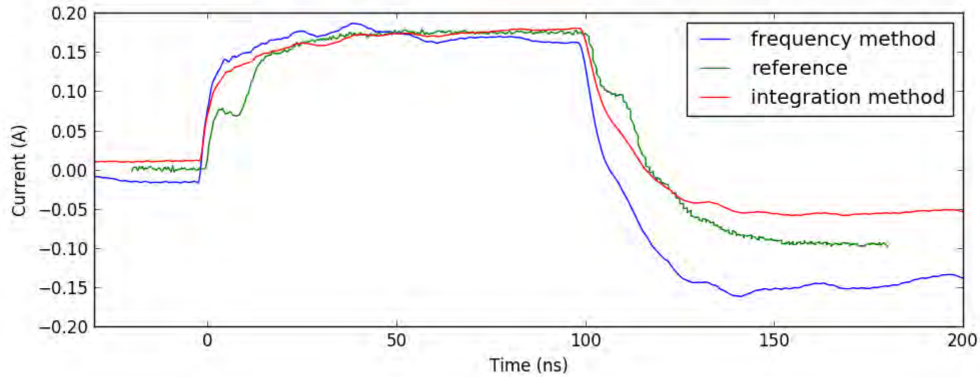

Figure 2.39: Reference current waveform versus frequency-domain and time-domain reconstructions

The two post-processing methods were implemented in Python language. The code is freely distributed [96] as open-source software under the MIT licensing [97].

2.5 Conclusion

In conclusion of this chapter, several tools have been presented for soft-failure analysis. The system-level modeling method is very helpful to create accurate models, in order to simulate waveforms propagating up to an integrated circuit. It was a first required step before being able to study the apparition of functional failures inside integrated circuits, at the silicon level.

The propagation and reflection mechanisms studied were used later on to create a custom pulse generator. This new generator, called TLP-HMM, reproduces the waveform of the HMM specification and IEC 61000-4-2/ISO 10605 standards. Combined together, they define the most widely employed pulse in the entire ESD field. The TLP-HMM brings several advantages compared to a standard HMM generator. Among other things, it offers advanced discharge reproducibility, a fully shielded propagation path and zero radiated emission. The current design is a prototype that helped identify improvements to make in future iterations. In particular, higher charging capability is required.

To test this generator against actual ESD guns, a set of 10 different ESD protections was stressed and destroyed with a TLP, a TLP-HMM and an HMM generator. The comparison of failure levels between all of them led to discover a correlation law using the simplest possible equivalent circuit. It relies on calculating the failure current, using the equivalent generator impedance, the ESD protection on-resistance and the charging voltage. Then, calculating this failure current for one generator allows to guess the failing charging voltage of any other. Charging voltages could be accurately guessed on the entire set of 10 protections.

Finally, two post-processing methods for a near-field on-chip probe were detailed. The first method relies on an integration of the measured signal in the time domain.

The second method processes the signal in the frequency domain, by compensating it with the sensor characterization. Accuracy of each method was roughly estimated. Future work will involve a better assessment of the accuracy, and improvements to the processing script.

Chapter 3

Study of soft-failures at silicon-level

3.1 Study of a real product

This chapter details a study case of a real ASIC from the automotive field exposed to ESD during normal operation. The studied chip performs high-level functions with significant roles inside the vehicle, such as communicating with sensors and performing safety-related duties. Tests and analysis are focused on one function in particular, the primary voltage regulation function of the device. In the final application, it is powered directly by the car's battery, and supplies the entire product. It is also a good opportunity to study the behavior of a complex analog function exposed to electrostatic discharges. This product was designed at NXP, and complete access to the schematic and layout was made available for this research work. The product operation, architecture and application are described in section 3.1.1.

This chip has a recommended application circuit provided by NXP, and a specification. They define many requirements to ensure proper operation, such as supply voltage range, current capability, etc. Among all those requirements is also defined the minimum constraints for external capacitive decoupling and filtering. Those constraints are not required by the functionality itself, but are needed to ensure good performance against electrical stresses with some decent margin. In this research study, the amount of external decoupling and filtering has been reduced intentionally. The objective is to reduce the bill of materials of the complete application and thus to diminish the cost for the equipment manufacturer. With this lighter configuration, and by running ESD simulations, it has been possible to discover a functional weakness. The failure is described in detail in section 3.1.2.

3.1.1 Product description

During testing, the integrated circuit is exposed to discharges while powered and in normal operation. The goal here is to identify functional failures and not hard-failures.

To operate correctly, the chip requires external components and cannot be tested in standalone. The architecture of a typical application containing the chip, its external devices, and interaction with other modules is given in Fig. 3.1. In this application, the system is powered by the battery to the left. The battery and the electronic module are connected with wires and cables. Those cables constitute the most likely entry point for electrostatic discharges.

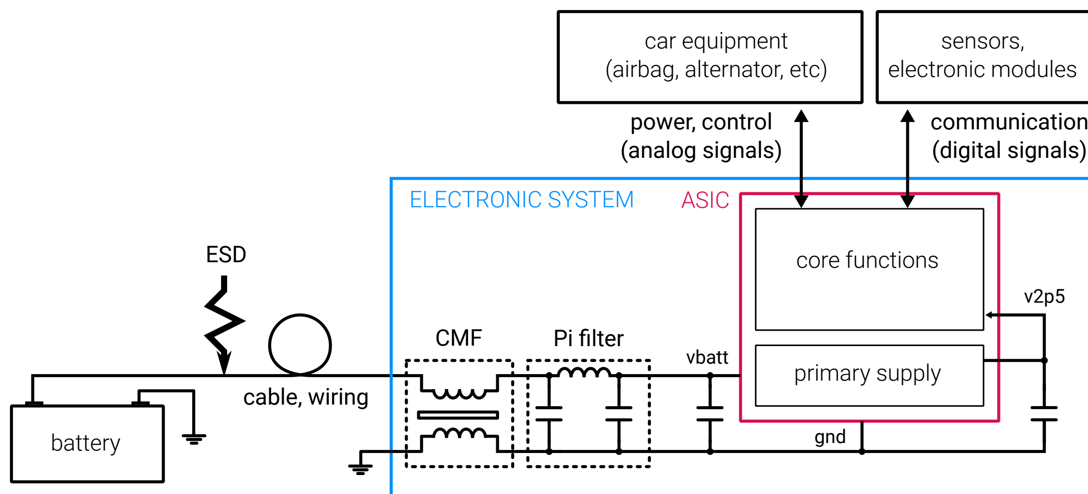

Figure 3.1: Overview of the system architecture

Inside the electronic module (in blue), the ASIC can be found (in red) along with decoupling capacitors for signals V_{batt} and V_{2p5}, and filtering devices. The Common Mode Filter (CMF) and Pi filter are the two main devices being removed in the lighter configuration.

Inside the integrated circuit, two key parts of the circuit have been highlighted. The primary supply is the function being studied in this chapter, and is powered by signal V_{batt}. Its detailed operation is provided later in this section, but overall it is a buck converter that steps down the battery voltage. On the output, it provides a regulated 2.5 V supply (signal V_{2p5}). V_{2p5} is used further in the ASIC, to power the core functionalities of the device constituted of digital cells, low voltage analog functions, communication buses, etc. The core of the circuit interacts with external equipment such as airbags for instance, and communicates with sensors or other modules. Given this system architecture, it is obvious that the V_{2p5} signal is critical for normal operation. The disturbance of this signal could cause a propagation of issues way outside the integrated circuit, impacting other electronic modules and making some functionalities temporarily unavailable.

Integrated supply function description

The next part of the study focuses on the primary supply function found inside the ASIC. Preliminary analysis showed that this function is put at fault during ESD testing. Apart from that, there are two motivations for testing this particular function. The battery input V_{batt} is an external pin, which is convenient to inject test stresses. The regulated voltage output V_{2p5} is also exposed externally, because the function requires a large capacitor for stabilization. This is very convenient to monitor externally the behavior of the primary supply.

The main function of the regulation is to down-convert a battery voltage to a 2.5 V regulated supply. Its architecture is given in Fig. 3.2. Several blocks are involved for processing the battery supply.

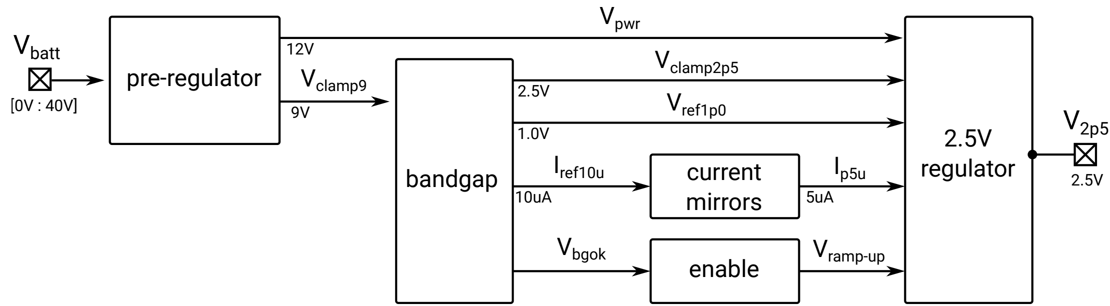

Figure 3.2: Architecture of the primary supply

The pre-regulator clamps the battery input voltage (V_{batt}) that can reach up to 40 V and down to 9 V. The clamped voltage is called V_{clamp9}, has a current capability smaller than a few mA and is used for low-power functions. The second output of the pre-regulator called V_{pwr} provides a 12 V clamped output with a larger current capability of tens of mA.

The bandgap reference, connected downstream, is powered by V_{clamp9}. After a startup delay, it generates a 1.0 V voltage reference on V_{ref1p0}. This reference is stable across a wide range of temperatures, process variation and process mismatches. The bandgap also outputs a 10 µA current reference on I_{ref10u}, and the V_{bgok} flag to signal it is ready for operation.

Finally, the LDO regulator generates a stable 2.5 V supply voltage on the external pin V_{2p5}. This output can deliver up to 20 mA. V_{2p5} is used further in the integrated circuit to power digital gates, like previously detailed. A 100 nF decoupling capacitor is required on V_{2p5} to absorb peak currents and help the regulator achieve stability.

The *current mirrors* provide copied current values from the bandgap to the regulator, while offering much larger output impedance. The *enable* block mostly checks and waits for the bandgap to be properly started. It then triggers a startup ramp-up sequence on the regulator.

3.1.2 Functional failure study

A negative TLP pulse is injected on top of the D.C. supply, connected to the input pin V_{batt}. The width of the discharge is the usual 100 ns, with a risetime of 1 ns. Failures start to appear with pulse amplitudes larger than −80 V. The failure is observed on the V_{2p5} output pin (Fig. 3.4). To perform the injection, the battery is replaced by a D.C. source and a TLP generator. Both devices are isolated from one another using a bias tee, as defined in the DPI standard [53]. This setup is simply a capacitor-inductor network as shown in Fig. 3.3.

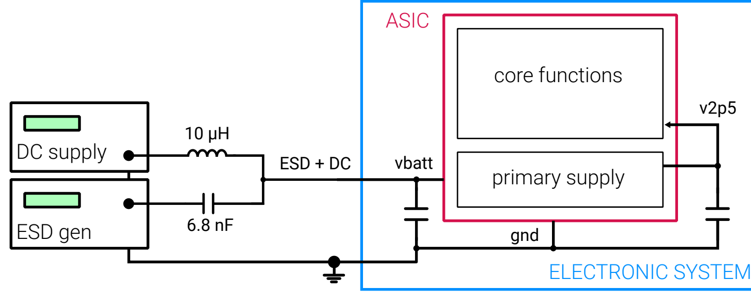

Figure 3.3: Injection setup to superimpose a stress on a DC voltage

The failure signature recorded on V_{2p5} is given in Fig. 3.4. The area of the curve in red corresponds to the entire restart. The nominal value for V_{2p5} is 2.5 V. The TLP pulse is visible at 53 µs. After a small delay of about 2 µs, the regulation function slowly shuts down. The output voltage falls for nearly 30 µs until reaching a voltage of 1.5 V. At this point, the supply cannot reliably power digital gates for instance, and is completely at fault. Afterwards, a new soft-start sequence begins. A soft-start normally happens only during system power-up, when the main external supply is switched on. During a soft-start, the supply voltage slowly rises from 0 V to its nominal value. It avoids overshoots that could damage sensitive blocks, and is a slow procedure that takes tens of microseconds to complete. The shut-down followed by the soft-start lasts in total about 50 µs. It corresponds to the time it takes for the signal V_{2p5} to recover. In comparison, the input disturbance on V_{batt} lasts only 100 ns.

Testing was also conducted using positive stresses, however no failure could be triggered up to the maximum discharge level. The integrated circuit seems much more sensitive to negative discharges. After this preliminary testing on a real chip, the analysis is conducted with simulation tools to understand how the failure appears internally.

A transient simulation of the integrated regulation function is ran. It uses the transistor-level schematic of the function, and its surrounding environment composed of decoupling capacitors, printed circuit board, D.C. sources and test generator. The simulation of V_{batt} is compared to a measurement in Fig. 3.5. The simulation setup reproduces the measurement setup, using the modeling approach presented in previous chapter. During the discharge, V_{batt} has a larger amplitude in simulation, and reaches a more negative voltage. The positive overshoot after the pulse is correctly reproduced,

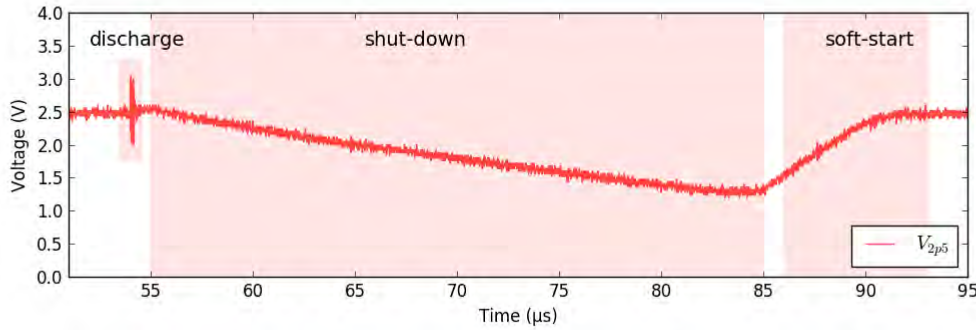

Figure 3.4: Measurement of V_{2p5} after a −100 V 100 ns negative stress

although it dampens slower in the simulation. It looks like the measurement has less bandwidth than the simulation. The accuracy is not great, but it is sufficient to reproduce the failure on the output. Also, the timescale is much shorter in Fig. 3.5 than in Fig. 3.4 and the analysis focuses here on events longer than a few microseconds.

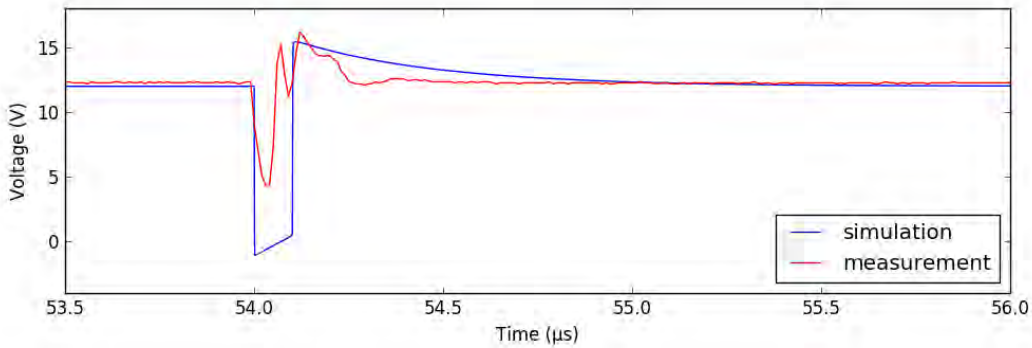

Figure 3.5: Measurement and simulation for V_{batt} (short timescale)

Fig. 3.6 provides the same comparison for V_{2p5}. The reset is clearly visible on both simulation and measurement. The restart happens almost at the same time in both waveforms, at about 32 µs after the stress was injected. Right after the ESD injection, the disturbance amplitude is a bit larger in simulation. But overall, the accuracy is satisfying. Both comparisons tend to indicate that simulations can be trusted to reproduce the failure in this study case.

So far, the waveforms of V_{batt} (external input) and V_{2p5} (external output) were shown. Simulations are now employed to observe the intermediate nets inside the integrated circuit. The waveform for the internal output V_{clamp9} of the pre-regulator is given in Fig. 3.7. The timescale is shorter than the previous curves. At 54 µs, V_{clamp9} is disturbed by the negative stress, in two phases. The first phase is 100 ns wide, and corresponds to the direct exposure to the stress. During this phase, V_{clamp9} reaches as low as 0 V for a brief amount of time. Afterwards, there is a second phase, that lasts ap-

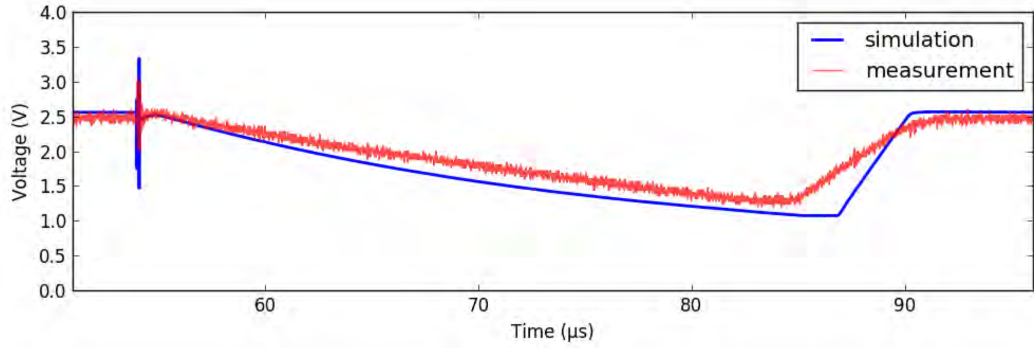

Figure 3.6: Measurement and simulation of the functional failure on V_{2p5}

proximately 650 ns. This second undervoltage will not be detailed but can be explained by the design and architecture of the block. Overall, V_{clamp9} is disturbed for 750 ns.

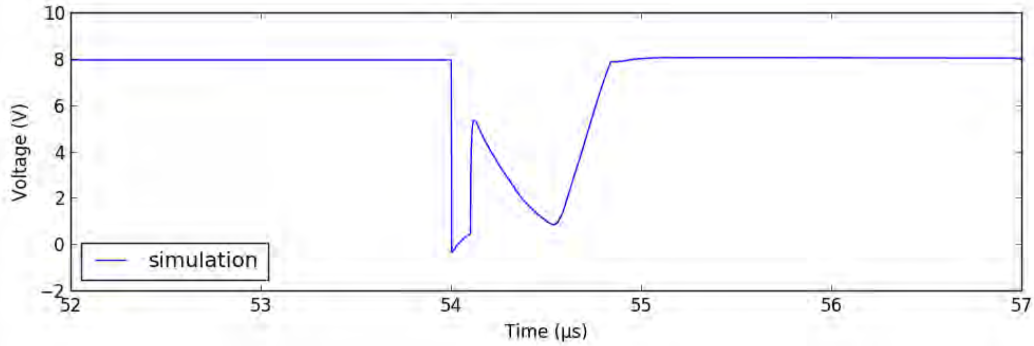

Figure 3.7: Simulated waveform of the V_{clamp9} internal net (short timescale)

V_{clamp9} is used as a power supply for the bandgap reference. The bandgap is expected to be disturbed because of the variation on V_{clamp9}. The observation of the 1.0 V bandgap reference V_{ref1p0} confirms it (Fig. 3.8). The reference drops down to 0.25 V, and is disturbed for about 3 µs.

Finally, V_{ref1p0} is used by the regulator to generate the 2.5 V external supply output V_{2p5}. Previously, Fig. 3.6 showed that V_{2p5} drops below 1.5 V, and is disturbed for more than 30 µs.

There is a clear trend regarding the duration of the failure. In the first block (pre-regulator), the disturbance width increased from 100 ns to 750 ns. In the second block (bandgap), it increased from 750 ns to 3 µs. In the third block (regulator), it reached 30 µs. After each block, there is an aggravation or an amplification of the failure. Ultimately, the final regulation function that takes a lot of time to recover is hit, causing a full system restart.

The next part of this research work is focused on developing measurement methods

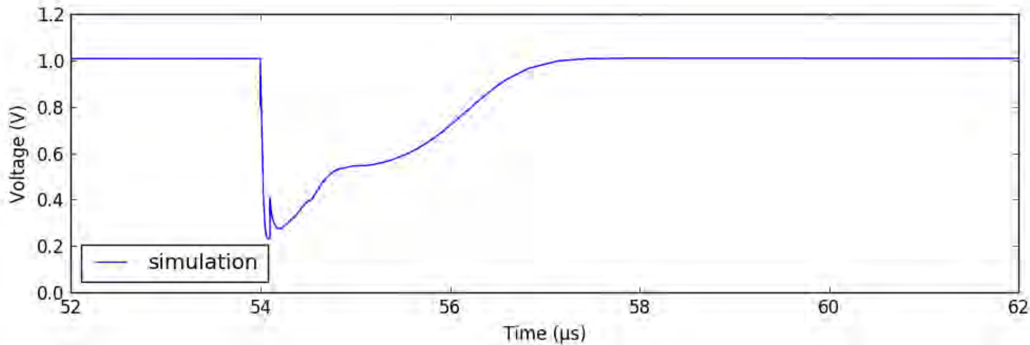

Figure 3.8: Simulated waveform of the V_{ref1p0} internal net

to acquire data at the silicon level, to confirm the simulations. A testchip is designed to validate new measurement and observation methods in section 3.2.1. Modeling methods are explored in section 4.1 as a way to understand and predict these functional issues.

3.2 Test vehicle

3.2.1 Test vehicle description

Integrated circuits are very dense and fragile devices, enclosed in plastic or ceramic packages. It is nearly impossible to measure electrical properties without physical access. For instance, it could be useful to measure the potential at a given net inside the circuit. With integrated circuits, this is not doable and most of the time the external connections are the only points of access. Even with physical internal access, placing micro-probes to contact metal connections can disturb sensitive parts of the device. To overcome these issues, new approaches are required. In this research, custom measurement structures have been implemented directly on-chip. They perform analog measurements at the silicon level.

The global architecture of the testchip is provided in Fig. 3.9. It contains two instances of the regulation function studied earlier in 3.1.

The first instance (right side of Fig. 3.9) is exposed to ESD stresses during tests. It is monitored in multiple points by the measurement and monitoring structures.

The second instance powers the monitoring functions and communication buses. It must not be disturbed by the discharges injected during testing on DC_2 pin. It has its own external supply pin DC_1, isolated from DC_2. Large external filtering and decoupling capability has been setup on DC_1. Except for the ground connection, the two regulators do not share connections.

The on-chip monitoring system is composed of several overvoltage and undervoltage detectors. They monitor voltages of multiple nets inside the supply under test. There are in total 9 detectors in the testchip. Five of them are dedicated to preliminary testing and self-validation, and are not actually monitoring analog blocks. The remaining four

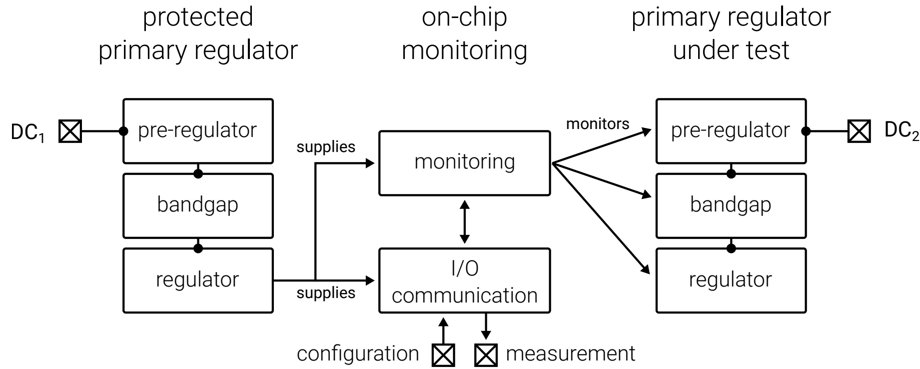

Figure 3.9: Global architecture of the test vehicle

blocks are monitoring the regulator under test (Table 3.1). Overvoltage and undervoltage detector thresholds can be configured externally using a communication bus. When new value is set through the communication, a digital to analog converter generates the new threshold for each detector. The detectors are able to detect level crossings from half a volt up to 13 V, which is designed to match the voltage range of most signals inside the chip.

Name	Nominal value	Function
uv_9V	9 V	UV detection on v_{clamp9} (settable threshold)
ov_9V	9 V	OV detection on v_{clamp9} (settable threshold)
ov_vref1p2	1.2 V	OV detection on bandgap reference (settable threshold)
uv_vref1p2	1.2 V	UV detection on bandgap reference (settable threshold)

Table 3.1: Detectors on core functions

The communication buses provide a connection between the internal detectors and the external world, using digital I/O. Configuration data can be provided from an external microcontroller and measurement data is output by the communication block. There are two readable buses and two writable buses. The first read and write buses are used for preliminary validation of the on-chip monitoring. The second set of buses are dedicated to the monitoring of the voltage regulation function.

The implementation of each monitoring function is detailed hereafter.

3.2.2 Voltage monitoring

Overvoltage and undervoltage detectors are built with latched comparators. A flag is raised if a monitored net crosses a threshold, and stored using a latch, until it can be read. The architecture of a single detector is given Fig. 3.10. The same architecture is used for the overvoltage and the undervoltage. Monitored and reference inputs are just

inversed on the undervoltage detector.

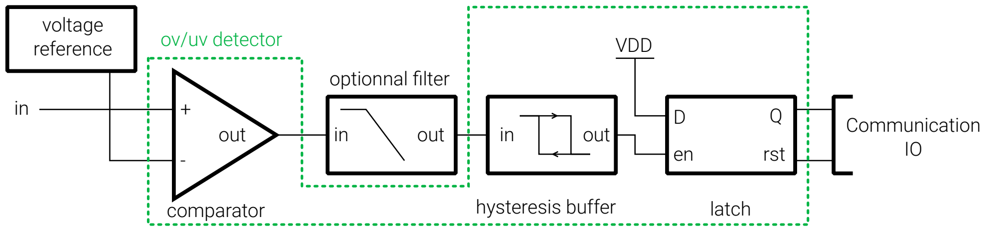

Figure 3.10: Architecture of the overvoltage detector

The first block in this detector is the comparator. It is designed with a two-stage operational amplifier with an output buffer (see Fig. 3.11). This topology is well suited for high-gain, open-loop comparators. This comparator provides a very high input impedance, to ensure the monitored net is not disturbed. A high-gain is useful for limiting the comparator's offset and to ensure that the comparison will be accurate. The offset of the designed comparator is below 5 mV and the switching speed under 20 ns (on a 50 pF load), which should be sufficient to detect fast glitches of several volts amplitude and a timescale similar to electrostatic discharges.

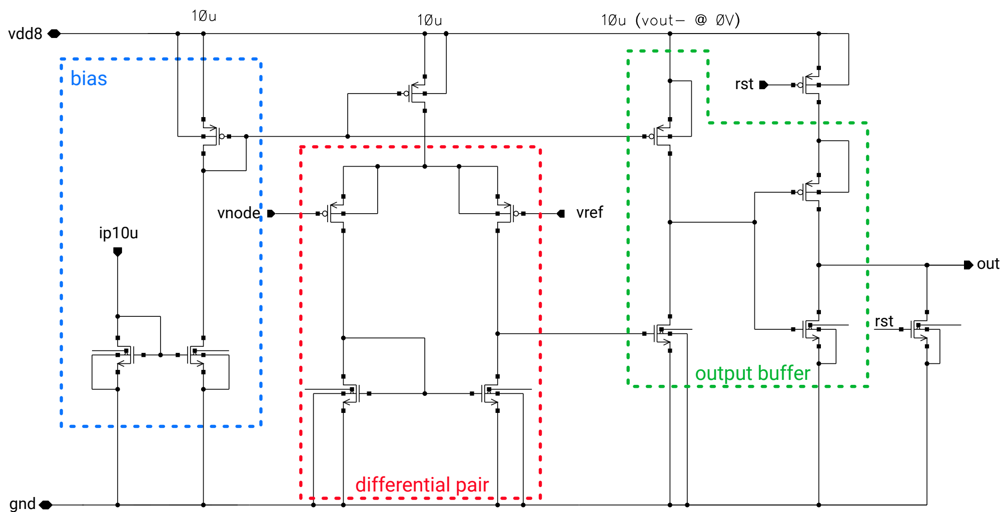

Figure 3.11: Comparator design

On the output of the comparator (Fig. 3.10), an optional RC filter can be connected. This filter can deglitch very short overvoltages, to only let large overvoltages pass through the detector. The strategy behind this filter is to use multiple detectors monitoring the same net, each one with a different filter. In function of which detectors is triggered, an estimation of the overvoltage length can be made.

After the filter, an hysteresis buffer guarantees that a clean digital signal will be fed to the latch. The triggering levels are set quite far away, with the low level near 2 V and

the high level at about 6 V.

Finally, the latch stores the overvoltage flag. By default it stores a low-level. Its copy input D is connected to the supply. If the hysteresis buffer triggers high, the enable pin triggers a copy in the latch. The output Q copies the value from the D, storing a logical high in the latch. This way, any detected overvoltage or undervoltage is stored until it can be read or the latch is reset.

The reference voltages for these comparators come from either fixed-values set by the protected supply, or Digital to Analog Converter (DAC) that can be reconfigured through the communication system.

3.2.3 Communication system

The manufacturing process at NXP for test vehicles requires a 48 pin package. On those 48 pins, a few are already required for ground connection and substrate connection. Each of the two instances of the regulation function needs a supply connection and two external decoupling capacitors. The on-chip current sensor requires 4 pins for the calibration pattern and two pins per actual sensor. In the end, the available pin count would be too small for allowing to connect each detector to its own external pin. To overcome this issue, a custom communication bus has been designed, to discuss with the testchip before and after ESD tests. Initially, the JTAG (Joint Test Action Group) [98] protocol was envisioned for this application. It is a test port for access and boundary-scan. It is commonly used to check that connections are correct between integrated circuits, and to configure internal parameters such as trim values and internal fuses. However, the JTAG system needs a digital state-machine for operation, described in any hardware description language (HDL). This step requires digital-synthesis, a step that converts a HDL sources into electrical netlist. Given the resource constraints in this research work, this step was not available for this test vehicle. Instead, a simplified serial to parallel protocol has been designed from scratch. The main idea is to design reusable communication cells that can be duplicated and connected in a chain fashion, to get a register map of any size easily. Changing the size of the register is simply a matter of adding or removing individual cells. No digital-synthesis is being required.

The chain of individual cells operates by propagating from cell to cell an enable signal. Each time a cell receives the enable signal, it will perform its task, then pass the enable to the next cell at the next clock edge.

Read cell

The read cell is constituted of a tri-state buffer and a D-latch (see Fig. 3.12). The output of the tri-state buffer is set in high-impedance when input x is low. This action releases the communication bus for other read cells and is the default state.

Fig. 3.13 shows the simulated behavior of a chain of 8 reading cells. Signals in green (*en1* and *clk*) must be provided externally, by a microcontroller for instance. Signals in blue (*en2* and *en8*) are internal control signals, to help the cells determine if they have

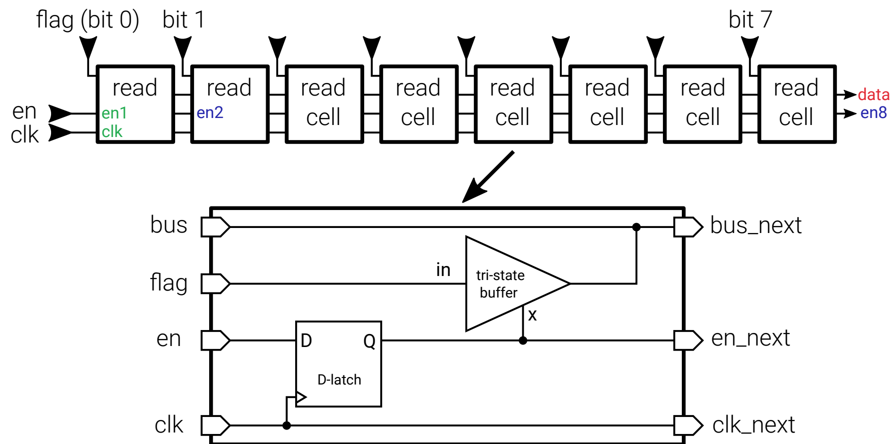

Figure 3.12: Read-only cell design

the right to write on the bus. The signal in red (*data*) is the data output, read by an external microcontroller.

The reading sequence is initiated by setting *en1* high. When *en1* is set high, the output of the first latch (*en2*) switches high at the next clock cycle. This means the first cell has the permission to write on the bus. During one clock cycle, the *flag* is written on *data* bus. At the next clock cycle, the enable signal is propagated to the next cell. The first cell no longer has the permission to write to the bus. The second cell writes to the bus, during a single clock cycle. The process is naturally repeated by the system, until the enable has been propagated to the last cell (*en8*) and all serial data was written.

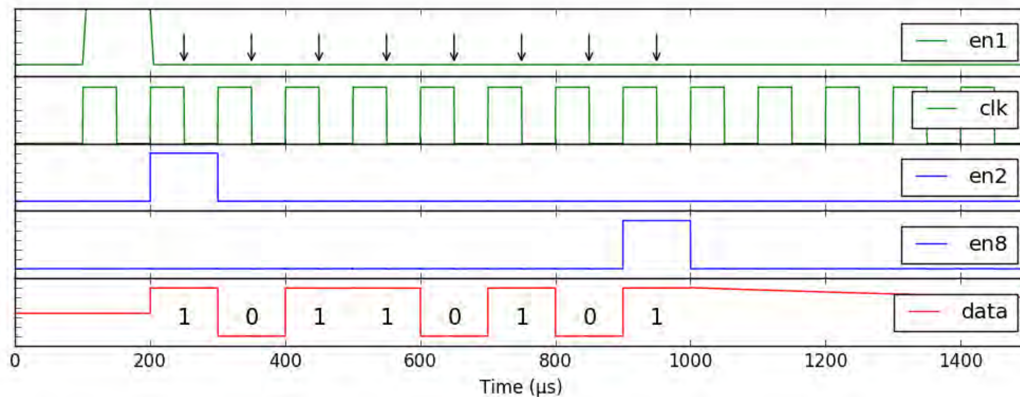

Figure 3.13: Time chart for the read cell

Write cell

The write cell is a bit more complex but operates on the same principle (Fig. 3.14). Data is placed serially by the user on the *bus* line, synchronously with the clock. The enable signal is propagated from cell to cell, so that each cell knows when to sample the bus line and store the value. Basically, this cell sets on its *output* the value on the bus when its enable is high (Fig. 3.15).

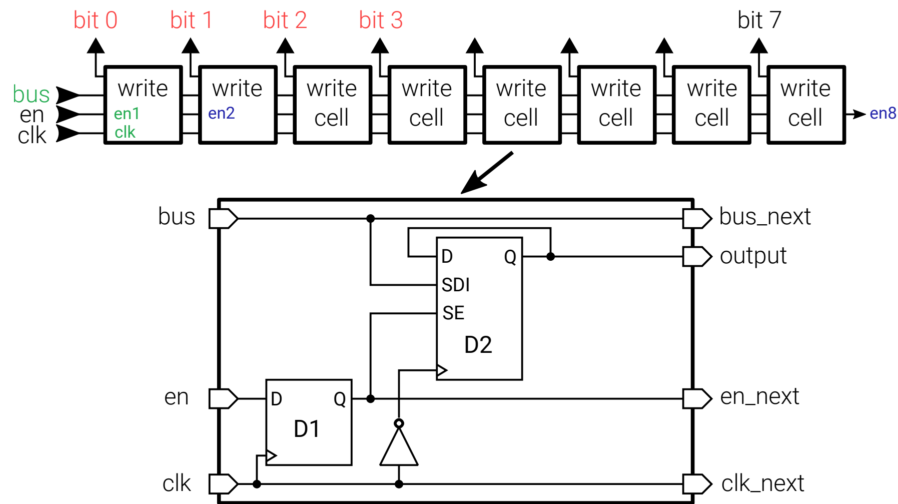

Figure 3.14: Write-only cell design

The truth table of this latch is given in table 3.2. D1 is a synchronous D-latch. The output Q copies the input D on rising clock edges. D2 is a synchronous D-latch with scan. The output Q copies the data input D on rising clock edges, storing a value. When the scan enable *se* input is HIGH, the data input D copies the value of the scan data input (*SDI*), effectively changing the stored value.

D	SDI	SE	CLK	Q
0	-	0	↗	0
1	-	0	↗	1
-	0	1	↗	0
-	1	1	↗	1
-	-	-	↘	Q

Table 3.2: D-latch with scan truth-table

Fig. 3.15 shows the simulated behavior of a chain of 8 writing cells. Signals in green (*en1* and *clk*) must be provided externally. Signals in blue are internal control signals, to help the cells determine to who belongs the data on the bus. The signals in red (*bit 0* to *bit n*) are the data output, set on each individual output bit. Ultimately, the

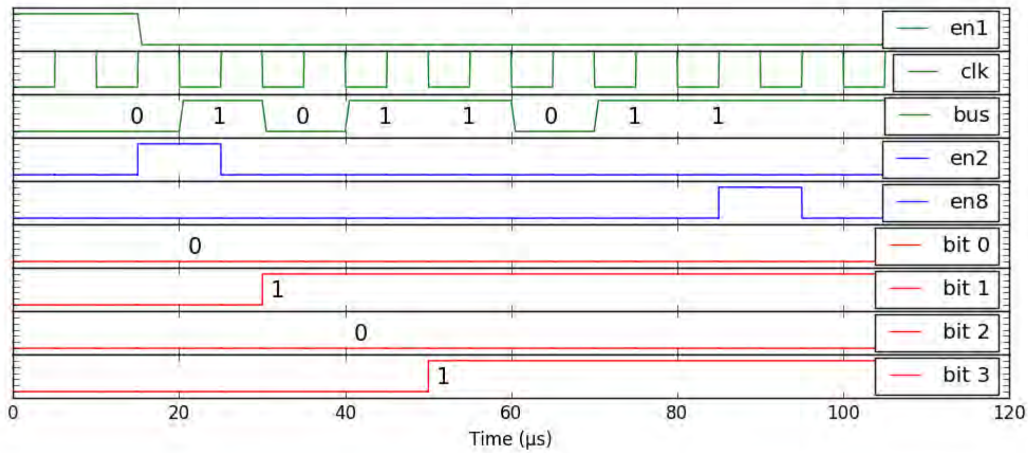

Figure 3.15: Time chart for the write cell

reading-cell performs a serial to parallel conversion. The serial data is set on *bus*, and the parallel outputs are *bit 0* to *bit n*.

3.2.4 On-chip near-field current sensors

Current sensing magnetic loops were integrated on silicon to measure current through a few critical nets. They are sensitive to currents circulating nearby, and were placed close to metal tracks in which current must be measured. By coupling, the sensor generates a voltage proportional to the derivative of the current in the track. Figs. 3.16 and 3.17 give respectively a visual representation of the metallic loop and its layout. This kind of integrated loop was studied in [99, 100, 101, 102].

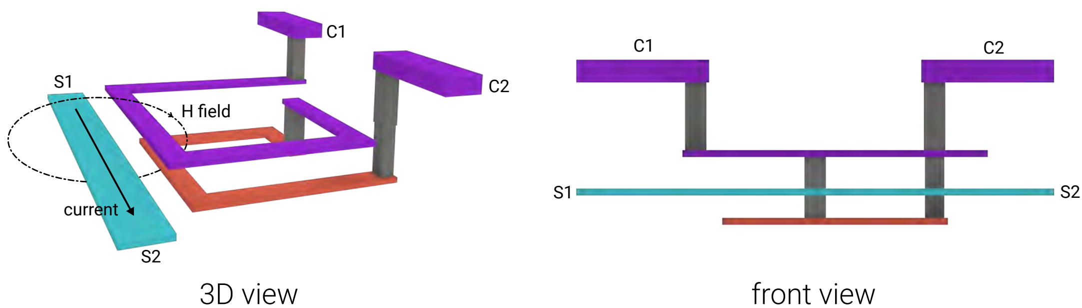

Figure 3.16: Near-field current sensor design

On silicon, three levels of metal are used to build the loop. The first level (in red) and the third level (in purple) form a circle. Metallic vias connect both levels to close the loop vertically. Finally, the sensed current is at the second level (pale blue), and circulates between nets *S1* and *S2*. An oscilloscope with 50 Ω input impedance performs

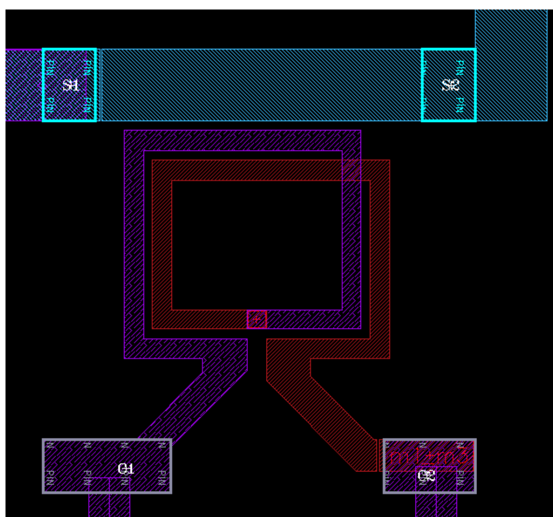

Figure 3.17: Near-field current sensor layout

a differential voltage measurement between pins *C1* and *C2*. An example of waveform obtained by injecting a rectangular pulse is given in Fig. 3.18. The obtained waveform requires specific post-processing to reconstitute the original current waveform. The post-processing is detailed earlier in section 2.4.

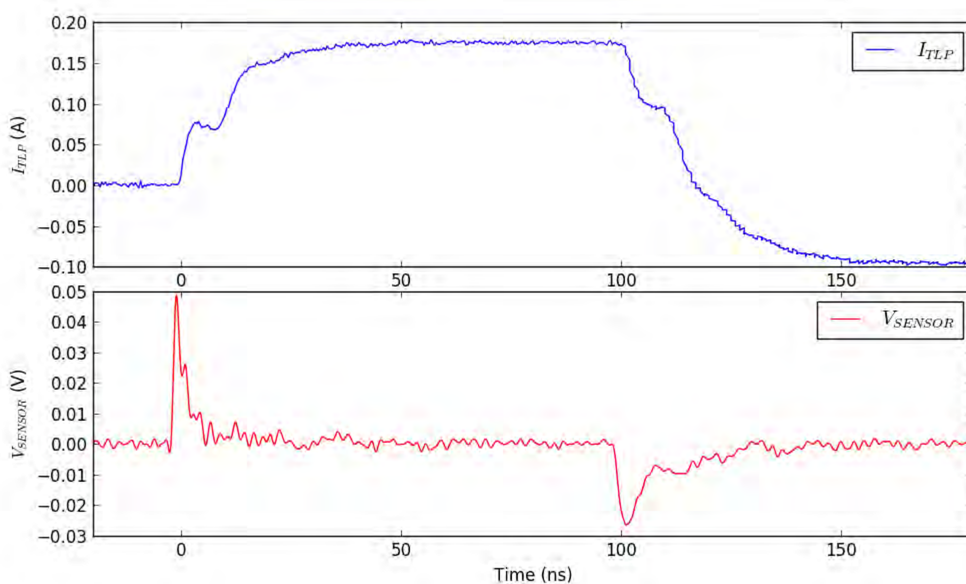

Figure 3.18: Waveform measured with an oscilloscope connected to the on-chip near-field sensor

In total, there are 6 near-field current sensors located on the device. The 6$^{\text{th}}$ sensor

is dedicated to calibration. The others are placed strategically on main I/O susceptible to be disturbed directly or indirectly by ESDs. Sensor *1* measures the current on the supply under test power input. During testing, this pin is exposed to ESDs coupled on top of a DC supply voltage. Internally, this input is protected by a large ESD protection, able to sustain IEC 61000-4-2 ESD gun discharges. Sensor *2* measures the current absorbed and deviated by the ESD protection into the *gndsub* metal ring (local ground reference). Sensors *3* measures the current flowing to the external stabilization capacitor of the regulator under test. Finally, sensors *4* and *5* measure the currents flowing from the *gndsub* metal ring into the external ground pins, connected externally to the board ground.

3.2.5 Topcell

The primary supply chain under test is directly extracted from a real product, described in 3.1.1. It is placed in appropriate operating conditions on the testchip, and behaves identically to the real product. Except for the two supply blocks, all the functionalities described previously were designed, simulated and the layout drawn. All layouts were assembled together to form the topcell (Fig. 3.19).

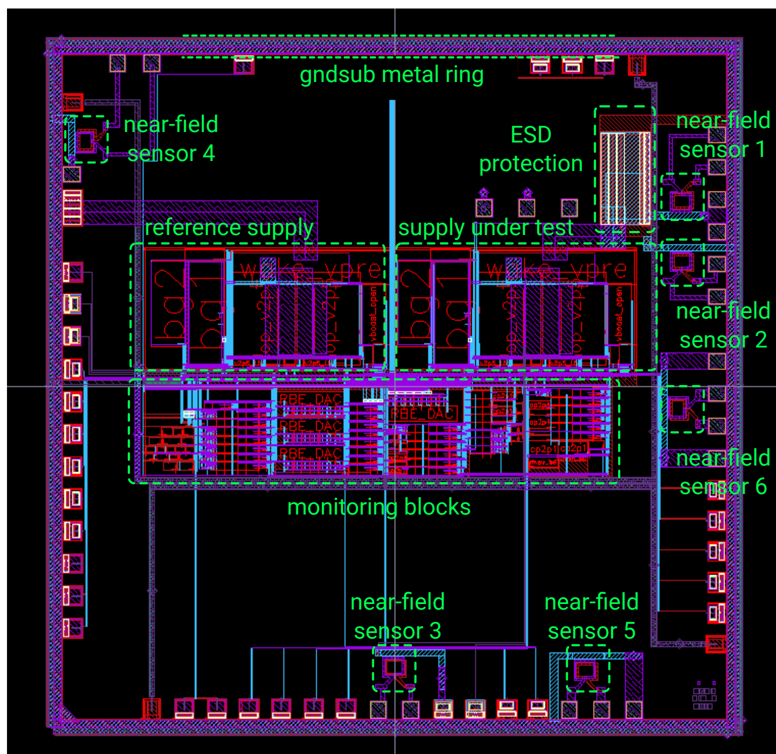

Figure 3.19: Top-cell layout

On the layout, a lot of silicon space was left empty. This is due to manufacturing constraints that enforced the silicon dimensions. After manufacturing and packaging,

the chip is tested. The entire testing process and results are documented in section 3.2.7.

3.2.6 Test boards

For providing the external devices required by the testchip, and communicating with it, a master-slave architecture has been chosen. The testchip is the slave, because it receives commands from the master for configuration and responds to reading requests. One PCB is designed for the master, and one for the slave. The slave board contains the testchip and the required external devices. The master board contains the microcontroller responsible for generating the frames for the testchip's monitoring system (section 3.2.3). The master board connects to a computer for providing a user interface, reading, writing and storing the monitoring data.

To protect the computer from ESD discharges, the two boards are isolated electrically. Each board is powered with its own isolated battery, to avoid conducted stress propagating in the AC supply network. The communication between the two is achieved with several optical fibers. Optical communication is ideal because it completely isolates both boards electrically, and the fiber itself is completely immune to electrostatic discharges and more generally to electrical disturbances. Each board packs its own set of optical to electrical converters, to make the conversion between the fiber and electrical signals.

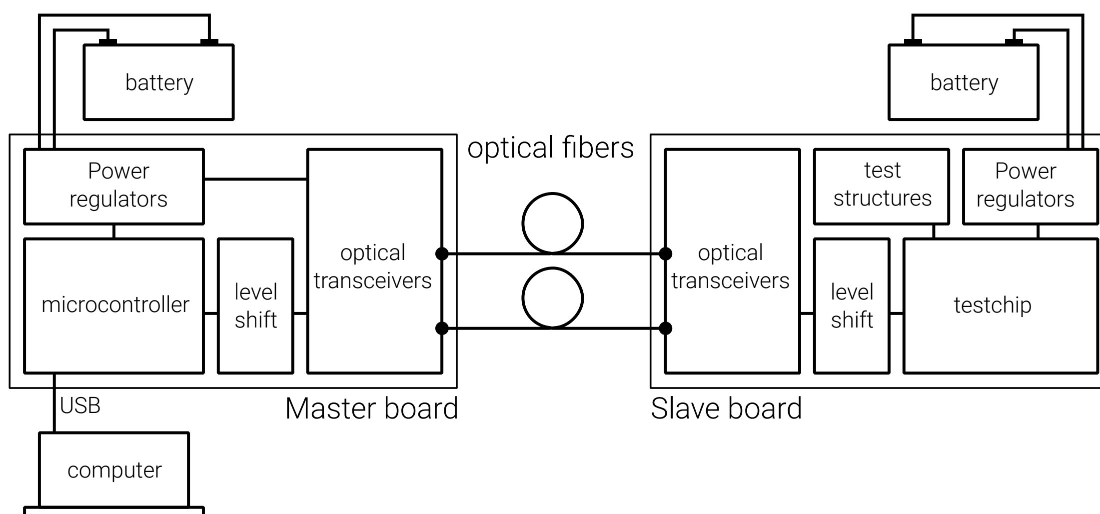

Figure 3.20: System architecture

A picture with both boards is given in Fig. 3.21. The microcontroller of the master board (on the left) is not visible because it is located on the other side. Two supply inputs are available on the slave board (on the right). The reference supply powers the monitoring block (and is heavily filtered at the board level as detailed before). The dut

supply powers the functions of the testchip that are tested and exposed to electrostatic discharges.

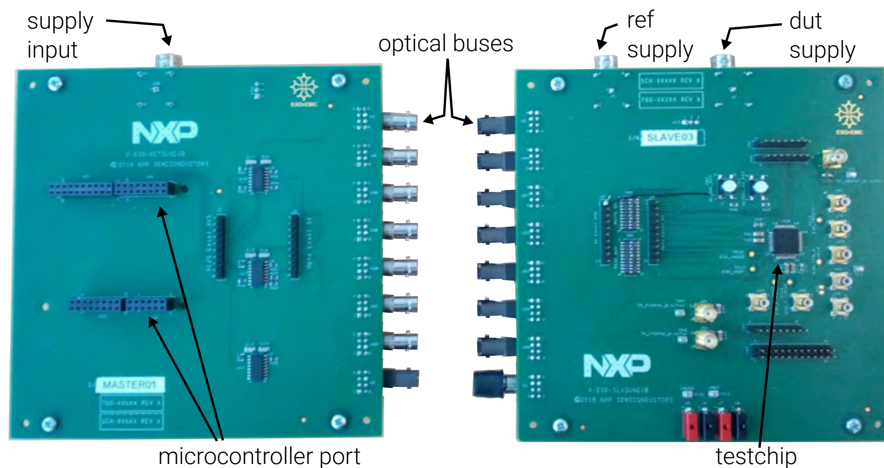

Figure 3.21: Picture of master and slave boards

3.2.7 Test vehicle verification and testing after manufacturing

The testplan for the testchip is constituted of 7 steps, described in Fig. 3.22. The verification of the on-board voltage regulation is checked with a voltmeter, to ensure that a regulated 12 V is well established. The on-chip regulation is checked with a voltmeter and observed with an oscilloscope to validate the behavior. All regulators from both boards and inside the testchip were found to operate as expected.

Optical communication

The communication between the optical transceiver is verified. Both the microcontroller and testchip were disconnected prior to injecting test frames on each transceiver. Then, the output of the matching receiver was observed to ensure that the frame was properly transmitted. Overall, minor issues were identified and corrected, and the boards were found functional. This validates the physical layer of the communication.

Master-slave communication

The complete communication is then tested. The microcontroller is used to send command frames such as reading requests on configuration data. The testchip is supposed to respond each time with some specific data in return. Unfortunately, very severe issues were found with this system. After extensive debugging and testing, it was concluded that the communication could not work as-is and needed corrections. As will be detailed later, the issue did not originally appear in the set of simulations ran during design to

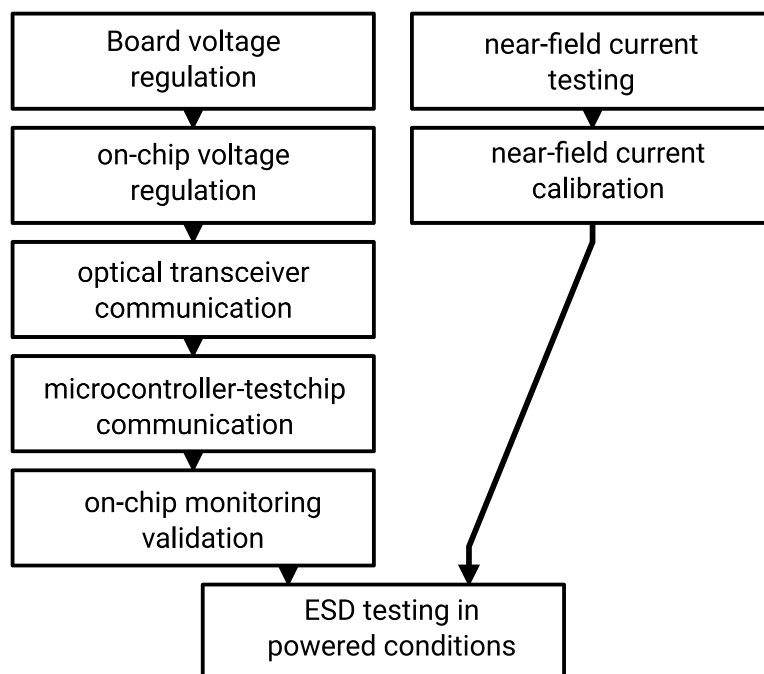

Figure 3.22: Test plan

validate the entire test vehicle. It required complex debugging steps such as parasitic devices extraction from layout to only partially reproduce the issue.

The test is conducted by sending a reading frame multiple times. By design, the integrated communication system expects a *clk* signal with a frequency lower than 2 MHz, and an *en1* signal that must be high for a single rising clock edge. With both these criteria met, the communication system should return the data on the *data* pin.

By design, each frame incorporates a few mechanisms to ensure the returned data is correct. Any *data* frame must start with binary code 1010 and end with binary code 01. The *en1* signal set on the external input is propagated from one read cell to the next one. The last cell of the chain is connected to the output pin *en_out*. Confidence in the data is increased if the *enable* signal (a pulse with a width of a single clock period) is observed on *en_out*,

After attempting multiple readings with the same board, with different boards and different clock frequencies, the results are inconsistent. Sometimes, the communication system returns an incomplete frame like in Fig. 3.23. In this case, the enable signal is not propagated correctly through the chain. The *en_out* signal (not displayed here) stays low all the time.

In other cases, the chain returns a complete but corrupted frame like in Fig. 3.24. The enable is correctly propagated, and is visible on *en_out*, however the data start pattern is not correct (b'1011 instead of b'1010) and some intermediate digital values are not clearly defined.

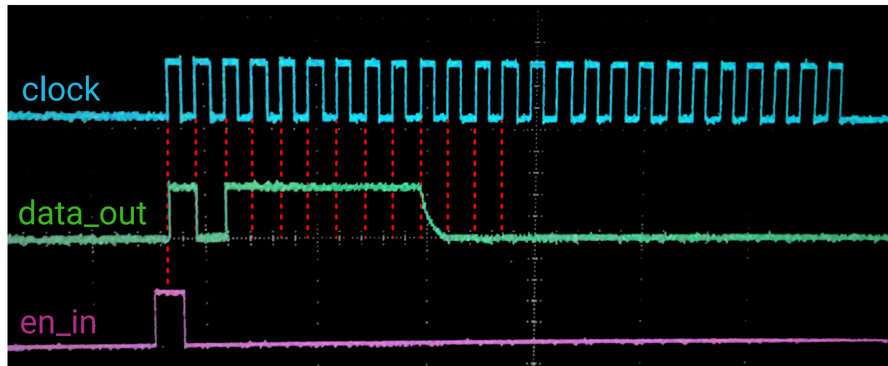

Figure 3.23: Read-only partially returned frame (4 ms/div, 5 V/div) - clock frequency 1 kHz

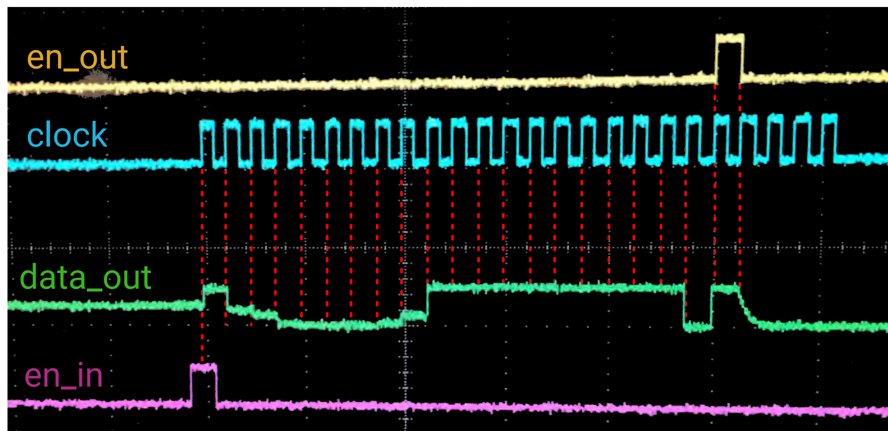

Figure 3.24: Read-only corrupted frame (4 ms/div, 5 V/div) - clock frequency 1 kHz

The clock frequency was initially suspected as a root cause for the problem. Previous measurements were taken for a slow 1 kHz clock frequency, which is far slower than the upper limit 2 MHz. Increasing the clock frequency at 10 kHz, 100 kHz and 1 MHz did not improve the situation.

The impact of parasitic delays causing the communication system to malfunction was also suspected. Multiple simulations of the entire read chain were run by placing large delays in multiple locations. No failure could be highlighted using this method.

Afterwards, RC parasitic device extraction was performed using the layout. All previous validation simulations were ran, without any success in finding the issue. For all simulations, the read chain performed correctly.

Substrate couplings were also suspected. Some reading issues could be reproduced, but this type of coupling is highly unlikely to happen for clock frequencies of 1 kHz.

Future work

A second revision of the testchip is planned. Since the investigation on the communication system is inconclusive, it was decided to remove it until the root cause of failure could be determined. Instead, detectors will be directly connected to pads, and most test or validation structure will be removed. To overcome the problem of low available pin count, it is possible to put on silicon more pads than the amount of external pins. Then, two different bonding diagrams will be made to connect each part of the available pads, to be able to use all detectors.

Chapter 4

Modeling methods for functional robustness prediction

The design flow of integrated circuits relies on circuit schematics, a symbolic view describing an electronic circuit. Those schematics are converted into a netlist composed of all components inside the schematic and connections between them. At silicon-level, these components are mostly capacitors, resistors, and transistor devices. Each element is described by a mathematical, physical or algorithmic model which is a representation of their behavior. In electronics, models usually link current and voltages at the different terminals of the device, and can accept external parameters such as temperature. With the netlist and the model library, the simulator knows the stimuli, the devices and the connections inside the circuit. It is able to simulate the circuit behavior, allowing for validation of the functionality very early in the design phase. As detailed in the global introduction, this is the main reason why simulations are so valuable and why simulation tools for ESD can avoid late and costly mistakes.

In the automotive field, ASICs used in electronic modules integrate a lot of functionalities. They must communicate with external sensors, process and interpret the data, then apply commands on other external devices. It is a lot of functionality to pack into the integrated circuit. In return, schematics are very complex and dense. To organize the design, a hierarchy is set in place, similar to a tree. The top-level cell has child cells themselves having child cells, until root cells composed of transistors, passive devices, etc. After the architecture definition, the transistor design phase starts from the bottom of the hierarchy. Basic blocks are designed with library devices, then blocks are connected together in rising complexity up to the top to match the conceived architecture. For that reason, the block design phase is usually called bottom-up. After the design phase, all the schematic views are converted and drawn into a layout view. The layout view represents the set of masks and layers that will be used during manufacturing to build the circuit.

Simulating the injection of an ESD into the circuit is rather challenging, because the simulator must solve voltage and current in all circuit nodes, while dealing with very fast and large amplitude ESD signals. It raises big convergence issues, that can prevent

the simulation to complete. When the simulation does complete, simulation time can be very important. To successfully debug a circuit, it takes multiples iterations and design tweaks to reach the desired goal. Therefore, the investigation time can be rather large.

Also, those models and schematic are not perfect and do not take everything into account. Parasitic devices can be extracted from the layout, but it requires the layout to be completed, which is not possible before nearing the end of the design flow. Also, extraction is a time consuming and complex task, that takes quite some time to be computed. Finally, some phenomena such as substrate coupling are simply not reproduced and need special tools for simulating them.

The System Efficient ESD Design (SEED) methodology is a novel approach for efficiently designing ESD robust applications. It is a significant trend in the ESD field supported by the Industry Council [103]. This methodology recommends a global approach where the ESD robustness is handled by both integrated circuits and electronic modules. The goal of this method is to provide the most efficient and cost-effective solution for designing products, with a combination of protections at the system level and at silicon level. So far, SEED applies to hard-failure of electronic systems. It is believed that this trend will also apply to soft-failure once the topic starts to be more experienced by the community. The major lock nowadays is the lack of analog IC function models that can be freely distributed, and that would allow equipment manufacturers to perform complete ESD simulations with the integrated circuit model.

Black box models are a potential solution to the issues and limitations described previously. They only reproduce the behavior of the device from an external point of view, without knowing intrinsic details. Because they abstract all the inner complexity, and are much simpler, they help drastically reducing simulation time of transistor-level schematics. They also hide the inner functionality and design details. They can be distributed freely without revealing intellectual property.

In this chapter, three different kinds of modeling approaches at the integrated circuit level are explored. A bottom-up modeling method is presented first. It focuses on mathematically modeling the interaction between an input and an output of individual block functions inside the chip. Those individual blocks can then be chained together to deduce the behavior of the complete functionality against a transient disturbance, using a much simpler model than the transistor-level schematic. A similar method is applied to a complete IC function. The goal is a bit different because the goal is to simulate electrically an IC function with a black box model. A characterization approach is presented, and current limitations are highlighted.

A common point between the proposed methods is to use the Wunsch and Bell (WB) technique [104], outside of its usual application scope. In the ESD field, WB is generally employed to estimate the hardware robustness of a device in function of a stress amplitude, width, risetime, or any other electrical parameter. The typical characterization process consists in injecting a set of rectangular pulses (Fig. 4.1) on a tested device, and observing for which pulses a destructive failure occurs. A TLP generator is often employed to generate pulses of parameterized amplitude. Pulse width variation on a TLP can also be easily achieved by using a longer charging cable. In this research work,

the WB approach is proposed as a non-destructive characterization tool. A set of parameterized pulses are injected on the input of the item under test while the output is being monitored.

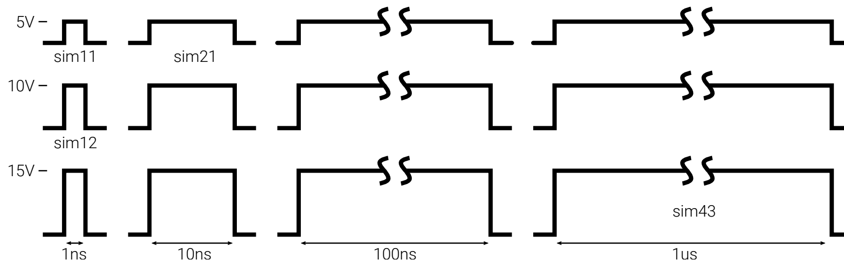

Figure 4.1: Typical set of parameterized characterization pulses

4.1 Intra-chip block modeling

4.1.1 Block failure characterization and modeling method

The modeling method presented in this section focuses first on studying low-level cells of the circuit. They are characterized individually, leading to the definition of a failure model for each cell. In a second step, the individual models are linked together. The connection between the models reproduces the connections between the cells in the actual circuit. Finally, an electrical stimulus such as an electrostatic discharge is fed on the input of the first model. It is applied on this model that produces an output signal. In turn, this signal is used as stimulus for the second model in the chain which is using it as input. The process is repeated until the last output, where the output signal represents the shape of the disturbance after going through the entire chain.

The main perk of this characterization method is the modularity, because each block is characterized independently of the others. The model built for each cell is reusable, and once the characterization is done it does not need to be repeated unless modifications are brought to the circuit. This method is called bottom-up because low-level functions components are characterized then assembled to model higher-level functions, rising from the bottom of the hierarchy to upper levels.

The motivation for modeling blocks individually is that a single block can be failing but the error can remain internal. Complete function can continue to operate without changes. In the other way around, not all blocks need to be failing in order to cause the complete function to fail as well. It is important to determine which blocks may be in fault to be able to fix the problem. This is why the characterization method presented here focuses on blocks and not complete functions.

The goal of this method is to build a propagation model and not an electrical SPICE model. The models built here are not usable directly in standard simulations and does not produce actual waveforms on their outputs. Instead, they represent input and output

waveforms by bounding boxes of a given amplitude and width. The methodology is built on the hypothesis that simplified ESD waveforms could be sufficient to estimate the robustness of an integrated function. This hypothesis is validated in the document.

Several refinements of the modeling methods were applied to solve issues as they were encountered. This chapter gives a logical history of those improvements in order to understand the starting phase and the corrective modifications. Initially, Wunsch and Bell characterization [104] is used to determine failure levels of individual cells when exposed to stresses of different width and amplitude. A single failure criteria was preliminary established for each model. It usually took the form of a voltage threshold applied on the output of a cell, above which a fault is recorded. This threshold is set prior to the simulation, and there is no general rule for setting it. The D.C. specification of the output can be used directly, if it exists, or a sound value in regard of the design, or an arbitrary level.

The first part of the modeling method is the characterization of each block using the electrical setup of Fig. 4.2 in a SPICE simulation environment. This setup provides appropriate biasing to the block with V_{DC} voltage source, in order to set the block function in operating conditions. It also enables the injection of the characterization signal on the tested input with V_{stress} transient voltage source. The characterization pulses are rectangular waveforms similarly to the Wunsch and Bell technique. Each simulation runs with a different pair of values for the **amplitude** and **duration** of the square signal. On the other side of the cell under test, the output is monitored. Prior to the simulation, a failure criteria consisting of a voltage threshold is set. If the output waveform goes above this threshold, the simulation is tagged as *fail*. The threshold is chosen depending on multiple parameters such as the functionality of the block or its DC operating point.

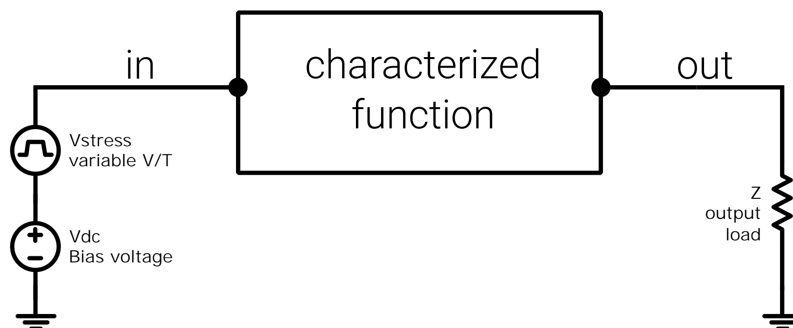

Figure 4.2: Block characterization setup (supply input)

The results can be summarized into a table. An example is provided with table 4.1. The simulations in red contain a fail, meaning that the output voltage crossed the failure threshold.

A curve can be built from this table to give a visual representation of the functional

	1 ns	10 ns	100 ns	1 µs
15 V	sim13	sim23	sim33	sim43
10 V	sim12	sim22	sim32	sim42
5 V	sim11	sim21	sim31	sim41

Table 4.1: Example of results on a set of simulations (x-axis: pulse width, y-axis: pulse amplitude, red color corresponds to a detected failure)

robustness of the block (see Fig. 4.3). The x axis is the duration of the input stress. The y axis is the amplitude of the input signal during the stress. The color of the curve (red or green) corresponds to the presence or absence of failure at the given input amplitude and width.

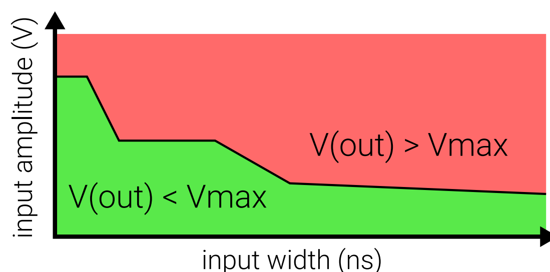

Figure 4.3: Visual representation of powered-on block testing results

Presence or absence of a failure is not the only information that can be obtained by monitoring the output. Because soft-failures are temporary issues, their duration is also very relevant. Using the same characterization setup as before (Fig. 4.2), it is possible to also measure the duration of a failure. It is possible to improve table 4.1 by replacing the fail or no-fail flag by the duration of the fail. This is illustrated in table 4.2. With those example values, for an input pulse stress of 5 V with a input pulse width of 1 ns, no failure was recorded. On the other hand, with a 5 V 1 µs stress, a failure was recorded and the output waveform crossed the threshold during 2 µs. A 15 V 2 µs stress caused a failure that lasted 30 µs.

	1 ns	10 ns	100 ns	1 µs
15 V	110 ns	150 ns	30 µs	30 µs
10 V		125 ns	540 ns	30 µs
5 V				2 µs

Table 4.2: Example result set containing failure width information (x-axis: pulse width, y-axis: pulse amplitude, a warmer color corresponds to a longer failure)

This improvement can also be transfered to the curve representation. A gradient is used rather than a fail or no-fail area. The gradient color for each location corresponds to the failure duration the output. The figure 4.4 provides an example of this improved representation. In this figure, the warmer the gradient, the longer the output is disturbed.

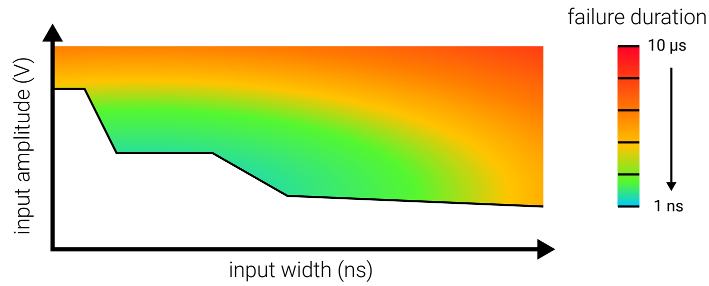

Figure 4.4: Improved curve for Wunsch and Bell powered-on characterization

The gradient can also be discretized into a few areas for better legibility as shown in figure 4.5. This representation looses some information compared to the gradient one but is easier to generate and read.

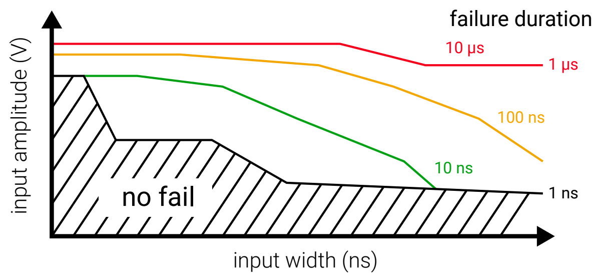

Figure 4.5: Improved discrete curve for Wunsch and Bell powered-on characterization

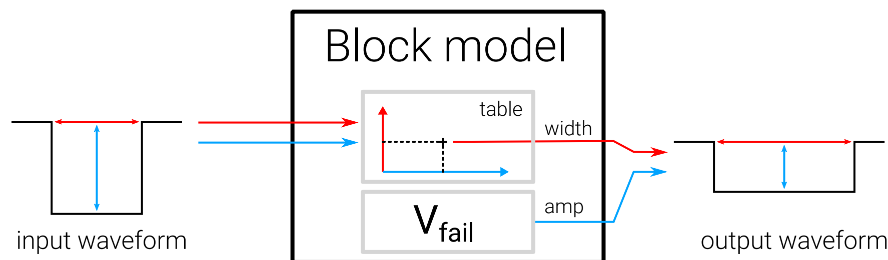

Figure 4.6: First modeling method

The model accepts a rectangular input waveform and returns a rectangular output

waveform (Fig. 4.6). More specifically, the width (red arrow) and the amplitude (blue arrow) of the input signal are the two parameters required by the model. Those values are fed to the characterization table to calculate the width of the output signal. The failure criteria V_{fail}, employed for establishing the characterization table, is also used directly as amplitude value for the output signal. Using the failure criteria for modeling the output amplitude is a large approximation and validity of this approach is checked in the next section. Ultimately, the goal is to investigate whether or not a fixed failure threshold is suitable for ESD functional analysis.

In the next section, those individual block models are chained together to deduce the robustness of a complete function. The process is explained in detail and is later validated with a real case study.

4.1.2 Block models chaining

This section presents the second phase of the method that consists in chaining individual block models to predict the robustness of a higher-level function. To present this concept of chaining models, a purely hypothetical example is taken first. The characterization process detailed previously is performed on two different blocks, called *A* and *B* (see Fig. 4.7). Those two blocks are part of an higher-level function. The function has an external input (called *in*) and an external output (called *out*). A stimulus is injected on the external input and the job of the model chain is to predict what will be the approximate waveform on the external output. Both blocks were previously (hypothetically) characterized and failure criteria V_{fail} for block *A* is 5 V and 2 V for block *B*. In practice, the threshold selection is done either from the block specification or datasheet, or directly from its design.

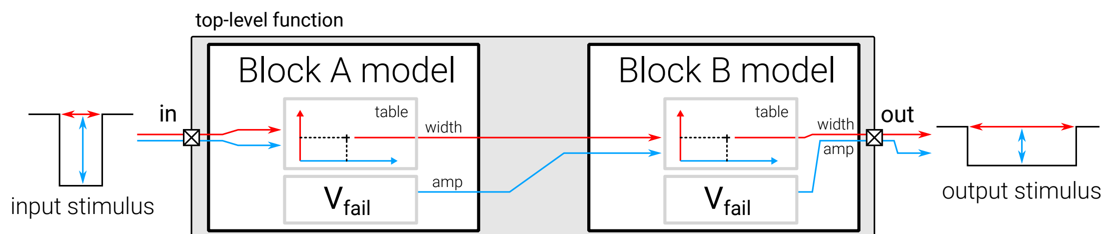

Figure 4.7: Top-level function model constituted of 2 blocks

The input stimulus is a rectangular 100 ns wide pulse with a 15 V amplitude. Those two properties are fed into the characterization of block *A* (Fig. 4.8). In the graph, multiple curves can be identified, each corresponding to a boundary between two disturbance durations. For a point located below the green curve (with label "10 ns"), no stress was recorded on the output. For a point located above the 10 ns curve and below the 100 ns curve, a stress was indeed recorded with a duration comprised between 10 ns and 100 ns. The exact value between those two boundaries is not known with this kind of visualization. In the analysis, the lower boundary is always chosen because the output

is disturbed for at least this value.

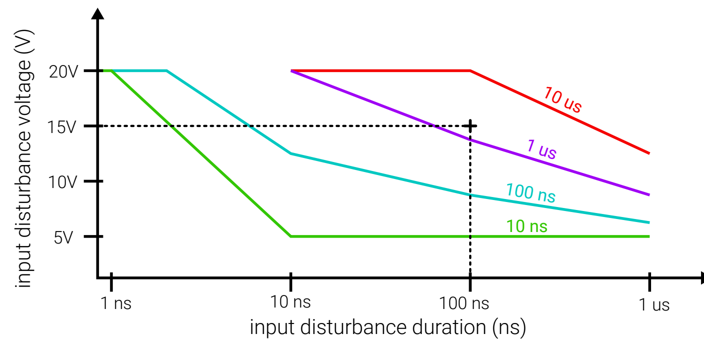

Figure 4.8: Model A curve and determination of impact of the TLP pulse - values in color represent the duration of failure on the output

With the given 15 V 100 ns stimulus, the curve predicts that the output will fall down below 5 V (V_{fail} of block A) during 1 µs. Those two values describe the signal on the output of block A. Those values are now used to describe the stimulus on block B, since both blocks are connected. The failure criteria that was used to extract the characterization curve also serves as amplitude for the output signal. It means that with a 5 V failure criteria, if a failure is recorded, the output waveform is approximated to also have an amplitude of 5 V.

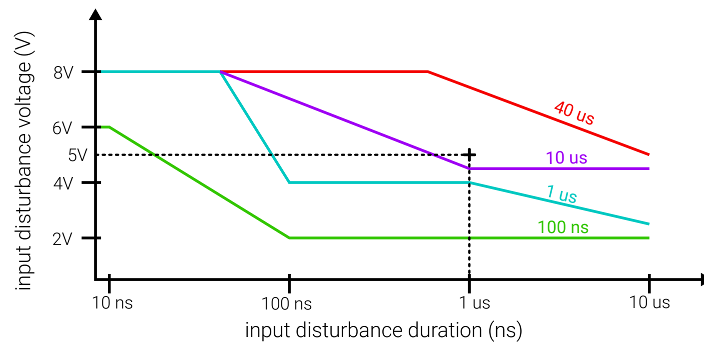

Figure 4.9: Model B curve and determination of impact of the TLP pulse

Fig. 4.9 shows an example curve for model B. The location of the stimulus from block A (5 V and 1 µs) is also placed on the curve. The curve predicts that with this stimulus, block B will be disturbed during 10 µs with an amplitude of 2 V (V_{fail} of block B).

This process can be repeated in theory with as many blocks as required by the original design, until the final pin is reached.

4.1.3 Application to the test vehicle

The method described in both previous sections (4.1.1 and 4.1.2) is tested in simulation on the voltage regulation function of the testchip. The testchip was presented in section 3.1.1, and it was shown that negative rectangular pulses can generate functional failures in it. The regulation function is composed mostly of a pre-regulator, a bandgap and a regulator.

One input and one output per block were selected (Table 4.3) for validating the characterization method. V_{batt} is the input pin of the pre-regulator and is also exposed externally. It is the battery input connection and constitutes a very likely ESD entry point. Nominal voltage on this pin is expected near 14 V.

V_{clamp9} is a 9 V output supply from the pre-regulator and an input for the bandgap. The bandgap block cannot operate without this supply voltage. This is why this pin was selected for the characterization. The failure criteria is set at 0 V, corresponding to a level where the ESD causes V_{clamp9} to go negative, which is a worse situation than without any DC supply.

V_{ref1p0} is the 1 V bandgap output reference. It is the main signal required by the regulator to produce the final 2.5 V V_{2p5} regulated supply. Failure criteria of V_{ref1p0} is chosen at 0.5 V, half the operating voltage. The choice of this particular level is not strict and another value could have been chosen.

V_{2p5} is the output of the regulator and the last signal in the considered function. It is an external node, that requires a large 100 nF decoupling capacitance. This output is used further in the original circuit to supply digital cells. The failure criteria for this net is chosen at 2.1 V. Below this value, digital cells are no longer guaranteed to operate properly.

input pin	DC value (V)	stress amplitude	stress width	output	fail criteria
vbatt	14 V	−1 V to −10 V	1 ns to 1 µs	vclamp9	< 0 V
vclamp9	9 V	−1 V to −15 V	10 ns to 10 µs	vref1p0	< 0.5 V
vref1p0	1.0 V	−0.5 V to −10 V	10 ns to 10 µs	v2p5	< 2.1 V

Table 4.3: Selected pins for characterization and characterization limits

Per-block characterization

The characterization is done using negative voltages, to reproduce failures observed previously with the testchip. It was observed for a sufficiently high negative voltage that a short pulse can cause a full restart of the primary supply and the V_{2p5} signal. The time taken by this restart is several order of magnitudes longer than the original pulse injected on the pre-regulator input.

The characterization setup for each block is provided in Fig. 4.10. They require a characterization load to simulate the impact of neighbor blocks, initially modeled with a 1 MΩ resistor. A high-impedance avoids drawing too much current on the output, which

could affect or prevent normal operation. This value is not chosen in a strict manner and other values could have been chosen. The goal is to perform a preliminary test. The impact of this load on the characterization is evaluated later on in the analysis.

The regulator setup (characterization C) is more complex because the characterized input is not a supply but a 1.0 V reference. The regulator must also be powered, and a 9 V DC supply is added for this purpose. A 100 nF decoupling capacitor is also connected on the output because it is required by the regulation function. The regulator needs a low-power biasing signal called $V_{clamp2p5}$, that is normally generated by the bandgap in the real circuit. This connection is represented in orange in the Fig. 4.10. In the setup provided here, blocks are characterized independently in different testbenches, therefore the bandgap and regulator cannot be connected together. Therefore, the orange connection cannot be made between the two blocks. $V_{clamp2p5}$ is left floating on the bandgap output. For the regulator, the biasing signal is modeled with a 2.5 V DC supply in series with a 1 kΩ resistor. The impact of the removal of this connection on the failure signature is discussed later.

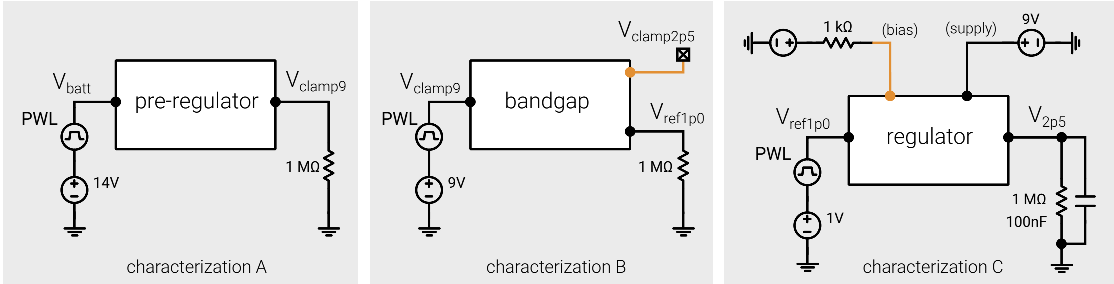

Figure 4.10: Block characterization setups

A set of simulations is run with those characterization setups. The only varying parameters are the input pulse amplitude and input width of each PWL source. Ranges for these parameters were given previously (Table 4.3). This type of parameterized simulations can be efficiently distributed on multiple machines. Characterization results are provided in Figs. 4.11, 4.12 and 4.13.

Model chaining

After the characterization phase, it is now possible to chain the models together. The goal is to evaluate the entire function's robustness. A rectangular pulse is injected on the global input (pre-regulator input). The chain of models is employed for predicting without running any simulation whether or not a failure will be found on the output pin. The input stress is generated by a TLP generator, producing a pulse of 1 µs duration with a −30 V amplitude.

Therefore, coordinates (1 µs, −30 V) are reported on the pre-regulator failure matrix (Fig. 4.11). This point indicates a failure on V_{clamp9} below 0 V (failure criteria) for a duration of 2300 ns. Coordinates (2300 ns, 0 V) are reported on the bandgap's failure

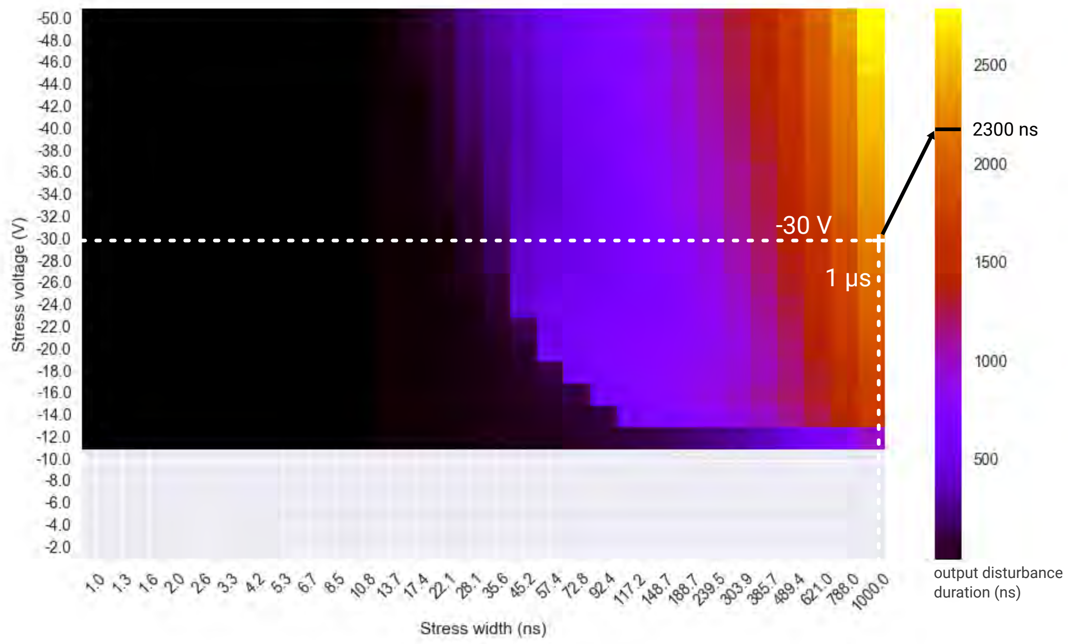

Figure 4.11: Pre-regulator V_{clamp9} failure matrix

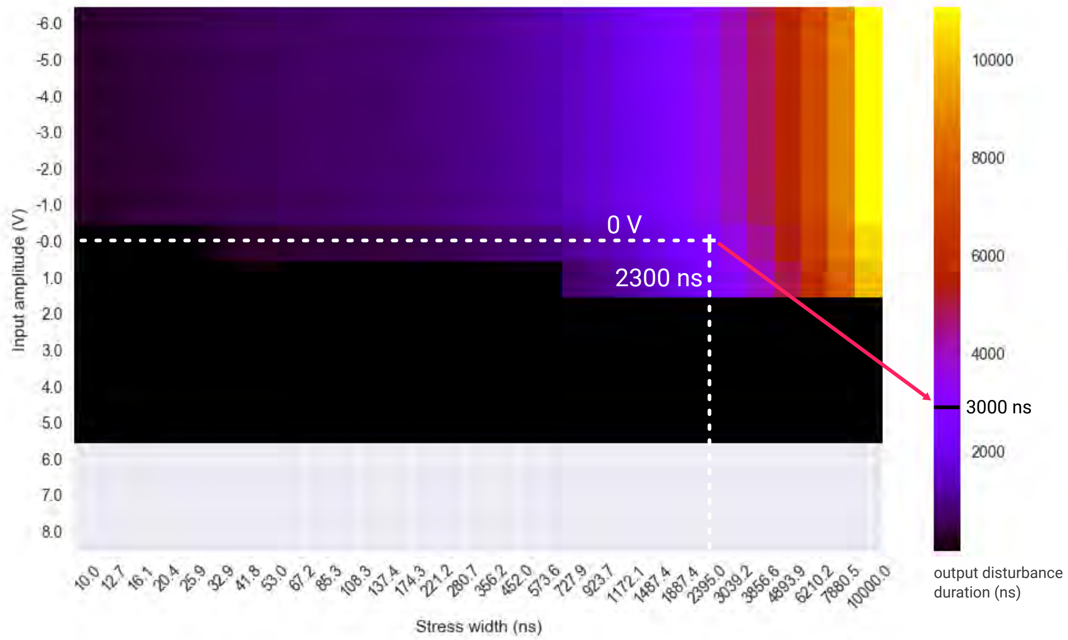

Figure 4.12: Bandgap V_{ref1p0} failure matrix

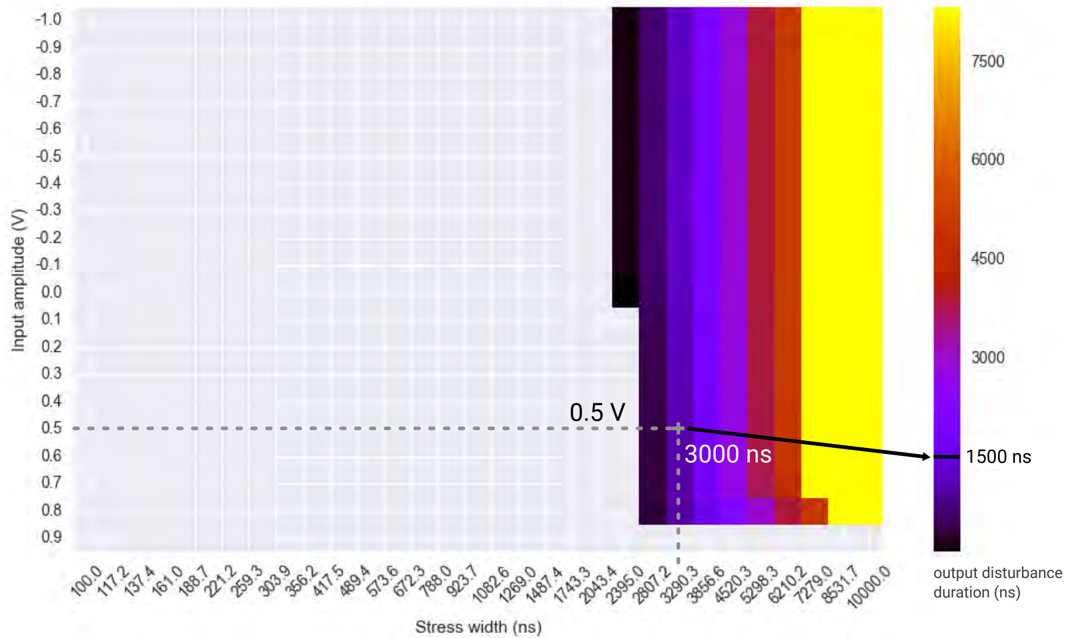

Figure 4.13: Regulator V_{2p5} failure matrix

matrix (Fig. 4.12). This point indicates a failure on V_{ref1p0} below 0.5 V for a duration of 3000 ns. Coordinates (3000 ns, 0.5 V) are reported on the regulator's failure matrix (Fig. 4.13). With those coordinates, the final signal V_{2p5} is estimated to fail (< 1.25 V) during 1500 ns.

The model chain estimates that the regulation function will fail during 1500 ns for a -30 V 100 ns stress on the input.

This result is tested against a simulation of the regulation function. The simulation setup is given Fig. 4.14. This simulation uses the full block schematic but the blocks are connected together only through the nets V_{clamp9} and V_{ref1p0}. For instance, the biasing signal in orange is still kept disconnected between the two blocks. This simulation serves as a reference for evaluating the model chain.

The complete simulation is ran with the same -30 V 1 µs input stress than the model chain. Signals V_{batt}, V_{clamp9}, V_{ref1p0} and V_{2p5} are compared with values obtained from the model chain. Simulation results are provided in Fig. 4.15. The model chain results are also plotted on the curve (red waveforms). Those waveforms are simply generated with the duration and amplitude predicted by the model chain.

Overall, the model chain predicts quite well the disturbance on the output of each block. V_{batt} has no waveform model because it is the external input signal.

V_{clamp9} is well modeled and both waveforms match quite well. It should be noted that the correlation on the amplitude between model and the real SPICE simulation is purely incidental. It is due to the fact that the failure criteria was arbitrarily set at 0 V, and that the block circuit design tends to clamp the output voltage near 0 V in case of

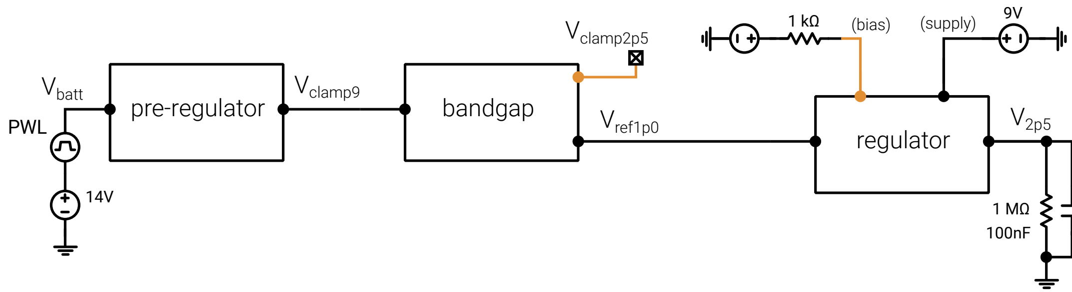

Figure 4.14: Reference simulation circuit

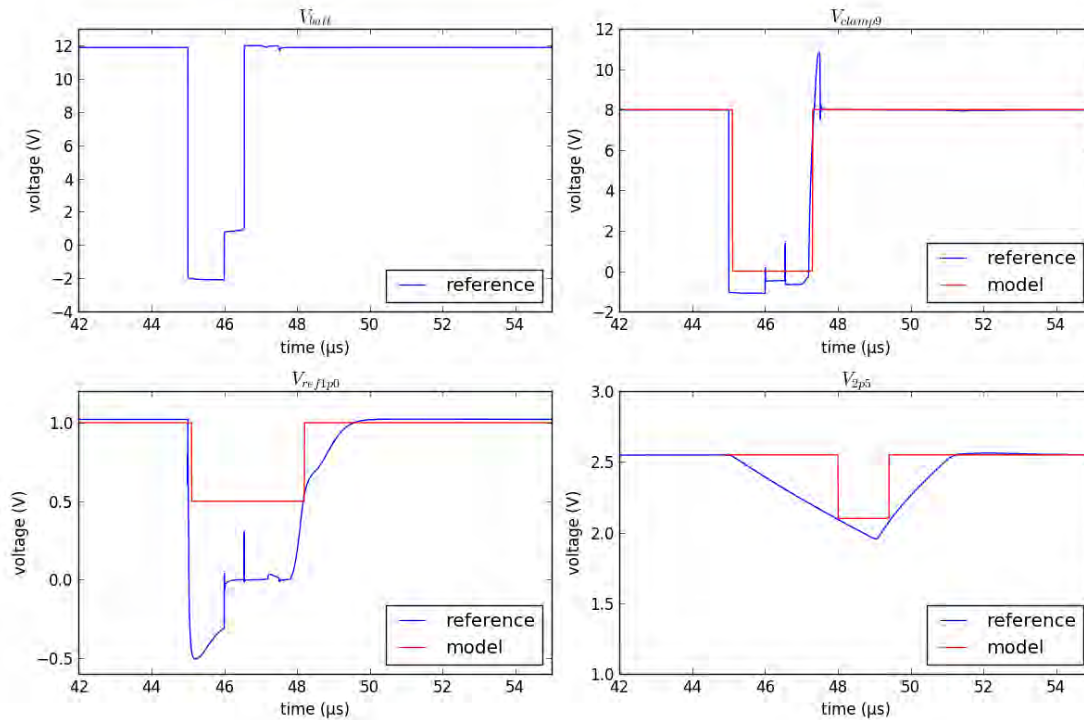

Figure 4.15: Reference simulation waveform - TLP stress −30 V 1 µs

a negative disturbance.

The width of V_{ref1p0} is also correctly modeled and matches the reference. On the other hand, the amplitude shows a large correlation difference. Here again, the design seems to clamp the output voltage near 0 V on negative transients. Since the failure criteria is set above that value at 0.5 V, both curves do not match.

Large differences are observed for V_{2p5} between model and reference. They are due to the triangular shape of the signal, that cannot be properly modeled with the rectangular shape. It is one of the first limitations of the model. Other limitations are discussed in the next section. Despite this, the disturbance was detected by the model which is

already a good achievement.

This first simulation proved that the model chain method definitely has some potential. It has also highlighted some limitations. The next section discusses further pitfalls of the model chain and an improvement is proposed and validated.

4.1.4 Limitations

Different sources of errors and potential improvements can be identified for improving the accuracy of the models. This section discusses those errors and how improvements can be implemented.

Impact of fixed failure threshold

The simulation presented earlier (Fig. 4.15) clearly showed that the fixed threshold is a major source of modeling error. The problem was particularly clear for the amplitude of signal V_{ref1p0}. Indeed, a fixed failure criteria leads to an oversimplification of the output waveform model, as illustrated by Fig. 4.16. The green waveforms show the case where the failure is not recorded, and the curve model is simply flat and constant (V_{OUT} model). The red waveforms show the case where a failure is well recorded, but the amplitude of the original signal goes way beyond the failure criteria. In this case, the curve model amplitude (V_{OUT} model) is not large enough and does not match V_{OUT}.

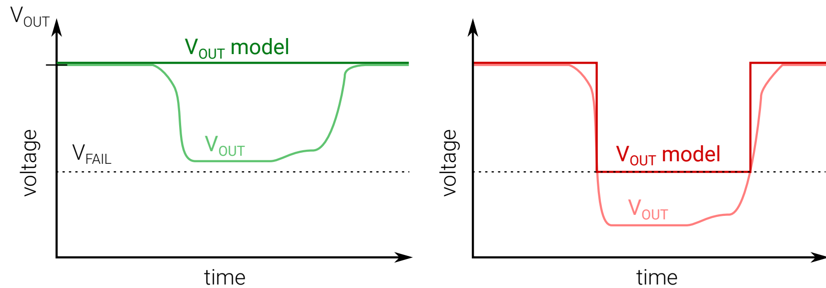

Figure 4.16: Lack of accuracy caused by the use of a single failure criteria to model the output

Originally, the fixed failure criteria was used for historical reasons. It came from characterization of hard-failure robustness performed with Wunsch and Bell method [104]. The methodology presented in this document started directly from this approach, and a first prototype was implemented using this same fixed failure criteria. In regard of the results presented earlier, the applicability of this fixed threshold for modeling soft-failure of analog block functions has been questioned. The analysis in this section demonstrated that **a fixed failure threshold is not suitable in the modeling of analog blocks**. This major observation is confirmed in the next section that discusses the impact of the fixed characterization load.

Impact of characterization output load

Previously, all characterization curves were extracted with a fixed output load of 1 MΩ. This value was selected because it is rather high-impedance and does not prevent proper circuit operation. It also draws a non-negligible amount of current and reproduces the circuit load of the complete schematic. It is possible that this fixed high-impedance load is a factor of error for the model chain.

In practice, each block sees a load impedance on its output much different than 1 MΩ. For instance, the output of the pre-regulator is used as a supply by other blocks. It can deliver a maximum current of 20 mA while maintaining 8 V, corresponding to a minimum output load this block can sustain is 400 Ω. The bandgap, on the other hand, provides a reference voltage at 1 V but can only deliver a small DC current in the range of 5 µA. More than 1 µA is enough to make the output fall of a hundred millivolts. In this case, the bandgap must see an output impedance of at least 1 MΩ.

To evaluate this impact, the pre-regulator is characterized again by with 4 different load values ranging from 500 Ω to 1 MΩ. Results are summarized in table 4.4. The three first column represent the input parameters, and the last column shows for how long the output was disturbed. The duration is measured using the failure criteria of the pre-regulator ($V_{clamp9} < 0$ V). It is the time during which the failure criteria was violated.

For the smallest 10 V stress amplitude, the failure time is largely impacted by the output load. The worst case is for the −10 V 1 µs pulse (Table 4.4). The output goes below 0 V for 1330 ns with 500 Ω on the output, but with 1 MΩ, no failure is observed. However, it is interesting to notice that for larger pulse amplitudes (below −30 V), the output load has a limited impact on the failure duration.

Those observations tend to indicate that once the output is at fault, having 500 Ω or 1 MΩ connected to it doesn't change the period during which it remains at fault. This is a major observation, because it shows that the output load value is not a key parameter during the characterization, and that the 1 MΩ value is sufficient for this study case.

Fig. 4.17 provides a visual representation of this observation, which is helpful for understanding this result. When the output is disturbed and its amplitude is near the failure criteria, the load value has a strong impact on the width of the failure. This is represented by the green curve in Fig. 4.17. A large load value such as 1 MΩ decreases the amplitude a little bit, causing the output to be above the failure criteria. With 1 MΩ, no failure is recorded. With a small load value (500 Ω) the output amplitude is increased a little bit (it becomes more negative). This time, it is below the failure criteria and a failure is recorded. This explains how the load has a large impact of the failure width for small stress amplitudes.

For large stress amplitude (red curve of Fig. 4.17), the amplitude variation caused by a 500 Ω load versus 1 MΩ is not sufficient to change the outcome. In both cases, a failure will be recorded.

In conclusion, the load value used during characterization does not seem to be the main source of error. Once again, it is proven that a fixed failure criteria is a major issue and limiting factor. It is responsible for the large variations observed in Table 4.4

load (Ω)	amplitude (V)	length (ns)	output disturbed (ns)
500	-10	10	10
5k			1
50k			None
1M			None
500		100	100
5k			1
50k			None
1M			None
500		1000	1330
5k			1289
50k			None
1M			None
500	-30	10	20
5k			10
50k			10
1M			10
500		100	506
5k			580
50k			594
1M			594
500		1000	2087
5k			2194
50k			2206
1M			2206
500	-45	10	46
5k			10
50k			10
1M			10
500		100	657
5k			715
50k			717
1M			727
500		1000	2668
5k			2764
50k			2800
1M			2800

Table 4.4: Impact of the output load on characterization results

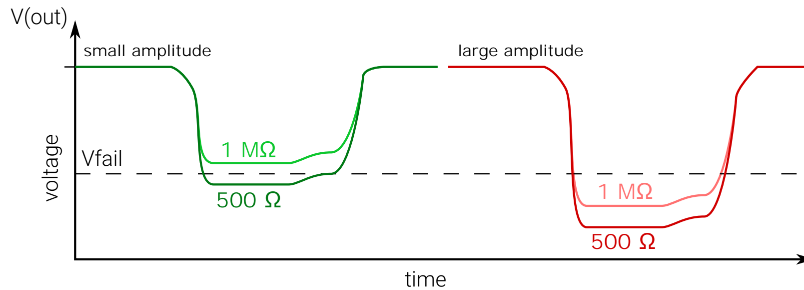

Figure 4.17: Represented impact of output load impedance on the output waveform during a disturbance with a small amplitude (green) and a large amplitude (red)

at small amplitudes. This result correlates with the observation made earlier in section 4.1.4.

Preliminary conclusion

Two different sources of errors were analyzed in this section. It was established that the fixed failure threshold is unsuitable for characterizing and modeling analog block functions. It should also be noted that defining this fixed threshold is an issue in itself, because very often a purely arbitrary value has to be chosen. In some rare cases, the specification could be used to set this criteria, but it remained mostly an arbitrary level. For digital cells, a fixed criteria is correct because above a certain input level disturbance an output can be switched and the failure is clear. However for the analog domain this rationale does not apply, because for most analog functions there is no clear failure. Most nets will have degraded values until extreme levels are reached where biasing might completely fail. Sometimes, the product is destroyed before reaching those extreme levels. In any case, the fixed threshold hides a lot of information about the degradation.

It was also suspected that the output load used during characterization might impact the results too much. In practice, it was proven in the case of the regulator that this is not exactly true. Changing the load can induce a variation, but seemingly more limited than the impact of the fixed failure criteria.

In the next section, a modification is brought to the characterization and modeling method. The fixed threshold is removed and replaced by a more flexible and powerful solution.

4.1.5 Proposed workaround

In the current approach, blocks are characterized using a fixed failure criteria on the output. It results in a characterization table, describing the duration of the output disturbance from the width and amplitude of the input stimulus. To remove and replace the failure criteria, the same exact approach is proposed. Since the output duration is

calculated with a table, then the output amplitude could be calculated using another table as well.

The new model contains two 2D tables instead of one, and the new table associates an output amplitude to an input width and amplitude. Fig. 4.18 summarizes the new model. **Table A** is the amplitude table, to calculate the **amplitude** of the output disturbance. **Table W** is the width table, to calculate the **duration** of the output disturbance.

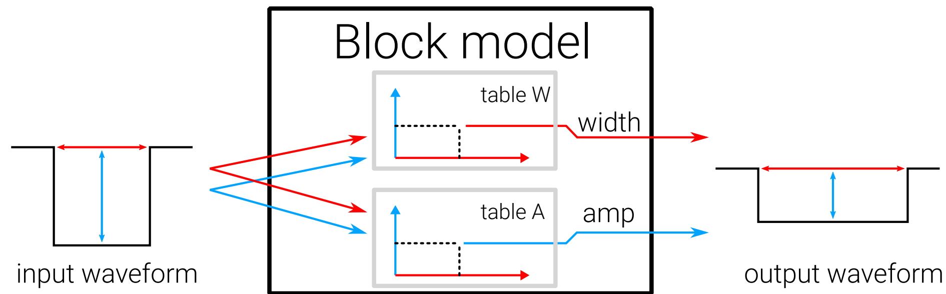

Figure 4.18: Improved modeling method

To extract both tables, the process is a bit different from the first methodology. For each characterization simulation, the maximum output amplitude is recorded. It is stored in table A. The duration is measured on the output at 90 % of this maximum amplitude. The validity of this threshold is discussed after in 4.1.6.

The rest of the methodology remains identical. In particular, model chaining is performed the same way since block models still accept an input width/disturbance and return an output width/disturbance.

Application of the improved method

The new characterization method is applied to all three blocks of the regulation function. The amplitude table of the pre-regulator is plotted in Fig. 4.19 and the width table in Fig. 4.20. Different patterns can be observed between both figures. The output amplitude gradient seems independent from the input width because it displays only horizontal lines, and depends only on the input amplitude. The output duration gradient is a lot more complex with multiple different patterns. Overall, large input amplitude and duration tend to result in long output disturbances. The other characterization tables of the bandgap and pre-regulator are provided in Annex B.1.

The chaining process is performed again with a −30 V 1 µs rectangular input stimulus. The reference curve and reference test setups remain identical to the ones presented earlier (Fig. 4.14).

The chaining process predicts that V_{clamp9} will be down at −1.6 V during 1800 ns. The −1.6 V value is obtained by taking coordinates of the input stimulus (−30 V, 1 µs) and applying them to Fig. 4.19. −1.6 V then corresponds to the gradient value at those

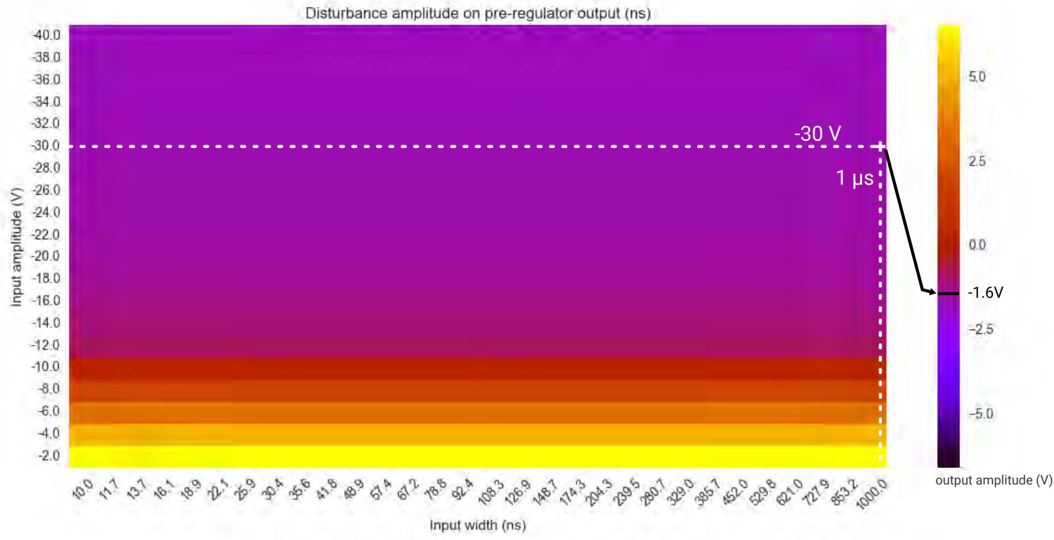

Figure 4.19: Pre-regulator V_{clamp9} amplitude matrix

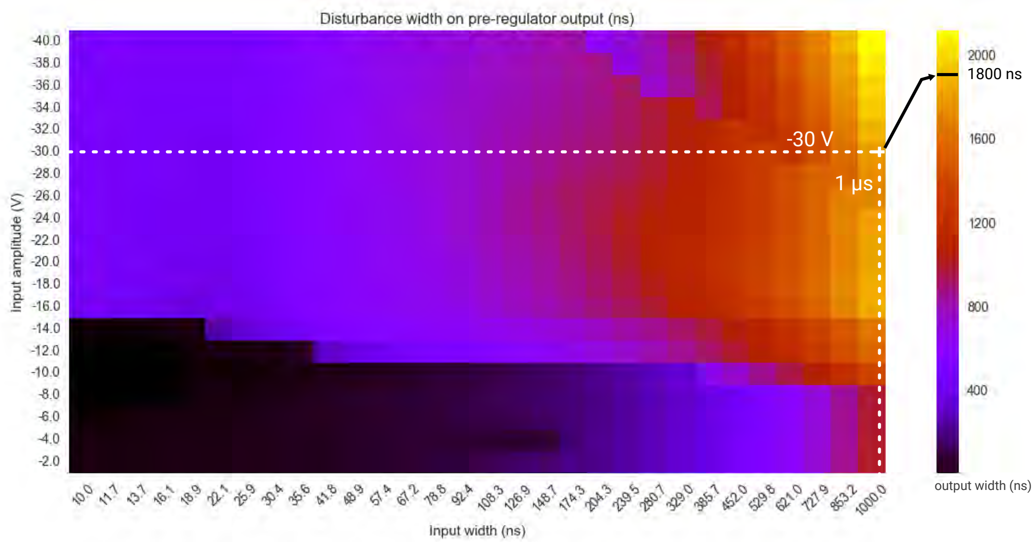

Figure 4.20: Pre-regulator V_{clamp9} width matrix

coordinates. The 1800 ns is obtained with the same input coordinates but applied to Fig. 4.20 instead. The same process is then used for the bandgap and the regulator. V_{ref1p0} is predicted at −1.25 V during 3300 ns. V_{2p5} is predicted at 2.0 V during 2700 ns. Those values are employed for generating model waveforms, and are compared to the reference simulation in Fig. 4.21.

The model matches correctly the simulation of V_{clamp9}, both in terms of amplitude and width. The width is slightly underestimated but overall the result is acceptable.

For V_{ref1p0}, the width is extremely well reproduced, but the amplitude is about twice the reference value. It seems that taking the minimum amplitude value during the characterization is not ideal. This error should be investigated further to determine the actual root cause and provide a solution. The last signal V_{2p5} shows a quite good correlation despite the fact that it is a triangle-like waveform. More validations were performed with (−20 V, 1 µs) and (−20 V, 100 ns) stimuli. The results are provided in appendix B.2. Overall, the modifications brought to the modeling method seemed to have a positive impact on the curve models. A lot of room is left for improvements, in particular for reproducing the bandgap output signal V_{ref1p0} that systematically suffers from amplitude modeling error.

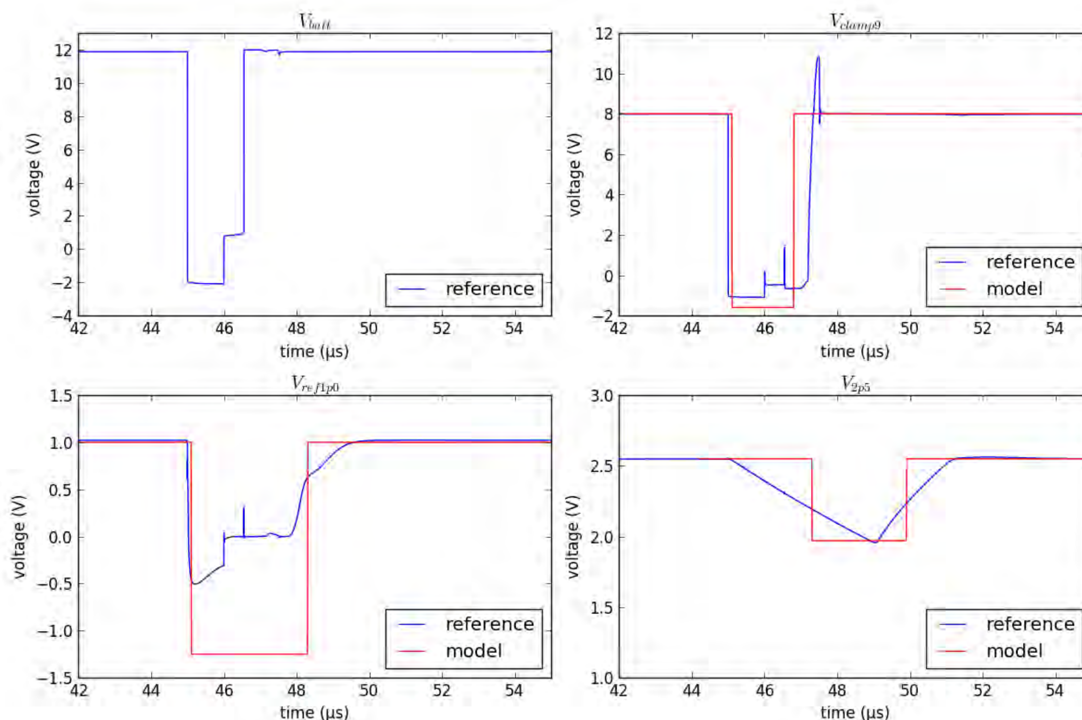

Figure 4.21: Reference simulation waveform : TLP stress −30 V 1 µs

This section presented a potential improvement over the model chain method initially proposed. This technique showed good results and seems promising for quickly estimating the robustness of a high-level integrated function. The next section discusses further improvements for extracting width and amplitude during characterization.

Potential improvements regarding parameters extraction

In the simulations described earlier, a single width and maximum amplitude per waveform were extracted manually. However, waveforms are never perfectly squared, and an width and amplitude cannot always be extracted easily. The challenge is to find the right

rule for simplifying them into a rectangular waveform, and extracting the two parameters. This applies to the input and the output waveforms during the characterization of a block.

Initially, the rules were to set V equal to the maximum value of the waveform (input or output), and W the width of the pulse at 90 % of V. This waveform simplification into a rectangular shape can be difficult to perform with some non-trivial curves. Two cases where this simplification is not straightforward are illustrated in Fig. 4.22.

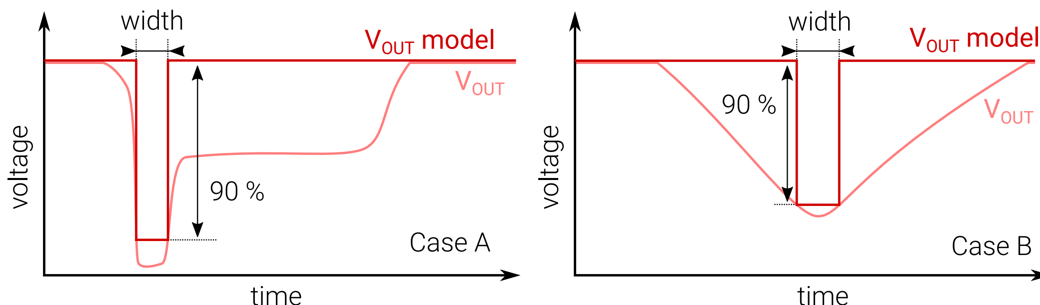

Figure 4.22: Improved output modeling method based on 90 % of maximum disturbance amplitude

Case A is often observed during the injection of an electrostatic discharge. The ESD signal is superimposed on top of a slow signal variation. In that case, the waveform exhibits a very short, high amplitude peak, followed by slower smaller-amplitude variation. The width of the pulse is much shorter than the original curve, leading the model to be very inaccurate.

Case B is observed on nets with high capacitive coupling to ground. Those signals are not directly disturbed by the ESD, but the block that drives them can go into reset. In this situation, the net slowly decreases then goes back to its nominal value once functionality resumes. With the 90 % threshold, a large area of the disturbed waveform is missing in the model, making it very inaccurate.

In both cases, the 90 % threshold leads to underestimating the total disturbance width. The modeled waveform has a much smaller duration and area than the original one. Overall, it was observed that the model and original waveform areas should be close for the models to work.

Instead of focusing on the peak amplitude, a smarter method is required. Ideally, it needs to extract a width and amplitude that would result in the same area than the original waveform, while looking as similar as possible.

A feature detection method using amplitude distribution could be performed to identify key amplitudes in the waveforms. Other techniques could be conceived, such as combining multiple rectangular waveforms to describe more complex waveforms. Basically, it would consist in breaking down a complex waveform into 2 or more rectangles, and applying each rectangle to the model chain. This waveform breakdown concept is illustrated in Fig. 4.23.

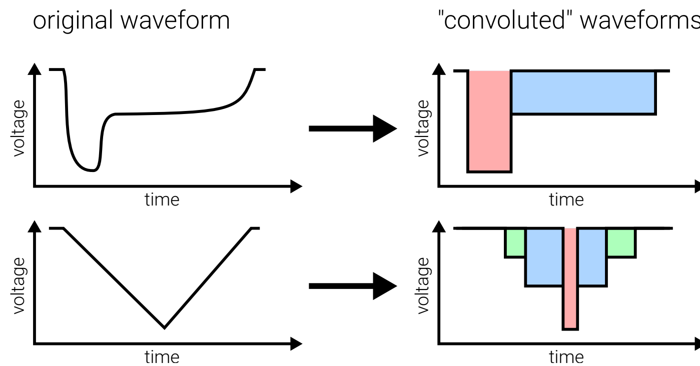

Figure 4.23: Waveform breakdown into rectangular shapes

4.1.6 Final conclusion and follow-up work

In this section, principles were detailed for a block modeling method, targeting powered integrated functions exposed to disturbances. It initially started off from the Wunsch and Bell method [104], which is based on a pass/fail failure criteria and targets hard-failure of electronic devices. The method was improved to fit better the modeling of analog functions, symbolized by an input, and output and a transfer function. The failure criteria was then removed because it was a large source of error. The final model is constituted of two characterization tables. The first one describes the **output amplitude** as a function of the input amplitude and duration. The second one describes the **output duration** as a function of the input amplitude and duration. For this purpose, waveforms observed on the inputs and outputs were simplified as rectangular shapes. Each table stores the transient response of the characterized block against a wide range of input disturbance configurations. On a single study-case, it was shown that this method is able to reproduce simplified waveforms of a disturbance propagating through a chain of block functions.

Some limitations must be overcome before this method can be applied to a larger scale. So far, only very linear circuit topologies were considered. A single input net and output net was studied per block. It is one-to-one relation. In reality, the relations are closer to many-to-one or many-to-many. A single input will impact multiple outputs when disturbed. Inputs do not have isolated impact, multiple inputs will affect the same group of outputs when they get stressed.

Also, more study cases are required to verify further the hypothesis under which ESD simulations at silicon-level can be performed using exclusively rectangular pulses, to disturb blocks in isolated testbenches.

4.2 Black box modeling approach

The goal of the black-box modeling method is to build a combined electrical and failure model of an integrated function between an input pin and an output pin. This model is developed to allow third-parties that don't have access to the integrated circuit design to perform ESD simulations of a board containing integrated circuits. Basically, this black box model is intended to act as a replacement for the IC function during ESD board-level simulations. This combined system-level and integrated circuit simulation approach is very valuable for designing robust applications, and is almost identical to the SEED [103] methodology introduced in previous chapters. The SEED methodology normally applies to hard-failure, but in this chapter the concept is pushed further with soft-failures. SEED recommends that the ESD robustness of a system should be handled by a collaboration between the board and the integrated circuit. To achieve this, it is necessary to have simulation tools capable of simulating both elements at the same time. The black-box model presented in this chapter is a potential solution to this issue. It does not reveal the internal IC design while allowing complete simulations of board and integrated circuits together to predict soft-failures. It also hides the internal complexity of the integrated circuit design, allowing significantly faster simulations and less convergence issues.

The proposed model is composed of two port models and a failure model as shown in Fig. 4.24. The electrical parts enable SPICE simulations with this model inside an electrical environment. The port model reproduces the behavior of the integrated circuit between an external pin and usually a ground pin. The failure part of the model watches the external input pin and detects conditions that would lead to a failure visible on the external output pin. If a fail was detected, the information is transferred to the output port model that will reproduce the behavior of the output during a failure.

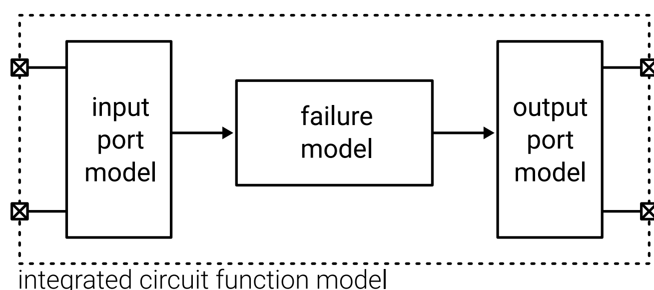

Figure 4.24: Black-box model principle

The failure model is obtained with a preliminary characterization method. It is also inspired by the Wunsch-Bell methodology [104]. The failure model is extracted first, using a set of rectangular pulses of variable amplitudes and variable widths applied on the input pin while monitoring the output pin. After this step, the robustness of the function against this range of stresses is known. A curve is built that describes the failure of the output when an input is stressed. The second step is to electrically model both the

input and the output ports. Initially, a TLP characterization of each port is performed to extract an equivalent I(V) curve. Since the circuit is stressed while being powered and in operation, it is studied afterward if this extraction should occur on a device powered as well or not, and what is the impact of the supply on the extracted curve. This characterization is based on the hypothesis that the quasi-static I(V) curve could be suitable for reproducing the behavior of the port both in DC and transient domain. It will be demonstrated afterward that this hypothesis is not completely true and an alternative approach is required for the output pin. This I(V) curve is converted in an electrical model using a piecewise-linear curve described in Verilog-A modeling language. Finally, once the two electrical models and the failure model have been constructed, it can be possible to join all the parts together to build the complete IC model.

To validate the concept, the characterization is performed on the integrated primary supply studied earlier (see Chapter 3.1.1). The input pin is called V_{batt} and accepts the battery supply voltage. The output pin is called V_{2p5} and is supposed to deliver a 2.5 V regulated supply. Fig. 4.25 summarizes the model configuration with those pins and function.

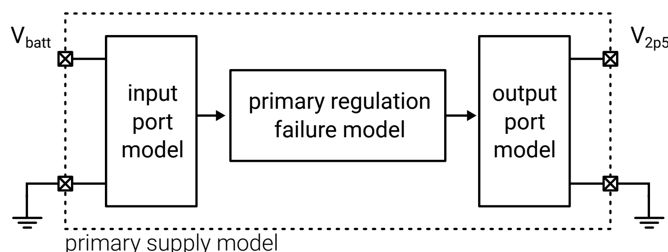

Figure 4.25: Black-box model applied to the primary regulation function

4.2.1 Function failure model

The primary regulation function is characterized by applying a set of rectangular pulses of variable widths and variable amplitudes on the input pin, while monitoring the behavior of the output pin. In case of significant variations of behavior, a failure is recorded. The characterization yields a lookup table (see Table 4.5) that associates to an input width and an input amplitude a flag representing the presence or absence of a failure.

The characterization pulses are injected on the V_{batt} input. If a voltage below 2.1 V is detected on V_{2p5}, a failure is recorded. This voltage threshold is the failure criteria. This value was chosen because it corresponds to a level below which digital cells powered by this supply will have noise margins too small for proper operation. The input stress amplitude range is -50 V to -500 V. The input stress width is comprised between 1 ns and 1000 ns. The characterization setup is given in Fig. 4.26. On the input pin, a 12 V bias supply is connected in series with the rectangular pulse generator. On the output, a 100 nF capacitor is connected because required by the voltage regulation function for stabilization.

input width (ns)	input amplitude (V)	Failure
10	1	No
10	2	No
etc.	...	...
100	1	No
etc.	...	...
1000	10	Yes
etc.	...	...

Table 4.5: Example of resulting table of failure characterization

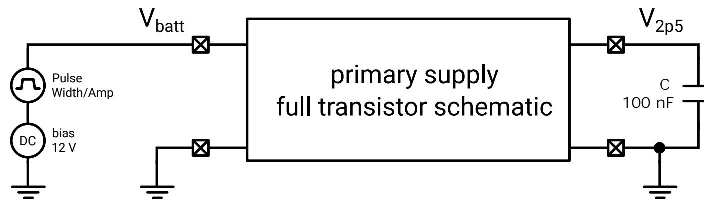

Figure 4.26: Black-box characterization setup

The result of the characterization is plotted in Fig. 4.27. The x-axis is the pulse width, the y-axis is pulse amplitude and a colored cell represents a failure on the output. This plot is simply a different representation of the lookup table discussed previously. The plot shows that a combination of long stresses and large amplitude are the most disturbing for the function. Amplitude or width alone are not necessarily sufficient to put the function at fault.

Now that the characterization step is done, the next part of this work focuses on electrical modeling of input and output pins.

4.2.2 Electrical pin models

I(V) curve extraction in powered and unpowered modes

The initial hypothesis in this section is that TLP characterization can be used to represent an input or output port of an integrated function. Extracting the TLP characteristic can be done with the device powered or unpowered. To see the impact of the biasing and to decide the best approach, TLP characterizations are performed in both conditions. The test setup for the input port is given in Fig. 4.28. The DC source can be configured at 0 V (unpowered conditions) or 12 V (powered conditions). The TLP is a perfect rectangular source in combination with a series 50 Ω resistor.

The test setup for the output port is given in Fig. 4.29. The main issue with this characterization is that it includes the external stabilization capacitor. It will be verified after if this external device is an issue for modeling. The results are provided for the

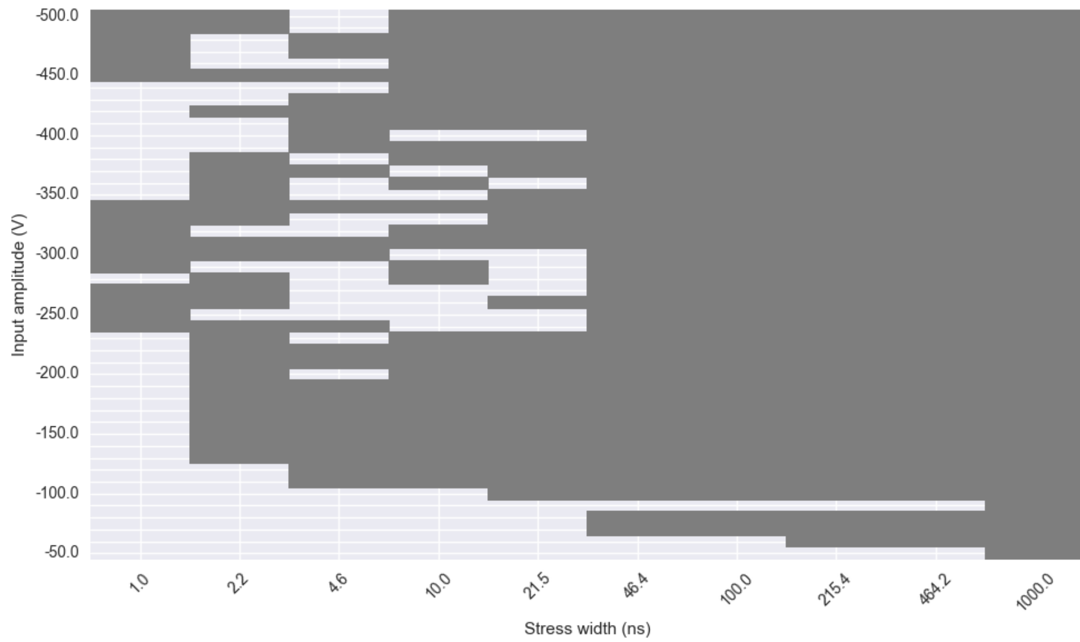

Figure 4.27: Black-box characterization of the regulation function (area in gray corresponds to a failure on V_{2p5})

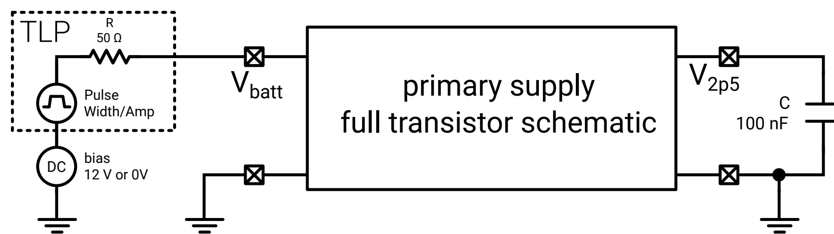

Figure 4.28: I(V) extraction of input port

input and output ports in Fig. 4.30 and 4.31.

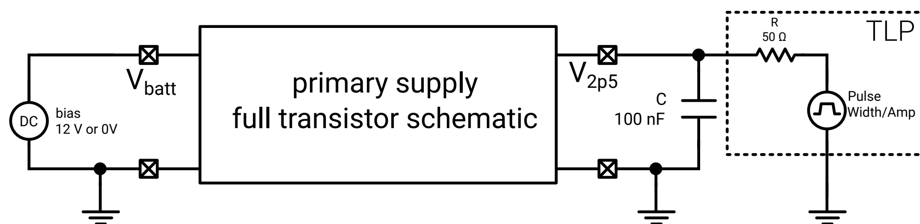

Figure 4.29: I(V) extraction of output port

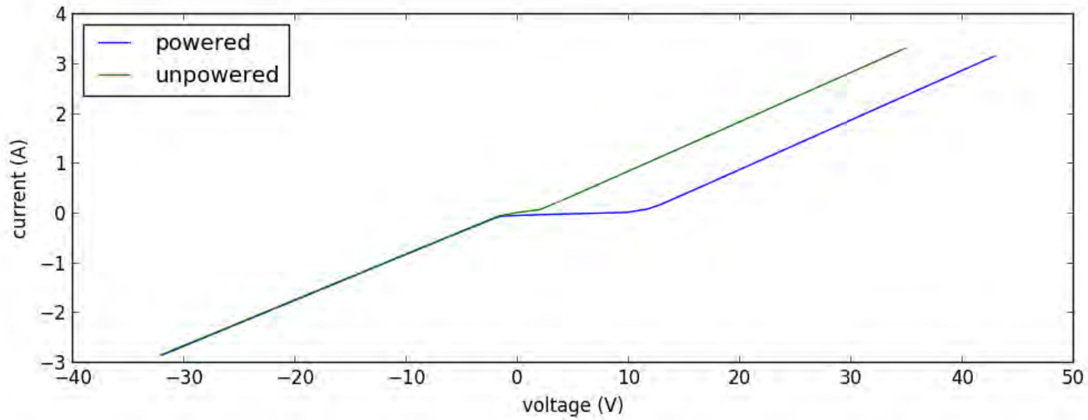

Figure 4.30: TLP characterization of function input in powered and unpowered conditions

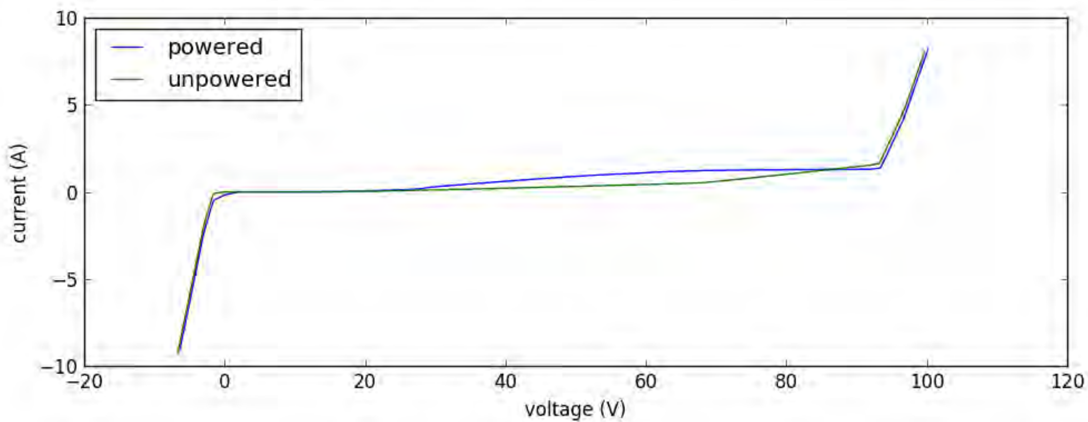

Figure 4.31: TLP characterization of function output in powered and unpowered conditions

For both ports, large differences are observed between powered and unpowered modes. Different amount of currents are absorbed by the device in each conditions. Ultimately, the powered configuration is chosen for the characterization because it is the one used for soft-failure testing (with the device in operation).

I(V) curve modeling

The second step of the modeling method is to build an electrical model of the function from those curves. A piecewise linear model seems well suited for this situation. A four-points piecewise linear model is written in Verilog-A (see Listing 4.1). The model is configured easily with 4 four (V_i,I_i) coordinates.

```
//Verilog-AMS HDL for "pwl_4pts" "verilogams"

`include "constants.vams"
`include "disciplines.vams"

module iv_curve (A, B);
  inout A, B;
  electrical A, B;

  parameter real v0 = -50.0;
  parameter real i0 = -10.0;
  parameter real v1 = -4.0;
  parameter real i1 = -2.0;
  parameter real v2 = 13;
  parameter real i2 = 12;
  parameter real v3 = 50;
  parameter real i3 = 18;
  real a1, a2, a3, b1, b2, b3;
  real curr;

  analog begin
    a1 = (i1-i0)/(v1-v0);
    a2 = (i2-i1)/(v2-v1);
    a3 = (i3-i2)/(v3-v2);

    b1 = i1 - a1 * v1;
    b2 = i2 - a2 * v2;
    b3 = i3 - a3 * v3;

    if(V(A,B) > v2)
      curr = a3 * V(A,B) + b3;
    else if(V(A,B) > v1)
      curr = a2 * V(A,B) + b2;
    else
      curr = a1 * V(A,B) + b1;

    I(A,B) <+ transition(curr,0,1n,1n);
  end
endmodule
```

Listing 4.1: Piecewise linear 4-points Verilog-A model

With this kind of model, convergence can be difficult to achieve if the piecewise-linear curve is not continuous at order 0. Electrically speaking, it is equivalent to switching the value of a resistor very abruptly. To ensure that this does not happen, it is important to use **exactly** the same coordinates at inflexion points, where the model switches between operating curves. This is taken into account in the current model.

During this TLP characterization, I(V) curves were extracted for a wide range of voltages. However, not the entire I(V) curve is relevant for those soft-failure simulations. Any part of the I(V) curve beyond the safe operating area is irrelevant because after that the function is destroyed. Therefore, it is important to fit the I(V) curve with the piecewise linear curve inside the SOA. For the input, the modeling is focused on a voltage range from −10 V to 40 V. On the output, the modeling range is from −5 V to 5 V. Those values are obtained from the function specification and correspond to the sustained input ranges.

Comparison of input model with reference circuit

The Verilog-A model is tested against the complete schematic for the function's input. The test setup is given in Fig. 4.32. Biasing and injection circuits are identical for both circuits. The full schematic is simply replaced by the Verilog-A input model.

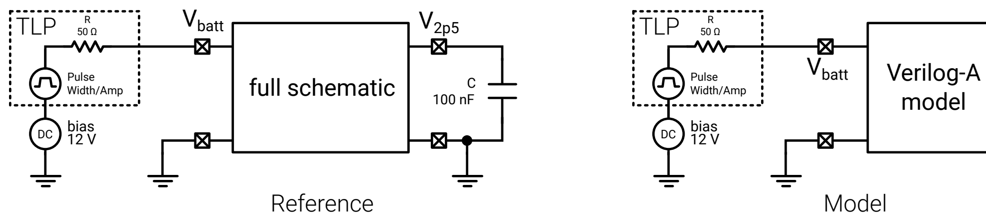

Figure 4.32: Testbench for comparing complete schematic with input model simulations

A first comparison is ran by injecting a −10 V TLP with the device powered. The voltage and current waveforms are provided in Fig. 4.33. Voltage matches well between the reference and the Verilog-A model. The DC behavior as well as the transient behavior are correctly reproduced. The current waveform has a poorer correlation. There is an offset in DC and in transient, probably due to a modeling error with the piecewise linear curve. There are two large spikes at the beginning and the end of the pulse that are not reproduced. This behavior was expected because the piecewise-linear model is not able to reproduce this kind of dynamic behavior. Overall, the accuracy remains acceptable for an ESD simulation. Other validations are provided in Appendix C.1 (see Fig. C.1 and Fig. C.2) for positive 20 V and 40 V TLP. They confirm that the input model performs correctly, and even better when exposed to positive stresses. Overall, this Verilog-A model is considered valid for the input port while considering that there is a lot of room for improvement.

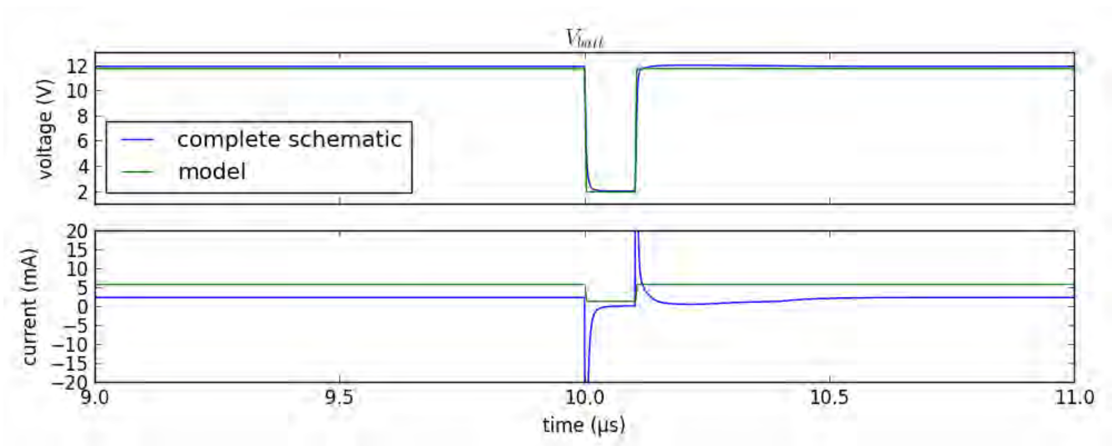

Figure 4.33: Comparison of complete schematic and model simulations for input port (−10 V TLP)

Comparison of output model with reference circuit

The output port is more complicated than the input port, because it is equivalent to an active device, unlike the input that can be assimilated to a passive port. The primary supply regulates a 2.5 V voltage on this output and drives a current into the external load to maintain that voltage. The Verilog-A I(V) model used for the input is just a voltage controlled current source and is not capable of regulating a voltage. A more complex architecture is proposed with Fig. 4.34. A DC voltage source is added to generate the regulated 2.5 V. In case of failure, the output port will also fail temporarily and the output voltage will fall down. A transient voltage source is added to the model to simulate the output fault.

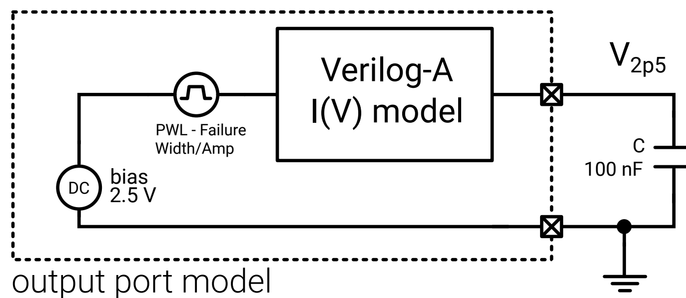

Figure 4.34: Architecture of the output port model

This new output port model is compared to the complete schematic in simulation. With the complete schematic, a failure is triggered by applying a negative −10 V TLP on the input port V_{batt} while watching the output V_{2p5}. For the model, the PWL source is used to fake a failure. The testbench is identical to the input validation testbench

shown previously (Fig. 4.32). Voltage and current waveforms are compared in Fig. 4.35.

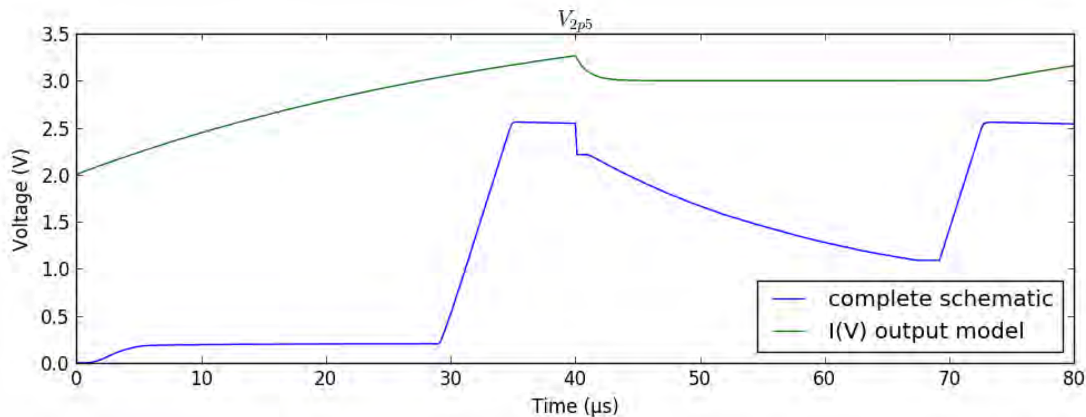

Figure 4.35: Comparison of complete schematic and model simulations for output port (−10 V TLP)

Large differences are observed between reference and model simulations. In the reference curve (in blue), the regulation function starts up between 0 µs and 35 µs. This part of the curve is not particularly relevant for the ESD analysis and can be ignored overall. At 40 µs the pulse is injected on the input (not plotted), resulting in a fault on this output. In turn, the reference curve exhibits the typical restart explained previously in chapter 3.1.2. The voltage drops until 1 V. The regulator restarts until it is operating properly again at 75 µs.

The model curve (in green) is very different from the reference. Initially, the 100 nF capacitor connected on the output (Fig. 4.34) is pre-charged at 2 V. This value is voluntarily set at a lower value than the nominal 2.5 V to ensure that the model alone is capable of reaching this DC operating point. Instead of reaching and stabilizing at 2.5 V, the output voltage keeps increasing. This can be explained by looking at the I(V) curve of the output magnified between 1 V and 4 V (see Fig. 4.36). At the beginning of the simulation, the I(V) model sees a potential difference of 2.0 V across its terminals. For a 2.0 V voltage, the I(V) curve model produces a value of 0.75 mA. It is not identical to the characterized value of 0.2 mA but the error remains acceptable. This non-zero current is therefore forced by the Verilog-A model into the capacitor, that keeps charging. In itself, the combination of the DC source and the I(V) curve does not seem suitable for modeling an active output.

Configuring the Verilog-A model to generate a zero current at 2.5 V will not solve the problem either because with a resistive load the output will need to supply a DC current at 2.5 V. The I(V) curve extracted with a TLP characterization in simulation does not seem to be usable as-is to model an active output. A more complex or different solution must be conceived and developed to solve those issues. One potential solution would be to create a custom Verilog-A model capable of regulating a voltage while offering proper output impedance. Overall, this study on input and output ports

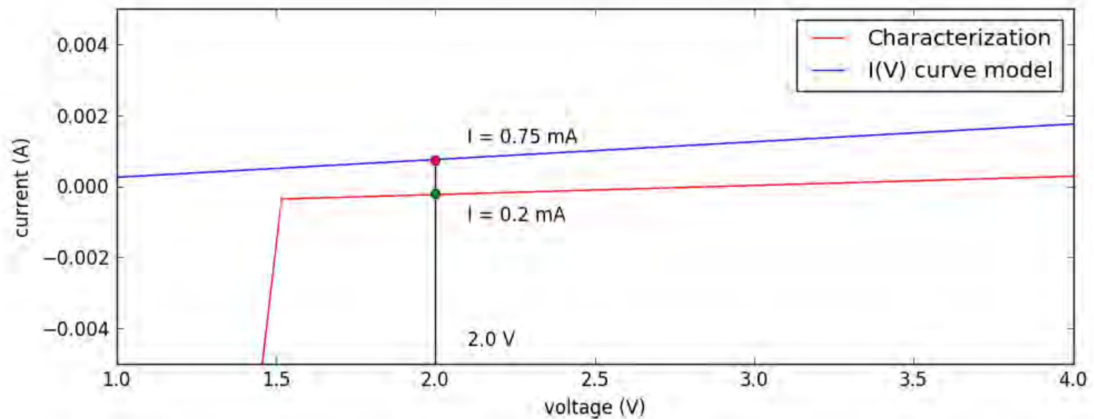

Figure 4.36: TLP characterization of function output near 2.5 V (magnified)

modeling has enabled to identify key issues preventing for now to develop a complete model of integrated function for powered ESD simulations. This is a first step toward more advanced models and modeling techniques that ultimately should enable better cooperation between silicon-design companies and equipment manufacturers, as described by the SEED methodology.

4.2.3 Conclusion on black-box modeling

Black box models are very promising for distributing SPICE models of integrated functions to third-parties without disclosing intellectual property. They do not disclose the internal design of the chip and might help achieve system-level ESD simulations with IC models. Ultimately, the goal is to follow the SEED [103] methodology that indicates that ESD robustness of a system should not be handled by a single component but with a collaboration between all parts (equipment, board, integrated circuit), using appropriate design techniques to ensure that the cooperation is efficient. In this section, a first attempt at extracting and creating black-box models for integrated functions was presented, in the context of ESD simulations. TLP characterization was performed on input and output pin of a biased function, to extract an equivalent impedance. The resulting I(V) curve was then modeled using Verilog-A modeling language, then used in circuit simulations. For the input pin that is somehow equivalent to a passive device, this model has shown promising results with excellent correlation in both DC and transient domains. The Verilog-A model performed particularly well for the input when exposed to a positive rectangular stress. The correlation was less accurate with a negative rectangular pulse but remained acceptable for an ESD simulation. For the output pin, the situation was more complex because it should be modeled by an equivalent active device. A first model was proposed specifically for modeling active outputs. Differences between the reference schematic and the model were large, showing that a different or more complex approach is required. Despite the lack of correlation, this study has enabled to

identify an important issue preventing to build a model of an integrated function, for ESD simulations. Solving this issue should be the topic of future work and research, and identifying it was already a significant milestone to reach for achieving this goal. Ultimately, black box models should enable to replace an integrated function during an ESD simulation, in order to reduce complexity, simulation time, and protect intellectual property.

Conclusion

Electrostatic discharges are a major source of stress for electronic devices. They can cause hardware failures, damaging permanently devices. This class of issues has been studied for ten years, and is still the core of ESD research. Recently, a new class of failures started to be considered. Electrostatic discharges can cause temporary disturbances on devices. Most recent integrated technologies enable large performances and massive integration, but also makes more challenging the protection of integrated circuits against external disturbances. In the same time, electronic modules have increasingly large responsibilities in regard of our safety. New trends for the autonomous car require electronic devices to take vital decisions for controlling the vehicle. Guarantying safety of operation against electrostatic discharge is critical.

This document detailed three years of research about functional robustness of integrated circuits against electrical transient disturbances. This field of research is relatively recent, and brings new challenges for ESD teams in integrated circuit design companies. During those three years, it became clearer that solving efficiently soft-failure issues requires dedicated tools. Those tools should enable broader interactions between circuit design team and ESD team. They should help detecting and localizing functional weaknesses inside the integrated circuit. They should also enable better collaboration between integrated circuit companies and equipment manufacturers to design robust boards and applications. Many tools were studied and proposed throughout this research work. All the different topics are synthesized in Fig. 4.37 that was also presented in the introduction.

Chapter 1 is a review of the state of the art in ESD testing and soft-failure analysis. It starts by describing common and recurrent test methods in the ESD field, and identifies relevant and realistic stress sources employed in laboratory environment. A review of the literature on soft-failure analysis and prediction method is conducted afterward. It showed that to this day there are rather few research on the topic of ESD-induced soft-failures at silicon level. Many general-purpose observation techniques exist such as EMMI and near-field scan. Among the simulation tools, it is common to find SPICE simulation of course, and more advanced techniques such as 3D full-wave electromagnetic simulations or TCAD simulations. These tools are highly interesting at the system and board level, to evaluate what fraction of an incoming discharge actually reach an integrated circuit. It is important to notice that no solution exists so far to investigate at chip level how functions are disturbed by electrostatic discharges. This point is a key

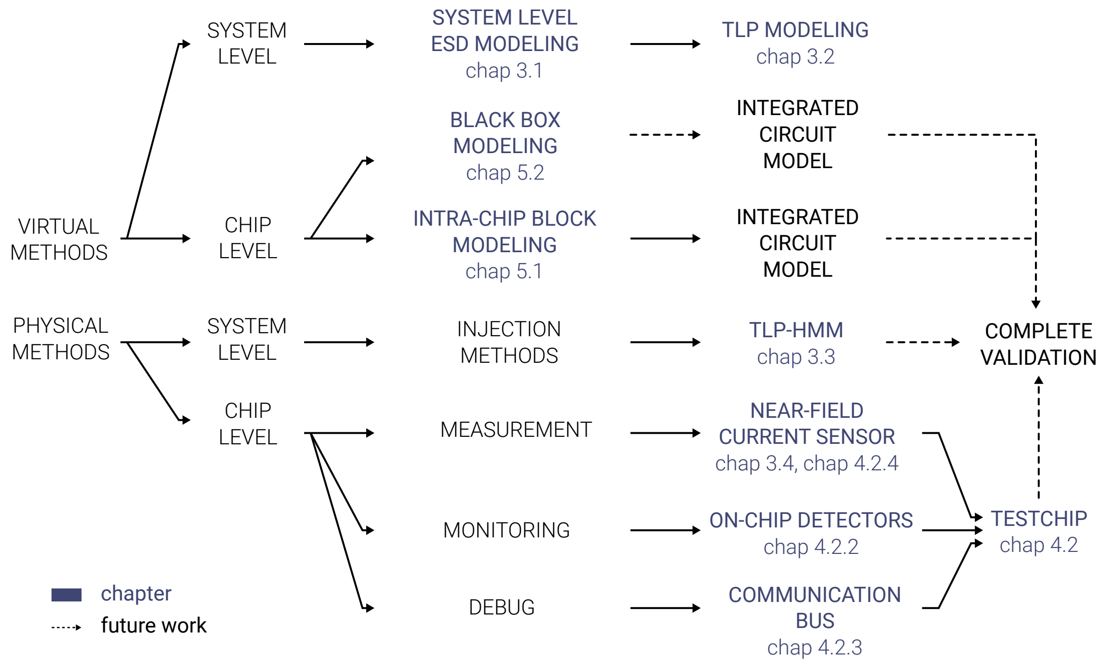

Figure 4.37: Explored research paths for soft-failure investigation and prediction

part of the research presented in this document.

In chapter 2, a modeling method of electronic systems for ESD is detailed. It relies and brings a few improvement over existing research conducted in the past on this topic. A modular approach is employed, where each component is modeled individually to form a library, then assembled together in a hierarchical fashion. Mostly physically based and most parameters can be extracted with simple tools, or by estimation where it is sometimes enough. A concrete case study is presented with the modeling of a complex TLP generator. It is perfect to illustrate a few key points for the modeling methods, and to demonstrate its accuracy against a lot of reference measurements.

The development of this model and the insights gained in the process led to the development of a new pulse generator. It reproduces the HMM waveform, one of the most widely used test pulse in the ESD field, but in a shielded and controlled environment. The benefits are increased reproducibility of testing results and a flexibility for shaping the pulse waveform. The prototype helped identified early issues and improvement to make.

When comparing this generator to actual ESD guns and standard TLP, a new correlation method has been discovered. It was validated successfully on 10 different ESD protections. Correlation methods between ESD generators are extremely valuable because they can ultimately reduce testing time. By testing a part with a single generator it is possible to predict the failure levels found with the others. Before being able to do so, the correlation method should be tested on a much larger set of ESD protection. Failure analysis on the destroyed parts should be conducted to verify if the failure

mechanism remains identical between the different generator.

In the last part of chapter 2, a detailed post-processing method for on-chip near-field sensor has been presented. It details the operation of the post-processing pipeline developed for this kind of sensor. The processing script is released [96] under an open-source license to promote collaboration and future improvements on the topic. Two different methods are evaluated and compared in order to reconstitute a current waveform from the voltage measured across the on-chip sensor.

Chapter 3 presents a real case study where a complex analog function goes into restart because of an ESD. The function is a primary regulator supply from a large automotive product. It is put in a lowered BOM configuration where the external filtering is reduced to diminish the total application cost. The ESD robustness of this configuration is studied, and a new failure is observed and explained. After this analysis, it was decided to build a custom chip integrating this particular function, alongside with custom monitoring structures. There were multiple objectives for making this test vehicle. The first goal was to acquire waveforms inside the chip, using on-chip measurement structures and sensors, to validate that standard circuit simulations can be employed during an ESD event. The second goal was to determine when and how analog function were disturbed by transient events, by using custom error detection cells. This data was meant to validate the modeling methods presented later in the document (in chapter 4). Creating an entire chip with custom cell design and block reuse, alongside with two application boards was extremely challenging, especially with limited resources and the constraints inherent to the test vehicle process. Despite extensive testing and validation, issues were met with the communication system responsible for outputting measurement data. However, the two regulation functions and the on-chip sensors worked properly. The extensive feedback and knowledge gained from the development of this custom chip is a ground work for new versions of this test vehicle and soft-failure research at silicon-level in general. It should help define testchip architectures in the future, and with the appropriate fixes the communication system will constitute a reusable and convenient framework for interacting with on-chip monitoring systems.

Chapter 4 is mainly focused on the development of tools for simulation environment. The value of simulation tools is well known, because it enables to detect issues very early in the development cycle, which is extremely valuable for avoiding late issues and cutting the cost of fixing them late. The main challenge for ESD at silicon-level is the complexity of the circuits and simulations. Convergence issues are very common and sometimes extremely difficult to avoid. Circuit complexity makes finding issues manually extremely hard. Most of the time, it is required to manufacture a first silicon to test the parts against ESD and identify soft-failures. To avoid very costly re-design and late fixes, new methods are required. In this research, two methods were developed and are described in detail.

The first method targets analysis and soft-failure prediction of analog function inside the chip, to detect weak spots during early design phase. It is constituted of two steps, a preliminary characterization and block modeling followed by a chaining process to connect multiple models together and predict their combined robustness. The char-

acterization is performed by injecting variable amplitude and variable width rectangular pulses. This characterization results in two different tables, that constitute the block model. Those tables or model can later be used to determine the response of the block on an output when an input is exposed to a stimulus. With multiple blocks, stimuli can be propagated from block to block, allowing to predict the shape of the waveform on the final output, just by knowing the waveform on the initial input. This approach was tested successfully on the test vehicle detailed previously. It has enabled to predict a failure on the regulator, for different input stresses inject on the battery input. In summary, this method was validated on a complex analog function coming directly from a real automotive product, and has made possible to predict the ESD robustness of this function using a purely behavioral model.

The second modeling method is more focused on facilitating cooperation between IC manufacturers and equipment manufacturers. It integrates well inside the SEED methodology, where interaction between these two actors helps design robust products against ESD with optimal cost and development time. The objective is to characterize and model the relationship between an input pin and an output pin, and to check if a board simulation can be conducted with this black-box IC model. It was shown that a TLP characterization constitutes a good base for a pin model, in particular for modeling input pins. For output pins that are supposed to drive a potential in DC conditions, it was demonstrated that this method does not work and requires modifications. The I(V) curve extracted with the TLP combined with a DC model fails to drive correctly the output voltage and current. It is an interesting result that calls for more research on this topic.

This research work is one of earliest studies on the topic of ESD-induced functional failures of integrated functions. It is probably the first to propose analysis and modeling methods at chip level capable of predicting the propagation of a disturbance through multiple analog block functions. The proposed simulation methods have shown great potential, and open up for many subsequent work and research. In particular, future work on the model-chain method could involve:

1. Simplification of waveforms into rectangular shapes: Waveforms are approximated by a single rectangular pulse. It was shown that some waveforms could be approximated better with multiple rectangular shapes. It is necessary to study if those multiple shapes could be applied on the model chain input and recombined at the end to deduce the impact of a complex input disturbance. Those potential improvements could improve further the accuracy of the model chain.

2. More robust characterization method: The influence of all elements of the characterization setup should be studied, and eventually taken into account in the model. The goal is to ensure that it is truly the block function that is being characterized, and that the characterization circuit does not interfere or impact the results. Ultimately, the model will be more portable and reusable.

3. Support of interactions between multiple pins: so far, the characterization is performed with one input and one output. It enables to apply a stimulus on an input

pin and deduce the signal on an output pin. The response on multiple output pins should be also be studied and modeled when multiple input pins are disturbed. It could enable to be complete models of analog functions that could reproduce the entire propagation of a fault inside the chip.

This concludes this study on the analysis and prediction of losses of functionality of analog integrated functions induced by electrostatic discharges. It is a first work that has explored many different approaches and has opened up new leads for future research work.

Appendices

Appendix A

TLP modeling

A.1 Validation curves

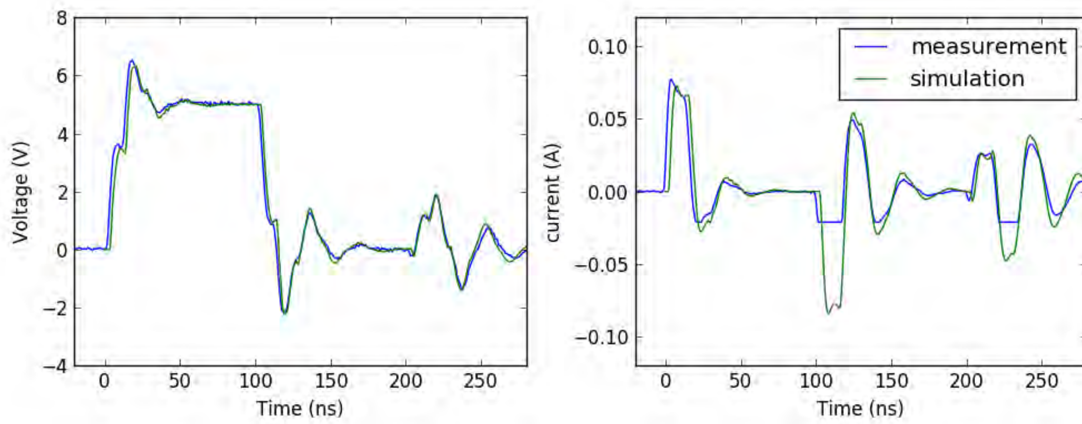

Figure A.1: Voltage and current waveforms comparison : 10 V charging voltage on open circuit

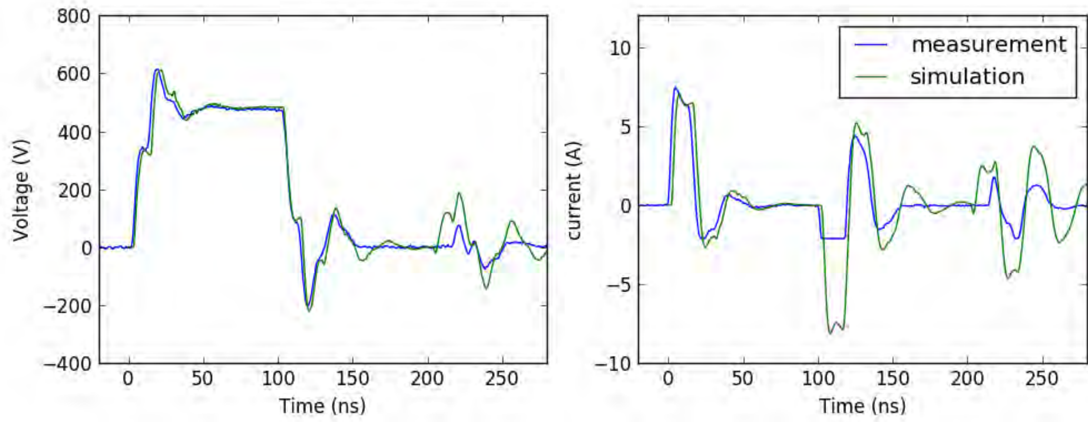

Figure A.2: Voltage and current waveforms comparison : 1000 V charging voltage on open circuit

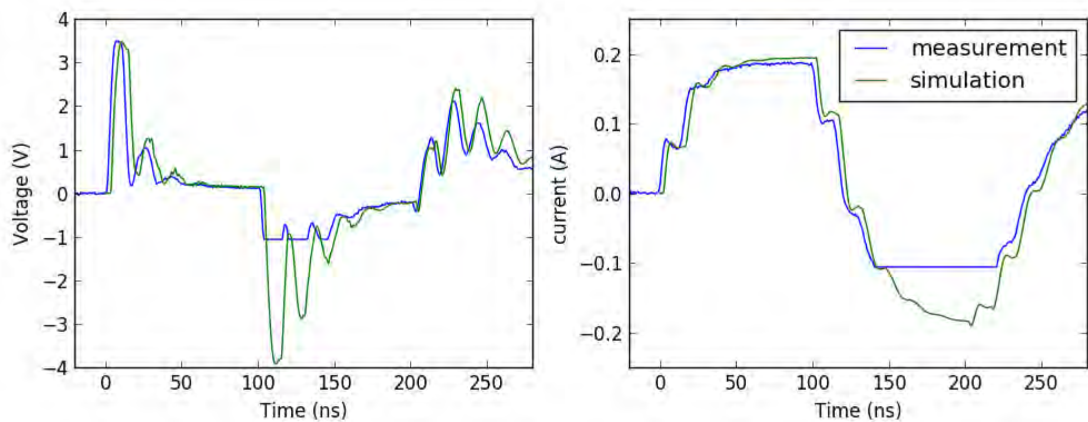

Figure A.3: Voltage and current waveforms comparison : 10 V charging voltage on a short circuit

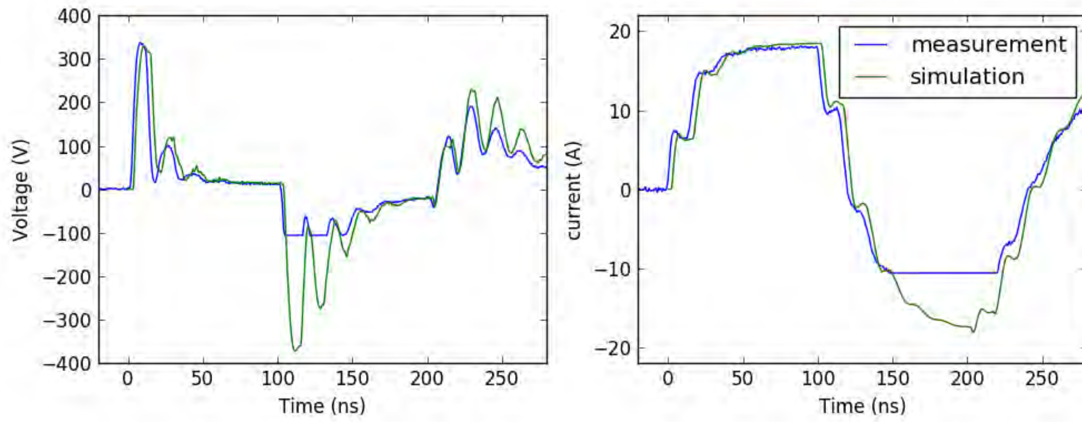

Figure A.4: Voltage and current waveforms comparison : 1000 V charging voltage on a short circuit

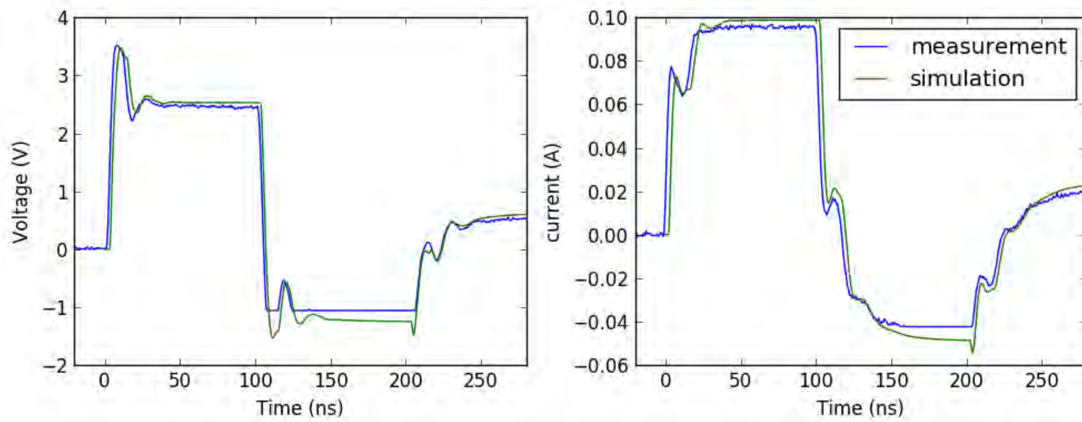

Figure A.5: Voltage and current waveforms comparison : 10 V charging voltage on 25 Ω

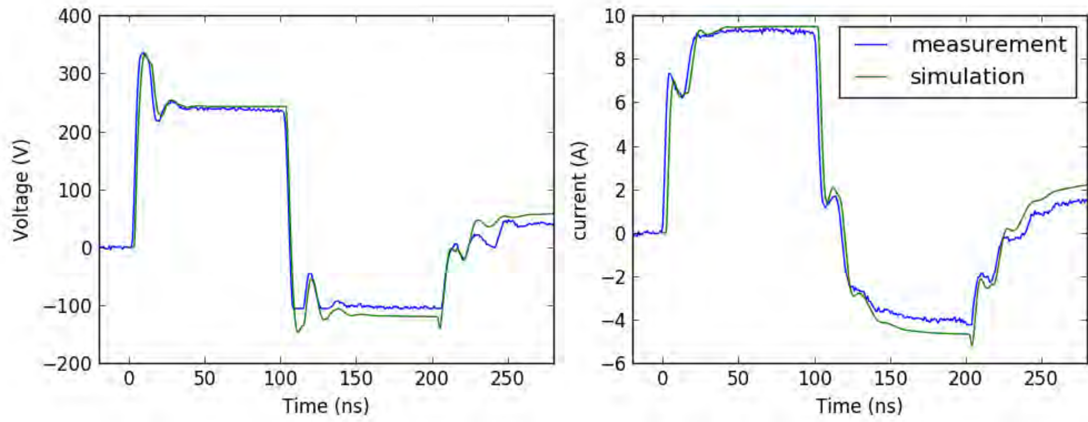

Figure A.6: Voltage and current waveforms comparison : 1000 V charging voltage on 25 Ω

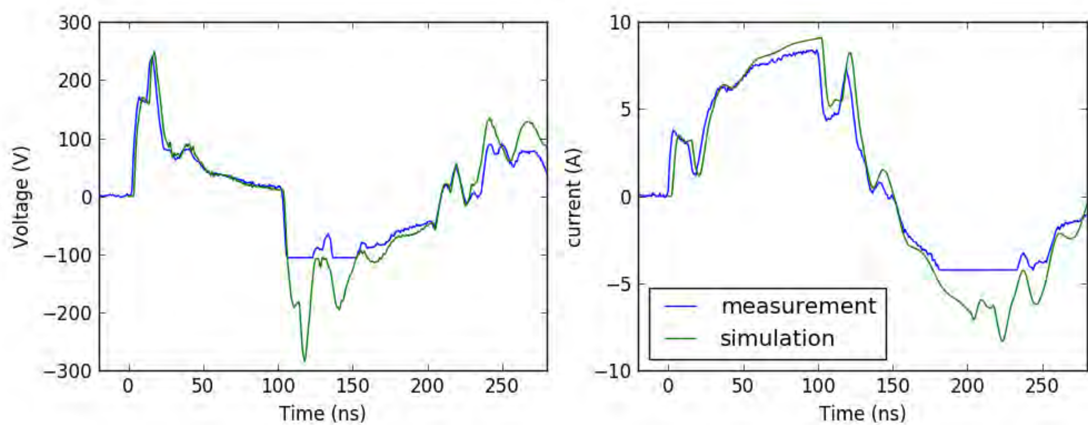

Figure A.7: Voltage and current waveforms comparison : 500 Vcharging voltage on a 470 nH inductor

Appendix B

Bottom-up block characterization and modeling

B.1 Characterizations

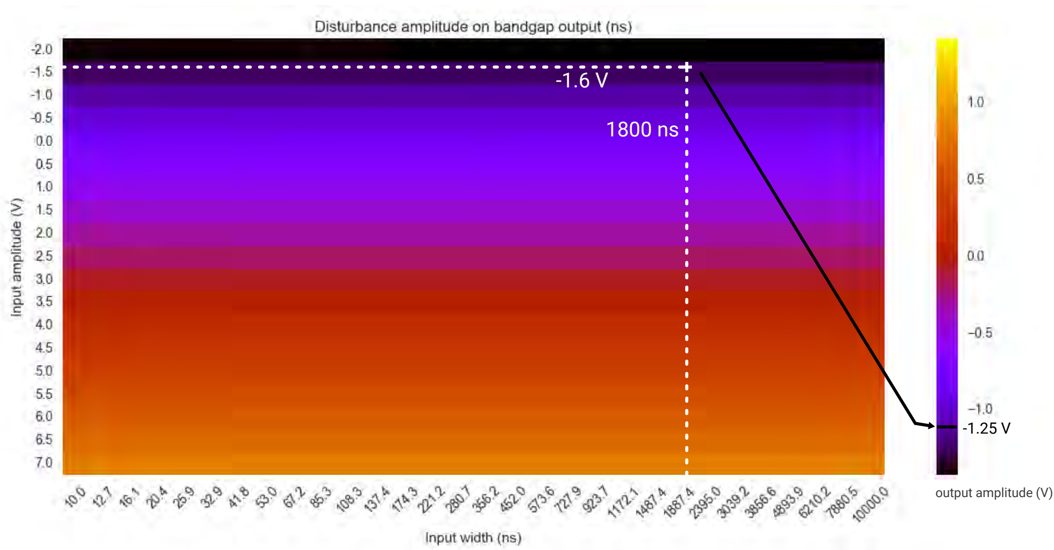

Figure B.1: Bandgap V_{clamp9} amplitude matrix

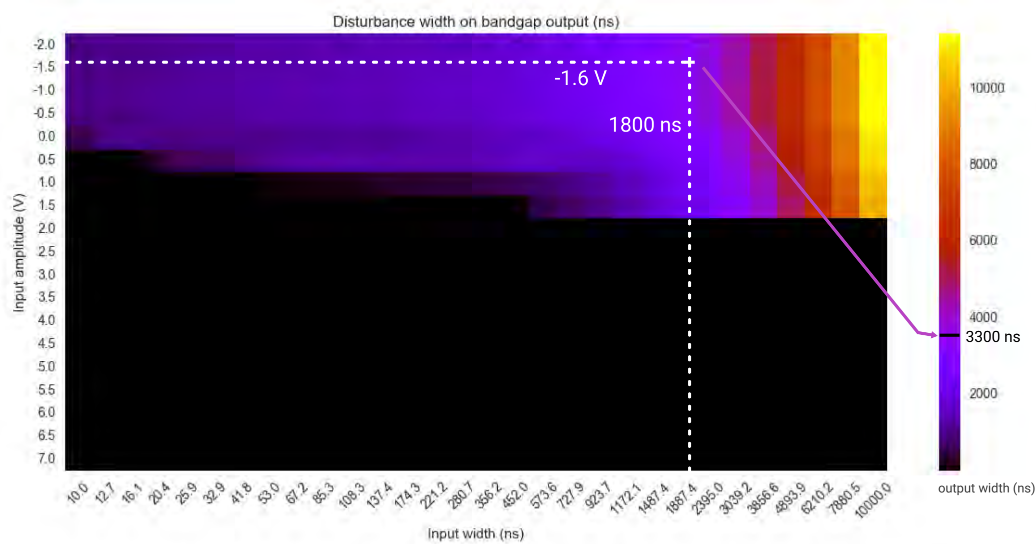

Figure B.2: Bandgap V_{clamp9} width matrix

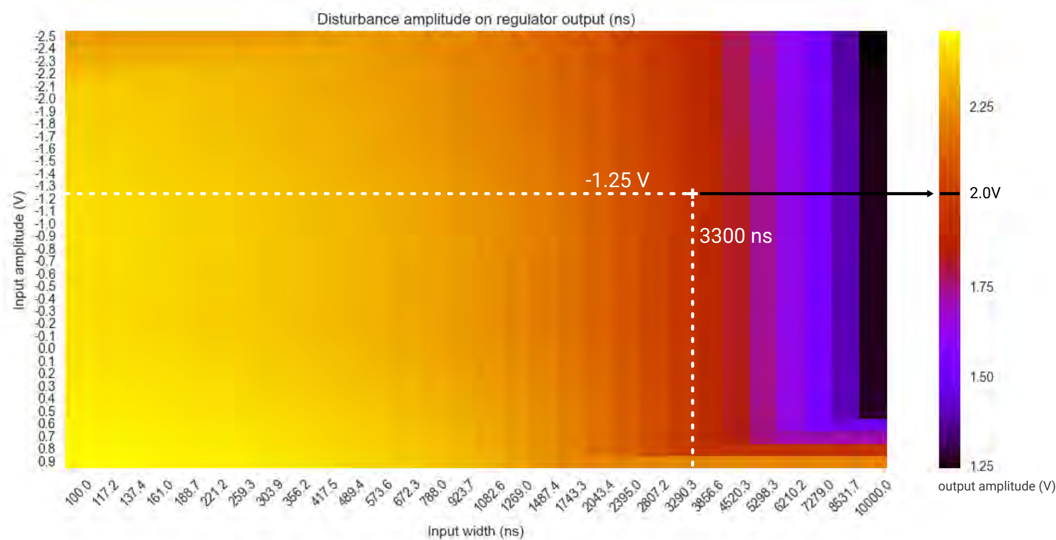

Figure B.3: Regulator V_{clamp9} amplitude matrix

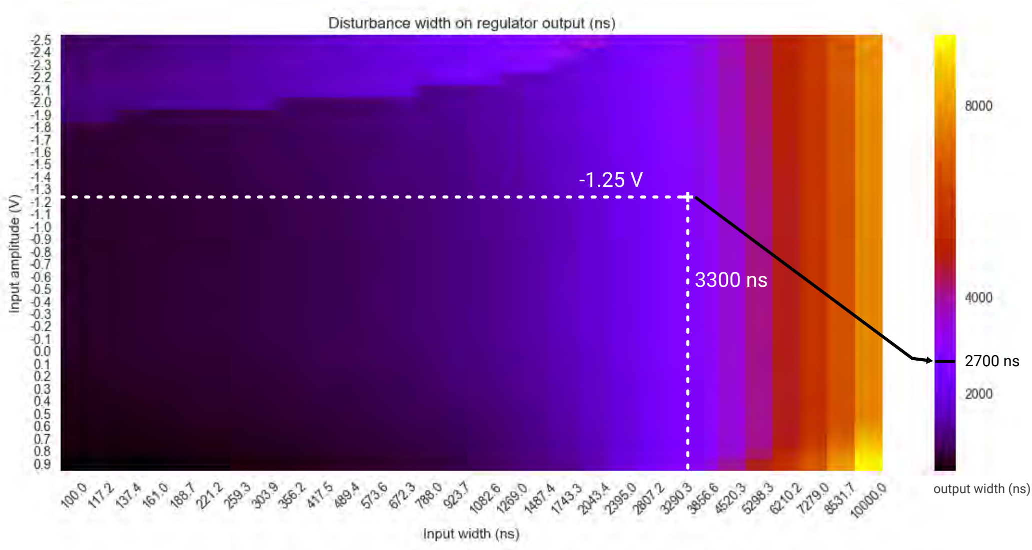

Figure B.4: Regulator V_{clamp9} width matrix

B.2 Improved model chain versus reference

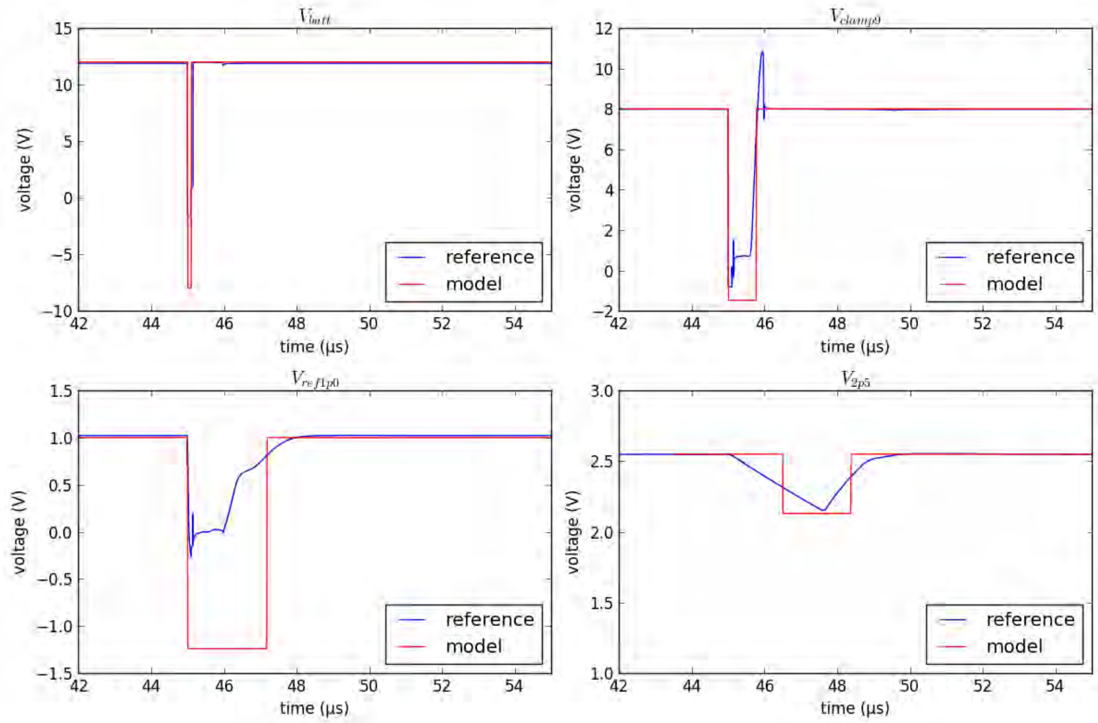

Figure B.5: Reference versus model chain waveforms for a −20 V 100 ns stimulus

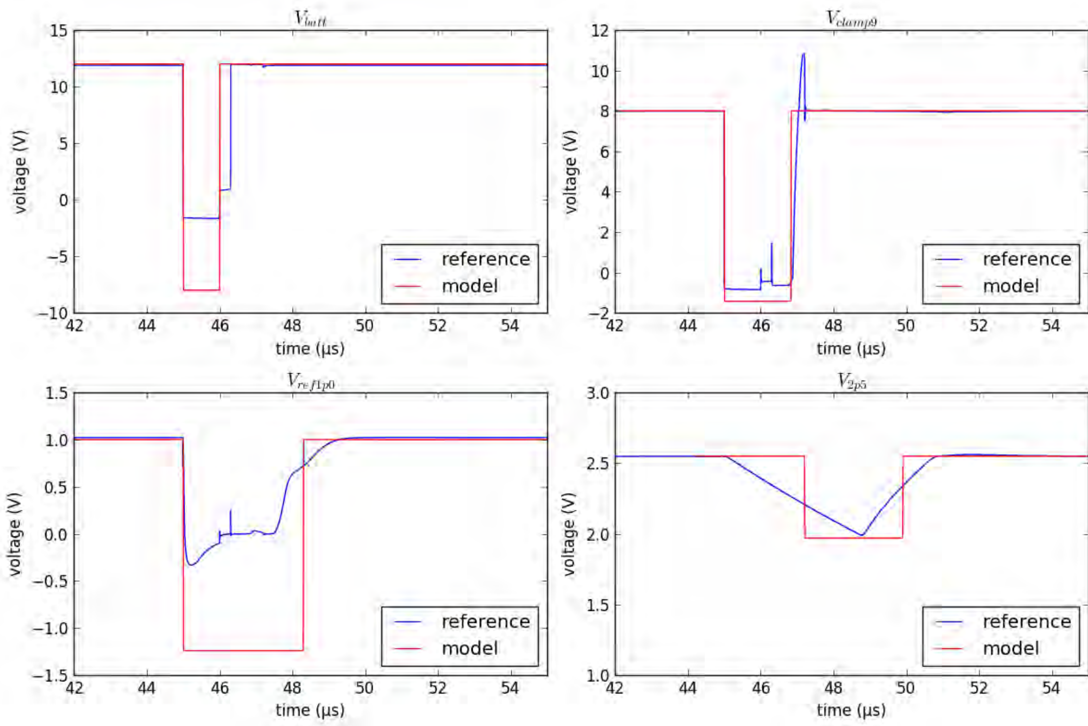

Figure B.6: Reference versus model chain waveforms for a −20 V 1 µs stimulus

Appendix C

Black box modelling

C.1 Additional validations

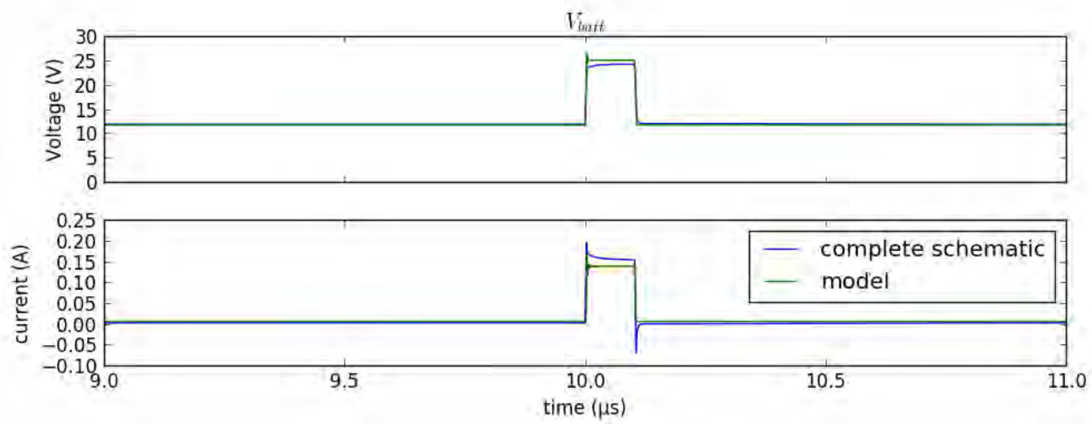

Figure C.1: Comparison of complete schematic and model simulations for input port (20 V TLP)

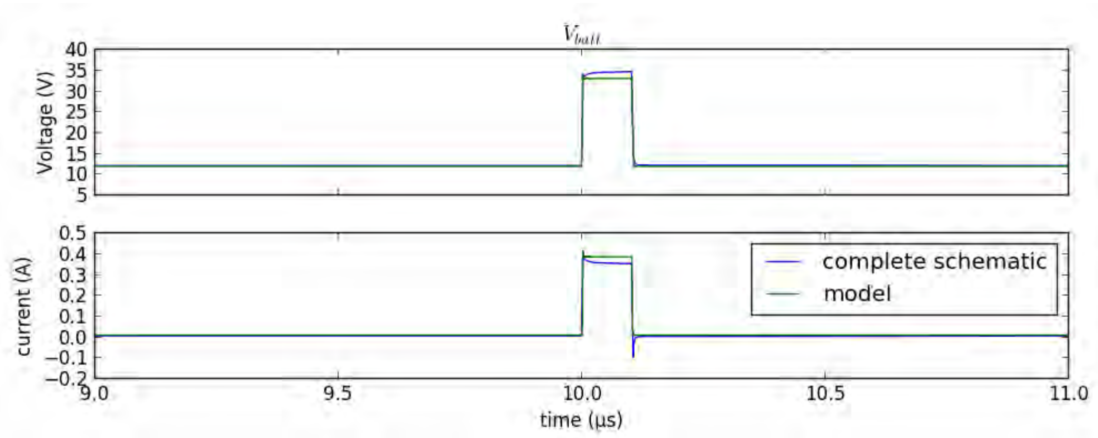

Figure C.2: Comparison of complete schematic and model simulations for input port (40 volt TLP)

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Acronyms

ASIC

Application Specific Integrated Circuit. 41, 81, 82, 101

BCI

Bulk Current Injection. 34

bias tee

A bias tee is a three-port network used for setting the DC bias point of some electronic components without disturbing other components . 84

BOM

bill of materials. 18, 137

CAN

Controller Area Network. 8

characteristic impedance

is the ratio of the amplitudes of voltage and current of a single wave propagating along the line; that is, a wave traveling in one direction in the absence of reflections in the other direction.. 45

CMOS

Complementary Metal Oxide Semiconductor. 18

DAC

Digital to Analog Converter. 90

D.C.

Direct Current : Conditions where the circuit voltages and currents are independent of time. 9, 30, 31, 33, 58, 70, 84, 104

DPI

Direct radio-frequency Power Injection. 31, 33

DUT

Device Under Test. 26, 28, 66

ECU

Engine Control Unit. 8

EMC

Electro-Magnetic Compatibility. 10, 52, 56

EMMI

Emission Microscopy. 37, 38

EPA

Electrostatic Protected Area. 15

ESD

Electro-Static Discharge. 8–12, 15–18, 20, 22, 24, 28, 30, 33, 36, 37, 40, 44, 50, 52, 62, 63, 81, 85, 87, 95, 96, 102, 104, 109, 121, 123, 133, 135

ESD gun

A device able to generate electro-static discharges in a laboratory environment for testing purposes.. 62, 63, 95

ESD protection

Electronic device that protects sensitive electronics from electro-static discharges, usually by deviating the discharge current into a near ground.. 95

ESR

Equivalent Series Resistor. 51

Fast Fourier Transform

A fast Fourier Transform algorithm computes the discrete Fourier transform of a discrete signal, or its inverse. Fourier analysis converts signals from usually time-domain to the frequency domain and vice-versa. Source: Wikipedia. . 76, 77

FPGA

Field Programmable Gate Array. 33

HMM

Human Metal Model. 26

I/O

Input and/or Output. 18, 41, 88, 95

IC

Integrated Circuit. 20, 31, 34, 40, 41, 50, 56, 123

LDO

A low-dropout or LDO regulator is a DC linear voltage regulator that can regulate the output voltage even when the supply voltage is very close to the output voltage.. 83

LIN

Local Interconnect Network. 8

MLCC

Multi-Layers Ceramic Capacitors. 51

MOS

Metal-Oxide Semiconductor. 15, 18

PCB

Printed Circuit Board. A printed circuit board (PCB) mechanically supports and electrically connects electronic components using conductive tracks, pads and other features etched from copper sheets laminated onto a non-conductive substrate. Source: Wikipedia. . 39, 41, 44, 50, 96

RF

Radio-frequency. 63

SEED

System Efficient ESD Design. 102, 123

SMD

Surface Mount Device. 50

S-parameters

Scattering parameters or S-parameters (the elements of a scattering matrix or S-matrix) describe the electrical behavior of linear electrical networks when undergoing various steady state stimuli by electrical signals. Source: Wikipedia. . 74–76

SPICE

Simulation Program with Integrated Circuit Emphasis. 20, 33, 41, 52, 58, 103, 104, 112, 123, 135

TCAD

Technology Computer-Aided Design. 41, 52, 135

TDR

Time-Domain Reflectometry. 22, 58, 77

TEM

Transverse Electro-Magnetic. 33

TLP

Transmission Line Pulsing. 20–23, 33, 34, 37, 40, 52, 58, 62–66, 84, 110, 124, 125, 129

TVS

Transient Voltage Suppressor. 52

Vector Network Analyzer

Instrument that measures network parameters of electrical networks. They are commonly used to measure S-parameters of two-port networks. Compared to an SNA (Scalar Network Analyzer), a VNA is able to measure amplitude properties, but also phase properties of the signals.. 74