Online ISSN 1848-3380, Print ISSN 0005-1144
ATKAFF 57(3), 589–598(2016)

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FCS-MPC Control Strategy for a New Fault Tolerant Three-level Inverter

DOI 10.7305/automatika.2017.02.1293
UDK [681.518.25.07-047.58:621.314.5.072.2.049]:629.7.067

Original scientific paper

In order to meet the high reliability of aviation inverters, the paper established a new three-level inverter which can increase the reliability in safety-critical applications, what's more, the new topology adding assistant leg to control neutral-point voltage independently. On the basis of the new topology, a mixed logic dynamic (MLD) model was established for the new inverter circuits, and takes finite control set model predictive control (FCS-MPC) for the new inverter. The method takes a discrete-time model of inverter to predict the future value of the all possible voltage vectors generated by the inverter. The vector which minimizes objective function in finite control set is selected as the control of inverter, the objective function used in this work evaluates the voltage error and the switch frequency at the next sampling time. The paper explicitly researched the solving algorithm and realization procedure of the new inverter circuit, its feasibility and validity is verified by the experiment.

Key words: Three-level inverter, Fault tolerant, Model predictive control, Mixed logic dynamic model

FCS-MPC upravljačka strategija novim trorazinskim izmjenjivačem otpornim na kvarove. Za postizanje visokog stupnja pouzdanosti avijacijskih izmjenjivača, u radu je postavljena nova topologija trorazinskog izmjenjivača za primjene u sigurnosno kritičnim sustavima koja ima dodatnu pomoćnu granu za nezavisno upravljanje naponom neutralne točke. Zasnivajući se na ovoj novoj topologiji, dinamički model s mješovitom logikom (MLD) postavljen je za električne krugove novog ispravljača koji za upravljanje pretvaračem koriste konačni skup upravljačkih signala dobivenih modelskog prediktivnog upravljanja (FCS-MPC). Metoda koristi vremenski diskretni model izmjenjivača za predviđanje budućih vrijednosti svih mogućih vektora napona koje generira izmjenjivač. Za upravljanje pretvaračem koristi se upravljački vektor iz konačnog skupa upravljačkih signala dobiven minimiziranjem funkcije cilja koja u obzir uzima grešku napona i frekvenciju sklapanja u sljedećem koraku diskretizacije. U radu je izravno razvijen algoritam za rješavanje problema i procedura za realizaciju nove topologije izmjenjivača, a izvedivost i validnost provjereni su eksperimentalno.

Ključne riječi: Trorazinski izmjenjivač, otpornost na kvarove, modelsko prediktivno upravljanje, dinamički model mješovite logike

1 INTRODUCTION

In recent years, the use of three-level inverters has increased during the last years in many application such as distributed generation, energy storage systems and uninterruptible power supply, due to lower harmonics of output voltage and current at same switching frequency compared to 2-level inverter[1-2]. However, the inverter still exist some problems, firstly, the unbalance of neutral point across the dc-link will generate order harmonic in output[3], a modulation strategy was proposed in [4] which ensures that the average neutral-point current within a switching period is equal to zero,. However, the non-idealities of the components, transients, etc., may cause the neutral-point voltage variation. Therefore, a closed loop controller is required to maintain the neutral-point voltage balance. The controllers proposed in [5] are based on nonlinear discontinuous model of the neutral-point voltage dynamics. This makes the controller design difficult. In [6] presents a four-leg hybrid converter, the fourth leg provides a reliable NP voltage under normal operation mode, However, when the fourth legs take the replacement of the fault phase, the NP voltage have to handle by the adjustment of control algorithm.

Secondly, since three-level inverters have a large number of semiconductor devices, which implies an increase in the number of components when compared with two-level inverter. This in turn brings a higher fault probability with a consequent reliability reduction, since any device failure may cause the inverter abnormal operation and economic losses [7], so improving the reliability is im-

portant to the continuous drive operation, one commonly practiced method is improving tolerance control [8][9] of the inverter, which may result in a degraded operation of the system, another way is made the inverter are operated in parallel to get the redundant operation [10]. In general, the new topologies of the three-level inverter should be researched.

Finite Control Set Model Predictive Control (FCS-MPC) is a sort of control strategy that can be applied for the control of power inverters, it makes use of the discrete finite number of switching states and the non-linear nature of the inverters, by the minimization of a objective function, which contains the goals, can be achieved by predicting the next output in the finite set of the switching states [11], it is widely used to control power electronic inverters. This technique has been successfully tested in [12],[13].

This paper presents a new solution to achieving fault-tolerant ability with the new three-level inverter and by adding an assistant leg to control neutral-point voltage independently to solve the control problem of neutral-point voltage.

In Section 2, an mixed logical dynamical (MLD) model for the new inverter model is founded. The three-level inverters which include discrete events in the differential equations are typical hybrid system, MLD model is one of the modeling methods of hybrid system [14], which takes the total system as a differential equation, so a MLD model could be founded in order to research the control of the new inverter. In Section 3 the FCS-MPC method of a new inverter based on MLD model is researched. In Section 4, the simulation and experiment are presented.

2 MATHEMATICAL MODEL OF INVERTER

2.1 The operation of new inverter

The new inverter topology is shown at Fig. 1, it consists in two symmetrical two-level inverters in series by transformers T_1 and T_2, switches $S_1 - S_6$ add to balance the voltage of neutral point O, the inverter output voltages have high order harmonic components due to the switching of the power semiconductors. Thus the inverter is connected to the load through a LC filter in order to provide a high quality sinusoidal voltage.

The switch states of A phase of inverter is shown in Tab. 1, similarly to the rest two phases, U_{A_1g} is voltage between A_1 and g, U_{A_2g} is voltage between A_2 and g, $r_1 - r_6$ are control signals of switch $S_{a1} - S_{a6}$, $r_7 - r_{12}$ are control signals of switch $S_{A1} - S_{A6}$.

In the new inverter, the special connection of the half-bridge modules was put forward as show in Fig. 2(b). The standard inverter unit in Fig. 2(a) is decompose into two bridge legs, when the two switches S_1, S_2 are conducted

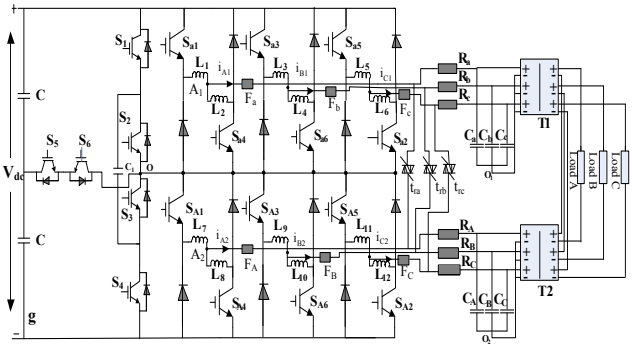


Fig. 1. New inverter topology

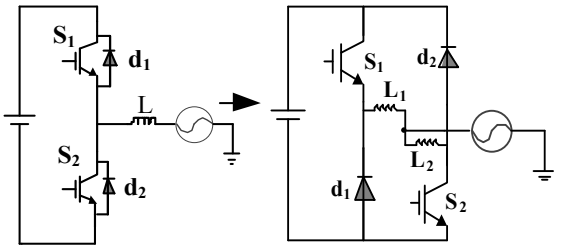


Fig. 2. Half bridge module

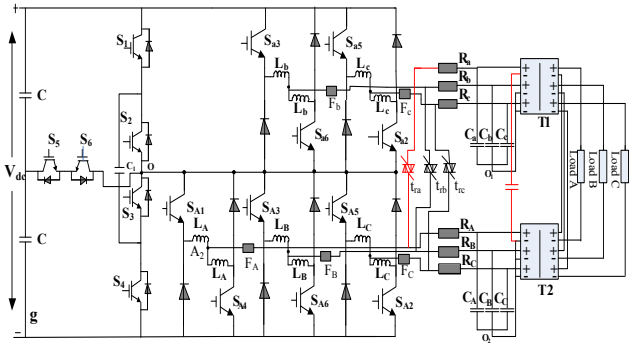
at the same time, the diodes d_1, d_2 can stop the short current, so the new modules guarantees that the shoot-through problem does not exist in the proposed topology, in this way, the dead time between the switches need not be set, the waveform quality of the voltage can be improved.

Within a three-level voltage source inverter, the probability of a failure in these devices is higher and must be therefore to be taken into account. Several factors can cause failures, such as transistor short-circuit and transistor open-circuit. The original NPC topology was changed by applying symmetry structure of two-level inverters. Obviously, the proposed topology has the additional redundancy to solve the semiconductors fault problems, as an example, suppose that an open-circuit failure of the *Sa1* power switch (phase A) while the inverter is supplying a three-phase nonlinear load, first step with some additional fast fuses connecting the failure leg to the symmetry half-bridge in order to realize continuous work as traditional two-level inverters (in Fig. 3(a))., in addition, it is nec-

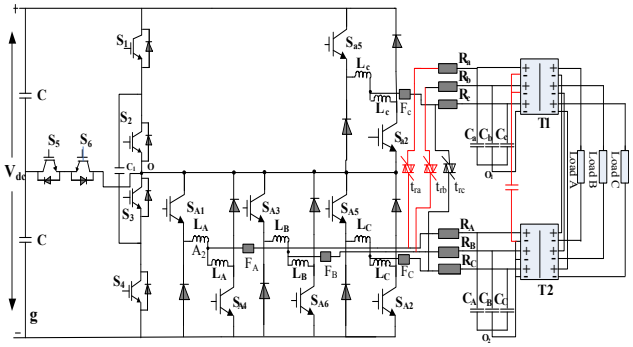
Table 1. Switch states of A phase

$(S_{a1}, S_{a4}, S_{a1}, S_{a4})$	$(U_{A_1g}$,$U_{A_2g})$
(1,0,1,0)	$(V_{dc}$,$V_{dc}/2)$
(0,1,0,1)	$(V_{dc}/2$,$0)$
(0,1,1,0)	$(V_{dc}/2$,$V_{dc}/2)$
(1,0,0,1)	$(V_{dc}$,$0)$

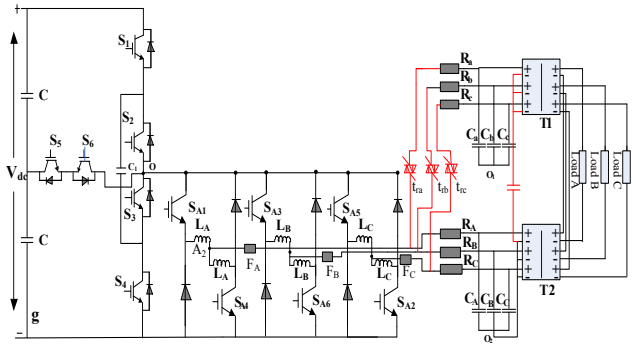
essary to connect the negative of the faulty output to the output of the symmetry leg. A similar process can be performed to two-phase fault Fig. 3(b) and three-phase fault Fig. 3(c), so the rest of the phases will be able to continue operating as two-level inverters normally.



(a) The fault-tolerant topology of one phase fault



(b) The fault-tolerant topology of two phase fault



(c) The fault-tolerant topology of three phase fault

Fig. 3. The inverter of fault events

To evaluate and compare the reliability of ANPC[15], NPC, and the new inverters, the inverter reliability is analyzed for a general purpose rather than an accurate reliability engineering calculation, therefore, some factors, such as quality factor, stress factor and temperatures factor are not considered. According to MIL-HDBK-217F military standard, the calculation method of reliability function of the device is show in literature [15] in detail.

The results in Fig. 4 show that the new inverter has higher reliability compared to ANPC and NPC inverters for multiple failure applications.

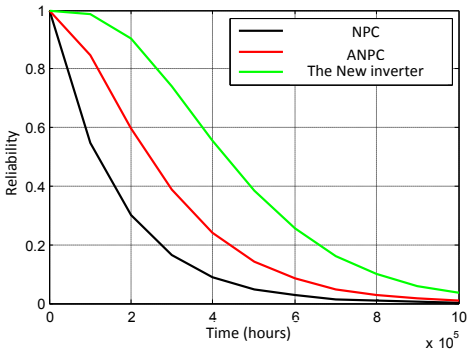


Fig. 4. Reliability with ANPC and NPC inverters

2.2 MLD model

MLD system can be viewed as a collection of systems of various types. A hierarchical structure arises when a logical control unit governs such a system by issuing logic decisions, this leads to the system framework shown in Fig. 5 which clearly illustrates this architecture. The top layer is a discrete event system, the bottom layer is a continuous system, the interface plays the role of facilitating communication between the two different layer by means of translating signals between them [16][17].

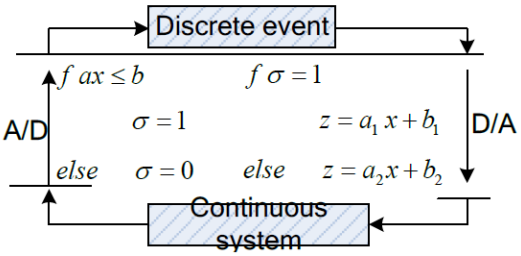


Fig. 5. MLD Structure Diagram

Each combination of switch state of inverter is defined as one discrete event, and each change of switch state will cause the inverter transforming from initial discrete event to objective discrete event.

For the inverter is symmetrical structures, the paper take phase A as an example, similarly to the rest two phases. As shown in Fig. 1, phase A of the inverter which form by the upper half-bridge A_1 and the lower half-bridge A_2, The switch states of phase A is shown in Tab. 1. The value of $r_1 - r_6$ are "1" or "0", and "1" means on, "0" means off, right is the positive direction of current i_{A1}, the working state of the upper half-bridge of phase A is shown as (1), similar way to the lower half-bridge.

$$\begin{array}{l}\text{when} \quad i_{A1} > 0\\ \quad \text{if} \;\; r_1 = 0, r_4 = 1, \text{then}, u_{A_1g}{=}V_{dc}/2,\\ \quad \text{if} \;\; r_1 = 1, r_4 = 0, \text{then}, u_{A_1g}{=}V_{dc},\\ \quad \text{if} \;\; r_1 = 0, r_4 = 0, \text{then}, u_{A_1g}{=}V_{dc}/2,\\ \text{when} \quad i_{A1} < 0\\ \quad \text{if} \;\; r_1 = 0, r_4 = 1, \text{then}, u_{A_1g}{=}V_{dc}/2,\\ \quad \text{if} \;\; r_1 = 1, r_4 = 0, \text{then}, u_{A_1g}{=}V_{dc},\\ \quad \text{if} \;\; r_1 = 0, r_4 = 0, \text{then}, u_{A_1g}{=}V_{dc},\end{array} \tag{1}$$

Replacing discrete event $i_{A1} > 0$ and $i_{A1} < 0$ with logical variable $\sigma_{A_1}{=}\,1$ and $\sigma_{A_1}{=}\,0$, "-" means "not". The mathematical expression of voltage u_{A_1g} is shown as (2), based on the logical relation in (1).

$$u_{A_1g} = V_{dc}\left[\bar{r}_4(r_1 + \bar{r}_1\bar{\sigma}_{A_1}) + \frac{1}{2}\overline{\bar{r}_4(r_1 + \bar{r}_1\bar{\sigma}_{A_1})}\right]. \tag{2}$$

The MLD model of the upper half-bridge of three phases can be shown as:

$$\left\{\begin{array}{l} u_{A_1g} = V_{dc}\left[\bar{r}_4(r_1 + \bar{r}_1\bar{\sigma}_{A_1}) + \frac{1}{2}\overline{\bar{r}_4(r_1 + \bar{r}_1\bar{\sigma}_{A_1})}\right]\\ u_{B_1g} = V_{dc}\left[\bar{r}_6(r_3 + \bar{r}_3\bar{\sigma}_{B_1}) + \frac{1}{2}\overline{\bar{r}_6(r_3 + \bar{r}_3\bar{\sigma}_{B_1})}\right]\\ u_{C_1g} = V_{dc}\left[\bar{r}_2(r_5 + \bar{r}_5\bar{\sigma}_{C_1}) + \frac{1}{2}\overline{\bar{r}_2(r_5 + \bar{r}_5\bar{\sigma}_{C_1})}\right]\end{array}\right. . \tag{3}$$

The relations between u_{A_1g} and $u_{A_1O_1}$, u_{B_1g} and $u_{B_1O_1}$, u_{C_1g} and $u_{C_1O_1}$ are shown in (4), where $u_{A_1O_1}$ means the voltages between point *A1* and neutral point O_1, $u_{B_1O_1}$ means the voltages between point B_1 and neutral point O_1, $u_{C_1O_1}$ means the voltages between point C_1 and neutral point O_1.

$$\left\{\begin{array}{l} u_{A_1O_1} = u_{A_1g} - u_{O_1g}\\ u_{B_1O_1} = u_{B_1g} - u_{O_1g}\\ u_{C_1O_1} = u_{C_1g} - u_{O_1g}\end{array}\right. . \tag{4}$$

In (4), u_{O_1g} means the voltage between neutral point O_1 and zero voltage point g, of which the expression is shown as (5):

$$u_{O_1g} = \frac{1}{3}\left(u_{A_1g} + u_{B_1g} + u_{C_1g}\right). \tag{5}$$

The discrete input vector of phase*A1, B1, C1* can be shown as (6):

$$\begin{bmatrix} u_{A_1O_1}\\ u_{B_1O_1}\\ u_{C_1O_1}\end{bmatrix} = \frac{V_{dc}}{3}\begin{bmatrix} 2 & -1 & -1\\ -1 & 2 & -1\\ -1 & -1 & 2\end{bmatrix} \times \times \begin{bmatrix} \bar{r}_4(r_1 + \bar{r}_1\bar{\sigma}_{A_1}) + \frac{1}{2}\overline{\bar{r}_4(r_1 + \bar{r}_1\bar{\sigma}_{A_1})}\\ \bar{r}_6(r_3 + \bar{r}_3\bar{\sigma}_{B_1}) + \frac{1}{2}\overline{\bar{r}_6(r_3 + \bar{r}_3\bar{\sigma}_{B_1})}\\ \bar{r}_2(r_5 + \bar{r}_5\bar{\sigma}_{C_1}) + \frac{1}{2}\overline{\bar{r}_2(r_5 + \bar{r}_5\bar{\sigma}_{C_1})}\end{bmatrix}. \tag{6}$$

In a similar way, the MLD model of the lower half-bridge of the three phases can be shown as:

$$\begin{array}{l} u_{A_2g} = V_{dc}\left[\frac{1}{2}\bar{r}_{10}(r_7 + \bar{r}_7\bar{\sigma}_{A_2})\right],\\ u_{B_2g} = V_{dc}\left[\frac{1}{2}\bar{r}_{12}(r_9 + \bar{r}_9\bar{\sigma}_{B_2})\right],\\ u_{C_2g} = V_{dc}\left[\frac{1}{2}\bar{r}_8(r_{11} + \bar{r}_{11}\bar{\sigma}_{C_2})\right].\end{array} \tag{7}$$

The discrete input vector of phase A_2, B_2, C_2 can be shown as (8):

$$\begin{bmatrix} u_{A_2O_2}\\ u_{B_2O_2}\\ u_{C_2O_2}\end{bmatrix} = \frac{V_{dc}}{3}\begin{bmatrix} 2 & -1 & -1\\ -1 & 2 & -1\\ -1 & -1 & 2\end{bmatrix} \times \times \frac{1}{2}\begin{bmatrix} \bar{r}_{10}(r_7 + \bar{r}_7\bar{\sigma}_{A_2})\\ \bar{r}_{12}(r_9 + \bar{r}_9\bar{\sigma}_{B_2})\\ \bar{r}_8(r_{11} + \bar{r}_{11}\bar{\sigma}_{C_2})\end{bmatrix}. \tag{8}$$

The output of the voltage of each phase equal to the summation of the upper half-bridge and the lower half-bridge:

$$\left\{\begin{array}{l} U_A = u_{A_1O_1} + u_{A_2O_2}\\ U_B = u_{B_1O_1} + u_{B_2O_2}\\ U_C = u_{C_1O_1} + u_{C_2O_2}\end{array}\right. . \tag{9}$$

Then, the discrete input vector of phase A, B, C in (9) is transformed to the expression of vector space by the transformation shown in (10):

$$U_{out} = \frac{2}{3}\left(U_A + \alpha U_B + \alpha^2 U_C\right), \tag{10}$$

where $\alpha = e^{j(2\pi/3)}$. Similarly, transforming three phase inductor currents i_f, three phase capacitor voltages u_c, three phase output currentsi_0 to the expressions of vector space, shown in (11):

$$\left\{\begin{array}{l} i_f = \frac{2}{3}\left(i_{Af} + \alpha i_{Bf} + \alpha^2 i_{Cf}\right)\\ u_c = \frac{2}{3}\left(u_{Ac} + \alpha u_{Bc} + \alpha^2 u_{Cc}\right)\\ i_0 = \frac{2}{3}\left(i_{A0} + \alpha i_{B0} + \alpha^2 i_{C0}\right)\end{array}\right. . \tag{11}$$

The dynamic performance of inductors and capacitors of inverter are respectively shown in (12) and (13):

$$\frac{di_f}{dt} = \frac{1}{L}\left(U_{out} - u_c\right), \tag{12}$$

$$\frac{du_c}{dt} = \frac{1}{C}\left(i_f - i_0\right). \tag{13}$$

Then, the MLD model of inverter can be shown as (14):

$$\begin{array}{l} \dot{x} = Ax + B_1U_{out} + B_2i_0,\\ y = Dx,\end{array} \tag{14}$$

where

$$x = \begin{bmatrix} i_f \\ u_c \end{bmatrix},\ A = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{bmatrix},\ B_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix},$$
$$B_2 = \begin{bmatrix} 0 \\ -\frac{1}{C} \end{bmatrix},\ D = \begin{bmatrix} 0 & 1 \end{bmatrix}.$$

The prediction model of inverter based on MLD model is shown in (15), which was obtained by the discretization of (14):

$$\begin{aligned} x(k+1) &= A^* x(k) + B_1^* u_n(k) + B_2^* i_0(k), \\ y(k) &= Dx(k), \end{aligned} \tag{15}$$

where $A^* = e^{AT_s}$, $B_1^* = \int_0^{T_s} e^{At} B_1 dt$, $B_2^* = \int_0^{T_s} e^{At} B_2 dt$.

2.3 The prediction model of reference output

In the proposed predictive algorithm, (15) is evaluated for each possible voltage vectors, giving different current predictions. The error between the voltage vector whose voltage prediction output and reference output should be close to zero, but the future reference value $u_c^*(k+1)$ is unknown. So it has to be predicted from the present and previous values, the reference output will be obtained by the second order Lagrange extrapolation formula [18], which is adopted in this paper, and shown in (16):

$$u_c^*(k+1) = 3u_c^*(k) - 3u_c^*(k-1) + u_c^*(k-2). \tag{16}$$

3 FCS-MPC OF THE INVERTER

3.1 Control of The Additional Leg

An important issue for multilevel inverters is the neutral point balancing, in order to balance the neutral point we need control the redundant leg. Before the in new inverter start to work, the voltage of the dc link capacitor C1 should be stable at around one half of the dc-link voltage.

In order to reduce the number of switching events in the fourth leg, the strategy shown in Table 2 is proposed. In this case, the state of the switches is determined in accordance with the voltage in the capacitor, the output currents, and the interval (or duty cycle) at which the output phases are connected to the NP. Then the variables of neutral voltage and current deviation are given as follows:

$$\begin{aligned} \Delta U &= V_{dc}/2 - U_{c1}, \\ i_{NP} &= d_{s_{a4}} i_{s_{a4}} + d_{s_{a6}} i_{s_{a6}} + d_{s_{a2}} i_{s_{a2}} \\ &\quad + d_{s_{A4}} i_{s_{A4}} + {}_{s_{A4}}\, d_{s_{A6}} i_{s_{A6}} + d_{s_{A2}} i_{s_{A2}}, \end{aligned} \tag{17}$$

where, d_{sx} is the duty cycle of IGBT which is connected to the natural point O in a sampling cycle, and i_{NP} is the locally averaged NP current.

Nevertheless, there still exist some problems that may occur in the switching process of the fourth leg, the following conditions are used to for in-depth analysis.

- If S2 and S4 are activated, the switching state will be known as "state A."
- If S1 and S3 are activated, the switching state will be known as "state B."

Table 2. Selection of the Proper State

$\Delta U > 0$	$i_{NP} > 0$	Action	C_1 states
1	1	$B \to A$	Discharge
1	0	$A \to B$	Discharge
0	1	$A \to B$	Charge
0	0	$B \to A$	Charge

If the current flowing through the NP i_{NP} is positive when switching occurs in the fourth leg, this current will flow through the D_1 and D_2 diodes as soon as S_2 is deactivated, meaning that a low voltage level will be obtained in the NP (Fig. 6(a)).

On the other hand, the current flowing through the neutral point i_{NP} is negative when switching occurs in the fourth leg, this current will flow through diodes D_3 and D_4 as soon as S_4 is deactivated, and a high voltage level will be obtained at the NP (Fig. 6(b)). It can be observed how the voltage through the NP may temporarily vary between the high and low voltage levels, depending on the direction of the current flowing through this point. These glitches introduce certain harmonic distortion in the output voltages generated.

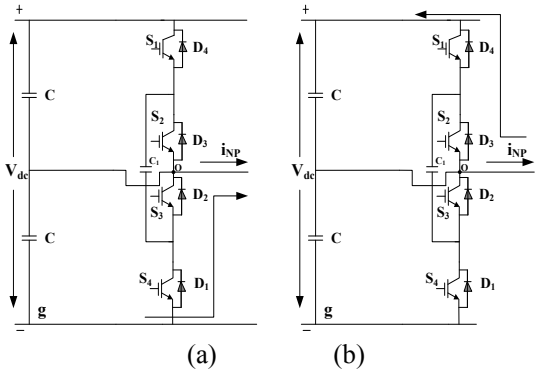


Fig. 6. Fourth-leg switching process between states "A" and "B" when (a) i_{NP} is positive and (b) i_{NP} is negative

Table 3 in Appendix outlines the switching sequences of the modified fourth leg shown in the inverter of Fig. 1. The conditions followed are the same as that used in Table 2. With this sequence, the voltage at the NP is always equal to $V_{dc}/2$, which means that the risk of glitches in the voltage waveform will be eliminated.

3.2 The choice of objective function

The transformation from three-phase static voltage A, B, C to two phase static $\alpha\beta$ is called Clarke static transformation. The transformation equations can be expressed as:

$$X_{\alpha\beta} = T_{ABC/\alpha\beta} X_{ABC}, \tag{18}$$

where,

$$T_{ABC/\alpha\beta} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}. \tag{19}$$

The relationship between U_α, U_β and U_A, U_B, U_C is as follows:

$$\begin{bmatrix} U_\alpha & U_\beta \end{bmatrix}^T = T_{ABC/\alpha\beta} \begin{bmatrix} U_A & U_B & U_C \end{bmatrix}^T. \tag{20}$$

Three-level inverter has 27 voltage vectors [19][20], which are used to design FCS-MPC for inverter. In order to choose a optimal voltage vector to control inverter, firstly, the values of $U_c(k+1)$ of 27 vectors are respectively computed according to expression (15). The choice of the optimal-model-based vector system may require high computational resources and high-speed real-time digital control systems, this paper adopts a new predictive control method [21],which uses the model equations of the system just once in each control cycle to predict the ideal optimal vector needed to control the state space variables. The choice of the converter output vector is obtained by minimizing the distance between the ideal vector and the converter available vectors, the vector corresponding minimal value of distance is selected as the control signals of inverter[22].

In this paper the new inverter is operated as a voltage source, three independent variables can be controlled – two ac line voltages $U_\alpha(t)$ and $U_\beta(t)$. The main objective of the optimizing controller must be the minimization of the ac line voltage errors, thus a linear or l_1-norm cost function can be set up in (21):

$$J = |U_\alpha^* - U_\alpha(k+1)| + \left|U_\beta^* - U_\beta(k+1)\right|, \tag{21}$$

where U_α^* is real part of output voltage of reference, U_β^* is imaginary part of output voltage of reference, U_α^* is real part of predictive voltage, U_β^* is imaginary part of predictive voltage.

3.3 The structure diagram of control strategy

A block diagram of the proposed method applied to the voltage control for the new inverter is shown in Fig. 7.

The main functions realized by Fig. 7 are listed as followings:

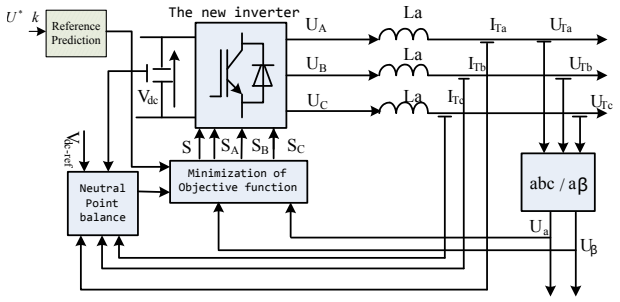


Fig. 7. The block diagram of FCS-MPC

1) The prediction module forecasts reference voltage of reference at next time using (16), and the results are sent to the module of objective function.

2) The prediction module forecasts the output voltage of inverter using (15). However, in the experimental verification, the delay provided by the digital signal processor and switching devices is inevitable[23], so it must be compensated. In an easy way, the delay provided by the digital signal processor can be compensated by calculating the cost function at the end of the next sampling period $U_c(k+2)$.

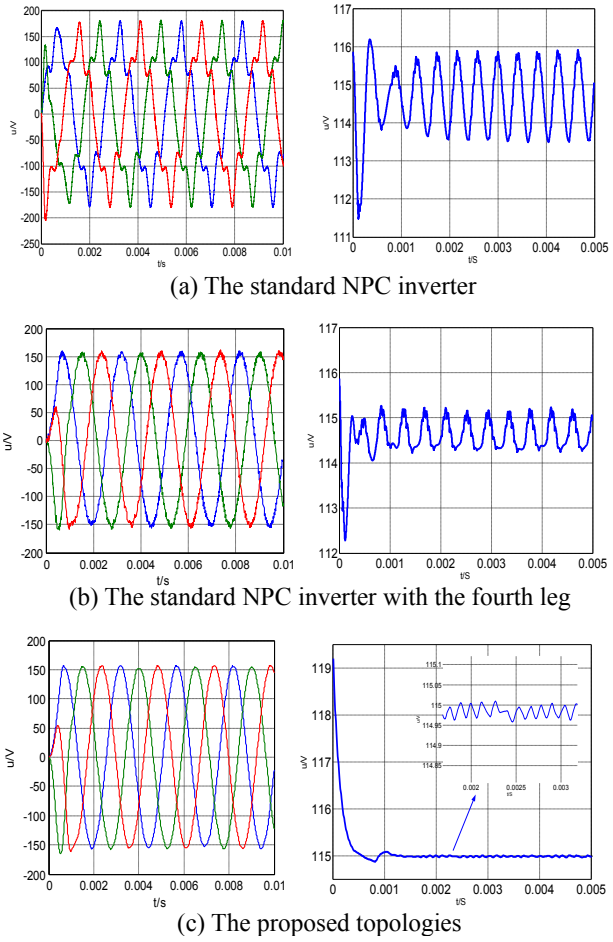
3) The current i_{NP} is computed by the expression of (17) using voltage of capacitor C_1.

4) The switch state, which minimizes the value of expression (21), is selected by the module of objective function as the control of inverter. This process is applied to every possible voltage vector generated by the inverter.

4 SIMULATION AND EXPERIMENT VERIFICATION

With topology of the new inverter in Fig. 1, the proposed control strategy is verified according to simulation based on MATLAB/SIMULINK, the parameters of simulation are shown as followings, $V_{dc} = 270$V, $L_1 = L_2 = \cdots L_{12} = 2$mH, $C_a = C_b = C_c = C_A = C_B = C_C = 40\mu$F, $C_1 = 8800\mu$F, $R_a = R_b = R_c = R_A = R_B = R_C = 25\text{m}\Omega$, sampling period T_s is 10μs, f means rated frequency is 400Hz. The fourth leg commutates alternating its state at every sampling cycle.

Fig. 8(a) shows voltage waveforms from the standard NPC inverter operate under a nonlinear load, the system becomes unstable. These wave-forms are show in Fig. 8(b), note that with the fourth leg the improved NPC inverter can reduce the low-frequency NP voltage oscillation. Whereas, in Fig. 8(c) the same load is connected to the proposed inverter, observing that the low frequency voltage oscillation in the NP is removed, and there are practically no glitches

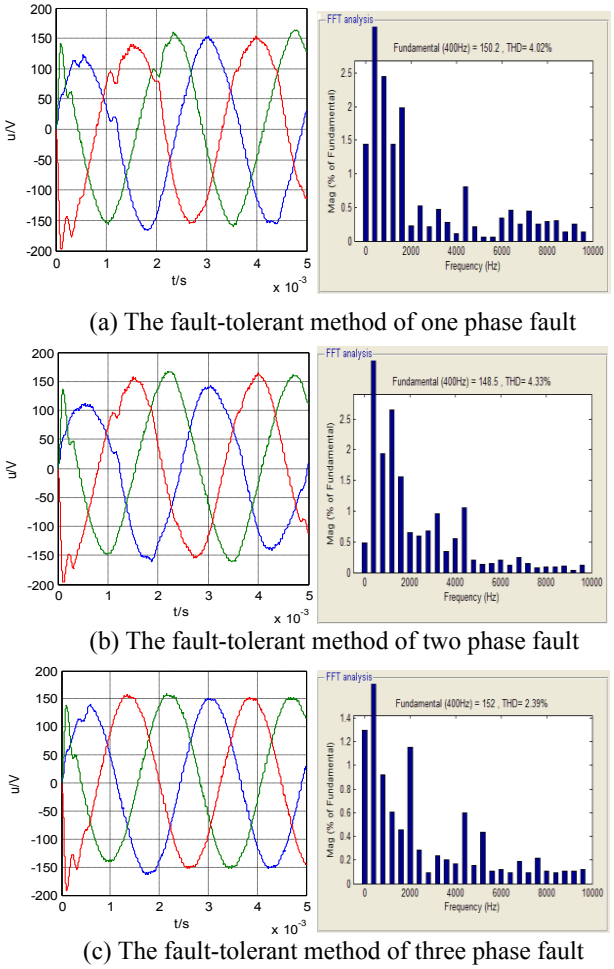


(a) The standard NPC inverter

(b) The standard NPC inverter with the fourth leg

(c) The proposed topologies

Fig. 8. Voltage waveforms and neutral Voltage for inverter over an nonlinear load



(a) The fault-tolerant method of one phase fault

(b) The fault-tolerant method of two phase fault

(c) The fault-tolerant method of three phase fault

Fig. 9. Simulation result of the faults

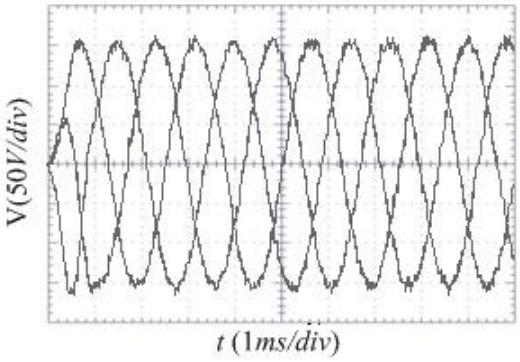
in the generated voltage waveforms, so the quality of these voltages is maximum attainable.

Simulation are carried out to confirm the fault tolerant of the proposed topology, Fig. 9(a) shows that the one phase fault in Sa1, it can be compute the three phase voltage THD (Total Harmonic Distortion)are 4.02%. So it can meet the demand of aviation requirement (THD<5%). Fig. 9(b) and (c) shows the results obtained when a two phase and three phase faults are happened to the topology of Fig. 1, respectively, from the results the voltage THD is acceptable to the standard.

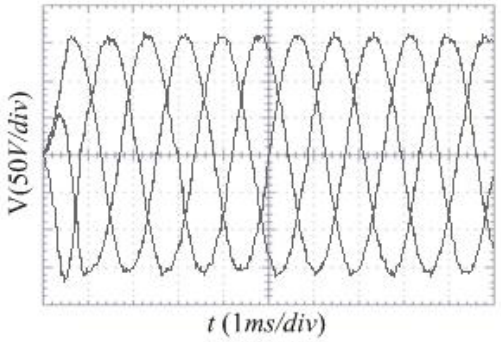
An experimental setup was developed using a DSP model TMS320C6713 for a sampling time $T_s = 10\mu$s, the operating conditions are given as follows: $V_{dc} = 270$V, $L = 2$mH, $C = 40\mu$F. Fig. 10(a) shows the voltage waveform obtained with the traditional fourth leg prototype under the nonlinear load conditions THD=2.96%, it can be observed the certain glitches appear in the output voltage waveform. As mentioned in the Section 3, this is due to the deadtimes allowed for the proper operation of the IGBTs of the fourth leg. On the other hand, Fig. 10(b) shows the output voltages waveform of the proposed topology, THD=1.74%. When the fault occurs in phase A1, the fault tolerant ability is shown in Fig. 10(c), THD=4.58%. At last the result of neutral point voltage control is given in Fig. 10(d).

5 CONCLUSION

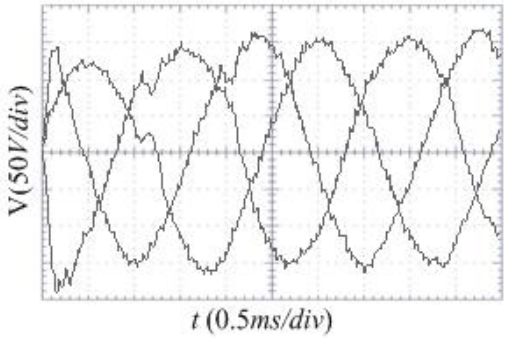
This paper presents a new approach to the three-level inverter in terms of fault-tolerance, the new inverter combined with an additional leg to control neutral-point voltage independently. On the basis of the new topology, a MLD model of inverter has been set up, and the model is used as the prediction model to research FCS-MPC for inverter, which guarantees well steady state characteristics and transient characteristics of inverter, the quality of output voltages has been also improved, in addition, the new topology combines with two-level inverter control tech-



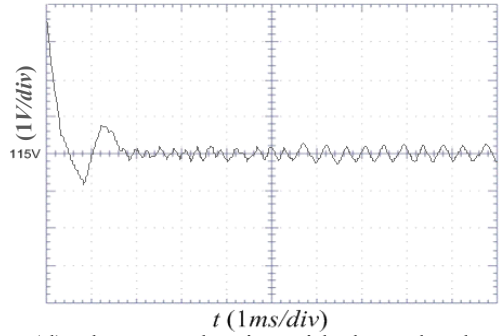
(a) The steady output voltage waveform



(b) The output voltage waveform under measurement noise



(c) The one phase fault test result



(d) The neutral point with the redundant leg control

Fig. 10. Experiment results

nique ensures the fault-tolerance to multiple failure modes of the semiconductors, the feasibility and effectiveness of control strategy are verified by experiment results.

ACKNOWLEDGMENT

This work support by the National Basic Research Program of China (973 Program)(2015CB755800).

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Table 3. Activation sequence of the fourth leg

Sequence	Transition between the states	$i_{NP} > 0$	Step1	Step 2	Step 3	Step 4	Step 5	Step 6
1	$A \rightarrow B$	1	Deactivate S_4	Activate S_5	Deactivate S_2	Activate S_1	Deactivate S_5	Activate S_3
2	$A \rightarrow B$	0	Deactivate S_2	Activate S_6	Deactivate S_4	Activate S_3	Deactivate S_6	Activate S_3
3	$B \rightarrow A$	1	Deactivate S_3	Activate S_5	Deactivate S_1	Activate S_2	Deactivate S_5	Activate S_4
4	$B \rightarrow A$	0	Deactivate S_1	Activate S_6	Deactivate S_3	Activate S_4	Deactivate S_6	Activate S_2

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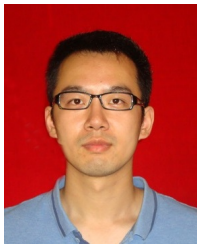

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Received: 2015-04-25
Accepted: 2016-10-06