ABSTRACT

Title of Thesis:	FAILURE MODES AND MECHANISMS ANALYSIS OF SILCON POWER DEVICES
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Silicon power devices are a major reliability concern for power electronics converters. Failure modes, mechanisms, and effects (FMMEA) is a well-established method for identifying and analyzing the critical failure mechanisms and improving the reliability of a system through the process. The effects of the various failure mechanisms (and modes) are system dependent and cannot be identified in isolation. This work establishes a Failure Modes and Mechanisms Analysis (FMMA) for silicon power devices that identifies the relevant failure modes and mechanisms for those components. Following the FMMA, a set of failure analysis case studies of silicon power devices which aid in the identification of failure causes and mechanisms for the FMMA are described. Finally, the criticality of the different mechanisms is discussed based on the severity of a failure within a given system, the occurrence of a failure mechanism for a given component, and the ability to detect a failure using techniques such as PHM, criticality can be identified for the mechanisms.

FAILURE MODES AND MECHANISMS ANALYSIS OF SILICON POWER
DEVICES

by

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Thesis submitted to the Faculty of the Graduate School of the
University of Maryland, College Park, in partial fulfillment
of the requirements for the degree of
Master of Science
2017

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Acknowledgements

First, I would like to thank my advisors Dr. Diganta Das and Prof. Michael Pecht for the many opportunities they have afforded me in my four years of undergraduate and graduate research at the University of Maryland and the Center for Advanced Life Cycle Engineering (CALCE). Their guidance and support throughout my education has helped me grow into a more complete engineer and a more critical thinker. Additionally, thank you to Prof. Abhijit Dasgupta and Prof. Patrick McCluskey for serving on my committee and providing invaluable insights.

Next, I would like to thank the many interns, Lukas Biel, Oguz Yz, Anderson Mbomgne, Daniel Weeber, Rafael Gudlin, Mateus Von Breit, and many others who so diligently supported my work at CALCE, all while visiting from a foreign country, learning a new field of study, and struggling with English as a second language. Without their efforts, this work would not have been possible.

I would also like to thank the many graduate students and research scientists at CALCE that I have had an opportunity to share my time with and learn from. Working with such a diverse and intelligent group has been an honor. Spending time with each of you in technical and, perhaps more importantly, non-technical discussion provided me with support, guidance, or even simply a break which was instrumental to the completion of this work.

To my family and friends, I thank you all for your love and support throughout my life, particularly over the last few years during my graduate career. To my father, who supported my siblings and me and provided us with more than we could ever ask

for despite the unfortunate passing of my mother, I am forever grateful. To my mother, I am thankful for the invaluable memories that act as a source of love, hope, and inspiration which she left my siblings and me with. To my siblings, Allison, Michael, and Lindsay, thank you for your support at home and the breaks from the stresses of work. To Christine, I am thankful for your love and the round-the-clock support you provided me during my graduate career. I am fortunate to have many great friends who have spent time with me, laughed with me, and supported me along the way. All of your support played a vital role to this work.

Finally, I'd like to thank the many companies that provide financial support to the research efforts at the University of Maryland and CALCE, making this work possible.

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Chapter 1: Introduction to Power Electronics

Electronics are increasingly ubiquitous in our daily lives as many existing and new technologies we rely on are electronic in nature. From the electric trains and vehicles we use for transportation, to the new wearable electronics which monitor our health, to the computers and cellphones which increase our productivity and allow us to communicate, the applications of electronics are endless and growing. All of these systems require a source of electrical power at a variety of voltages and frequencies. Power electronics systems are those systems which convert one form of electricity into another [1].

Traditionally, power is generated at a central location where it is sourced from the burning of fossil fuels, solar radiation, wind energy, or geothermal. The electricity is then sent over large distances through three-phase alternating current (AC) transmission lines to distribution substations. The power is sent using three-phase AC as it is more efficient than sending through single phase AC. The electricity is then converted from three-phase AC to single-phase AC to be distributed to residential homes. There are two main forms of residential AC power, the North American standard at 120V and 60Hz and the European standard of 240V at 50Hz. However, most of the electronics we use are designed to operate at a specific frequency and voltage level which is different from the single phase AC standards.

That is to say that most of the electronics we use must first convert their source of electricity into one that they can function with through some form of power electronics converter. Take for example a typical cell phone battery and charger. The

lithium ion battery is charged using a battery monitoring system which is generally powered using a 5V direct current (DC) USB standard. This means that in order to charge the cell phone's battery from a wall outlet, the power must first be converted from standard wall power of single phase AC to a 5V DC using an AC-DC converter. Another example is solar power which is generated at a central solar station using solar irradiation on panels which output a DC form of electricity. This DC power must then be converted through an inverter into three-phase AC power for transmission to the end users. The on-demand capability and reliable operation of the power electronics within or associated with the electronics they source is therefore essential to the electronics operation.

1.1 Power Electronics Topologies

There are many different forms of power electronic converters including AC-DC, DC-DC, DC-AC, and AC-AC. Most of these power electronic converters are achieved by assembling a variety of active and passive components. These components are switches, diodes, capacitors, inductors, and resistors. The use of switches allows for the converter to operate in discrete states depending on whether any given switch is in the open or closed state. Electrical analysis of the various states of the switches shows that the input voltage is then converted to an output voltage of differing voltage level and/or frequency. Complete electrical analysis of each type of electrical converter is outside of the scope of this work however, they can be found in Mayergoyz [1].

As a result of the switching between multiple operating states, ripples in the output voltage and current profiles develop. Passive components such as capacitors and inductors act to reduce this ripple across the output of the converter. However, the use

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of passives increase the size of the converter. There is general trend for reduction in size weight power, and cost throughout the market. One method for reducing the size and weight of the components is by reducing the ripple caused by the switching and therefore allowing for the use of smaller and lighter passive components. To reduce the ripple, power electronic converters are being manufactured with switches that operate at higher frequencies which reduces the time required between operating states.

Two examples of topologies are shown in Figure 1 and Figure 2. The first is a DC-DC boost converter which converts one form of DC power to DC power at a higher voltage. During a switching period, the switch is in the on-state for some portion of the time and the off-state otherwise. The portion of time that the switch is in the on-state divided by the total switching period is defined as the duty cycle (D). By definition the range of the duty cycle is between 0 and 1. The output voltage, V_{out}, for this DC-DC converter is:

$$V_{out} = \frac{V_{in}}{1 - D} \tag{1}$$
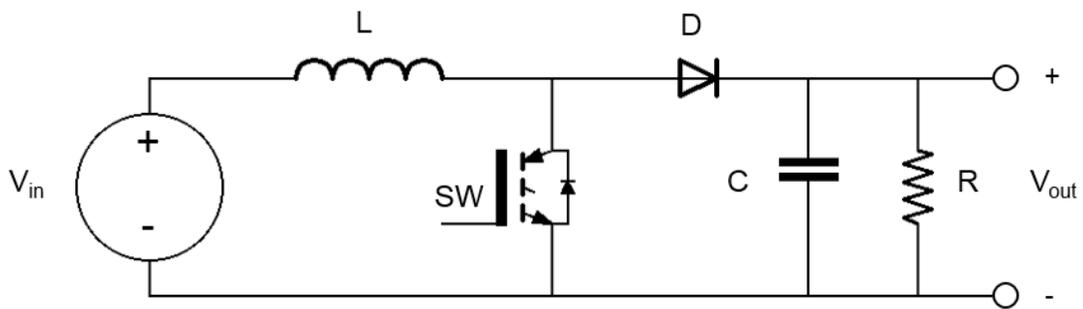
Figure 1: DC-DC boost converter

The second converter shown in Figure 2 is a DC-AC single phase converter. This converter operates on a more complex switching principle than the DC-DC boost converter shown in Figure 1, called Pulse-Width Modulation (PWM). The name refers

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to the fact that to achieve the desired AC output power, the converter is continually modulating the duty cycle of each of the switches. The use of PWM techniques allows for the AC output voltage to take on any frequency up to practical limits of the switching devices. A complete discussion of PWM techniques can be found in Mayergoyz [1].
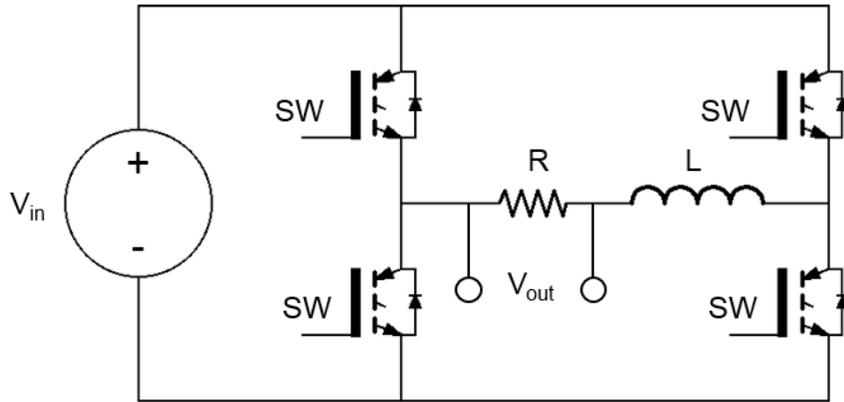
Figure 2: DC-AC single phase converter

There are a variety of AC-AC converters, the most well-known of which are transformers. However, transformers are limited to converting AC power of one voltage level to AC power of another voltage level and cannot be used to change the frequency of the AC power. Many applications operate by changing the input AC frequency, such as an AC motor changing frequency input to achieve a different output torque. To achieve variable output frequency, the input power is sent to an AC-DC converter whose output is connected to the input of a DC-AC converter, see Figure 3.
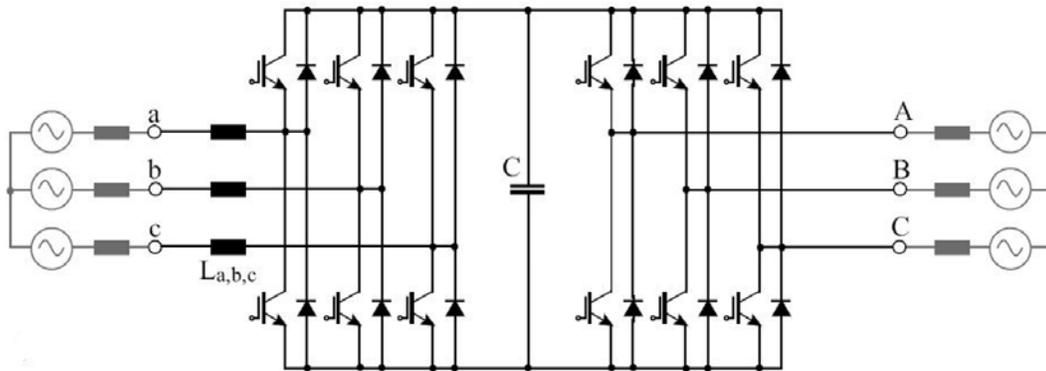
Figure 3: AC-AC Converter (image from: https://commons.wikimedia.org/wiki/File:Three_Phase_AC_AC_voltage_DC. jpg)

1.2 Power Electronic Components

As discussed in the previous section, power electronic converters are made up of similar components in different topologies. One of the components is the switch. To achieve the high switching frequencies that are desired in power electronics, solid state switches, or transistors, are used. There are many types of transistors including power metal-oxide semiconducting field effect transistors (MOSFET) and insulated gate bipolar transistors (IGBT). These transistors are vertically structured and designed to handle the significant currents that power electronic systems must provide. The work presented herein focuses on these solid state switches.

Another solid state component used in power electronic converters are diodes. In some instances, as in the DC-DC boost converter, the diode is essential to the working principle of the converter. In other instances, the function of the diodes is to prevent voltage spikes across the solid-state switches due to their parasitic inductance. Diodes typically used in power electronics are vertically structured like the transistors that are used. Specifically, Schottky and PIN diodes are used in these applications.

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Another component used in power electronic converters are capacitors. These capacitors serve a variety of purposes including the suppression of the ripple at the output of DC converters. For this purpose, electrolytic capacitors are typically used as they are able to achieve the large capacitance values necessary for this function. Another function that capacitors serve is electromagnetic interference (EMI) suppression at the output of AC converters. Electrolytic capacitors cannot be used in these applications as they are polar devices therefore thin film capacitors, which are nonpolar, are often selected to serve this function.

1.3 Operating Environment

Power electronics can be called upon to operate in a wide variety of environments. Some are harsh high temperature and high humidity environments such as under-the-hood applications in a car, some may be operated in outdoor environments. Due to the high currents causing joule heating and switching losses at high frequencies, power electronic systems can regularly experience temperatures in excess of 100ºC. 80% of respondents to an industry survey of power electronic converters said that their power converters are rated for over 1 kW, 12% of respondents use power converters rated for over 1 MW [2]. Even with aggressive cooling regimes such as liquid cooling maintaining the power components used in these converters at a low temperatures is a challenge. Additionally, due to varying operational loads, including planned downtimes, power electronics may experience significant swings in temperature. Over 85% of respondents to the earlier mentioned industry survey said that their power electronics can experience temperature swings in excess of 30ºC and

47% of respondents said the temperature swings for their application were in excess of 80ºC [2].

Due to the large thermal cycles observed in their life cycle profiles, thermomechanical stresses caused by mismatches in coefficients of thermal expansion of the different materials which make up power electronics packages are of significant concern in power electronics converters. In particular, the power switches which dissipate the most heat are of highest concern.

Many power electronics applications are operated in outdoor environments. Examples include automotive under-the-hood applications such as inverters in an electric vehicle, smart meters mounted on the outside of residences, wind turbines, and solar panels. In addition to uncontrolled environmental temperature, the humidity in outdoor environments are uncontrolled and can swing between high and low RH values or stay at high average values (e.g., above 80% in coastal Florida).

1.4 Power Semiconductors

In this thesis, power MOSFETs and IGBTs will be discussed in further detail. Together these two component types make up over two-thirds of power semiconductors which are used in power converters [2].

1.4.1 Power MOSFET

Power MOSFETs have the same operating principle as traditional MOSFET devices; however, these devices have a vertical structure, see Figure 4. This vertical structure allows them to block higher voltages than traditional MOSFETs by giving the devices a large drift region at the expense of increased on-state resistance. Figure 4

shows a single elementary cell; in a full device, thousands of these cells are connected in parallel, allowing the device to conduct currents up to 100 A [3]. Power MOSFETs have switching frequencies on the order of 1 MHz.
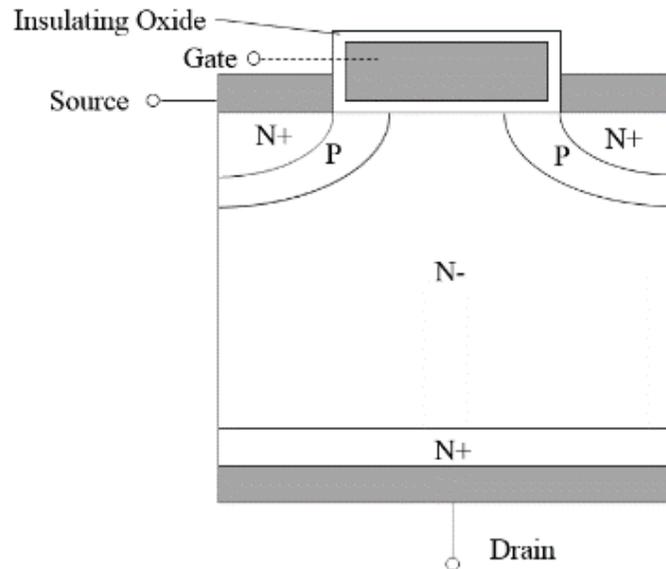
Figure 4: Elementary Cell of Power MOSFET

1.4.2 IGBT

Insulated gate bipolar transistors (IGBTs) are high-power switching devices that are found in many common medium- and high-power applications. These vertically structured semiconductors consist of an NPN-MOSFET driving the gate of a PNP bipolar junction transistor, see Figure 5. Similar to a power MOSFET, an IGBT is made up of many of these elementary cells connected in parallel [3]. By combining the switching characteristics of a MOSFET and the current-handling capabilities of a BJT, these devices reach fast switching speeds of 1–150 kHz and high collector/emitter current handling of up to 1500 A. They also are able to operate with high collector-emitter voltages of 600–6500 V. When compared with power MOSFETS, IGBTs have

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higher current and voltage ratings; however, they have lower switching speeds in the range of 10-100 kHz.
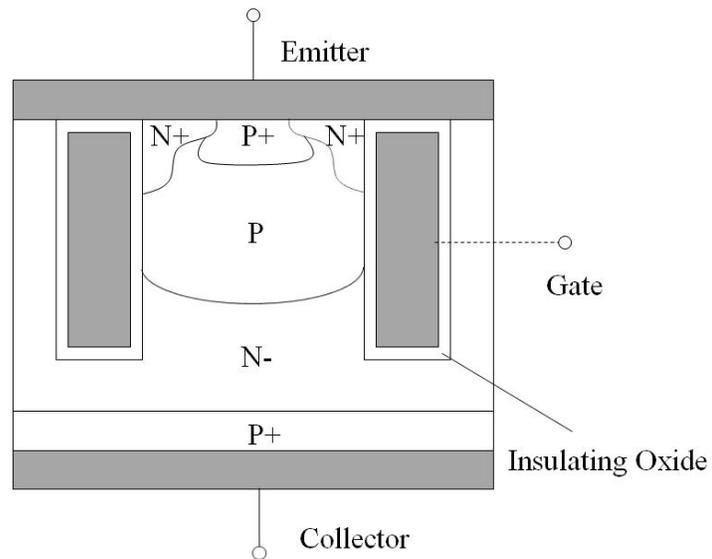
Figure 5: Elementary Cell of IGBT

1.5 Power Semiconductor Packaging

Electronics packaging serve four fundamental purposes: provide electrical interconnection, provide a path for thermal dissipation, protect the circuit from damage due to environmental exposure, and provide mechanical support for the circuit that facilitates handling and assembly. For power semiconductors, these are accomplished through two configurations: discrete components and modules. Press-packs are a third type of power package used; however, a discussion of the press-pack failure mechanisms is outside the scope of this work. An introduction to each type of packaging is given within this section.

1.5.1 Discrete Component Packaging

Discrete components are packaged individually and typically house a single semiconductor die. Functionally, they are a single switch with three leads: a controlling gate lead, and two leads which are connected in series with the circuit in which they switch. Transistors housed in discrete packages are typically rated for lower operating conditions than those used in module packages. One of the main advantages of these types of packages is that they come in a few well defined packages such as TO-220, see Figure 6, and TO-247 (Transistor Outline). They come in leaded or surface mount packages for connection to the printed circuit board (PCB). These packages are commodity items which are used as components in larger systems. Typical applications of these discrete components include appliances, high intensity discharge lighting, solar microinverters, and home appliance motors.
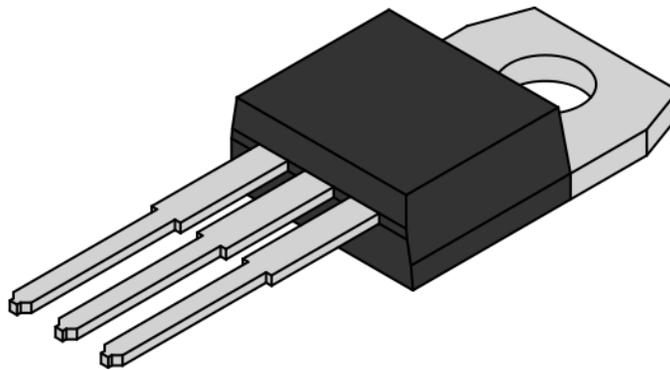
Figure 6: TO-220 Package

A cross section of a TO-220 part is shown in Figure 7 which will be necessary for understanding the stresses within the package in subsequent sections. Internal to the package, a semiconductor die, typically power MOSFET or IGBT, is soldered to a collector baseplate made of copper. Wirebonds, which connect the die to the leads, are typically made of aluminum for power packages; however, there is potential to change

to copper. Finally, the die and wirebonds are encapsulated in an epoxy molding compound to enable mechanical rigidity and protect the die from the environment.
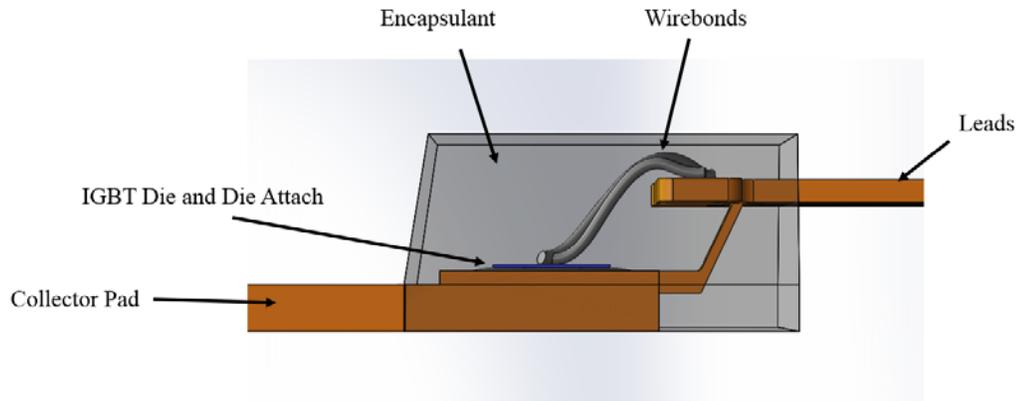
Figure 7: Cross-section of TO-220 package

1.5.2 Module Packaging

The second common form of power semiconductor packaging is modules, see Figure 8. These packages typically house many power semiconductors in a half or full bridge power converter configuration. These packages are typically designed to handle significantly higher electrical and thermal stresses than discrete packages. These modules can be purchased as commodity items but are specially designed to meet a customer's electrical and thermal needs. Module packaged power semiconductors are used in generators in wind turbines, traction control in electric trains, and electric vehicles.

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Figure 8: Power semiconductor module

A cross section of a typical power semiconductor module is shown in Figure 9. The semiconductor dies are soldered to a substrate metallization which is typically aluminum or copper. This metallization is on a ceramic substrate, typically alumina or aluminum nitride, which electrically insulates the semiconductor dies from the heat sink. Together the metallization and the substrate are referred to as Direct-Bond Copper or Aluminum (DBC or DBA) depending on the choice of metallization. This substrate is able to withstand significantly more thermal and electrical stress than would be expected for discrete components. The DBC/DBA is then attached to a larger baseplate or heat sink which is used to cool the semiconductors on the substrate. A silicone gel is used to encapsulate the package after it has been assembled. This has a higher breakdown strength than air and thus increases the insulated between wirebonds and the metallizations.
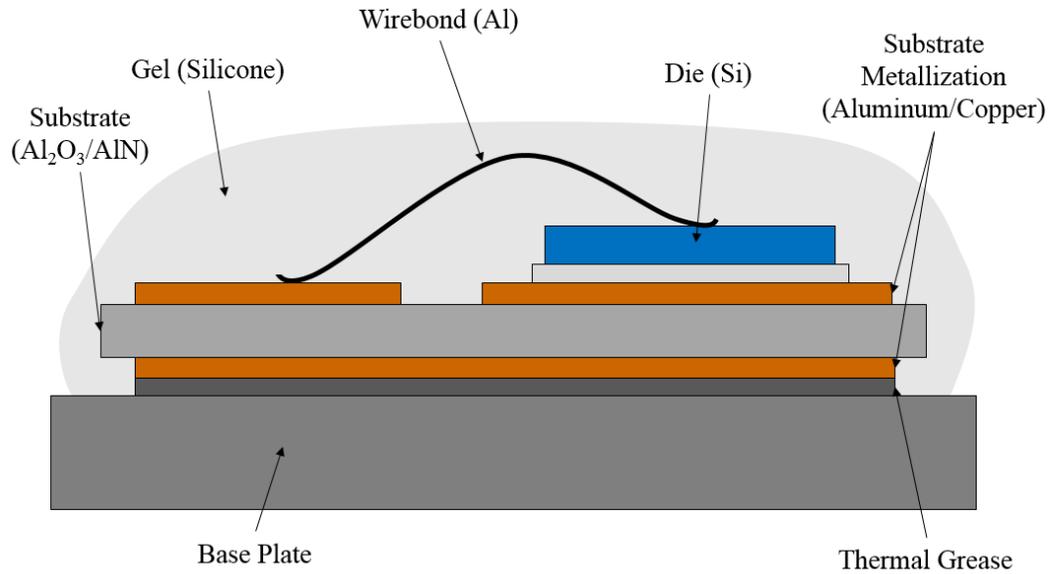
Figure 9: Schematic cross-section of typical power semiconductor module

1.6 Reliability Approach

Reliability is defined by Kapur and Pecht as "the ability of a product or system to perform as intended (i.e. without failure and within specified performance limits) for a specified time, in its life cycle conditions" [4]. To achieve a reliable product a variety of perspectives are taken by engineers including traditional statistical methods, test and field data based methods, and the physics of failure perspective.

This thesis takes the physics-of-failure (PoF) approach to reliability to better evaluate the failures in power electronic systems. The physic-of-failure method identifies all materials, geometries, environmental and operating conditions, and any other loads to determine the reliability of a system. In this perspective, failure mechanisms which are the physical, chemical, electrical processes which through which the failure occurs. These failure mechanisms ultimately cause the failure of the system and can be modelled when appropriate material, environmental and application

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environment information are available. Using these models, methods for improving reliability by can be identified and quantified.

1.7 Motivation

Yang et al. completed a survey of several different industries which use power electronic converters to identify reliability concerns. 31% of survey respondents identified "semiconductor power devices" as the most fragile components in their power converter systems, followed by capacitors [2]. Power semiconductors were defined as MOSFETs, PiN diodes, IGBTs, thyristors, integrated gate-commutated transistors (IGCT), and gate turn-off thyristors (GTO). Another survey of variable frequency power converters used in industry showed that approximately 38% of faults in surveyed systems were attributed to failure of the power converters [5]. A third survey showed that approximately 34% of power electronic system failures can be attributed to power devices [6].

Based on these surveys and failure analyses studies completed in this thesis, it is evident that there are significant reliability concerns pertaining to power converter systems and in particular, with the power semiconductor devices which are the foundation of these systems. A more complete understanding of their failures is essential to improve the reliability of these systems from both the perspective of a component manufacturer and a system integrator.

1.8 Thesis Structure

One method for identifying possible reliability concerns is called the failure modes, mechanisms, and effects analysis (FMMEA). To better understand failures of

power semiconductors, the framework for an FMMEA is established with a three pronged approach. First is the discussion and establishment of a list of relevant failure mechanisms and modes for power semiconductors to be discussed in Chapter 2: Failure Modes, Mechanisms and Effects Analysis for Power Semiconductors. Chapter 3: Failure Analysis Case Studies will further refine and verify the failure modes and mechanisms table identified in the previous chapter through the use of case studies of from real fielded systems. In Chapter 4: Failure Mechanism Criticality Analysis, a framework for identifying critical failure mechanisms of a system is identified. Finally, in Chapter 5: Contributions and Future Work, contributions of this work and avenues for future work are identified.

Chapter 2: Failure Modes, Mechanisms and Effects Analysis for Power Semiconductors

In this section an introduction of failure modes, mechanisms, and effects analysis is given. Following the introduction to FMMEA, a discussion of the failure mechanisms for power semiconductors is discussed. Finally, the failure modes and mechanisms will be tabulated as a baseline for creating an FMMEA.

2.1 Failure Mode, Mechanisms, and Effects Analysis

FMEA is a method for developing comprehensive lists of failure modes for a system and analyzing the effects of the failure mode to the larger system. FMECA expands upon FMEA by introducing a criticality metric through which the failure modes are ranked based on the severity, occurrence and detectability of each failure mode. The criticality analysis allows engineers to focus on these critical failure modes, identified by a risk priority number, to reduce the effects to the end user or system manufacturer.

These methods for identifying failure modes and were first established in the 1940s by the United States military. The US Department of Defense published and updated MIL-STD-1629A – Procedures for Performing Failure Mode, Effect, and Criticality Analysis [7]. The Society of Automotive Engineers (SAE) published ARP926 in the 1960s [8]. The electronics industry had used it but formally codified adopted the FMEA process when JEDEC Solid State Technology Association published of JEP131 in 2005 [9].

The JEP131 document defines FMEA as: "an anticipatory thought process designed to utilize as much knowledge and experience of an organization as possible toward the end of addressing potential issues defined in a new project. The objective is to reduce the probability that a customer is exposed to a potential product and or process problem by performing a thorough risk analysis," [9]. FMEA should be completed by a group of subject matter experts for the systems identified. In this thesis work, the JEP document is used as a primary source since it is particularly developed for semiconductor components. Several definitions related to failure are established in Table 1.

Table 1: Definitions related to FMEA, FMECA, FMMEA

Failure	A product no longer performs the intended function in an acceptable manner
Failure Mode	The way in which a failure is physically observed
Failure Site	The location of the failure
Failure Mechanism	The processes by which physical, electrical, chemical and mechanical conditions induce failure
Load	Application/environmental conditions (e.g., electrical, thermal, mechanical, chemical)
Stress	Intensity of the applied environmental load at the failure site

The development of an FMEA is as follows. First the system which is to be analyzed must be clearly defined. Then the system should be broken down into subsystems either in a functional, geographical/architectural, or combination of the two. In this step, all the functions of the subsystems should be identified. Next, identify all the possible failure modes that the subsystem can experience which may be done using a variety of techniques including testing, engineering judgement, and simulation.

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Then, for each mode, identify the possible causes of failure for each of the failure modes. Here, a life cycle profile for the product should be developed to help understand the various stresses the component may see not only during operation but also during manufacturing, storage, and transportation. Finally, identify how the failure effects the end user. Like the life cycle profile, this information is application specific. Once these steps have been taken the FMEA is completed.

A final step for FMEA and FMMEA is to attempt to prioritize the failure modes, mechanisms, and effects to allow for effective usage of resources to address reliability concerns. Here again, the analysis is highly application specific. Some guidelines for identifying critical mechanisms in a system are established in Chapter 4: Failure Mechanism Criticality Analysis.

As opposed to FMEA which identifies the high risk failure modes to update the design and reduce risks to acceptable levels, FMMEA takes the FMEA an additional step and identifies the failure mechanisms associated with failure causes and modes [10]. For failure mechanisms, relevant failure model(s) can be identified which can illustrate how the stress leads to the failure of a system. Failure mechanisms are highly dependent on the materials, geometries, and stresses within a system.

In the literature, only Patil et al. have published a FMMEA for silicon power devices, see Figure 10; however, this FMMEA is limited to only discrete IGBT parts, power cycled at high mean temperatures with large junction temperature swings [11]. The FMMEA was developed for the purposes of identifying failure precursor parameters for prognostics applications and it served that function well. Such an FMMEA is limited in several respects, first as will be discussed in failure mechanism

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criticality analysis, FMMEA requires application knowledge, therefore this is not truly an FMMEA and it makes no effort to account for failure mechanism criticality. Second, Patil et al.'s list does not include all relevant failure mechanisms for silicon power devices in the reasonably expected operating conditions.

Potential Failure Modes (Sites)	Potential Failure Causes	Potential Failure Mechanisms (Parameters affected)
Short circuit, loss of gate control, increased leakage current (Oxide)	High temperature, high electric field, overvoltage	Time dependent dielectric breakdown (V_{th}, g_m)
Loss of gate control, device burn-out (Silicon die)	High electric field, overvoltage, ionizing radiation	Latch-up ($V_{CE(ON)}$)
High leakage currents (Oxide, Oxide/Substrate Interface)	Overvoltage, high current densities	Hot electrons (V_{th}, g_m)
Open Circuit (Bond Wire)	High temperature, high current densities	Bond Wire Cracking, Lift Off ($V_{CE(ON)}$)
Open Circuit (Die Attach)	High temperature, high current densities	Voiding, Delamination of Die Attach ($V_{CE(ON)}$)

Figure 10: FMMEA developed by Patil et al. [11]

2.2 Power Semiconductor Failure Mechanisms

This section provides a description of relevant failure mechanisms that have been observed in silicon power devices and a table summarizing the failure modes, sites, causes, and mechanisms. Once a life cycle profile has been identified, a list of failure modes and mechanisms that may be precipitated from the stresses present in the life cycle profile must be established in an FMMEA. While there are many potential sources of thermal, mechanical, and electrical stresses on the power semiconductor components, the mechanisms which may be precipitated are dependent on the physical

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(i.e., geometry and material) characteristics of the power semiconductor component. This section provides an overview of the failure mechanisms which have been reported in power semiconductors. It is not intended to be a comprehensive listing of all the relevant literature on each possible failure mechanism; however, a basic description and several sources are identified for each of the mechanisms.

2.2.1 Aluminum Reconstruction

The die metallization for power semiconductors is typically aluminum. Additionally, if the substrate is DBA then there is aluminum metallized on the ceramic substrate. Due to thermal cycling of the component due to joule heating, switching losses, changes in the temperature of the environment, and the mismatch of thermal coefficients of expansion between the aluminum and silicon and ceramic substrate, thermo-mechanical stresses are generated within the package. These stresses can be significant enough to cause yielding of the aluminum metallization, causing it to buckle and form hillocks. This mechanism is referred to as aluminum reconstruction [12], [13], [14], [15], [16], [17], [18], [19]. The reconstruction of aluminum can increase in the resistance of the metallization layer. Aluminum reconstruction can be exacerbated by electromigration which can happen if significant current densities are present in the metallization. Aluminum metallization that is coated with a passivation layer, typically silicon nitride, has been shown to resist reconstruction; however, bond pads, which make up a significant portion of the total metallized area, are not passivated and therefore remain unprotected.

2.2.2 Wirebond Fatigue

Wirebond fatigue is also a thermo-mechanically driven failure mechanism. Due to the large diameter of wire used to handle high current densities in power devices, aluminum wirebonds must be wedge-bonded on both ends of the connection unlike gold or copper wirebonds which are typically used in low power applications with smaller wires that can be ball bonded. Fatigue of these wedge bonds occurs due to joule heating, switching losses, changes in the temperature of the environment, and the mismatch of thermal coefficients of expansion of the aluminum wire and the silicon die [12], [13], [14], [18], [19], [20], [21]. Wirebond fatigue manifests itself as either lift off or heel cracking. The heel of the wedge bond acts to as a stress concentrator and a crack propagates through the heel. In bondwire lift off, the wedge delaminates from the surface of the bond pad at the heel and toe sides of the wedge bond and propagates inward. Bond wire fatigue results in an increase in the on-state resistance of the power device and can lead to an open circuit.

2.2.3 Die Attach Fatigue and Delamination

Another location of thermo-mechanical stress due to CTE mismatch is the die attach which connects the die to the substrate. As the die is vertically conductive, the die attach must be conductive as it is part of the electrical path of the power semiconductor component. Similar to the aluminum metallization and wirebonds, the die attach is in intimate contact with the die and undergoes thermo-mechanical fatigue and possible delamination [14], [19], [20], [21], [22], [23]. Delamination occurs when the separation is between the die itself and the die attach material; however, fatigue can occur and propagate through the die attach. Figure 11 shows an IGBT die attach before

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power cycling and Figure 12 is the same die attach after failure. The IGBT shown was power cycled from 100ºC to 200ºC until failure and imaged using acoustic microscopy. Over time this degradation of the die attach results in increased on state resistance of the power semiconductor. Additionally, the delamination of the die attach increases the thermal resistance of the die attach, decreasing the ability of the die attach to dissipate heat generated at the die. Increased thermal resistance results in higher die temperature impacting the electrical characteristics of the device.
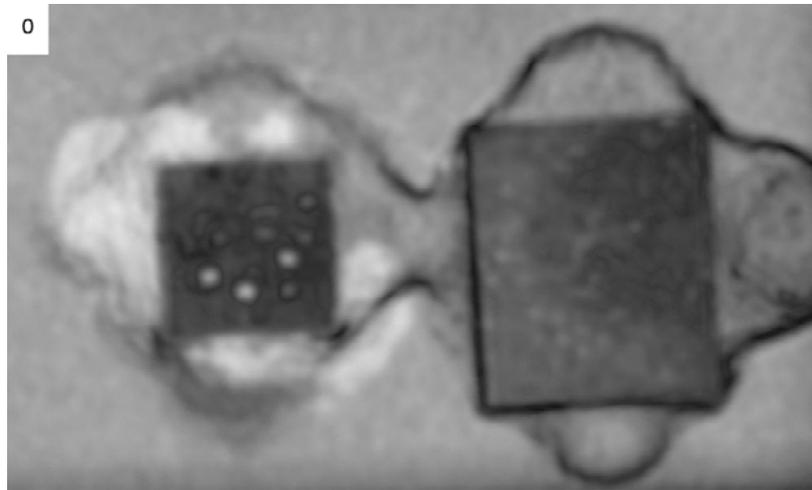
Figure 11: IGBT Die attach before power cycling
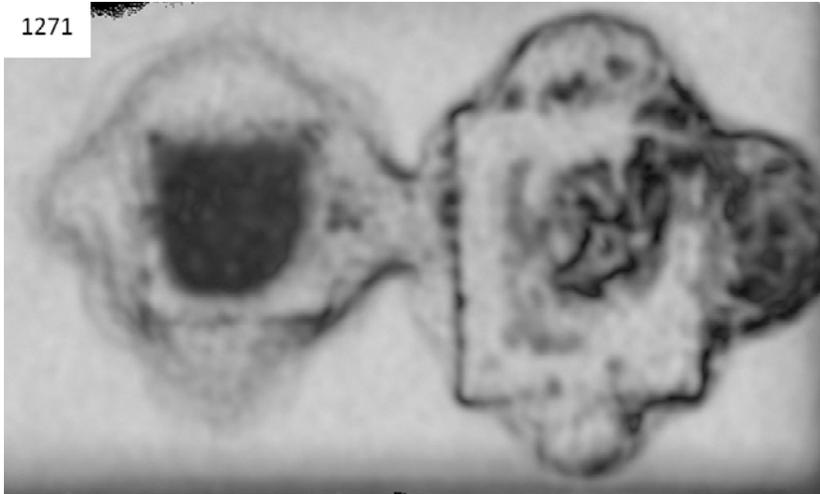
Figure 12: IGBT die attach after power cycling, the component survived 1271 power cycles

2.2.4 Substrate Cracking

The substrate itself is a possible location of failure within a power module. The ceramics in the DBC and DBA substrates can crack when subjected to thermo-mechanical cycling due to operational and environmental loading [24], [25]. The substrate acts to insulate the conductive paths of the power package from the heat sink or other cooling mechanisms. Therefore when cracking occurs, the insulation properties of the ceramic break down and a reduced insulation strength is observed. Depending on the electrical connection of the heat sink, this can create a significant leakage path within the power package.

2.2.5 Bondwire Melting

While the die is the most significant source of joule heating within the power package, the parasitic resistance of the wirebonds also acts as a heat source. The wirebonds are encapsulated in either silicone gel or an epoxy molding compound

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(EMC) depending on whether or not the package is a discrete or a module. Both silicone gel and EMC are poor conductors of heat. This means heat generated within the wirebonds is difficult to dissipate and the wire can see elevated temperatures. If the power package is used near or at its current rating and effective measures are not taken to cool the package, the wirebond can melt [26]. The result of this failure is an open circuit of the transistor.

2.2.6 Die Attach Voiding

Another failure mechanism related to the die attach is voiding of the die attach [27], [28], [29]. Small amounts of voiding are residual in the die attach from the manufacturing process. Power cycles grow and coalesce the smaller distributed voids which are initially present in the solder. Before and after X-ray images of an IGBT die attach, which was power cycled between 125°C and 175°C until failure, are shown in Figure 13 and Figure 14 respectively. Like die attach fatigue, die attach voiding results in an increase in the on-state resistance of the power package and increases the thermal resistance of the packaging, thus increases the junction temperature of the package.
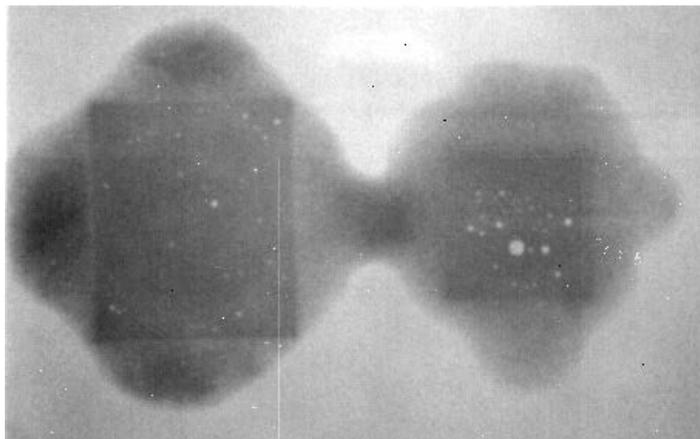
Figure 13: X-ray image of IGBT die before power cycling, residual voiding present from manufacturing process

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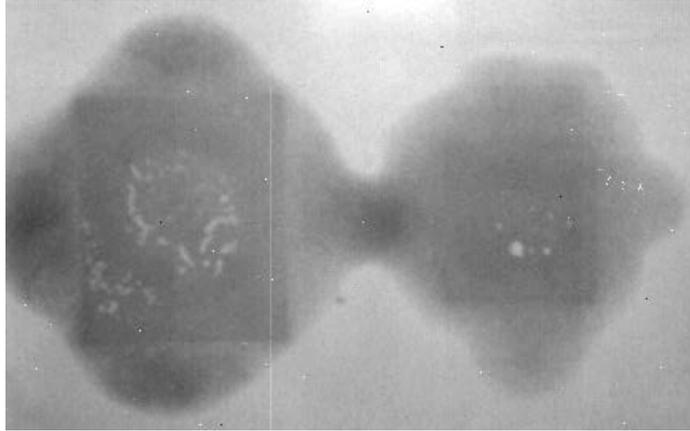
Figure 14: X-ray image of IGBT die after power cycling to failure

2.2.7 Aluminum Corrosion

When moisture is present within the package, corrosion of the aluminum wirebonds and bond pads can be of concern [30], [31]. In the presence of moisture, aluminum reacts to form $Al(OH)_3$ which passivates its surface and passivates the aluminum. This passivation layer can become soluble in the presence of contaminants such as halogens. During power cycling of a component, the encapsulant layer can delaminate from the base plate thus developing a path for moisture and contaminants to ingress into a component. Similar to the thermo-mechanical fatigue mechanisms, corrosion would cause an increase in the on-state resistance of the power semiconductor and is a wearout failure mechanism.

2.2.8 Latch-up

There are parasitic circuit elements associated with the power package as semiconductors and metals have non-ideal material properties associated with them. One particularly harmful parasitic element within power components are parasitic

thyristors. Thyristors are switches which only require a voltage or current pulse to turn on, unlike other switches such as MOSFETs or IGBTs which require a voltage on a gate be maintained for the switch to be in the on-state. Thyristors continue conducting after the removal of the gate voltage or current pulse until the electric potential between the anode and cathode is zero. Power semiconductor device have a parasitic thyristor incidentally built in.

Switches like MOSFETs and IGBTs are expected to conduct only when a gate voltage is applied, therefore the activation of the thyristor may cause the loss of gate control of the device. Such an event is referred to as latch-up and is observed as a short circuit between the conduction terminals [32], [33], [34], [35], [36]. The thyristor is activated when the current exceeds the so-called latching current of the device. In an IGBT, this overcurrent forces current into the base of the parasitic NPN transistor, see Figure 15, as the local high-current density in the P region at the base increases the resistance locally.
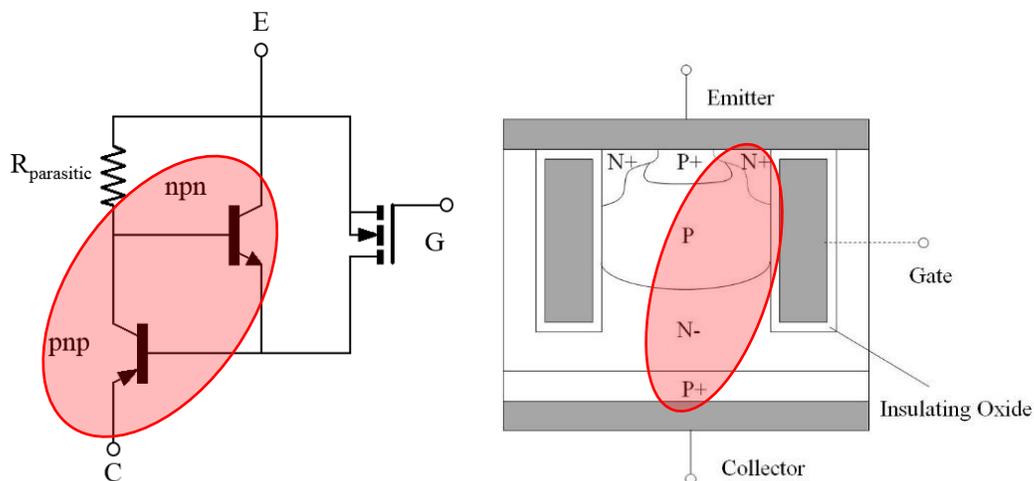
Figure 15: Parasitic thyristor within an IGBT

Latch-up of a device does not inherently cause a destructive failure of the component. In the unlikely event that the latch-up event is detected and measures are taken to remove the current from the device, the event can be stopped and the device will function normally. However, if the latch-up event is not identified, it can lead to a thermal runaway causing the device to burn-out. Latch-up is an overstress failure mechanism and is observed as a short circuit of the device.

2.2.9 Avalanche Breakdown

The avalanche breakdown [32], [35], [37], [38], [39] mechanism can precipitate, often during switching, when the drain-source or collector-emitter voltage exceeds the breakdown voltage of the power device. Electrons within the device gain sufficient energy to impact atoms within the device and ionize the atoms and releasing additional electrons. If these impacts continue, the device can "avalanche" as an increasing number of electrons are freed and able to impact atoms to free addition electrons. Avalanche breakdown often occurs during switching of a device when the inductance of the power semiconductor or the system within which it's operating, creates a voltage spike on the system. Avalanche breakdown manifests itself as a short circuit of the device and is considered an overstress mechanism.

2.2.10 Partial Discharge

The silicone gel that encapsulates the metallizations and wirebonds within power modules is used to increase the breakdown strength of these conductors. However, due to the high voltage and geometries of the conductors the electric field within the package can still be enhanced and cause a partial discharge within the

silicone gel [40], [41], [42], [43]. Over time, these discharge events can develop a carbonized, conductive path within the gel leading to increased leakage. Locally, partial discharge can cause bubbles in the gel to form due to the local heating events. Partial discharge within the gel is observed as increased leakage, developing towards a short circuit and is a wearout mechanism.

2.2.11 Electrochemical and Silver Migration

Often die attaches contain silver, as a sintered silver paste or a tin-silver alloy solder, which has a strong propensity to migrate under a variety of conditions [44], [45], [46], [47], [48]. In the presence of moisture, silver and other metals show some slight solubility. If an electric field is also present, the silver and other metals will migrate from the anode to the cathode through electrochemical migration. At the cathode, the silver will deposit and form dendritic structures back towards the anode. Given time, these dendrites can grow long enough to short the cathode and the anode. Mass transport of silver can also happen through corrosion, particularly in the presence of sulfur. Unlike electrochemical migration, in silver migration due to corrosion, there is no expectation of growth direction. Silver migration and electrochemical migration manifest themselves in an increased leakage current and are wearout failure mechanisms.

2.2.12 Dielectric Breakdown

It is essential that the insulated dielectric that forms the gate of voltage controlled devices maintains dielectric integrity for the device to operate. If the electric field through the gate exceeds the dielectric strength of the insulating material, then the

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terminals will short and permanent damage will be done to the gate [49]. For silicon devices, the gate is made of silicon dioxide. Dielectric breakdown can occur due to an overvoltage event on the die for a short period of time. One possible cause of this overvoltage is an electrostatic discharge (ESD). Such cases would be overstress events and likely result in a shorting of the gate to one of the conduction terminals.

2.2.13 Time Dependent Dielectric Breakdown

Dielectric breakdown can also occur over time through a process called time-dependent dielectric breakdown [50], [51], [52], [53]. One leading explanation for this mechanism is that Si-Si bonds within the dielectric are weak and over time the application of an electric field breaks down these bonds, creating locations within the dielectric through which electrons can jump to and travel through the insulating gate. Time dependent dielectric breakdown manifests itself as high gate leakage current and is a wearout mechanism.

2.2.14 Hot Carrier Injection

Some electrons may gain sufficient energy while travelling through the MOS channel to be able to tunnel through the gate oxide layer [54], [55], [56]. These electrons become "hot", referring to their individual speed, and as a consequence energy, as opposed to the bulk temperature of the device itself, as they travel along through the gate channel when the device is conducting. These electrons can cause impact ionization near the end of the channel which can produce electrons which can inject themselves into the gate dielectric. All these steps can cause damage at the interface of the silicon and silicon dioxide or allow the carriers to become trapped

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within the dielectric itself. Hot carrier injection (HCI) causes parameters associated with the gate such as the gate threshold voltage to shift. Under HCI damage, gate threshold voltage would drift higher, requiring higher gate voltage to be applied to achieve the same level of conduction in an otherwise healthy device. Hot carrier injection is reported to be more common at low temperatures, unlike most other mechanisms which are thermally accelerated. At lower temperatures, lattice scattering is reduced allowing longer free paths for electrons to accelerate, gaining energy to create hot carriers. HCI is a wearout mechanism.

2.2.15 Competing Failure Mechanisms

The failure mechanisms discussed in this chapter are not all independent of each other. In many cases one failure mechanism may lead the device to failure through another mechanism. For example, the degradation of the die attach can cause a latch-up event on the die. Power cycling through delamination and voiding causes both an increase in electrical and thermal resistance. This leads to an increase in the temperature of the die during operation as more power is dissipated due to the resistance increase and heat cannot leave the package as easily. Additionally, as portions of the die attach have "disconnected" from the die, current crowding occurs, leading portions of the device susceptible to latch up failure event though the device itself is still conducting the same amount of current. In such an instance, it is evident that one failure mechanism drove the device to failure through another mechanism. Due to the potential of failure mechanisms to convolute each other, it is important for engineers to understand such mutually accelerating factors when designing systems.

2.3 Power Semiconductor Failure Modes and Mechanisms (FMM)

In the previous section, a list of relevant failure mechanisms was developed for silicon power semiconductors. Such a list that we name FMM is the foundation of any FMMEA which may be developed for a component. This list, as well as information from the life cycle profile in the context of the application should be combined to establish an FMMEA. The failure mechanisms discussed previously are tabulated in Table 2.

Table 2 is organized to include the failure mode, location, causes, and mechanism. Systems integrators will find this information useful for identifying the failure causes and mechanisms that should be considered in the design of the system. For example, if they are aware that moisture will be present in the application, they should consider relevant measures to prevent ECM and silver migration. The corollary to this is that if they are confident that no significant moisture will be present then such measure may not be necessary in the design of the system.

Another possible application of this table is for failure analysis engineers. Based on the information that they establish during the failure analysis, this table can help lead the failure analysis team to identify the cause and mechanism associated with the failure. Once the cause has been identified, the proper steps can be taken to reduce the likelihood of future failures or identify risks for fielded systems.

Table 2: Failure Modes and Mechanisms of Silicon Power Devices

Location Designations – D = Die, P = Package
Mechanisms Classification – O = Overstress, W = Wearout

Potential Failure Mode	Potential Failure Location	Potential Failure Causes	Potential Failure Mechanisms
Short circuit	Collector-emitter path – (D)	Collector-emitter current above latching trigger current, high temperature, cosmic rays	Latch-up – (O)
		Collector-emitter voltage exceeds breakdown voltage, high-frequency switching, unclamped inductive switching	Avalanche breakdown – (O) Secondary breakdown – (O)
	Gate Oxide – (D)	Gate voltage exceeds breakdown voltage of gate	Electrical overstress (EOS) – (O) Electrostatic Discharge (ESD) – (O)
	Encapsulant – (P)	Electric field between bond wires exceeds dielectric strength of encapsulant	Partial Discharge – (O)
Increased collector-emitter leakage current	Periphery of die – (P)	Presence of moisture, high temperature, mobile ions, high electric field	Electrochemical migration (ECM) – (W)
		Presence of silver within package, moisture, high temperature, high electric field	Silver Migration – (W)
Reduction of dielectric strength	Insulating Substrate – (P)	Temperature and power cycling, CTE mismatch	Substrate Cracking – (W)

Potential Failure Mode	Potential Failure Location	Potential Failure Causes	Potential Failure Mechanisms
Increased gate leakage current and gate threshold voltage	Gate Oxide – (D)	Prolonged gate voltage application, high temperature	Time-dependent dielectric breakdown (TDDB) – (W)
		High MOS-channel currents, low temperature	Hot Carrier Injection (HCI) – (W)
On-state resistance increase (may develop into open circuit)	Bond wire – (P)	Temperature and power cycling, CTE mismatch	Bond wire cracking and lift off – (W)
		Presence of moisture and contaminants such as halogens	Aluminum corrosion – (W)
	Surface Metallization – (D and P)	Temperature and power cycling, CTE mismatch	Aluminum reconstruction – (W)
	Die attach – (P)	Temperature and power cycling, CTE mismatch	Voiding, delamination of die – (W)
Open circuit	Bond wire – (P)	High temperature due to power dissipation	Bond wire melting – (O)

Chapter 3: Failure Analysis Case Studies

The failure modes and mechanisms discussed in the previous section are part of the FMMA which is a "living" analysis. That is to say that all FMMA should be continually updated and confirmed with continued experience and additional expert judgement just as a FMEA or FMMEA would be. As part of that effort, five failure analysis case studies are presented in this section which were all used to confirm some of the failure modes and mechanisms shown in Table 2 in 2.3 Power Semiconductor Failure Modes and Mechanisms (FMM. Each case study describes the process of analytical and physical analysis of a failure from an industry application and the insights derived from the analysis.

3.1 Failure Analysis Preparation and Method

Failure analysis yields insights into what caused the devices to fail, whether there was a manufacturing defect that caused a latent failure or a design issue that caused the failure in nominal use conditions, and how to reduce and remove these defects to prevent future problems. Having a comprehensive FMMA document is useful in the process of developing failure analysis steps and drawing conclusions from the results. All failure analysis information gathered in an organization should be used as an input toward the FMMA for components of interest so that future decisions regarding the use of such components can benefit from such experience. For these failures, the failure modes and mechanisms list shown in Table 2.

The second step in the analysis is to compile information regarding the failure of the component within the power semiconductor package. Life cycle and operating

conditions such as storage temperature, operating temperatures, humidity levels, and electrical characteristics, should be noted. This information should be compared with the information in the FMMEA to determine critical failure mechanisms that may have caused the failure. The identified potential failure mechanisms will be the point of focus for the ensuing inspection of the device. Additionally, the date code, lot numbers, and any other traceability information of the failed components should be identified to determine if a specific lot is experiencing a higher incidence of failure relative to other lots. This information can also be useful in determining the possible level of exposure to operating conditions and time in the field. If one can identify such an anomalous lot, that lot should be set aside for analysis and comparison with non-anomalous, nominal lots.

The communication with customer or partner seeking failure analysis needs to establish the life cycle profile for the period up to the reports of failure. It is possible that, like the traceability information, the failures may be location and/or application dependent. A template of information collection should be used so that the life cycle covers all relevant phases of life cycle above and beyond just the operation and includes steps such as storage and testing. The collected information and documentation needs to be confirmed with the customer to ensure that the communication is correct including the failure mode(s) by which the failure was observed.

The potential failure mechanisms identified by the FMMA and operating and environmental conditions should be used to determine which analysis techniques should be used and in what order since the defects and conditions caused by various mechanisms are different. Non-destructive analysis of the parts should be completed

before a part is destructively analyzed. For example, if it is suspected that a power semiconductor device has issues with wire bonds, all available part groups should first undergo an optical inspection for any visual anomalies, then the relevant part groups should undergo an electrical characterization. All part groups should then undergo X-ray analysis for internal, non-destructive inspection. Once all non-destructive analysis steps have been taken, destructive steps may proceed. This may include decapsulation or mounting and cross-sectioning for more direct observation of the internals of the package. Such destructive steps may actually be performed on separate parts or a subset of the part groups.

In the failure analysis process, many companies find identifying the cause of failure is more critical than finding the exact failure mechanism. However, identifying a failure mechanism is useful in determining the cause and making design improvements. Once a failure mechanism is identified in a failure case, the FMMA table can be cross-referenced to identify likely causes. Additionally, by identifying the failure mechanism which led to the failure, one can identify a failure model which relates stresses to time or cycles to failure. This model can then be used to improve the reliability of the system by identifying how the stresses act on the system and taking steps to mitigate the effects of the stress.

3.2 Case 1: Appliance Motor Control Board – IGBT

The first case was an IGBT used in a three phase-ac home appliance motor control board that was experiencing a high early life failure rate. Due to the high incipient failure rate, it is likely that the associated failure mechanism for the IGBT is an overstress type; however, wearout mechanisms may have still occurred. For a typical

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washing machine's spin cycle, which is its most electrically intense cycle, the three-phase motor can be expected to operate in excess of 18,000 RPM, with the motor drawing approximately 650 W of power with phase voltages of up to 250 V [57]. The home appliance motor control board was sent to a failure analysis facility where the cause was determined to be an EOS event; however, no cause for the failure was presented. Additionally, significant voiding in the solder was noticed underneath the IGBTs. The home appliance manufacturer sent these results to the IGBT manufacturer who claimed there were no defects or problems with the IGBTs. CALCE was sent several fully assembled motor control boards in addition to several unmounted and unused IGBTs for a failure analysis. Specifically, the critical failure mechanisms identified by the FMMEA given the operating conditions are latch-up, avalanche breakdown, and secondary breakdown. The failure analysis will involve procedures that will attempt to verify these results, such as X-ray imagery for inspection of voiding in the assemblies as well as decapsulation for the inspection of the die surface for burn marks.

For the IGBTs on the motor control board, the most significant observation of the failure analysis was the consistent presence of the burn mark in the lower center of the active region of the IGBT die, Figure 16. There are several potential causes of the burn mark on the die, including a latch-up event or avalanching of the die.
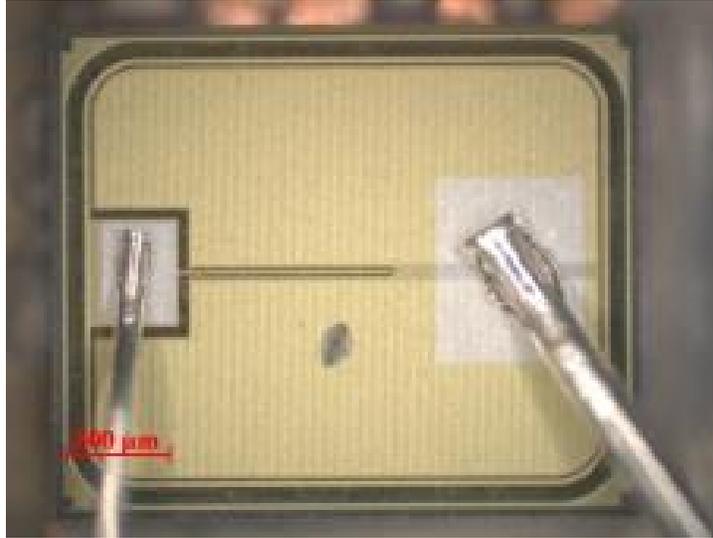
Figure 16: Burn mark in the center of the IGBT die.

In the case of latch-up, there is a parasitic thyristor doping structure within the IGBT that is activated due to overcurrent or temperature that causes the device to lose gate control [58], [59]. At a given temperature, a device has a threshold current for activation of the thyristor, which decreases with increasing temperature. When the parasitic thyristor is activated, the device will only stop conducting when the collector and emitter terminals switch polarity, i.e., the collector-emitter voltage is shorted to zero. Latch-up is not immediately destructive, but if the device is not turned off promptly it will lead to localized current crowding and consequently burning. Due to the decrease in the activation threshold current with increasing temperature, proper thermal management of the IGBT is key to preventing a latch-up event.

Avalanching events are another potential cause of localized burning, in which case the collector-emitter voltage terminals is raised above its rated value, causing the IGBT to break down [60], [61]. Avalanching may be caused by switching the device too fast or without a voltage clamp. The inductive nature of the external circuitry as well as the IGBT creates voltage spikes that cause the IGBT to avalanche. The stored

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inductive energy is ohmically dissipated through a localized circular burn on the die. Avalanching typically occurs at the spot on the die with the highest temperature due to the low resistance at this point. Generally, this is near wire bonds due to high currents around the wire bond but not under them because the wire bonds act as a heat sink on the die. Avalanche breakdown can be prevented using proper voltage clamps to prevent inductive voltage spikes from occurring across the collector-emitter voltage or by slowing the speed of switching, thus allowing the device more time to dissipate the electrical energy within.

The exact cause of the failure for the IGBTs on the motor control board was not determined; however, based on the significant voiding observed between the PCB and collector-base plate in the X-ray images, it is likely that the thermal management of the devices was insufficient. The motor control board manufacturer switched IGBT manufacturers and did not experience the same failures in their boards as with the previous IGBT manufacturer.

This failure analysis confirmed avalanche breakdown and latch-up events as mechanisms in the failure mode and mechanisms analysis. Additionally, the poor soldering which increased the thermal resistance of the die attach was identified as a cause of these mechanisms due to the elevated die temperature.

3.3 Case 2: AC/DC Power Supply Unit – Power MOSFET

Case 2 involves a power MOSFET used in as an active ORing device in an AC/DC power supply that outputs up to 1100 W at 56 V. The FMMA was cross-referenced to identify the most likely failure mechanisms for each power semiconductor in their respective operating environment. Active ORing FETs are used

in modern systems over conventional diodes due to their low on-state resistance values. These power MOSFETs can be expected to provide up to 24 A of continuous current and block voltages up to 100 V [62], [63].

The power MOSFET failed in short circuit and was thought to have been caused by a manufacturing defect related to a specific date code by the power supply's manufacturer, who alerted the power MOSFET manufacturer of the failures. An internal failure analysis was completed by the power MOSFET manufacturer, and it was determined the failure occurred due to an electrical overstress (EOS) event; however, the power MOSFET manufacturer did not accept responsibility for the failures. CALCE was sent several samples from both the suspect lot and non-suspect lots. Additionally, aged and unused samples from both lots were provided for testing. The failures of the power MOSFETs were not necessarily immediate; therefore, the failure mechanism could have been either wearout or overstress. The critical failure mechanisms are those associated with a short circuit failure, specifically, latch-up, avalanche breakdown, secondary breakdown, and time-dependent dielectric breakdown. In addition to generic failure analysis, the devices were tested for die surface anomalies by decapsulation and gate oxide quality through electrical characterization.

In the case of the power MOSFETs, the failure analysis yielded several key observations. First, the devices from the anomalous lot showed a 10% higher conductance than those from a nominal lot. To investigate this anomaly, modified avalanche breakdown tests and a C-V characterization were completed. The breakdown test did not yield discrepancies between the lots, suggesting that there are not

significant differences between the anomalous and nominal lots in regards to doping concentration. The difference in the C-V characteristics suggests that there may be differences in the quality of the gate oxides of the lots, which could produce the variations observed in the I-V behavior of the power MOSFETs.

Slight variations in the manufacturing process of the device can have significant impacts on the qualities of the oxides within a semiconductor device. One failure analysis showed that an N-channel power MOSFET used in an automotive application had an on-resistance drift caused by an excursion in the die fabrication process, which created an undesired nano-scale oxide layer between the silicon substrate and the source pad [64].

Another observation of the failure analysis was the presence of non-contact areas underneath the ball bonds of the wire bonds, see Figure 17. A failure analysis presented by Gore et al. showed that even this slight lift-off of the bond can cause electrical overstress of the device in operation [65].
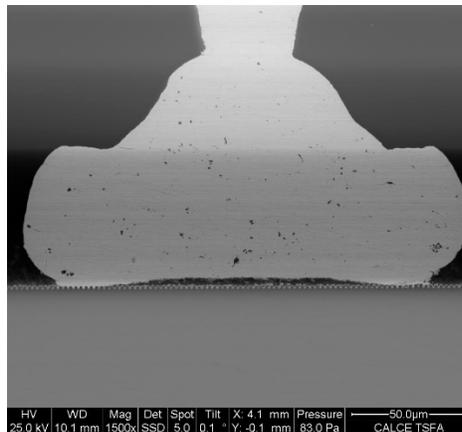
Figure 17: Source ball bond with incomplete contact area under the ball.

Variations between incoming lots can affect the end application even when the power semiconductors meet their manufacturers' specification. This variation in

conductance between power MOSFETs lots demonstrates a need to continually monitor incoming components. One way to achieve this is to create baseline data of known healthy power MOSFETs to include any non-destructive measureable features such as I-V and C-V characterization. The baseline data can then be compared to any incoming parts to identify any seemingly anomalous lots that are unfit for assembly.

3.4 Case 3: Transistor ESD – MOSFET

Case 3 involves a traditional MOSFET that was used on a medical device control board that failed unexpectedly before the product had even been released. It was reported that the MOSFET not functioning as expected. Given the environment and operating conditions of the MOSFET, it is not expected that thermal stresses played a role in the failure of this component. Similarly, given the short period of time that the MOSFET was operating, it was possible that some form of EOS event occurred and ESD was identified as the critical failure mechanism. To analyze the MOSFET for ESD, it was first inspected electrically to confirm the failure. Then the MOSFET was non-destructively using optical and X-ray analysis. Finally, the device was decapsulated to observe for any die-level indications on how the device failed.

ESD occurs when a charged object shorts to another uncharged object through contact or dielectric breakdown. During such events localized high currents and voltages can cause localized burn marks which can result in permanent damage. For example, a burn mark can create a permanent conductive path by carbonizing the encapsulant of the package of a component, or ESD can create an open circuit. In either case, the component will no longer behave as expected.

The electrical characterization of the MOSFET confirmed that the device had failed. The failed MOSFET showed a linear current response to applied voltage consistent with that of a 26 kΩ resistor, independent of the applied gate voltage. This result suggests that there is a conductive path within the package. This observation is consistent with that of an ESD event, and the failure analysis proceeded to optical and X-ray inspection.

In the event of ESD, it is unlikely that the MOSFET will show any abnormal characteristics in optical and X-ray analysis, such as visible burn marks on the outside of the package or damage to the lead frame. When compared with a separate healthy component, see Figure 18, no discrepancies were observed that could be attributed to the failure. Again, these results are consistent with an ESD event and the failure analysis proceeded with acid decapsulation to remove the encapsulant and observe the die.
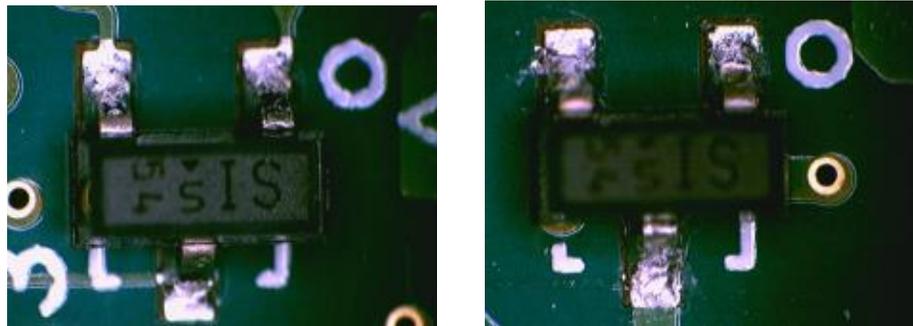
Figure 18: Healthy MOSFET (left), failed MOSFET (right).

Both the failed MOSFET and a separate healthy MOSFET were decapsulated to observe any abnormal die level behavior such as burn marks. The acid decapsulation used was fuming nitric acid warmed to 70 ºC, the results are shown in Figure 19. It is evident from the decapsulation that there are burn marks likely consisting of charred

epoxy on the failed die. Such a mark is consistent with an ESD event that caused localized breakdown of the epoxy, thereby carbonizing the epoxy and creating a conduction path between the drain and source of the transistor.
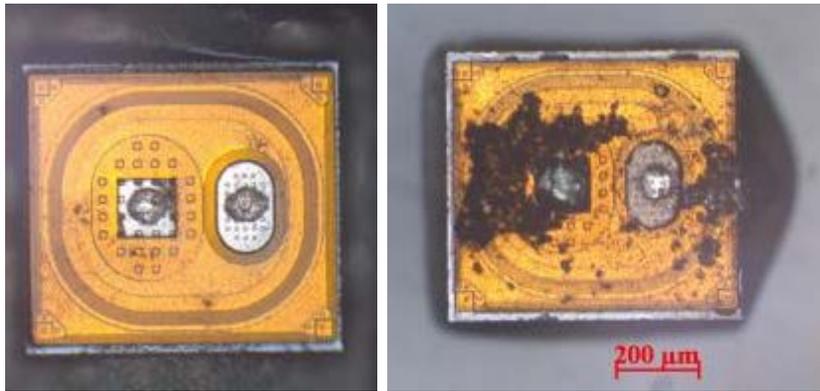
Figure 19: Decapsulated dies - healthy (left) and failed (right).

All of the findings of the failure analysis were consistent with an ESD event causing the failure of the MOSFET. It is not possible to definitively state that ESD caused the failure, however, those familiar with the board believe it was likely improperly handled in the laboratory during product testing and an ESD inadvertently may have been introduced to the board. Considering this priori with the evidence from the analysis, it is most likely that ESD was the cause of the board's failure.

This case study highlights the importance of proper handling of electronic components, particularly in laboratory environments, to prevent unanticipated failure. The case also illustrates the difficulty of finding an ESD failure in a component when assembled. There are no optically observable failure signatures on the component. Only in the electrical characteristic of the MOSFET was the failure evident, and then to identify the mechanism, the MOSFET had to be decapsulated.

This case study confirms the ESD mechanism on the failure modes and mechanisms analysis. It identifies ESD as an overstress mechanism.

3.5 Case 4: AC/DC Converter – Discrete IGBT

Case 4 involves the failure analysis of a three-phase IGBT bridge rectifier that failed in field operation. The bridge is composed of six discrete TO-247 IGBTs packaged within a larger plastic housing. The bridge is rated for 600 V and 80 A, therefore it is expected that significant thermal stresses could have been induced within the package during operation. The rectifier was reported to be experiencing short circuit events. The potential critical failure mechanisms were latch-up, avalanche breakdown, and secondary breakdown. As received, the bridge had experienced too much damage to be electrically characterized. Therefore, the analysis began with non-destructive optical and X-ray examination of the module.

The optical inspection of the bridge package showed that areas of the package have experienced high temperature exposure. Although the package was already black, there were visible signs of residue from a thermal event that occurred within the package, see Figure 20. The bridge rectifier was then X-rayed to observe for any anomalies within the package. The X-ray revealed that several leads of the discrete IGBTs had been destroyed in the failure event, see Figure 21. These observations all show a thermally driven failure event consistent with the critical mechanisms identified earlier. Following the non-destructive inspection of the package, the bridge rectifier was deprocessed.

Figure 20: Three-phase bridge rectifier (left), after removal of top plate (right). Both top views.
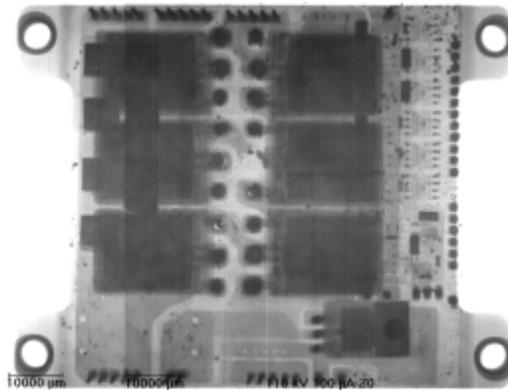
Figure 21: Top view X-ray image of bridge rectifier showing damaged leads on internal IGBT packages.

The removal of the top plate revealed significant charred residue throughout the package, further confirming a thermal failure event. To better observe the potential failure site, the package was cleaned with a Dynasolve solvent which removed both the charred material as well as the silicone gel, which was used to increase the voltage withstanding potential between the leads of the IGBT, see Figure 22. Following the cleaning, the baseplate was removed for observation of the discrete IGBT packages. Many of the IGBTs showed cracks in their encapsulants. The cracks were likely caused

by extreme heating during the failure event. In several extreme cases, the IGBTs showed wire bonds that had melted, see Figure 23.

Figure 22: Bridge rectifier after cleaning.

Figure 23: IGBT removed from bridge rectifier with melted wire bonds.

The melting of the wire bonds suggested significant heating of the bond wires due to high current. Locally, the aluminum wire bonds would have had to experience temperatures in excess of 660 ℃ in order for the aluminum to melt. This observation suggested that the device had overheated possibly due to the joule heating from the wirebonds. The next logical step in the failure analysis process was to review the ratings of the component for any discrepancies between use conditions and rated conditions.

The IGBTs used in the bridge rectifier are manufactured by International Rectifier and have a current rating of 85 A [66]. The datasheet specifies that the current

rating is limited by the packaging of the IGBT and not the die itself. Further investigation into current limited by the package led to International Rectifier Application Note 1140 [26] which states: "International Rectifier defines what can be called the 'ultimate current' for power packages on discrete products. This ultimate current represents the largest current any given package can withstand under the most forgiving of setups for heat management. The bench setup used in measuring the ultimate current at International Rectifier is full immersion of parts in a nucleated-boiling inert fluid." Nucleated-boiling in an inert fluid has a significantly higher heat flux than more traditional methods of conduction to a heat sink as was present in the module. This suggests that if the user of the IGBT is not using full immersion nucleated boiling, then the package must be adequately derated to reflect the decreased heat flux of the cooling system it is used in.

The IGBTs used within this module were encapsulated in a silicone gel, not immersed in a cooling fluid, thus the heat flux out of the package was reduced. The current rating for the module was 80 A, a derating of only 5 A from the IGBT's rating in full immersion cooling. This derating is inadequate in maintaining the component within its thermal rating.

The root cause failure mechanism was not determined in this failure analysis as it is possible that the thermal event was initiated by a short circuit mode but it is clear that the device failed due to a thermally related event likely due to inadequate derating of the IGBT components in the design phase of the bridge rectifier. This case illustrates the importance of understanding device ratings and the necessary derating that must occur to ensure reliable operation. This failure analysis case is an example of how

failure analysis can be used to identify design weaknesses and flaws. This case study identifies wirebond melting as a failure mechanism in the failure modes and mechanisms analysis.

3.6 Case 5: AC/DC Converter IGBT Module

Case 5 also involves a three-phase bridge rectifier like Case 4; however, the component to be analyzed was a fully integrated power module which used IGBT dies packaged on a direct-bond copper substrate instead of discrete IGBT packages. A short circuit failure occurred in the rectifier during an integration test of the module. As the failure was observed in an integration test, which is simply a first run of multiple subsystems together made by a system manufacturer, it was not expected that any fatigue-related mechanisms were involved in the failure. Additionally, it was not expected that during this test the thermal management was inadequate or thermal load was high, therefore the critical failure mechanisms identified for the module were those associated with electrical stress: latch-up, unclamped inductive switching, secondary breakdown, ESD, or EOS. Similar to the previous analyses, the failure analysis process began with non-destructive analysis including optical and X-ray imagery.

The optical imagery did not reveal any abnormalities on the module's outer packaging. Nothing was observed that would indicate thermal or mechanical stress events such as charring or indentation, see Figure 24. The X-ray imaging was difficult to interpret as the module contained several levels of populated printed circuit board (PCB) on top of the DBC substrate, see Figure 24. That being said, there appeared to be nothing that would indicate significant damage had occurred internally to the module.

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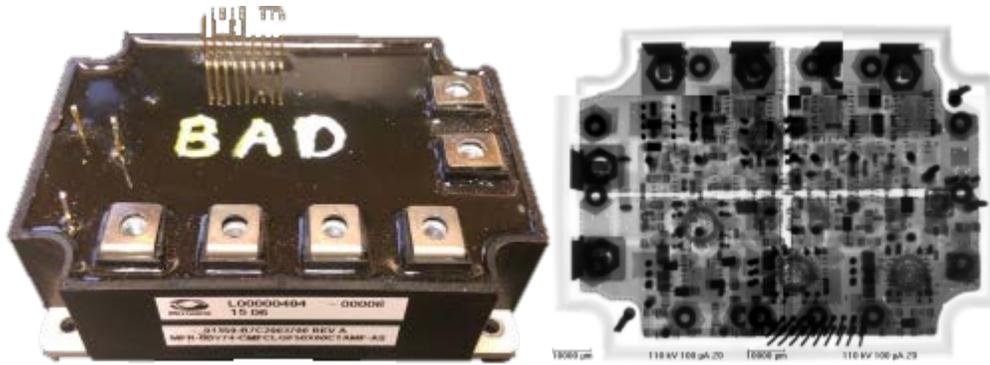
Figure 24: Failed three-phase bridge rectifier module (left), X-ray image of module (right).

A digital multimeter was used to probe each of the legs of the three-phase bridge. It was identified in this step that a short circuit occurred in one leg of the rectifier. It was not possible to determine if the failure occurred in the diode or the IGBT die within that leg; however, this portion of the electrical characterization significantly narrows the sites of interest during deprocessing of the module.

The next step of the analysis was to deprocess the module to directly observe the internal structure of the module. The module packaging included three separate encapsulants, see Figure 25. The outer layer was composed of an epoxy resin as a barrier against environmental hazards such as moisture and this layer was mechanically removed. The middle layer was a polyurethane resin that encapsulated the PCBs that were mounted above the DBC substrate. These PCBs contain logic devices used to control the three-phase bridge rectifier. These devices are not designed to withstand the high temperatures that are experienced within the power module and the power devices are capable of operating within, therefore, this polyurethane acts to prevent the PCBs from experiencing high-temperature excursions. This layer was removed using an industrial solvent from Dynasolve. The final type of encapsulant was a silicone gel that

was laid over the dies on the DBC. This gel acts to increase the breakdown voltage withstanding capabilities of adjacent wire bonds. This silicone encapsulant was removed using a different industrial solvent from Dynasolve. Figure 26 shows the deprocessed module.
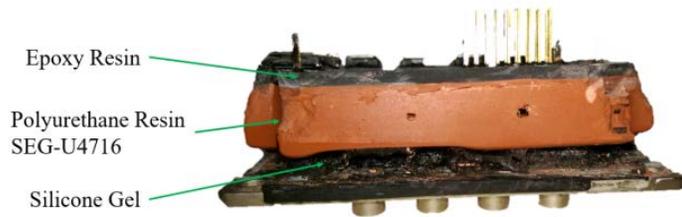
Figure 25: Bridge rectifier with side wall removed.
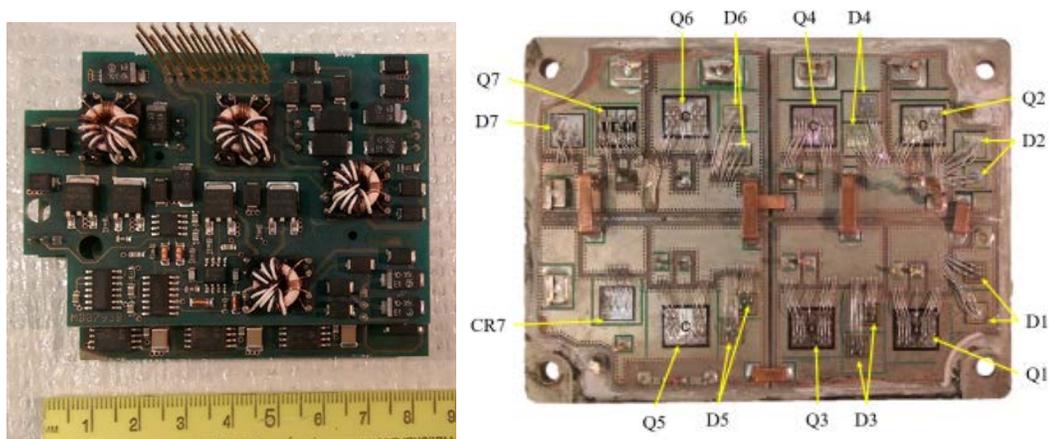
Figure 26: Decapsulated PCBs (left), decapsulated DBC (right).

Following the deprocessing of the module, additional optical inspection was conducted along with electrical characterization once the dies could be directly probed. Optical inspection did not reveal any abnormalities at this stage either. These observations are consistent with an EOS event or ESD. It is unlikely that latch-up or secondary breakdown occurred because failure mechanisms often involve a significant amount of dissipated energy on the die, which leaves a burn mark on the die.

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Subsequently, electrical characterization was completed on all of the dies. All of the IGBTs and diodes were functioning nominally except Q3, which appeared to have a short based on the I-V curves across the collector-emitter path.

After identifying the Q3 failure, additionally electrical characterization was completed to gain a better understanding of the failure site within the die. Each of the three terminal pairs were tested: collector-emitter, gate-collector, and gate-emitter. It was identified that the gate had shorted to the collector terminal. Such an observation suggests some type of EOS event caused a breakdown of the dielectric which insulates the gate from the collector and emitter, such as ESD or overvoltage.

The likely cause of failure was an overvoltage that occurred during the operation of the module during the integration test. One possible hypothesis is that when the legs of IGBTs are placed in parallel as in the bridge rectifier module, the voltages can oscillate, causing significant voltages to develop on the gate [18], [19]. It is possible that these oscillations exceeded the maximum voltage rating of the gates.

3.7 Remarks

By using an FMMA in the FA procedure a targeted process is developed which helps determine the root cause and failure mechanism. Each of these cases followed a failure analysis procedure guided by FMMEA. In each of the cases the FA process identified a design flaw or manufacturing defect and corrective action could be taken to prevent future failures.

The FA process first identifies the LCP and compares it against the elements such as failure causes in the general FMMA. The failure mechanisms that considered likely are identified based on this comparison and the necessary tools for investigation

and analysis are identified. The five cases presented in this thesis all illustrate the proper application of failure analysis to identify root cause failure mechanisms and failure sites for power electronic components and systems.

Chapter 4: Failure Mechanism Criticality Analysis

Both FMEA and FMMEA call for a criticality analysis to prioritize failure modes and mechanisms respectively. Such prioritization allows for efficient allocation of resources for enabling and improving reliability of a system. One difficulty for prioritizing failure mechanisms for component level FMMEA is that the information necessary to make the decision is highly application dependent. This chapter will describe the traditional method for defining and estimating criticality and establish component-level information based guidance for ranking failure mechanisms based on criticality.

4.1 Traditional Approach to Criticality

Through JEP131B, JEDEC outlines three components for critically ranking failure modes: severity, occurrence, and detection [9]. Each of the three categories is separately given a ranking from 1 to 10 based on the judgement of the team that is completing the analysis with 10 being the most severe, highest occurrence, and most difficult to detect respectively. These three metrics are then multiplied together create a risk priority number (RPN). Failure modes with higher RPNs are determined to be of more concern than those with lower RPNs. Corrective actions meant to be prioritized to lower the RPN of the highest failure modes. The RPN should be updated after corrective actions are taken and the design should be re-evaluated. As the rankings are based on the judgement of the team, RPN rankings should not be compared with another group's RPN ranking for the same or any other system.

The severity of a failure mode is dependent on the effects to the end user. First and foremost, severity should consider any potential to harm the users of a system. If there is potential to harm due to the effects from a certain mode (or mechanism), that mode (or mechanism) should be assigned a higher severity rating. The next considerations should include costs to the user and the system manufacturer. Costs take on a variety of forms but may include legal, warranty and returns, associated maintenance, and brand reputation. Based on the judgement of the team a severity ranking should be given which takes into consideration these factors. It is evident that the severity of the failure is application dependent. Component level severity will be discussed subsequently.

The occurrence of a failure mode is how likely it is to occur. Considerations for occurrence should include environmental and loading conditions as well as system materials, geometries, and part types. Using this information, it is possible to establish a probability of a mode or mechanism that can then be ranked according to the judgement of the FMEA development team. This information is also application dependent.

Finally, the detection metric for a failure mode is traditionally defined as the ability to detect a failure mode before shipping the product to the customer. Traditionally, in the electronics industry detection deals with the escape rate of any given test or screen. JEDEC suggests using inverse of the escape rate as one way of quantifying the detection of the mode. As the scope of the FMEA developed for a system level, individual power semiconductors are not assumed to be tested at the

system integration level. Therefore, a different approach to detection will be taken in the subsequent discussion.

4.2 Severity

Severity is determined by the effect to the end user. In the absence of this information, severity must be viewed in a different context. However, all silicon power devices will be used in a larger circuit and thus have other electrical components nearby. For the purposes of a component level prioritization, severity will be determined by the potential of the failure to be catastrophic and effect nearby components.

With respect to silicon power devices, overstress mechanisms which result in short circuit failure have the most potential to damage the system around them. Short circuits can create significant joule heating, which, if uncontrolled can damage nearby components and potentially start a fire thus increasing the associated costs of failure. Figure 22 depicts an example of a failure which caused damage to nearby components. The wearout mechanisms can be considered less severe because it is likely that only the silicon power device fails, not harming other nearby components, and the system can potentially be repaired or replaced.

4.3 Occurrence

Occurrence is dependent on the application operating and environmental conditions. Certain failure mechanisms can only be expected to occur when specific stressors are present. For example, electrochemical migration is not a concern in an application where humidity is below the threshold for initiation. To calculate a value

for an occurrence there are two approaches: one for wearout mechanisms and one for overstress mechanisms. For wearout mechanisms, one must identify a failure model which relates the stressors with the materials and geometries of the system, from this a time to failure or equivalent can occur giving an indication of the occurrence of the mechanism in the application. One example of this is the use of the Norris-Landzberg model for calculating fatigue of die attach (see Table 3 for more examples of failure models). Failure models express time-to-failure, or equivalent, as a function of the stresses action on a system. Overstress failures are given a high priority with respect to occurrence as the stresses which are reasonably expected in the life cycle profile should be designed against. Assuming the proper design precautions have been taken, overstress mechanisms are unlikely to occur in the field and can only be quantified by identifying a probability that an overstress condition could occur. For example, the probability that a lightning strike causes a burnout of a device due to overcurrent can be a "measure" of occurrence.

Table 3: Examples of failure models for failure mechanisms

Potential Failure Mechanisms	Model
Electrochemical migration (ECM)	Barton and Bockris Model [67]
Silver Migration	DiGiacomo Model [68]
Substrate Cracking	Paris' Law [69]
Time-dependent dielectric breakdown (TDDB)	E model [70]
Hot Carrier Injection (HCI)	N-channel model [71]
Bond wire cracking and lift off	Meyyappan-Hansen-McCluskey [72], Hu-Dasgupta-Pecht [73]
Aluminum corrosion	Peck [74]
Voiding, delamination of die	Coffin-Manson Model [75]- [76], Norris-Landzberg Model [77]

4.4 Detection

Detection in the traditional sense is determined by the ability to detect a failures, defects, and non-conformities before it leaves manufacturing or assembly. For a component level discussion, this traditional definition is not applicable. Therefore, detection will be considered as the ability to detect a failure in operation, before the failure occurs. For an expected loading profile, overstress mechanisms can be avoided through proper selection of parts and appropriate de-rating. However, overstress failures may still occur due to random and unpredictable loading excursions such as lightning strikes or crashes.

Not all mechanisms are unpredictable as accumulating damage changes some observable and measurable parameters. The ability to monitor and predict failure is a field of study referred to as prognostics and health management (PHM). In PHM, in-situ data is monitored and analyzed for purposes of anomaly detection, fault classification, and remaining useful life calculation. Wearout mechanism can be detectable and several groups have successfully implemented PHM for silicon power devices [11], [78], [79]. Certain wearout mechanisms are more detectable than other wearout and overstress mechanisms depending on the feasibility and correlation with damage of electrical parameters associated with the mechanism. PHM techniques and methods are developing rapidly and reducing in cost and ease of implementation; however, the development and implementation of a PHM framework is not yet trivial and therefore it may only be cost efficient for certain critical components and applications. Additionally, competing failure mechanisms may convolute the

measurement signals as they have the same or similar failure modes making it difficult to distinguish between the failure modes and take necessary corrective action.

4.5 Example: Microinverter

Given that all the components of criticality are application dependent, it is not prudent to make generic claims about the criticality of the failure mechanisms. To better illustrate the guidance described in the previous sections an example of component level guidance is given for a solar microinverter.

Microinverters are DC-AC inverters used for solar panels to converter the DC output of the solar panel into grid-level AC power, see Figure 27. They are called microinverters because each solar panel is paired with a single inverter which only carries the relatively small power load of the individual panel. This is different from more traditional string or central inverters where multiple solar panels are strung together in series and parallel and the combined output is inverted in a central location. When a solar microinverter fails, only a single panel is taken offline unlike the central or string inverters where failure shuts down the entire system.

Figure 27: Solar Microinverter

For the purposes of criticality discussion, a solar microinverter will be assumed to operate in a Florida-type environment. Florida environments experience relative humidity about 80% on most days of the year [80]. The implication of the humidity is that there is potential for significant moisture to be present in the life cycle profile of the power devices internal to the microinverter. Another concern for microinverters is that daily thermal cycles due to changes in the ambient temperature as well as loading due to operation lead are regularly 15°C [81]. These thermal cycles mean that concerns regarding thermal fatigue should be given more weight. One more consideration is that the relatively low power of a single microinverter means that only standard TO parts are used. Therefore, failure mechanisms related to modules need not be considered.

Given the previous considerations, the mechanisms that are of most concern with respect to this solar inverter application are electrochemical migration, silver migration due to the moisture from the humidity. Wirebond, chip metallization, and die attach degradation is also a concern given that the application has significant thermal cycling in the life cycle profile. Finally, module level mechanisms such as substrate cracking or partial discharge within the silicone insulating gel are not going to be present in a microinverter.

Chapter 5: Contributions and Future Work

The primary contribution of this work is the development of a failure modes and mechanisms analysis (FMMA) for silicon power devices. The combination of modes, mechanisms, causes, and sites resulting from this analysis covers reported and observed failures for silicon power devices. An FMMA in this level of detail and granularity did not exist in literature. The only prior work reported on failure modes and mechanisms analysis were reported in prognostics and health management articles and are limited to the type of loading used for their test condition. Similarly, failure analysis literature showed cause and effect diagrams limited to specific failure incidents without generalization. A literature review of the failure mechanisms is presented and used as the source material for establishing the FMMA. Several failure analysis case studies were used to illustrate failure mechanisms in the FMMA based on failure analysis of components and modules. This FMMA of silicon power devices can be used in conjunction with a life cycle profile to identify critical failure mechanisms of the power semiconductor for a given system.

An additional contribution is the establishment of failure mechanism criticality at a component level. As discussed in Chapter 4: Failure Mechanism Criticality Analysis, traditional criticality analysis is based on system level effects and occurrence. This work established component level information guidance for the critically discussion of failure mechanisms for a given component in a system. While the final decision regarding severity of a failure is dependent on the functions of a system and how it is configured (e.g., redundancy) the nature of failure at component level can inform such a decision. A failure, that is, loss of functionality of the part, caused by

one mechanism can be more destructive to the system than others affecting the severity. The occurrence of a failure mechanism is guided by the type of failure mechanism. Overstress failure mechanisms inform the criticality by establishing a probability of an overstress event (e.g., a lightning strike) o in the life cycle profile of the component. Wearout mechanisms inform the criticality using failure models, inputting stresses, materials, and geometries and outputting time or cycles to failure. Finally, the detectability of degradation before failure through the use of PHM techniques establishes a detectability ranking of the failure mechanisms which can be used to inform the criticality ranking. Amongst those failure mechanisms that can be monitored using PHM, some are more practical to monitor compared to others based on how well-established, economic, and practical such techniques may be. The size, weight, and cost budget of the system will impact the ability to implement such detection schemes. Thus based on the severity of a failure within a system, the occurrence of a failure mechanism for a given component, and the ability to detect a failure using techniques such as PHM, criticality can be identified for the mechanisms.

Future Work

The present work comprehensively analyzes silicon power device failure mechanisms; however, due to a variety of factors, other power semiconductor technologies are also in use and development. For example, due to the high-power dissipation of power electronics systems, the components which make up these systems experience high operating temperatures. Silicon power devices are limited to operation around 175°C before thermally generated carriers allows significant conduction of such devices even in the off-state. Wide-band gap (WBG) devices use different

semiconductor technology such as silicon carbide (SiC) and Gallium nitride (GaN) which have larger band gaps than silicon and thus can operate at higher temperatures without thermally generated carriers. These devices are processed and sometimes packaged differently compared to silicon devices. Future work can be to establish a similar FMMA for these WBG devices as the expected operating conditions and failure mechanisms are different from traditional silicon power devices.

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