Integrated transmitter circuit for multiport reconfigurable antenna

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ABSTRACT OF THE
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This master's thesis was a part of an academic research project[a] where the target is to design an integrated circuit (IC) to dynamically tune the operating frequency of a transmitter antenna. A multiport antenna model was provided by Prof. Viikari's group who recently presented a novel idea of multiport antenna tuning. In this concept the multiport antenna feeds are excited with weighted signals having certain amplitudes and phases, thus leading to antenna tuning at the desired operating frequency. However, it is not feasible to dynamically scale the antenna feeding signal amplitudes and phases with discrete electronics. Therefore, the system on chip solution (SoC) approach was studied in this thesis.

Initially, the concept was studied on theoretical level and with circuit simulations. The tuning analysis framework was developed to scrutinize the antenna weighted signal characteristics. This analysis provides the two most important specifications for the IC i.e., the accuracy required for on-chip amplitude and phase tuning. For the antenna under consideration, the on chip phase and amplitude tuning system have 6 bit and 3 bit scaling resolutions respectively. The tuning system is designed for a 4-port reconfigurable antenna where each antenna feed has a separate phase tuning and amplitude tuning block. The tuning system was simulated along the 4-port antenna at 2 GHz, and the simulation result validates the multiport tuning concept. This novel integrated tuning system is scalable as well as capable of tuning any reconfigurable multiport antenna.

[a] A collaboration of Electronic circuit design group with Prof. Ville Viikari's group at the department of Electronics and Nanoengineering.

Keywords: transmitter, integrated circuit, multiport antenna

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First of all, I am thankful to Almighty Allah for giving me strength and courage at each stage of my life. I wish to express my sincere gratitude to my supervisor Prof. Jussi Ryynänen and advisor Kari Stadius for their guidance and general support, as well as Prof. Ville Viikari and Jari-Matti Hanula for this amazing collaboration. In addition, I would especially like to thank Jerry Lemberg for teaching me to do things efficiently rather than working hard, and Faizan Ul Haq in learning the IC layout flow, in addition to their technical and moral help. The fruitful discussions with my other colleagues, and their suggestions were invaluable. Finally, I would like to thank my parents, siblings (Sana, Zahra, Shahbaz, Zainab), my finance Khadija, and nephews (Abdullah, Fareed), who not only supported me financially and morally but also inspired me to chase for higher ambitions in life.

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Ali Raza Saleem

Contents

Abbreviations

3G/4G/5G	Third/Fourth/Fifth generation wireless telecommunications
BB	Base band
CA	Carrier aggregation
CMOS	Complementary metal oxide semiconductor
CPU	Central Processing Unit
DAC	Digital to analog converter
DCDL	Digitally controlled delay line
DE	Delay element
DSP	Digital signal processing
DTC	Duty cycle
GPS	Global Positioning System
IC	Integrated circuit
INT	Interpolation
LNA	Low noise amplifier
LO	Local oscillator
LTE	Long term evolution
MPS	Miniaturization/Less Power/ High Speed
MCH	Memory Controller Hub
MUX	Multiplexer
PA	Power amplifier
PD	Propagation delay
PGEN	Phase generation
PIFA	Planar inverted-F antenna
RF	Radio frequency
SoC	Signal component separator
SoC	System on Chip
TARC	Total Active Reflection Coefficient
TDL	Tapped delay line
TX	Transmitter
UWB	Ultra wideband
WiMax	Worldwide Interoperability for Microwave Access
WiFi	Wireless Fidelity

Symbols

a	Incident wave
b	Reflected wave
d_r	Delay resolution
I_{PMOS}	PMOS transistor current
K	Open loop gain of amplifier
m	Amplitude tuning bits
M	Mutual coupling
n	Phase tuning bits
R_L	Load impedance
R_{on}	Transistor on resistance
S_{tran}	Transmitted signal
S_{11}	Input reflection coefficient
T_{in}	Input signal time period
T_{out}	Output signal time period
V_{drop}	LDO drop-out voltage
V_{ref}	LDO Reference voltage
V_{sup}	LDO supply voltage
V_{tune}	PA supply voltage
V_L	Load voltage
V_+	Amplifier non-inverting voltage
$Z_{out,PA}$	Output impedance of power amplifier
Z_o	Characteristic impedance

1 Introduction

As the era of 5G and IoT has already started,the significant improvements are going to take place in radio-frequency (RF) technology. According to RCRWireless survey [1], it is estimated that there will be almost 20–50 billion devices connected to the internet as per various tech giants. Since the demand of higher capacity, higher data-rates, miniaturization, lower power consumption and interoperability across a wide range of spectrum are obvious, the performance and complexity of existing RF front-ends have become challenging. In other words, new radio standards require support for multiple standards and its often desirable to have backward compatibility as well.

In a RF transceiver, the antenna must be properly matched to RF front-end through a matching block to have minimum reflection coefficient and maximum power transfer. To operate across multiple bands of spectrum, one of the existing solution to dynamically tune the frequency i.e., frequency reconfigurability are matching networks with tunable capacitors [2], [3] and switchable matching networks [4]. The increased number of matching blocks will affect certain constraints like power, volume and cost, thus are not considered a viable solution. Another possibility would be the antenna tuning via multifeed antenna transceiver architecture [5] where an optimum combination of amplitude and phase of antenna feeds can adjust the frequency characteristics. It is an empirical approach where one has to go through all possible combinations to see where the required minimum reflection coefficient is achievable and the antenna can transmit only at these frequencies. Moreover, one can only cover small number of frequencies.

Recently Prof. Viikari's research group from our department has proposed a new tuning method where a multiport antenna is used for frequency reconfigurability [6]. In contrast to previous approach, the feeding signal amplitude and phase can be determined theoretically through a well defined procedure for any arbitrary multiport antenna. Furthermore, the availability of wide range of frequencies with higher instantaneous broadband also compliment future transceivers.

The increased level of integration in CMOS processes to deep submicron scale have brought us to a point where the system-on-chip (SoC) solutions are preferable [7]. The purpose of my thesis is to design an integrated transmitter circuit which tunes the multiport antenna based on Prof. Viikari's tuning method. Since the on chip resources are finite and sufficient, the scaling of signal amplitude and phase is also finite. Therefore, one of the target is to determine the amplitude and phase resolutions. In other words, how much the antenna matching profile degrades if the antenna feeding signals are not properly weighted. This problem is solved through an analysis framework which evaluates the antenna tuning performance in the presence of variations in feeding signal amplitude and phase. This in turn gives insight about the desired amplitude and phase scaling resolutions, one of the most important specifications needed as these will dictate our system complexity. Fig. 1 shows simplified block diagram of the proposed system consisting of transmitter and the tuning blocks to scale the phase and amplitude of the feeds. Finally, the mapping of these constraints to an integrated circuit with minimum possible die area is desired.

In Chapter 2, the antenna tuning is reviewed to provide background for the frequency reconfigurability concept and the multiport antenna tuning method is also thoroughly discussed. Then, the tuning analysis is done in Chapter 3, and the circuit level design of the phase tuning block and the amplitude tuning block are presented in Chapter 4 along with the simulation results. Finally, the work is concluded in Chapter 5 with future directions.

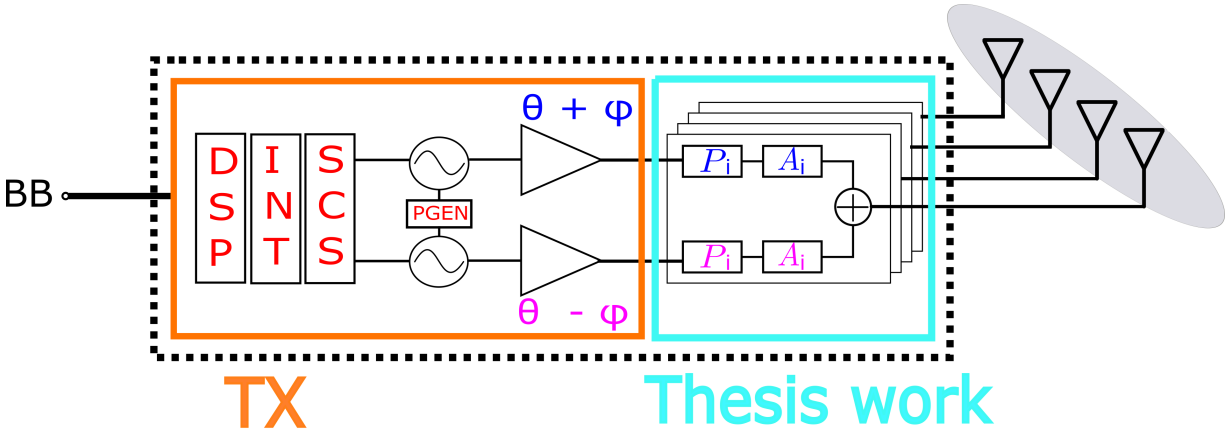


Figure 1: An integrated circuit consisting of a digital transmitter (TX) with different blocks used for digital signal processing (DSP), interpolation (INT) and signal component separation (SCS). It is followed by the outphasing architecture and the main outcome of the thesis work: the phase tuning (P_i) and the amplitude tuning (A_i) blocks designed to weight the antenna feeds in order to have tuning where $i = 1 \ldots 4$ represents the corresponding antenna feed.

2 Antenna Tuning Techniques

This chapter contains description of various antenna matching or tuning methods, and their pros and cons. Section 2.1 discusses the traditional single-port antenna tuning. This is followed by multiband antennas in Section 2.2 and the frequency reconfigurable antennas in Section 2.3, which are the existing solutions for frequency tuning. In Section 2.4, the antenna tuning via multiple feeds is presented and its limitations are considered. Lastly, the novel concept of frequency reconfigurability based on multiport antenna is thoroughly presented.

2.1 Antenna tuning

Antennas are the most important part of any radio communication to transmit/receive electromagnetic waves at a distance. Its evolution from simple Hertz dipole to fractal/metamaterials based antenna arrays [8],[9] is quite vivid. The antennas are designed to operate at specific frequencies requiring efficient power transfer between radio electronics and antenna. Since the antenna impedance is different at different frequencies leading to impedance mismatch at the antenna interface. The traditional way to tune the antenna is to have a matching block at the antenna interface that maximizes the power transfer from the power amplifier (PA) or low-noise amplifier (LNA) to antenna in an RF transceiver as shown in Fig. 2.

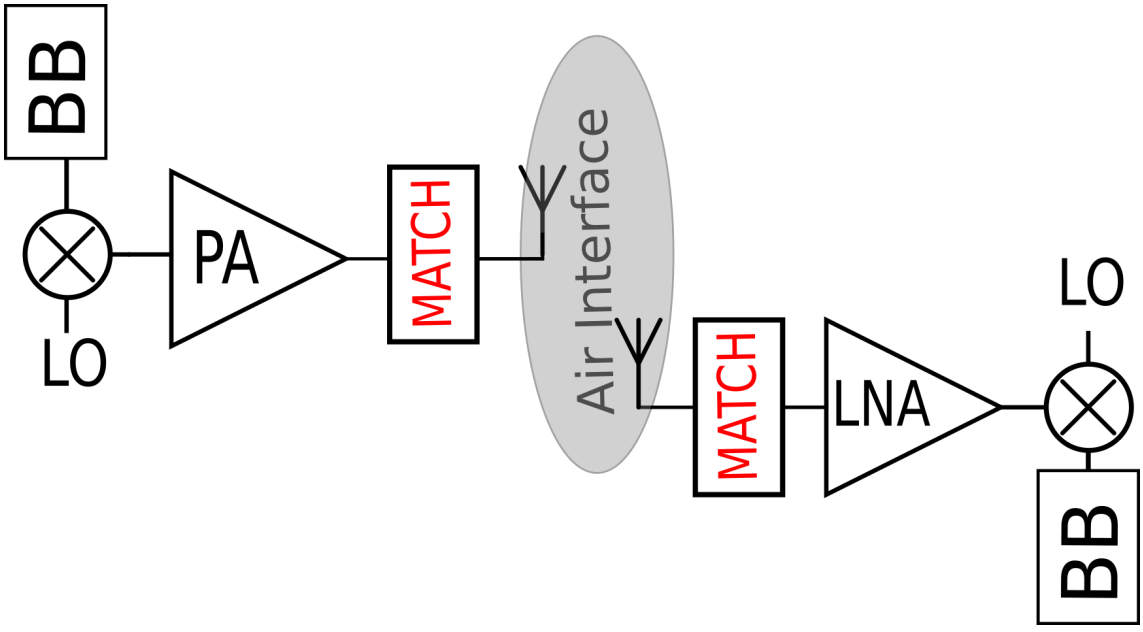


Figure 2: General RF transceiver block diagram

In the context of RF transmitter[1], the impedance mismatch is determined from the reflection coefficient seen at the antenna interface. Another parameter used

[1]The same holds for the RF receivers.

interchangeably to measure the impedance mismatch is voltage-standing wave ratio (VSWR). In addition, the matching condition is achieved over a bandwidth where the antenna can transmit efficiently. The typical way of impedance matching is to find a 2-port network e.g., the traditional L-section matching networks are the notable ones still being considered in celluar mobiles [10]. The objective of the matching network is to follow the tuning mantra "*minimum reflections/maximum power*" at the antenna interface.

Consider the front-end equivalent circuit of RF transmitter where $Z_{out,PA}$ is PA output impedance and the antenna structure is represented by load impedance (Z_{ant}) as shown in Fig. 3 and Fig. 4. The matching section tune the antenna by making $Z_{out,PA}$ equal to the characteristic impedance (Z_o) of transmission line. These simple topologies are used to achieve narrow band and wide band tuning respectively. The important parameters such as reflection coefficient and power delivered to the antenna are illustrated in Fig. 6 and Fig. 7.

It is clear that the number of passive components affect the tuning conditions and critical parameters. However, the addition of more passive components (or blocks) deteriorate the volume and power constraint. The need of several services within a limited band of interest require multiple switchable matching sections along with filtering as shown in Fig. 5. Depending on type of matching (narrow or wideband), the matching sections ($L1, L2, \ldots, Ln$) can be designed. To operate across multiple bands, a better wide band performance can be achieved by increasing the number of antennas. Though this configuration makes the frontend simple but the cost, volume and power consumption are the limiting factors leading to shorter battery life. As far as matching is concerned, the return loss (Γ_{ant}) and voltage standing wave ratio (VSWR) are defined as followed:

$$\Gamma_{ant} = -20 \times log|S_{ant}| \tag{1}$$

$$VSWR = \frac{1 + \Gamma_{ant}}{1 - \Gamma_{ant}} \tag{2}$$

where the reflection coefficient (S_{ant}) is

$$S_{ant} = \frac{b}{a} = \frac{Z_{ant} - Z_o}{Z_{ant} + Z_o} \tag{3}$$

The power delivered to the antenna load in terms of incident (a) and reflected (b) power waves is given by the following:

$$P_{del} = \frac{1}{2}\left(|a|^2 - |b|^2\right) \tag{4}$$

where "a" and "b" are

$$a = \frac{V + Z_o I}{2\sqrt{2Z_o}} \tag{5}$$

$$b = \frac{V - Z_o I}{2\sqrt{2Z_o}} \tag{6}$$

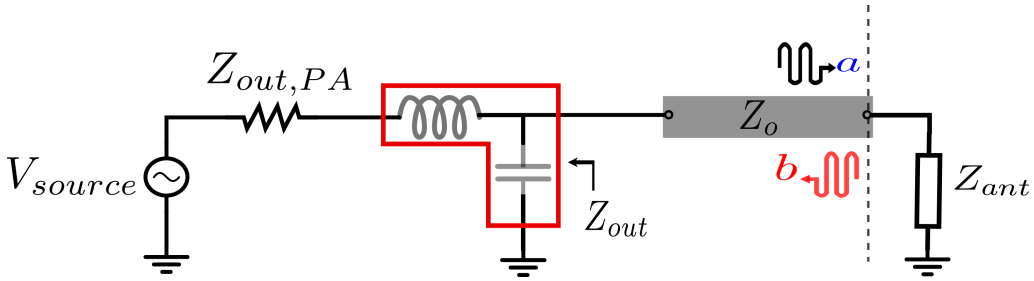


Figure 3: L2-section for narrowband matching

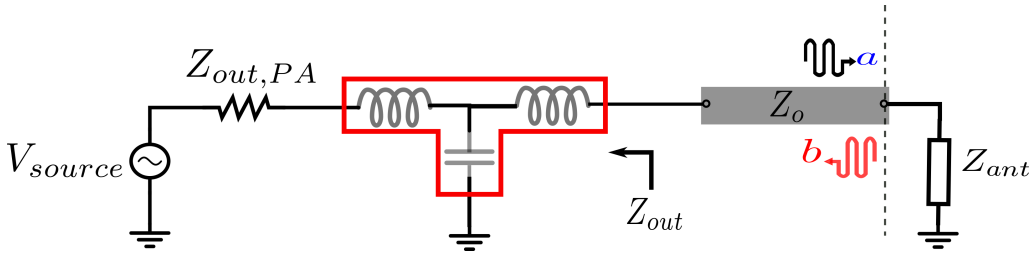


Figure 4: L3-section for wideband matching

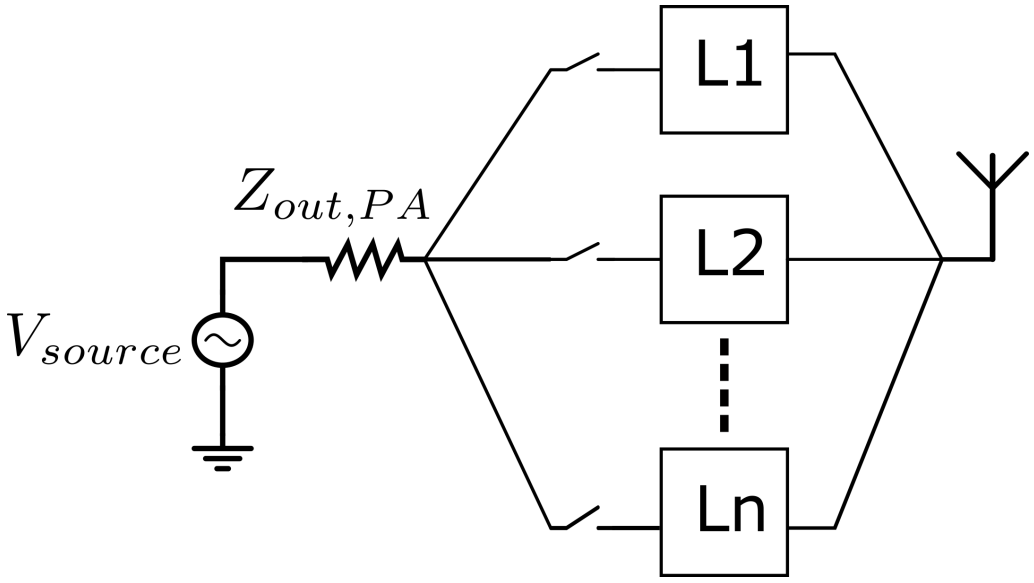


Figure 5: Switchable matching sections

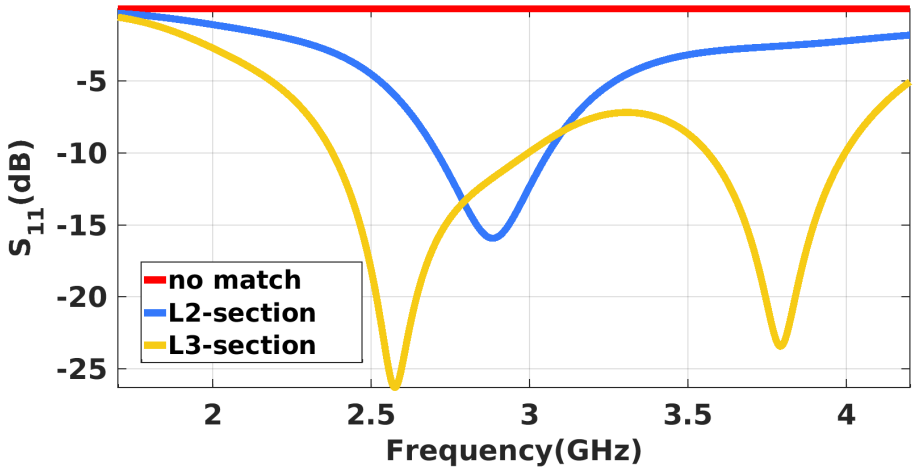


Figure 6: Return Loss profile of L2 and L3 matching sections

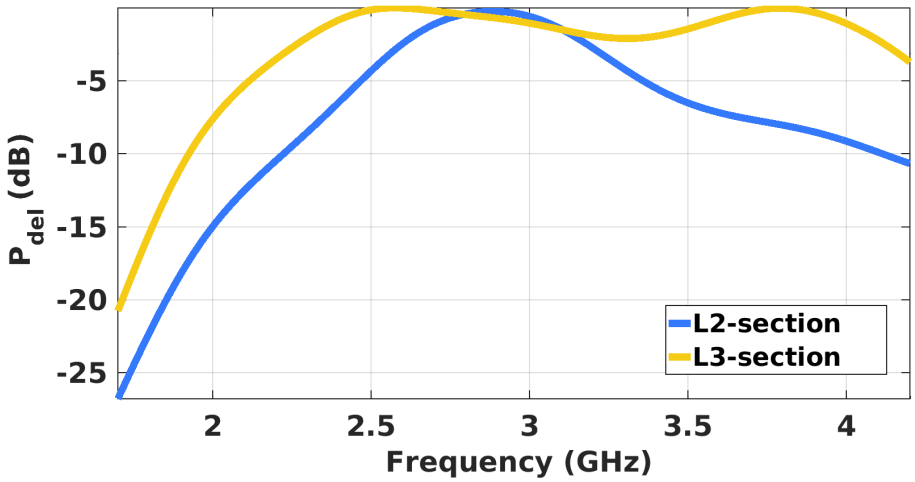
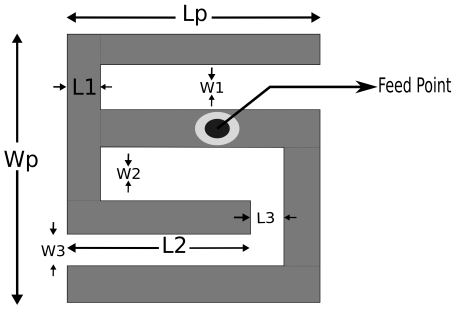


Figure 7: Relative power profile for the L2 and L3 matching sections

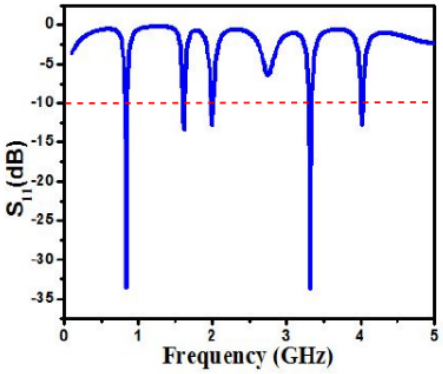
2.2 Multiband Antenna

The multiband antennas consist of multiple antenna sections each having particular dimensions for a certain band. It support and integrate various standards into a single mobile device as shown in Fig. 8. These antennas also provide inter-band features such as the carrier aggregation (CA) in advanced long term evolution (LTE) to enhance link data rates and implicit data security[11]. The specific dimensions of the antenna sections play their role in achieving multiband capability. Now, the planar multiband antennas are currently the choice for mobile terminals [12],[13]. As

the new standards are being introduced, the new services along with demands of diversity and MIMO are provided at the cost of more antenna modules in limited space. Therefore, the need of multiradio in a limited space will result into poor isolation and degraded performance. The performance issues of bandwidth and efficiency are mainly the consequence of smaller form factor [14]. This put stringent requirement of filtering on the frontend making it bulky and power hungery.



(a) EC-shaped multiband patch antenna



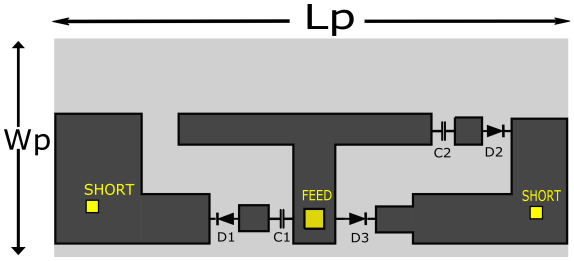
(b) S_{11} (dB) or Return loss

Figure 8: A Compact EC-shaped multiband patch antenna supporting multiple bands [15]

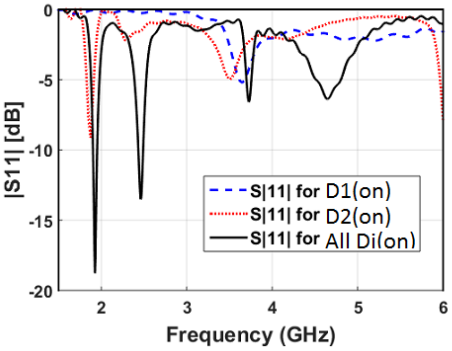
2.3 Reconfigurable Antennas

The frequency reconfigurable antennas have been considered better candidates instead of the multiband antennas in terms of isolation and performance. These antennas consist of multiple sections being turned on/off with dc-bias switches to achieve reconfigurability over a finite set of frequencies. The switches may consist of RF MEMS [16], varactor PIN diodes [17], and optical switches [18] as well. For instance, a planar inverted-F antenna (PIFA) [19] has been tuned to six different bands using PIN diodes as shown in Fig. 9. Regarding multi-band tuning issue, this approach is providing reasonable tuning and relaxed filter requirements making it resilient to out-of-band noise.

The current mobile terminal contains approximately 8 radios. Moreover, the number of antennas per band (or service) and control modules will soar depending upon the data rates and reliability needed as shown in Fig. 10. It is clear that there are two main challenges in this method. Firstly, the large number of switches are required for fine-grain frequency tuning and also they have to be integrated on the limited space which is not as trivial as it seems. Secondly, the switch selection (either PIN diodes or RF MEMS) will dictate the overall cost, power and critical performance parameters [20].



(a) A planar inverted-F antenna (PIFA)



(b) S_{11} (dB) or Return loss

Figure 9: Tunable PIFA structure supporting GSM1800/WCDMA/m-WiMax/WLAN [19]

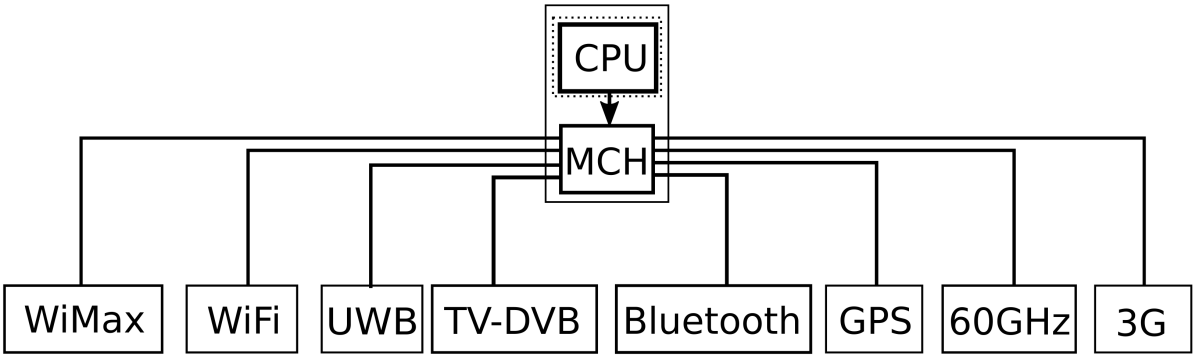


Figure 10: A mobile platform comprising multiradio standards [20]

2.4 Multi-Feed antenna technique

An alternative to existing frequency reconfigurable techniques where an antenna with two feeds is used for tuning purpose. The concept is centered around particular excitation where the feeding signal amplitudes and phases adjust the antenna frequency response [5]. The important parts of the multifeed system are signal splitter, measurement and control blocks presented in Fig. 11.

The signal to be transmitted (S_{trans}) is split into multiple signals $[S_1, S_2, ..., S_n]$ with the particular amplitude and phase difference among them. The amplitude and phases are scaled with either vector modulators $[V1, V2, \ldots, Vn]$ or attenuator and phase shifters. To have reconfigurability, these scaled signals $[S'_1, S'_2, \ldots, S'_n]$ where $S'_i = S_i\,(A_i, \Phi_i)$ excite the multifeed antenna configuration and the antenna is tuned to the desired frequency. The robustness of design is clear from the measurement and control block providing dynamic tuning. The measurement block may periodically sense the actual transmitted signal (S_{meas}) and the control block will run an iterative

algorithm that varies the amplitudes and phases until the measurement element detects the desired frequency of transmission. Though the goal of tunability has been achieved, however, there is no proper procedure reported to determine the proper feed signals amplitude/phase in order to have tunability. In addition, it requires consistent measurements to have signal scalings required for antenna tuning.

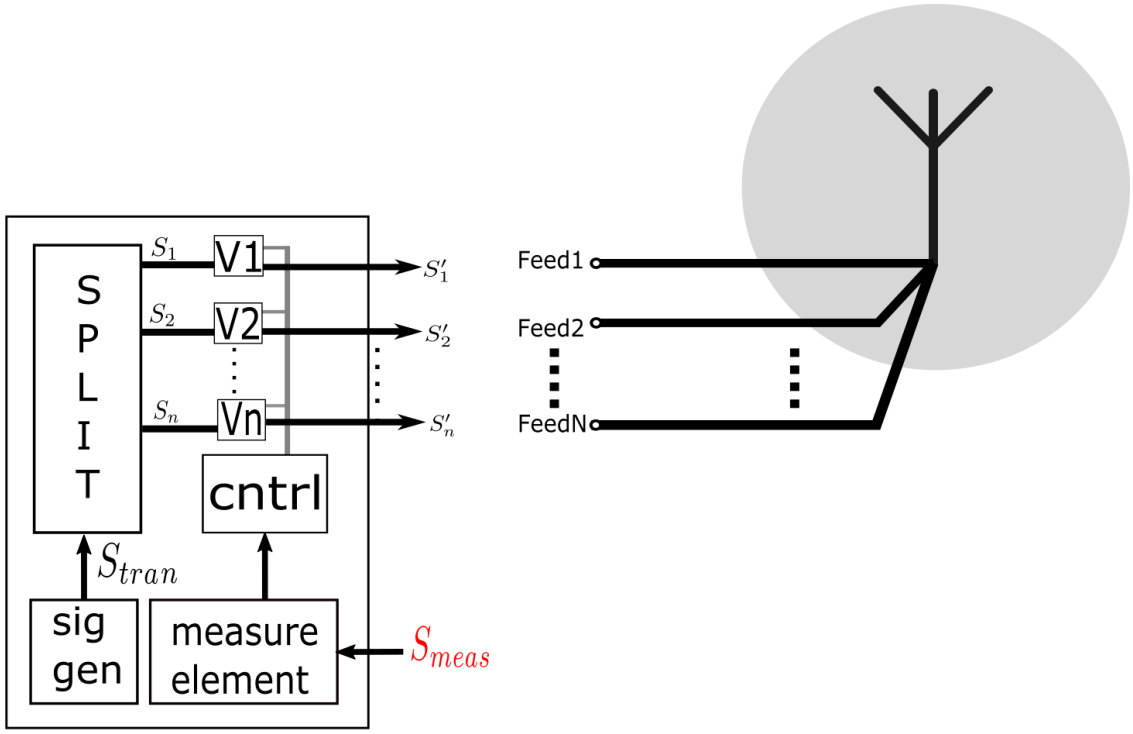


Figure 11: A Multi-feed antenna configuration

2.5 Multiport Antenna Approach

The thirst of fine grain frequency tuning over several frequency bands have led us to the multi-antenna systems which are designed around the crucial need of higher capacity, more bandwidth and reliability. The use of multiple antennas will enhance the wideband performance, and the target is to achieve maximum efficiency at all ports. In addition, the antennas are in close proximity where the mutual coupling will alter the port impedances making the tuning challenge non-trivial [21]. It seems to require a bulky hypothetical multiport matching network whose port impedances have to be varied in order to achieve our tuning objective at the cost of degrading antenna efficiency which is highly undesirable.

Recently Prof. Viikari's research group from our department has proposed a new tuning method where a multiport antenna is used for frequency reconfigurability [6]. This novel concept is presented for frequency reconfigurable antennas where the several antenna elements along with coherent transmitters[2] are used as a whole

[2]The same discussion hold for receiver side tuning as well.

to achieve wide tuning range. In comparison to *port decoupling* [22], the beauty of this technique lies in the mutual coupling which have been utilized for tuning purpose rather than canceling it as shown in Fig. 12. The signal to be transmitted is weighted differently with certain amplitudes and phases at the antenna ports. The combination of these weighted signals will result into coupled waves which will interact destructively with the reflected waves corresponding to the impedance mismatches at the ports, thus minimizing the reflections and maximizing the power delivered to the antenna. These optimal signals are determined from the antenna scattering parameters with the proposed mathematical procedure.

The optimal signal excitations have already been used in digital beamforming applications e.g., the beam steering and polarization adjustment [23]. With difference to these applications, this new method adjust the frequency characteristics of the antenna array. With regard to the multifeed approach, it uses multiple antennas instead of one and it also has signal weight calculation framework to determine weighted excitations resulting into efficient operation at a particular frequency we are interested to operate our antenna.

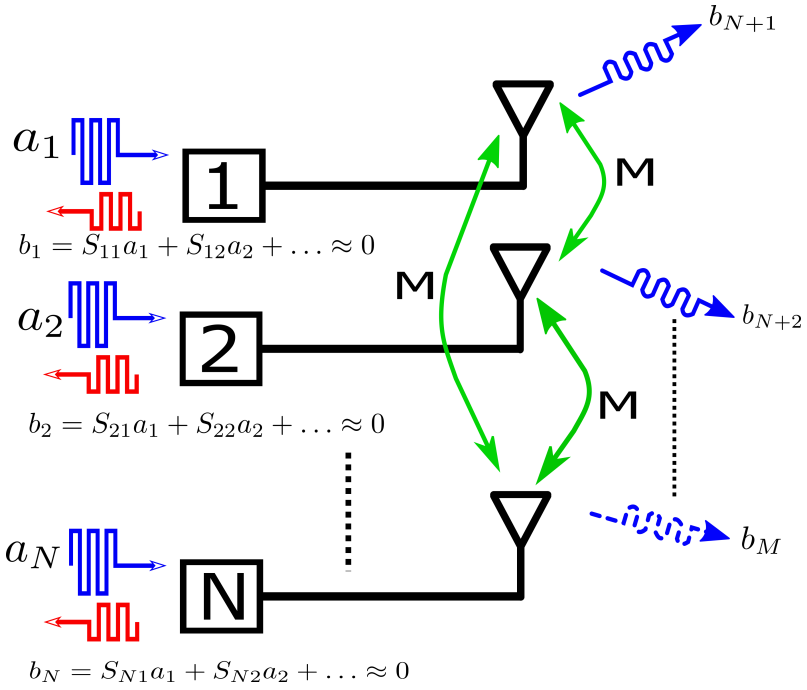


Figure 12: Multiport antenna with optimal excitations $(a_1, a_2 \ldots a_N)$ affect mutual couplings (M) in such a way that the reflected waves $(b_1, b_2 \ldots b_N)$ are minimized. Thus, the maximum power couples to far-field modes of antenna $(b_{N+1}, b_{N+2} \ldots b_M)$.

2.5.1 Optimization method

The scattering parameters have been the de-facto representation of any physical circuit including linear and non-linear devices since 1950's. These parameters are used in various ways such as in simulations for designing systems, measurements and sharing results as a high-fidelity model. Similarly, the multiport antenna consisting

of N-elements can be represented by the following scattering matrix:

$$\begin{bmatrix} b_1 \\ \vdots \\ b_N \\ \vdots \\ b_M \end{bmatrix} = \begin{bmatrix} S_{11} & \dots & S_{1N} & \dots & S_{1M} \\ \vdots & \ddots & \vdots & \ddots & \vdots \\ S_{N1} & \dots & S_{NN} & \dots & S_{NM} \\ \vdots & \ddots & \vdots & \ddots & \vdots \\ S_{M1} & \dots & S_{MN} & \dots & S_{MM} \end{bmatrix} \begin{bmatrix} a_1 \\ \vdots \\ a_N \\ \vdots \\ a_M \end{bmatrix} \tag{7}$$

where subscripts $1 \dots N$ corresponds to the feeding ports and $N+1 \dots M$ to the far field modes of antenna. Assuming a lossless antenna simplifies the scattering matrix (S) where most of the power goes to the far field zones. Thus, the far field modes $(b_{N+1}, b_{N+2} \dots b_M)$ are neglected from the analysis. Now, the matrix in Eq. 21. reduces to

$$\mathbf{b} = \begin{bmatrix} b_1 \\ \vdots \\ b_N \end{bmatrix} = \begin{bmatrix} S_{11} & \dots & S_{1N} \\ \vdots & \ddots & \vdots \\ S_{N1} & \dots & S_{NN} \end{bmatrix} \begin{bmatrix} a_1 \\ \vdots \\ a_N \end{bmatrix} = \mathbf{Sa} \tag{8}$$

The reflected waves ($\mathbf{b}$) have to be zero ideally in order to tune the antenna, which is not possible. These reflections can be minimized to an extent having negligible effect on the antenna performance. It follows that the specific excitations ($\mathbf{a}$) will minimize the reflected waves ($\mathbf{b}$), and input port reflection coefficients (S_{ii}). On the other hand, the antenna matching efficiency (η) can be described as the total power accepted by the antenna to the total incident power as shown in Eq. 22. The total power accepted by the antenna is represented by the dissipation matrix $\mathbf{D} = \mathbf{I} - \mathbf{S^H S}$ where $\mathbf{I}$ is the identity matrix and $(.)^{\mathbf{H}}$ is hermition operator. The tunability also implies that the efficiency(η) has to be maximized which can be done by choosing the excitation vector ($\mathbf{a}$) equal to the eigen vector of $\mathbf{D}$ corresponding to the largest eigen value [24]. The tuning ability of a multiport antenna is described by the total active reflection coefficient (TARC). The efficiency (η) and total active reflection coefficient are related via Eq. 23.

$$\eta = \frac{P_{delivered}}{P_{available}} = \frac{\mathbf{a^H a} - \mathbf{b^H b}}{\mathbf{a^H a}} = \frac{\mathbf{a^H a} - \mathbf{a^H S^H S a}}{\mathbf{a^H a}} = \frac{\mathbf{a^H (I - S^H S) a}}{\mathbf{a^H a}} = \frac{\mathbf{a^H D a}}{\mathbf{a^H a}} \tag{9}$$

$$TARC = \frac{\sqrt{b^H b}}{\sqrt{a^H a}} \tag{10}$$

$$\eta = 1 - TARC^2 \tag{11}$$

2.5.2 Antenna specifications

The antenna under consideration is designed by J. M. Hannula working under supervision of Prof. Viikkari. It consists of four monopoles of different length. The elements are designed in such a way that the wideband performance will be significantly increased. In contrast to an antenna array, the elements are resonating

at different frequencies due to different lengths. As a result, the tuning range will cover several frequency bands. A compromise has to be made regarding the number of antenna elements depending on the requirement of usable impedance bandwidth. The antenna operates in the range of 1 to 7 GHz with critical parameters such as efficiency $> 90\%$ and TARC < -10dB. The designed antenna and its scattering parameters are shown below in Fig. 13 and Fig. 14. The simulated and measured s-parameters of the antenna are from J. M. Hannula's work.

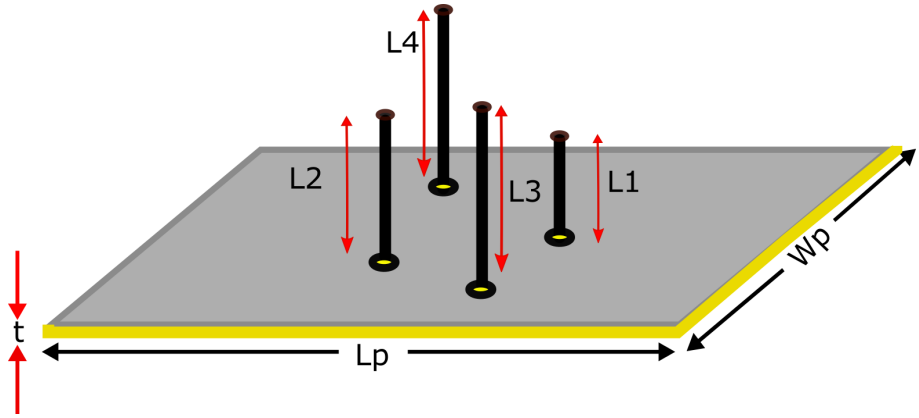


Figure 13: A multiport antenna comprising four monopoles

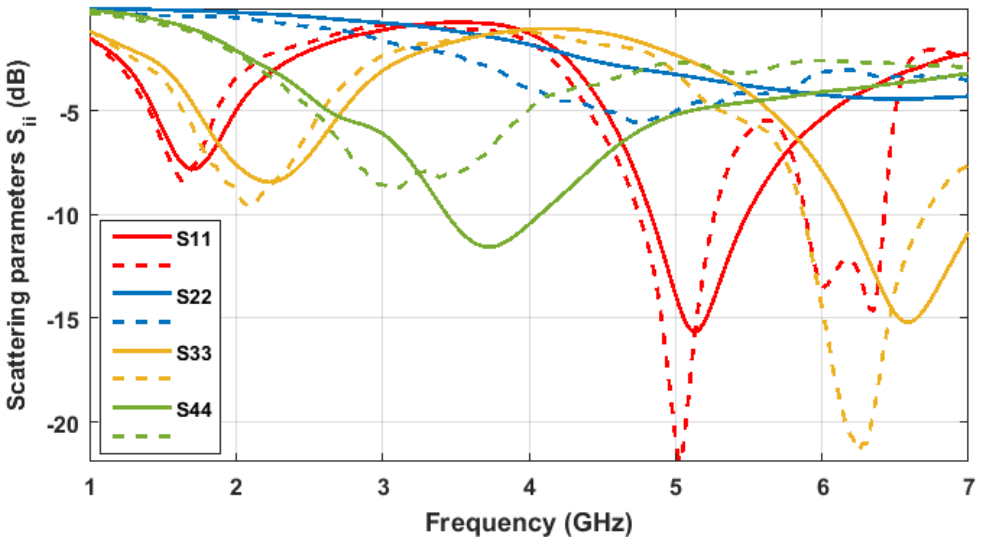


Figure 14: Input scattering parameters of 4-port antenna: simulated (solid) and measured (dashed) antennas

2.5.3 Weighted signals

The optimal excitation vector or weighted signal $\mathbf{a} = [a_1, a_2, \ldots a_N]$ with specific amplitudes and phases tune the antenna at the desired frequency. Consider a test case of 2 GHz where the weighted signal amplitudes $\langle A1 \ldots A4 \rangle$ and phases $\langle P1 \ldots P4 \rangle$ are presented in Eq. 24. This signal result in minimum reflections at the input ports and the whole incident power is delivered to our antenna load at that frequency. The total power delivered ($P_{delivered}$) and the TARC are related via Eq. 13 and Eq. 14. Instead of matching the port impedances through matching blocks, the mutual coupling effect minimize the port reflections shown in Fig. 15. On the whole, the system performance at 2 GHz can be represented by the power and TARC profiles illustrated in Fig. 16 and Fig. 17.The mathematical procedure for weight calculations enable us to determine the weighted signal for any given multiport antenna. Therefore, the weighted signal amplitude and phase for the whole frequency range covering 1 GHz–7 GHz are shown in Fig. 18 and Fig. 19.

$$\begin{bmatrix} A_1 \angle P_1 \\ A_2 \angle P_2 \\ A_3 \angle P_3 \\ A_4 \angle P_4 \end{bmatrix} = \begin{bmatrix} 0.59 \angle 160^\circ \\ 0.08 \angle -18^\circ \\ 0.68 \angle 90^\circ \\ 0.43 \angle 0^\circ \end{bmatrix} \tag{12}$$

$$\mathrm{P}_{\mathrm{delivered}} = \sum_{i=1}^{4} P_{i,del} \tag{13}$$

$$\mathrm{TARC} = 10 \log_{10} \left(1 - P_{delivered}/P_{incident}\right) \tag{14}$$

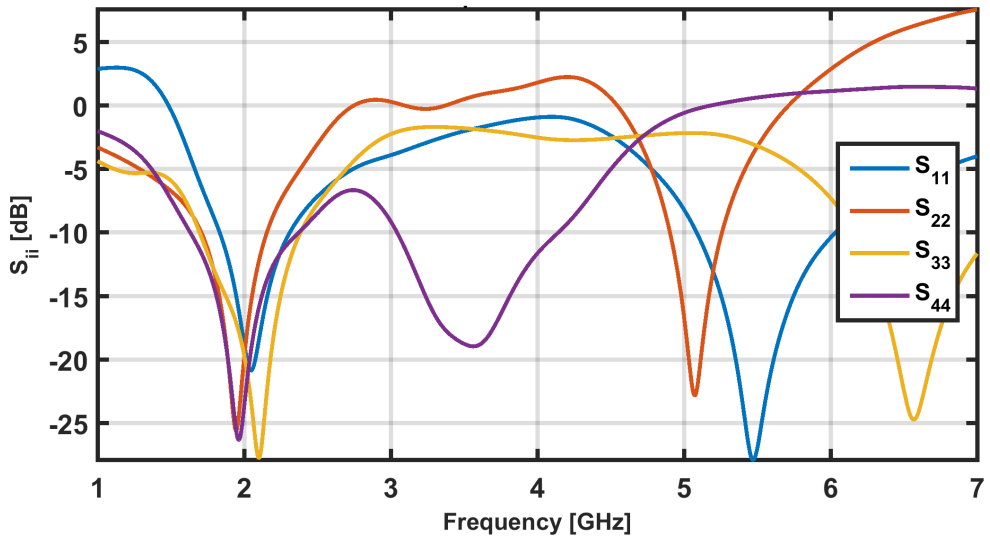


Figure 15: The 2 GHz weighted excitations result into matching condition where all the ports are matched

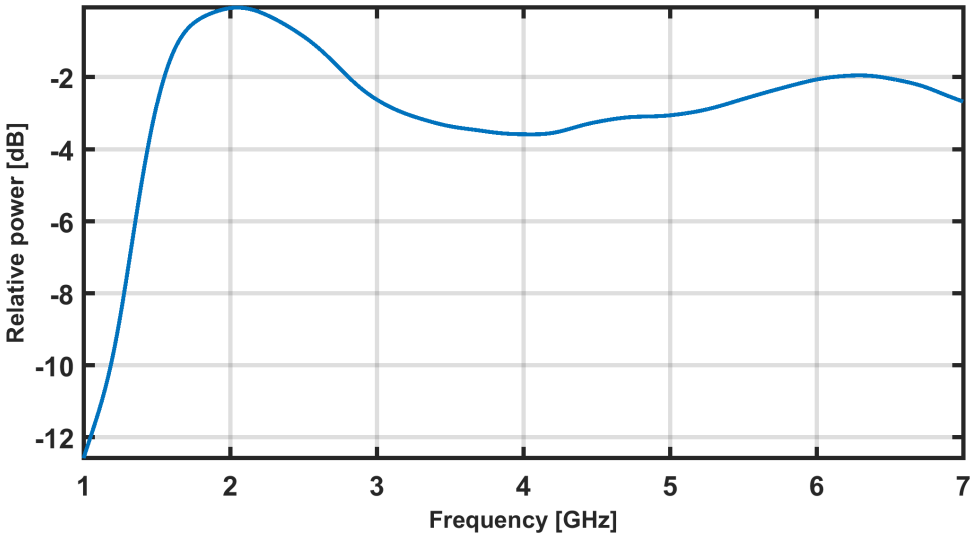


Figure 16: Relative power profile with maximum power at 2 GHz

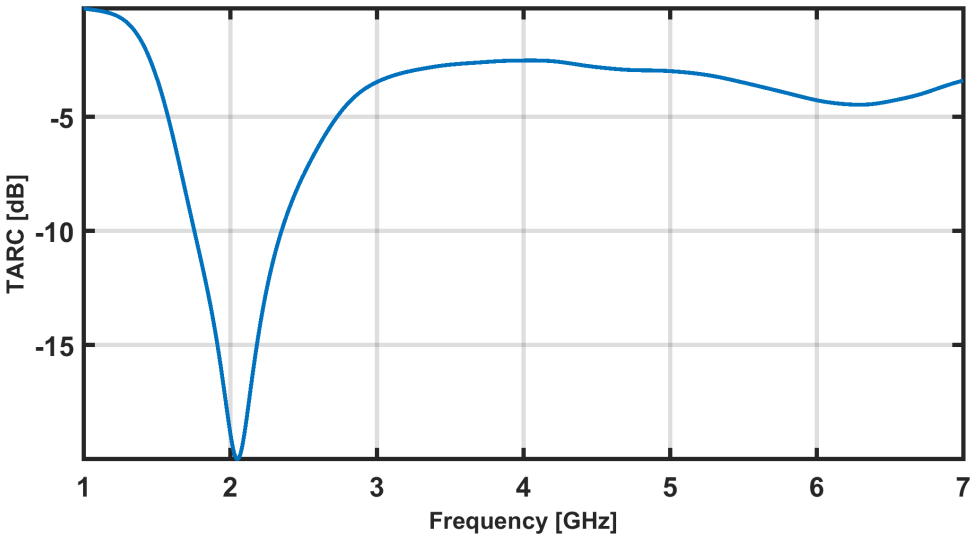


Figure 17: TARC profile with minimum reflection loss at 2 GHz

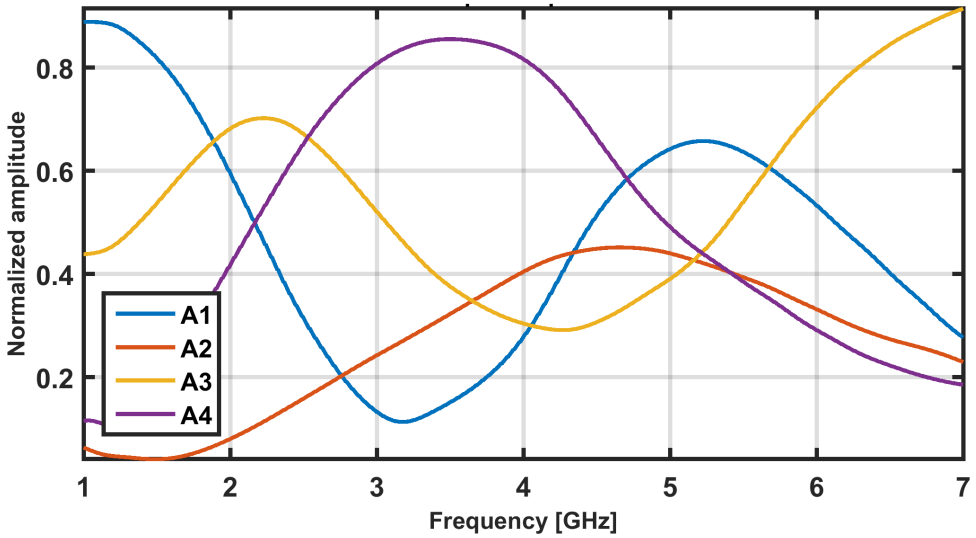


Figure 18: Amplitude profile consisting of weighted signal amplitude characteristics for the whole spectrum

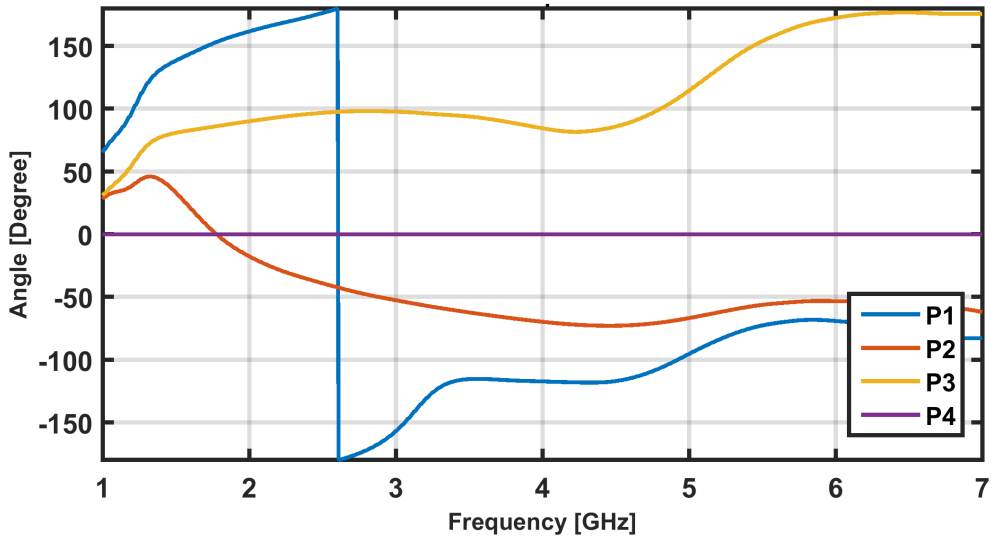


Figure 19: Phase profile consisting of weighted signal phase characteristics for the whole spectrum

2.5.4 Tuning Objective – TARC performance

The TARC represents the tuning benchmark or matching ability of a multiport antenna. It is used to determine the antenna performance for the whole range of frequencies e.g., the antenna under consideration has an operating range from 1–7 GHz. Therefore, the weighted signals have been applied covering each frequency point of the spectrum, and the corresponding minimum possible TARC represented

by TARC[i] is determined as shown in Fig. 20. It is clear that the given antenna can achieve tunability over large frequency ranges at the expense of more antenna elements. As per the antenna constraints such as efficiency$>90\%$ and TARC <-10dB, the coverable spectrum is from 1.6–6.8 GHz.

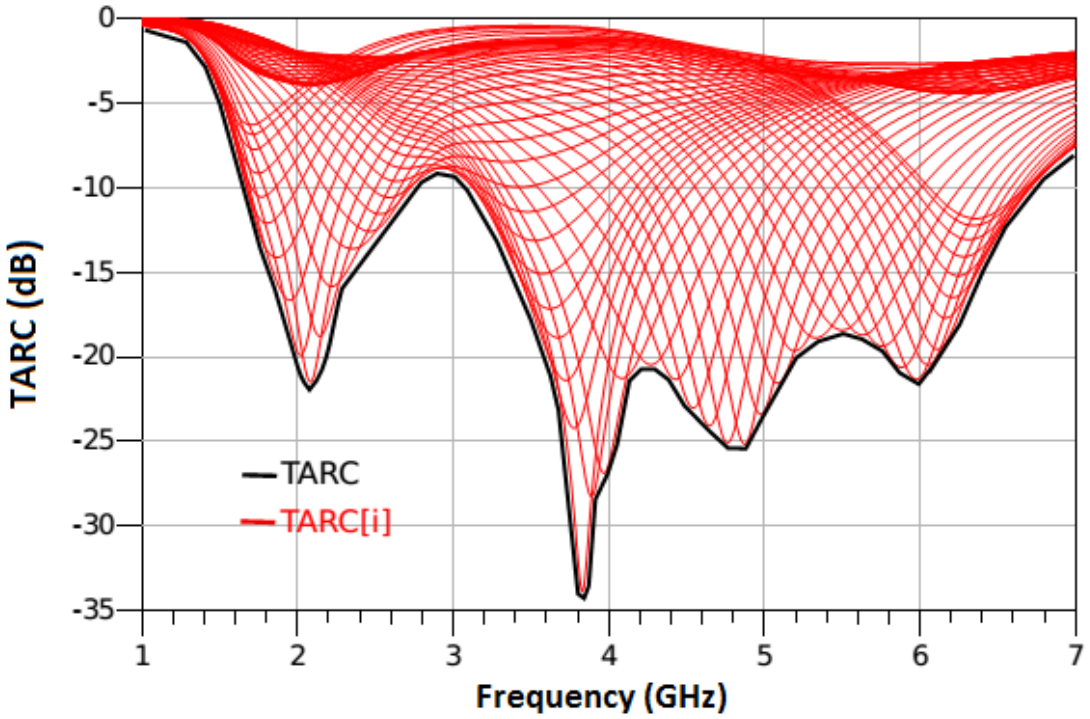


Figure 20: Multiport antenna TARC profile

2.6 Summary

- Traditional matching circuits serve simple and viable tuning, however the scalability issues rise with the number of antennas.
- Multiband antennas have multiband tuning feature with poor isolation requiring high quality filters for out of band noise.
- Reconfigurable antennas enable tunability over several bands of the spectrum. These antennas demand complex bias circuitry consisting of expensive switches in order to cover more frequency bands.
- Multifeed approach, a static technique where the antenna feeding signal characteristics are determined with an iterative algorithm which may result into tuning of antenna.
- The multiport antenna tuning approach provides dynamic frequency tuning over several frequency bands. A well defined mathematical procedure pro actively presents the weighted signal amplitudes and phases for the whole spectrum. The tunability of any multiport antenna is possible with that technique.

3 Tuning Analysis

In this chapter, the weighting of antenna feeds and its effect on the multiport antenna tuning performance are presented. Section 3.1 discuss those effects introduced by weighted signals using a proper methodology known as the tuning analysis. This approach gives insight about the possible variations in weighted signal characteristics such as amplitude and phases along with the tuning benchmark, the TARC in Section 3.2 and Section 3.3 respectively. Then, the transition from discrete level implementations towards the system on chip solution is proposed with its implicit benefits while utilizing latest technology.

3.1 Tuning framework

The tuning of antenna requires weighted excitations with certain amplitudes and phases. These amplitude and phase parameters ($A_i \angle P_i$) are accurate and continuous in an ideal case as illustrated in Fig. 21. However, the exactitude of signals fall apart in the implementation domain where the practical factors dictate the accuracy and precision. Such limitations deteriorate the antenna performance, and the extent of degradation is solely dependent on the variations in excitation signal amplitudes and phases. Therefore, these variations are studied through a tuning methodology specifically developed to illustrate the consequences in tuning performance. In the tuning approach, a controlled amount of error is introduced in feeding signal amplitude and phase to understand the antenna tuning capability. It also targets for the amplitude and phase specifications which satisfy the tuning criteria (TARC < -10dB) under various restrictions.

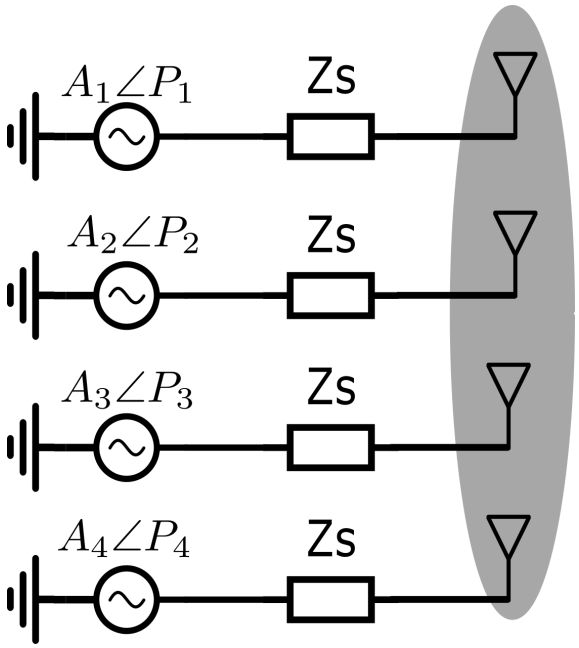


Figure 21: Multiport tuning system

The tuning analysis includes the factor of finite achievable accuracy as a basis of the method. This in turn demand the weighted signal characteristics defined in Fig. 18 and Fig. 19 on Page 15 to be quantized. Therefore, the amplitude profile and the phase profile can be described with discrete levels with particular resolutions. For instance, the fixed step sizes of "0.1" for amplitude and "5 degree" for phase descriptions are assummed as shown in Fig. 22 and Fig. 23. With these new weighted profiles, the tuning benchmark is compared against the ideal one as shown in Fig. 24. In that case the resolution required to scale amplitude and phase can be estimated: the total amplitude levels of 10 are feasible with approximately m-bits ($m = 3$) and the phase step size of 5 degrees correspond to ($360/5 = 72$) levels with n-bits ($n = 7$). Hence, this approach serves as a basis to determine either these resolutions are enough for tuning purposes or not.

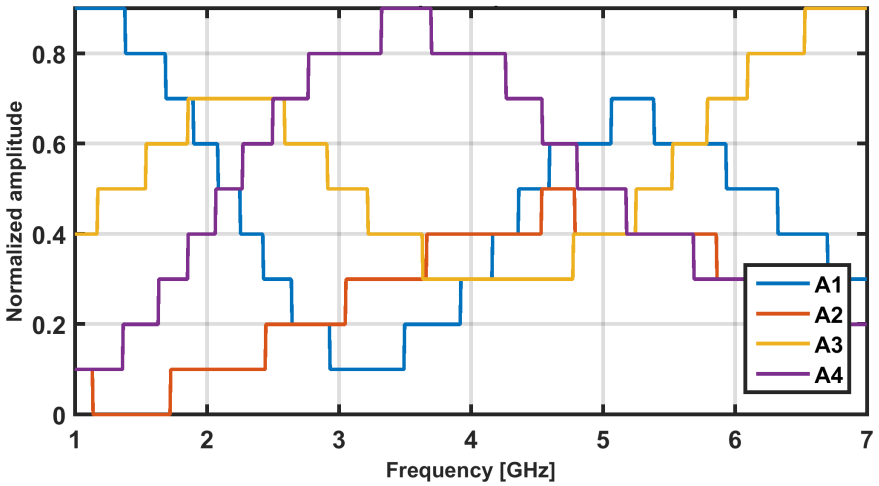


Figure 22: Quantized amplitude profile consisting of discrete amplitude levels of 0.1

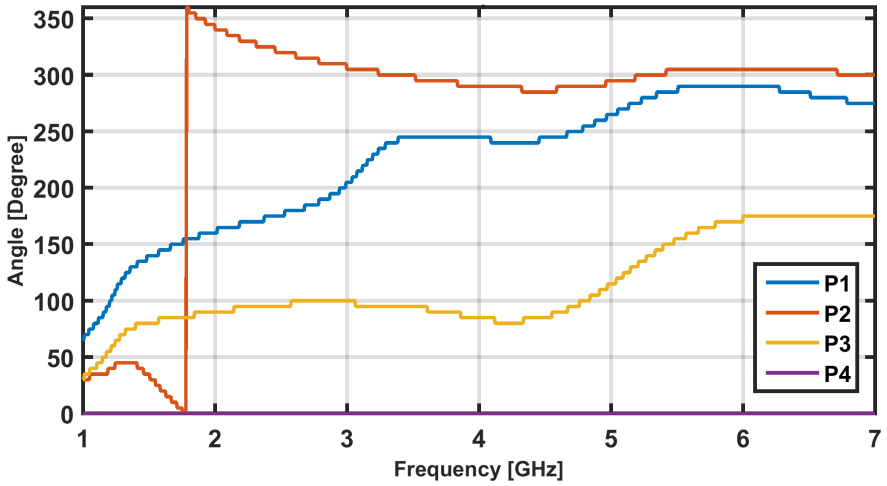


Figure 23: Quantized phase profile consisting of discrete phase steps of 5°

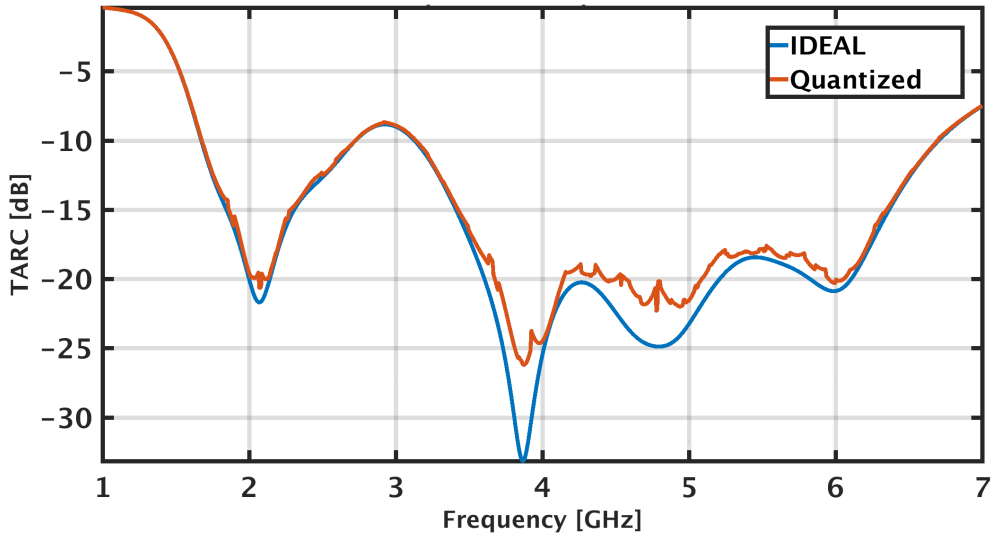


Figure 24: System TARC performance for ideal and quantized profiles

3.2 Amplitude tuning

The amplitude tuning refers to the method where the *amplitude parameter* is under consideration, in order to determine its impact on tuning of antenna. During this analysis, the phase characteristics are kept constant as that of Fig. 23. In particular, the amplitude is confronted with different size of errors which can be analyzed separately or as a whole. Firstly, the amplitude parameters are studied on individual basis at a single frequency and the resulting TARC profiles are depicted. For example, the weighted signal for the 2-GHz case based on the quantized weighted profiles is

$$\begin{bmatrix} A_1\angle P_1 \\ A_2\angle P_2 \\ A_3\angle P_3 \\ A_4\angle P_4 \end{bmatrix}_{f=2GHz} = \begin{bmatrix} 0.59\angle 162^\circ \\ 0.08\angle -18^\circ \\ 0.68\angle 90^\circ \\ 0.42\angle 0^\circ \end{bmatrix}_{IDEAL} \rightarrow \begin{bmatrix} 0.6\angle 160^\circ \\ 0\angle 340^\circ \\ 0.7\angle 90^\circ \\ 0.4\angle 0^\circ \end{bmatrix}_{Quantized}$$

Now, only one of the signal amplitude is varied at a time by adding error sizes of $[\pm 10\%, \pm 20\%, \pm 30\%]$ while keeping other phases and amplitudes unchanged, in order to see the related variations in the TARC profile shown in Fig. 25. Since the second signal is zero in that case, it can be neglected from the analysis. The same procedure is applied on each of the amplitude parameter, and it can also be described by the following scheme:

- $\cancel{A_i}$: $A_{j\neq i}, P_{j=1...4}$ are intact.
- $[A_i, A_2, A_3, A_4]$=[0.6 0 0.7 0.4]; $[P_1 : P_4]$=[160° 340° 90° 0°]
- Error-size (ΔA): $\pm 0.1, \pm 0.2, \pm 0.3$
- $A_i \leftarrow A_i + \Delta A$ then $i \leftarrow i + 1$

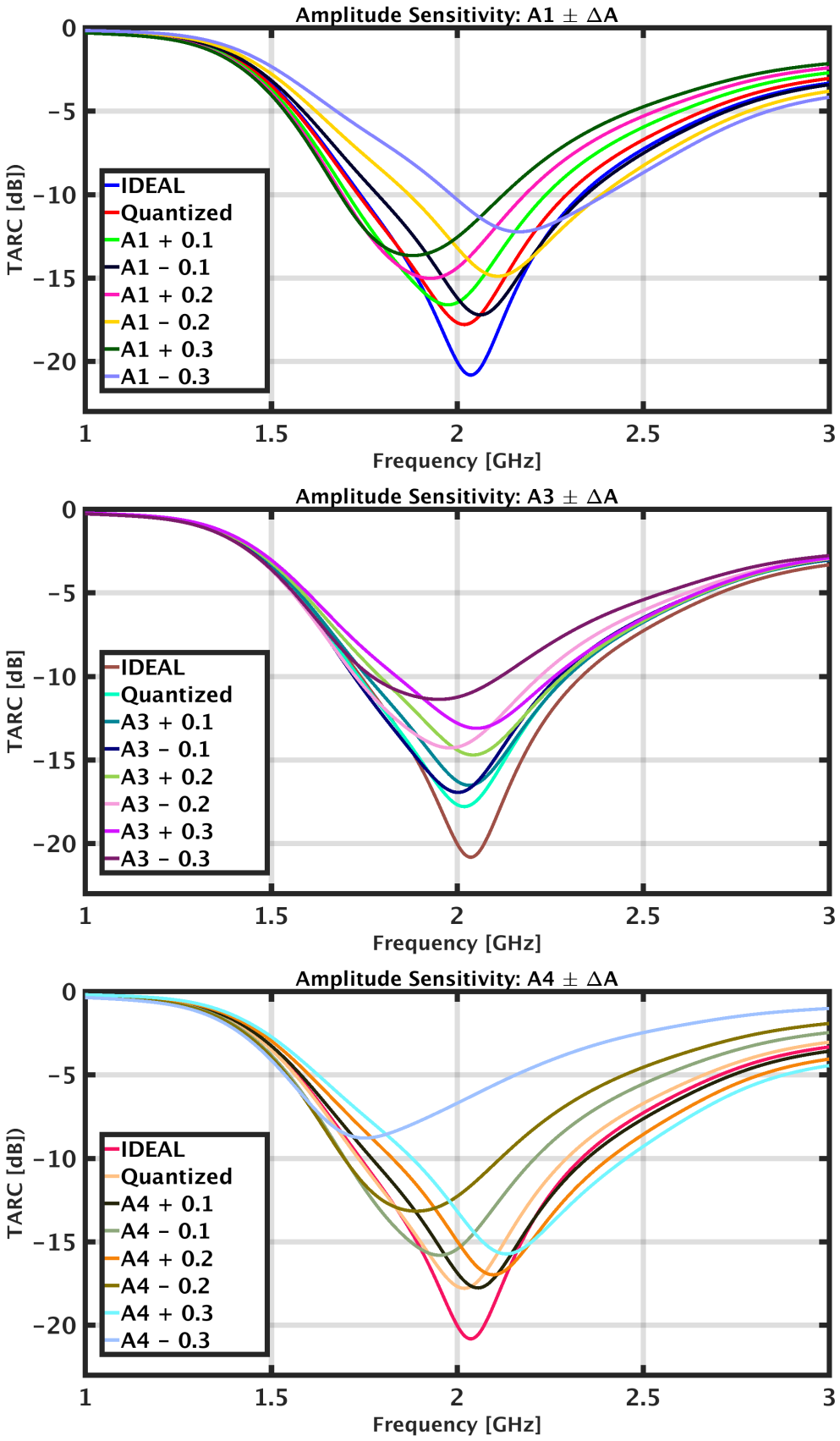


Figure 25: Independent amplitude tuning of feeding signal amplitudes(A_1, A_3, A_4) with error sizes of $(10\%, 20\%, 30\%)$ while keeping the phase characteristics constant.

As the error size is increased, the TARC profiles are being shifted away from the frequency of interest and the tuning performance is exacerbated. This shows the amplitude sensitivity of the feeds which is clearly indicated by the distorted TARC profiles. Turning to the system amplitude tuning which is also essential to scrutinize the tuning ability of antenna. In this scenario, the error sizes of $(10\%, 20\%, 30\%)$ are added to the all amplitude parameters simultaneously while the phases are kept constant:

$$\mathrm{A_i} \leftarrow \mathrm{A_i} + \Delta\mathrm{A}$$

$$\mathrm{P_i} \leftarrow \mathit{constant}$$

where $i = 1 \ldots 4$ and the corresponding system performance can be assessed with respect to the desired tuning threshold as illustrated in Fig. 26. There are various practical decisions which can be made regarding this result. For instance, the tuning threshold and the number of feeds can be compromised at a certain frequency or in a particular band. Therefore, it is one of the system specification profiles which affect the system complexity and performance trade-off.

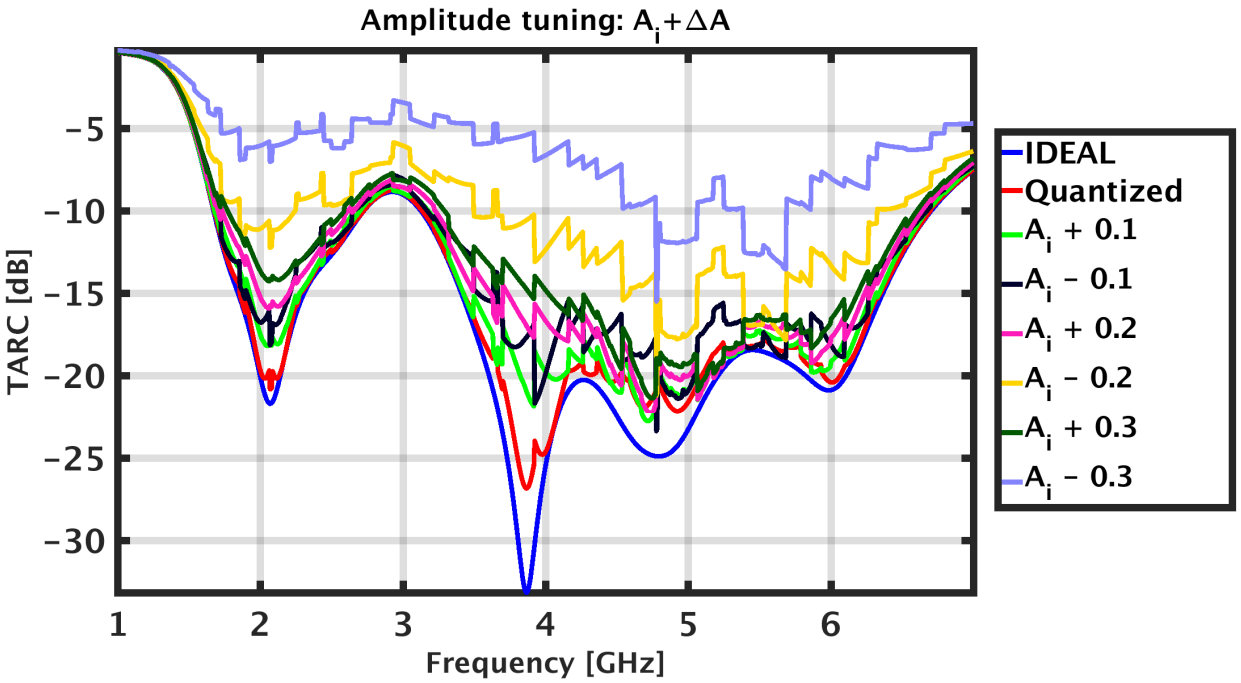


Figure 26: System amplitude tuning

3.3 Phase tuning

The phase tuning refers to the method where the *phase parameter* is under consideration, in order to determine its impact on tuning of antenna. In contrast to amplitude tuning, the amplitude characteristics are kept constant as that of Fig. 22. In particular, the phase is confronted with different size of errors which can be analyzed separately or as a whole. Similarly, the case of 2 GHz is studied with respect to phase tuning and the TARC curves are analyzed. Here the error sizes of $[\pm 5^\circ, \pm 10^\circ, \pm 15^\circ]$ are added to the individual phases while keeping other phases and amplitudes unchanged, in order to see the related variations in the TARC profile shown in Fig. 27. In the same way, it can also be described by the following procedure:

- $\not{\mathrm{P}}_\mathrm{i}$: $\mathrm{P}_{\mathrm{j}\neq\mathrm{i}}, \mathrm{A}_{\mathrm{j}=1\ldots4}$ are intact.
- $[\mathrm{P}_\mathrm{i}, \mathrm{P}_2, \mathrm{P}_3, \mathrm{P}_4]$=[160° 340° 90° 0°]; $[\mathrm{A}_1 : \mathrm{A}_4]$=[0.6 0 0.7 0.4]
- Error-size(ΔP): $\pm 5^\circ, \pm 10^\circ, \pm 15^\circ$
- $\mathrm{P}_\mathrm{i} \leftarrow \mathrm{P}_\mathrm{i} + \Delta\mathrm{P}$ then $\mathrm{i} \leftarrow \mathrm{i} + 1$

As the error size is increased, the TARC profiles are being shifted up representing the degradation. The TARC performance is relatively better than the amplitude tuning in terms of the sensitivity and the tuning threshold. With regard to the system phase tuning, the concurrent addition of error to all the phases will only shift the reference phase of the coherent signals and the system phase tuning cannot be evaluated. Therefore, the system phase tuning will be studied for each phase independently. In this scenario, the error sizes of $(5^\circ, 10^\circ, 15^\circ)$ are added to each phase separately to study the TARC behavior in the whole spectrum as shown in Fig. 28 and Fig. 29. From these results, it is clear that the phases can with stand more variations with reasonable tuning performance. It ultimately reduces the complexity, and ease the design of phase shifters.

Independent phase tuning at 2 GHz

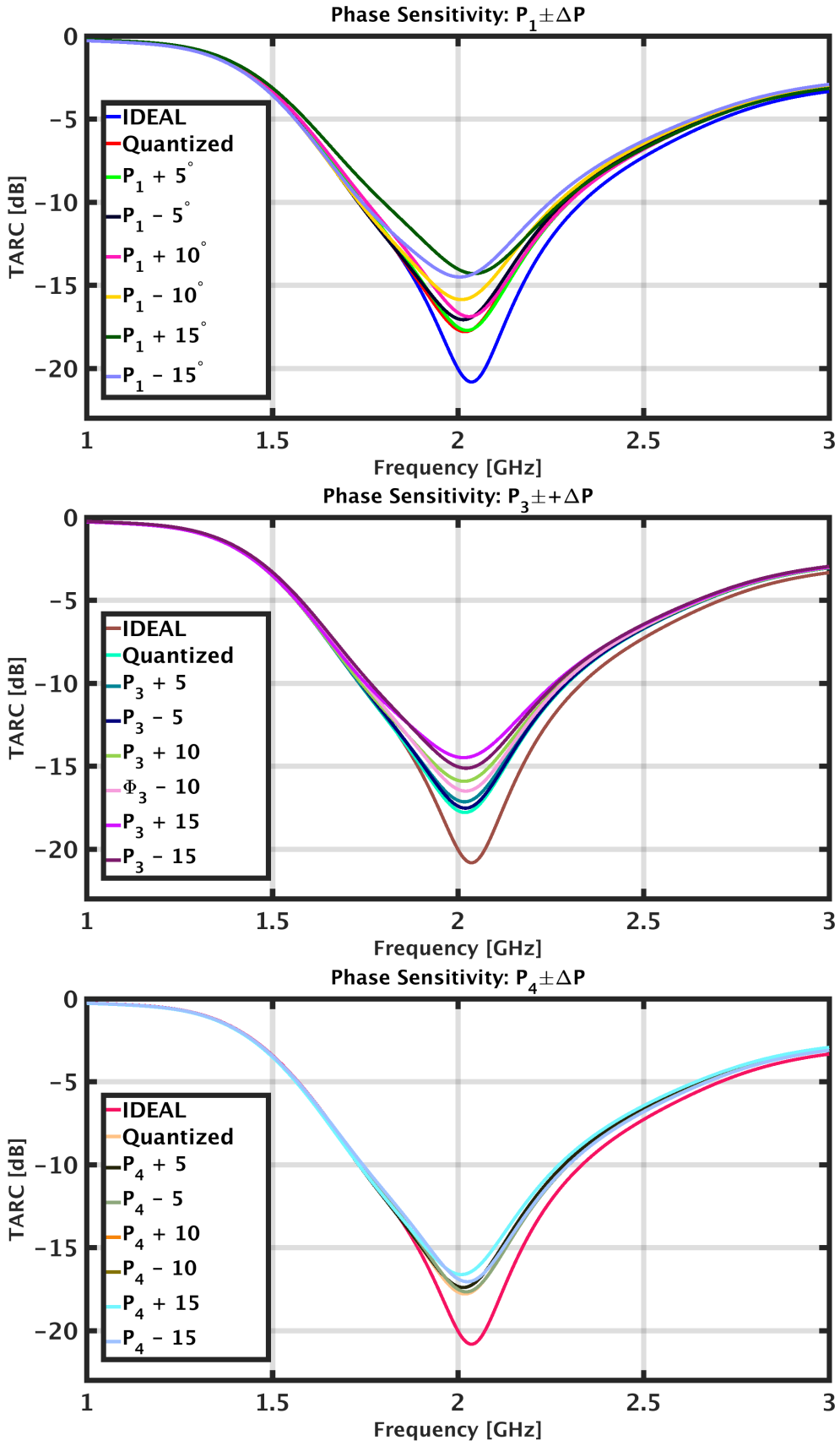


Figure 27: Independent phase tuning of feeding signal phases(P_1, P_3, P_4) with error sizes of $(5°, 10°, 15°)$ while keeping the amplitude characteristics constant.

System phase tuning

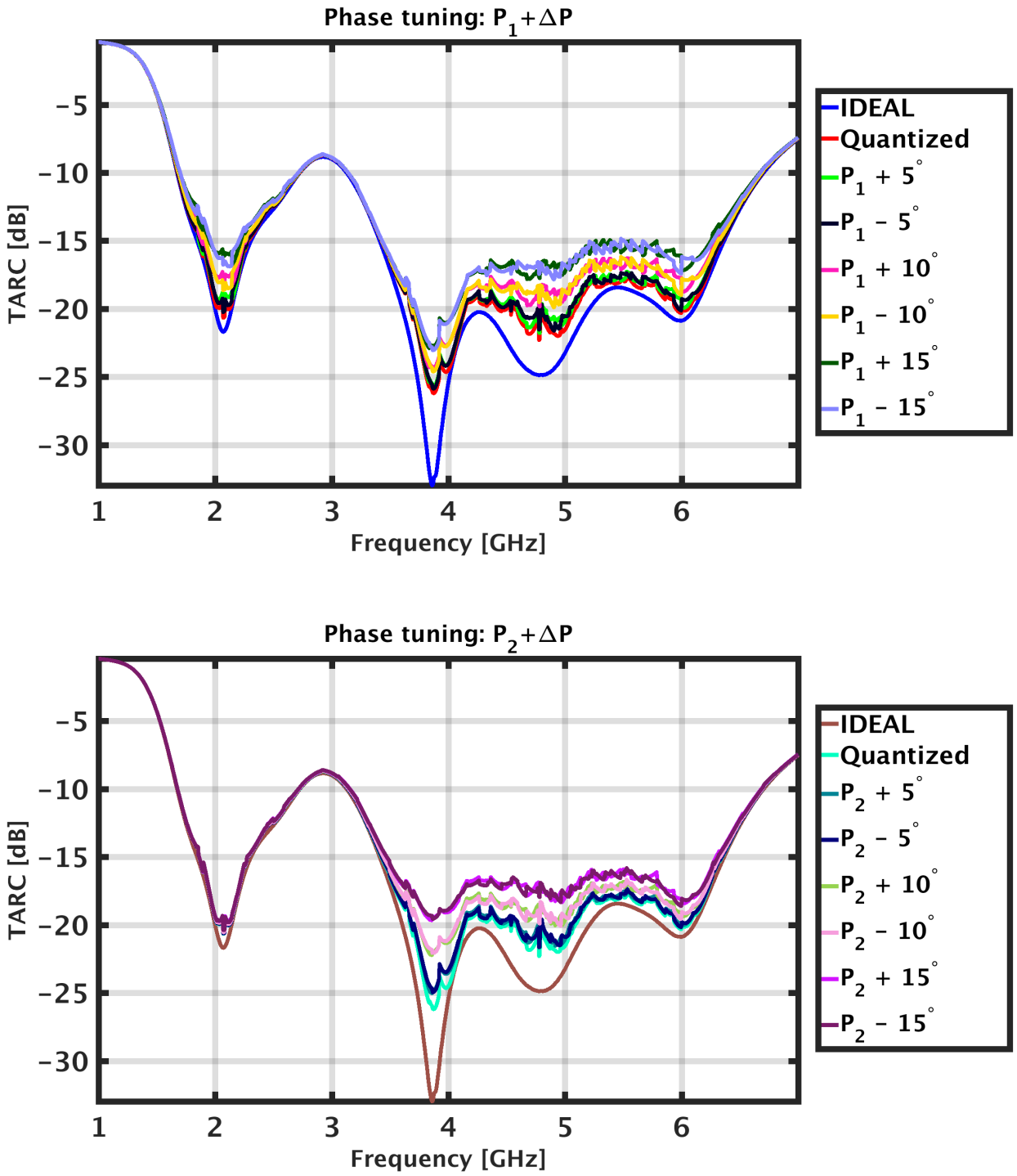


Figure 28: System phase tuning of feeding signal phases P_1 and P_2 with error sizes of $(5°, 10°, 15°)$ while keeping the amplitudes of all feeding signals constant

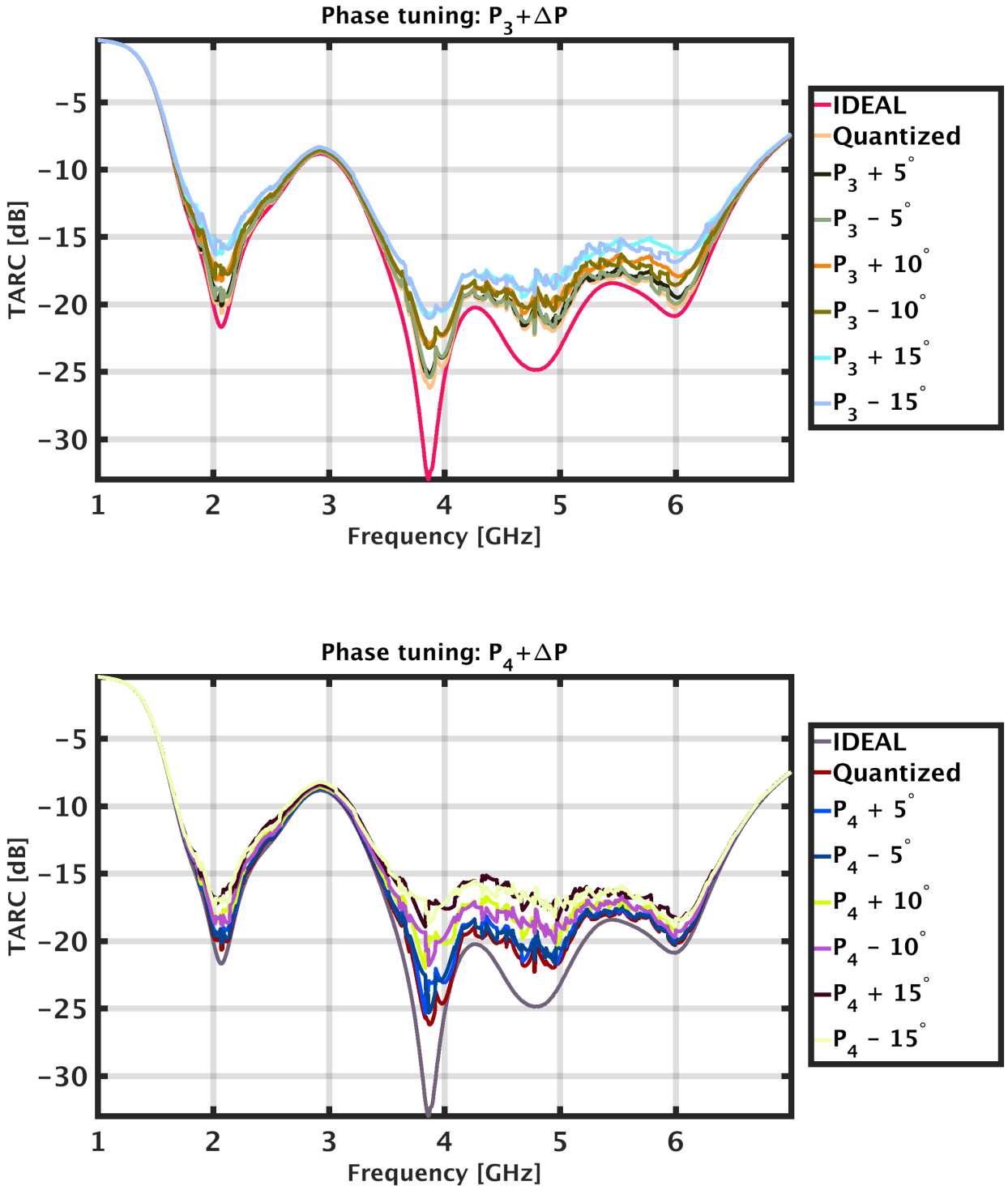


Figure 29: System phase tuning of P_3 and P_4 with error sizes of $(5°, 10°, 15°)$ while keeping the amplitudes of all feeding signals constant

3.4 Technology Limitations

In RF electronics with discrete components, the amplitude tuning can be simply achieved with customized attenuators (A_i) and the phase tuning with the transmission line based phase shifters (P_i). With regard to the phase shifters, a continuous 360° phase shift is possible at a single frequency [?], however, it requires redesign of these components to cover the new frequencies along with more hardware and cost.

Furthermore, it becomes even challenging to have fixed amount of phase resolution in the whole spectrum 1–7 GHz. Therefore, the fundamental relation is revisited regarding the phase and the corresponding time delay as shown in Fig. 30. It depicts that the constant phase is possible at the expense of tunable time delay which makes the presented approach, a static one. Thus, the dynamic phase tuning is currently not possible in the area of discrete electronics.

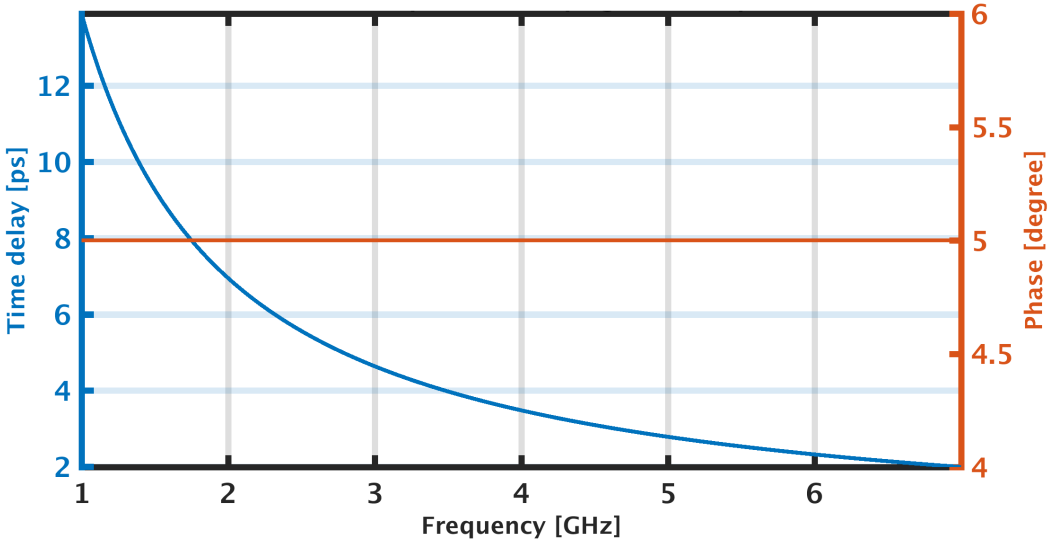


Figure 30: Constant phase of 5° ($\Phi = 360 \times f \times T_{delay}$) requires tunable delay element

Turning to the system on chip solution where the former issues are significantly resolved and the *'All digital implementation'* trend enables state of the art solution for the amplitude and phase tuning. The technology shift is inevitable for fulfilling the dynamic phase tuning and scalability issues. Therefore, the ultimate target is to tune the multiport antenna with an integrated circuit which comprises of a digitally intensive transmitter and the auxiliary tuning blocks to properly weight the antenna feeds as shown in Fig. 31. Furthermore, the amplitude tuning is possible with the low dropout regulator (LDO) and the phase tuning is done with delay entities having fixed time delay resolution with respect to the technology being used. Therefore, the current CMOS technology can be considered a better candidate providing requisite features in addition to miniaturization, less power consumption and high speed operation.

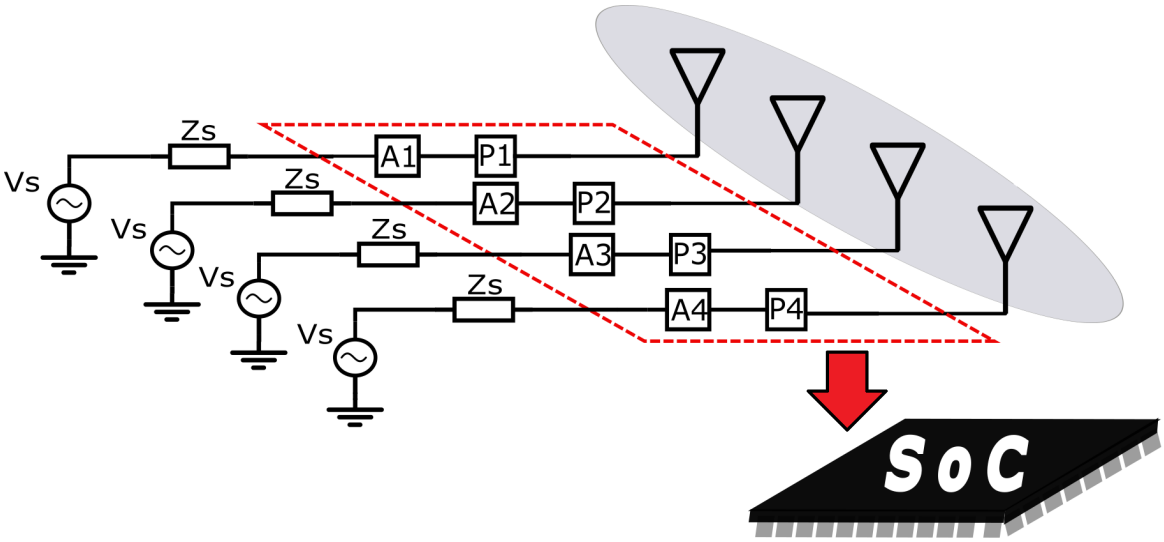


Figure 31: Transition from static approach towards system-on-chip solution

Now, it is worthwhile to consider the simplified block diagram of our proposed SoC in Fig. 32. Without going into gory details, It can be seen that the transmitter output is divided into four branches followed by the tuning blocks for the phase tuning (P_i) and the amplitude tuning (A_i) respectively. In addition, these blocks are being directed by the transmitter for the weighting of signals, and it is signified by the digitally controlled inputs (m, n), providing sufficient resolution for amplitude and phase tuning.

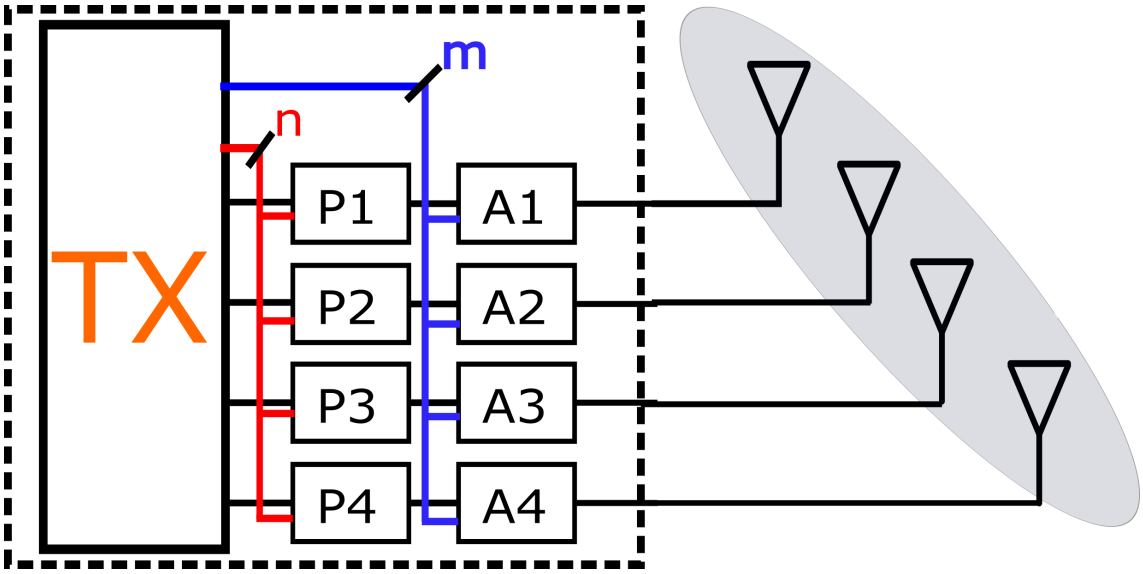


Figure 32: Transition from static approach towards system-on-chip solution

3.5 Phase tuning in SoC

From the amplitude tuning analysis, the number of amplitude tuning bits (m) are 3. As far as the phase tuning is concerned, the phase is manipulated in terms of time delays in SoC. The phase tuning bits (n) and the associated accuracy to generate required phase depend on the delay entity being used. In addition, the minimum achievable time resolution will determine either we can achieve the required phase at a particular frequency with the given technology or not. Further on, the phase tuning is represented in terms of the time delay (T_{delay}) characteristics based on the phase profile of the weighted signal illustrated in Fig. 33.

$$T_{delay} = \frac{\phi}{360 \times f} \tag{15}$$

where "f" is the frequency of signal with phase "ϕ" in degrees.

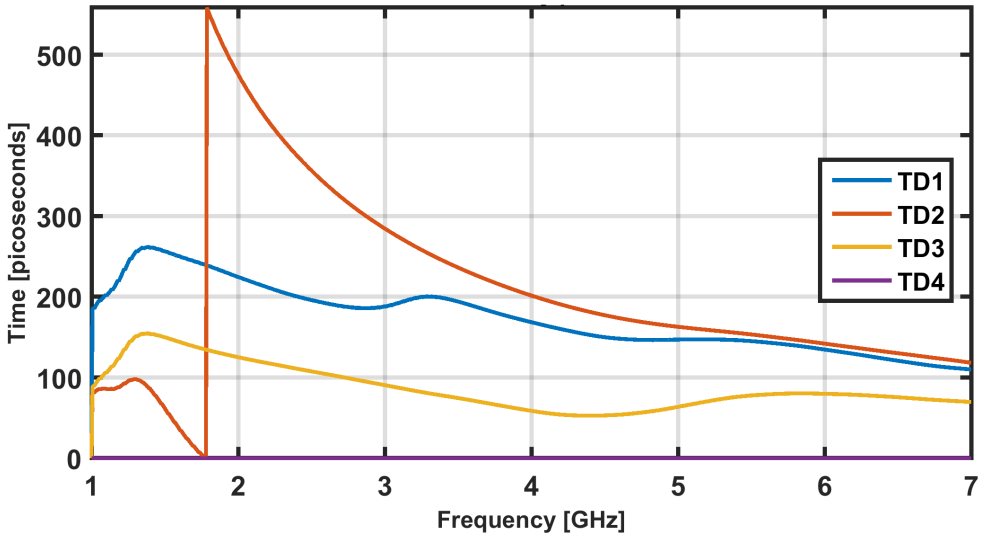


Figure 33: Time delay profile based on weighted signal phase characteristics

The phase tuning resolution depends on the maximum number of delay entities required to cover the time delay characteristics. These are determined from the time delay profile and the resolution of the delay element being used. Therefore, the delay elements of various resolutions are used for illustration purpose and the associated elements at certain frequency are shown in Fig. 34 and 35.

To assess the phase tuning performance, the phase profiles of the weighted signal based on the delay elements are reconstructed in Fig. 36 and 37. The corresponding TARC performances will decide the resolution bits(n) needed for phase tuning. As per the results, the 10ps delay element is chosen and the number of bits (n) are given by:

$$n = \log_2[\max(\mathrm{DE_i})] \approx 6$$

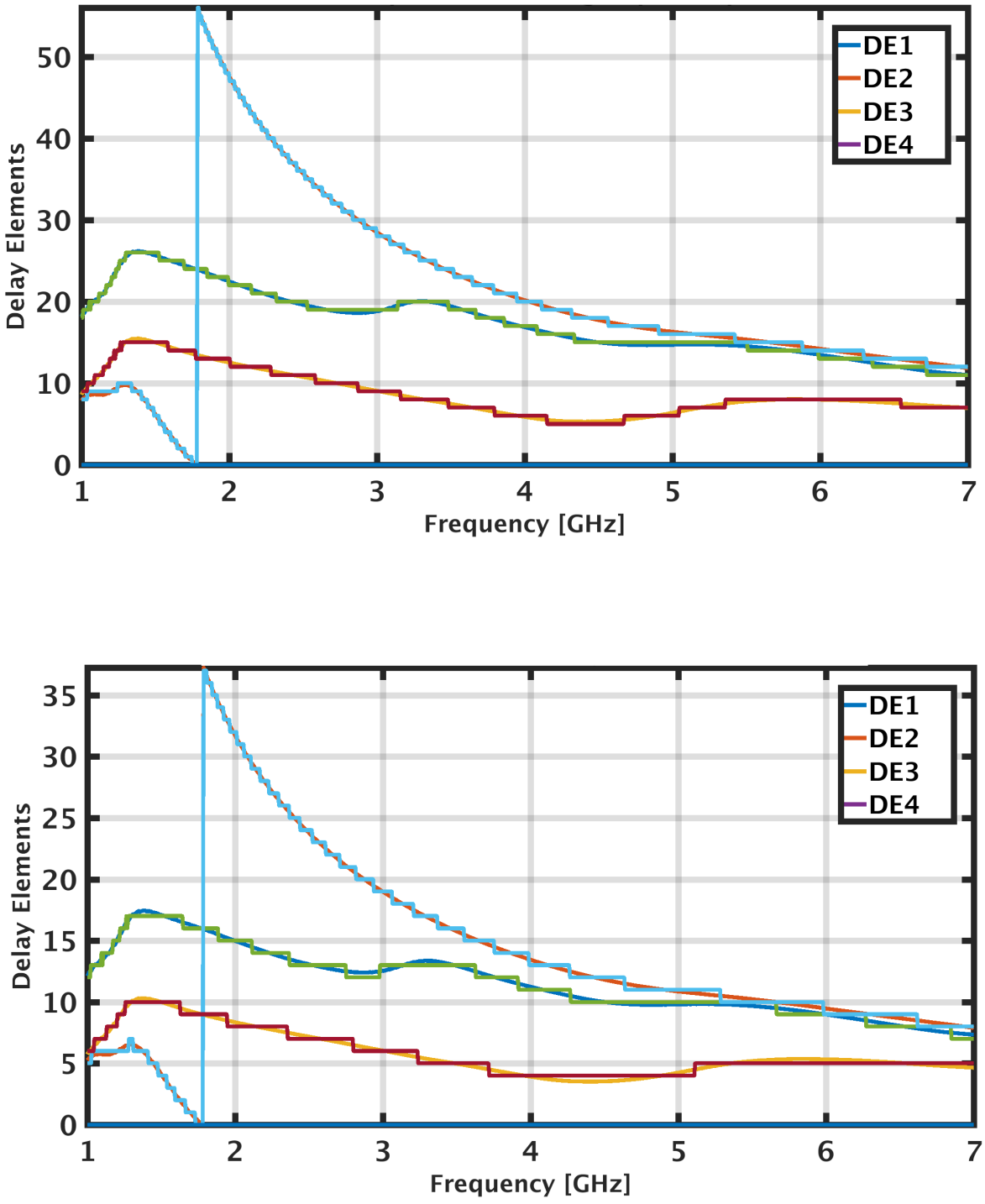


Figure 34: Number of delay elements required based on 10ps and 15ps delay element

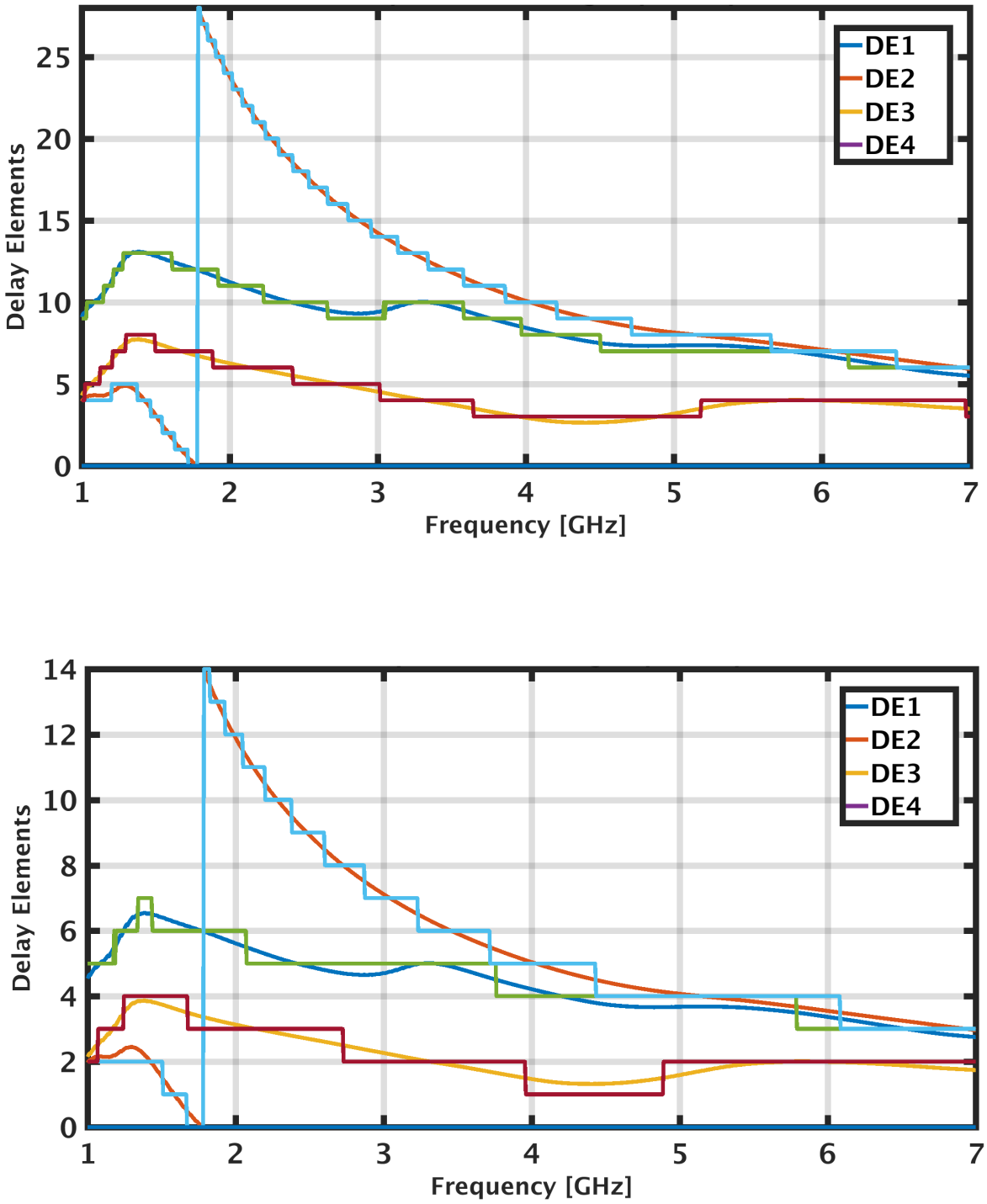


Figure 35: Number of delay elements required based on 20ps and 40ps delay element

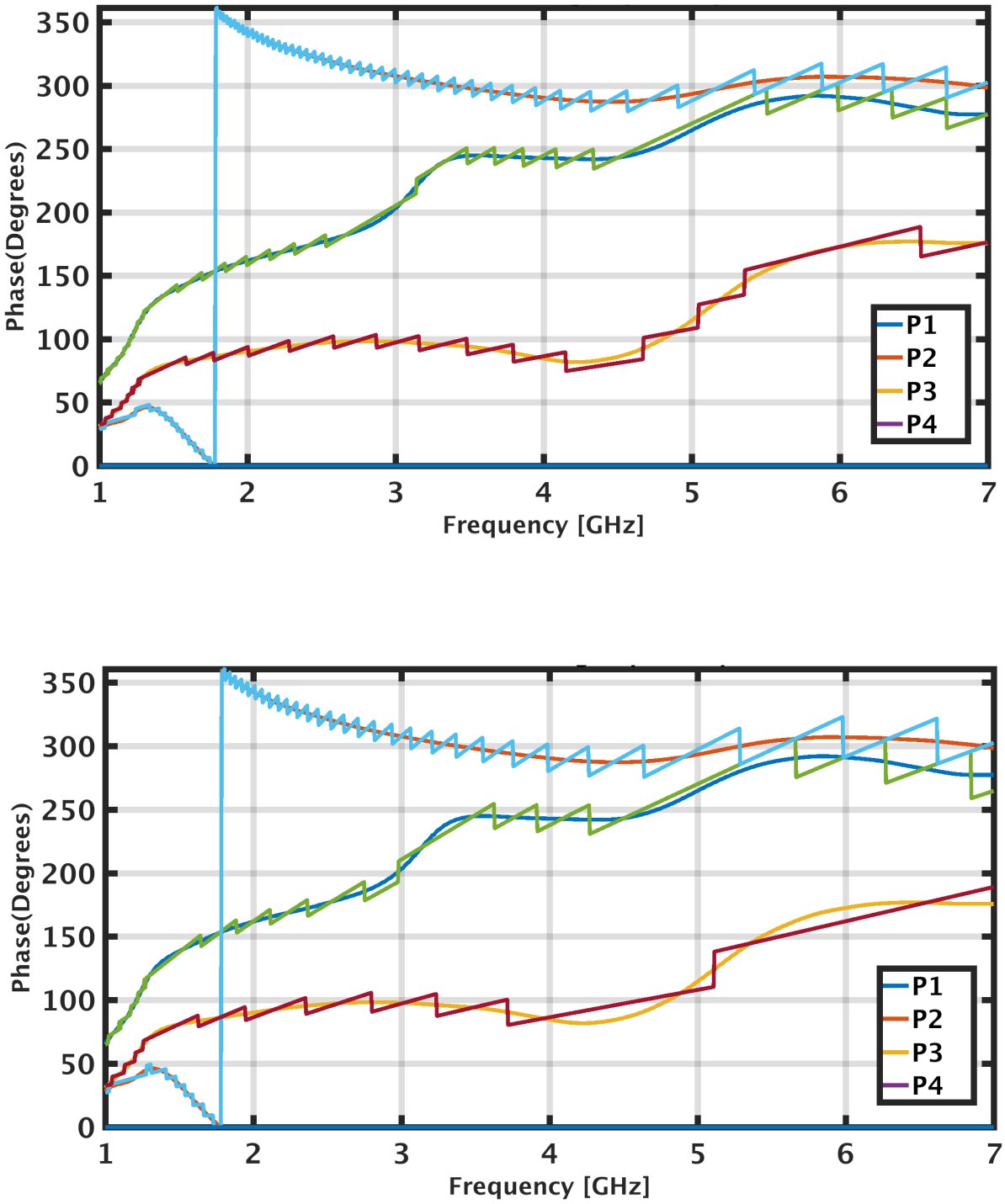


Figure 36: Phase profiles reconstructed from 10ps and 15ps delay element

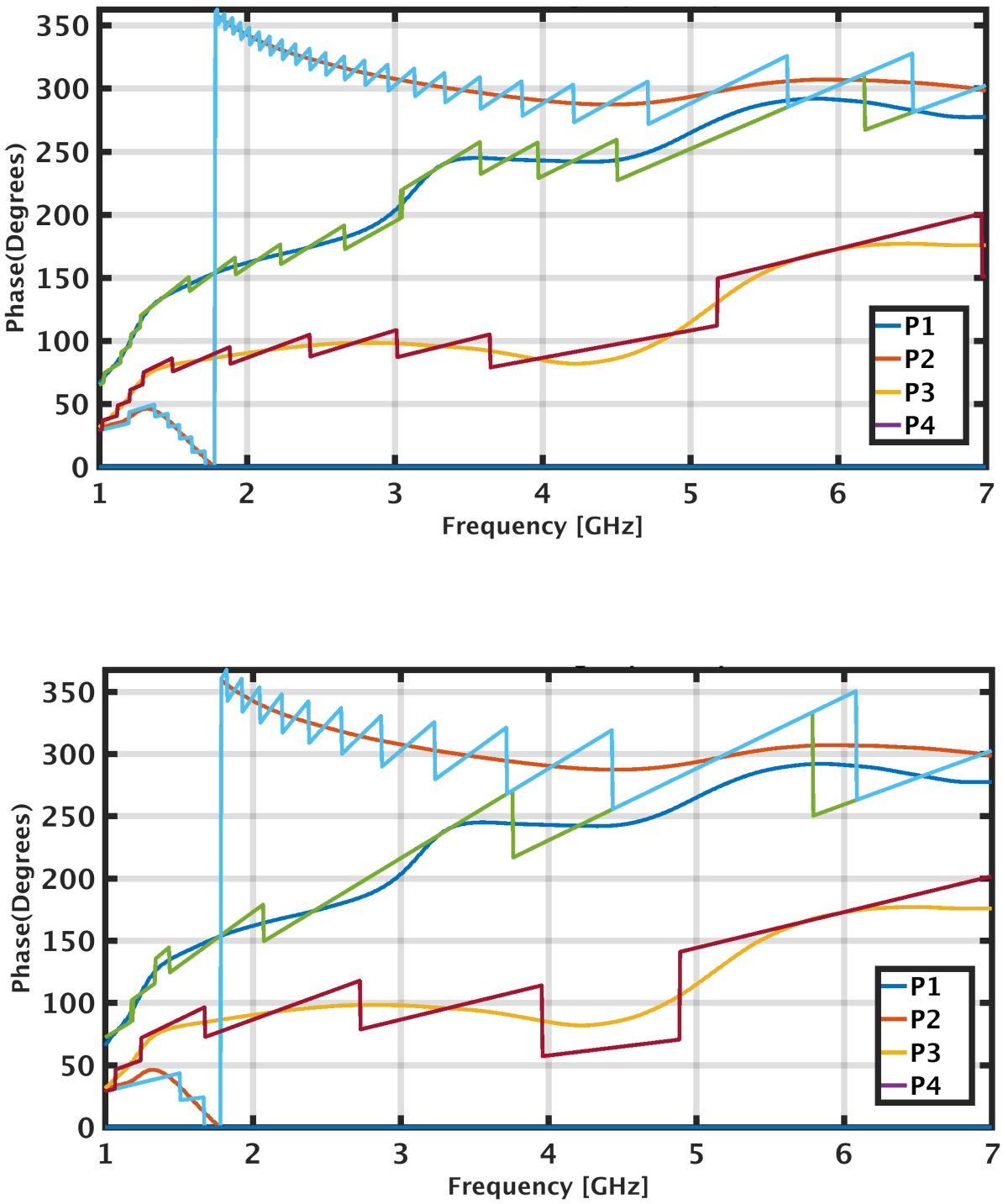


Figure 37: Phase profiles reconstructed from 20ps and 40ps delay element

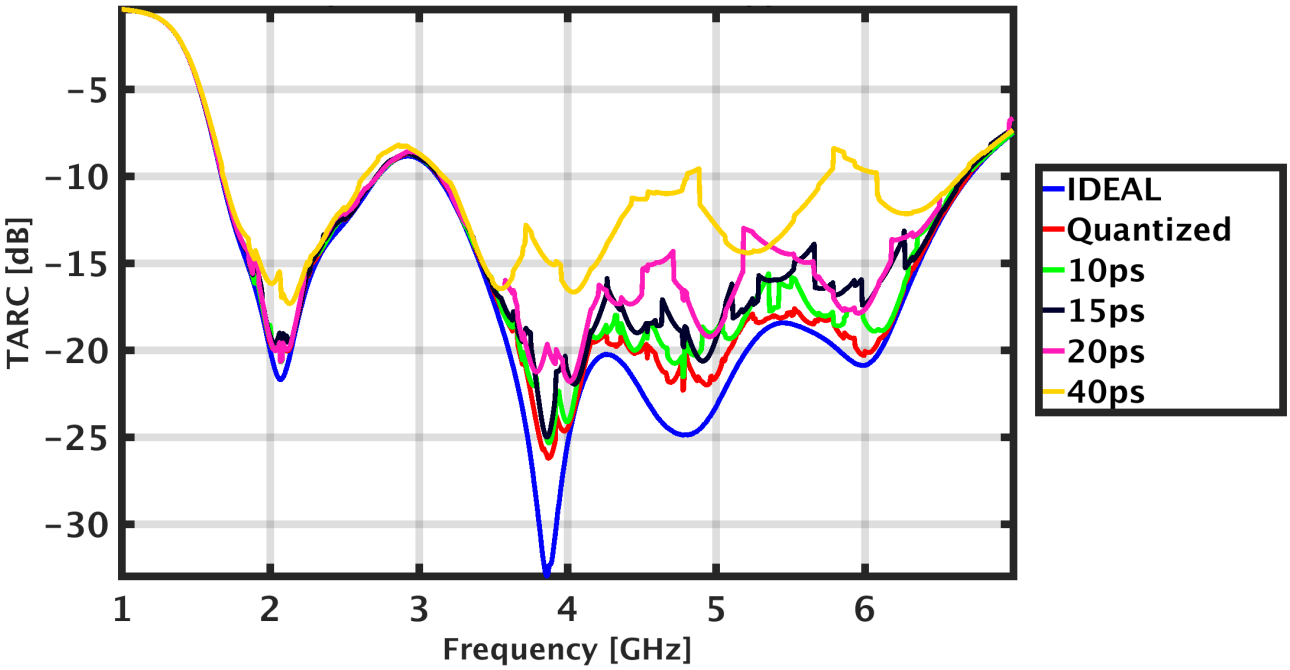


Figure 38: System phase tuning performance based on various delay elements along with the quantized(fixed phase resolution) and ideal profiles

3.6 Summary

- The accuracy to generate weighted signal has limitations and it affects the TARC performance.
- The tuning analysis determines the accuracy required in amplitude and phase scaling.
- The amplitude scaling is determined from the amplitude tuning analysis as it specifies the resolution bits ($m = 3$) for the given antenna.
- The phase tuning is kind of a static approach in discrete domain, and it limits the dynamic phase tuning. Therefore, the SoC is considered a better solution.
- The phase tuning is represented in terms of time delays in SoC and the number of resolution bits ($n = 6$) are chosen based on a 10ps delay element.
- The amplitude and phase resolution bits (m,n) are (3,6).

4 Tuning system design

In this chapter, the tuning system is designed and implemented with latest 28nm CMOS technology. It comprises of two sub-systems: the phase tuning block and the amplitude tuning block. Fig. 39 shows the block diagram of the tuning system, which include four phase tuning blocks (Pi) followed by the four amplitude tuning blocks (Ai). Section 4.1 describes the phase tuning block which is formed by a delay chain and a multiplexer. Then, the block level simulation results are presented. The amplitude tuning block has two major components: a power amplifier (PA) and a low drop out regulator (LDO). These sub-blocks are designed and implemented in Section 4.2. Finally, Section 4.3 presents the system level simulation of the tuning system and its effect on the antenna tuning performance.

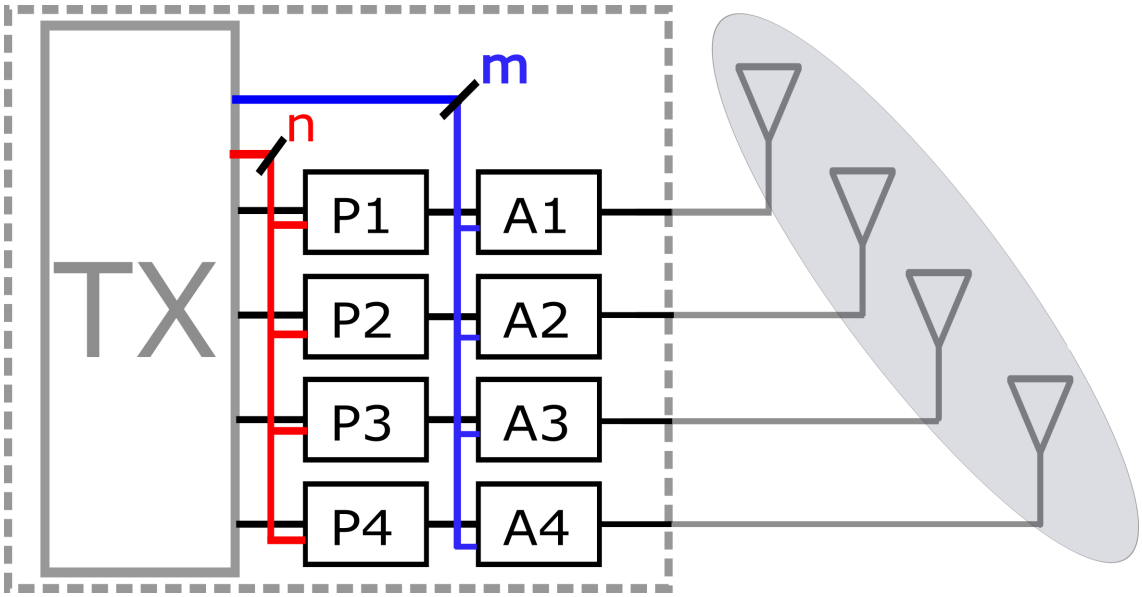


Figure 39: Tuning system consisting of phase tuning (P_i) blocks with (n = 6) bits control and amplitude tuning (A_i) blocks with (m = 3) bits control

4.1 Phase tuning block

In SoC, the phase tuning is achieved with delay tuning circuits. The delay tuning normally contains one core block which is mainly a delay chain for delaying purpose, and an auxiliary block e.g., a multiplexer for tapping the different outputs of the delay chain. Several CMOS delay architectures are available depending on the requirements [25], the target is to consider the method which fulfills the desired specifications shown in Fig. 33 on Page 28.

4.1.1 Delay chain

The delay chains are classified on the basis of how the delay is generated by the circuit. Firstly the digital delay lines where the digital input directly maps to the required delay value. In contrast, the analog delay lines are controlled with analog signals. Opting for the digital control, a digitally controlled delay line (DCDL) was selected. The delay line has two characteristics: the delay step (d_r) which is the smallest possible time step and the delay range (DR) corresponding to the maximum time a signal can be delayed. Fig. 40 presents the transfer function of DCDL where the abscissa denotes the decimal equivalent of the digital input value (n) and the ordinate shows the associated delay (T_d). The desire delay value is given by

$$T_d = D_{min} + (N-1) \times (d_r) \tag{16}$$

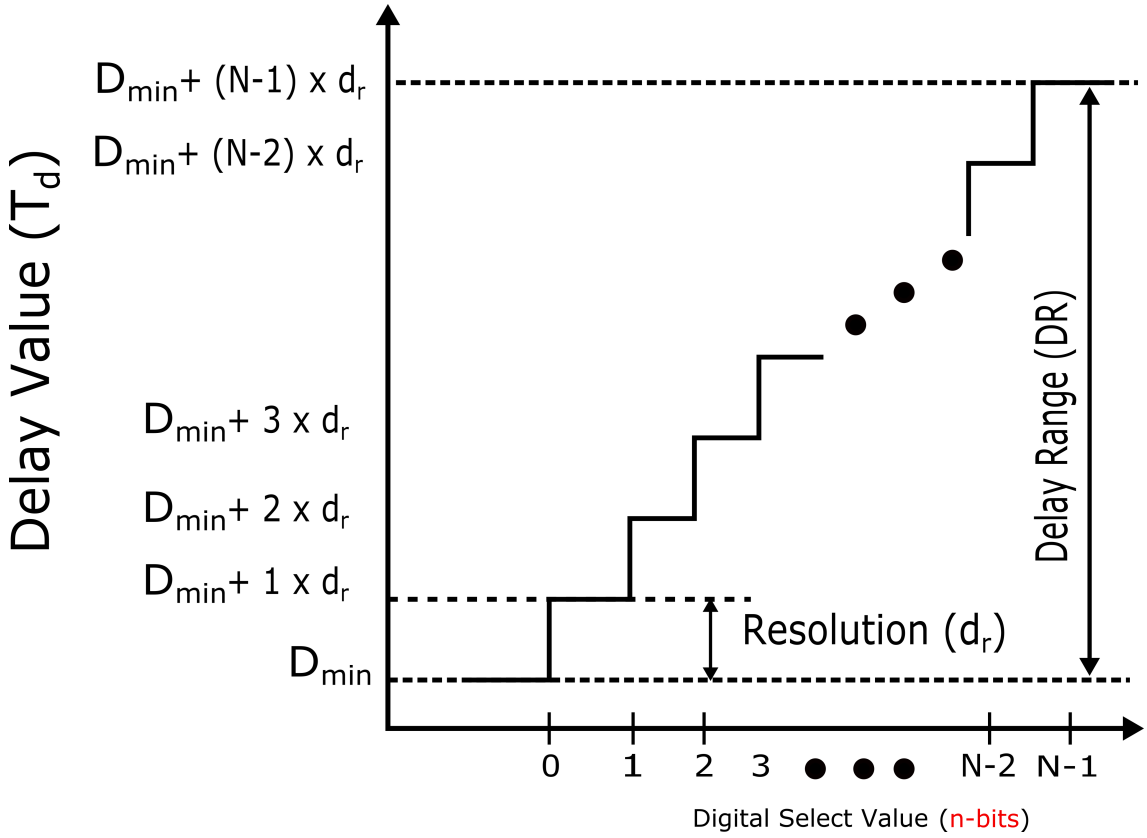


Figure 40: Digitally controlled delay line (DCDL) transfer function [26]

Since one of the major constraint was to minimize the chip area, a simple topology named as tapped delay line (TDL) was considered as shown in Fig. 41. It consists of N identical fixed delay elements (DE) which can be logic gates or flip-flops. The delayed versions of input signals are tapped from the outputs (O < i >) where $i = 0 \ldots N-1$. The DE dictates the delay step (d_r) and the delay range (DR) by the following relation

$$DR = N \times d_r \tag{17}$$

It was shown in Chapter 3 that a 10 ps DE has a relatively better performance than others. Therefore, the delay chain has 10 ps delay elements. The DE used is a buffer including two minimum sized cascaded inverters delaying the signal by delay step (d_r). In general, the delay step (d_r) relates the transistor parameters via the gate delay Eq. 18 where L, W, C_{load}, V_{dd}, μ, C_{ox}, V_{th} and α are the transistor channel length, channel width, load capacitance, supply voltage, carrier mobility, gate oxide thickness, threshold voltage and technology parameter respectively. Therefore, the minimum length transistor are used in order to have smallest delay resolution

$$d_r = \frac{\Delta Q}{\Delta I} = \frac{C_{load} V_{dd}}{\frac{W}{2L} \mu C_{ox} \left(V_{dd} - V_{th}\right)^{\alpha}} \tag{18}$$

Ideally, the input/output signals of delay entity has no imperfections. However, the parasitic model of DE gives specific insights about the behavior of the entity. Fig. 42 illustrates the DE parasitics model in which the main non-idealities are modelled as capacitors. These capacitances include the gate, drain, source, bulk and wiring capacitances. In addition, when the input signal (0 or 1) is applied to the DE, the transistors (Mn1, Mp1, Mn2, Mp2) are turned on/off. These transistors have certain on and off resistance which forms an RC combination, thus resulting in signal distortion. Though the distortion does not affect the amplitude levels, however it can cause duty cycle variations and jitter(uncertain amount of delay) in the ouput signal. Moreover, the longer delay lines have a timing jitter approximately equal to square root of the length of delay line ($\sqrt{N}$) [27]. Therefore, the key parameters of interest are duty cycle (DTC) and the propagation delay (PD) as these will affect the phase tuning block performance.

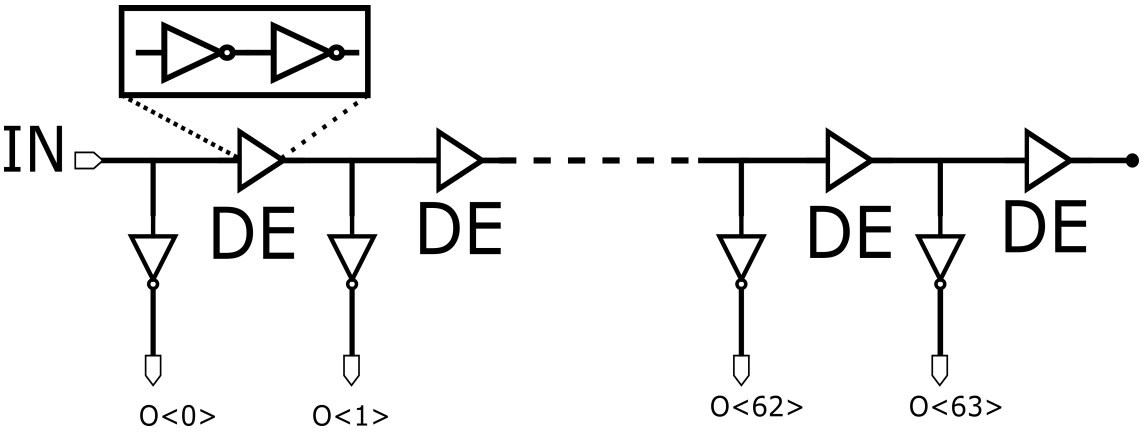


Figure 41: Tapped delay line for (n=6) bits resolution [27]

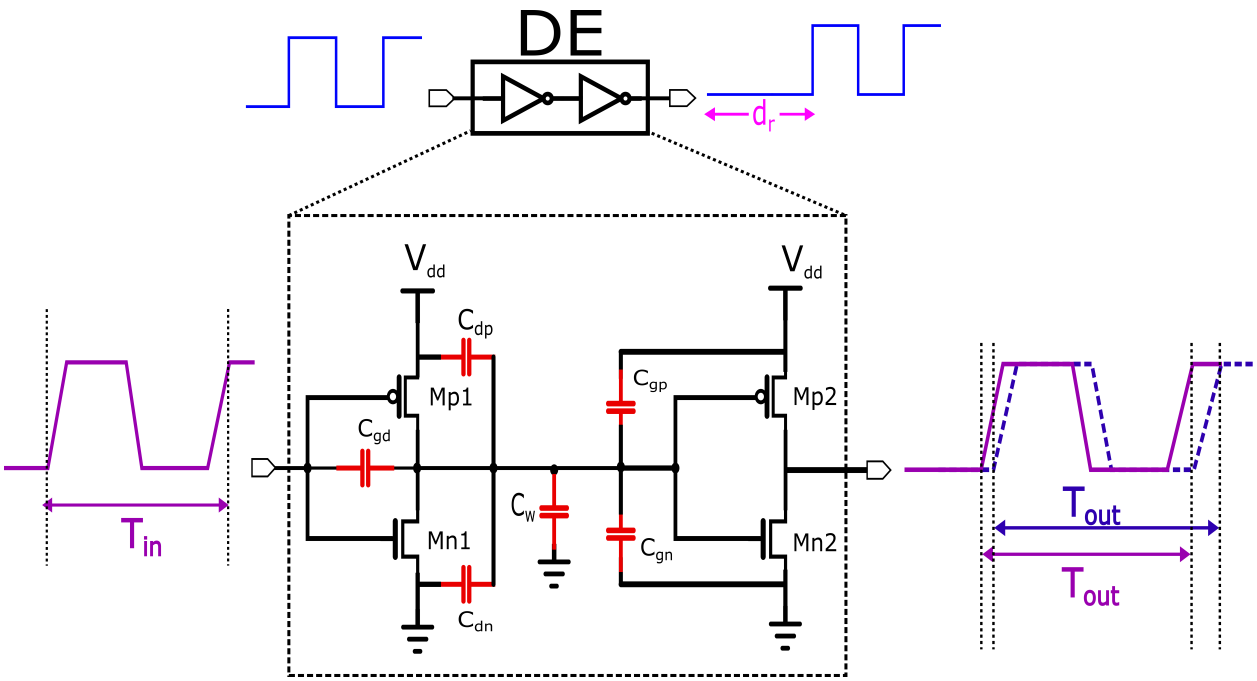


Figure 42: Parasitic model of the delay element with input/output characteristics representing variation in the duty cycle and the propagation delay [28]

4.1.2 Auxiliary block–Multiplexer

The phase tuning block consists of a 6-bit resolution delay line with 64 outputs (2^6). To select different outputs of the delay line, an auxiliary block such as a multiplexer is required in order to utilize the dynamic delay tuning. To select one output out of 64, a multiplexer of dimension 64x1 is used as shown in Fig. 43.

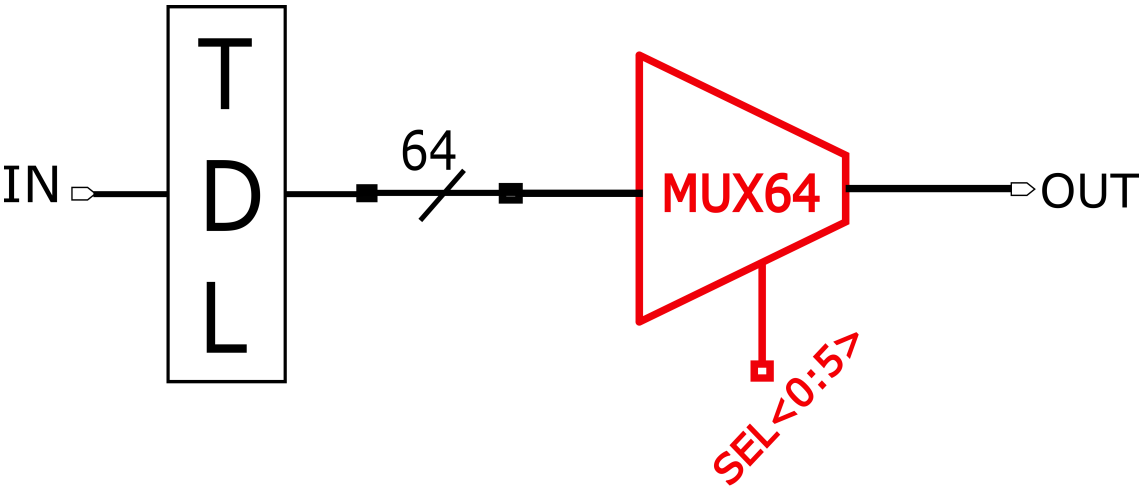


Figure 43: Tapped delay line followed by a 64 x 1 multiplexer having 6-bit select input SEL $< 0 : 5 >$

Firstly, a simple 2x1 multiplexer (MUX) is designed using an inverter and two transmission gates (NMOS/PMOS facing each other). Fig. 44 describes the circuit level design of MUX in which the input signals A or B are selected depending on the select signal S(1 or 0). For S=0, the input signal A is connected to the output F whereas the input signal B is connected when the select signal S is 1. Re-usability of such primitive entities pave the way for higher level designs e.g., Fig. 45 describes the 8x1 multiplexer based on the 2x1 multiplexers. This approach is known as multiplexer tree where the smaller dimension multiplexers e.g., 2x1 MUX are able to accomplish the same function as that of a higher dimension multiplexer. Fig. 46 implies that the 64 x 1 multiplexer can be designed by using few 8x1 MUXs which are basically 2x1 MUX at the bottom of hierarchy.

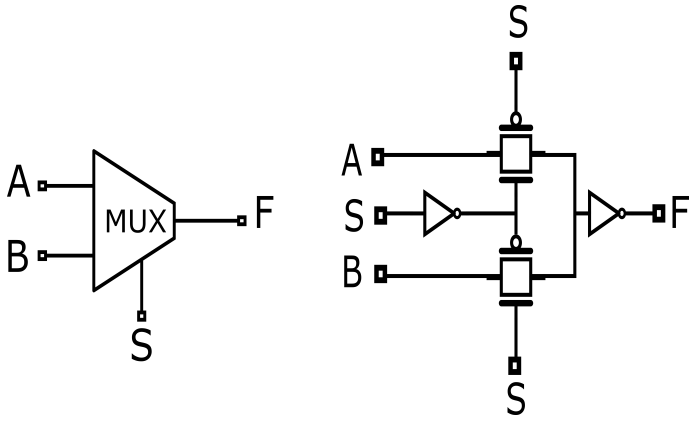


Figure 44: Block diagram of a 2x1 multiplexer along with circuit level design

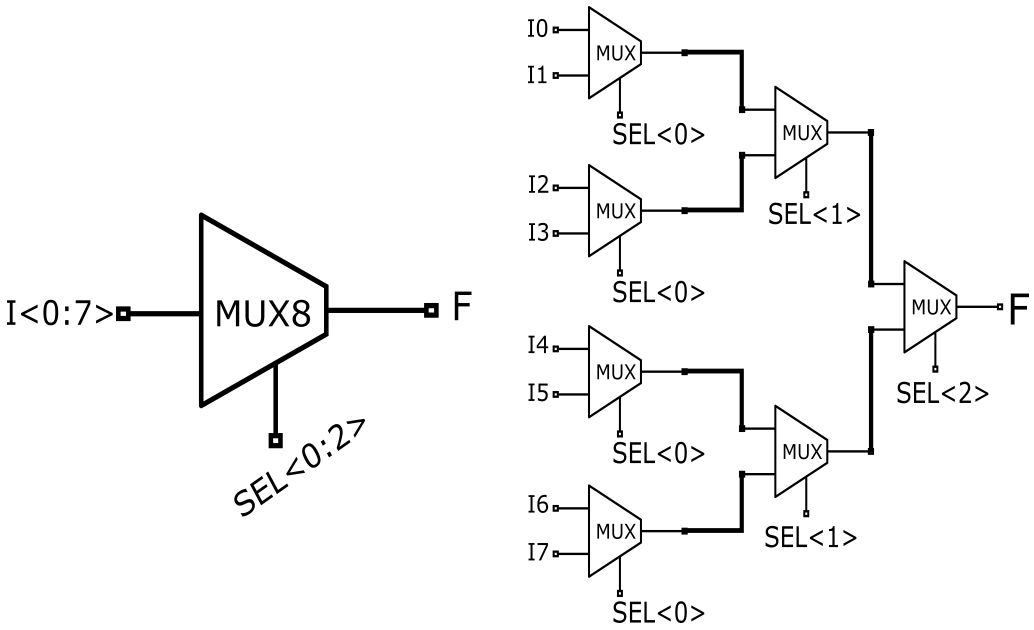


Figure 45: Block diagram of a 8x1 multiplexer based on (2x1) MUX

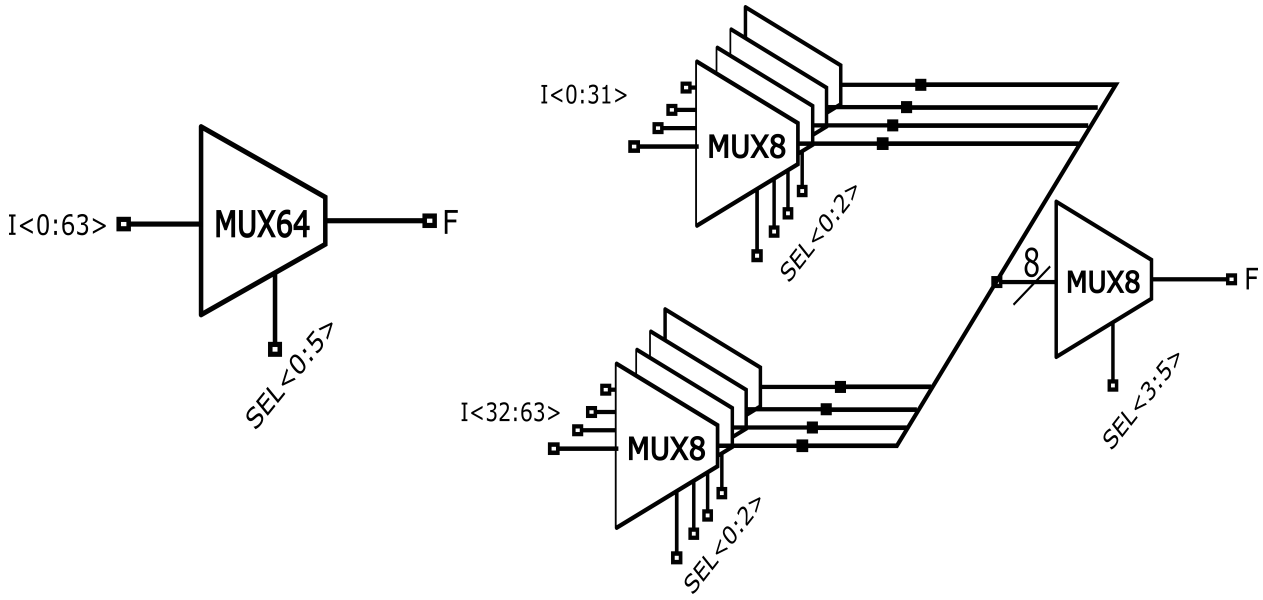


Figure 46: Block diagram of a 64x1 multiplexer based on (8x1) MUX

4.1.3 Simulation results

The design of phase tuning block pours down to the tapped delay line (TDL) and a 64x1 multiplexer as shown Fig. 47. The digital control input (n) allows 6 bit resolution, and selection of 64 delayed versions of the input signal which satisfies the design specifications. The block performance is determined in terms of the the duty cycle (DTC) variations and the propagation delay (PD) across the TDL.

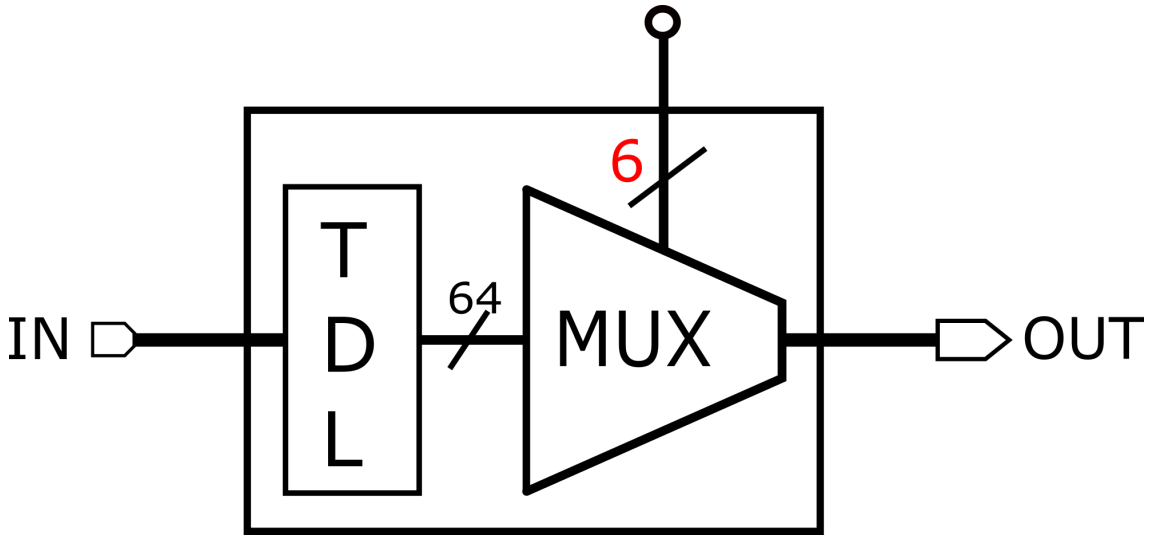


Figure 47: Phase tuning block: A tapped delay line with a 64x1 MUX

A test signal of 2 GHz is applied at the input of the phase tuning block and the 6-bit select input pattern is swept in order to tap each output of the TDL to the output of the MUX. Fig. 48 illustrates the several delayed versions of the input

signal, thus the phase tuning block utilizes its 6-bit digital input. Fig. 49 shows the propagation delay profile where the tapped inputs and the associated delays are plotted against each other. This result indicates that the designed block follows the DCDL transfer function in Eq. 16 which is a linearly increasing function. In addition, the multiplexer logic equally adds a static delay of 100 ps to each tapped input. This static delay does not affect the phase tuning performance unless it varies along the TDL.

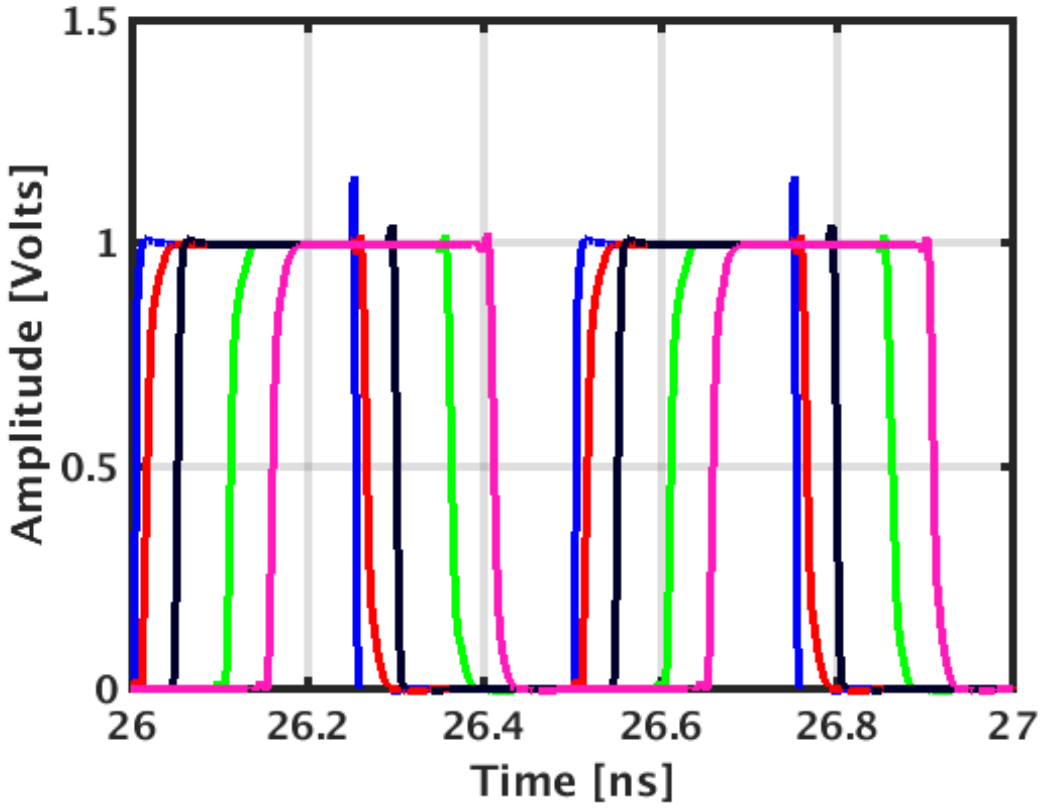


Figure 48: Phase tuning block: Several delay tuned signals

Fig. 50 shows the layout of phase tuning block where the delay chain and multiplexer are bounded by dotted lines. The idea was to consider the area consumption of the block to die total area. Turning to the post layout results, Fig. 51 shows the propagation delay profile where the delay step (d_r) has changed from 10 ps to (12 ps – 16 ps) across the chain. A maximum variation of 4 ps is observed which corresponds to phase variations of 1.5° to 10° in the whole spectrum 1 GHz – 7 GHz. The From Chapter. 3, the phase tuning analysis has shown that the phases can easily withstand such variations.

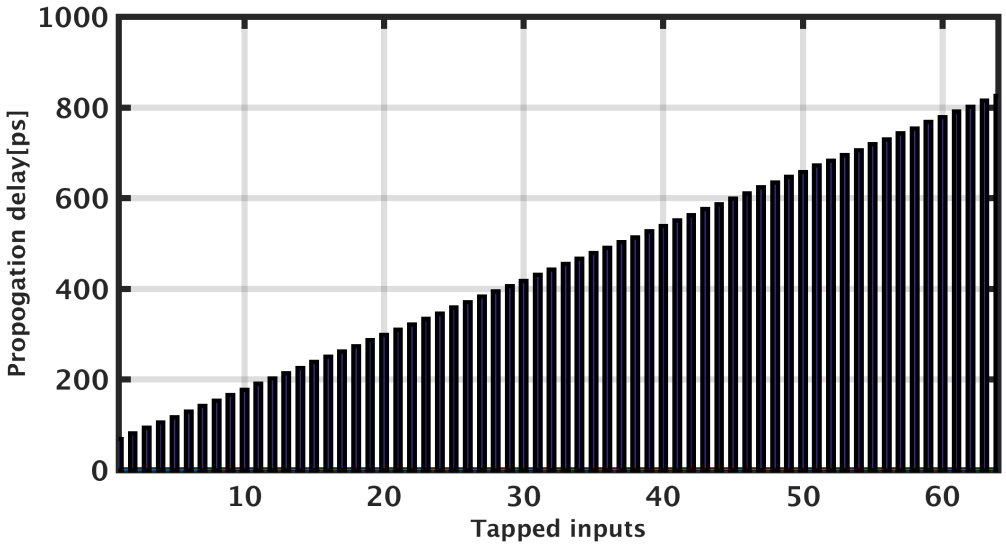


Figure 49: Propogation delay profile of 2 GHz ps (Pre-layout)

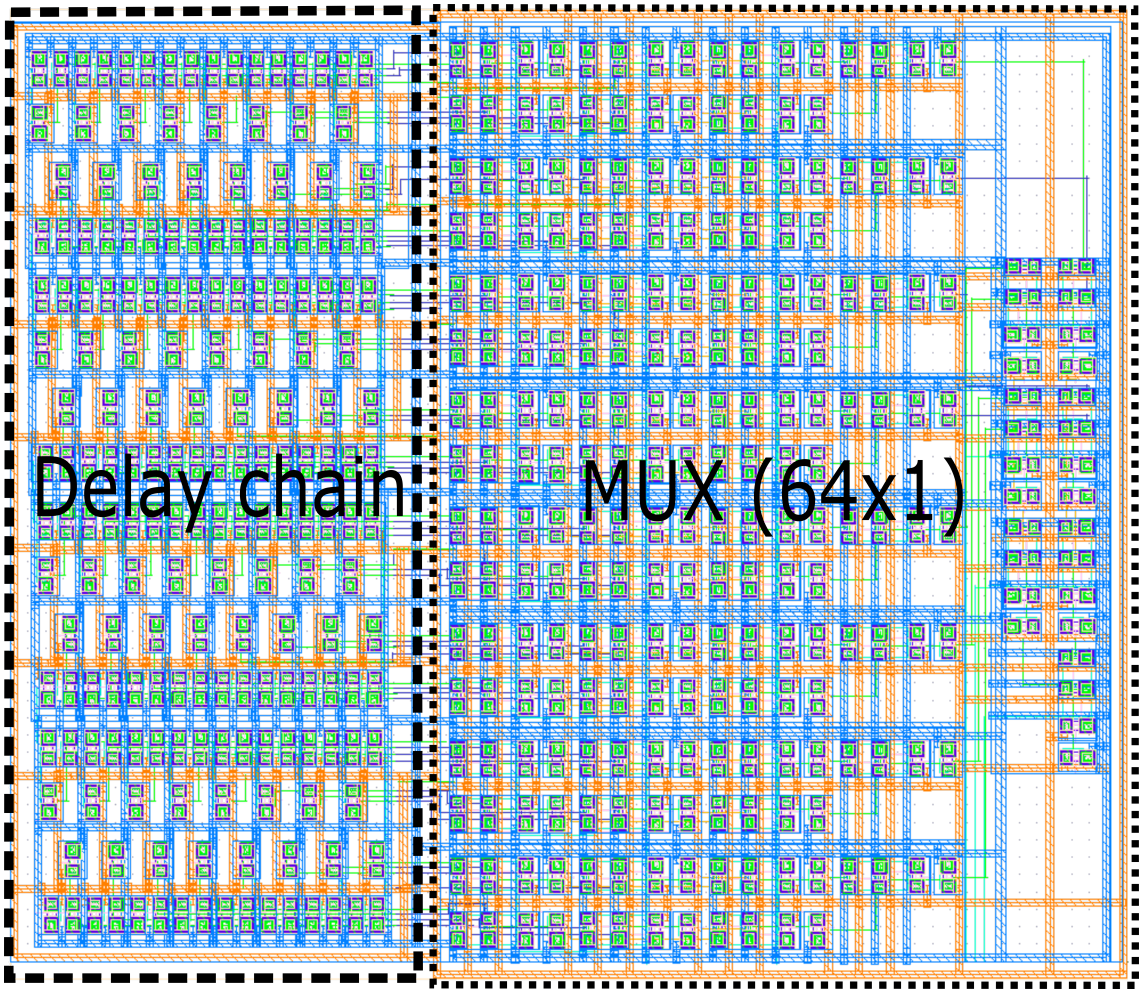


Figure 50: Layout of phase tuning block

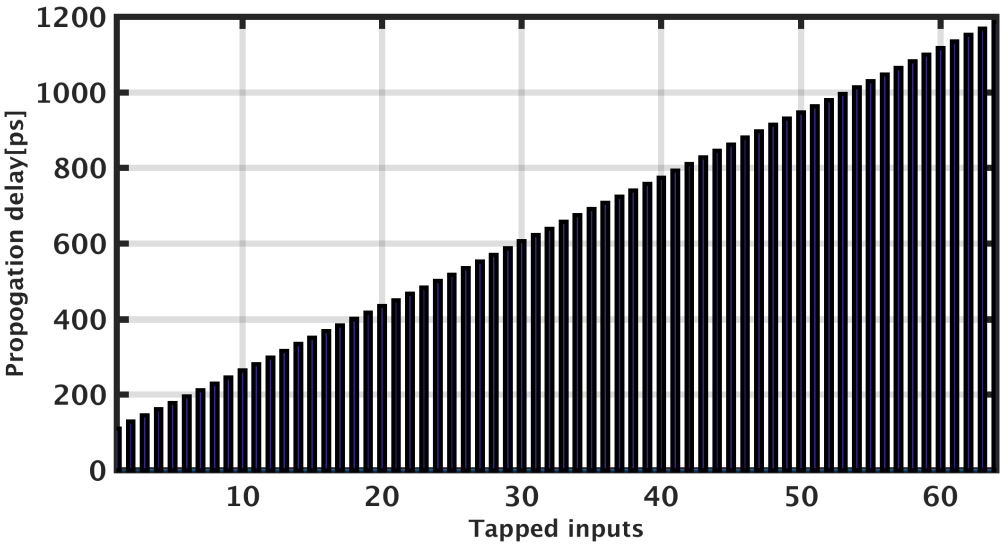


Figure 51: Propogation delay (PD) profile of 2 GHz (Post-layout)

Similarly, the duty cycle variations are evaluated for the 2 GHz signal reference signal having 50% duty cycle. These results are shown in Fig. 52 where DIN and DOUT represents duty cycle of the input and output signals respectively. The post layout simulations compliments the pre-layout results, thus resulting a reliable duty cycle performance.

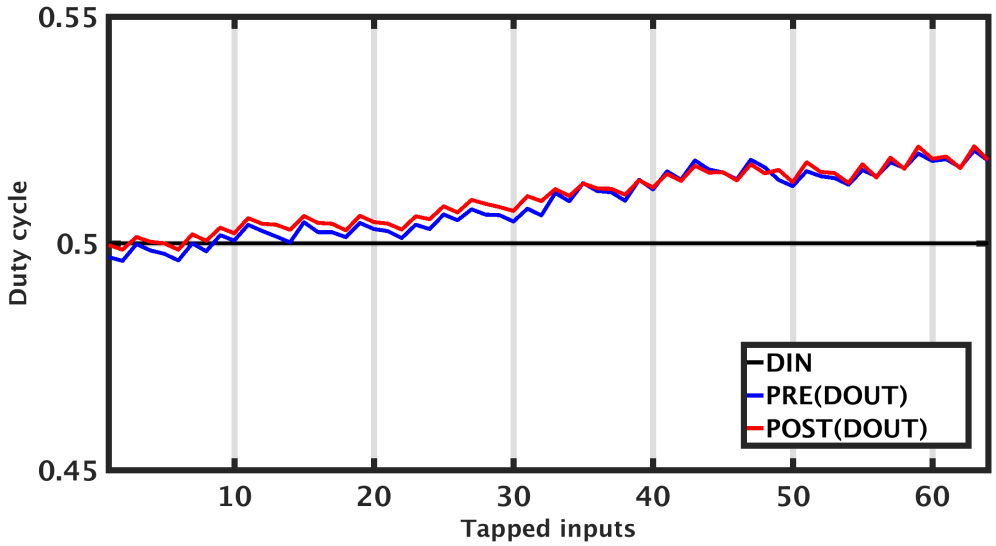


Figure 52: Duty cycle (DTC) profile of 2 GHz (Post-layout)

Now, the phase tuning block is scrutized at other frequencies in the whole spectrum ranging from 1 GHz–7 GHz as it will give deep insight about the tuning block performance. Especially, the propagation delay profiles and the duty cycle variations are plotted against the tapped input for the whole range of frequencies illustrated in

Fig. 53 and Fig. 54. From the system propagation delay profile, it follows that the delay profile is linearly increasing at other frequencies as well. On the other side, the duty cycle performance gradually deteriorates along the chain at higher frequencies. It is clear that the duty cycle varies between 50% – 56% across the tapped inputs in the whole spectrum. The specications of phase tuning block are tabulated in Table. 1.

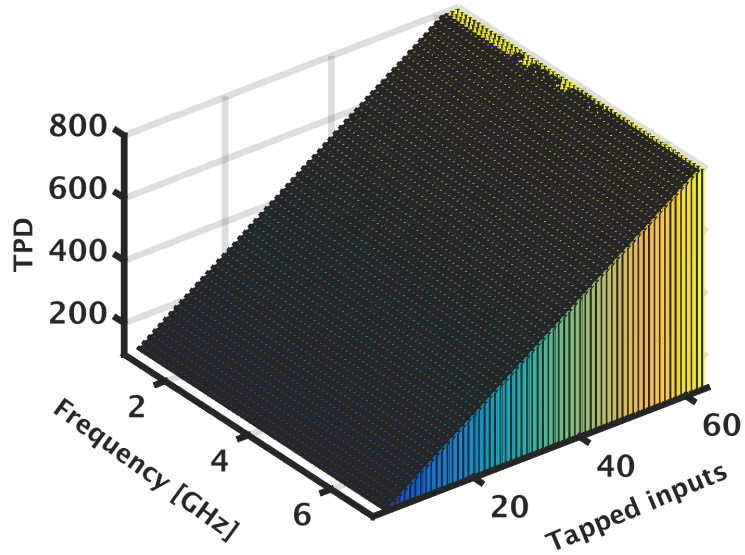


Figure 53: Propogation delay (PD) profile of phase tuning block

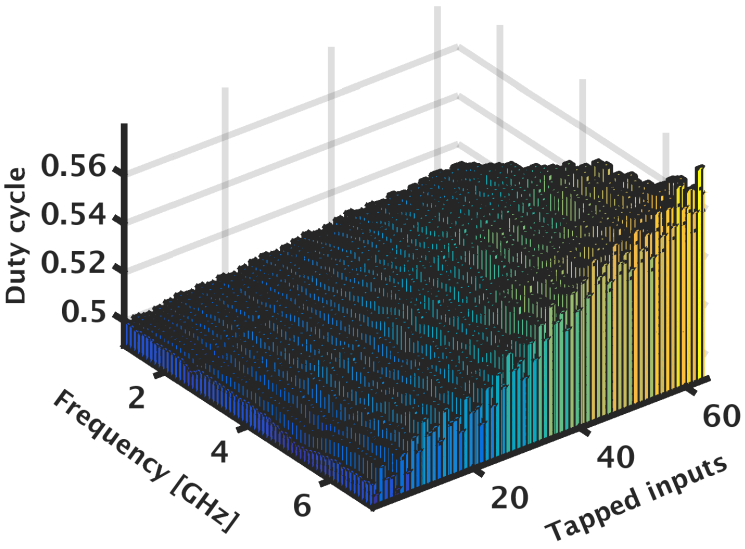


Figure 54: Duty cycle profile of phase tuning block

Duty cycle (DOUT)	$50\% - 56\%$
Delay range (DR)	826 ps
Area	$3500\mu m^2$
Power consumption	2 mW @ 2 GHz
Process variations	DOUT (μ,σ): 52%, 4%
	DR (μ,σ): 826 ps, 1.8 ps

Table 1: Phase tuning block performance at 2 GHz where μ and σ denote mean and standard deviation respectively.

4.2 Amplitude tuning block

In the tuning system, the amplitude tuning block follows the phase tuning block in order to scale the amplitude of the antenna feeds. This block has two main objectives: the amplitude scaling of the phase tuned signal and driving of the antenna as a load. Fig. 55 shows the block level diagram of the amplitude tuning system where these objectives are accomplished with a low-drop out regulator (LDO) and a power amplifier (PA). The block operates by taking the digital input (m) which enables the LDO to generate several scaled versions of output voltage (V_{tune}) which in turn regulates the supply of the PA.

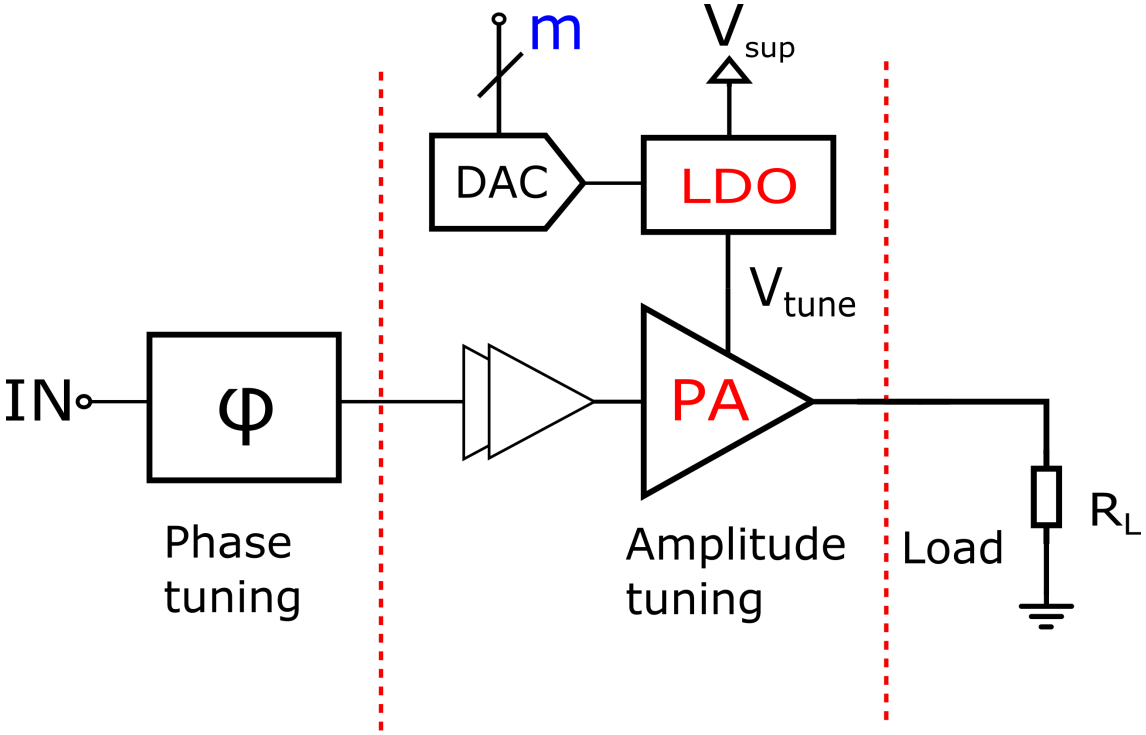


Figure 55: Amplitude tuning block consisting of an LDO and a PA

Turning to the design requirements, the amplitude tuning range is the major factor dictating the design of each individual block i.e., the PA and the LDO. From the Fig. 22 on Page 18, the amplitude ranges from 0.1 to 0.9. Therefore, it is required

that the LDO should regulate the PA supply in such a way the that the PA output voltage conforms to this specification. This requirement affects the PA design as the PA power tuning range is given by the following expression where the load resistance of 50Ω results into 9 dB tuning range.

$$\frac{0.1^2}{2R_L} < P_L < \frac{0.9^2}{2R_L} \tag{19}$$

4.2.1 Power amplifier (PA)

A highly efficient PA is always desired. Though several PA classes are available, the non-linear or switching PAs ideally provide 100% efficiency. Especially, the class-D PA which has 100% efficiency along with maximum output power capability [29]. The class D PA is an inverter based switching PA where the two transistors PMOS and NMOS are turned on and off like switches as shown in Fig. 56. Each transistor is in the on-state for half of the time period of the input signal where as the other is off during that interval. These switches periodically connect the PA supply voltage (V_{tune}) to the output load resistance (R_L) resulting into a square output voltage (V_L) with peak value equal to supply voltage (V_{tune}).

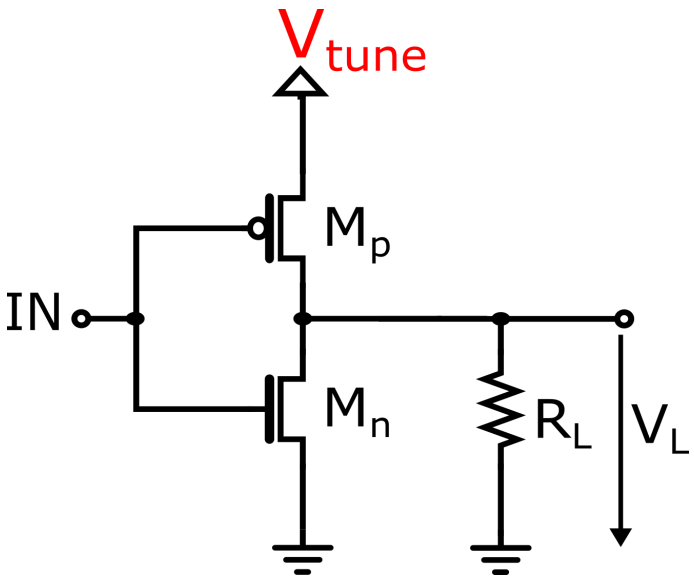


Figure 56: Schematic of the class D power amplifier

To begin with the input signal which is a square wave coming from the phase tuning block. This signal amplitude is scaled by varying the supplying voltage (V_{tune}). Based on the tuning range specifications, the voltage (V_{tune}) range is initially considered from 0.1 V – 1 V. The PMOS (M_p) and NMOS (M_n) are 1 V transistors. Their dimensions are chosen in such a way that the on resistance of the PMOS is around 50 Ω – 60 Ω. The PA properly works when the input signal is high (1) and the lower switch is on. However, it malfunctions for the low input signal (0) as the voltage (V_{tune}) drops below the threshold voltage (V_{tp}) of the PMOS, thus turning it off even when it should be on. Moreover, the change in supply voltage

also affects the threshold voltage of the PMOS. Therefore, the minimum value of the voltage (V_{tune}) should be greater than the threshold voltage (V_{tp}), e.g., 0.8 V is a reasonable, assuming the threshold voltage (V_{tp}) is 500 mV. Now the lower limit of V_{tune} is 0.8 V. The upper limit of 1 V should accordingly change in order to provide the scaling of load voltage (V_L). Now, the V_{tune} has a new range from 0.8 V – 1.8 V. This range affects the transistor specifications as it require 1.8 V transistors.

After selecting the proposed tuning range, the class D PA input is excited with a 2 GHz square wave signal to analyze the amplitude scaling effect at the PA output. Fig. 57 shows the output voltage response of PA for sweeping of voltage V_{tune} from 0.8 V – 1.8 V. The PA power tuning range is around 10.8 dB as shown in Fig. 58

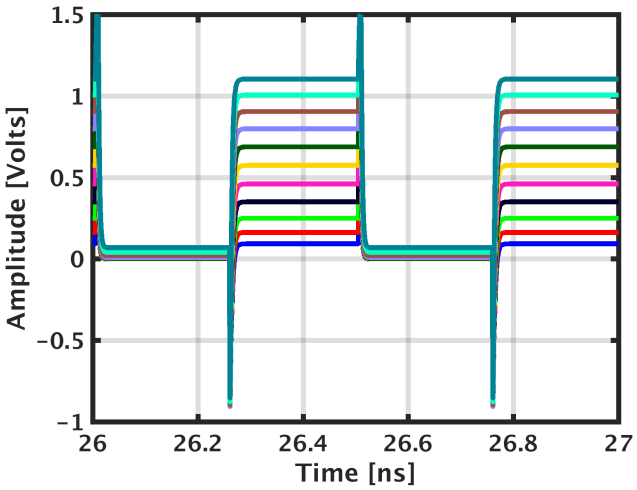


Figure 57: Supply regulation ($0.8 < V_{tune} < 1.8$) provides amplitude scaling of PA output signal from 0.1 V – 1.1 V

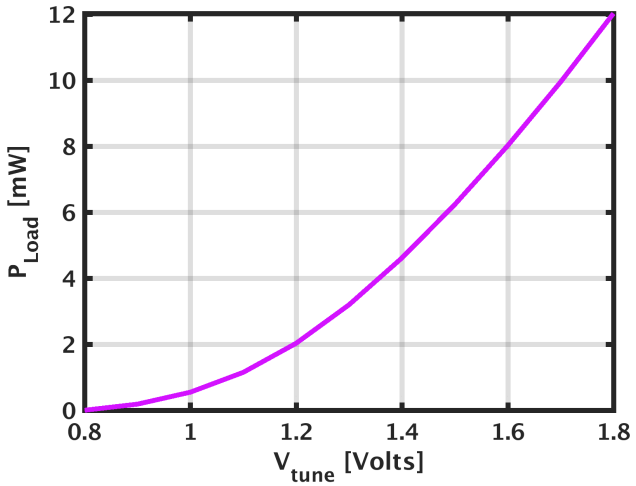


Figure 58: Load power of PA for various supply voltages

4.2.2 Low Drop-out regulator (LDO)

Fig. 59 show the schematic diagram of low drop-out out regulator (LDO) which regulates the PA supply voltage (V_{tune}). It consists of a PMOS transistor and a voltage divider network in the negative feedback loop ensuring stable operation. The current (I_{BIAS}) represents the current consumption of the following blocks such as the PA. Fig. 60 illustrates the LDO characteristics , the interested region is the drop out region where the PMOS device acts as resistor having on resistance (R_{on}). The current through the PMOS (I_{PMOS}) defines the dropout voltage (V_{drop}) given by

$$V_{drop} = I_{PMOS} \times R_{on} \tag{20}$$

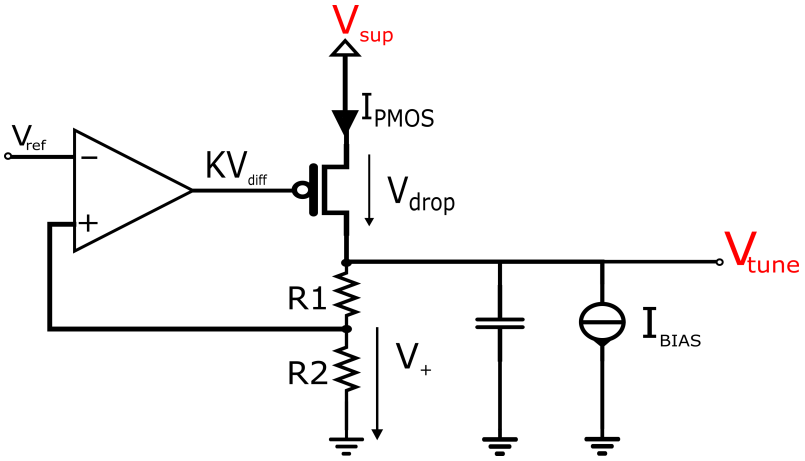


Figure 59: Schematic of the low dropout regulator (LDO)

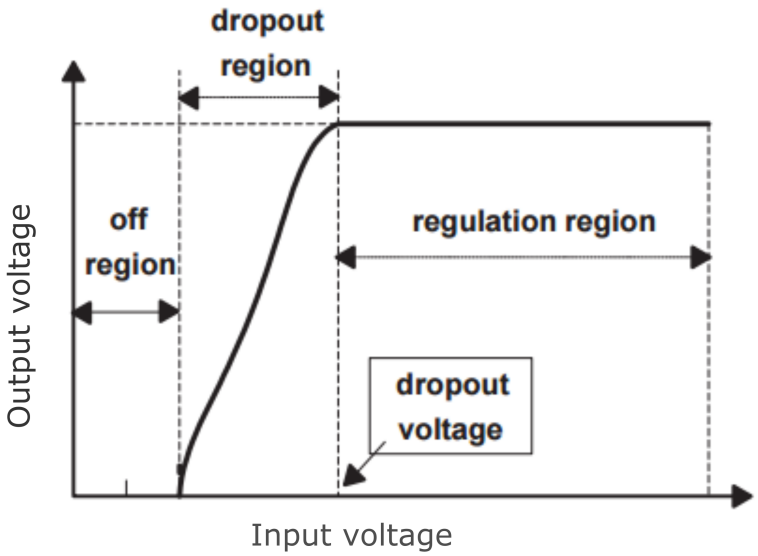


Figure 60: Input/output characteristics of an LDO [30]

The current (I_{PMOS}) creates voltage reference across resistance (R_2) and the non-inverting input of operational amplifier. This in turn drives the gate of PMOS with voltage difference (KV_{diff}) where K denotes the gain of the amplifier. The operation of the LDO can be inferred from the node equations described in Eq. 21– Eq. 23. The Eq. 25 indicates that the output voltage (V_{tune}) follows the input reference voltage (V_{ref}) for large value of resistance $R2$ assuming a constant input voltage (V_{sup}) of the LDO.

$$\mathrm{V_g = KV_{diff}\,(V_+ - V_{ref})} \tag{21}$$

$$\mathrm{V_{tune} = I_{PMOS}\,(R1 + R2)} \tag{22}$$

$$\mathrm{I_{PMOS} = g_m V_{SG} = g_m(V_{sup} - V_g)} \tag{23}$$

Simplifying the above equations for V_{tune}, assuming $g_m R2 >> 1$:,

$$\mathrm{V_{tune} = \frac{Kg_m(R1 + R2)}{Kg_m R2} V_{ref} + \frac{g_m(R1 + R2)}{1 + Kg_m R2} V_{sup}} \tag{24}$$

$$\mathrm{V_{tune} \approx (1 + \frac{R1}{R2}) V_{ref} + \frac{(1 + R1/R2)}{K} V_{sup}} \tag{25}$$

The desired range for the voltage (V_{tune}) is 0.8 V – 1.8 V. To achieve this specification, an ideal 3-bit digital to analog converter generate different reference voltages (V_{ref}), thus enabling LDO to provide V_{tune} in the range 0.75 V – 1.58 V as shown in Fig. 61 and Fig. 62. The LDO output contain ripples corresponding to variations in the output bias current assuming the voltages V_{sup} and V_{ref} are resilient to supply variations. These ripples can be significantly reduced by increasing the open loop gain (K) or using a large capacitor at the output.

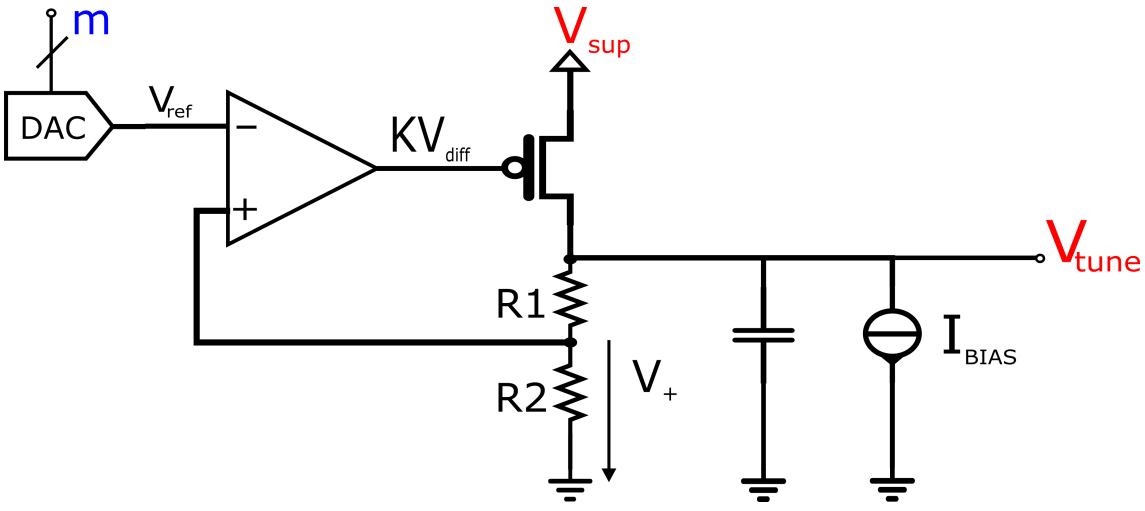


Figure 61: The LDO incorporating a 3-bit DAC

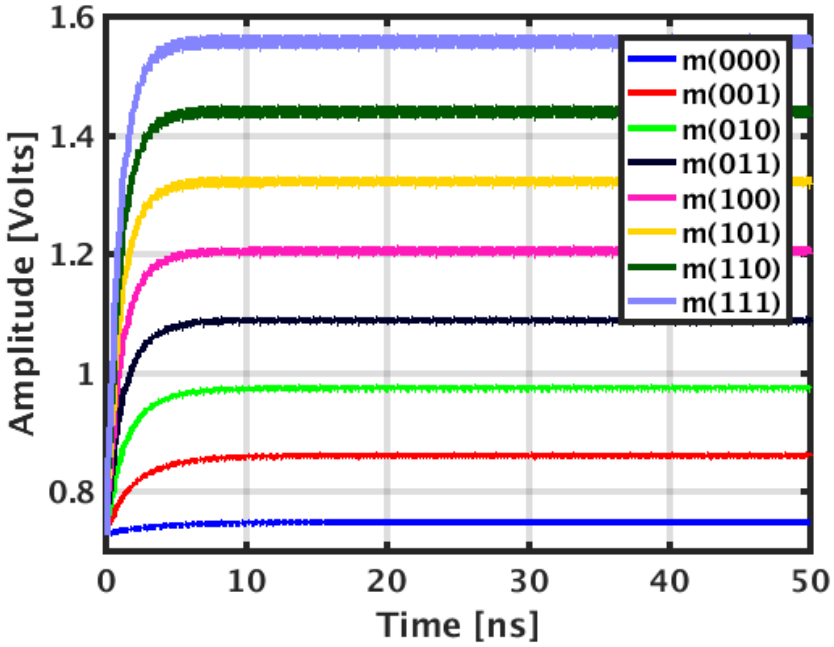


Figure 62: Different versions of LDO output voltage (V_{tune}) for a 3-bit digital control

4.2.3 Simulation results

Fig. 63 shows the block level diagram of the amplitude tuning block. A test signal of 2 GHz is applied at the input of the block with the digital input (m) varying from 000 – 111. Since the LDO provides 0.75 V – 1.58 V output rather than 0.8 – 1.8 V, Fig. 64 shows the associated voltage drop in the block output as compared to Fig. 57

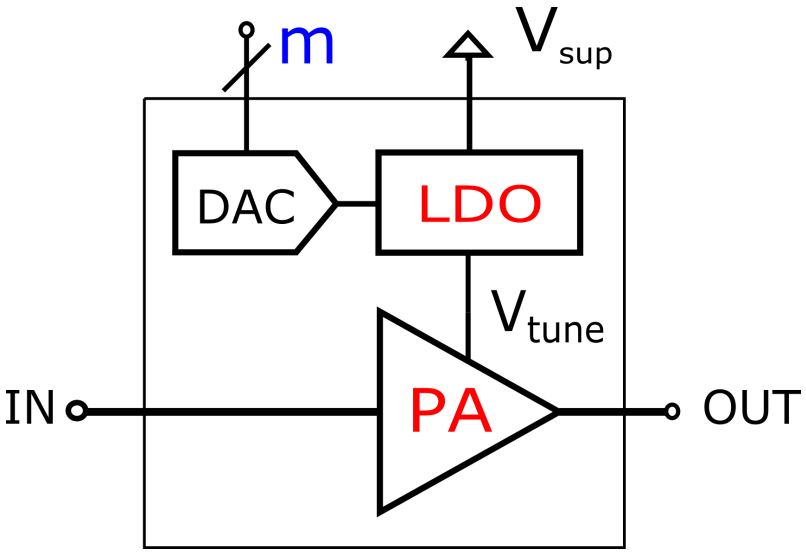


Figure 63: Block diagram of amplitude tuning block

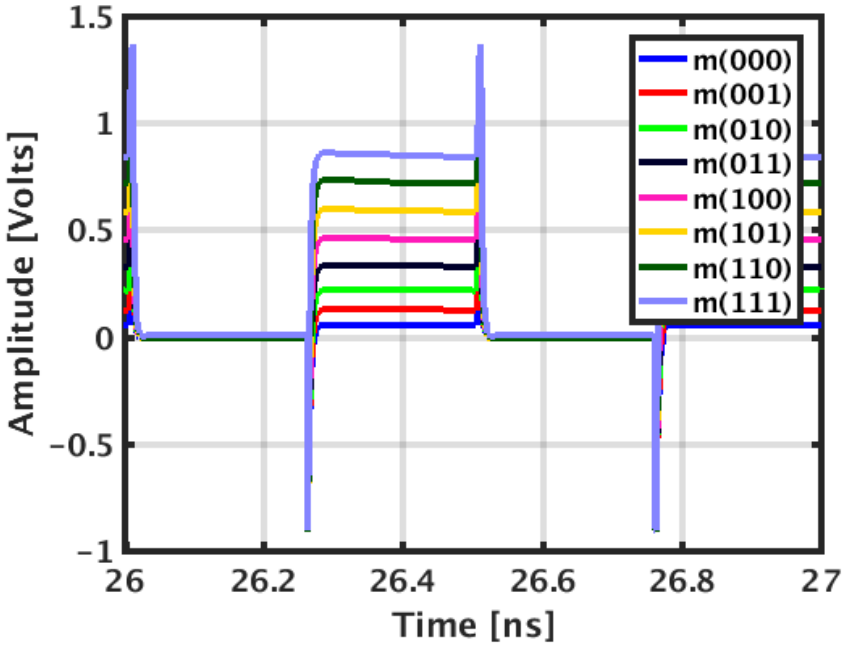


Figure 64: Output response of amplitude tuning block

4.3 System simulations

After designing the individual blocks, the amplitude and phase tuning blocks are connected to a 50 Ω load as shown in Fig. 65. Fig. 65 shows two different output voltages (V_{OUT}) with different amplitude scaling and delay tuning. The 3-amplitude tuning bits used are "111" and "100" illustrating 0.8 V and 0.4 V square wave signals. In the same way, the 6-phase tuning bits were chosen: "000001" pattern represents delay by 10 ps whereas "010111" maps to 230 ps i.e., delayed approximately half of the period for a 2 GHz input signal.

Similarly, the whole tuning system was calibrated to 2 GHz where the feeding signal amplitudes and phases are tuned based on the digital inputs "m" and "n" respectively as shown in Fig. 67. The Table. 2 tabulates the weighted signal amplitudes (A), phases (P), delays (D) along with associated digital inputs (m , n). Based on the settings, the tuning system generates four feeding signals with required amplitude and delays plotted in Fig. 68. When the antenna feeds are excited with weighted signals, a maximum output power is delivered at the desired frequency.

Signals	Amp.	Phase (°)	Delay(ps)	m	n
Feed 1	0.6	160	222	101	010111
Feed 2	0.1	340	472	001	101111
Feed 3	0.7	90	125	101	001101
Feed 4	0.4	0	0	100	000000

Table 2: Tuning system calibration settings at 2 GHz

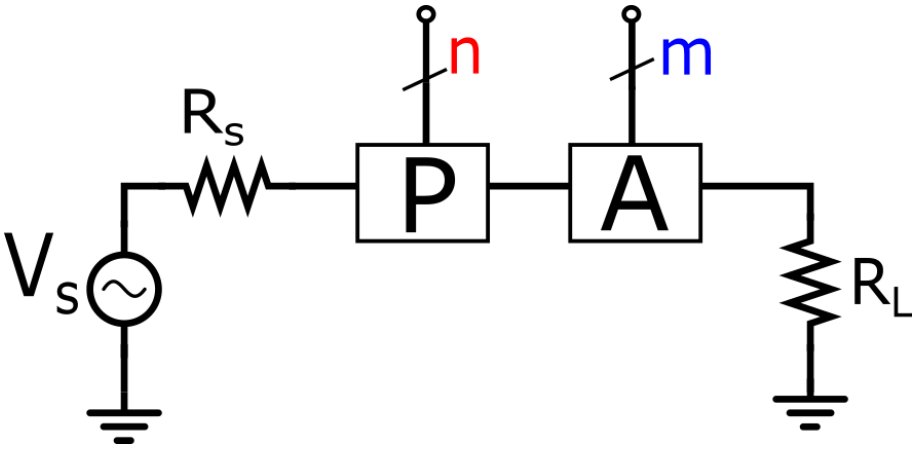


Figure 65: Amplitude and phase tuning

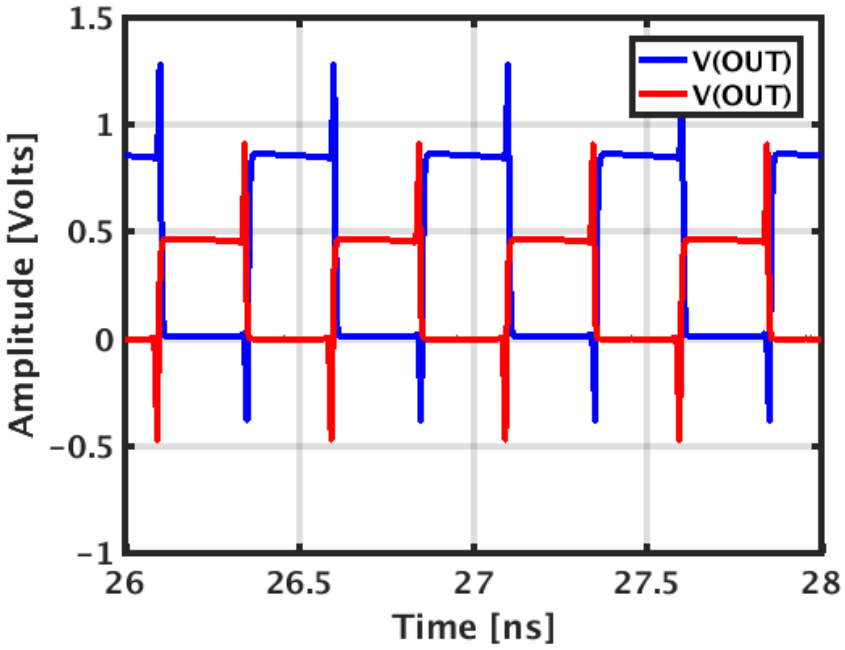
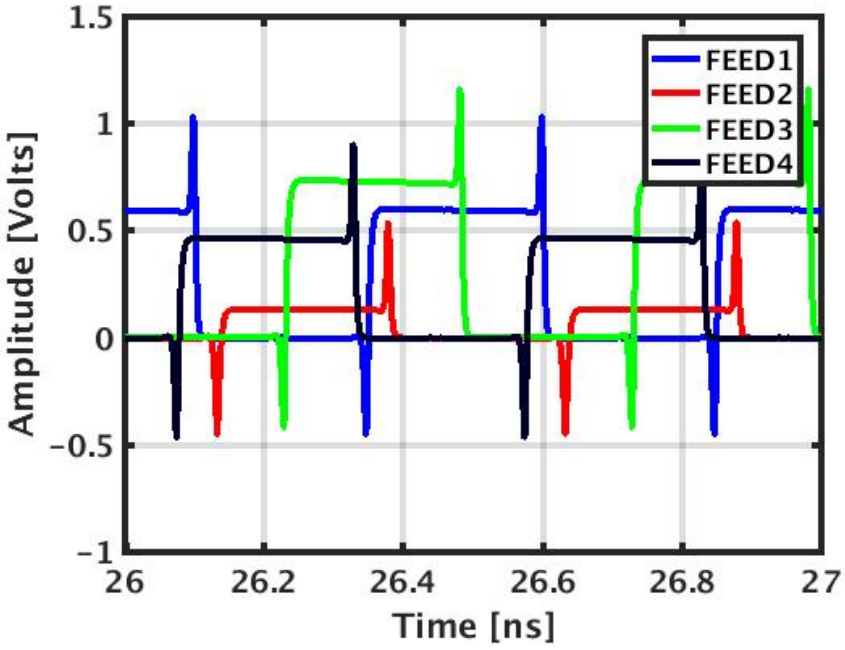


Figure 66: Example of amplitude and delayed tuned signals with different control bits "m" and "n"



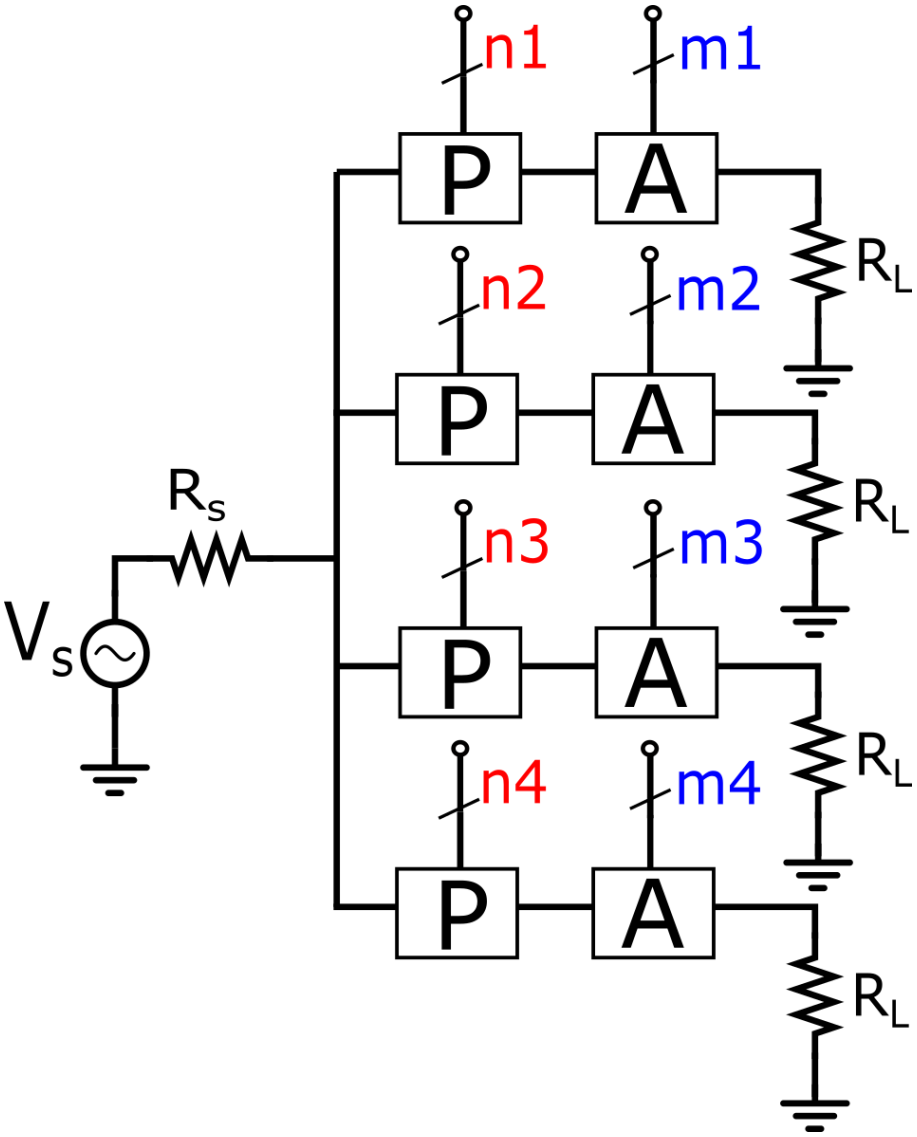


Figure 67: 4-port tuning system

Fig. 69 shows the antenna tuning performance at 2 GHz along with the ideal profile. In ideal case, the antenna exactly tunes to 2 GHz, however, the IC design results into a shifted tuning profile at 1.7 GHz. There are mainly three reasons for this shifted tuning: Firstly, the excitation signals are pulses rather than ideal sinusoidal excitations. These pulses have DC offset which causes mismatch in the amplitude of the feeds, thus translating the antenna tuning. Moreover, the pulse signals contain odd harmonics e.g., a third harmonic contributes at 5.1 GHz. Secondly, the output impedances of four PAs are acting as source impedances which vary around 50 Ω – 60 Ω instead of constant 50 Ω in comparison to ideal sources. Finally, the isolation of PAs should be kept in mind as the PAs directly drive the antenna feeds.

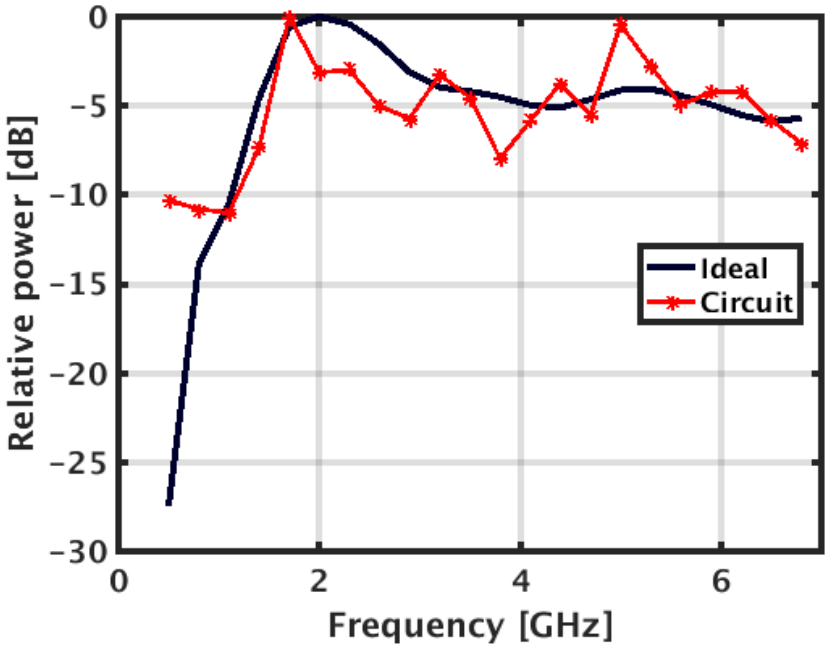


Figure 69: Comparison of power profiles at 2 GHz

4.4 Summary

- The tuning system comprises of four phase tuning blocks followed by four amplitude tuning blocks. These blocks are directed with digital inputs (m,n)=(3,6).
- The phase tuning block is composed of a 6-bit tapped delay line (TDL) and a 64x1 multiplexer to tap 64 outputs of TDL. Its performance is characterized by two factors: the duty cycle and the propagation delay.
- The amplitude tuning block contains a class D power amplifier and a low drop-out regulator. The LDO regulates the supply of PA in order to scale the amplitude. In addition, the LDO is digitally controlled with 3-bit an digital to analog converter (DAC).
- The 4-port tuning system is simulated at 2 GHz. The simulation results demonstrate that the tuning objective is achieved at a slightly different frequency. This difference is due to various reasons including the type of excitation, variation in source impedances and isolation issues.

5 Conclusion

In this thesis, an integrated transmitter circuit solution is proposed to tune the multiport reconfigurable antenna. The antenna tuning is based on novel technique where antenna feeds are excited with certain amplitudes and phases, thus tuning the antenna at the desired frequency. Currently, the area of discrete electronics does not provide feasible solution for dynamic weighting or scaling of antenna feeds (amplitude and phase). Therefore, the system on chip (SoC) solution approach was considered.

The weighted signal characteristics were studied using the tuning analysis framework which was especially developed in order to extract the important specifications for the integrated circuit. These specifications were related to accuracy of the on chip generation of weighted signals. Based on the analysis, the amplitude and phase scaling resolutions were 3 bits and 6 bits respectively. The integrated circuit design mainly focused on the tuning system design in 28 nm CMOS technology enabling signal amplitude and phase scaling. The tuning system contains two subsytems: the phase tuning block and the amplitude tuning block. The phase tuning block includes a tapped delay chain which provides dynamic phase tuning with 6-bit resolution. In phase tuning block, the critical parameters are delay range and duty cycle providing deep insight about the phase tuning performance. The phase tuning block has a delay range of 830 ps with duty cycle variations of 50%–56% in the whole spectrum. In the amplitude tuning block, the low dropout regulator (LDO) and power amplifier (PA) provides amplitude scaling feature. The LDO incorporates a 3-bit DAC in order to generate several scaled versions of the output voltage. The LDO input is a constant 2.5 V supply whereas its output voltage ranges from 0.75 V–1.58 V. This output voltage regulates the supply of class D PA which ultimately scale the amplitude of PA output signal. The PA output signal scales from 0.1 V – 0.86 V. The designed tuning system needed 4 amplitude tunig blocks and 4 phase tuning blocks as the antenna under consideration was 4-port. A test signal of 2 GHz was applied to the tuning system where all the amplitude and phase tuning blocks were calibrated to 2 GHz settings. The simulation result validates the novel tuning concept with a difference that the tuning is achieved at 1.7 GHz. This divergence results from the non-ideal excitations, output impedance variations and isolation issues.

To conclude, the major tasks were the development of the tuning analysis framwork and the design of tuning system in general. I have already completed the layout of phase tuning block. However, the amplitude tuning block requires further modifications and post layout simulations. Though the concept is currently verified at 2 GHz, the next task is to determine the tuning performance at other frequencies in the spectrum 1 GHz – 7 GHz. Overall, the on chip mulitport antenna tuning is a promising concept with a significant demand for further research, including the fully functional digital transmitter design along with the proposed tuning system.

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