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Thermal Analysis, Parasitic Extraction, and Wirebond Reliability Studies of

Power Electronic Modules

Thermal Analysis, Parasitic Extraction, and Wirebond Reliability Studies of Power Electronic Modules.

A thesis submitted in partial fulfillment
of the requirements of the degree of
Master of Science in Electrical Engineering

By

Shilpa Prabhudeva
Visveswaraya Technological University
Bachelor of Engineering, 2011

December 2014
University of Arkansas

This thesis is approved for recommendation to the Graduate Council.

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Committee Member — Committee Member

ABSTRACT

This thesis research investigates thermal performance, parasitic extraction and wirebond/encapsulation reliability of power electronic modules. Thermal performance is critical to the power electronic modules. As such, thermal analysis is an important part of the power electronic module design process. Several cases are studied on generalized power modules with a full bridge layout. A database is built based on these results. The studies are performed using SolidWorks thermal simulation tool. The database involves several parameters such as power dissipation, maximum junction temperature, ambient temperature, convection coefficient required to cool the module, size of the baseplate, heat-sink size, substrate size, spacing between dies, and different materials that can be used for the power electronic module. Using this database, procedures to select appropriate parameters in a thermally efficient layout for the power electronic modules are illustrated using examples. It was found that, for optimum performance, ΔT (maximum junction temperature – ambient temperature) should be greater than 125°C for power modules with medium and high power dissipation. Also, for a low ΔT and high power dissipation, baseplate acts more like a thermal resistance than a heat-spreader. Hence, it is ineffective to employ base-plates for these cases. Increasing substrate size to bring down maximum junction temperature is more effective in higher power dissipation cases than those for medium or low power dissipation.

Parasitic extraction for an electronic power module using a time domain reflectometry (TDR) method in the form of differential inductance waveforms was developed. These measured parasitic inductance and parasitic capacitance are compared with the parasitic parameters extracted using a Q3D extractor software. The accuracy of the measurement results from these two different approaches is studied in detail.

Reliability of wirebonds in the case of encapsulated and un-encapsulated power modules were investigated by subjecting them temperature cycling from -55°C to 250°C. It was found that the solder flux affected the reliability of the wirebonds. As such, it is recommended that the power connectors on the power substrate should be free of flux, as the residual solder flux can affect the nearby wirebonds in the power modules. As expected, the differences in the coefficients of thermal expansion between the power substrate bond wires and encapsulation affect the reliability of the wirebonds. Large diameter wirebonds tend to be stronger and can withstand the stress and strain created by the different material systems in the power electronic modules.

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CHAPTER 1. INTRODUCTION

Power electronic module is an optimal compact package of a circuit which includes multiple power semiconductor devices (MOSFETs, diodes, IGBTs etc.), and sometimes along with passives (resistors, and capacitors etc.) and their control circuitries. These power modules are later integrated into a corresponding power electronic system which performs a specific function. Power electronic modules are widely used in various home and industrial applications like automobiles, motor controllers, power supplies, robotics, air conditioners, refrigerators, continuous power distribution systems, etc.

A power module design is optimized before fabrication; to provide for size and weight reduction, lower parasitic, thermally optimum, higher efficiency and improved performance. Trade-off between cost and reliability is the major factor that affects designing of power electronic systems. Since individual packages are not required for power semiconductor devices; and all power semiconductor devices can be incorporated into a single package, power electronic modules should provide for high reliability with lower cost and smaller size.

The first step in the power electronic module design is to choose an appropriate topology. Once this is done, the module is designed using Q3D software manually or using a layout designing software tool. This designed virtual module is subjected to thermal and parasitic simulations to optimize the design.

Thermal simulations can be performed using the SolidWorks software. These simulations provide the maximum junction temperature for module designed for certain parameters. The operating parameters and design are varied until a maximum junction temperature (for example, 250°C) is achieved. This thermally optimized design is later subjected to parasitic simulations

using Q3D software to re-optimize the module with respect to parasitics. This design for layout is later fabricated using several fabrication processes and tested.

1.1 Thermal Analysis

Several design parameters such as power dissipation, maximum junction temperature, and convection coefficient affect the performance of a power electronic module. Hence, it is very crucial in selecting appropriate parameters while designing a layout. Usually trial and error methods are employed when layout is designed manually. This is a very tedious and time-consuming process. Even when a layout is designed using computer aided design tools, most of these parameters should be provided by the designer initially to the designing software.

This thesis aims to provide a "rough" database that predicts the thermal behaviors of the module for several different parameters. When designers use this database to select their parameters, module behavior becomes predictable to a good extent. Thermal analysis is performed on a generalized module using SolidWorks software, and their results are represented in a way that helps in choosing parameters. This is shown in Chapter 3. Chapter 3 also provides a few examples which demonstrate the parameter selection procedure.

1.2 Parasitic extraction of power modules

Parasitic analysis is performed on a virtual power module before fabrication for electrical characterization. However for verification purposes, it is also required to extract parasitic from a fabricated module. Chapter 4 develops the physical extraction of parasitic inductances using a time domain reflectometry (TDR) method.

1.3 Reliability of wirebonds

Temperature cycling can reveal failures associated with the mismatches of coefficients of thermal expansion of different material systems in the power electronic modules. Thermal cycling of power electronic module is performed from -55ºC to 250ºC using a daisy-chain wirebond and results/behavior of the modules with encapsulation and without encapsulation is compared.

1.3 Chapter Organization

This thesis is organized into six chapters. Chapter 1 introduces the objectives and rationales behind research work. Chapter 2 discusses the background concepts. Chapter 3 discusses results from the thermal analysis of a power electronic modules. Chapter 4 develops the parasitic extraction measurements using the time domain reflectometry method. Chapter 5 presents the thermal cycling results of power electronic modules with and without encapsulation. Chapter 6 concludes the thesis.

CHAPTER 2. BACKGROUND CONCEPTS

2.1 Heat transfer in power modules

Heat transfers between solids when they are in contact. As heat transfers through several layers in series thermal resistivity increases, thus decreasing the heat-transfer rate. Similarly, as heat transfers through layers in parallel, thermal resistivity decreases, thus increasing the heat-transfer rate.

In a power electronic module, there are several layers in series – like die, direct bonded copper substrate, solder, baseplate – and heat-sink is normally considered to be in parallel due to fins. Hence, a complex structure of several layers in series and parallel need to be considered to calculate the total thermal resistance of the complete structure.

Heat is dissipated by power semiconductor dies in the power electronic module and in a multiple chip module where several power semiconductor dies dissipate power, thermal coupling takes place. This further increases maximum junction temperature of the power electronic module. This in-turn demands a better cooling system. To increase the efficiency by increasing heat-transfer rate would place the power semiconductor dies far apart that heat-dissipated by one power semiconductor die does not couple with that of the other.

The calculation shown below is an example for a minimum distance between two power semiconductor dies to avoid thermal coupling completely before a heat-sink is attached. Figure 2.1 shows the several layers of a typical power electronic module.

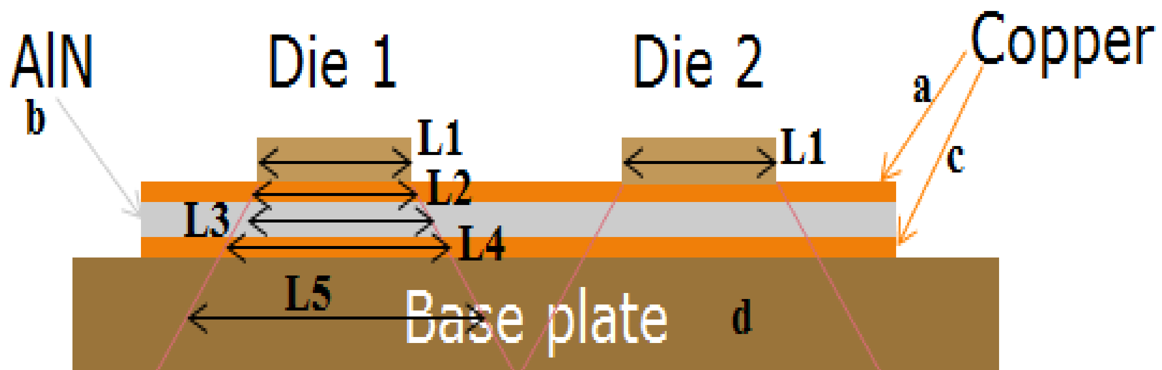


Figure 2.1: Layers in power module (solder layer is neglected)

Power semiconductor die is placed on the DBC substrate (copper, AlN, copper) and baseplate. Since the solder layer is very thin and when an ideal case is considered, solder layers can be ignored. The red lines in Figure 2.1 indicate the heat-spreading as it passes through various layers. The heat-spreading angle (α) changes as it passes through each layer. In Figure 2.1, L1, L2, L3, L4, and L5 indicate the power semiconductor, the top copper layer, the DBC dielectric layer, the bottom copper layer, and the baseplate layer, respectively. The following symbols are used:

'K' defines thermal conductivity of each material.

K_{Cu} = Ka = Kc = Kd = 393W/m-K

K_{AlN} = Kb = 170 W/m-K

K_{Al} (baseplate is usually followed by Al heat-sink) = 240W/m-K

'T' indicates thickness of each layer.

Ta = Tc = 0.3mm

Tb = 0.65mm

Td = 6.35mm

The angle of spreading 'α' is given by [1]:

$$\alpha=\tan^{-1}\left({}^{k_{top\ layer}}/_{K_{bottom\ layer}}\right)\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(2.1)$$

From equation (2.1), we have

$$\alpha_a=\tan^{-1}\left({}^{Ka}/_{Kb}\right)=\tan^{-1}\left({}^{393}/_{170}\right)=66.6°$$

$$\alpha_b=\tan^{-1}\left({}^{Kb}/_{Kc}\right)=\tan^{-1}\left({}^{170}/_{393}\right)=23.4°$$

$$\alpha_c=\tan^{-1}\left({}^{Kc}/_{Kd}\right)=\tan^{-1}\left({}^{393}/_{393}\right)=45°$$

$$\alpha_d=\tan^{-1}\left({}^{Kd}/_{Ke}\right)=\tan^{-1}\left({}^{393}/_{240}\right)=58.6°$$

where α_a is the angle of spreading at the interface of the power semiconductor die and the top copper layer, α_b is angle of spreading at the top copper layer and the DBC dielectric layer, α_c is angle of spreading at the DBC dielectric layer and the bottom copper layer, α_d is angle of spreading at the interface of the bottom copper layer and the baseplate layer. The surface length of thermal effect for one dimensional model is given by [1]:

$$L(\text{of next layer})=2\ t_x \tan(\alpha_x)+L(\text{of previous layer})\ldots\ldots\ \ldots\ldots\ldots(2.2)$$

L1 is the length of the power semiconductor die, 4.08mm for the 50A CREE MOSFETs. Then,

$$L2=2\ t_a \tan(\alpha_a)+L1=2\ (0.3\times10^{-3})\tan(66.6)+4.08\times10^{-3}=5.47\times10^{-3}\text{m}$$

$$L3 = 2\, t_b \tan(\alpha_b) + L2 = 2\,(0.65 \times 10^{-3})\tan(23.4) + 5.47\times10^{-3} = 6.0326\times10^{-3}\mathrm{m}$$

$$L4 = 2\, t_c \tan(\alpha_c) + L3 = 2\,(0.3 \times 10^{-3})\tan(45) + 6.0326\times10^{-3} = 6.6326\times10^{-3}\mathrm{m}$$

$$L5 = 2\, t_d \tan(\alpha_d) + L4 = 2\,(6.35 \times 10^{-3})\tan(58.6) + 6.6326\times10^{-3} = 27.43\times10^{-3}\mathrm{m}$$

From the above analysis, the minimum distance between the two 50A CREE SiC power MOSFETs in order to have a complete heat spreading without any thermal coupling is 27.43mm – 4.08mm = 23.35mm.

This distance is not practical to achieve between the two power semiconductor dies in a multiple chip module as the size of the module becomes very large. Hence, power semiconductor dies are placed close to each other due to size constraint. In this case, thermal coupling needs to be considered as well. Maximum junction temperature increases due to thermal coupling, and hence, a more effective cooling system needs to be employed to cool the module. Using software which incorporates finite element analysis and iterative methods for thermal simulations, it is possible to evaluate the maximum junction temperature of the power electronic modules, and hence, the convection coefficient required to cool the power electronic module.

2.2 Encapsulation

Encapsulation is an insulating layer applied on the power electronic modules to protect their underlying components. These components can be chips/dies, wire connections and substrate, etc. These encapsulations need to be electrically insulating to avoid shorting of the components due to high voltage/current surges. Since heat dissipation occurs at chips and encapsulation is in contact with them, it would be ideal if encapsulation also aids in uniform heat distribution over the module. Also, there should be good adhesion between substrate and encapsulation after curing.

Encapsulation must be chosen in such a way that the difference in coefficient of thermal expansion (CTE) between the substrate and encapsulation must be as low as possible. This is required in order to mitigate any sort of undesirable thermal and mechanical stress [2]. Gel form is preferred for encapsulation under pre-cured condition. This is because applying or coating encapsulation on the power electronic module becomes easier. Once applied, encapsulation needs to solidify after curing and still retain its adhesion and insulating properties.

When encapsulation is applied on the power electronic module, care must be taken to prevent air bubbles within the encapsulation layer. If curing needs to be performed at high temperature, temperature must be increased in a rate low enough to avoid air bubbles. Air bubbles needs to be avoided as the trapped moisture or gases might induce corrosion in the power components.

Nusil R-2187 silicone elastomer encapsulation needs to be cured at 80ºC for an hour. Temperature of the oven is first increased to 40ºC and left there for an hour, and then increased to 60ºC and left for another hour, before finally increasing it to 80ºC at which the actual curing happens. Also, rate of temperature increases must be kept low enough to achieve effective encapsulation. An air bubble in power electronic module is shown in Figure 2.2.

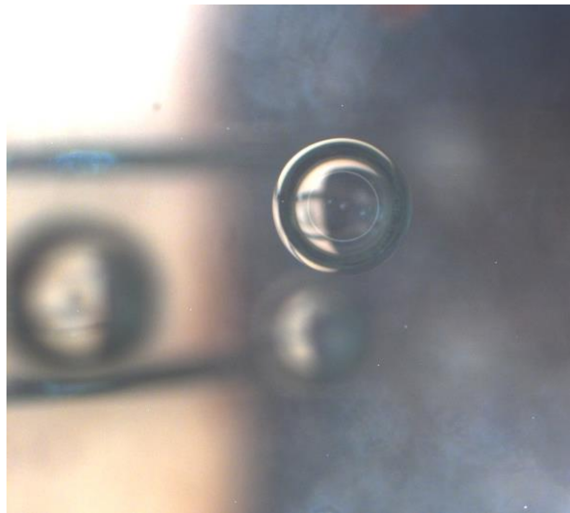


Figure 2.2. Air bubble in encapsulated power electronic module

2.3 Wirebonding

Most of the interconnections in power electronic modules are usually achieved using wirebonds. Some of these interconnections are

- Connecting two different traces
- To make connections with/between dies (source/drain/gate) and traces of interest.
- Make connection to power connectors which in turn act for external connections.

2.3.1 Bond wire material

Several materials for wires have been investigated for the power electronic module packaging. Some of them are mentioned below:

- Gold and Gold-alloys. This material is preferred in thermo-compression or thermo-sonic bonding. It has good electrical properties and high reliability. [3]
- Copper wire is a good substitute for Au wires as it costs less and has similar electrical properties. [4]
- Beryllium-doped Au wires have strong wire properties, and hence, can bear high stress. They are mainly used for automated bonding which adds a lot of mechanical stress on wires. [5]
- Aluminum wires are used as bond wires in this thesis. Al bond wires are preferred for high current density and weigh relatively low. They are available in both thin/fine (< 3mil wire diameter) and thick/heavy wires (> 3mil wire diameter). 5mil and 12mil aluminum bond wires are used to make interconnections in the wirebond reliability test structures in Chapter 5. Al wires are usually 99% pure and the other 1% is usually silicon or magnesium. Magnesium doping provides a better fatigue resistance [6]. Al 1%Si wire is precipitation strengthened and Al 1%Mg is solution strengthened. Both have similar

break and yield strength for a wide range of annealing temperature. According to Hongwei Liu, elongation increases with annealing temperature for 1%Mg Al wires and reaches its highest around 250°C – 300°C. Whereas for 1%Si Al wires, two high peaks and another low peaks were recorded between 200°C and 300°C [7].

2.3.2 Wirebonders

Different types of bonders are available for both automated and manual wirebondings. Wedge bonder is discussed here as this is the bonder used to make wirebonds for the wirebond reliability test modules as reported in Chapter 5.

Ultrasonic wedge bonder:

Ultrasonic wedge bonder attaches/welds wire to a substrate using ultrasonic energy at room temperature. The bonder has a capillary through which bond wire is fed. The capillary is pointed at the first bonding position and wire is bonded using ultrasonic energy. This is called the head of the wirebond. The voltage and time to weld the wire should be calibrated according to the wirebond diameter. Once head connection is made, the wedge bonder's capillary is lifted to a loop height (this needs to be set based on the module design) and steps back (step back needs to be set according to the module design as well) to the second position. The bonder now makes second bond at this position using its ultrasonic energy. This is the tail of the bond. Bonds are made at room temperature. Once the second bond is made, the wire following second bond is cut. Figure 2.3 shows a wedge bond. An orthodyne ultrasonic wedge bonder shown in Figure 2.4 was used to create the aluminum wedge bond shown in Figure 2.3.

Figure 2.3. Wedge wirebond

Figure 2.4. Orthodyne ultrasonic wedge bonder

2.3.3 Failure mechanisms

A power electronic module houses several interconnections using wirebonds. The number of wirebonds in a single power electronic module can vary from 10s to 10000's. Sometimes a single wirebond failure in critical spots like gate connections can cause failure of the entire power electronic module. Hence study of wirebond failure is very important to assess the reliability of power electronic modules. Wirebond failure is the largest failure mode for an integrated circuit as shown in Figure 2.5.

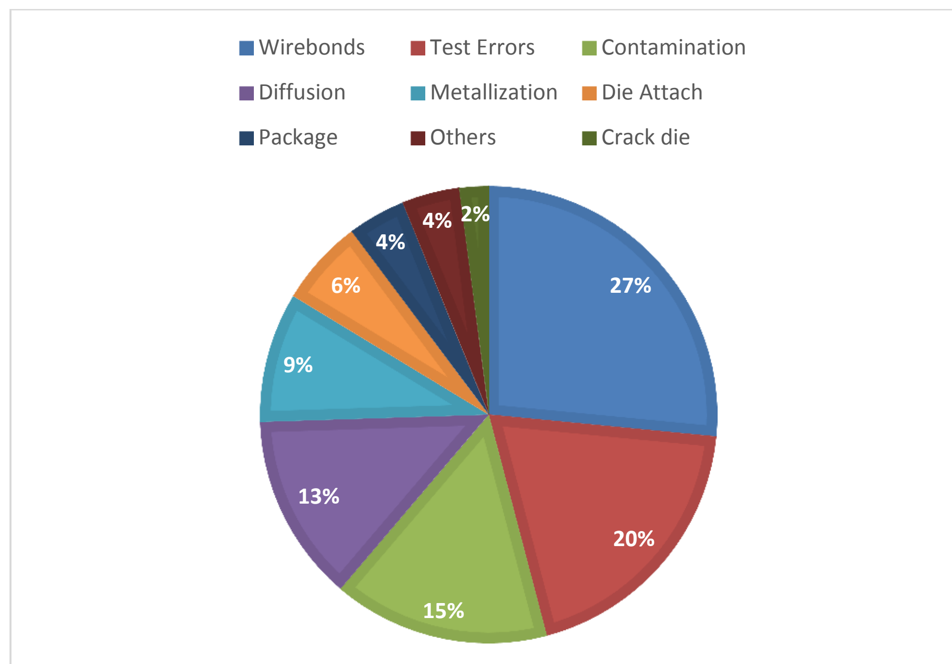


Figure 2.5: Failure modes of an integrated circuit [Source: Solid state technology ICE "Road maps of packaging technology"] [8]

Some of the failure mechanisms for wirebonds are:

- Insufficient energy (ultrasonic energy in case of ultrasonic wedge bonder) applied on the bond wire while welding it to the substrate. This causes weak bonds, and hence, a small amount of stress can cause failure.
- When energy more than the required levels is applied while bonding, it can cause extra stress, and hence deform the bond heel.

- Improper tool calibration like wirefeed length, step back, loop height.
- Wirebonds are subjected to mechanical stress due to other materials in power electronic modules like encapsulation. If mechanical stress is big enough, it may cause wirebond failure as well.
- Wirebonds may corrode due to moisture and gases at bonding points.
- Contamination of the substrate or un-clean substrate lead to thermo-oxidative degradation, and hence, corrosion in aluminum bond wires at its heel.
- Breakage of bonds when handled roughly.
- In a case where wirebonds jump over a trace, shorting of the middle undesirable trace with other traces can occur.
- Thermal cycling of the module can add thermal stress on the wirebonds and cause lift-off of wirebond at it heals.
- When hard or thick wires are welded to fragile surfaces like gate pad of a power semiconductor die, the surface damage can occur.
- Even if the wire is well bonded, due to intermetallic failures and formation of Kirkindall voids, a high electrical resistance region at the bonding area can fail interconnections.

CHAPTER 3. THERMAL ANALYSIS OF POWER ELECTRONIC MODULES

3.1 Introduction

When designing a layout for any circuit, it is easier if there is a database from which one can select certain parameters. Like choosing the right size of the substrate from the efficiency at which the power module is supposed to work, or choosing the type of cooling required (convection coefficient that specifies if free/forced air/liquid cooling) to maintain a particular maximum junction temperature for a given ambient temperature etc.

This chapter includes:

- Study of how different parameters – like power dissipation, maximum junction temperature, ambient temperature, convection coefficient required to cool the module, size of the baseplate, heat-sink size, substrate size, spacing between dies, different materials that can be used for module – affect each other in a layout.
- To provide a rough database that aids in choosing parameters like convection coefficient or optimum substrate size for a layout.

The layout of power electronic module can be designed in many ways for the same circuit. To provide for more generalized database, a full bridge circuit is considered. As this is one of the most common topologies used in power electronic modules. For this full bridge circuit, a generalized layout is designed; on which thermal simulations are performed using Solidworks thermal simulator. This layout is later subjected to various conditions virtually; similar to what power electronic modules would experience in actual operation situation. Thermal behavior of this power electronic module in simulated conditions for various parameters is recorded to prepare a database, and to further study them.

3.2 Full bridge circuit

The most common topology used in power module packaging is the full bridge topology since it can deliver a large amount of energy transfer. A half-bridge topology is used in many cases too, but since the full bridge is larger and can accommodate more power semiconductor dies, the full bridge is considered here. A complete full bridge circuit is given in Figure 3.1.

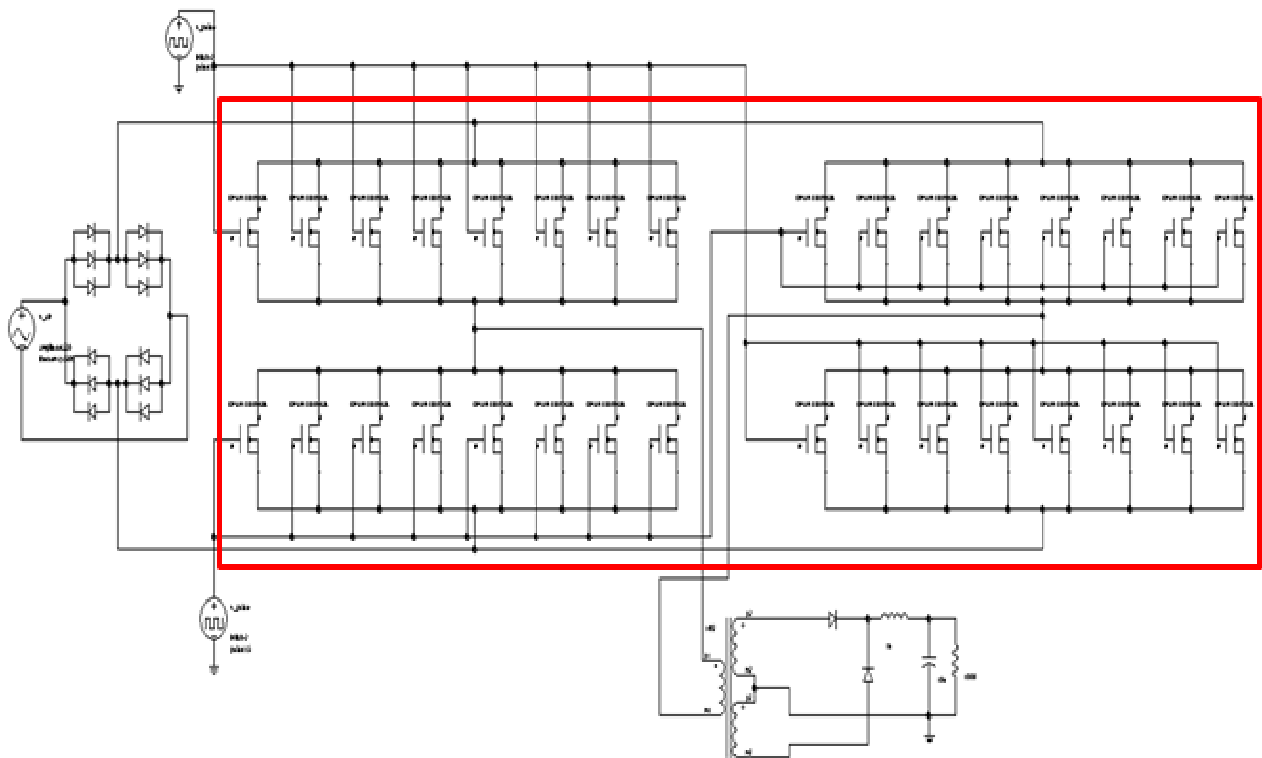


Figure 3.1. Full bridge circuit

For a 50KW power electronic module and 92% efficient, the total power dissipation by the module is 4KW. For a 50KW power module that is 95% efficient, the total power dissipation by the module is 2.5KW. Hence power dissipation by the module depends on the efficiency and how much power the module is capable to output from the given input without being damaged. The maximum power dissipation case by module considered in this thesis is 4KW (higher power dissipation cases are possible but is not considered here). This needs to be distributed between all

the MOSFETs equally. For this extreme case, it's best to consider 32 MOSFETs. This gives 8 MOSFETs on each leg and 125W of power dissipation by each MOSFET rated at 20A.

Since a generalized layout is to be designed for simulation purpose; a layout is designed only for part of a circuit shown in the Figure 3.1 which is inside the red box.

3.3 Full bridge layout

Several layouts were designed and the most optimized layout was chosen. Size of this substrate is 53mm X 58mm. Of-course the MOSFETs can be rotated to better aid wire-bond connections. In this layout, dies are distributed evenly throughout the substrate, thus providing for good thermal balance. As shown, 8 power MOSFET dies are arranged in a linear array with a common drain on the power substrate. Also, silicon carbide (SiC) MOSFETs are used in this power electronic module as they can operate under high temperature conditions. Figure 3.2 shows the layout on which thermal analysis is performed and results of the same are shown later in this chapter.

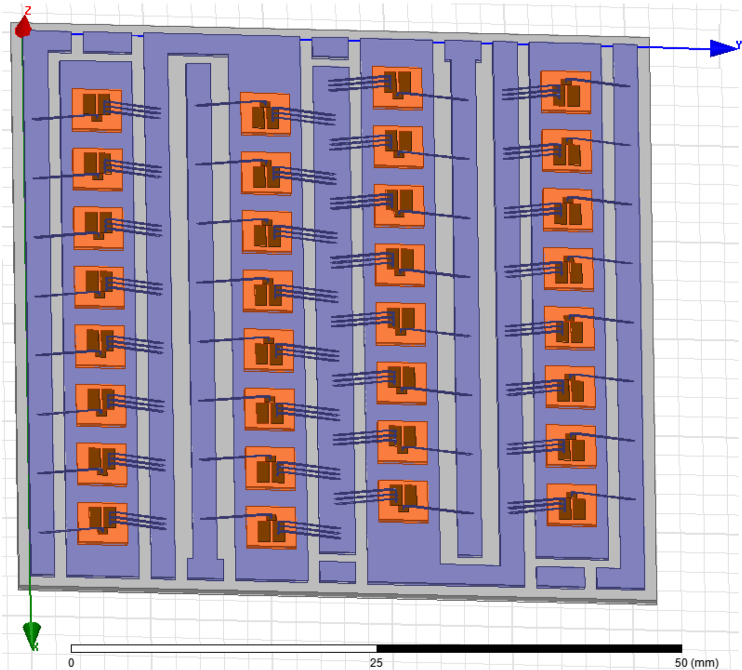


Figure 3.2. Full bridge layout.

3.4 Parameter constraints applied on power module for simulations

- *Power dissipation (PD):* As mentioned in section 3.2, maximum limit to power dissipation by module is considered to be 4KW. For analysis, total power dissipation by module is considered to vary from 640W to 4000W. However, three main cases considered are; low 1.6KW, medium 2.5KW and high 4KW.
- *Maximum junction temperature (Tjmax):* It is the maximum temperature allowed on the power electronic module and is usually at the center of the die. Two cases of maximum junction temperature are considered for analysis 250°C and 200°C.
- *Ambient temperatures (Ta):* This is the temperature at which the module is placed and provides data on the external environment of the working module. Several cases of ambient temperatures are considered like 25°C, 50°C, 75°C, 100°C and 125°C. However, 100°C is considered is most cases unless specified otherwise.
- *Size of DBC or substrate:* Original (smallest) size of the module considered based on the layout design is 53mm X 58mm. This is the substrate size on which thermal analysis is performed until specified otherwise.
- *Convection coefficient (CC):* This value gives us the required cooling system/technique that is needed to be employed, to bring the maximum junction temperature of the module to desired levels. It varies significantly depending on the above parameters. The smaller is the convection coefficient; the more favorable it is to the thermal management system.

Thermal simulations are performed on a DBC substrate with the above parameters individually and the results are plotted. Figure 3.3 shows the SolidWorks designed DBC substrate model on which simulations are performed.

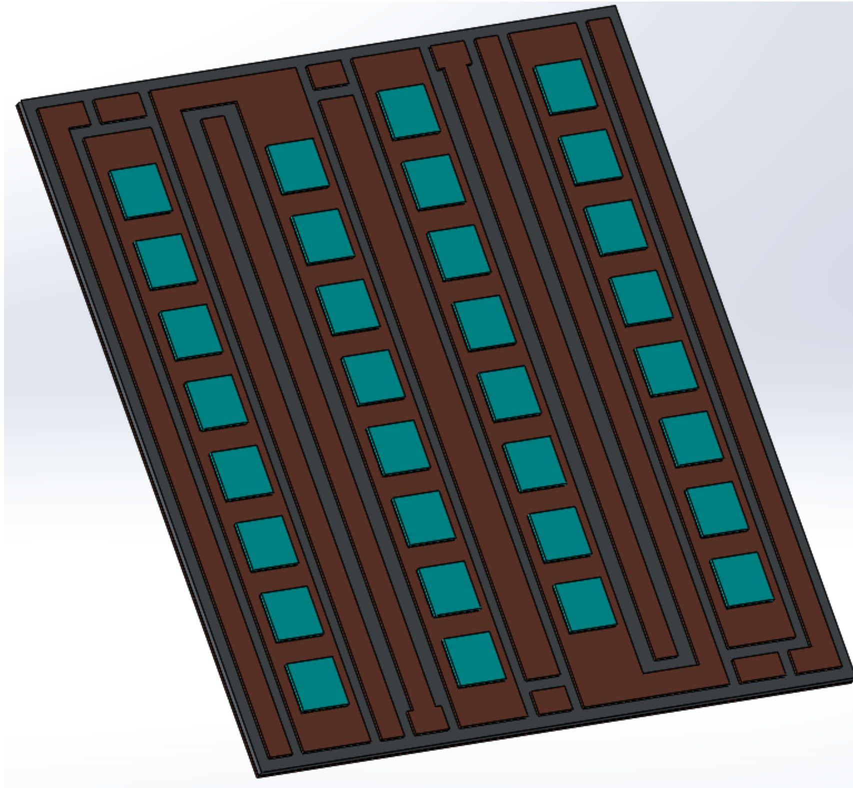


Figure 3.3. DBC substrate designed in SolidWorks

In some layout design software (PowerSynt), baseplate feature attachment option is made available and the convection coefficient assigned to the baseplate would be equivalent to both heat-sink attached to baseplate and the convection coefficient given to this heatsink. For this purpose, thermal simulations are performed on the DBC substrate with baseplate attached to it. Baseplate provides for mechanical strength of the power electronic module and also helps in balanced heat-spreading over the substrate. Baseplate is slightly bigger than the DBC substrate (5mm increase on x and y directions). SolidWorks model for the same is given in Figure 3.4. Baseplate material used is copper. This is because the DBC substrate's copper comes in contact with the baseplate via solder preform/paste hence; to facilitate best thermal distribution and to achieve good heat spreading copper baseplates are preferred. Also it provides best coefficient of thermal expansion match (CTE for copper is 16.7ppm/°C).

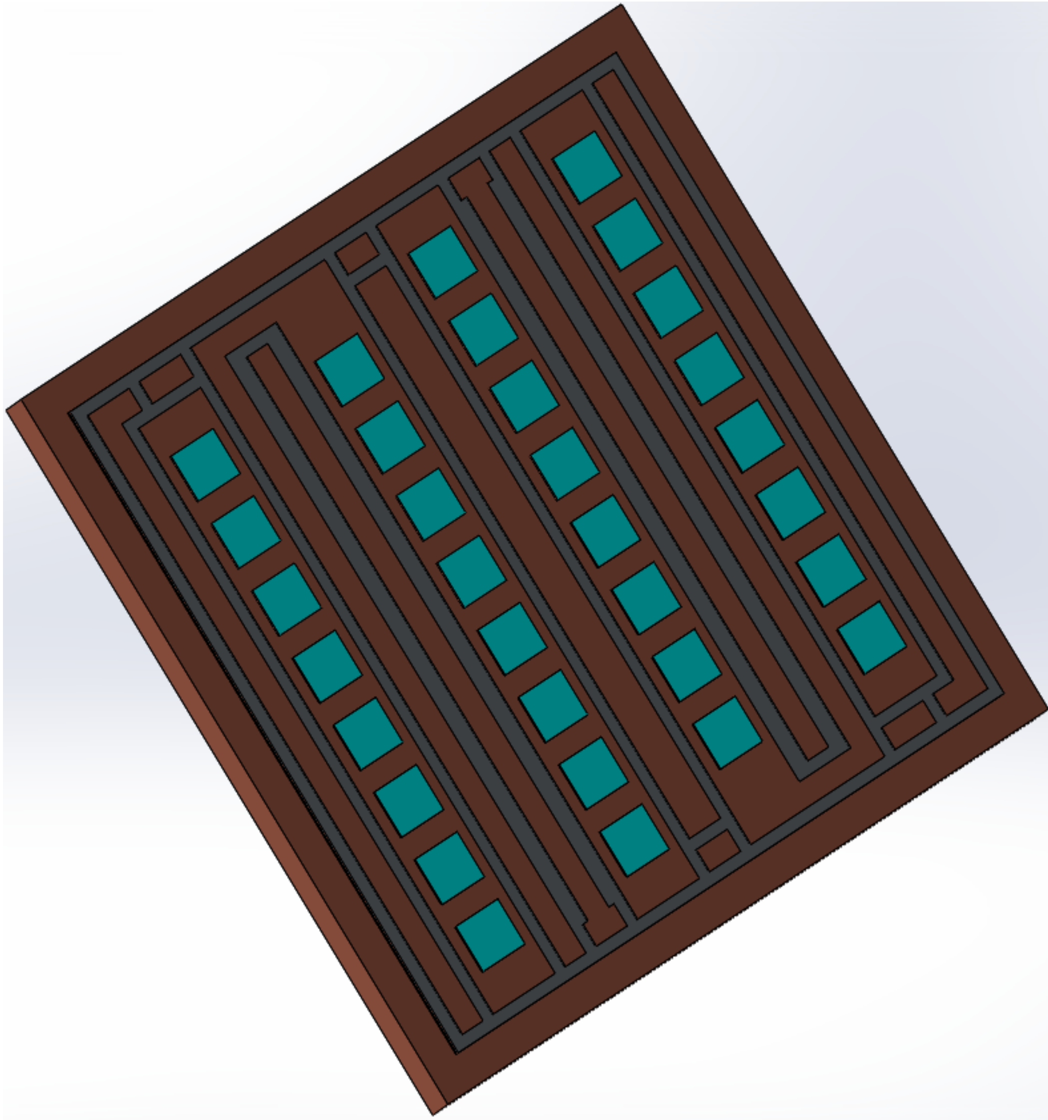


Figure 3.4. DBC substrate with baseplate designed in SolidWorks

In all cases, heatsinks are attached to the power electronic modules to increase the cooling surface area. Hence, heatsink is also designed in SolidWorks and is attached to the baseplate. A general design of heat-sink is considered with each fin of 2mm wide, and spacing between each fin is 2mm as shown in Figure 3.5(a). Finally, the heatsink attached to the power electronic module (along with baseplate) is given in Figure 3.5(b).

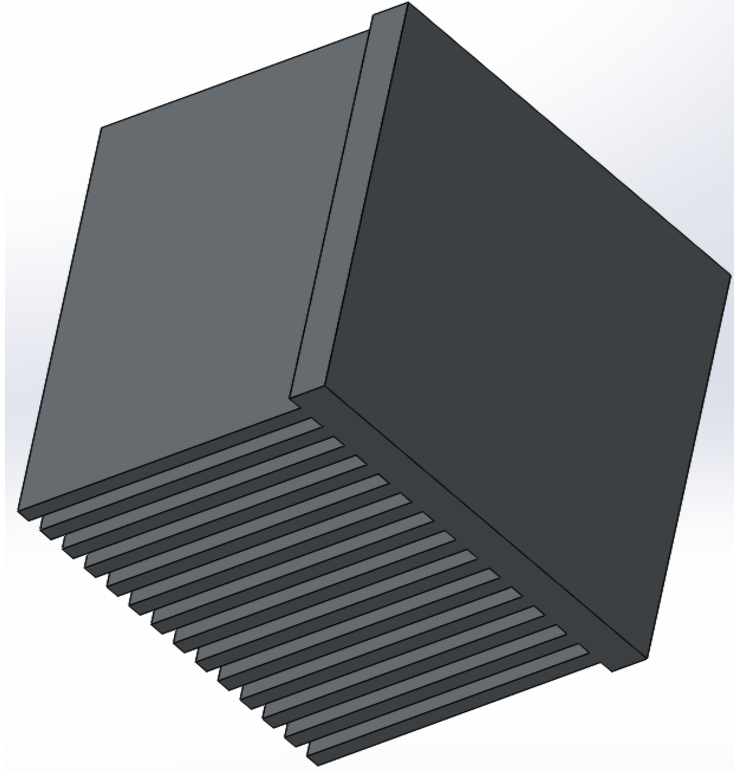


Figure 3.5(a). Heatsink design

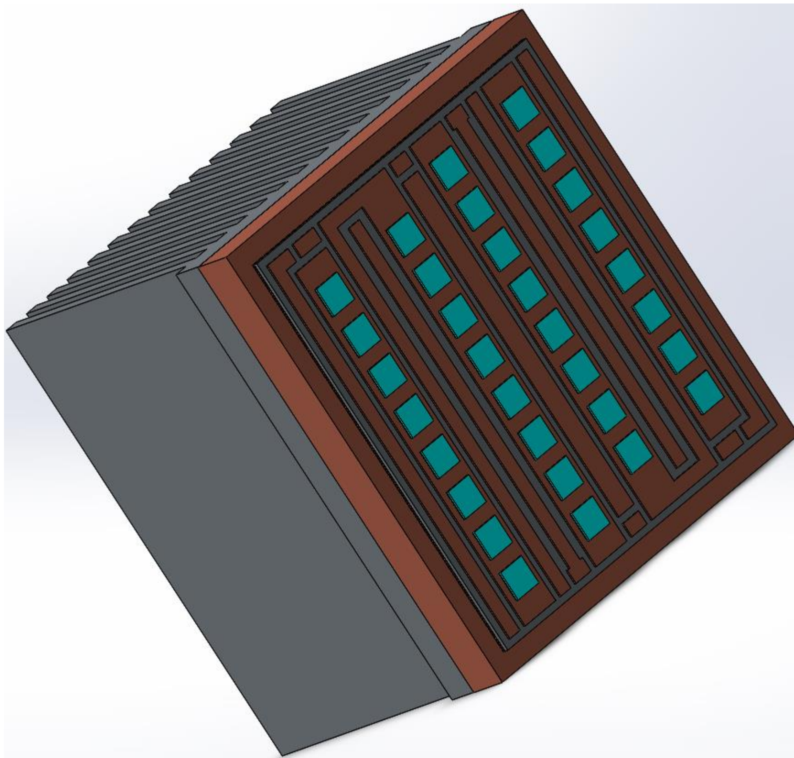


Figure 3.5(b). DBC substrate with baseplate and heatsink designed in SolidWorks

Thermal Study is chosen in SolidWorks simulator to perform steady state thermal analysis. Figure 3.6 shows some of the steps in assigning parameters for simulations. Convection coefficient and ambient temperatures are applied for the power module in SolidWorks on the backside of the substrate (for no baseplate or heatsink condition) or on the backside of the baseplate (for baseplate and no heatsink condition) or to all the exposed faces of the heatsink (for heatsink condition) using *Convection* in *Thermal Load* as illustrated in Figure 3.6(a).

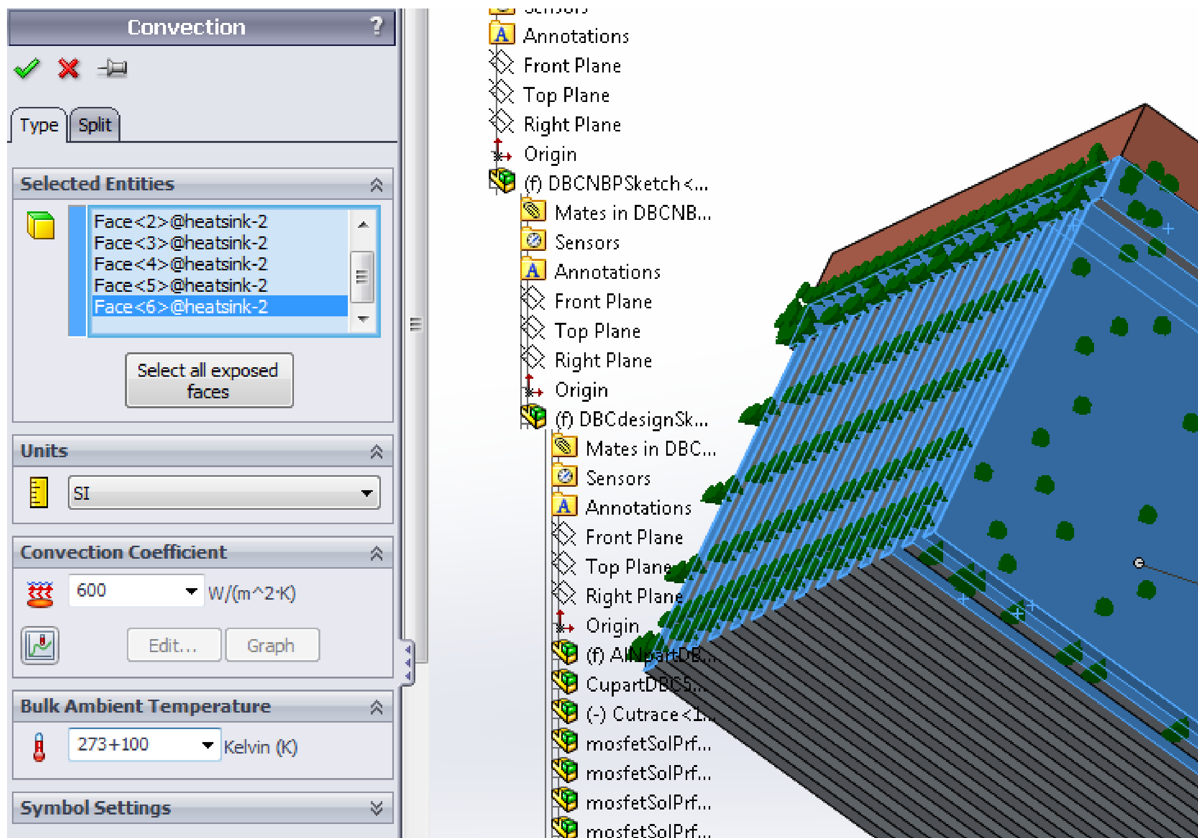


Figure 3.6(a). Assigning convection for power module in SolidWorks (heatsink condition)

Although not all MOSFETs are functioning at the same time; in steady state thermal analysis, due to high switching speeds of the dies, off-time of the dies does not make much difference thermally (NOT electrically) due to thermal mass and slow heat-spreading. Hence it can be considered that power is dissipated equally by all the MOSFETs at a time as an average. From

this assumption, power dissipation is given to the power module by assigning power dissipation for each device (MOSFET, JFET, diodes etc.). Suppose the total power dissipated by the module is 3.2KW, and then equally divide the power between all the dies. In this case since there are 32 MOSFETs, each MOSFET is given 100W of power dissipation (3200/32 = 100W). This power dissipation is assigned using *Heat Power* in *Thermal Loads* and choosing every single MOSFET as shown in Figure 3.6(b).

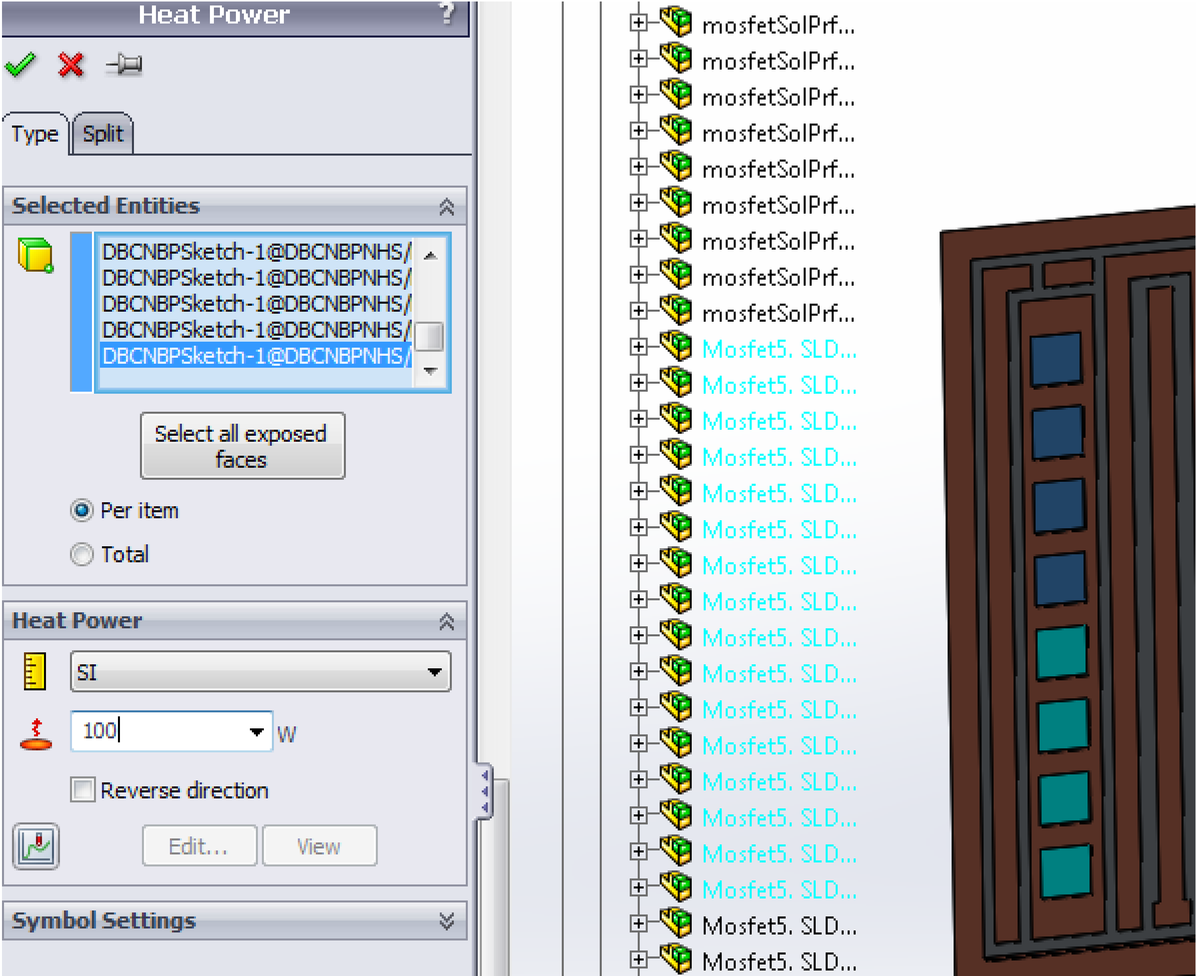


Figure 3.6(b). Assigning power dissipation for power module in SolidWorks

When all the parameters are applied to the power module, mesh is chosen and the simulation is performed to obtain the simulated results (meshing parameters are chosen depending on the

design and size of the module). Simulated results are normally the maximum junction temperature of the module. Parameters are varied using *Convection* and *Heat Power* thermal loads to obtain different/desired junction temperatures.

Curvature based mesh is chosen for the simulations of the power electronic module. Figure 3.6(c) shows the meshed power module (after Convection is assigned). Figure 3.6(d) shows the thermally simulated module. Maximum temperature is usually at the center of the die (usually on the die which is placed at the center of the module). Red areas indicate corresponding high temperatures and blue indicates corresponding low temperatures.

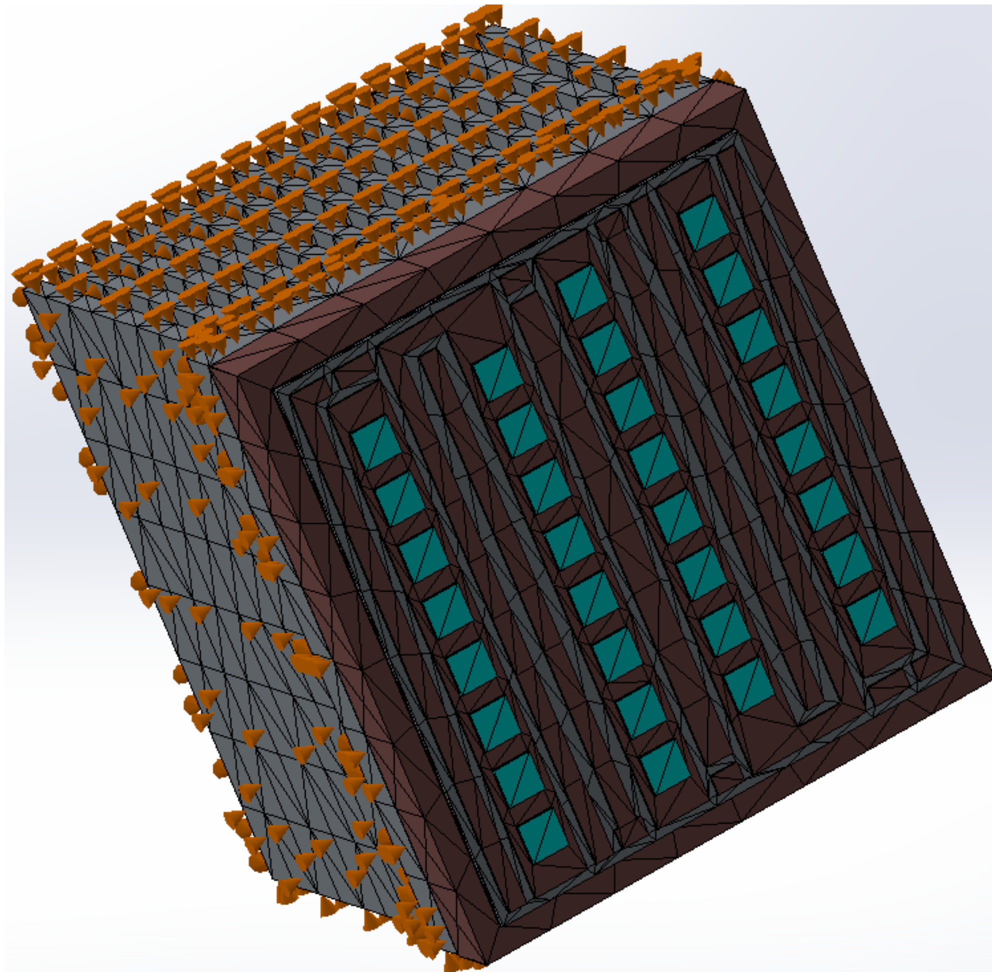


Figure 3.6(c). Meshed power module

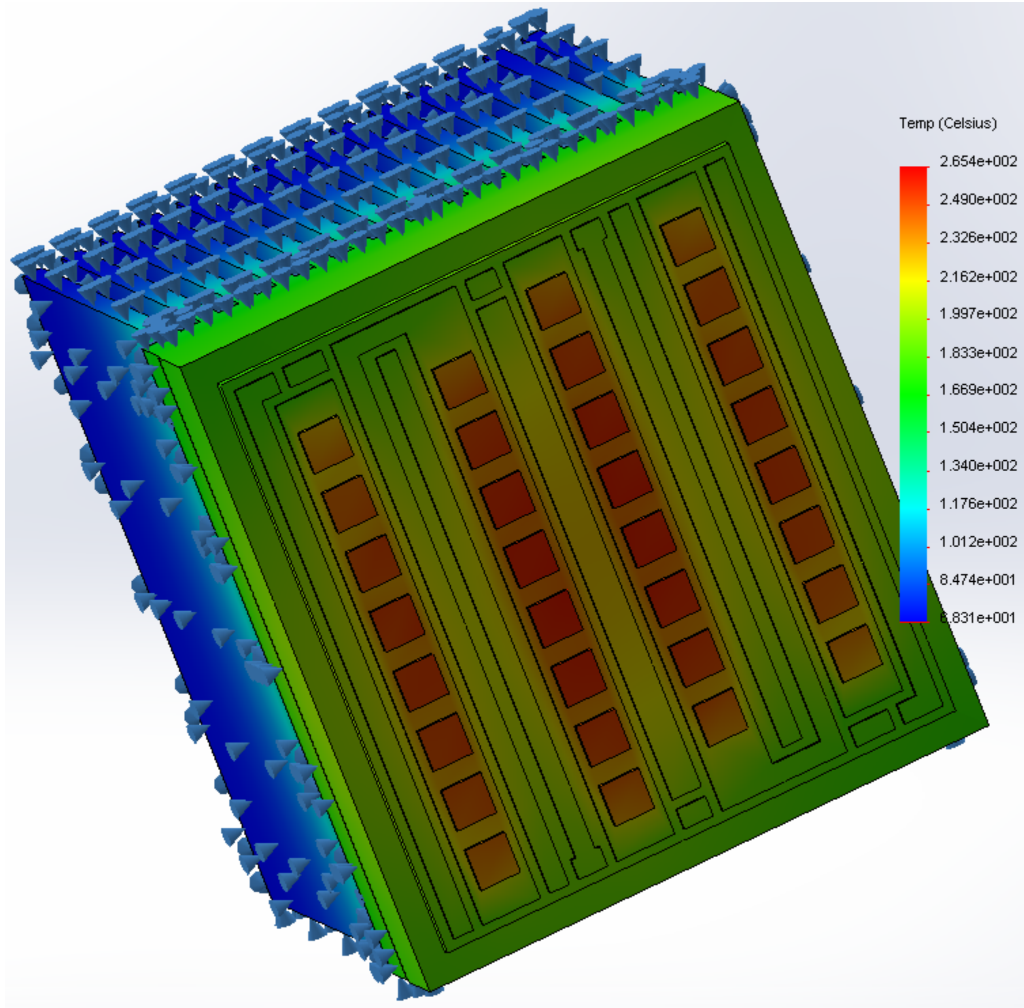


Figure 3.6(d). Simulated result

3.5 Material selection

Properties of different materials that can be used in fabrication are studied. Thermal simulations are performed on these different materials to discuss which materials are best suited for thermal analysis in later section.

3.5.1 Insulating material in DBC substrates

AlN and Al_2O_3 are the two mainly used insulating substrates for the DBC. Table 3.1 compares the thermal properties of these two materials.

Properties	Al_2O_3	AlN
Thermal conductivity (W/m. K at 20ºC)	24	170
Coefficient of thermal expansion (ppm/K at 20 to 200ºC)	6.8	4.7
Specific heat (J/Kg. K)	880	740
Dielectric strength (KV/mm)	16.7	20
Relative price per DBC (Al_2O_3 base)	1	2.5

Table 3.1. Al_2O_3 and AlN material properties comparison [accuratus.com, remtec.com]

Next, simulations are performed using both materials on model shown in Figure 3.6. The simulation results are shown in Figure 3.7.

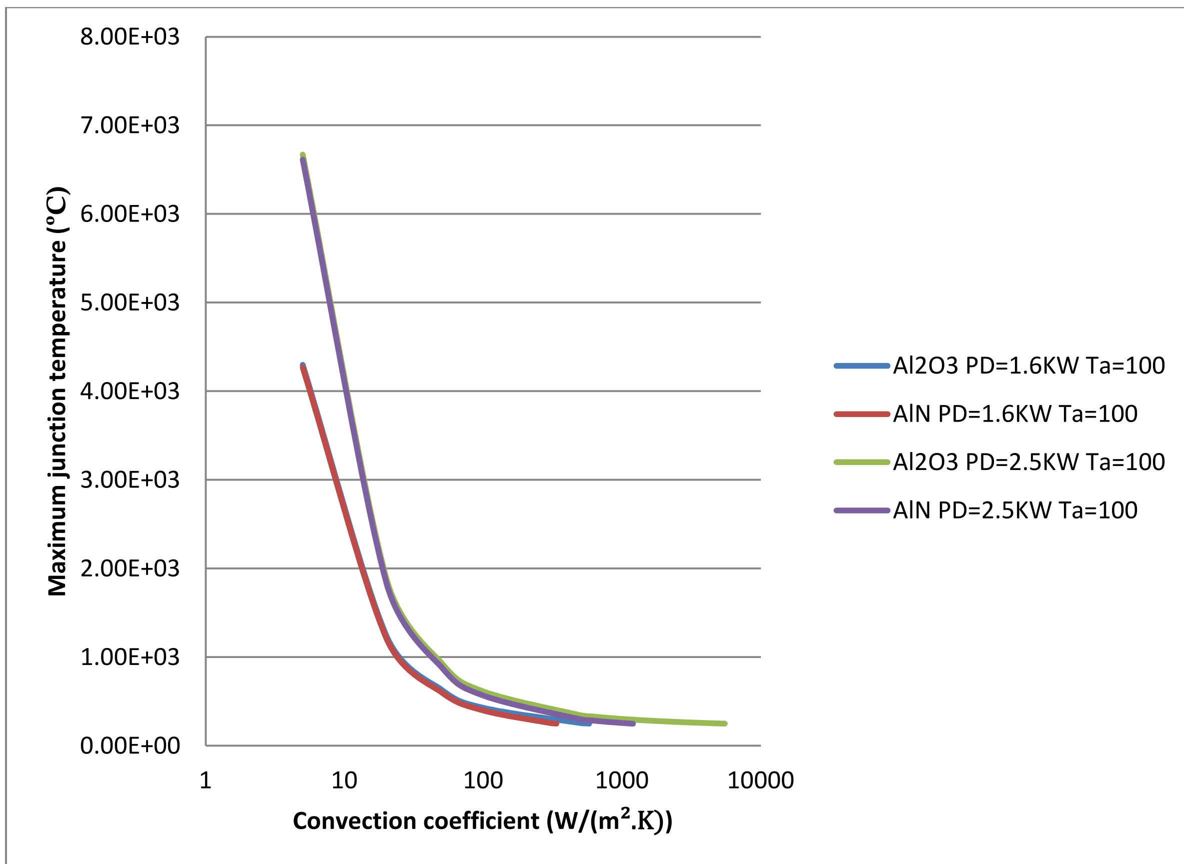


Figure 3.7. Convection coefficient versus maximum junction temperature for Al_2O_3 and AlN materials

Figure 3.7 shows the plot for convection coefficient (CC) versus maximum junction temperature (Tjmax) for Al_2O_3 and AlN substrate materials under 100ºC ambient temperature and different power dissipations (1.6KW and 2.5KW).

It can be seen from Figure 3.7 that although Al_2O_3 and AlN follow the same curve for similar power dissipations, maximum junction temperature of 250ºC is reached quicker (lower convection coefficient) in the case for AlN. That is, for 2.5KW (and 1.6KW) of power dissipation, Al_2O_3 based substrate needs around 5500W/m^2K (and 580W/m^2K) to reach 250ºC of Tjmax whereas AlN requires only 1200W/m^2K. Also, for 1.6KW of power dissipation, Al_2O_3 based substrate needs around 580W/m^2K to reach a 250ºC Tjmax whereas AlN requires only 340W/m^2K.

From Table 3.1, thermal conductivity of AlN is much higher than that of Al_2O_3. Hence, AlN conducts or transfers heat better than the Al_2O_3 dielectric. So, when performance is the main factor in designing the layout, it is always better to choose AlN as the insulating material for the DBC substrate. However if price is the main factor and performance takes second place, then Al_2O_3 is the better option.

3.5.2 Different heat-sink materials

As discussed in Chapter 2, heatsink reduces the temperature of the power module by a significant value by increasing the surface area that is exposed to the external environment (ambient temperature).

Varieties of heatsink materials are available in the market today. Some of the most commonly used heat-sink materials are: Al alloys 1050A, 6061, 6063 and copper. Properties of these metals are given in the Table 3.2.

Property	1050A	6061	6063	Cu
Density (g/cm^3)	2.71	2.7	2.7	8.92
Melting Point (°C)	650	650	600	1083
Modulus of Elasticity (GPa)	71	70	69.5	117
Electrical Resistivity (Ω.cm)	2.82x10^{-6}	3.7–4.0 x10^{-6}	3.5x10^{-6}	1.71x10^{-6}
Thermal Conductivity (W/m.K)	222	173	200	391.1
Thermal Expansion (x10^{-6} /K)	24	23.5	23.5	16.9

Table 3.2. 1050A, 6061, 6063, Cu material properties comparison table [Datasheets from www.aalco.co.uk]

Simulations are performed for all the four heatsink materials (for the model shown in Figure 3.6), for 2.5KW power dissipation and 100ºC ambient temperature. The plot obtained for maximum junction temperature versus convection coefficient is shown in Figure 3.8 for the four materials. Also, Figure 3.9 shows the convection coefficient required by each of these materials to maintain a 250°C maximum junction temperature.

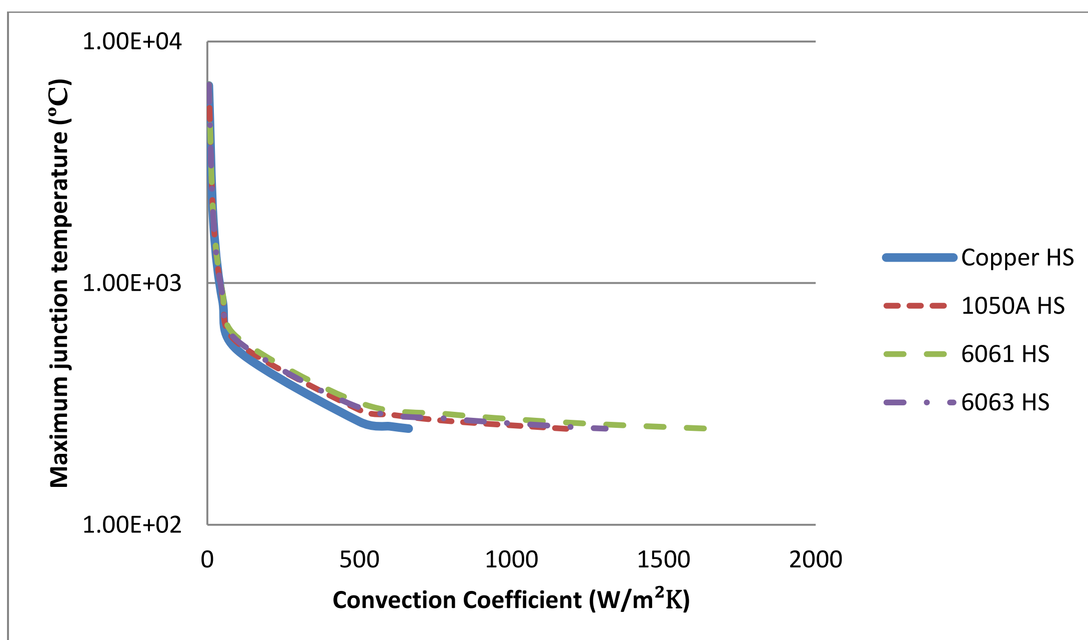


Figure 3.8. Convection coefficient versus maximum junction temperature for four materials

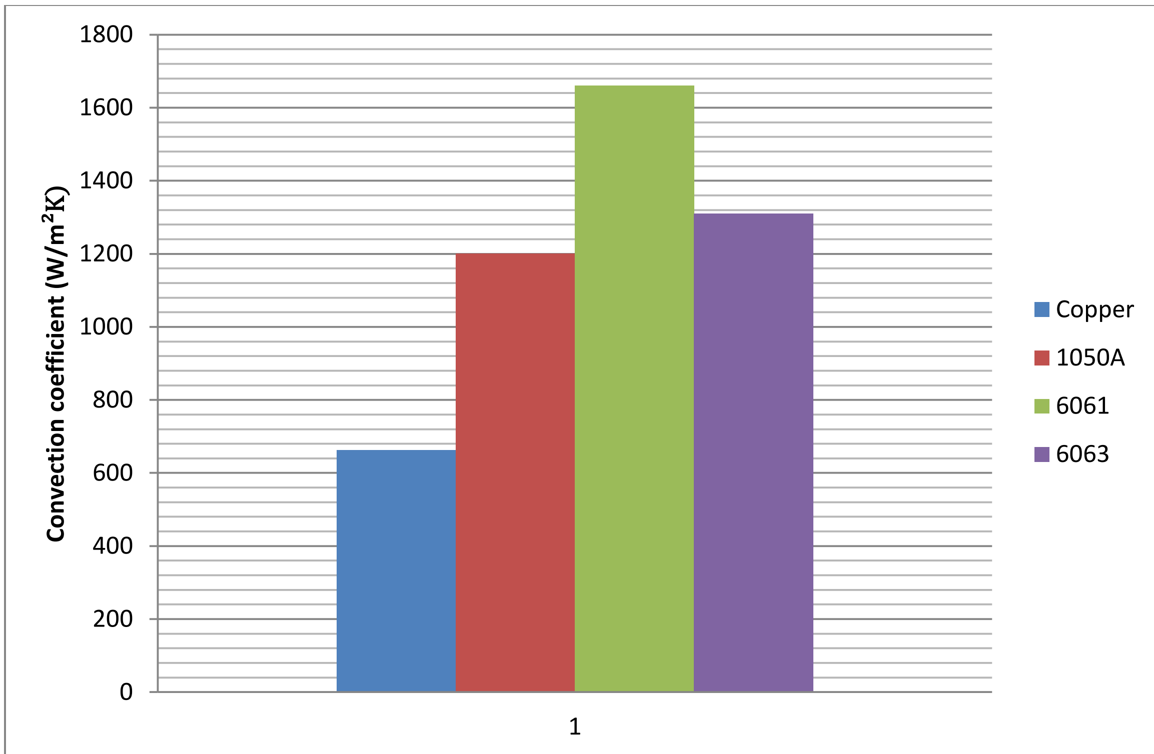


Figure 3.9. Convection coefficient required by each material to maintain a maximum junction temperature of 250ºC

Copper and 1050A Al alloy produce best results as seen in Figures 3.8 and 3.9. Based on the plots above, copper is the best material for heat-sink since it requires almost only half the convection coefficient to cool the substrate when compared to that of the 1050A Al alloy. But, from Table 3.2, the density of copper (8.92g/cm^3) is much higher than that of 1050A (2.71g/cm^3). Hence if copper is used as a heatsink material the power electronic module becomes heavy. Due to this trade-off, Al alloy 1050A is used for heatsinks when a reduced weight is important. Therefore for thermal simulations later in this chapter, Al alloy 1050A material is used as the heatsinks.

3.6 Study on ambient temperature variations

To study the effect of ambient temperature on the power electronic module, maximum junction temperature versus convection coefficient is plotted for different ambient temperatures at 25ºC,

50ºC, 100ºC, and 150ºC for 2.5KW power dissipation. Figure 3.10 is for model shown in Figure 3.3 with no baseplate and no heat-sink condition.

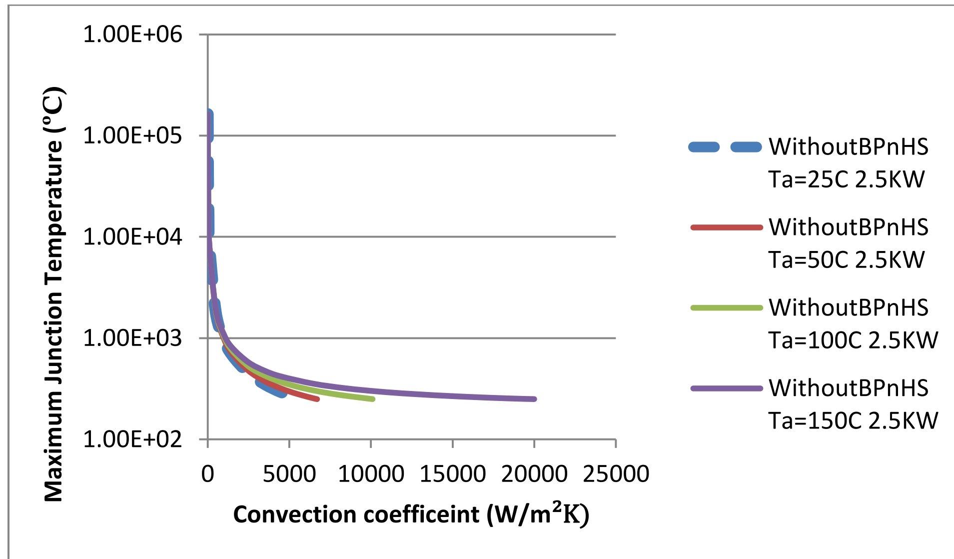


Figure 3.10. Convection coefficient versus maximum junction temperature (without BP or HS) for different ambient temperature and 2.5KW power dissipation

Similarly, Figures 3.11 and 3.12 are for models shown in Figures 3.4 and 3.5, respectively (with base plate, and with baseplate and heatsink, respectively).

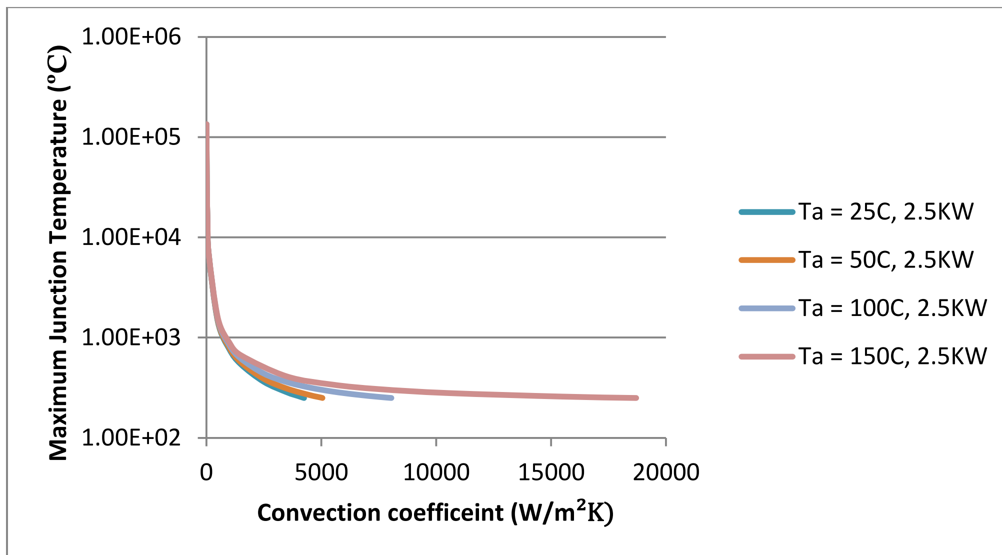


Figure 3.11. Convection coefficient versus maximum junction temperature (with BP and without HS) for different ambient temperature and 2.5KW power dissipation

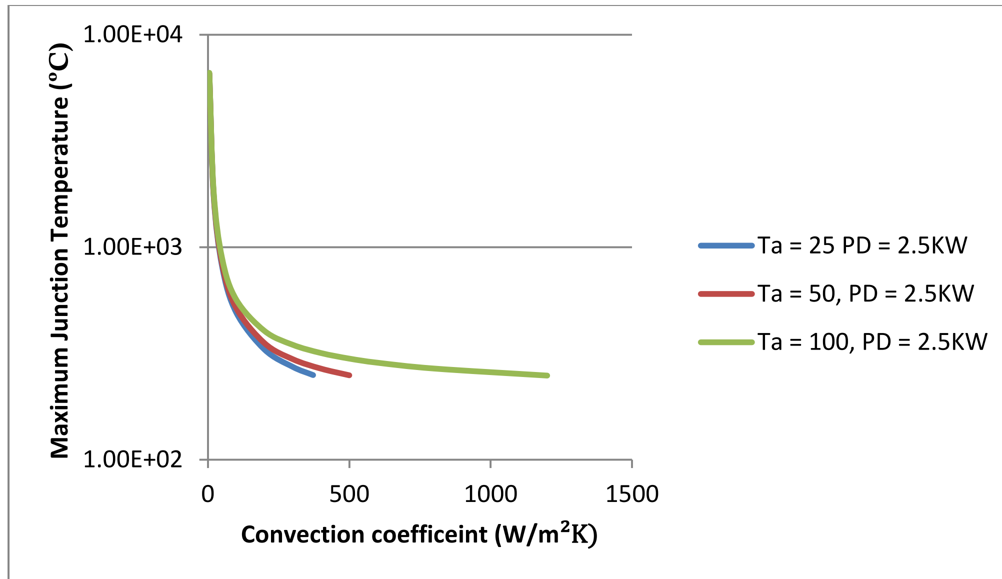


Figure 3.12. Convection coefficient versus maximum junction temperature (with BP and HS) for different ambient temperatures and 2.5KW power dissipation

As seen in Figures 3.10, 3.11, and 3.12, convection coefficient versus Tjmax plots show exponential behaviors. Also, Tjmax in most of the power electronic module does not exceed 250ºC or 300ºC. Hence, the power electronic module with heatsink and convection coefficient larger than 260W/m^{2}K is of importance.

Three main cases considered are:

- No heatsink and no baseplate: baseplates are not used to improve power cycling capability in some cases. To provide equivalent convection coefficient to heatsink and cooling system given to this heatsink, this case is considered.
- With baseplate and without heatsink: there are several software that provide for only baseplate while layout is generated (for example: PowerSynt [9]), to provide the equivalent convection coefficient to heatsink and cooling applied to this heatsink case two is considered.
- With baseplate and heatsink: most power modules design includes both baseplate and heatsink.

Similarly for 1.6KW and 4KW power dissipations, data collected is shown in Figures 3.13, 3.16 (no baseplate and no heat-sink condition), 3.14, 3.17 (with base plate and without heat-sink) and 3.15, 3.18 (with baseplate and heat-sink conditions). From these plots, the type of cooling required for a particular ambient temperature and power dissipation conditions can be determined.

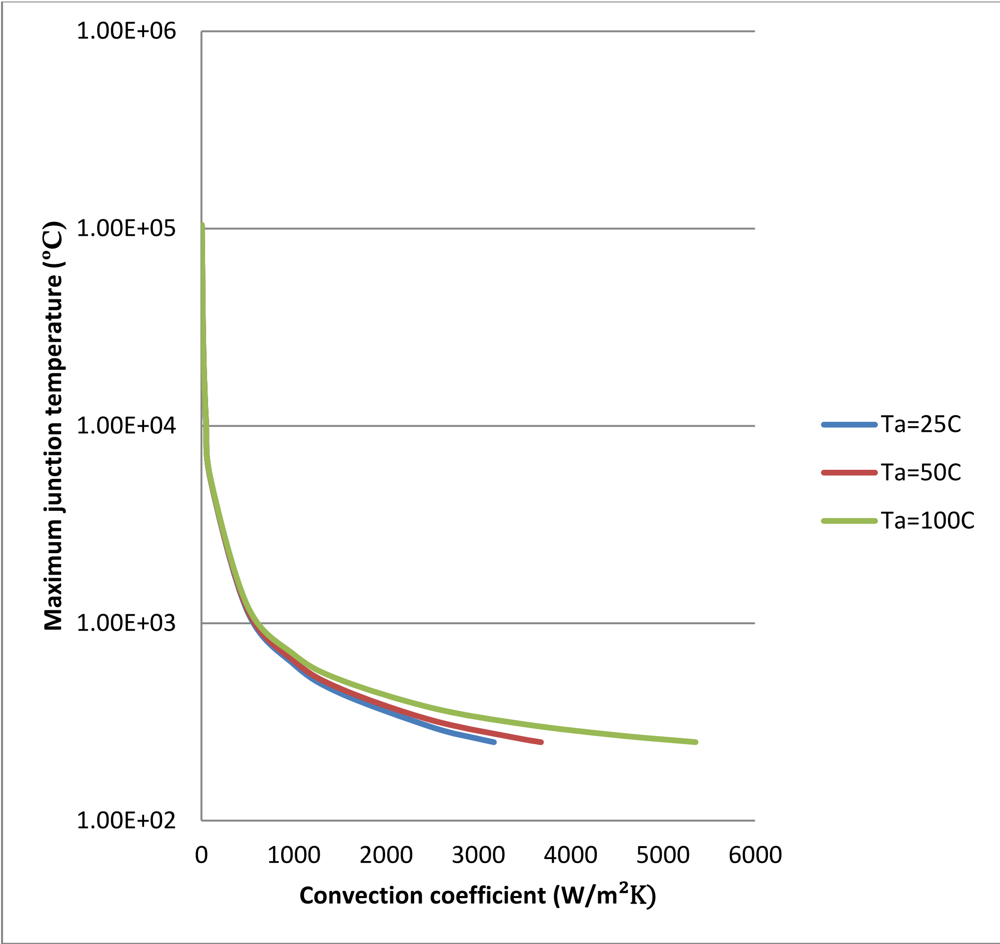


Figure 3.13. Convection coefficient versus maximum junction temperature (without BP or HS) for different ambient temperatures and 1.6KW power dissipation

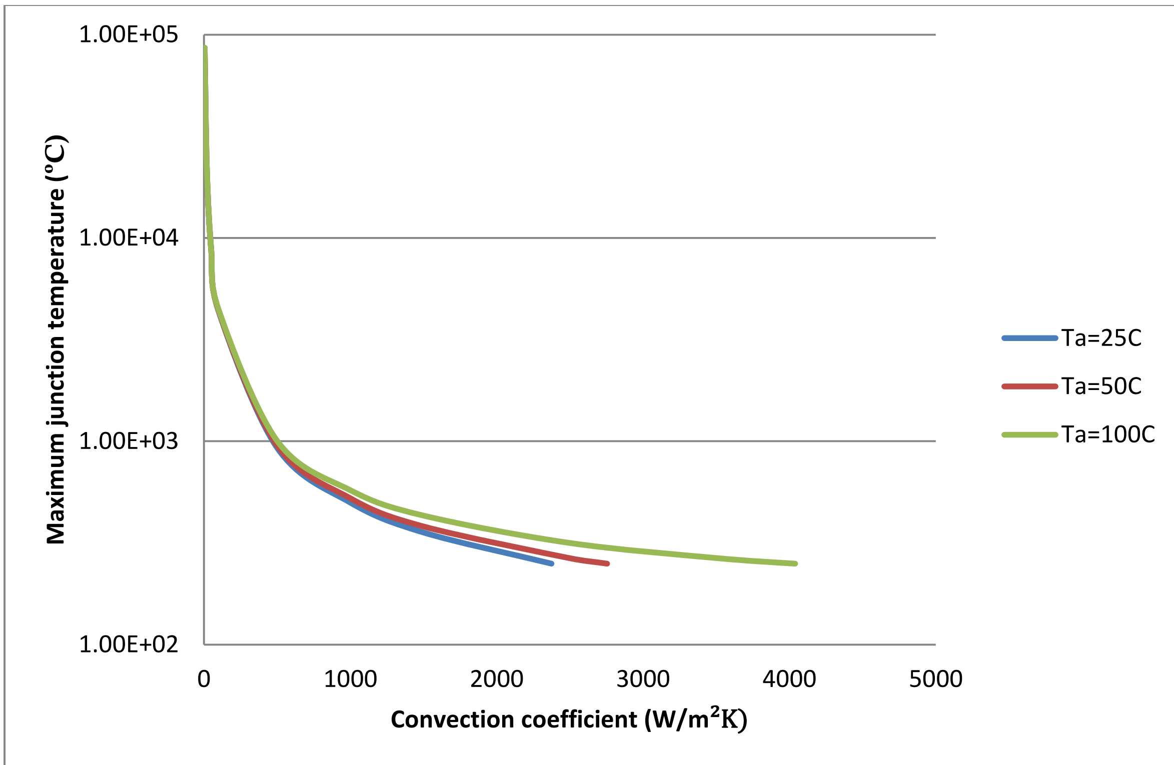


Figure 3.14. Convection coefficient versus maximum junction temperature (with BP and without HS) for different ambient temperatures and 1.6KW power dissipation

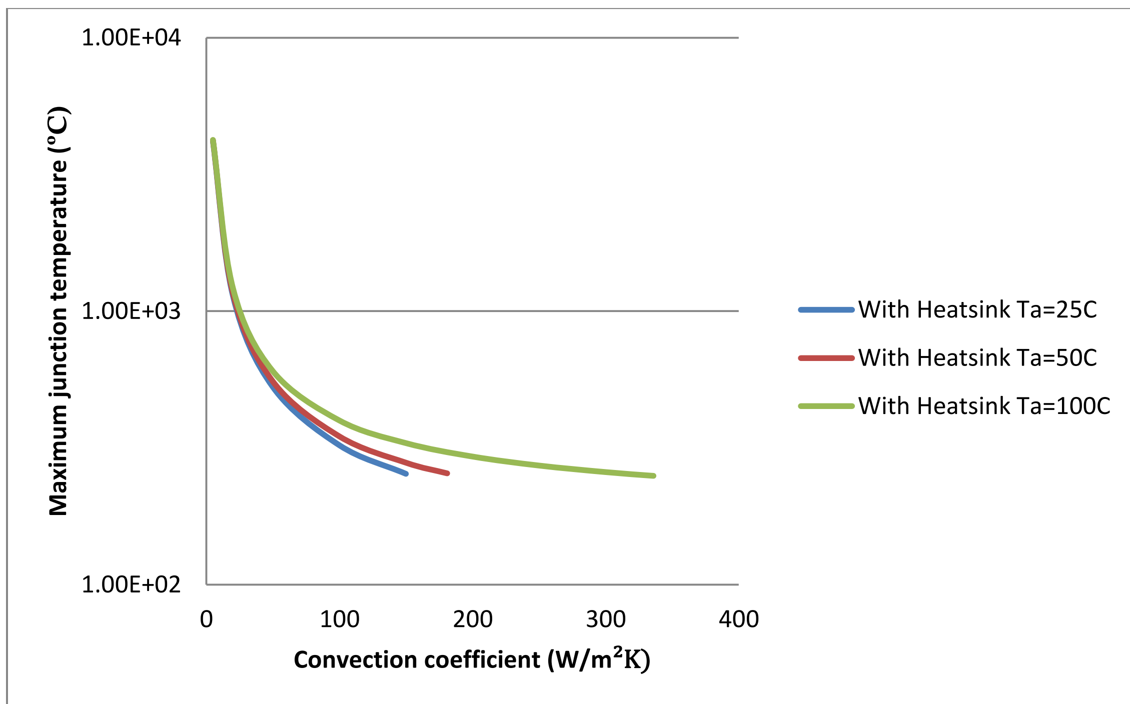


Figure 3.15. Convection coefficient versus maximum junction temperature (with BP and HS) for different ambient temperatures and 1.6KW power dissipation

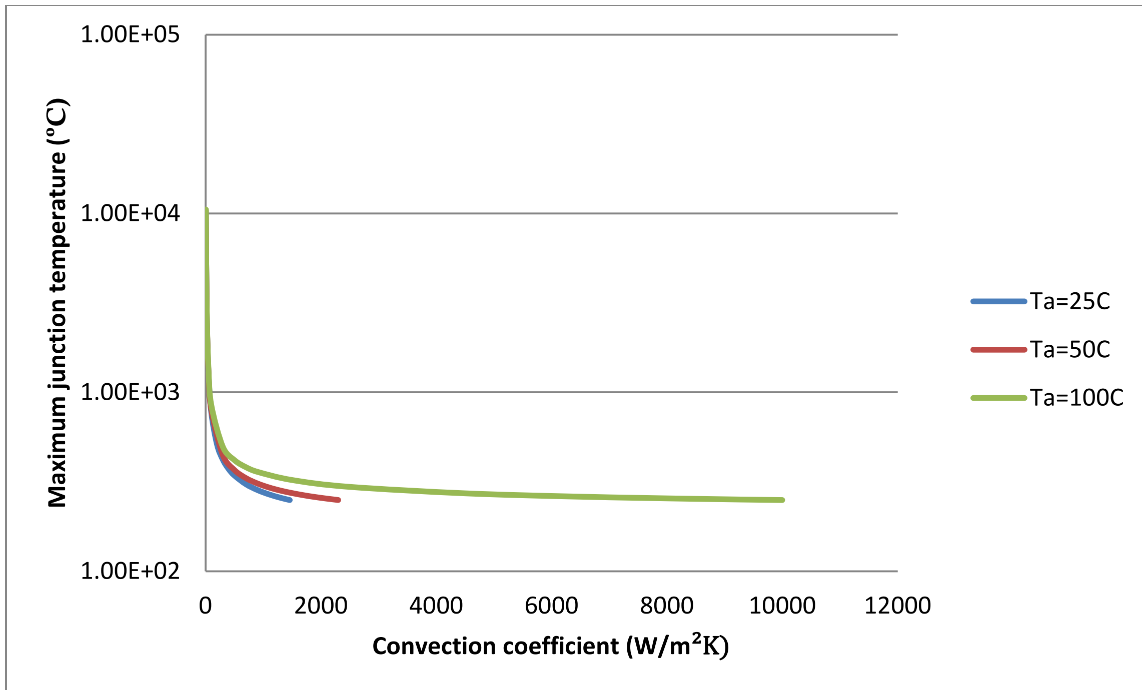


Figure 3.16. Convection coefficient versus maximum junction temperature (without BP or HS) for different ambient temperatures and 4KW power dissipation

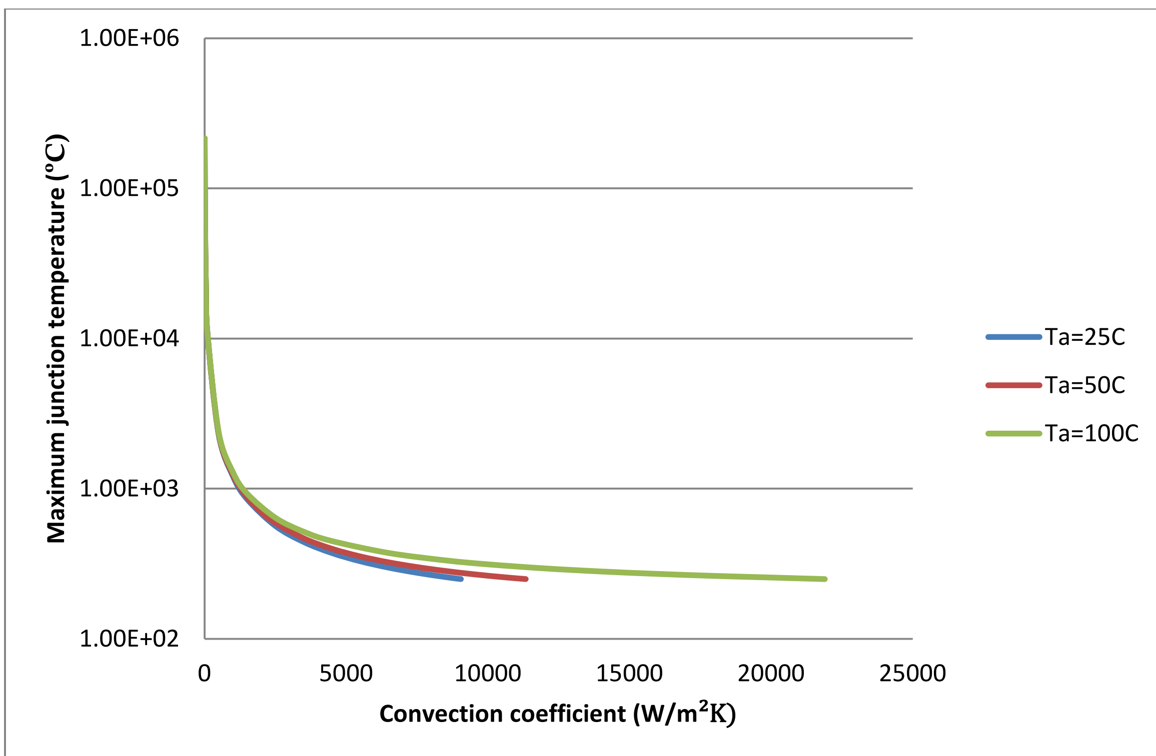


Figure 3.17. Convection coefficient versus maximum junction temperature (with BP and without HS) for different ambient temperatures and 4KW power dissipation

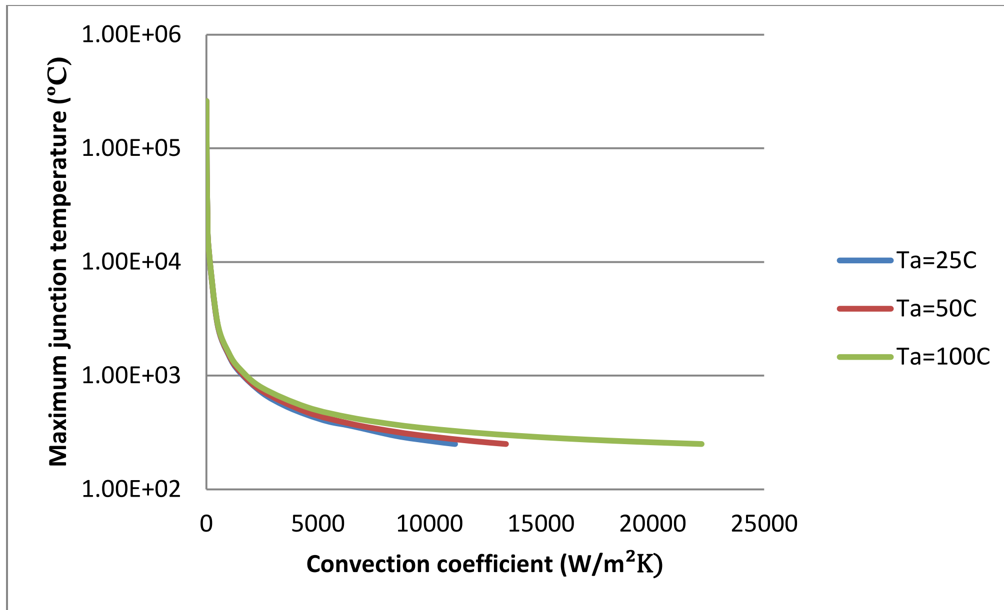


Figure 3.18. Convection coefficient versus maximum junction temperature (with BP and HS) for different ambient temperatures and 4KW power dissipation

From these plots, it is obvious that the lower the ambient temperature, the lower is the convection coefficient required to achieve a similar junction temperature. The greater is the difference between ambient temperature and junction temperature ($\Delta T = Tjmax \sim Ta$), the lower is the convection coefficient, and hence, a lower cost cooling system can be employed for good performance.

3.7 Study on power dissipation (heat generated by dies) variations

This section is to study the type of cooling needed to be employed for the power electronic module with changes in power dissipated by them. Different power devices (power semiconductor dies) have different thermal resistance and drain-to-source resistance. Hence, for the same current (or different currents) passes through the device, heat/power dissipation changes. In this section, total power dissipated by the module is varied from 640W to 3.2KW and the results are plotted. Another parameter considered here along with varying power is the ambient temperature (variation from 20ºC to 100ºC).

3D graphs are shown below which include power dissipation versus convection coefficient for various ambient temperatures and Tj = 250ºC:

- Without baseplate or heatsink (Figure 3.19)
- With baseplate (Figure 3.20)
- With heatsink (Figure 3.21)
- All the above three cases for comparision (Figure 3.22)

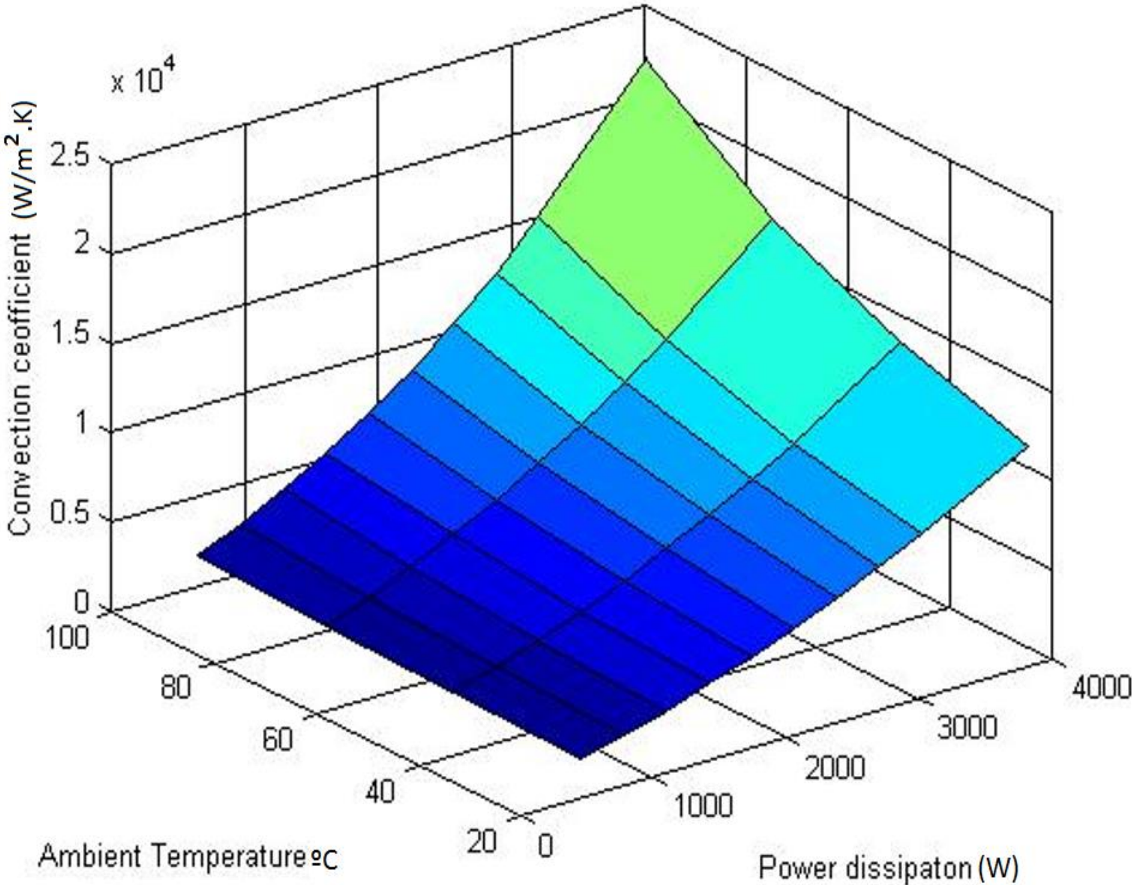


Figure 3.19. Power dissipation versus convection coefficient for various ambient temperatures, and Tj of 250ºC (without BP or HS condition)

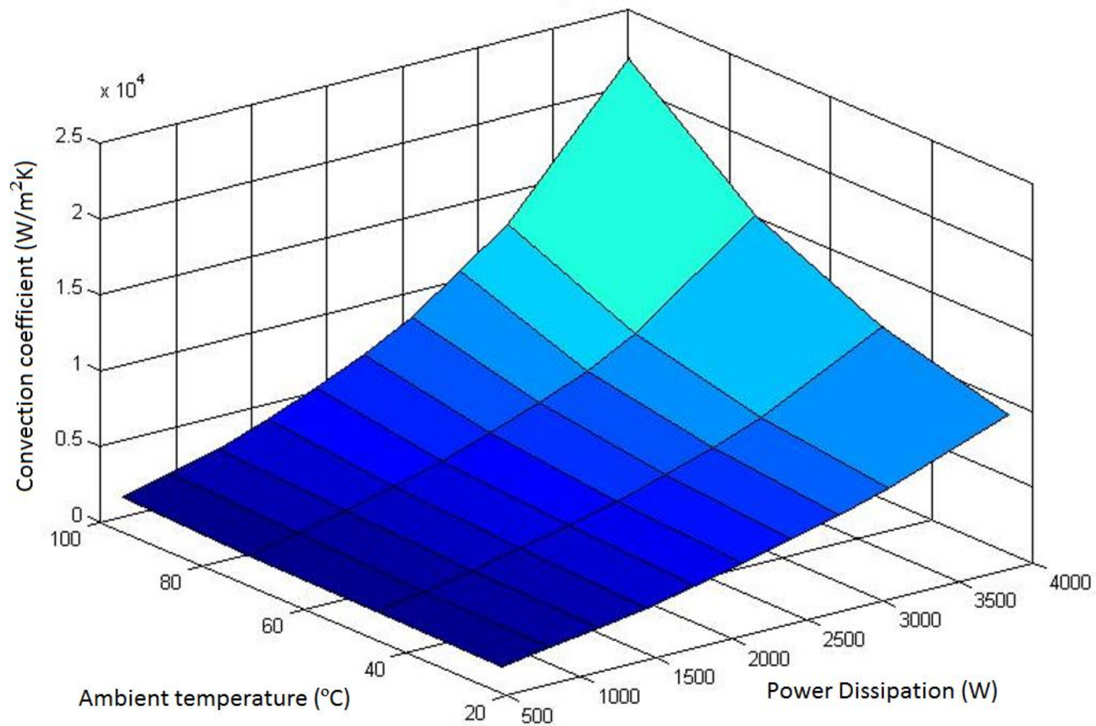


Figure 3.20. Power dissipation versus convection coefficient for various ambient temperatures, and Tj of 250ºC (with BP condition)

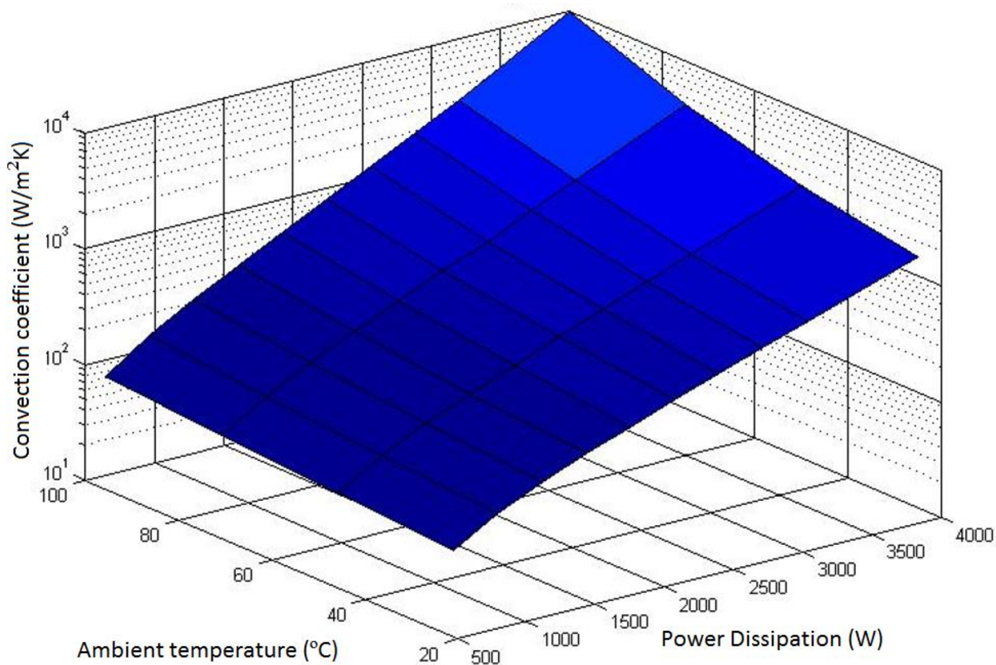


Figure 3.21. Power dissipation versus convection coefficient for various ambient temperatures, and Tj of 250ºC (with BP and HS condition)

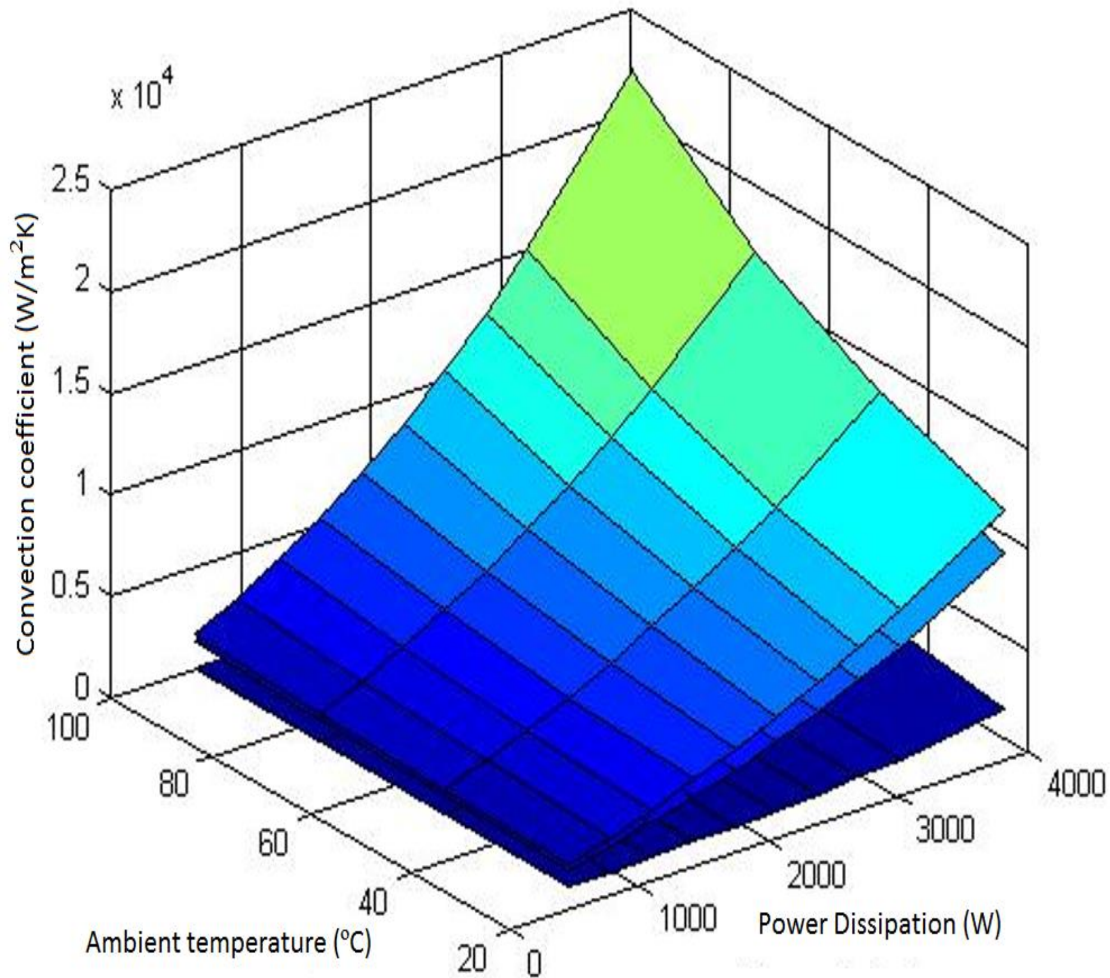


Figure 3.22. Power dissipation versus convection coefficient for various ambient temperatures, and Tj of 250ºC (all three cases for comparision)

3D graphs are shown which include power dissipation versus convection coefficient for various ambient temperatures and Tj = 200ºC for:

- Without baseplate or heat-sink (Figure 3.23)
- With baseplate (Figure 3.24)
- With heatsink (Figure 3.25)
- All the above three cases for comparision (Figure 3.26)

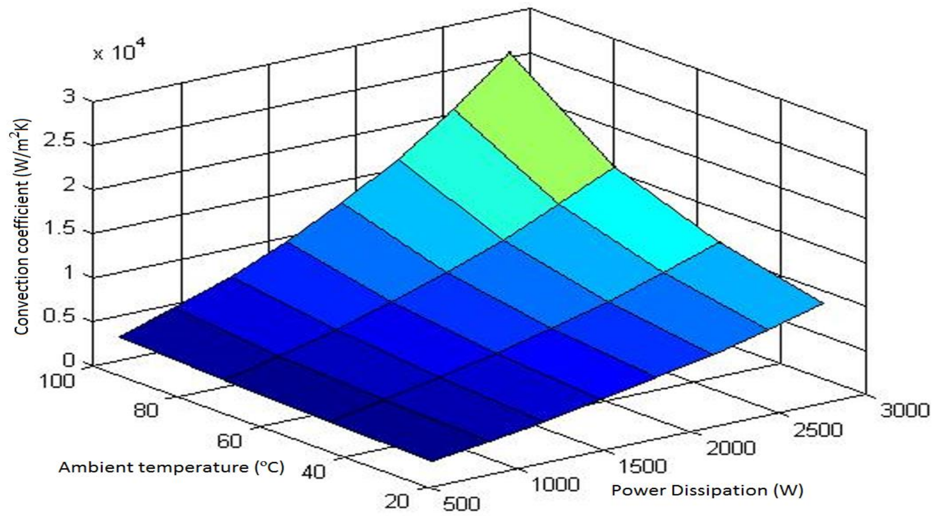


Figure 3.23. Power dissipation versus convection coefficient for various ambient temperatures, and Tj of 200ºC (without BP or HS condition)

From these figures, it is self-explanatory that the lower the power dissipated by the module, the lower convection coefficient is required to achieve the same junction temperature.

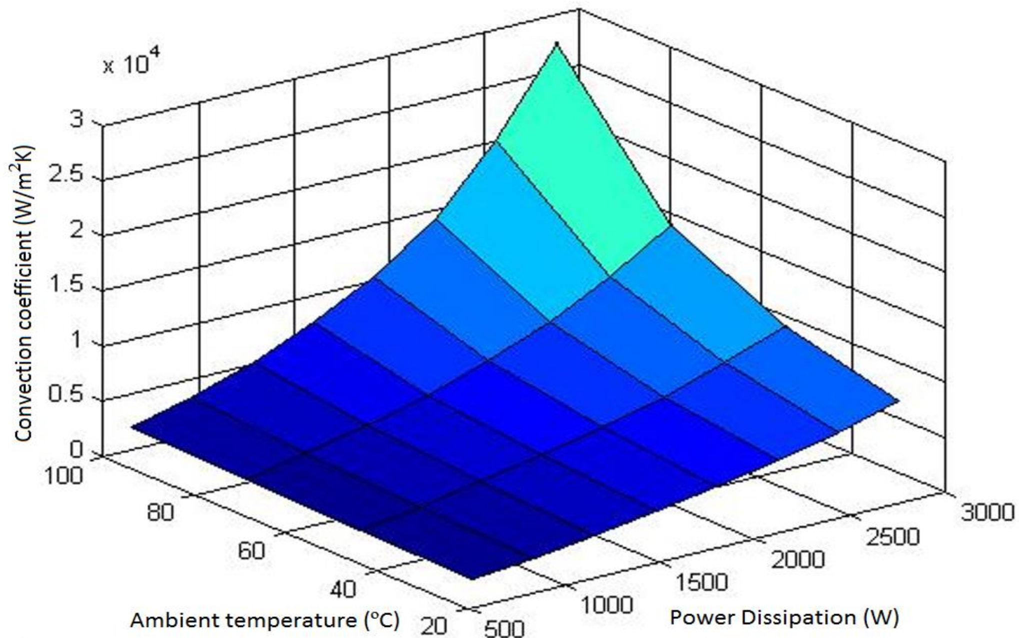


Figure 3.24. Power dissipation versus convection coefficient for various ambient temperatures, and Tj of 200ºC (with BP condition)

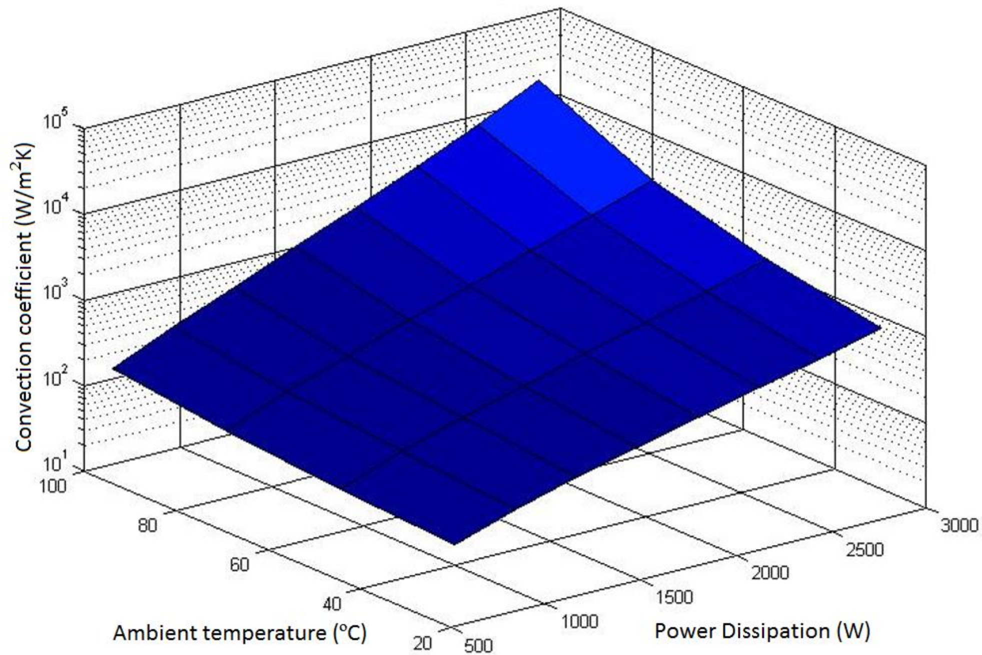


Figure 3.25. Power dissipation versus convection coefficient for various ambient temperatures, and Tj of 200ºC (with BP or HS condition)

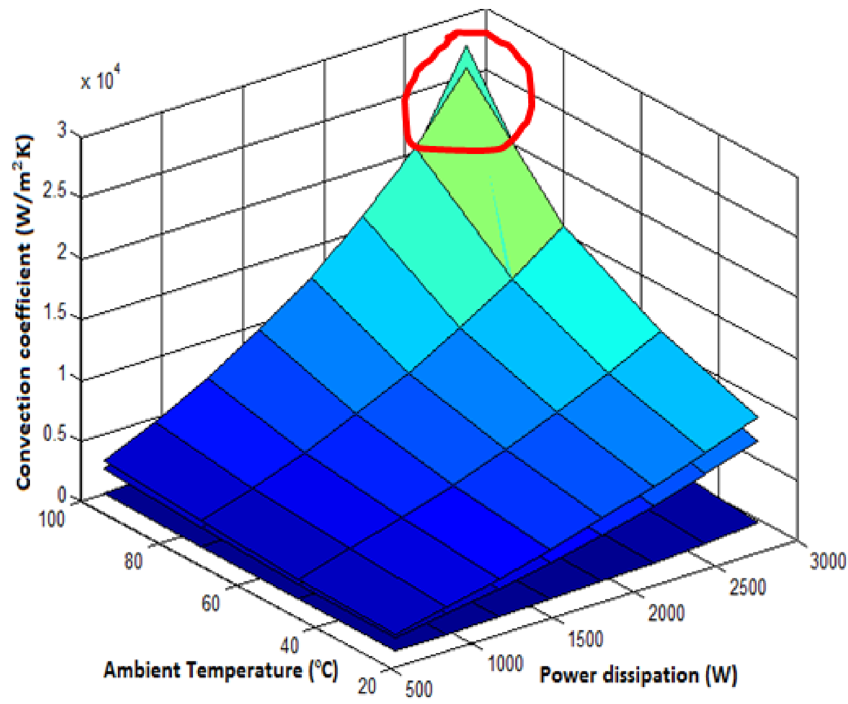


Figure 3.26. Power dissipation versus convection coefficient for various ambient temperatures, and Tj of 200ºC (all three cases for comparision)

Figure 3.26 shows that, for most range of ambient temperature, and power dissipation conditions, the convection coefficient required to maintain the maximum junction temperature of 200ºC is lower when baseplate is attached when compared to when baseplate is not attached to the substrate. However after a certain range, that is, at high power dissipation and high ambient temperature conditions, the convection coefficient required to maintain 200ºC is more when baseplate is attached to substrate than when baseplate is not attached to the substrate. This is because for high power dissipation and low ΔT, baseplate acts more like a thermal resistor than a heat-spreader. This inceases the convection coefficient, and hence, decreasing the ease at which excess heat is removed from the substrate. Thus a designer needs to take precautions or decide whether it is advantageous or disadvantageous to employ baseplate in a design for certain parameters.

Two dimensional representaions for some of the results are shown in Figure 3.27 and 3.28.

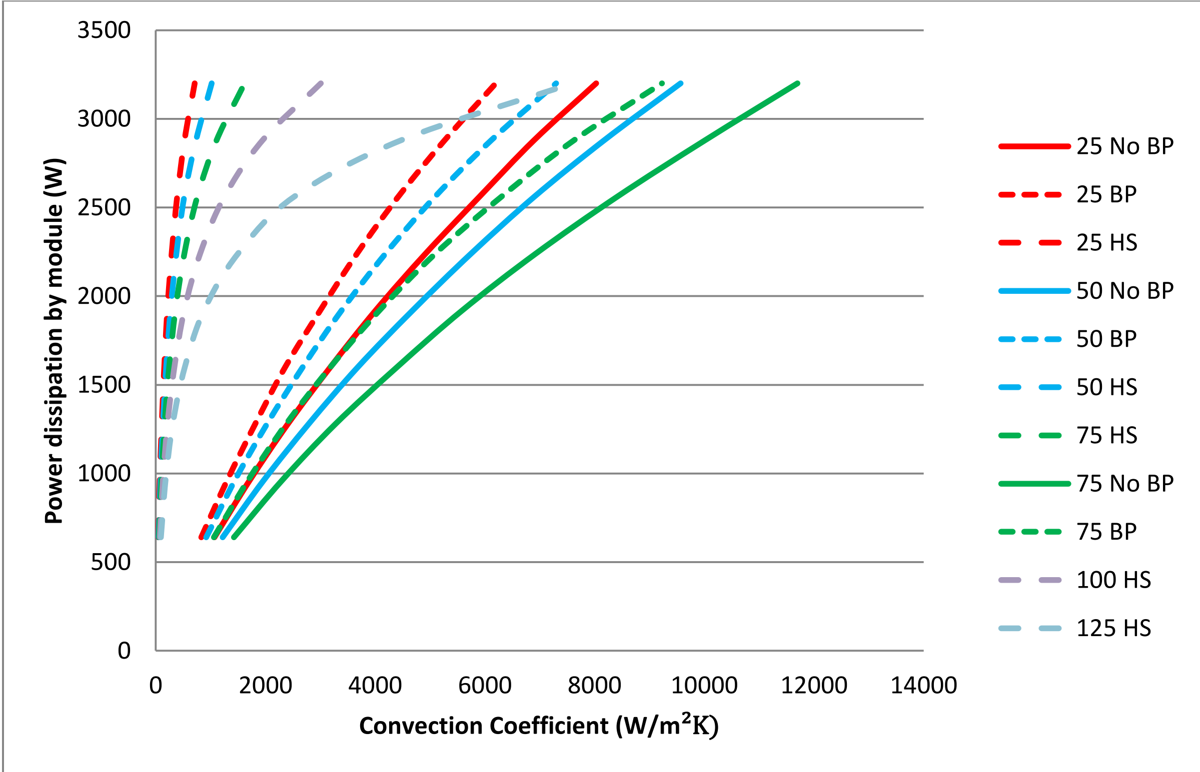


Figure 3.27. Convection coefficient versus power dissipation for few cases.

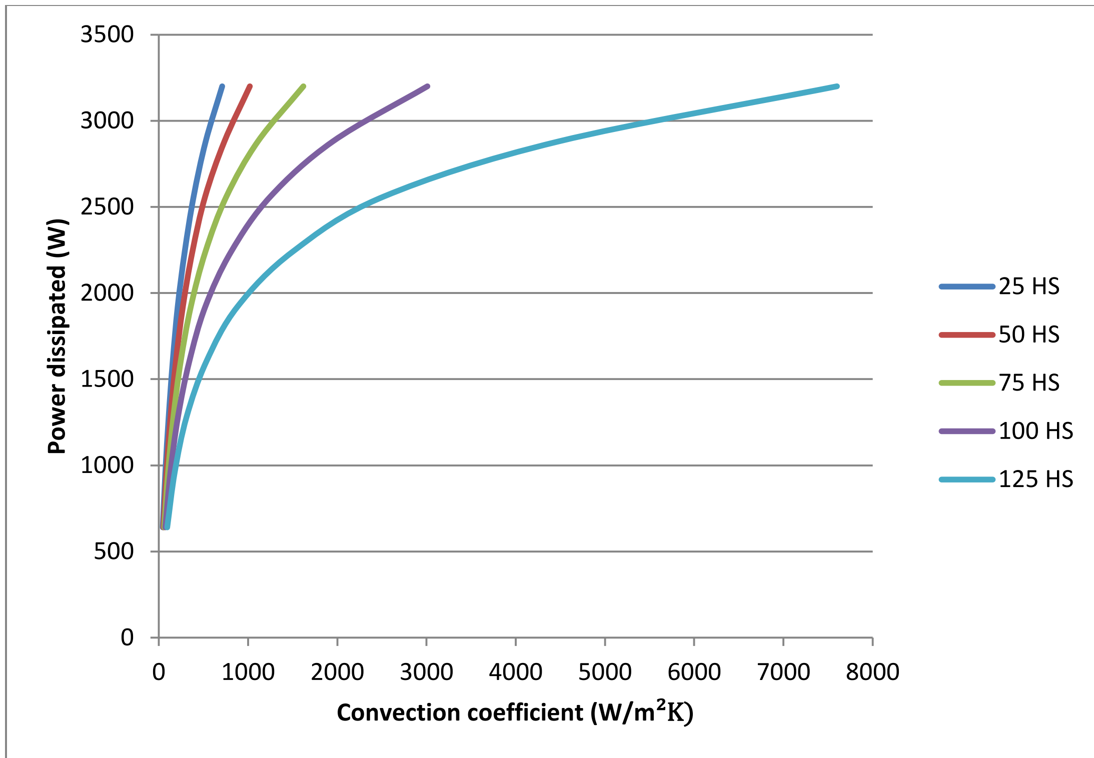


Figure 3.28(a). Convection coefficient versus power dissipation with different ambient temperatures (with BP and HS condition)

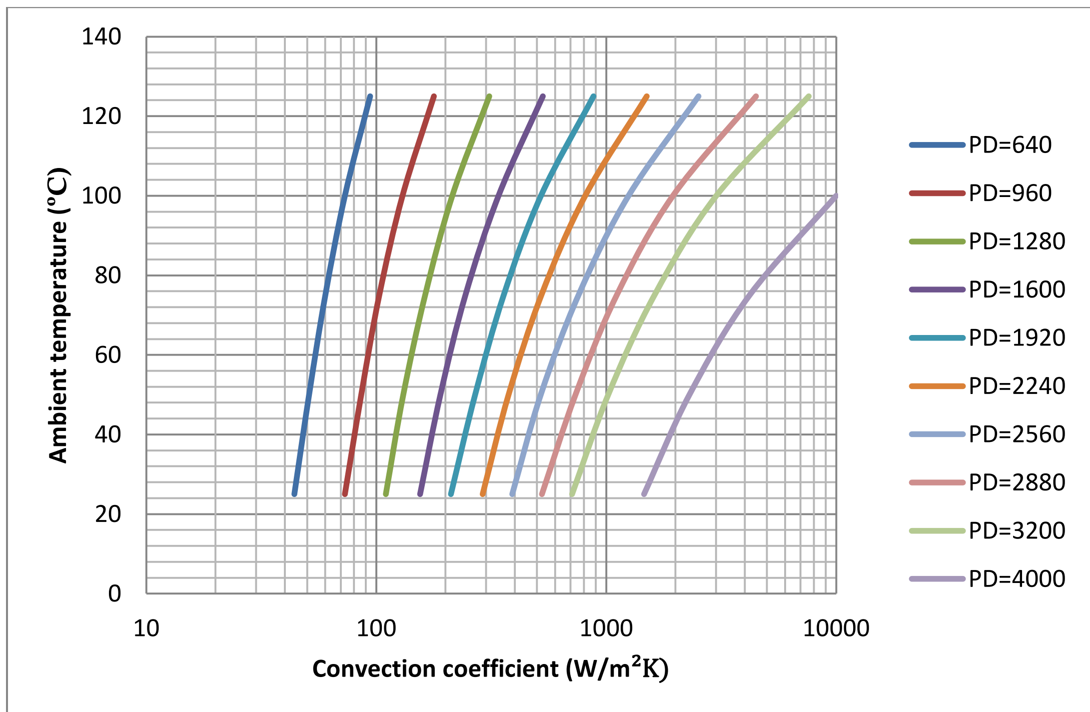


Figure 3.28(b). Convection coefficient versus ambient temperature for different power dissipations.

The results from Figure 3.28(a) are used to plot Figure 3.28(b) but with a different axis. This plot is used later in this chapter to help in choosing the optimum substrate size for an example.

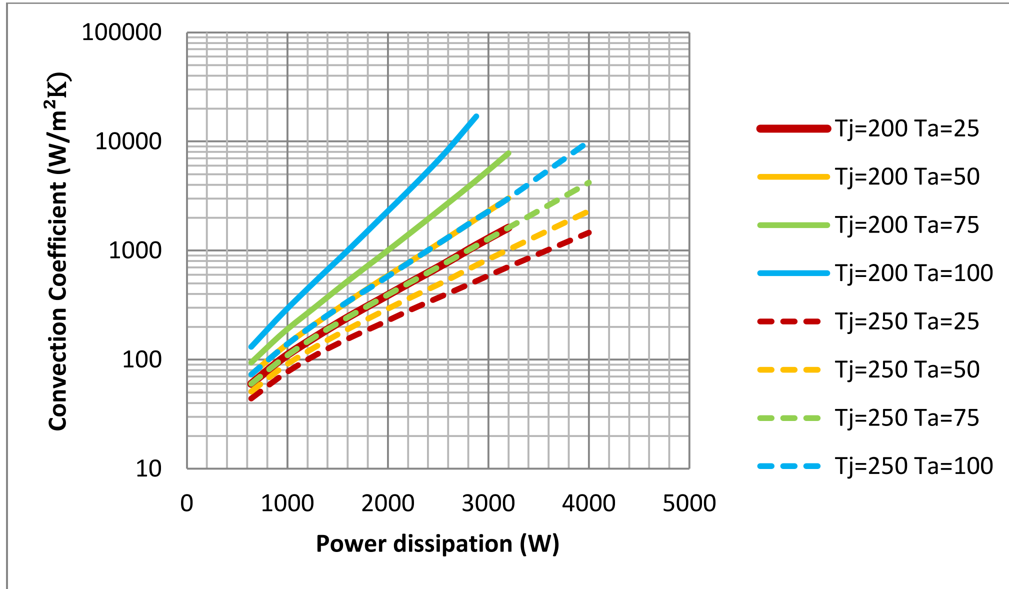


Figure 3.28(c). Semilog plot for power dissipation versus convection coefficient with different ambient temperatures (with BP and HS condition)

Since ΔT = Tjmax – Ta, so as the ΔT increases, the convection coefficient decreases for same power dissipation. This ΔT can be increased by using lower ambient temperatures. As seen in the above plots - despite employing heatsinks, for the case of 3.2KW power dissipation, 250ºC maximum junction temperature, and ambient temperatures of 25ºC, 50ºC, 75ºC, 100ºC, 125ºC; the convection coefficients required are 710, 1020, 1620, 3010, and 7600 W/m^{2}K, respectively. Also for 2.5KW power dissipation and 200ºC maximum junction temperature, and ambient temperatures of 25ºC, 50ºC, 75ºC, 100ºC; the convection coefficients required are 750, 1250, 2550, 7700 W/m^{2}K, respectively. That is, as it reaches ΔT of 125ºC, convection coefficient values double. Hence for optimum functioning, it is best to maintain ΔT > 125ºC. This is observed in all cases in the above Figure 3.28(c). However as power dissipation increases (beyond 4KW), convection coefficient doubles much earlier. Then the ΔT increases correspondingly. That range is not investigated in this thesis work.

3.8 Study on varying baseplate size

Baseplate, as mention in Section 3.4, provides mechanical strength and balanced thermal distribution over the power substrate. As discussed in Section 3.4, copper metal is used for baseplate. Simulations are performed for a constant substrate size as well as for increase in size of baseplate from 5% to 50% without the heatsink.

Figures 3.29, 3.30, 3.31, 3.32, 3.33, and 3.34 are shown below to illustrate the variation of baseplate and its corresponding effect on other parameters.

- Parameters Ta = 100ºC, Power dissipation = 1.6KW, 2.5KW, 4KW. Tj = 250ºC

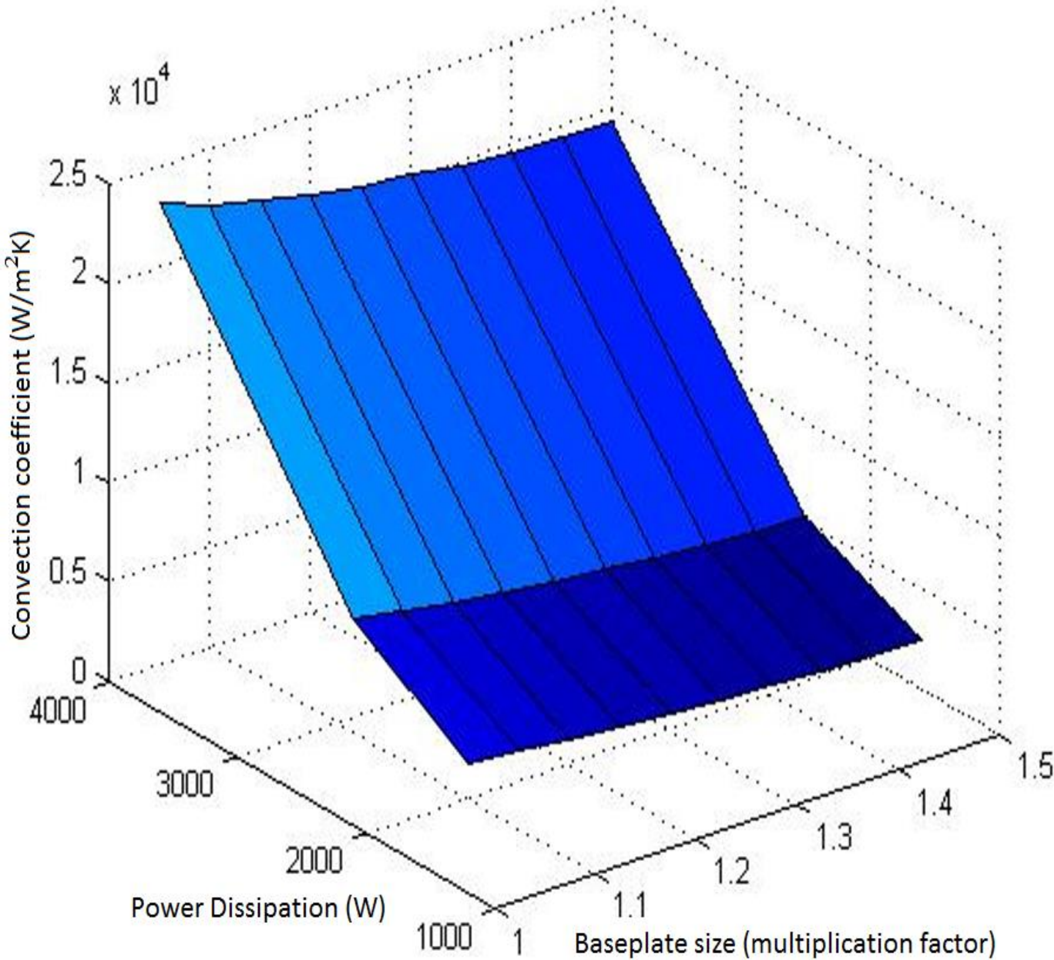


Figure 3.29. Baseplate size versus power dissipation and convection coefficient for Ta of 100ºC and Tjmax of 250ºC

- Parameters Ta = 100ºC, 125ºC. Power dissipation = 1.6KW, 2.5KW. Tj = 250ºC

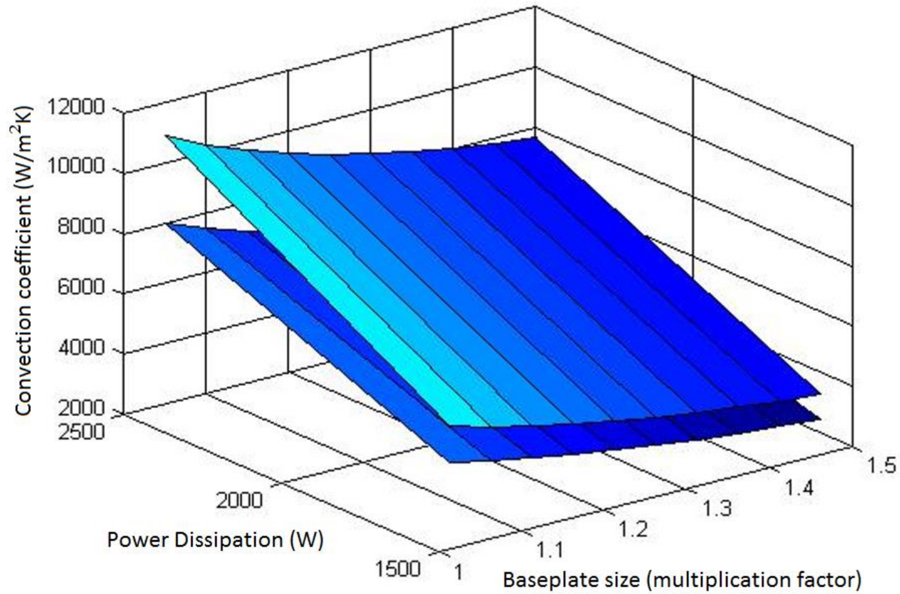


Figure 3.30. Baseplate size versus power dissipation and convection coefficient for different ambient temperatures of 100ºC, 125ºC and Tjmax of 250ºC. Two cases of ambient temperatures are plotted to show comparison

- Parameters Ta = 100ºC, Power dissipation = 2.5KW.

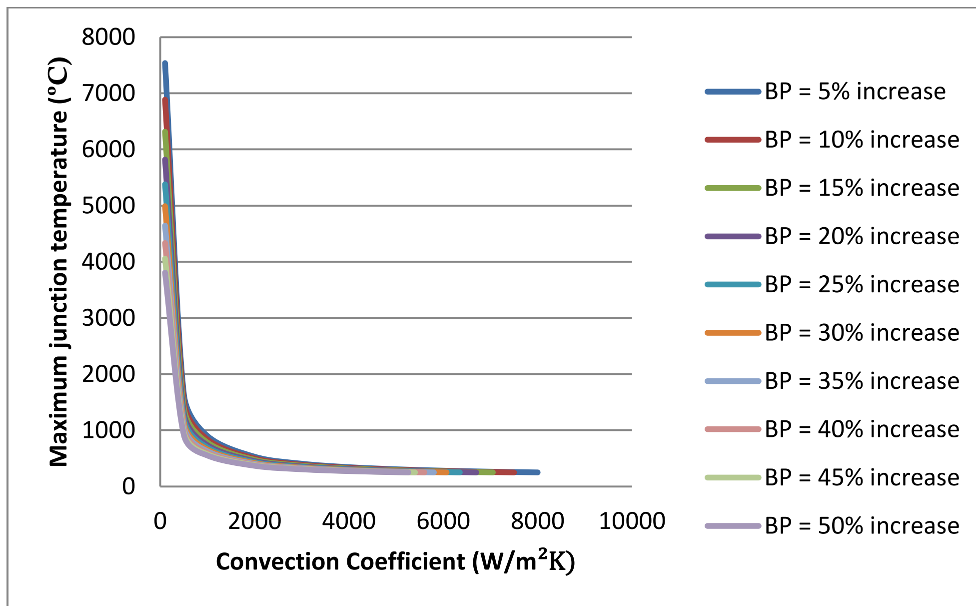


Figure 3.31. Convection coefficient versus maximum junction temperature for different baseplate sizes, and for 2.5KW power dissipation

- Parameters Ta = 100ºC, Power dissipation = 1.6KW.

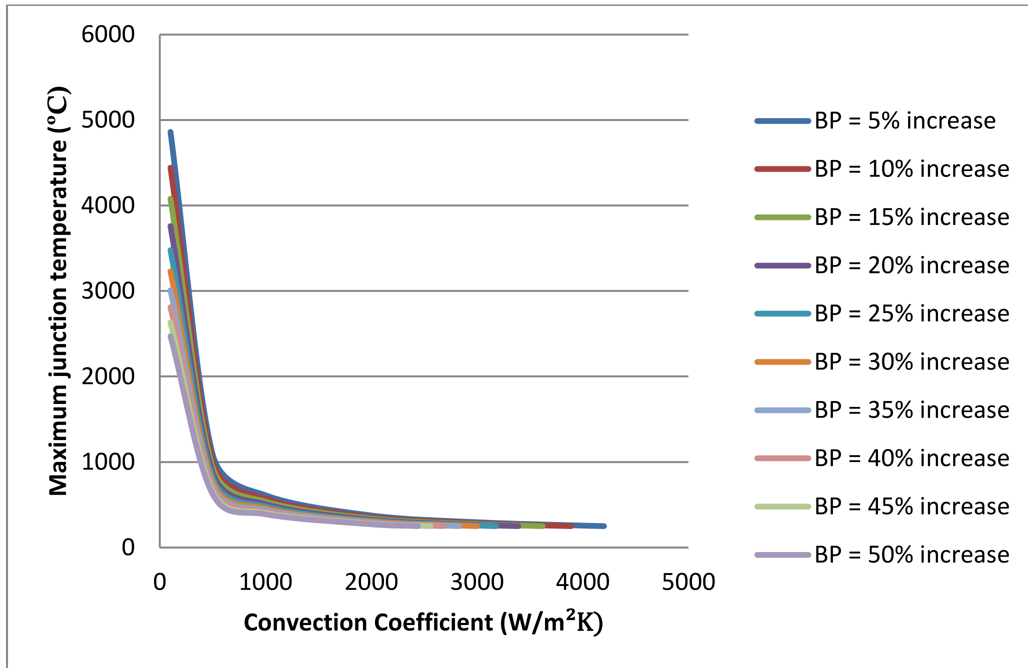


Figure 3.32. Convection coefficient versus maximum junction temperature for different baseplate sizes, and for 1.6KW power dissipation

- Parameters Ta = 125ºC, Power dissipation = 2.5KW.

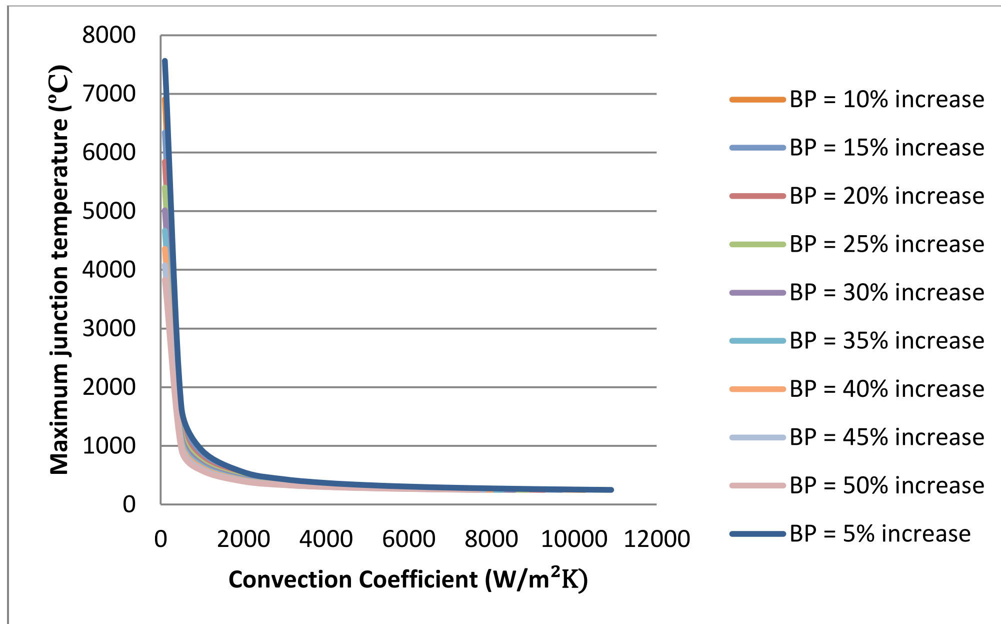


Figure 3.33. Convection coefficient versus maximum junction temperature for different baseplate sizes, and for 2.5KW power dissipation

- Parameters Ta = 125ºC, Power dissipation = 1.6KW.

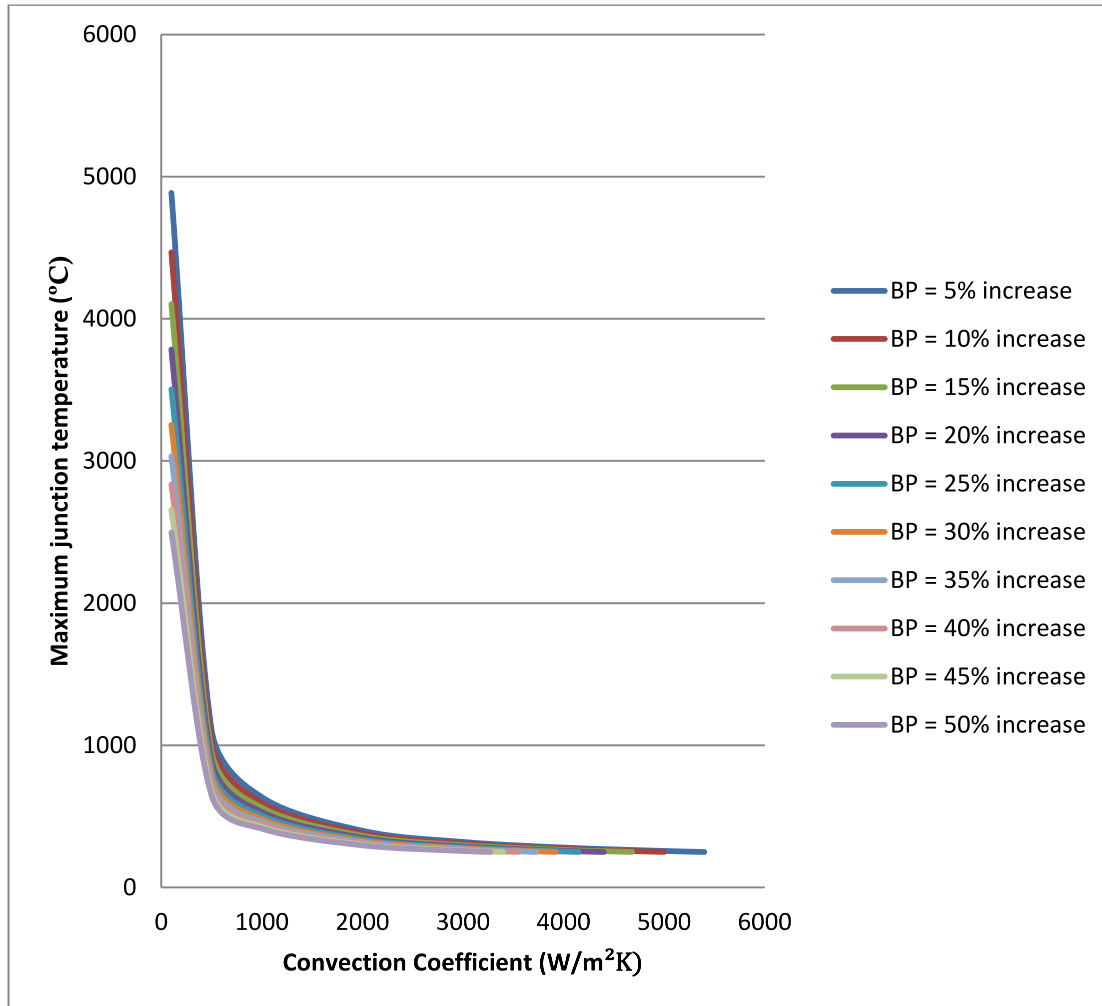


Figure 3.34. Convection coefficient versus maximum junction temperature for different baseplate sizes, and for 1.6KW power dissipation

As can be seen from Figures 3.31 to 3.34, Tjmax varies rapidly with increase in convection coefficient until 1000W/m^{2}K is reached. After this, the plots take sharp turn and continue to behave almost constant (varying only by a little).

- For Tjmax = 250ºC, the convection coefficient versus baseplate percentage size increase is plotted in Figure 3.35 for various parameters of power dissipation of 2.5KW, 1.6KW and ambient temperature of 100ºC, 125ºC.

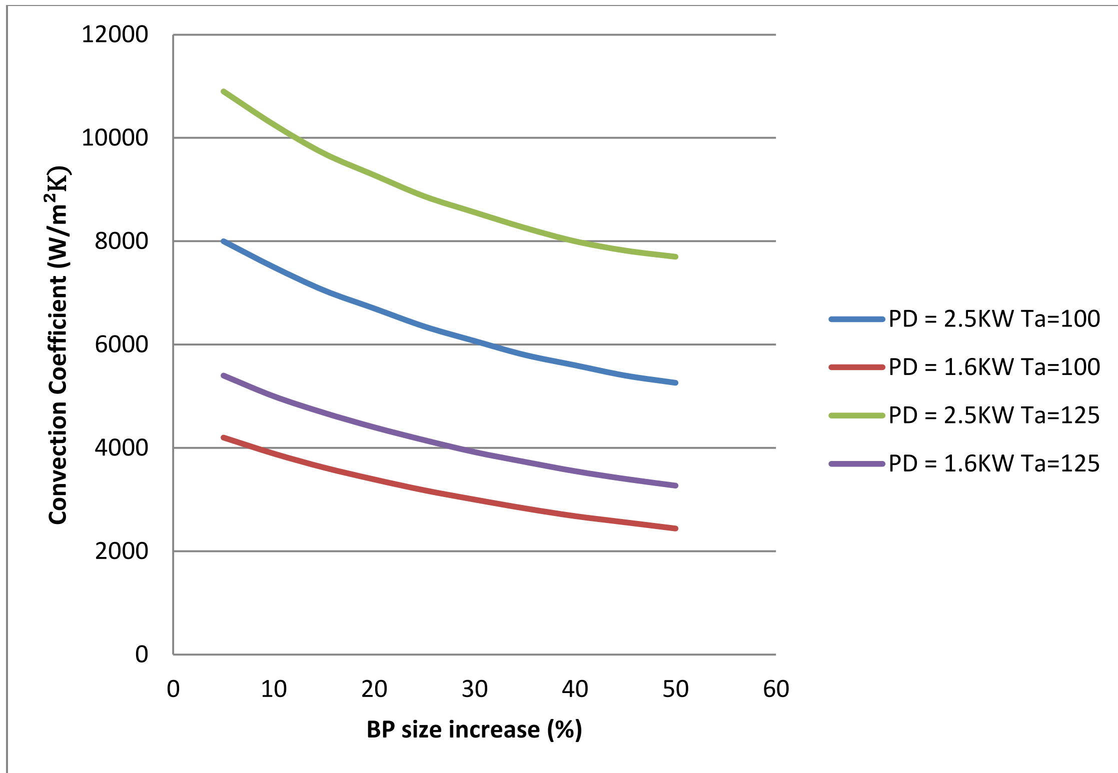


Figure 3.35. Baseplate size increase versus convection coefficient for 2.5KW and 1.6KW power dissipation, and 100ºC and 125ºC ambient temperatures

It is straight forward to see from the graph that the larger the baseplate the better would be the heat spreading, and hence, a better heat removal aid for the module provided the thickness of the baseplate remains constant.

3.9 Study on varying heat-sink size

As discussed in Section 3.5.2, 1050A Al alloy is chosen for the heatsink material. Simulations are performed for a constant substrate size; increase the size of both baseplate and heatsink - thus increasing the exposed surface area - from 5% to 50%. When size of the heatsink is increased, it may be possible to add a fin to the heatsink thus adding a thermal resistance in parallel.

Plots in this section provide study on variation of the size of heatsink and its corresponding effect on other parameters. Figures 3.36 and 3.37 show the three dimensional plots.

- Parameters Ta = 100ºC, Power dissipation = 1.6KW, 2.5KW, 4KW. Tj = 250ºC

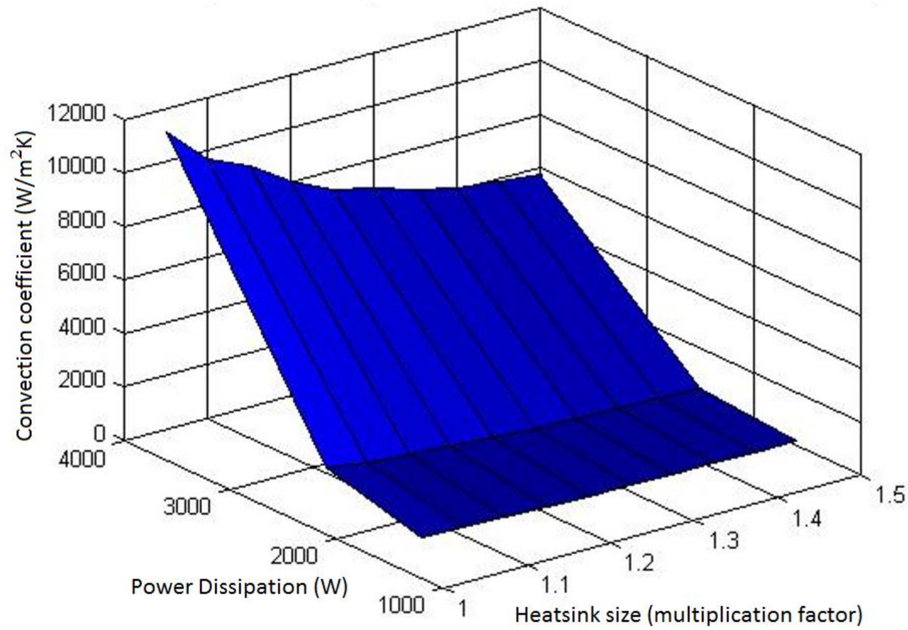


Figure 3.36. Heatsink size variation versus power dissipation and convection coefficient for ambient temperature of 100ºC and Tjmax of 250ºC

- Parameters Ta = 100ºC, 125ºC. Power dissipation = 1.6KW, 2.5KW. Tj = 250ºC

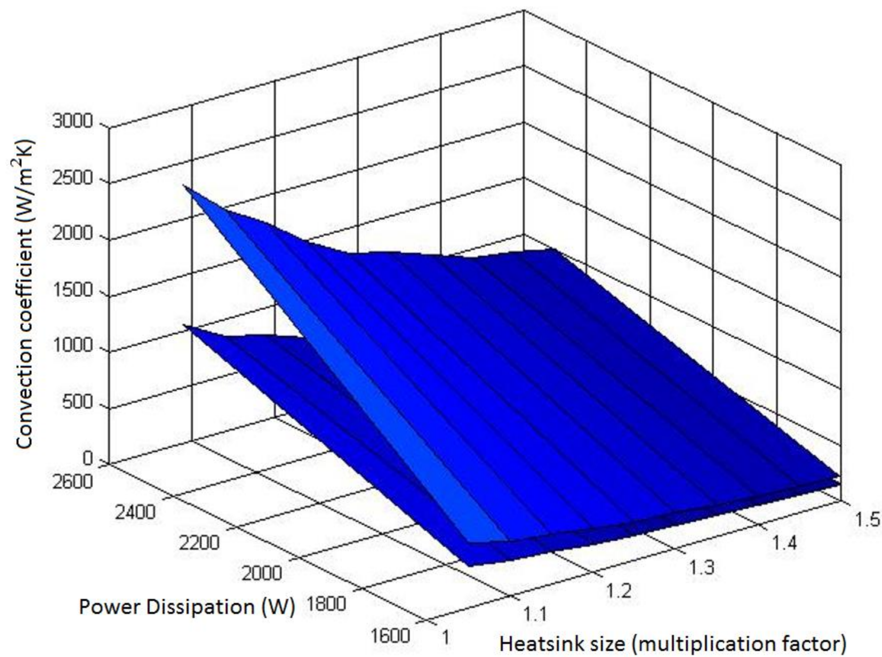


Figure 3.37. Heatsink size variation versus power dissipation and convection coefficient for ambient temperatures 100ºC, 125ºC (to show the comparison) and Tjmax 250ºC

- Parameters Ta = 100ºC, Power dissipation = 2.5KW.

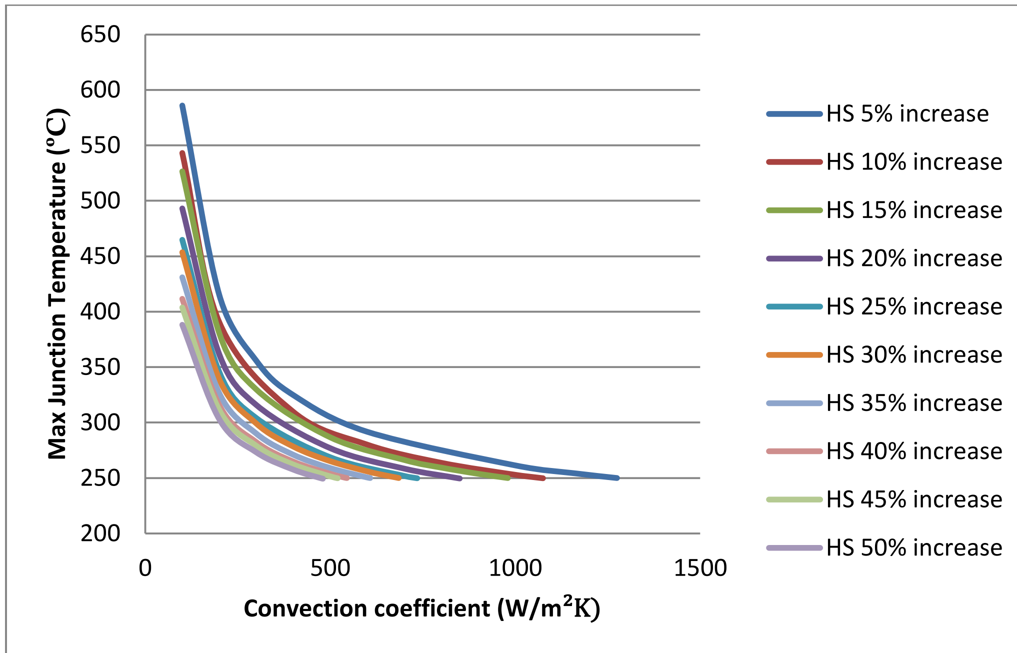


Figure 3.38. Convection coefficient versus maximum junction temperature for different heatsink sizes for 2.5KW power dissipation

- Parameters Ta = 100ºC, Power dissipation = 1.6KW.

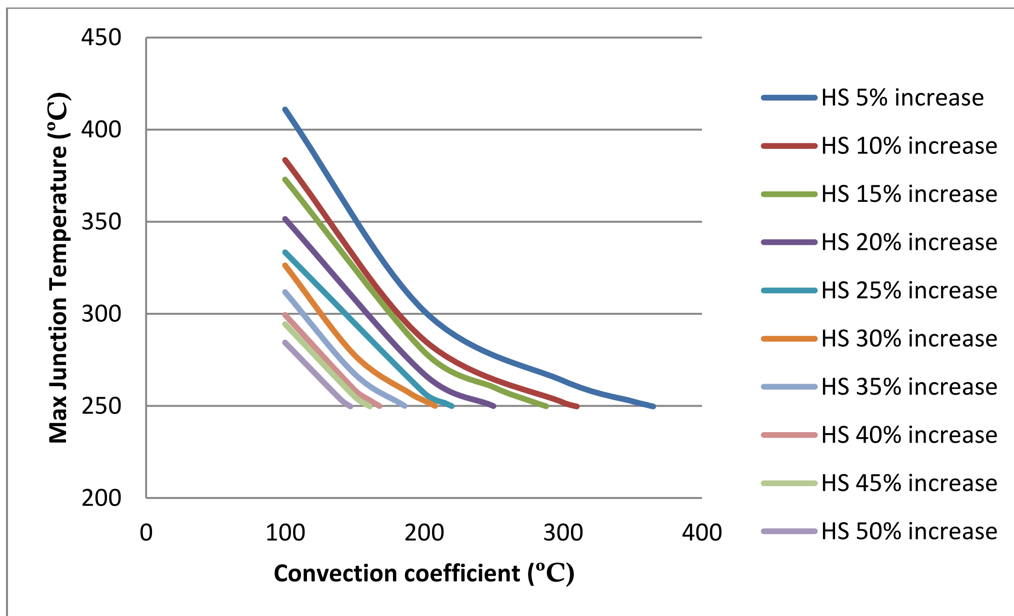


Figure 3.39. Convection coefficient versus maximum junction temperature for different heatsink sizes for 1.6KW power dissipation

- Parameters Ta = 125ºC, Power dissipation = 2.5KW.

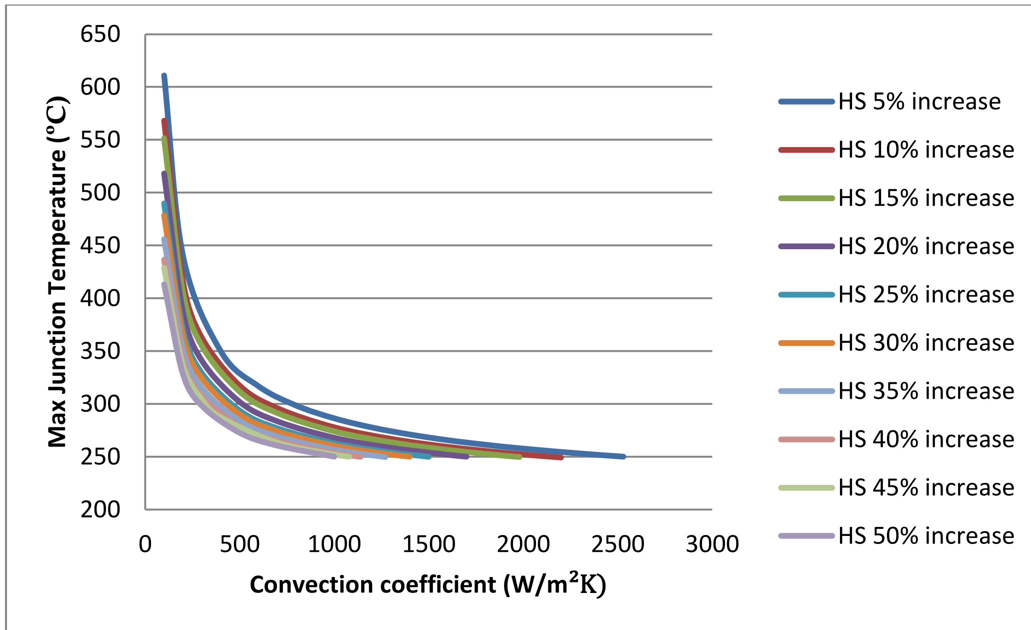


Figure 3.40. Convection coefficient versus maximum junction temperature for different heatsink sizes for 2.5KW power dissipation

- Parameters Ta = 125ºC, Power dissipation = 1.6KW.

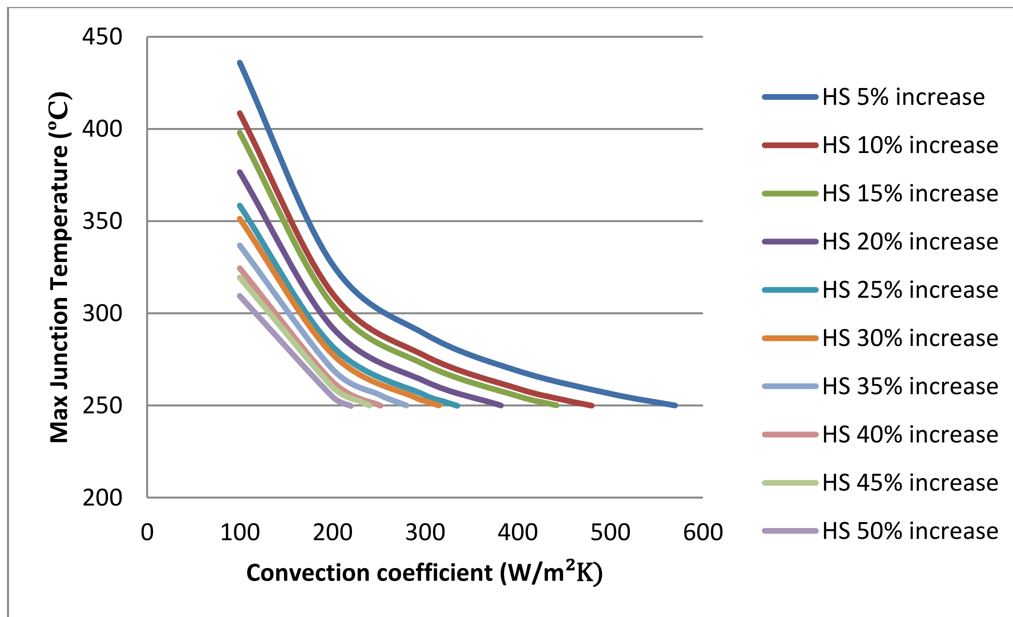


Figure 3.41. Convection coefficient versus maximum junction temperature for different heatsink sizes for 1.6KW power dissipation

- To obtain Tjmax = 250ºC, the convection coefficient versus heatsink size increase for various parameters is given in Figure 3.42.

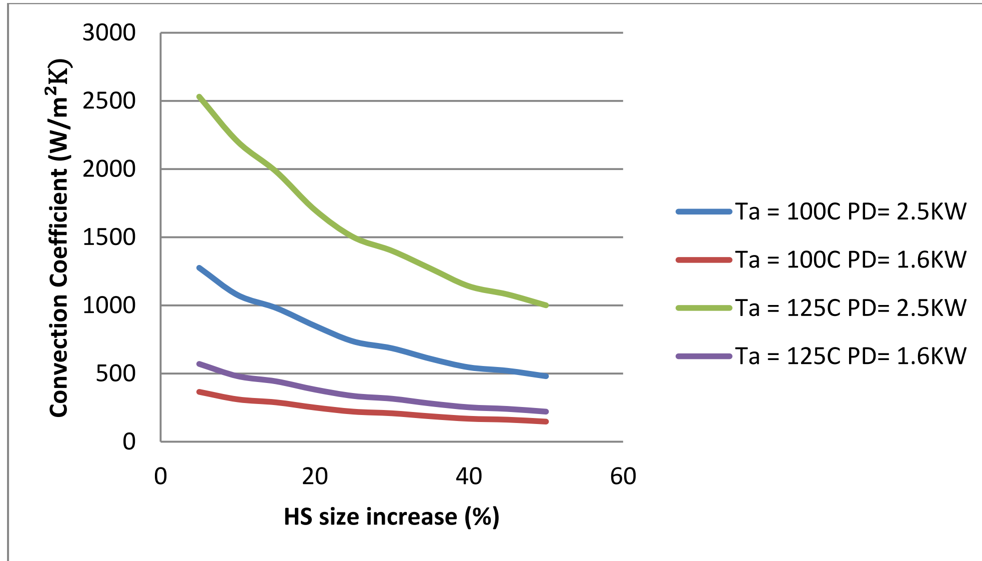


Figure 3.42. Convection coefficient versus heatsink size increase

As can be seen in Figure 3.42, for power dissipation=2.5KW and Ta=125ºC, the change in convection coefficient is from 2500W/m²K to 1000W/m²K, whereas, for power dissipation=1.6KW and Ta=100ºC, the change in convection coefficient is only from around 360 W/m²K to 150 W/m²K. That is, there is a significant change in convection coefficient when increasing the size of heatsink for higher power (dissipation) modules than for low power dissipation modules.

3.10 Study on varying substrate (DBC) size

Increasing the substrate size increases the surface area and helps in better heat spreading. Also, the spacing between the dies increases thus reducing thermal coupling in the layout. So theoretically, increasing the substrate size would need a lower convection coefficient for the same Tj according to Newton's cooling law. Figures 3.44, 3.45, 3.46, 3.47, 3.48, 3.49, 3.50, 3.51, 3.52, and 3.53 show the effects of increasing the substrate size on other parameters.

- Parameters Ta = 100ºC, Power dissipation = 1.6KW, 2.5KW, 4KW. Tjmax = 250ºC, without baseplate condition.

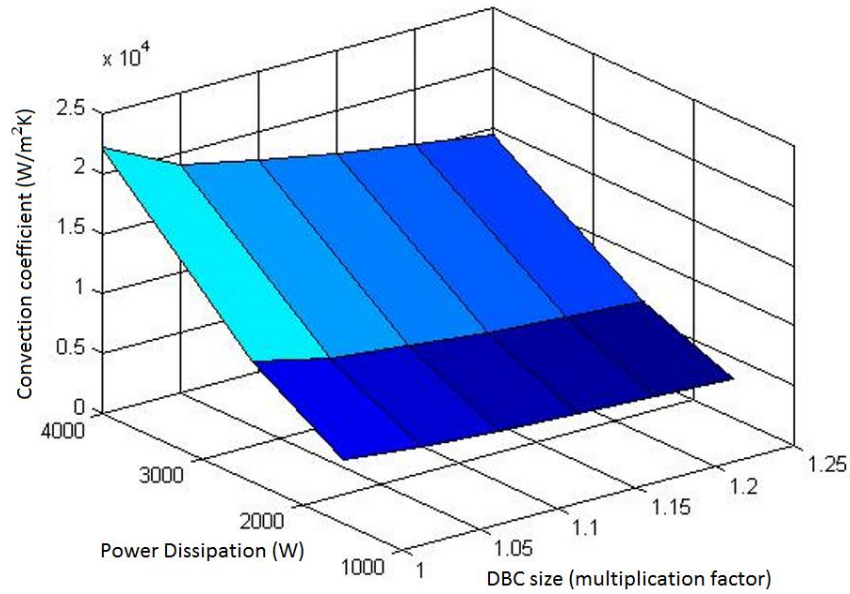


Figure 3.43. Convection coefficient versus power dissipation and substrate size for Tjmax=250ºC (no BP or HS condition)

- Parameters Ta = 100ºC, Power dissipation = 1.6KW, 2.5KW, 4KW. Tjmax = 250ºC, with baseplate condition

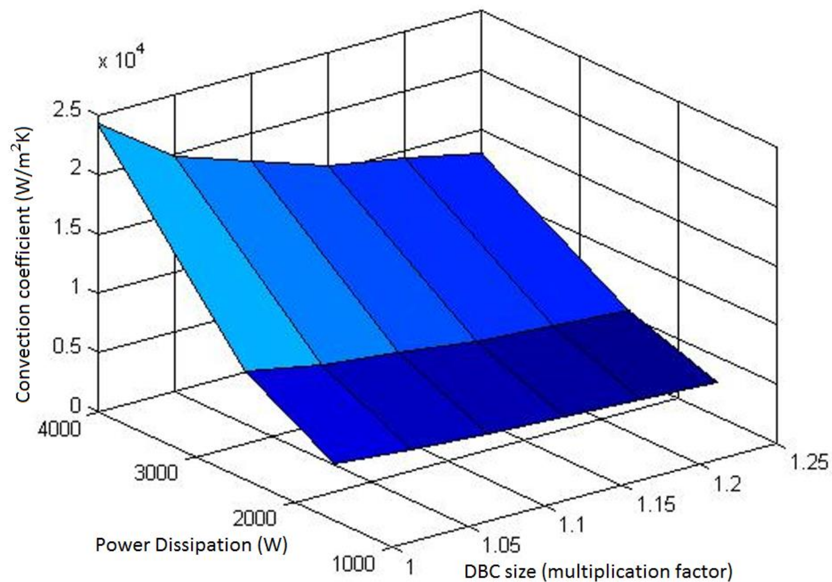


Figure 3.44. Convection coefficient versus power dissipation and DBC size for Tjmax=250ºC (with BP condition)

- Parameters Ta = 100ºC, Power dissipation = 1.6KW, 2.5KW, 4KW. Tjmax = 250ºC, with heatsink condition

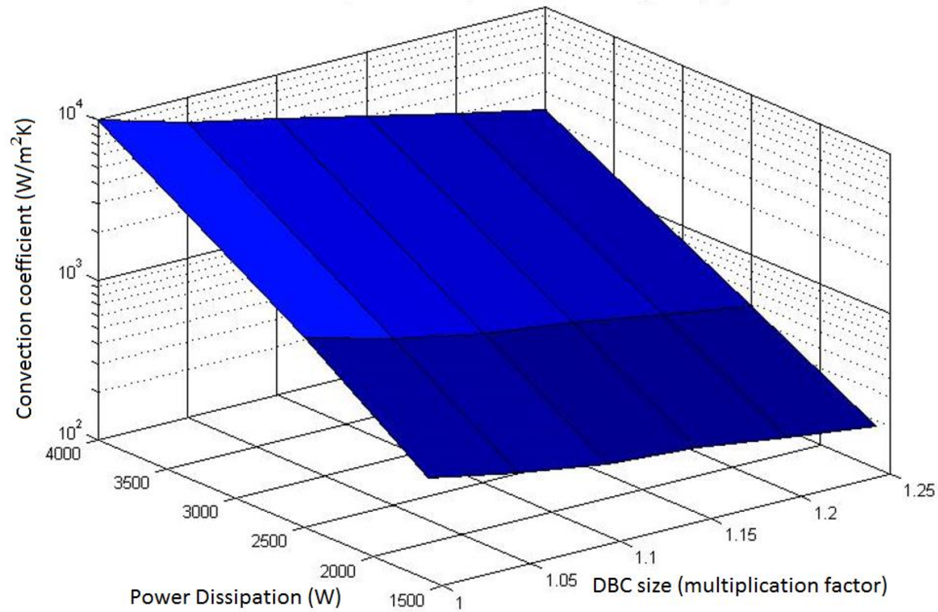


Figure 3.45. Convection coefficient versus power dissipation and DBC size for Tjmax=250ºC; (with HS condition)

- Parameters Ta = 100ºC, Power dissipation = 1.6KW, 2.5KW, 4KW. Tjmax = 250ºC

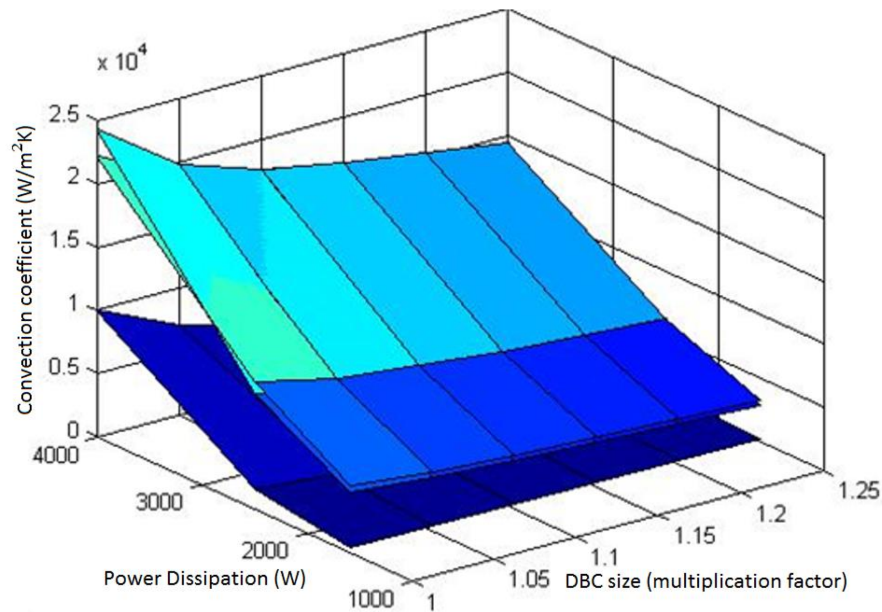


Figure 3.46. Convection coefficient versus power dissipation and DBC size for Tjmax=250ºC; all three cases

- Parameters: Ta = 100ºC, Power dissipation = 1.6KW, without baseplate or heat-sink condition

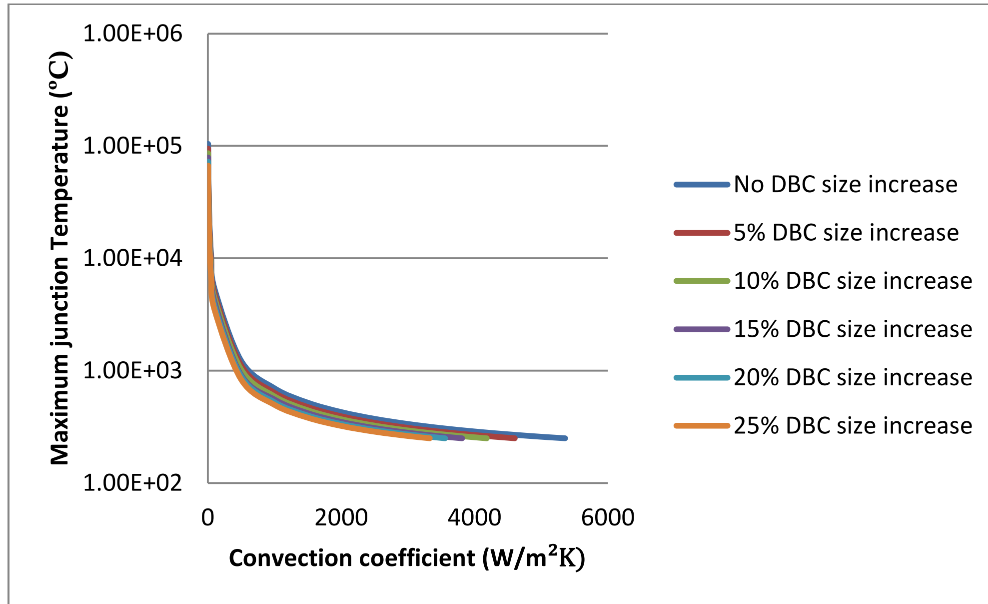


Figure 3.47. Convection coefficient versus maximum junction temperature for various DBC sizes, Power dissipation 1.6KW (without BP or HS condition)

- Parameters: Ta = 100ºC, Power dissipation = 1.6KW, with baseplate but no heatsink

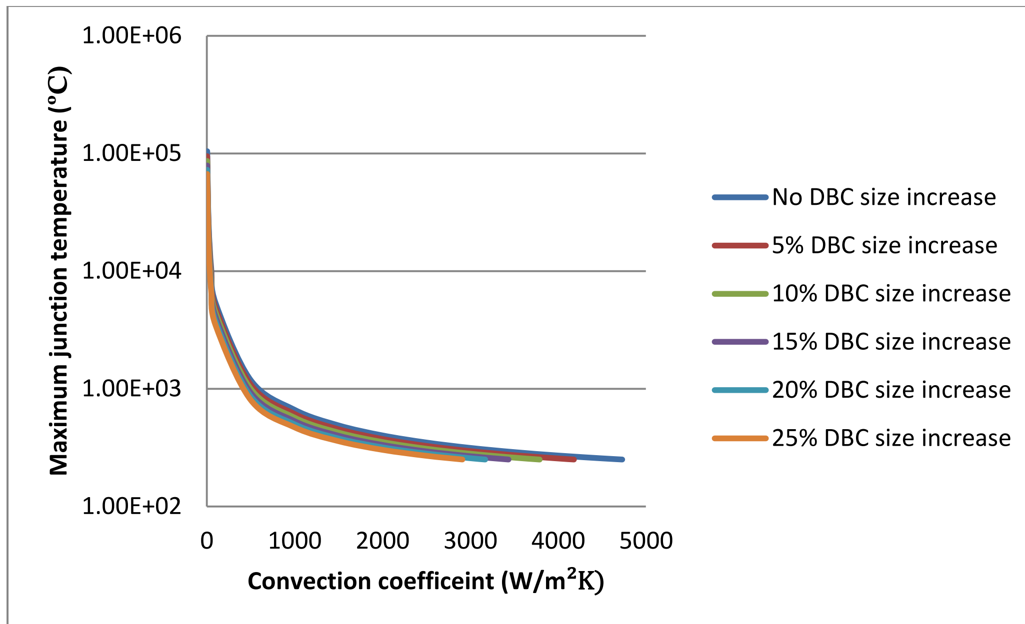


Figure 3.48. Convection coefficient versus maximum junction temperature for various DBC sizes Power dissipation 1.6KW (with BP condition)

- Parameters: Ta = 100ºC, Power dissipation = 1.6KW with heatsink

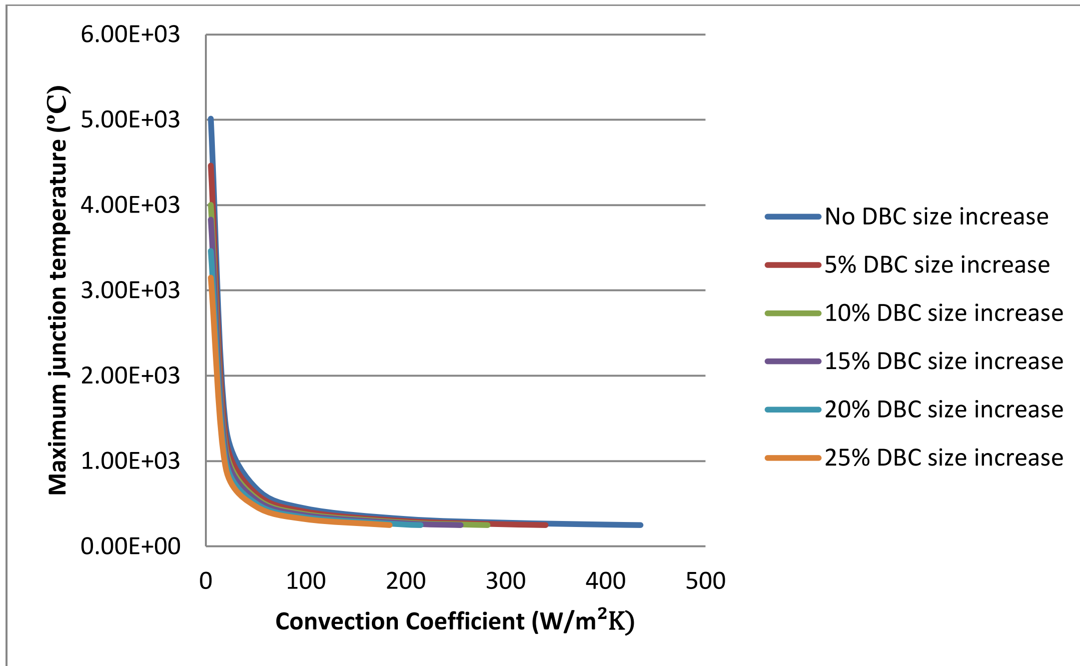


Figure 3.49. Convection coefficient versus maximum junction temperature for various DBC sizes Power dissipation 1.6KW (with HS condition)

- Parameters: Ta = 100ºC, Power dissipation = 2.5KW without baseplate and heatsink

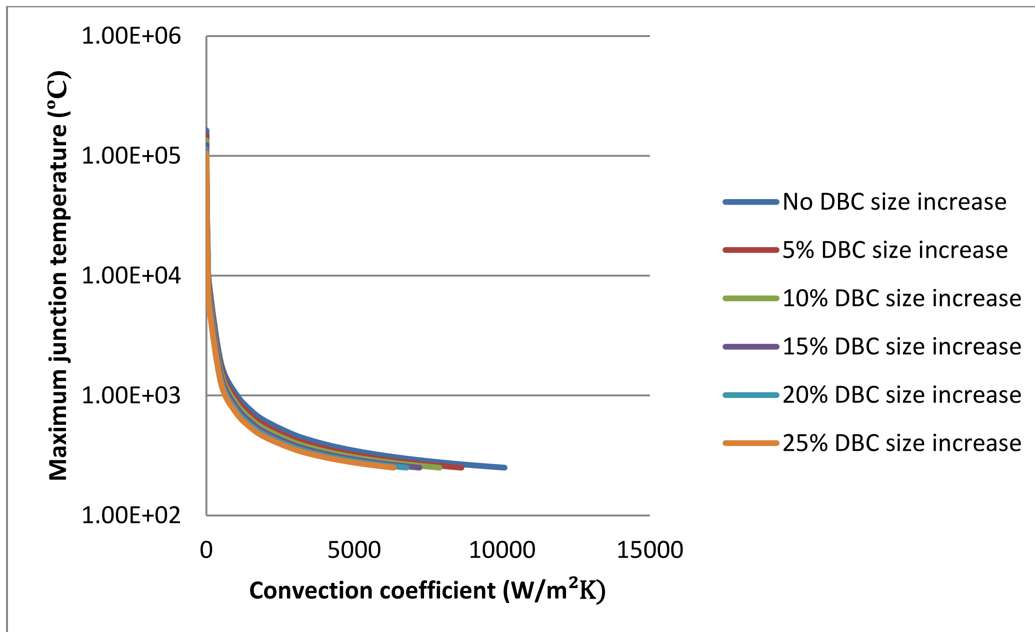


Figure 3.50. Convection coefficient versus maximum junction temperature for various DBC sizes Power dissipation 2.5KW (without BP or HS condition)

- Parameters: Ta =100ºC, Power dissipation = 2.5KW, with baseplate and without heatsink

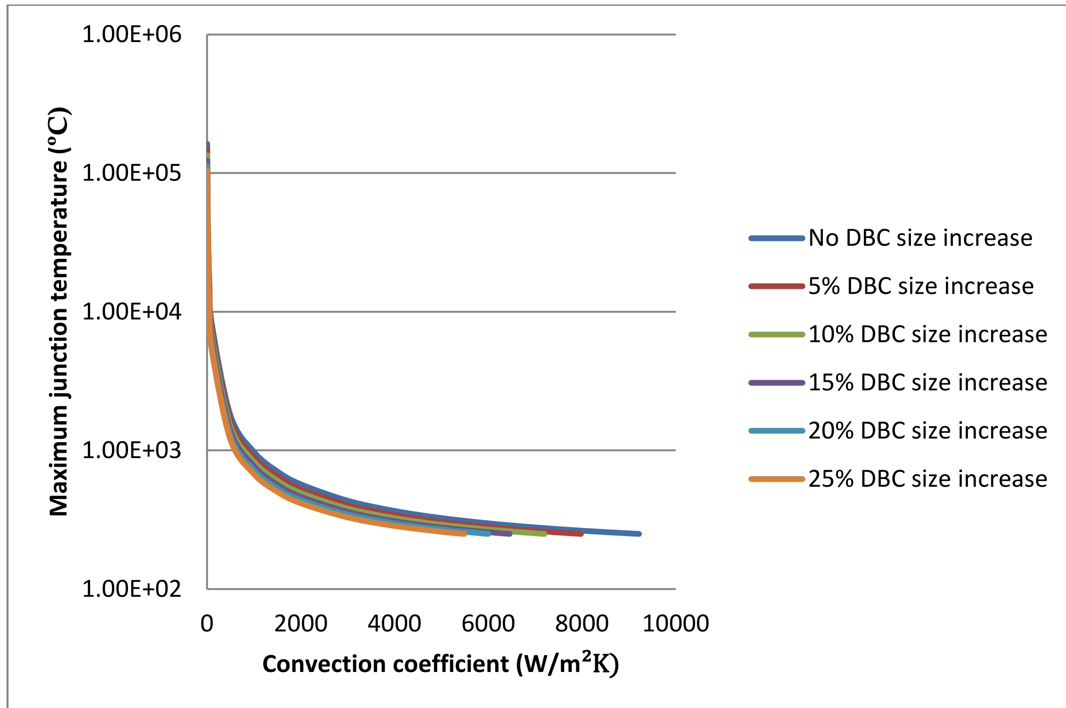


Figure 3.51. Convection coefficient versus maximum junction temperature for various DBC sizes Power dissipation 2.5KW (with BP condition)

- Parameters: Ta = 100ºC, Power dissipation = 2.5KW, with baseplate and heatsink

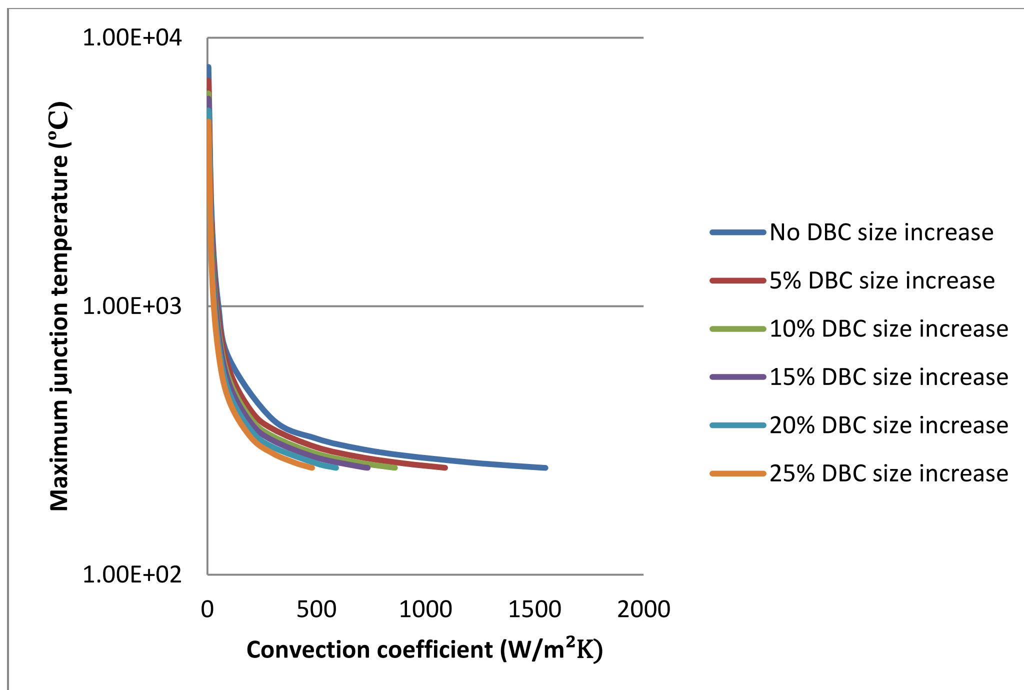


Figure 3.52. Convection coefficient versus maximum junction temperature for various DBC sizes Power dissipation 2.5KW (with HS condition)

- To get Tjmax = 250ºC, the convection coefficient versus substrate size increase for various parameters is given below.

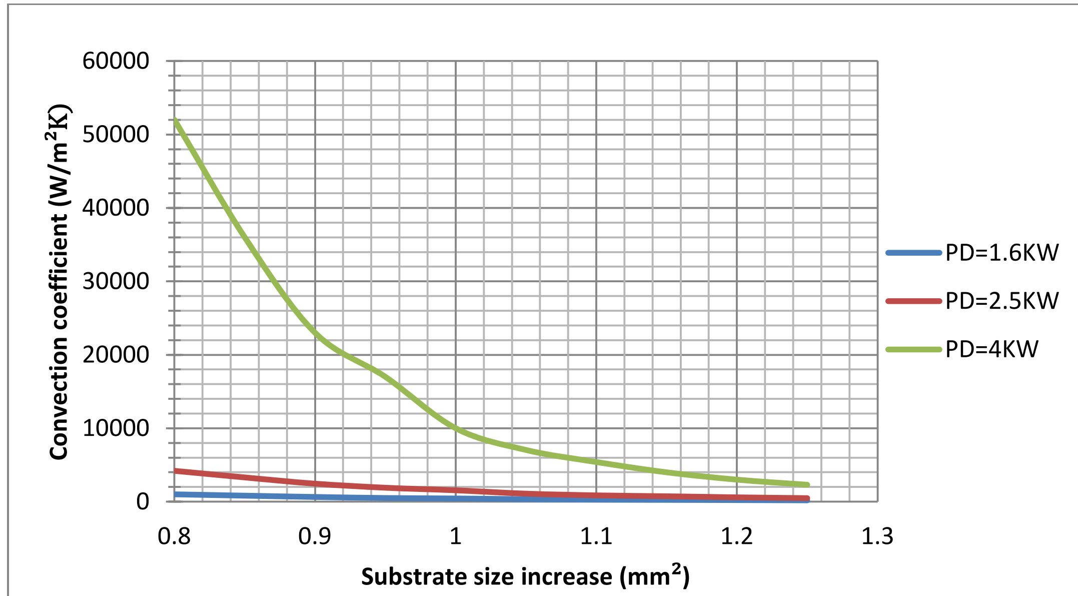


Figure 3.53(a). Convection coefficient versus substrate size increase (linear plot)

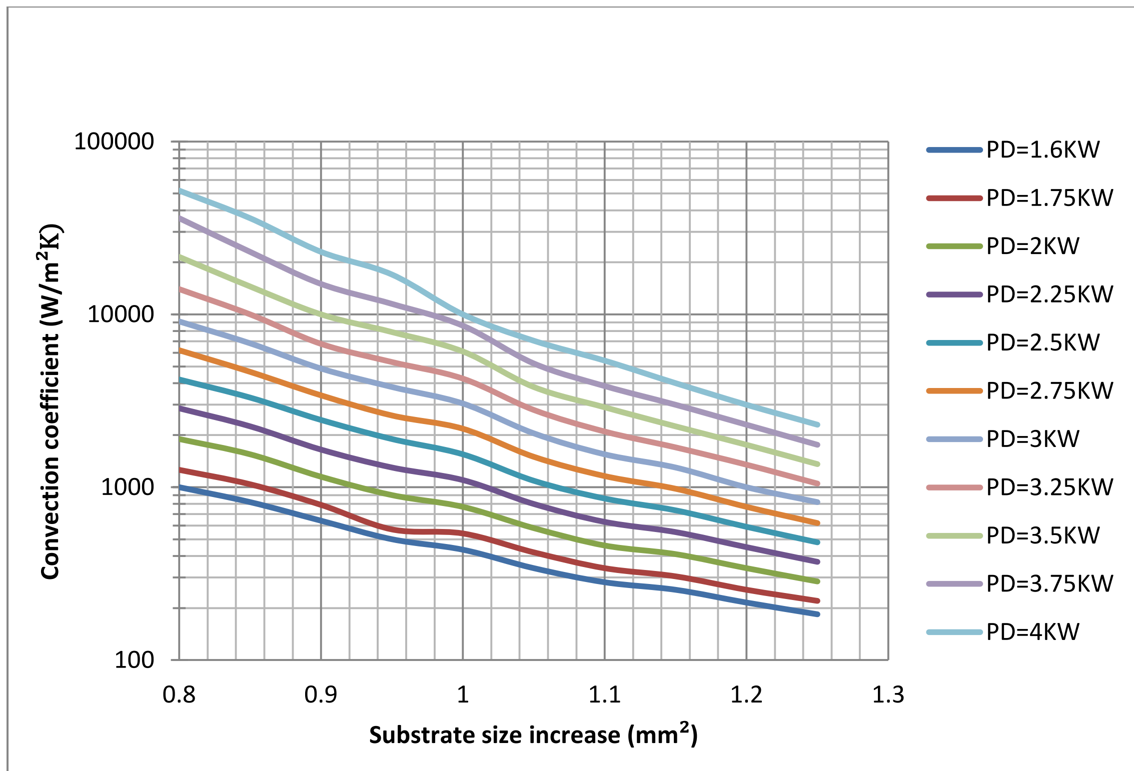


Figure 3.53(b). Convection coefficient versus substrate size increase (semi-log plot)

As can be seen in Figure 3.53, for a power dissipation of 4KW and an ambient temperature (Ta) of 100ºC, the change in convection coefficient is from 10000W/m²K to 2000W/m²K, whereas, for a power dissipation of 1.6KW and an ambient temperature (Ta) of 100ºC, the change in convection coefficient is only from around 435W/m²K to 185W/m²K. Thus, there is a significant change in convection coefficient when increasing the substrate size for higher power dissipation modules than those low power dissipation modules.

3.11 Discussions on results

For an efficient thermal management system, layout needs to be designed by selecting appropriate parameters for best performance. From the data provided in the previous section:

- Select appropriate material for fabricating a power module.
- Choose ambient temperature and maximum temperatures such that $\Delta T \geq 100$ºC for low cost cooling systems.
- For modules that dissipates high power, increase the heatsink size to achieve Tjmax for lower convection coefficient.
- If point three still fails to provide desired results, increase size of the substrate. Note that an increase in the substrate area affects the Tjmax significantly for high power dissipation cases than those low power dissipation cases.

3.11.1 Application examples

Example 1:

A 50KW power module is 95% efficient and is of size 60mm X 65mm. Suppose this module is placed in an ambient temperature of 75ºC; find the convection coefficient required to maintain a maximum junction temperature 250ºC for a heatsink attached condition.

Solutions:

Step 1: A 50KW power module is 95% efficient means it dissipates 2.5KW power (50000 – 50000 X 0.95 = 2500W).

Step 2: Thermal analysis in sections 3.5 to 3.9 were done on a prototype substrate with a size of 53mm X 58mm. As the substrate size in the question is 60mm X 65mm, we cannot directly use those graphs (graphs from sections 3.5 to 3.9) to obtain convection coefficient for the above question. So, first consider the size change variations before using those graphs. Increasing the prototype substrate (53mm X 58mm) to about 10%, substrate size becomes 59mm X 64mm ≈ 60mm X 65mm.

Step 3: From Figure 3.53(b), find y-axis (convection coefficient) with respect to 1.1 on x-axis (substrate size increase 1.1) for 2.5KW power dissipation. Convection coefficient noted as shown in Figure 3.54 is 860W/m²K. That is, for substrate size increase by 10% (x-axis=1.1), convection coefficient required to maintain Tjmax=250ºC for power dissipation=2.5KW and Ta=100ºC is found to be 860W/m²K as shown in Figure 3.55 below (it is same as Figure 3.53(b)).

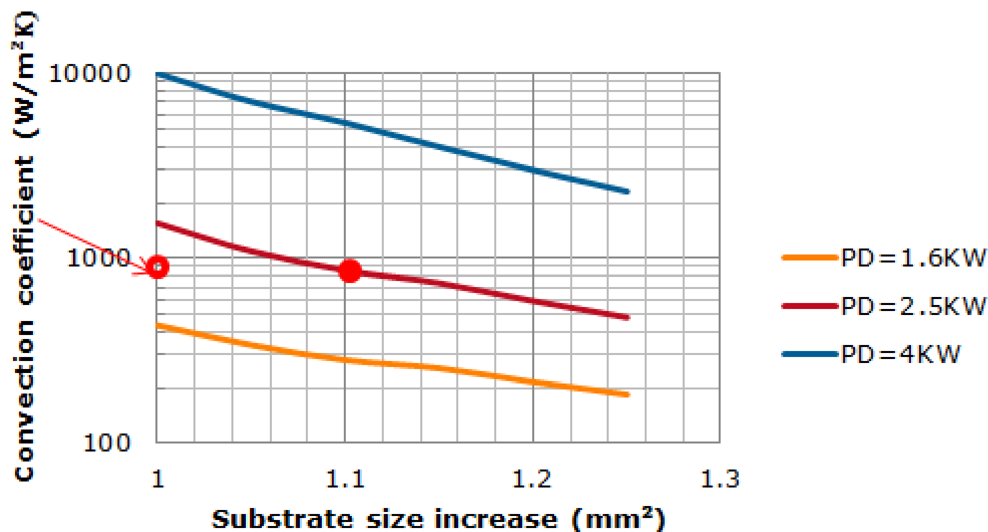


Figure 3.54. Find y-axis (convection coefficient in W/m^{2}K) with respect to 1.1 on x-axis (substrate size increase 1.1); for 2.5KW power dissipation.

Step 4: However, requirement in question is for Ta=75ºC, not Ta=100ºC. Figure 3.28 can be plotted in semi-log (for x-axis) and is shown in Figures 3.55(a) and 3.55(b).

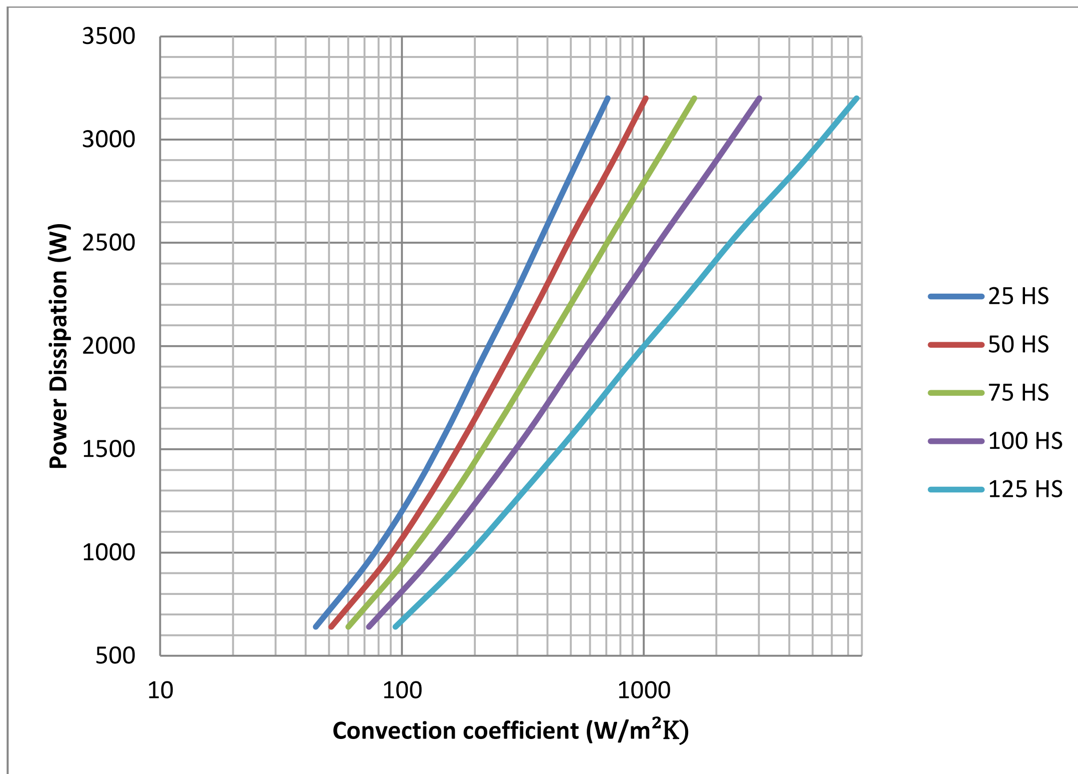


Figure 3.55(a). Semi-log plot of Figure 3.28 for better reading values.

Step 5: Locate 860W/m²K convection coefficients on the Ta=100ºC line (ignore y-axis values since equivalent convection coefficient is needed to be found); point 1 in Figure 3.55(b). Move horizontally left till Ta=75ºC line is met; point 2 in Figure 3.55(b). Read the corresponding convection coefficient; point 3 in Figure 3.55(b). This is found to be a little less than 590W/m²K.

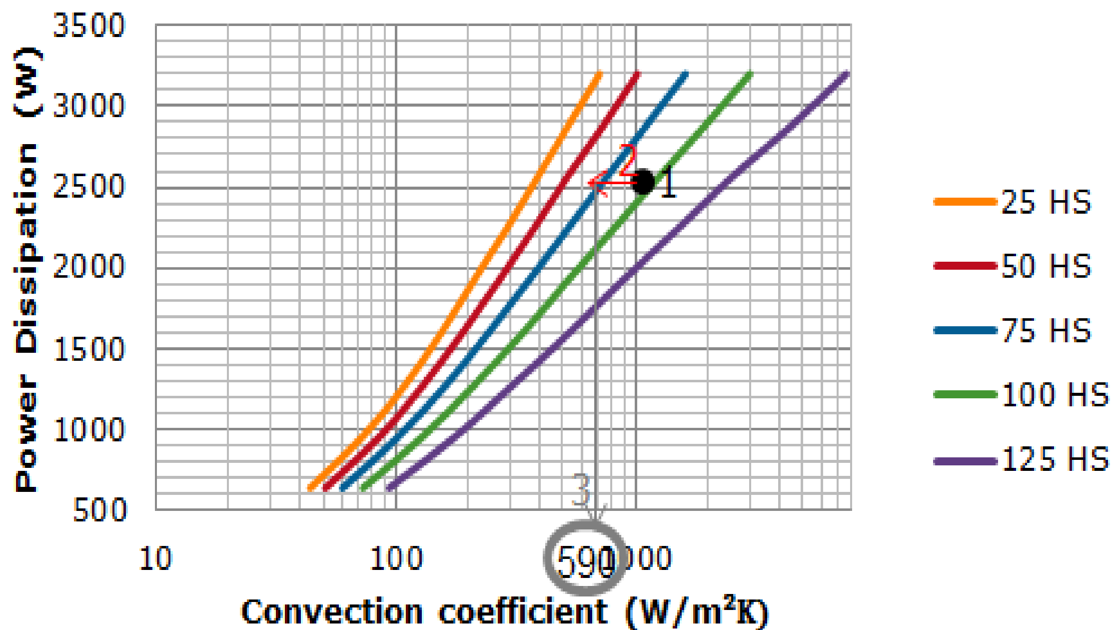


Figure 3.55(b). Obtaining convection coefficient for Ta=75ºC

This is the convection coefficient required to maintain a Tjmax of 250ºC for Ta of 75ºC for a 60mm X 65mm power module which dissipates 2.5KW power.

To verify this; for a module with size mentioned above, the same parameters were given and simulated in SolidWorks. This gave Tjmax=247ºC ≈ 250ºC.

Example 2:

A 50KW power module that is 95% efficient, is placed in an ambient temperature of 75ºC, and expected to have a maximum junction temperature of 250ºC.Choose an optimum substrate size for a corresponding convection coefficient.

Solutions:

Step 1: 50KW is 95% efficient => module dissipates 2.5KW power.

Step 2: On a 2.5KW power dissipation line, locate for ambient temperature 75ºC (shown in point 1). This is the desired parameter.

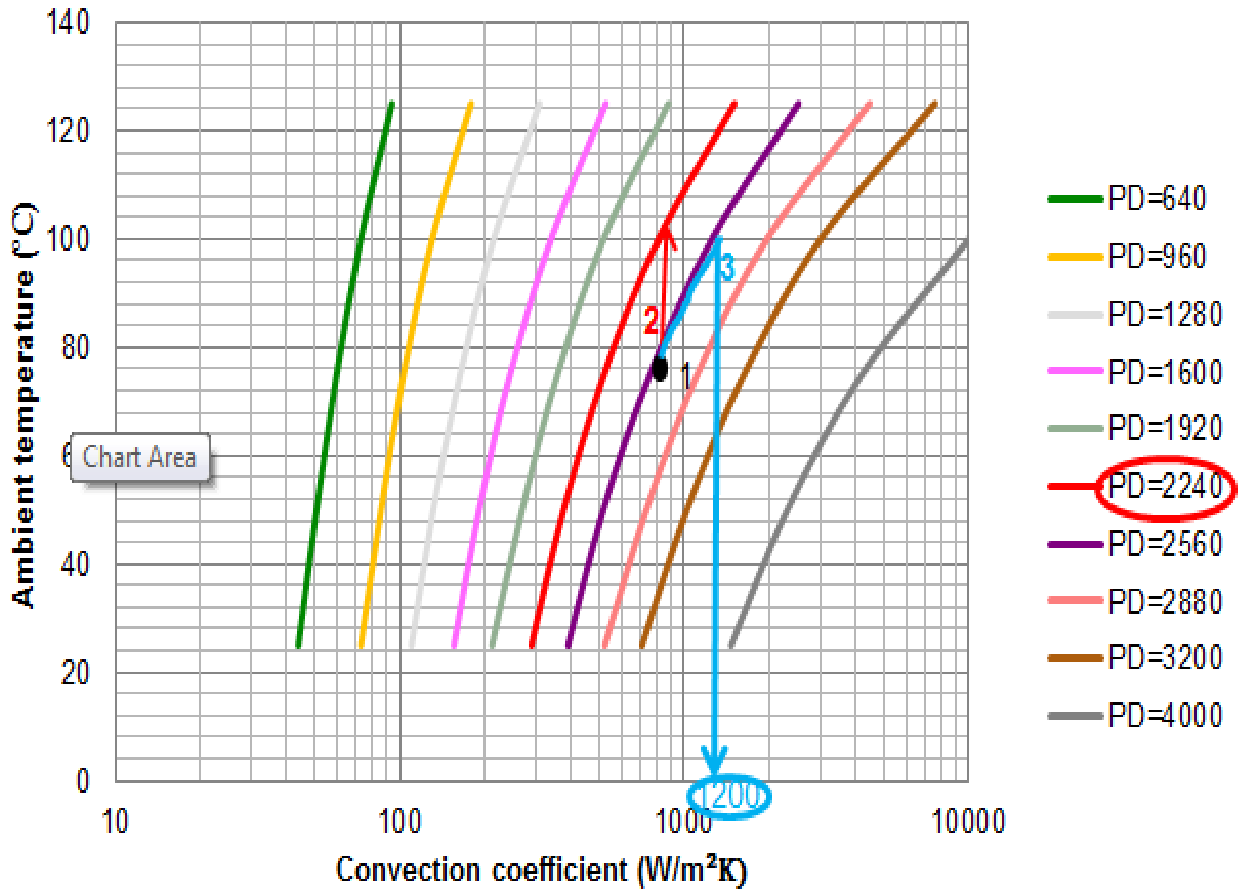


Figure 3.56(a). Ambient temperature versus convection coefficient for different power dissipations

Step 3: Travel vertically upwards till Ta of 100ºC is met (shown in point 2). This is done since the plot to find the size of substrate was plotted for 100ºC. So, it is necessary to find equivalent power dissipation for 100ºC Ta which is same as 2.5KW power dissipation and 75ºC Ta. The power dissipation met is the equivalent power dissipation (T_{PD}). This is found to be T_{PD} = 2.24KW.

Step 4: From the same point 1, move along the 2.56KW power dissipation line until it intersects 100ºC ambient temperature (shown as point 3). The convection coefficient obtained is the equivalent convection coefficient (T_{CC}). This is found to be T_{CC} = 1200W/m^{2}K.

Step 5: Use equivalent power dissipation and equivalent convection coefficient to find the optimum size for the substrate.

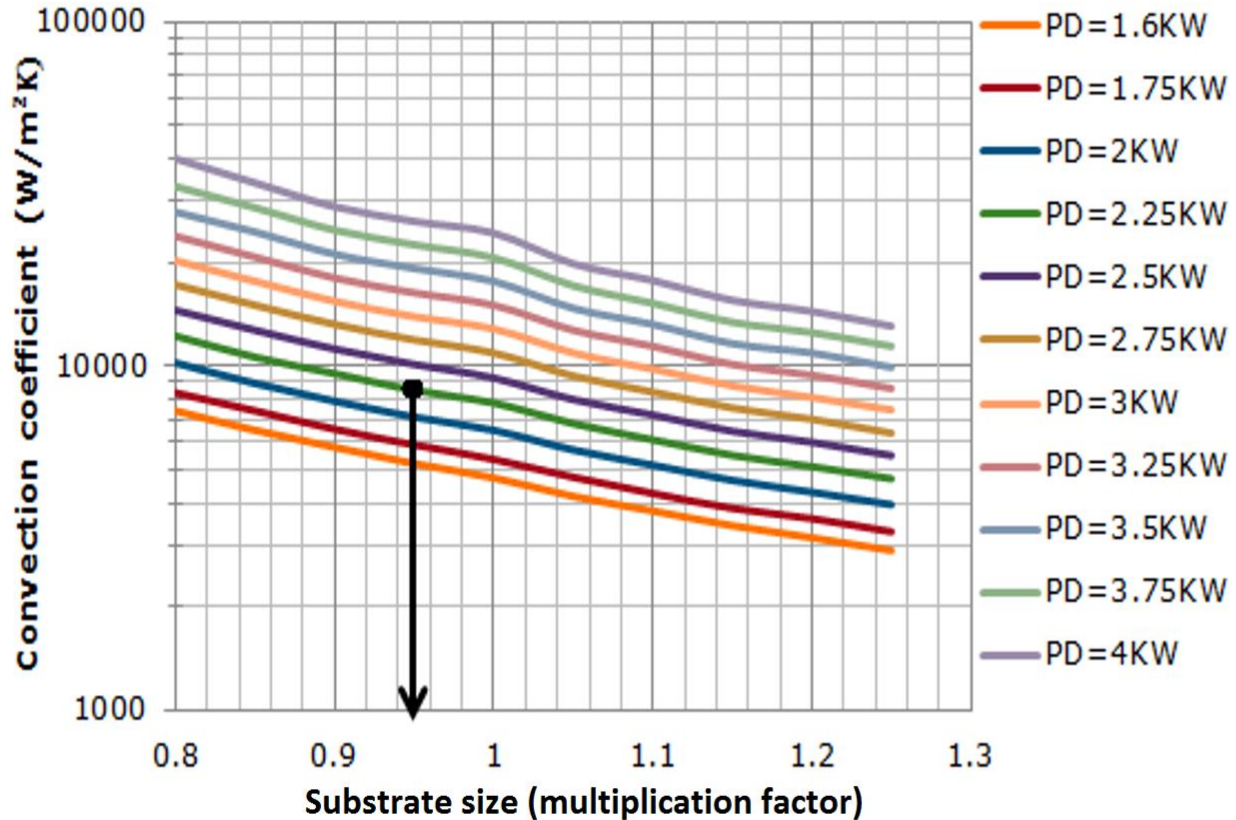


Figure 3.56(b). Convection coefficient versus substrate size plot to find the optimum size

For convection coefficient (y-axis) 1200W/m^{2}K and power dissipation line 2.25KW, find the corresponding substrate size (x-axis). This is found to be 0.95 of the original size. Original size is 53mm X 58mm, 0.95 of this size is 50.35mm X 55.1mm.

Hence, the optimum substrate size for a power module with power dissipation 2.5KW, a Ta of 75ºC, and a Tjmax of 250ºC is approximately 50mm X 55mm.

3.12 Summary

Thermal analysis on a power module for different parameters is performed and their effects on each other are studied. These parameters were varied to study the behavior for different ranges.

Examples were provided in previous section to show how this study can be employed to select parameters for a module.

- Power module behavior becomes predictable for known parameters.
- Thermal analysis performed on a generalized module under different conditions provides a database; from which designers can select parameters for their layouts. Since many designers currently design their layouts manually, trial and error methods are used to fix the parameters. This is a very tedious and time consuming process. From graphs provided above, some parameters can simply be looked up. Of course this data comes with some percentage error depending on the layout design.
- Even when a software is used to design a layout (PowerSynt), some parameters (like substrate size, equivalent convection coefficient of heat-sink and cooling given to the heat-sink etc.) needs to be chosen. Instead of simply guessing these values, a parameter value can be extracted for the layout designing software.

3.12.1 Significance of the results

- As explained in section 3.7, for every case of power dissipation, the consistent results were obtained for ΔT greater than 125 ºC. Hence, for optimum functioning, ΔT (Maximum junction temperature – Ambient temperature) must be greater than 125ºC for power modules that dissipates medium and high power.
- For a low ΔT and high power dissipation conditions, baseplate acts more like a thermal resistance than a heat-spreader. Hence, it is ineffective to employ base-plates for these cases.
- Increasing substrate size to bring down maximum junction temperature is more effective in higher power dissipation cases than in medium or low power dissipation cases.

3.12.2 Limitations

- Results from this chapter can be used to obtain the initial values for parameters. Actual behavior of the module may vary slightly.
- This chapter provides database only for a certain range of parameters like: power dissipation range from 640W to 4KW, ambient temperature range from 25ºC to 125ºC, maximum junction temperatures of 200ºC and 250ºC, substrate size from 1967mm^2 to 4803mm^2.
- These results best apply for power electronic modules with symmetric design, or results may not be so accurate for asymmetric layout designs.
- Power semiconductor dies, and hence, power dissipaters need to be evenly distributed throughout the layout.

CHAPTER 4. PARASITIC EXTRACTION OF A POWER MODULE

4.1 Introduction

In any electronic components, the presence of undesirable impedances effects their performance and efficiency. These undesirable impedances are usually parasitic inductances (emphasized in this chapter), or parasitic capacitances. Parasitics are insignificant in low power and low frequency conditions. However, in high power and high frequency conditions, they significantly affect performance of the power electronic module by affecting their power dissipation, accuracy, efficiency, delay, uniformity in current distribution, reliability etc.

Before fabricating power modules, predicting these parasitic circuit elements becomes very important as they affect the behavior of the power electronic modules. Ansys Q3D software which uses integral equations and finite element (FEM) matrices to calculate parasitics is used for verification purpose in this chapter.

Knowledge on parasitic circuit elements in power electronic modules before actual fabrication helps in developing better design to improve their performance. This increases product quality and decreases cost. It is also necessary to measure these parasitic circuit elements in a fabricated module before mass production for design verification.

Extraction of parasitics in a fabricated power module can be performed using a time domain reflectometry method (TDR) [12]. This chapter developes the TDR method in parasitic characterization of power electronic modules. The TDR concept is shown in Figure 4.1.

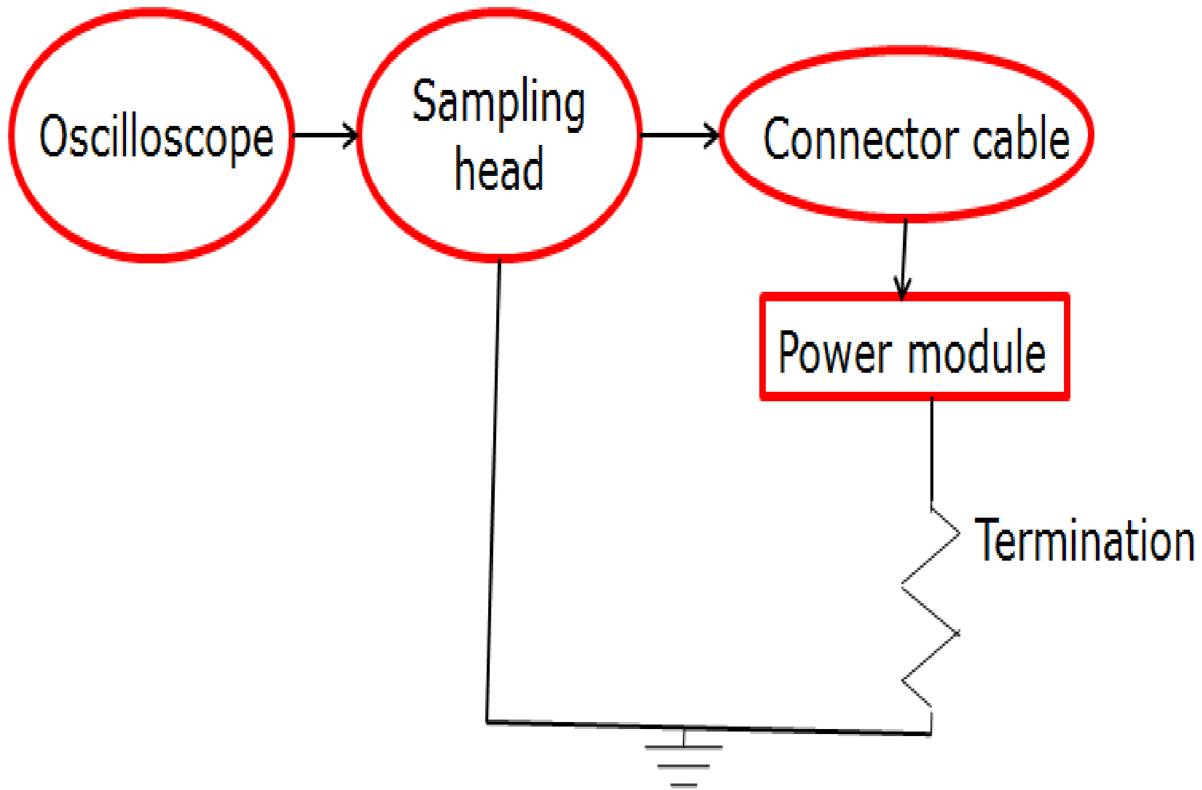


Figure 4.1. Basic block diagram representation of TDR method

TDR measurement technique propagates a high frequency step signal, also referred as incident signal, through the region of interest (ROI) in the device under test (DUT). This region of interest in power electronic module can be a simple copper trace or a high density connector. The incident signal reflects back at a termination and the reflected signal is captured by the sampling head. Apart from this, there is also a shorted waveform which is the incident signal reflected back without being passed through the ROI. These captured incident, reflected, shorted waveforms are evaluated and the corresponding resultant impedance and parasitic inductance waveforms are calculated [11]. From the inductance waveforms obtained, the limits are identified and the respective parasitic values are calculated. Figure 4.2 shows an example of TDR waveforms.

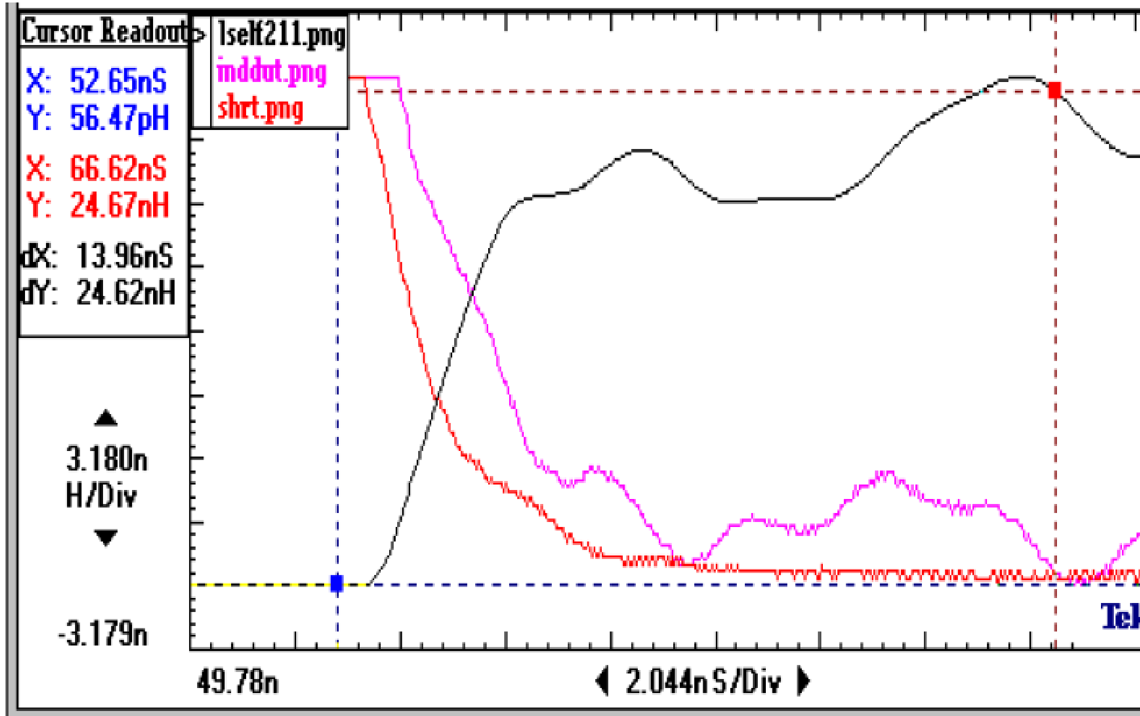


Figure 4.2. TDR Waveforms for an example test vehicle in parasitic inductance measurement

Since parasitic inductance waveforms are calculated from the incident signal and its corresponding reflected signal, TDR method can be referred to as an echo measurement technique. Parasitic values obtained from simulations (on a virtual power module designed in Ansys Q3D software) and, parasitic values extracted from the fabricated power module (using TDR method) are compared to verify the TDR parasitic measurement technique.

4.2 Test vehicle description

4.2.1 Test vehicle A

Predefined 25Ω, 50Ω and 75Ω micro-strips are used as test vehicles for initial verification to test their impedances using the TDR measurement technique.

4.2.2 Test vehicle B

The test vehicle designed using the Q3D software is as shown in Figure 4.3.

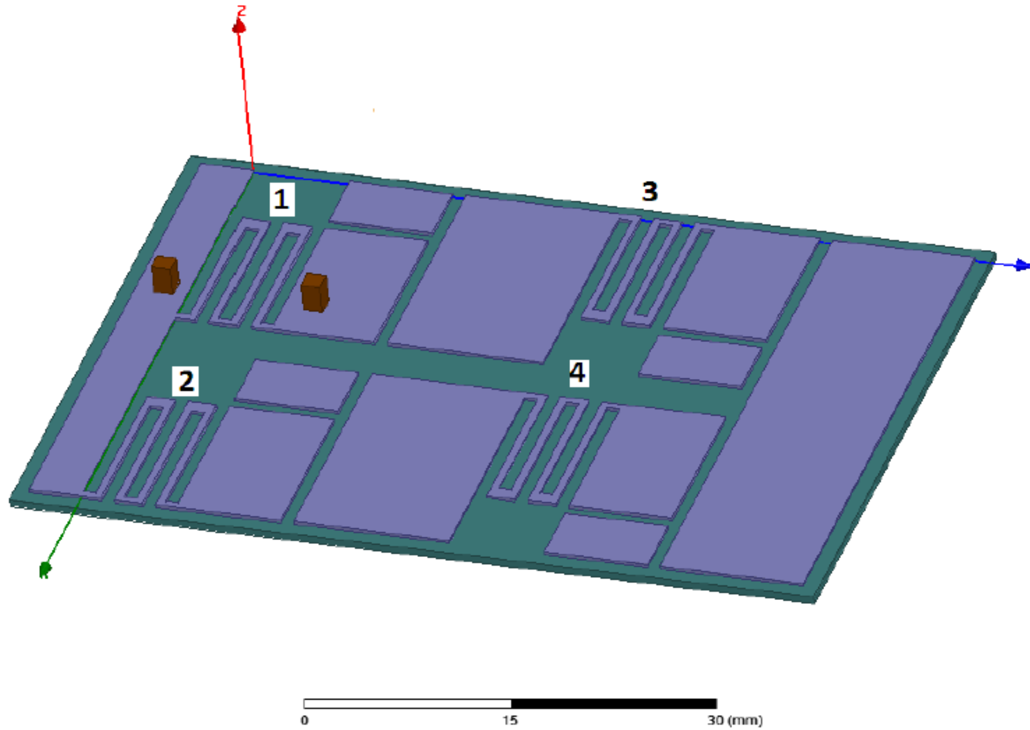


Figure 4.3. Test vehicle B, designed to measure parasitic

The size of this test vehicle is 45.02 mm × 62.36 mm × 0.65 mm. As shown in Figure 4.3, the test vehicle has four serpentine traces (as shown in figure), each for which their parasitics are obtained by:

- Simulate using Q3D software
- Measure using the time domain reflectometry technique.

Results obtained from both the above mentioned methods are compared. Trace dimensions are shown in Figure 4.4. Since power electronic modules are usually operated below 500 KHz, so the parasitics are also simulated at the same frequency.

The substrate (direct bonded copper or DBC) goes through the entire process involving Ni plating of DBC, dry film, etching, and photoresist strip. The whole test vehicle was fabricated as meticulously as possible, since this test vehicle is used to compare the physical characteristics with that of the simulated module.

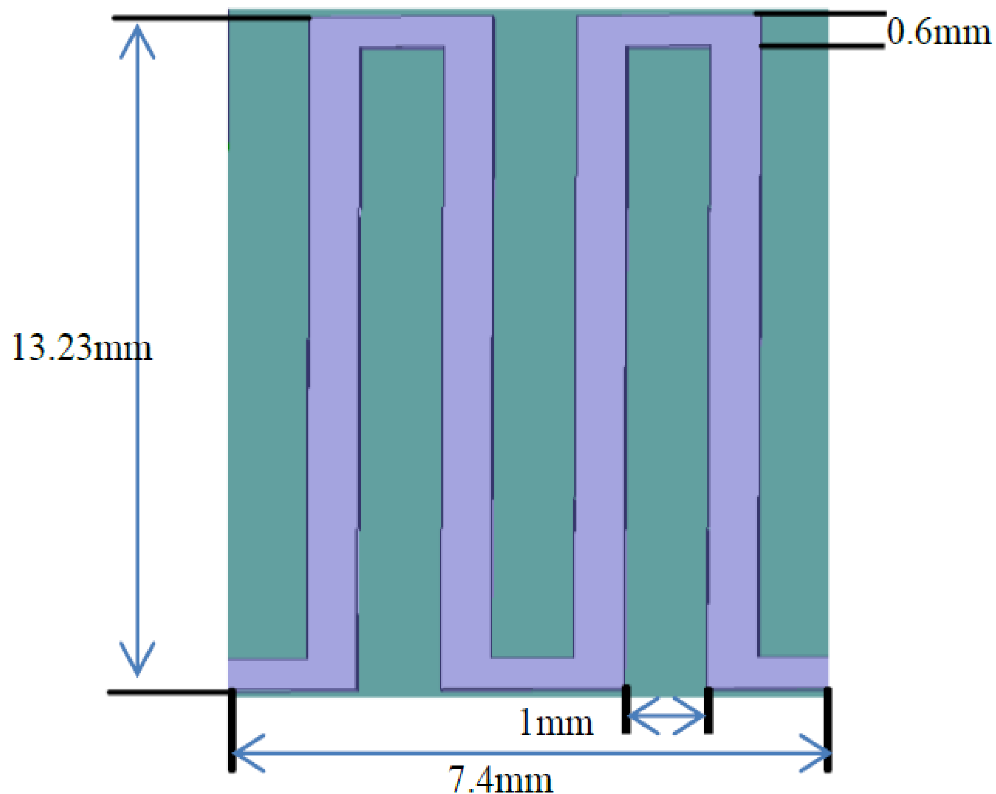


Figure 4.4. Trace dimensions.

4.3 Experimental setup for Time domain reflectometry

Experimental setup for TDR method is shown in Figures 4.5(a) and 4.5(b). Oscilloscope is set to produce a step signal of 250mV amplitude with a rise time of 35ps. The rise time decides the minimum distance between two points for which parasitics can be measured. The higher is the rise time, the better would be the resolution. For a 35ps of rise time, 8mm resolution can be achieved.

A 50Ω SMA male connector is used to connect the sampling head to obtain the incident signal from oscilloscope. This in turn is connected to a 50Ω co-axial cable to match its output impedance and this whole arrangement is connected to the region of interest in DUT as shown in the Figures 4.5(a) and 4.5(b).

Figure 4.5(a). Experimental setup for TDR

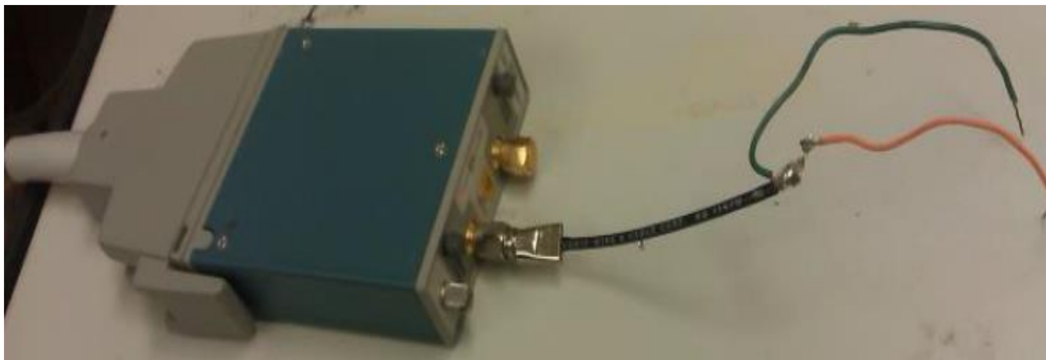


Figure 4.5(b): Focused on the sampling-head.

Initial impedance mismatch between the sampling head and co-axial cable is calibrated so that it does not affect the parasitic measurement. This calibration eliminates contact parasitics, and hence, improves the accuracy of measurements.

4.4 Initial verification for impedance measurements using TDR method

Impedance is measured on predefined micro-strips using TDR method to verify the experimental set-up. If the measured impedance matches the impedance of the micro-strips, then the setup is verified.

Incident step signal (shown in Figure 4.6) and reflected signal from DUT (micro-strips) are captured by the oscilloscope and transferred to a computer to be analyzed using the IPA 310 software. This software computes the impedance waveforms from which the impedance values are calculated using *impedance processing (Z processing)*. Impedance waveforms for the micro-strips of 50Ω, 25Ω, and 75Ω are shown in Figures 4.7, 4.8, and 4.9, respectively.

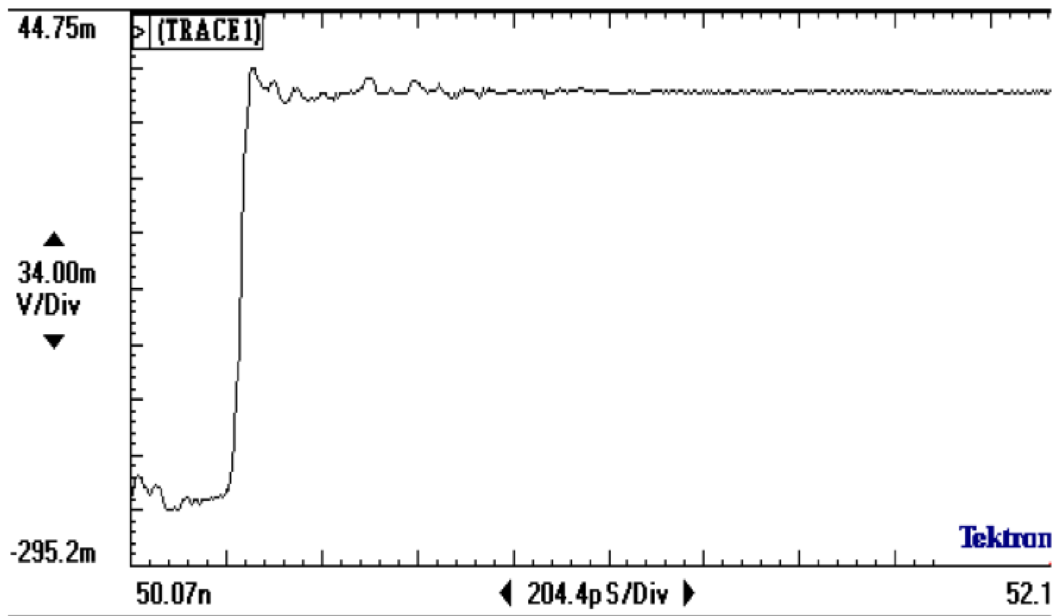


Figure 4.6. Incident step signal or waveform incident on micro-strips.

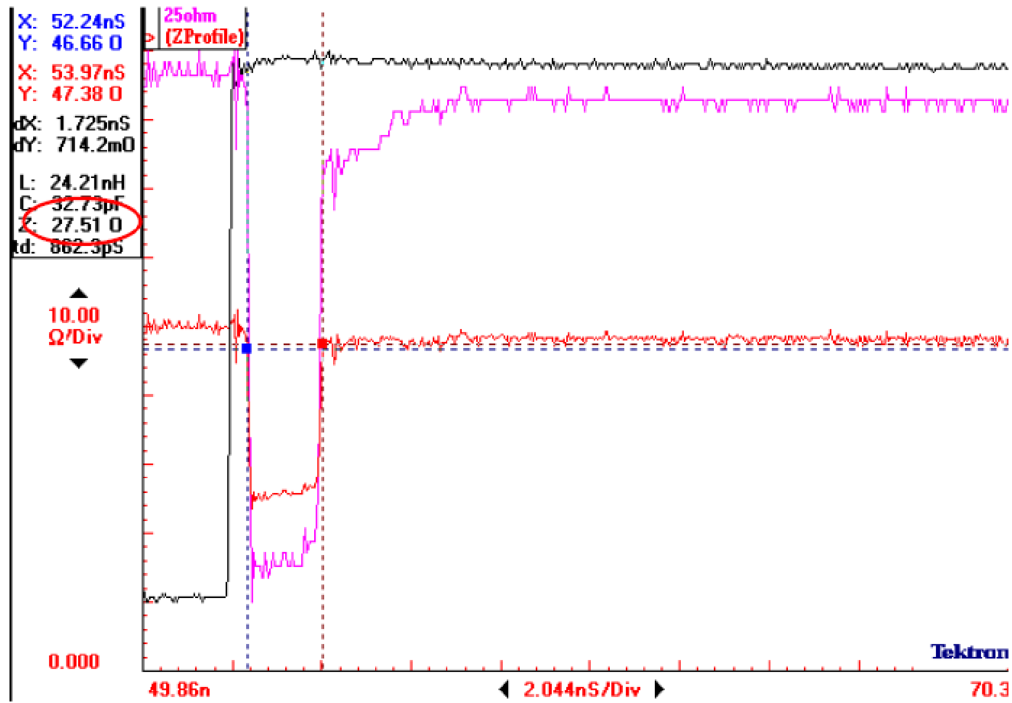


Figure 4.7. Impedance waveform for 25 ohms

Figure 4.8. Impedance waveform for 50 ohms

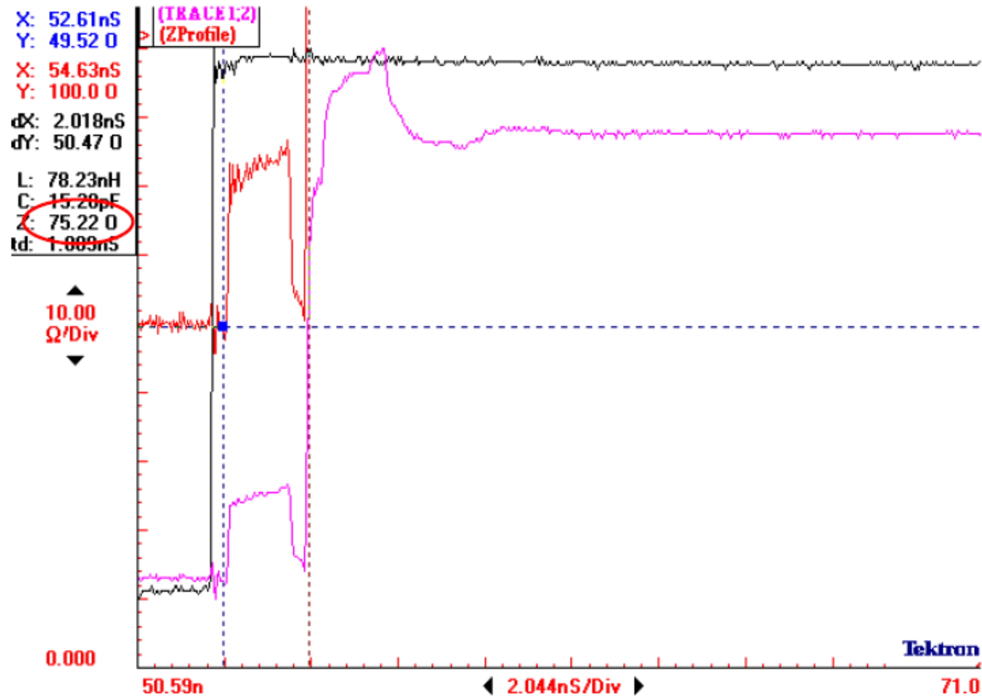


Figure 4.9. Impedance waveform for 75 ohms

From the above Figures 4.7, 4.8, and 4.9 obtained using the TDR method and IPA 310 software, the impedance values are 27.51, 49.55 and 75.22 ohms (left hand side of the figures circled in red), which are very close to the rated 25, 50, and 75 ohms, respectively.

This principle can be used to measure parasitic impedance on electronic packages which is not discussed in this thesis. The main focus is on the parasitic inductances rather than parasitic impedances.

4.5 Results and discussions

Simulations are performed on a virtual power module using the ANSYS Q3D software, where the AC analysis results yield an absolute value. The extracted parasitic values using simulations for four serpentine traces 1, 2, 3, and 4 as shown in Figure 4.3 are 20.345×10^{-9}H, 20.87×10^{-9}H, 22.008×10^{-9}H, and 21.646×10^{-9}H, respectively.

For physical parasitic extraction employing TDR method, the step signal (Figure 4.6) is passed through each of these traces individually, and the reflected waveforms are captured. The reflected waveforms and the shorted waveforms are transferred to a computer with IPA310 software. This software computes the parasitic inductance using the *self-inductance processing*.

For the four traces, TDR method yields waveforms shown in Figures 4.10, 4.11, 4.12 and 4.13.

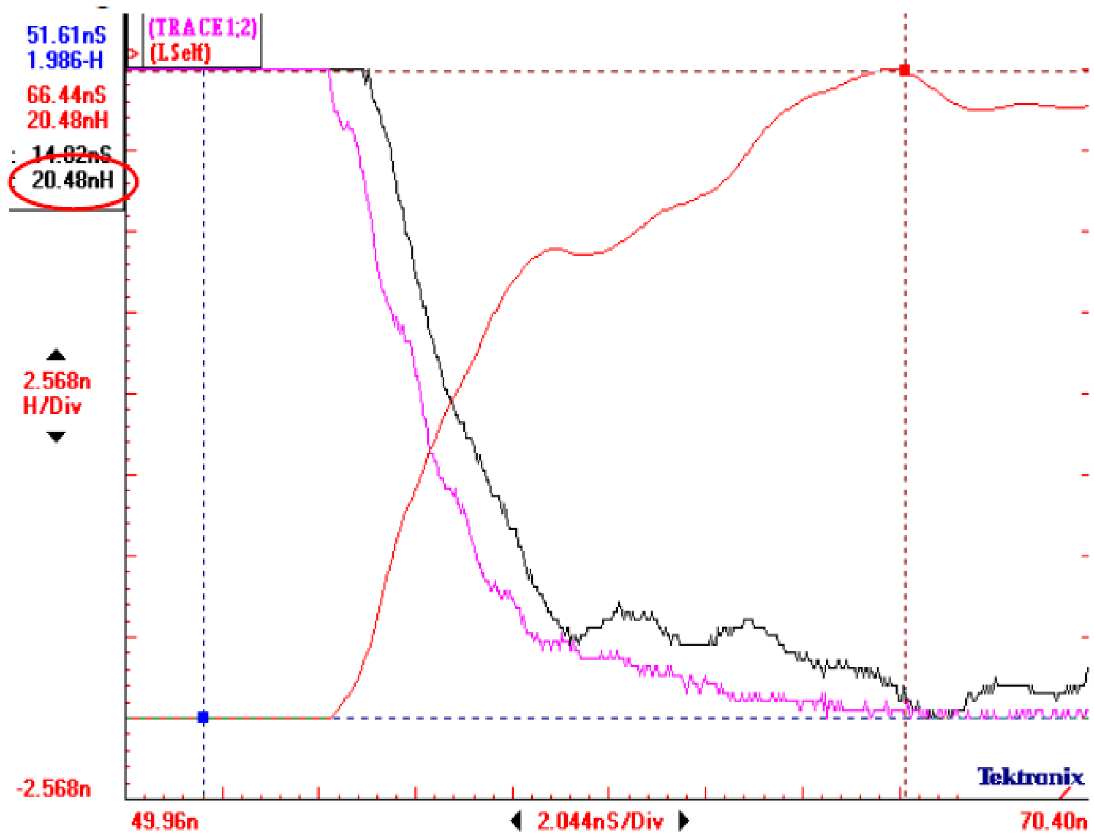


Figure 4.10. Reflected (black), shorted (pink) and inductance waveforms (red) for trace 1.

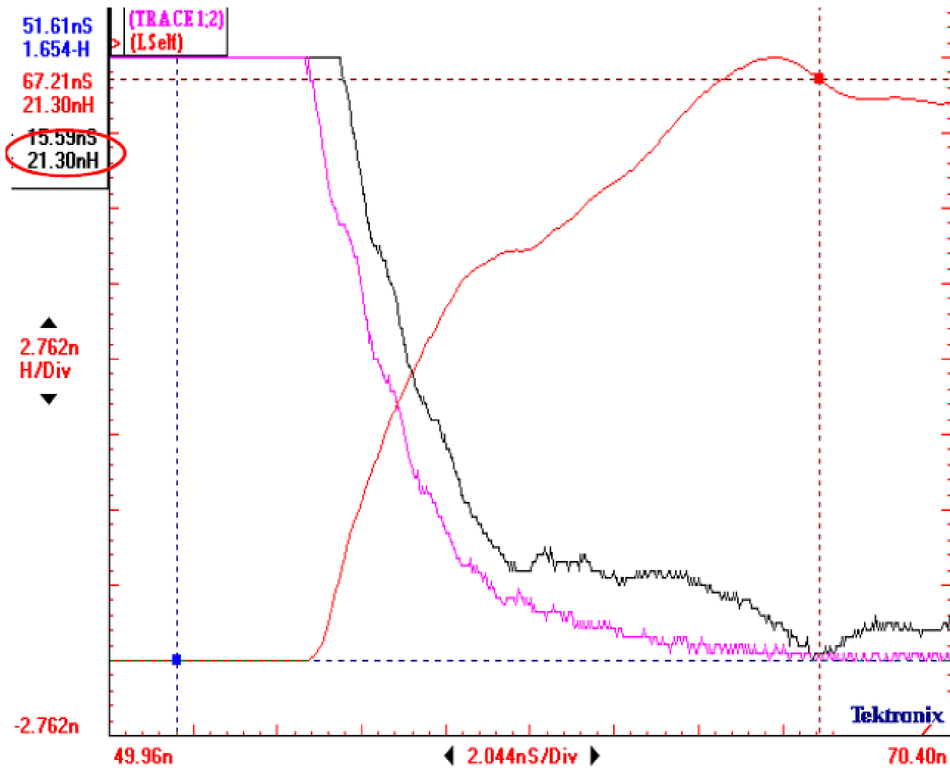


Figure 4.11. Reflected (black), shorted (pink) and inductance waveforms (red) for trace 2.

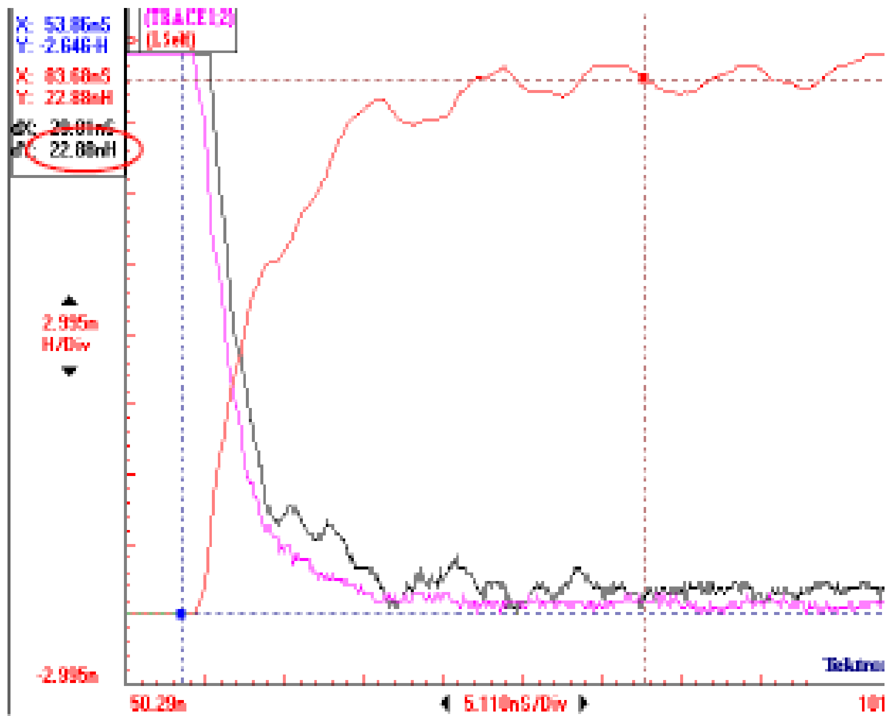


Figure 4.12. Reflected (black), shorted (pink) and inductance waveforms (red) for trace 3.

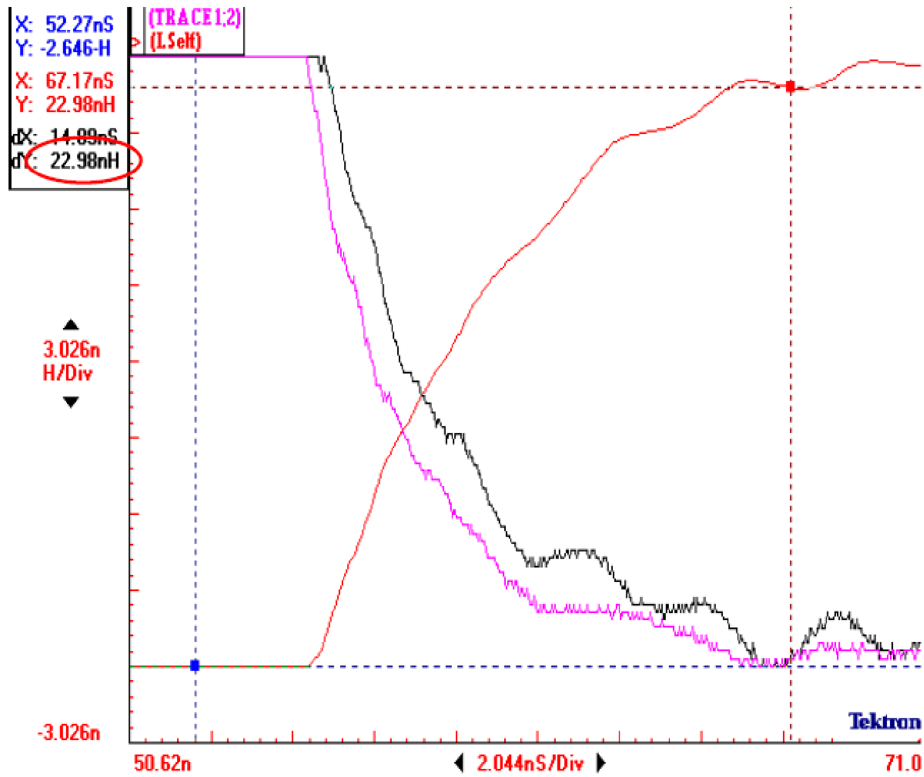


Figure 4.13. Reflected (black), shorted (pink) and inductance waveforms (red) for trace 4.

The parasitic inductance waveforms and the corresponding parasitic inductance values calculated are displayed, which can be seen in Figures 4.10, 4.11, 4.12 and 4.13. Red color waveforms indicate the parasitic inductance waveforms, and the parasitic inductance values are circled in red color (dY). The results obtained using TDR method and simulations are shown in Table 4.1.

Trace	Simulated results (nH)	TDR method results (nH)
1	20.345	20.48
2	20.870	21.30
3	22.000	22.88
4	20.784	22.98

Table 4.1. Comparison of parasitics obtained using simulations and TDR method

From Table 4.1, TDR method yields 90-99% accurate results. That is within a ±3nH difference.

4.6 Summary

From Table 4.1, the TDR measured and Q3D simulated parasitic inductances are almost similar. Hence, it can be concluded that as long as the module is fabricated accurately as the design, the parasitics extracted using the two methods are almost the same. Hence, TDR parasitic measurement technique proves to be useful for parasitic characterization of power electronic modules. Better oscilloscopes and updated software are available which provides more accurate values.

4.6.1 Applications

- Module verification: Post-fabrication electrical characterization or verification of certain properties is necessary to check proper functioning of power electronic modules. This is performed to check if the designed module (using 3D software technology) is similar to the final module before releasing for mass production.

  Since increase in parasitic values considerably increases power dissipated by a power electronic module, and become more significant for high power and high frequency operations, it is necessary to minimize the parasitics. Other than the power testing (maximum voltage and maximum current tolerable by power module), parasitics predicted (using software) at some critical regions can be extracted physically (using TDR) and compared to the predicted values for verification.

- Non-destructive failure analysis: In case of undesirable behavior of power electronic modules, parasitic measurement proves to be a diagnosis tool. For this analysis, the modules can be divided into several regions. Simulate parasitic values for each of these regions using software on a virtual model. Simulated parasitic values are taken as

reference and considered as *ideal* parasitic values. Then parasitics at the same region of interest on the actual fabricated module are measured using the TDR method. These are *actual* parasitic values. Comparing the actual parasitics with the simulated/ideal parasitics, it is possible to narrow down the defected/malfunctioning region.

This kind of analysis does not include any sort of cutting or stripping of the module, parasitic characterization can be done without destructing the module. Hence, it can be used as a non-destructive tool for failure analysis.

4.6.2 Limitations

- Resolution or the minimum distance between two points of measurement using the TDR measurement is fixed for a particular rise time. To achieve a better resolution or to measure parasitic for closer points, the incident signal must have a fast rise time.
- For solid traces, the TDR parasitic results are very accurate however, for wire bonded module and very large traces, its accuracy may vary from 70 to 95 percent.

CHAPTER 5. INVESTIGATION OF WIREBOND RELIABILITY

5.1 Introduction

In this chapter, daisy design modules were fabricated using a standard fabrication procedure. These modules underwent thermal cycling tests to assess the integrity of their wirebond/encapsulation. The following effects and parameters were investigated:

- Effect of flux residues from solder paste on an un-encapsulated power module.
- Effect of flux residues from solder paste on an encapsulated power module.
- Bond wires with diameter 5 mils and 12 mils with encapsulation.
- Bond wires with diameter 5 mils and 12 mils without encapsulation.

Module layouts based on daisy chain design are shown in Figure 5.1 and Figure 5.2.

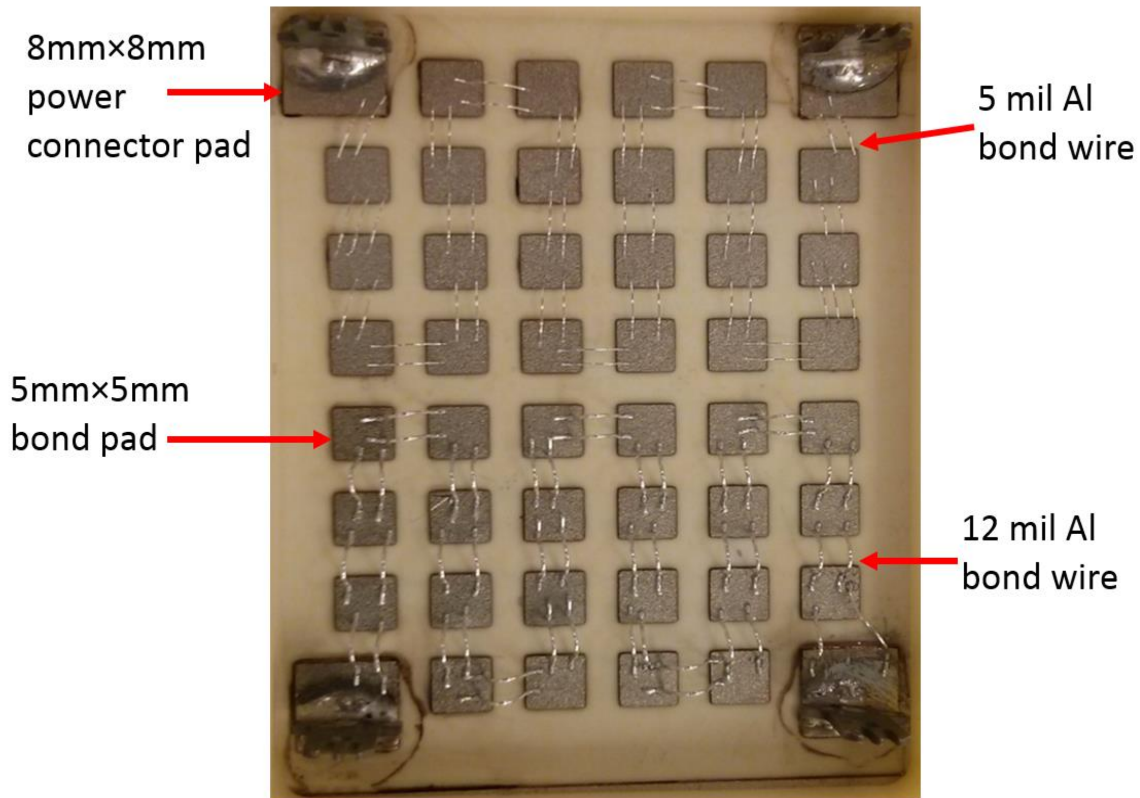


Figure 5.1. Test module with a daisy chain design with power connectors

As shown, each rectangular bonding pad is 5mm × 5mm. The corner rectangular pads are 8mm × 8mm. These pads are for the power connectors. The spacing between each pad is 4mm.

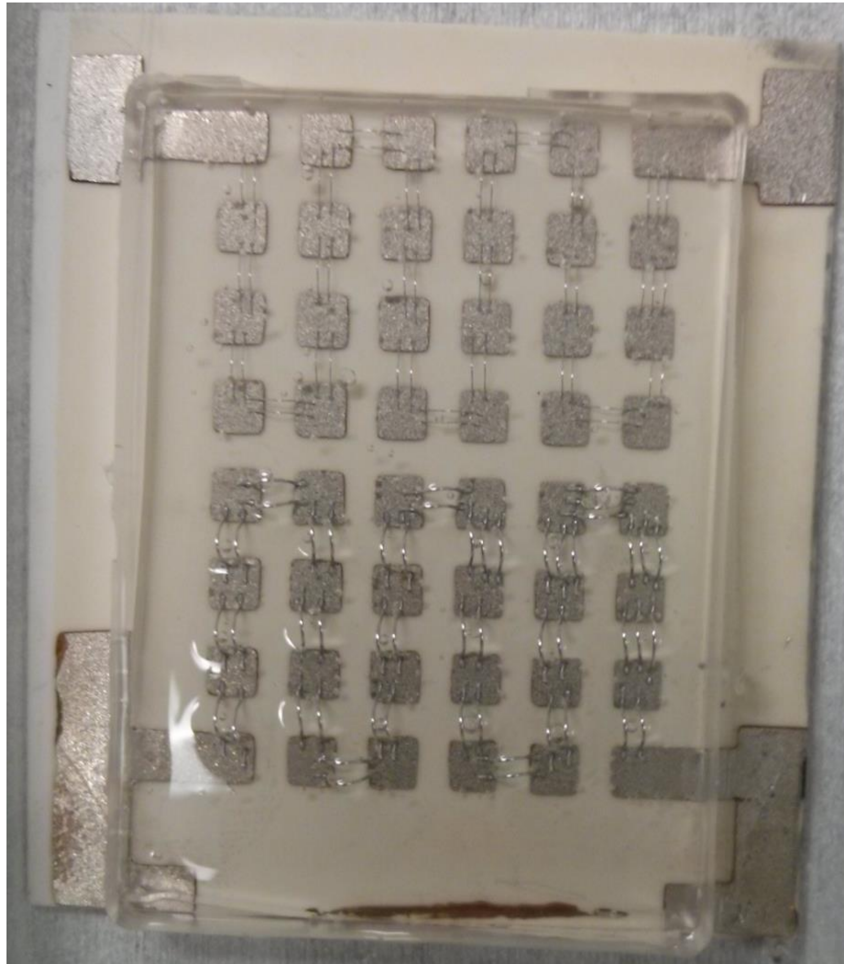


Figure 5.2. Test module with a daisy chain design without power connectors

The corner pads are extended out in such a way that probes can be connected to the end traces. This avoids the necessity to use power connectors for electrical connections.

Module shown in Figure 5.1 incorporates a solder paste in its fabrication process whereas module shown in Figure 5.2 does not incorporate a solder paste in its fabrication process. This is to check the reliability of the module with and without the usage of a solder paste, and hence, the flux incorporated with it.

The following steps are used to fabricate the test modules [1]:

- Ultrasonic cleaning and HCl bath.
- Ni plating: plate a thin layer of Ni on top of DBC substrates
- Dry film: laminate the Ni plated substrate with a thin photosensitive/photoresist film.
- UV rays exposure.
- Develop layout pattern on the substrate.
- Etch substrate to obtain the required pattern; etching bath (chem cut).
- Strip excess photoresist material off the substrate.
- Dicing
- Wirebond
- Power connectors are attached using solder paste (optional)
- Encapsulate the test structure.

5.1.1 Materials used to fabricate

Various materials were used to build the power module and their properties are discussed below.

A. Direct bonded Copper (DBC) substrate:

DBC substrate used for fabricating test structures consists of 0.65mm thick Al_2O_3 ceramic layer sandwiched between two 0.3mm layers of copper. Properties of these insulating substrates are given below and are later used for calculation purposes.

Material Property	**Values**	**Units**
Coefficient of thermal expansion	7.1	ppm/K
Tensile strength	206.9	MPa
Elastic modulus	345	GPa

Table 5.1. DBC substrate material properties [2]

B. Solder paste:

Solder paste is used to attach power connectors to the DBC substrate. Solder paste used here is 92.5% Pb, 5% Sn, 2.5% Ag. Solder flux contains mainly of Rosin (90% or more), other inert materials, and less than 1% of halogens. Table 5.2 provides material properties of solder paste.

Material Property	Values	Units
Thermal conductivity	0.26	W/cm.°C
CTE at 20°C	29	ppm/°C
Tensile strength	4210	PSI
Shear strength	2240	PSI

Table 5.2: Solder paste material properties [indium.com]

C. Power connectors:

Power connectors used are of 0.0032’’ thick and made of C26000 brass. It has a matte tin finish. [12][13]

D. Bond wires:

Wedge bonders are used to wirebond the aluminum (99% aluminum and 1% silicon) bond wires. Table 5.3 lists the properties of the aluminum bond wires.

Material Property	Values	Units
Coefficient of thermal expansion	23	ppm/K
Young’s modulus	69	GPa

Table 5.3. Al bond wire material properties [2]

E. Encapsulation:

Silicone elastomer from Nusil R-2187 is used as the encapsulation. This silicon elastomer has 2 parts; part A and part B that need to be mixed in 10:1 ratio before applying on the substrate.

Material composition of part A is silica amorphous and that of part B is silica amorphous, dimethyl, methyl hydrogen siloxane copolymer. [nusil.com, MSDS Nusil R-2187]

After application on the substrate, the encapsulation needs to be cured at 80°C for 3 hours and then at room temperature for another 20 hours to complete the cure process.

5.2 Theoretical Stress calculations on wirebonds due to thermal cycling

Considering that the board expansion causes the bond wire, displacement of bond wire needs to be considered to calculate the stress on the wire. This expansion of board and wire is due to their difference in coefficients of thermal expansion (CTEs). Major displacement of wire takes place in one direction and assuming this dimension to be x-dimension, theoretical stress calculation are made. The displacement is given as

$$u = (\alpha_{Al} \sim \alpha_{DBC})\Delta T . x \quad (5.1)$$

where,

u = displacement

α_{Al} and α_{DBC} are the coefficients of thermal expansion of aluminum wire and DBC board, respectively.

ΔT = Change in temperature

Strain is calculated per unit measurement of length. Hence [1],

$$\varepsilon_x = (\alpha_{Al} \sim \alpha_{DBC})\Delta T \quad (5.2)$$

$$\varepsilon_x = (23 \times 10^{-6} - 7.1 \times 10^{-6}) \times (250 - (-55))$$

$$\varepsilon_x = 4.85 \times 10^{-3}$$

Since the stress on the wirebond is due to pulling of wirebond on its either ends, the significant non-zero component stress component is calculated. Stress can be calculated using the Equation 5.3. [1]

$$\sigma_x = E_{Al} \times \varepsilon_x \tag{5.3}$$

where,

σ_x = Stress in Pa

E_{Al} = Young's modulus in Pa.

Hence,

$$\sigma_x = 69 \times 10^9 \times 4.85 \times 10^{-3}$$

$$\sigma_x = 334.65 MPa$$

5.3 Experimentation and Testing

5.3.1 Experimentation on un-encapsulated and encapsulated modules having power connectors and solder paste without cleaning solder flux

Layout of the module is based on daisy chain design. Two test structures or samples are fabricated with and without encapsulation. Both samples underwent temperature cycling.

In these test structures, power connectors were attached to the modules using a 92.5Pb 5Sn 2.5Ag high temperature solder paste. The flux residues from the solder paste were not cleaned. This was done in order to study the effects of flux on the power module. Once power connectors were attached, one of the test structures were encapsulated using the Nusil R-2187 silicone elastomer and the other test structure was without encapsulation.

Both the samples (with and without encapsulation) were first tested for connectivity which showed good connection results prior to temperature cycling.

Temperature cycling was performed using a DELTA 9023 furnace shown in Figure 5.3.

Figure 5.3: Thermal cycling furnace

These test structures were then subjected to thermal cycling using the following profile.

- High temperature 250°C, dwell time 60 minutes.
- Low temperature -55°C, dwell time of 5 minutes.
- Iterative: 25 cycles.

Low temperature cooling was accomplished using liquid nitrogen.

5.3.1.1 Observations:

Figures 5.3 and 5.4 show the modules after 25 thermal cycling cycles for the un-encapsulated and encapsulated modules, respectively.

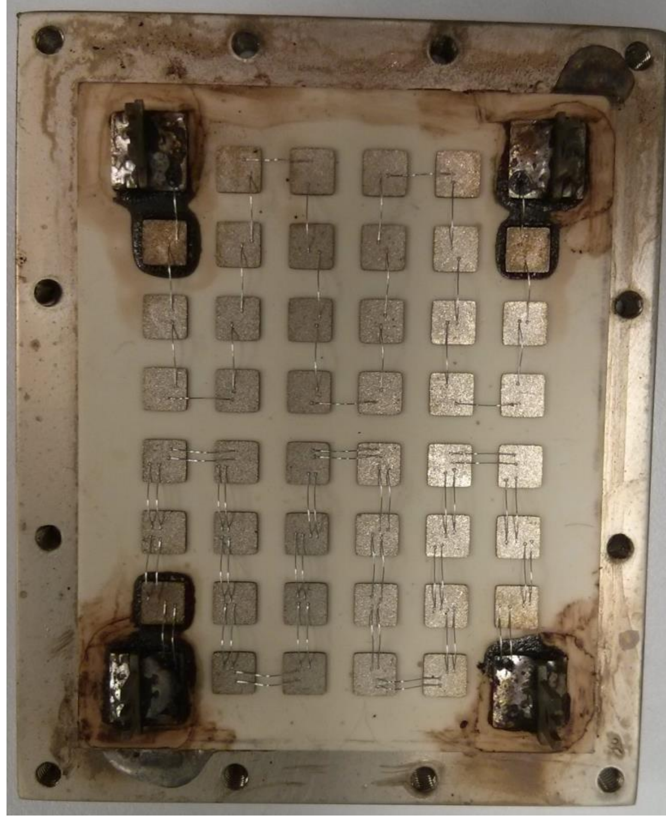


Figure 5.4(a). Un-encapsulated test module after thermal cycling

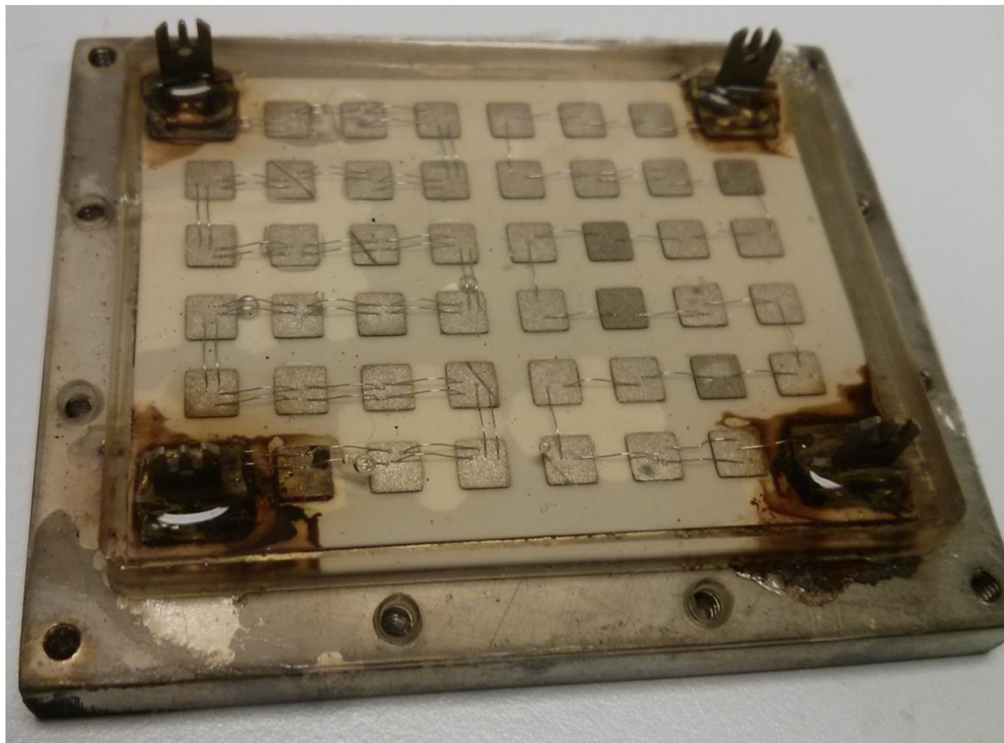


Figure 5.4(b). Encapsulated test module after thermal cycling

A. As seen in the Figures 5.4(a) and 5.4(b), there are regions with dark brown coloration on both the modules, relatively higher in the case of encapsulated test structure than the un-encapsulated one. These dark brown regions are located where flux is left behind around the power connector pads. Wirebond failures occur at these regions, possibly due to corrosion or oxidation degradation of the solder flux.

B. Significant cracks in encapsulated modules appeared in less than 48 hours of continuous exposure to air at the power connector locations. Figures 5.5(a) and 5.5(b) show cracks occurred at the power connectors where there is highest concentration of solder paste, and hence, the largest amount of solder flux being left. This can occur due to the CTE mismatches between the power connectors (CTE 19.9ppm/°C), solder paste (CTE 29ppm/°C), and substrate (for Al_2O_3 substrate 7.1ppm/°C). Cracks in these areas cause displacement of wirebonds, and hence, failure of the test module.

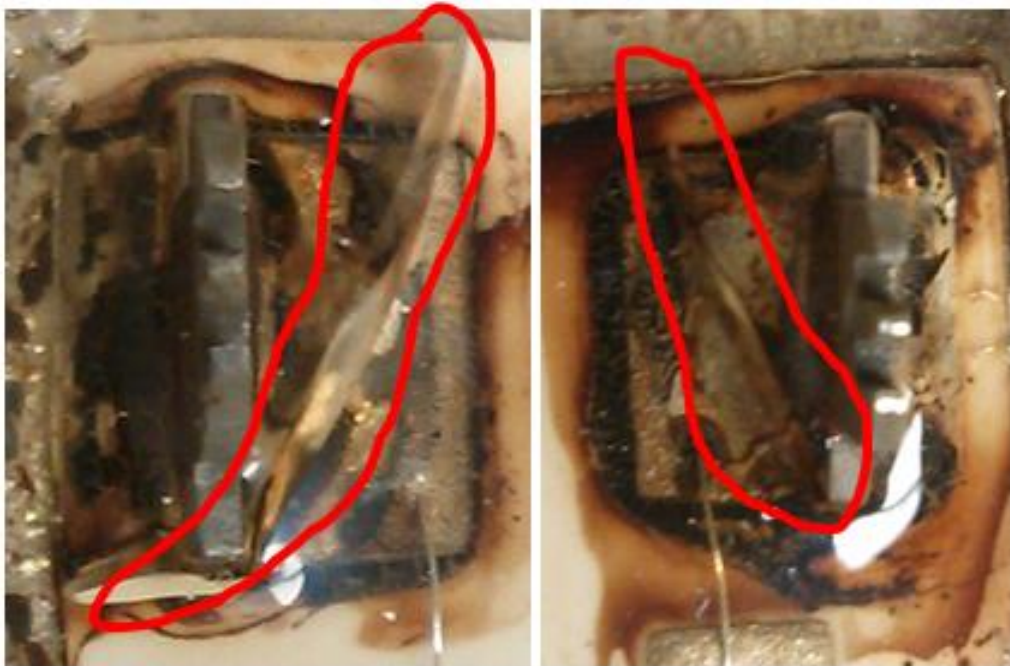


Figure 5.5(a) and (b). Cracks developed in encapsulated test structure

C. Cracks in encapsulation expose some parts of the module to air. This exposure further increases corrosion rate. Aluminum bond wire reacts with small quantities of flux and some other combination of materials destroy its high degree of passivity. These conditions can cause damage to aluminum bond wire; degradation of aluminum bond wires at its connection ends can cause dislocation, and hence, destroy the good wirebond connection. Figures 5.6(a) and (b) show the wirebonds dislocation, and hence, bond failure. It is important to note that the wirebond failure occurs only in encapsulated module and not in the un-encapsulated one. In Figure 5.6(a) it can be observed that the substrate at the perimeter of the wirebond heel, where there is good amount of flux, seems to be cracked, and has damaged the substrate. These microscopic cracks increase the electrical resistance between the substrate and bond wire, and can cause bond wire failure.

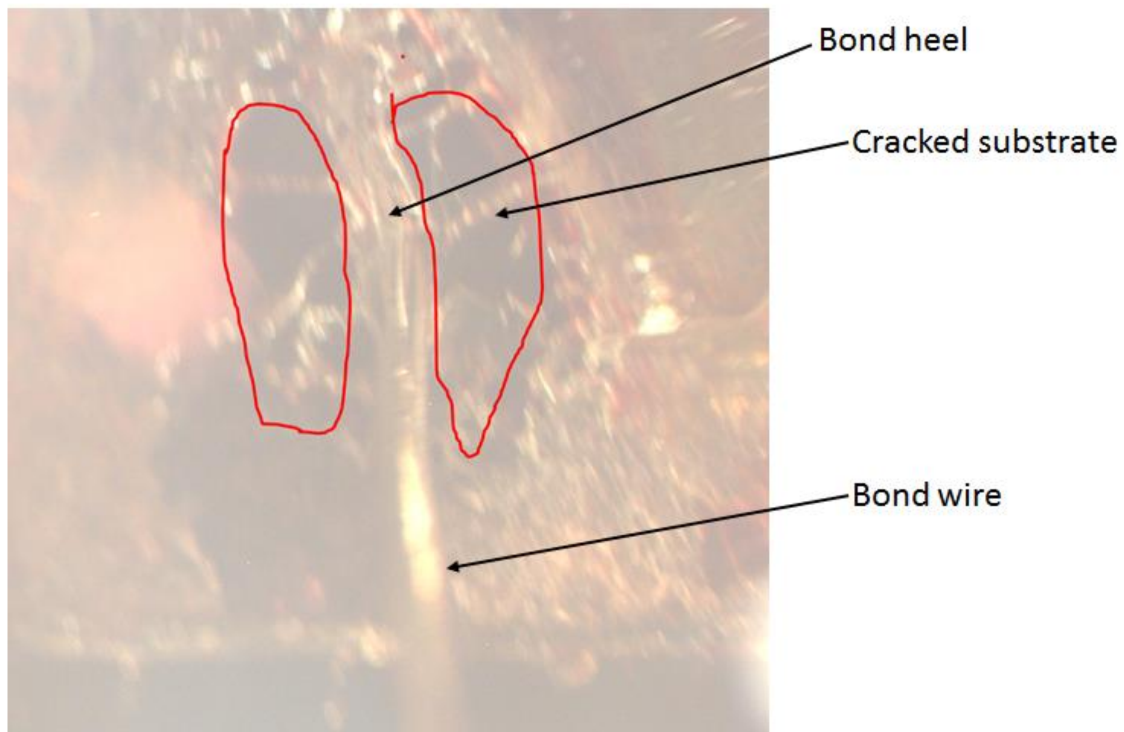


Figure 5.6(a). Faulty wirebonds observed in the test module

Figure 5.6(b). Faulty wirebonds observed in the test module

5.3.2 Experimentation on encapsulated modules having power connectors and solder paste; steps were taken to clean solder flux

Layout design employed for the test structure design is the same as the previous experiment (daisy chain design). Power connectors are attached to the modules using the 92.5Pb 5Sn 2.5Ag high temperature solder paste. The flux residues from the solder paste were cleaned as much as possible before wirebonding and encapsulating the module with Nusil R-2187 silicone elastomer. To clean the flux following procedure was employed:

- Clean or degrease the substrate with Acetone.
- Use abrasive paper to scrape the flux off (#500 was used) and wash it with de-ionized water.
- Re-clean the surface with IPA or isopropanol and wait till it dries.
- Place the substrate in Asher chamber and expose it to Argon for 2 hours then oxygen to remove the flux residues. Plasma treatment hours can be varied and optimized to make best wirebond connections.

These test structures were later subjected to thermal cycling using the following profiles:

- High temperature 250°C, dwell time 60 minutes.
- Low temperature -55°C, dwell time of 5 minutes.
- Iterative: 25 cycles.

Low temperature cooling was performed using liquid nitrogen.

5.3.2.1 Observation:

A. Dark brown coloration in the module is significantly reduced as shown in Figure 5.7. This indicates that the module is not corroded (or less degradation due to air exposure) as in the previous experiment. Since all other parameters in the fabrication process were kept the same as in the experiment 5.3.1 section, and the only procedure included was cleaning of the flux. Thermal cycling of the module did not cause significant brown coloration at the critical spots. This proves that change in color, and hence, trigger for corrosion was infact due to flux material present left in the solder paste.

Figure 5.7. Flux cleaned and encapsulated test structure after thermal cycling

B. Figure 5.8 shows critical regions where cracks were to appear. There are no cracks or very little cracks at these regions unlike the previous test results in 5.2.1. This proves that thermo-mechanical stress that caused cracking at the power connectors region were highly related to flux and encapsulation. Of course after constant exposure to air for more than 5 to 7 days cracks can be developed, but not as significant as in previous experiment. This can be avoided or reduced to a good extent by storing the module in vacuum as mentioned in [14].

Figure 5.8. No cracks at critical points

C. It is not easy to completely remove flux from the substrate. This is because, there will be some flux trapped between the substrate and power connectors or substrate and solder paste. So it is best to use a no-clean solder paste or solder paste that does not require flux for attachment.

5.3.3 Experimentation on un-encapsulated and encapsulated modules for wirebond reliability

In this test, layout of the module has the same daisy chain design but without power connectors. The connector pads are extended such that measurements can be made without power connectors. This is done to avoid solder paste and flux effects on the wirebonds. Both bond wires

of diameters of 5 mil and 12 mil are used. This is done to later check the reliability of the 5 mil and 12 mil bond wires after thermal cycling. Layout of the module is shown in Figure 5.9.

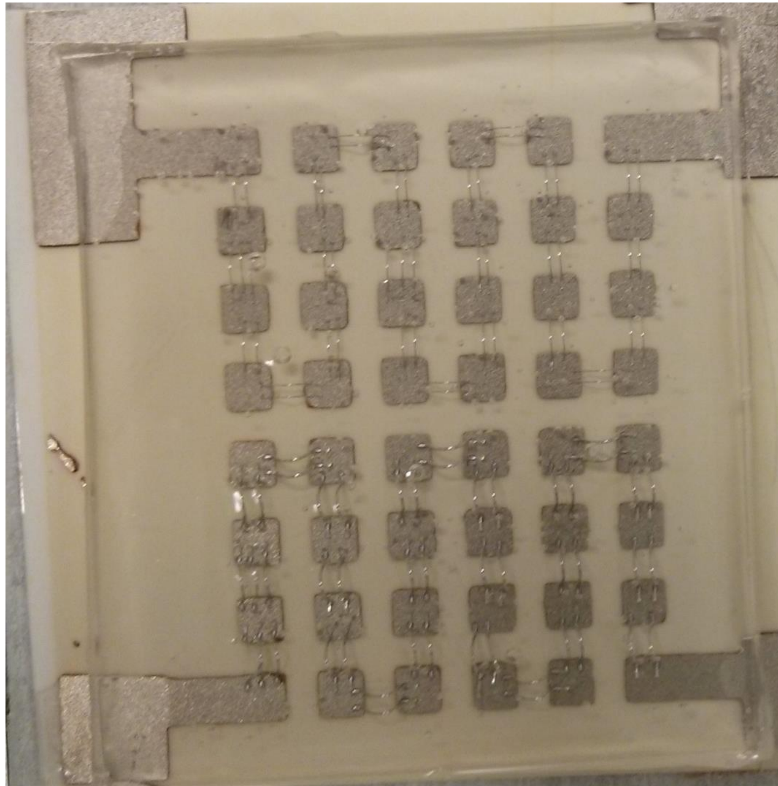


Figure 5.9. Test module with no power connectors

These test modules were subjected to thermal cycling using similar profile as before:

- High temperature 250°C, dwell time 60 minutes.
- Low temperature -55°C, dwell time of 5 minutes.
- Iterative: 25 cycles.

Low temperature cooling was performed using liquid nitrogen.

5.3.2.2 Observation:

Wirebonds loses their shape at the points where wire connects to the surface (bond position). This change in shape depends on the bonder and type of bonding.

In wedge bonding, edges of wire are flattened, and hence, diameter of the wire decreases. This deformation is given by

$$Deformation\ ration = {(Wire\ width\ at\ bond\ points)}/{(Actual\ diameter\ of\ wire)} \ldots..[5.4]$$

For 12 mil wirebonds, wire width at bond points is around 8 mils. Hence,

$$Deformation\ ration = {8}/{12} = 0.667 \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots...[5.5]$$

For 5 mil wirebonds, wire width at bond points is around 3 mils. Hence,

$$Deformation\ ration = {3}/{5} = 0.6 \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots..[5.6]$$

Table 5.4 shows the connectivity test results for the encapsulated and un-encapsulated test structure before and after thermal cycling.

Before thermal cycling	5 mil wirebonds path	12 mil wirebonds path
Encapsulated layout	Pass	Pass
Un-encapsulated layout	Pass	Pass

Table 5.4(a). Wire-bonded trace/path connectivity test before thermal cycling

After thermal cycling	5 mil wirebonds path	12 mil wirebonds path
Encapsulated layout	**Fail**	Pass
Un-encapsulated layout	Pass	Pass

Table 5.4(b). Wire-bonded trace/path connectivity test after thermal cycling

Wirebond pull tests were performed on wirebonds before and after thermal cycling. Their measured strengths are shown in Table 5.5.

	5 mil wirebonds (gramsForce)	12 mil wirebonds (gramsForce)
Before thermal cycling	55-70	550-600
After thermal cycling	40-50	350-500

Table 5.5. Wirebond pull strength

As seen in Table 5.5, the 12 mil wirebond strength is much larger than those for the 5 mil wirebonds. Hence when the same thermal stress (due to thermal cycling) is applied on both the bond wires, 5 mil wirebonds tend to fail relatively quicker than the 12 mil bond wires. Also, from Table 5.5, pull strength decreases after thermal cycling, and hence, proving that thermal stress affects the reliability of the wirebonds.

Some other observations and discussions from the experiment are given below:

A. One of the test structures was designed in such a way that a large trace of copper in the DBC substrate was exposed without being encapsulated. As seen in Figure 5.10, copper is delaminated from the insulating Al_2O_3 layer. This is due to the CTE mismatch, and hence, thermal stress between the Al_2O_3 (7.1ppm/°C) substrate and the copper layer (17ppm/°C).

Figure 5.10. De-lamination of Copper layer from the Al_2O_3 substrate.

Theoretical stress calculations can be made by applying same concept as in Equation (5.2):

$$\varepsilon_x = (\alpha_{Cu} \sim \alpha_{Al2O3})\Delta T \text{ ....[5.7]}$$

$$\varepsilon_x = (17 \times 10^{-6} - 7.1 \times 10^{-6}) \times (250 - (-55))$$

$$\varepsilon_x = 3.02 \times 10^{-3} \text{ ....[5.8]}$$

Equation (5.3) is used to calculate stress on copper layer,

$$\sigma_x = 120 \times 10^9 \times 3.02 \times 10^{-3} \text{.................................[5.9]}$$

Young's modulus for copper can vary from 110GPa to 128GPa and 120GPa is considered for calculations.

$$\sigma_x = 362.4MPa \text{..[5.10]}$$

Force on the copper layer is equal to the product of thermal stress and area, hence directly proportional to area. Hence design a module in such a way that layout has copper traces have small areas. Having large copper traces encapsulated will add force from thermal stress on the encapsulation, instead of directly on copper trace. So, to avoid applying higher force on a large copper trace which causes de-lamination, the area outside the encapsulation borders should be decreased.

Large copper trace was encapsulated in such a way that, 2mm × 8mm space was left un-encapsulate on one side and 20mm × 8mm on the other side. Figure 5.11 shows that de-lamination is higher on the 20mm × 8mm side than on 2mm × 8mm side. Encapsulating even the 2mm × 8mm space will further avoid de-lamination.

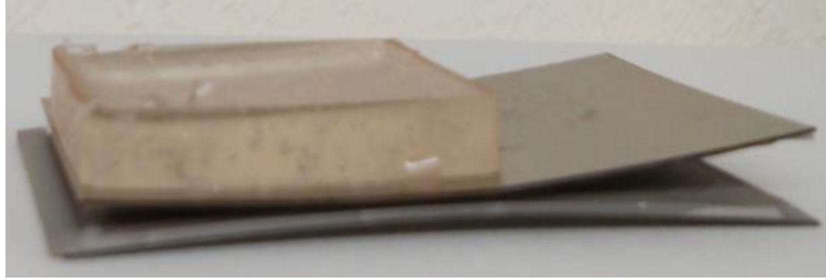


Figure 5.11. De-lamination of copper layer decreases with encapsulation.

B. Slight de-lamination of the encapsulation was observed at the corners of the module in some test structures as shown in Figure 5.11. This de-lamination of encapsulation adds extra stress on the wirebonds at the corner regions and if strong enough, can cause wirebond lift-off at its connection points, and hence, create a wirebond failure.

Figure 5.12. De-lamination of encapsulation from the DBC substrate

To avoid this, encapsulation with higher adhesion properties to the substrate and less viscous is preferred. Also, encapsulation which hardens less after cure than the Nusil R-2187 is preferred. A high temperature Hysol epoxies, TSE351 silicones should be investigated.

C. In one of the test-structures, the cured encapsulation developed a long horizontal crack after thermal cycling as shown in Figure 5.12

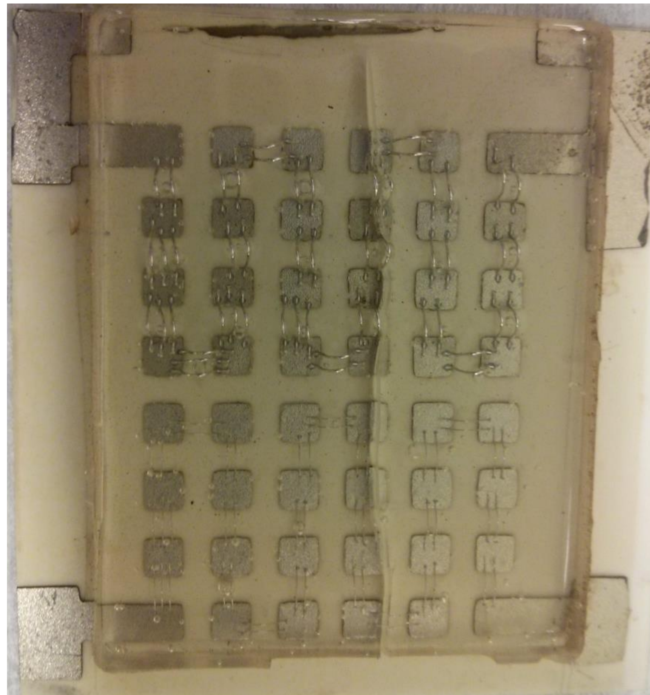
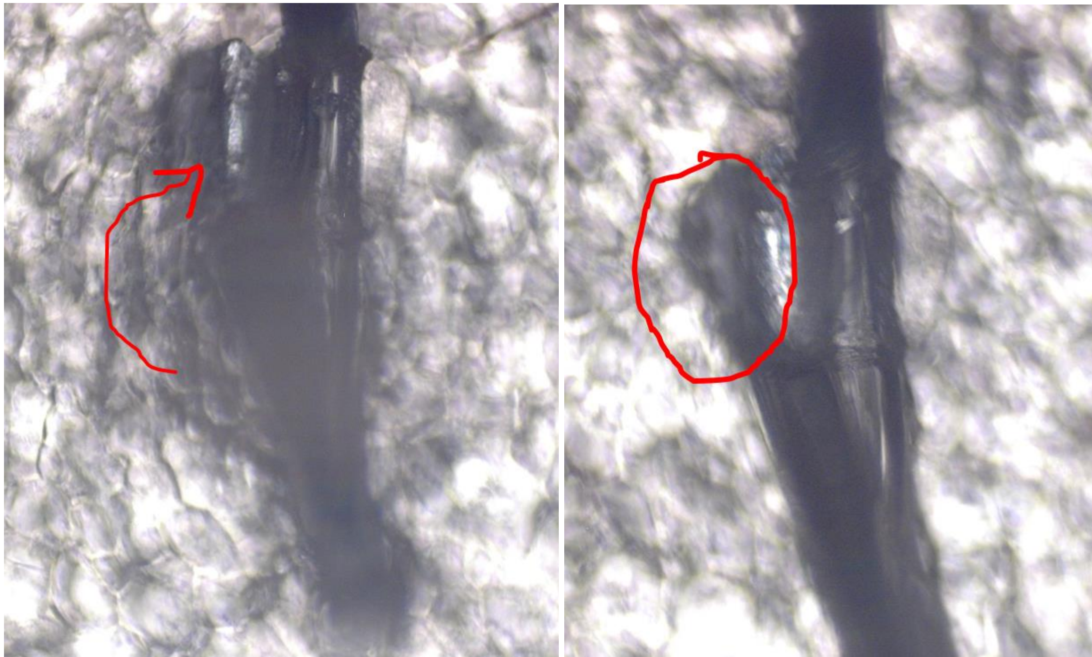


Figure 5.13. Horizontal crack developed on the test module

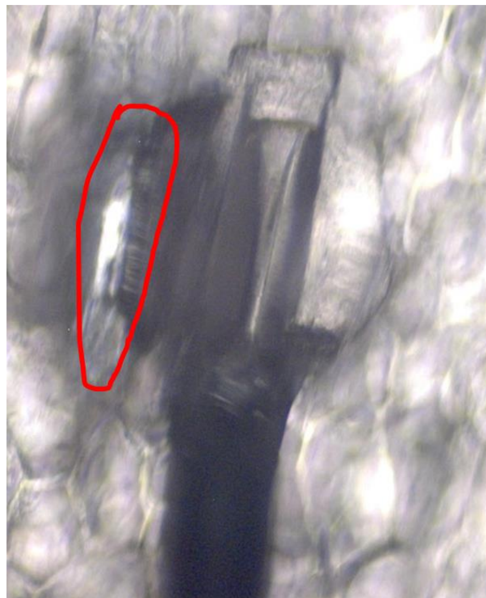
Under microscopic observation, some of the 5 mil wirebonds in the path of this crack seem to be displaced. However, 12 mil wirebonds were working just fine. This indicates that the thermal and mechanical force was high enough to dislocate the 5 mil wirebonds, but was not high enough to displace the 12 mil wirebonds.

D. Following microscopic observations in Figure 5.13 show some of the faulty 5 mil wirebonds. Heel of the 12 mil wirebonds shows no breakage or dislocation unlike 5 mil

wirebonds. These 12 mil wirebonds are strong enough to withstand the stress from thermal cycling and still form good connections. The 12 mil wirebonds are shown in Figures 5.14 (a) and (b).

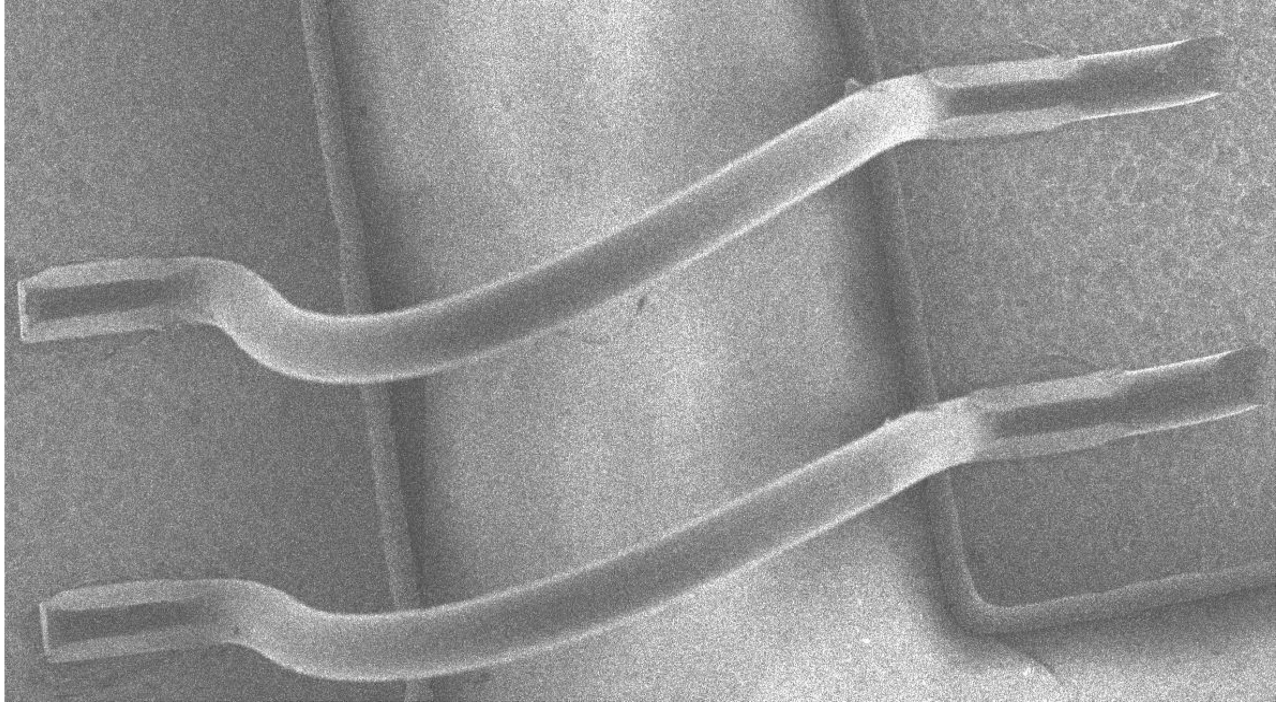


(a) (b)



(c)

Figure 5.14. Faulty 5 mil wirebonds.


(a)

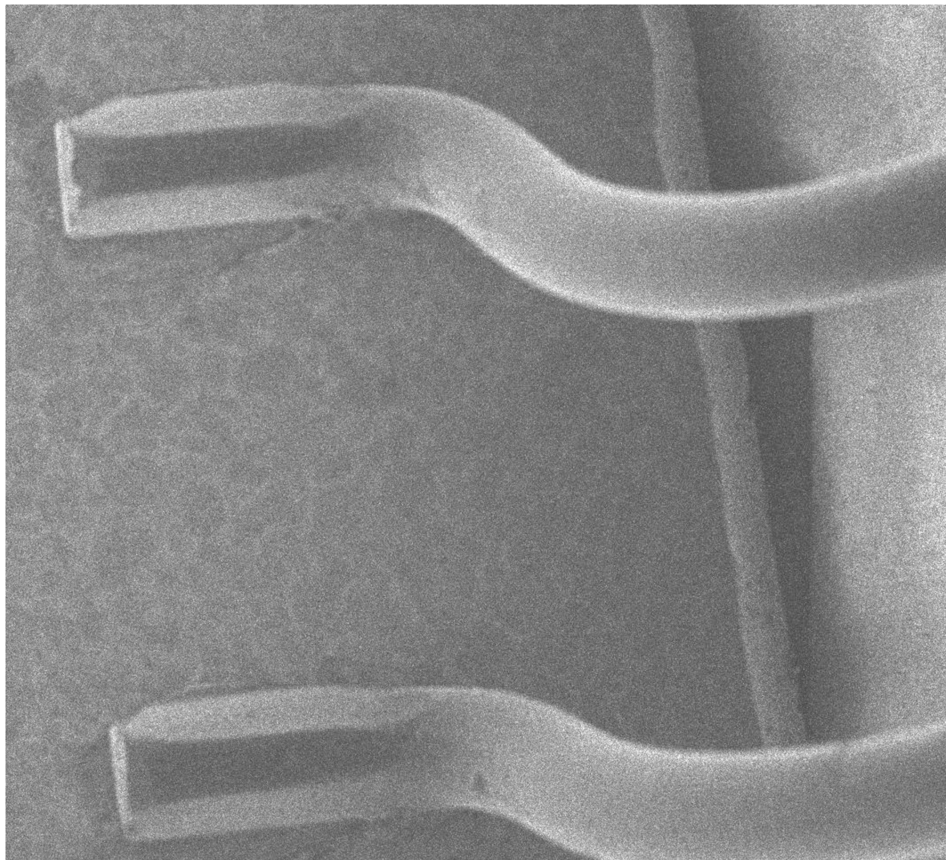

(b)

Figure 5.15. 12 mil wirebonds

5.4 Improving wirebond reliability

From Table 5.4(b), it was concluded that thermal cycling on test structure with encapsulation caused thermal and mechanical stress enough to dislocate or damage 5mil wirebonds, but were not enough to cause reliability issues in 12mil wirebonds. To increase the reliability of 5mil wirebonds on test structure with encapsulation, it is necessary to avoid application of stress directly on wirebonds. A thermally stable conformal coating which acts as a buffer layer between wirebonds and encapsulation was chosen for this purpose. Material chosen is a polyamideimide (PAI), Tritherm A 981-H-25.

Steps included in fabrication process:

- After cleaning the substrate, wirebond the test structure.
- Spin coat the test structure at 2000RPM with polyamideimide (PAI) and cure at 200ºC for an hour.
- Repeat above step one more time to give test structure two coatings (thick) of polyamideimide.
- This test structure is encapsulated.

5.4.1 Observation

A. Table 5.6 shows connectivity test results for non-PAI coated and PAI coated, encapsulated test structures (AlN and Al_2O_3) after thermal cycling. Figures 5.15(a) and (b) shows PAI coated test-structures before and after thermal cycling.

After thermal cycling	5 mil wirebonds path	12 mil wirebonds path
Non-PAI coated	Fail	Pass
PAI coated	**Pass**	Pass

Table 5.6. Wire-bonded trace/path connectivity test after thermal cycling

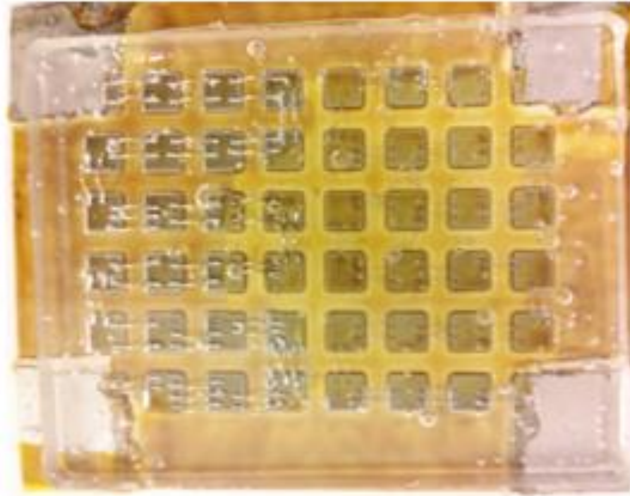


Figure 5.16(a). PAI coated test structure before thermal cycling

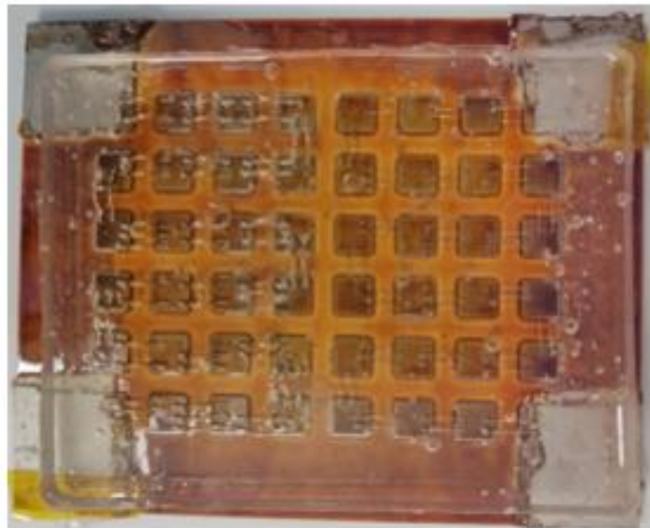


Figure 5.16(b). PAI coated test structure after thermal cycling

As seen in Table 5.6, both 5mil and 12mil wirebonds in PAI coated test structures PASS connectivity tests after thermal cycling. The mechanical stress on the wirebonds due to thermal cycling will be absorbed by the PAI coated on the wirebonds. This decreases the stress on wirebonds, and hence, increasing wirebond reliability.

B. From Figure 5.15(b), it can be seen that there were no cracks developed on the encapsulation layer of the PAI coated test structure. However, Figure 5.16 shows large cracks on the encapsulation layer when the test structure was not coated with PAI. Hence,

apart from improving wirebond reliability, PAI also improves thermal stability and decrease mechanical failure of encapsulation.

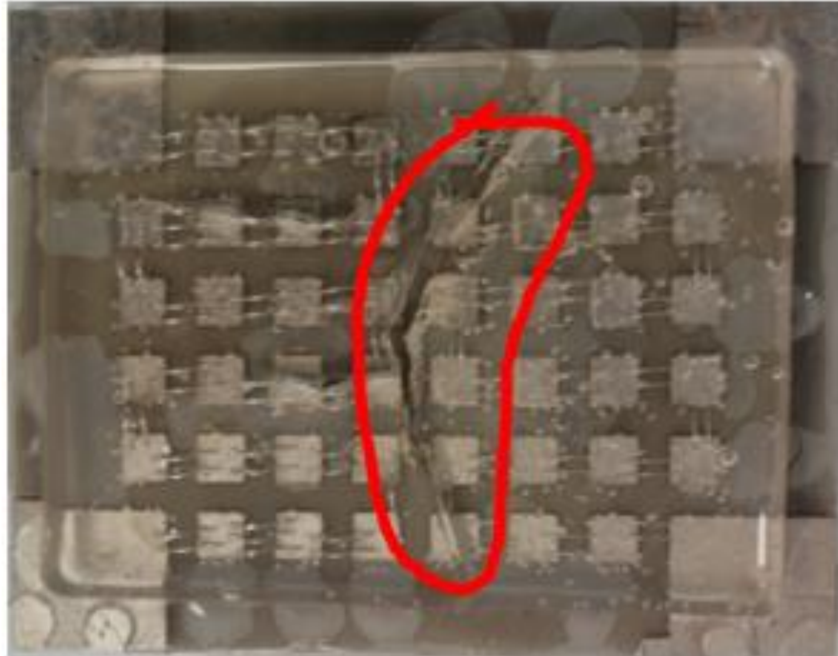


Figure 5.17. Non-PAI coated test structure

5.5 Discussions and conclusion

For an effective power module,

- Use solder pastes or solder preforms that has no flux. This is preferred in order to avoid corrosion in the module and additional thermal stress on the wirebonds.
- If in case of using solder pastes which contains flux, make sure to clean the substrate as much as possible to remove all the flux before encapsulating it. Cleaning the flux depends on the type of solder and flux used. Generalized process includes:
    - Degreasing with acetone.
    - Scrubbing solid and hard flux with abrasive sheets.
    - Cleaning with IPA (isopropyl) solution.
    - Exposing it to Argon and Oxygen in Asher chamber under plasma conditions.

- Larger the diameter of the wirebond, higher is the pull strength, and hence, it can tolerate higher stress levels. Thus improving its reliability. Hence, 12 mil wirebond has a better reliability compared to 5 mil wirebond. In cases where only small diameter wirebonds can be used (for example; gate connections), for improved reliability wirebond can be done under high temperatures or other types of bonding can be used (example: instead of wedge bonder, go for ball-wedge bonder etc.).
- Coating the substrate with polyamideimide proves to be a good fabrication step to improve wirebond reliability and provides stability to encapsulation.
- To avoid de-lamination of copper layer from the underlying insulating layer, design with small copper pads and traces.

CHAPTER 6. CONCLUSION

6.1 Conclusions and discussions

In this thesis research thermal analysis is performed on power electronic module using SolidWorks thermal simulator. Simulations were performed on various parameters such as power dissipation, maximum junction temperature, ambient temperature, substrate size, and convection coefficient. The results provide a good estimation in selecting parameters for thermally efficient power modules layout design. For optimum performance, ΔT (maximum junction temperature – ambient temperature) should be greater than $125^{O}C$ for power electronic modules that dissipates medium and high power. For a low ΔT and high power dissipation, baseplate acts more like a thermal resistance than a heat-spreader. Hence, it is ineffective to employ base-plates for these cases. Increasing substrate size to bring down maximum junction temperature is more effective in higher power dissipation cases, than those for medium or low power dissipation.

Time domain reflectometry (TDR) technique proves to be a good measurement technique for parasitics in power electronic modules. Parasitics were simulated using Q3D software on test structures and compared to measurement results from the TDR technique. Both results showed similar parasitic values with good accuracy. This approach provides a way for verifying parasitics in power electronic modules. TDR technique can also aid in non-destructive failure analysis of a malfunctioning module.

Reliability of wirebonds for various parameters is investigated and results are presented. Flux from solder paste, if left un-cleaned, can cause a reliability issue. Residual solder flux can cause corrosion that can lead to wirebond failure. Thermal cycling was performed on 5 mil and 12 mil wirebonds with and without encapsulation. It was noted that the 12 mil wirebonds have a better

reliability than the 5 mil wirebonds. This is due to the increased strength at the heel of 12 mil wirebonds because of a larger heel diameter, and hence, can withstand higher stress levels. Coating the substrate with polyamideimide proved to be a good fabrication step to improve wirebond reliability, and to provide stability to encapsulation. 5mil wirebonds reliability improved after coating the substrate with polyamideimide. Also, there were no cracks observed on the encapsulation layer after thermal cycling the PAI coated test structures. To avoid de-lamination of copper layer from the underlying insulating layer, copper layers should be encapsulated.

6.2 Future works

- Results obtained from studies of thermal analysis in SolidWorks simulation tool can be used to obtain a rough approximation values when selecting initial values for parameters. More detailed and accurate studies can be made using software other than SolidWorks like Ansys, Comsol etc and their results can be used to set up a more accurate database.
- Other parameters such as number of dies and its relation to uniform heat distribution in power electronic module can be considered to further improve the design data.
- Accuracy in parasitic inductance extraction using the TDR technique can be further improved using better fixtures and high precision tools with a faster rise time.
- Methods to extract parasitic capacitance and impedance on fabricated power electronic modules should be considered.
- Flux trapped beneath the power connectors can be reliability problem. Effective means to remove this residual flux is to be investigated.
- Other reliability tests such as thermal shocks and power cycling can be performed on modules to better understand the wirebond failure of power modules.

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