Interleaved Buck Converter Based Shunt Active Power Filter with Shoot-through elimination for Power Quality Improvement

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Dedicated

to

my son

Zinith Patel

... Ranjeeta Patel

Declaration of Originality

I, *Ranjeeta Patel*, Roll Number *512EE8011* hereby declare that this dissertation entitled *Interleaved Buck Converter Based Shunt Active Power Filter with Shoot-through elimination for Power Quality Improvement* presents my original work carried out as a doctoral student of NIT Rourkela and, to the best of my knowledge, contains no material previously published or written by another person, nor any material presented by me for the award of any other degree or diploma of NIT Rourkela or any other institution. Any contribution made to this research by others, with whom I have worked at NIT Rourkela or elsewhere, is explicitly acknowledged in the dissertation. Works of other authors cited in this dissertation have been duly acknowledged under the sections "Reference" "Bibliography". I have also submitted my original research records to the scrutiny committee for evaluation of my dissertation.

I am fully aware that in case of any non-compliance detected in future, the Senate of NIT Rourkela may withdraw the degree awarded to me on the basis of the present dissertation.

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Abstract

The “shoot-through” phenomenon defined as the rush of current that occurs while both the devices are ON at the same time of a particular limb is one of the most perilous failure modes encountered in conventional inverter circuits of active power filter (APF). Shoot-through phenomenon has few distinct disadvantages like; it introduces typical ringing, increases temperature rise in power switches, causes higher Electromagnetic Interference (EMI) and reduces the efficiency of the circuit. To avert the “shoot-through”, dead time control could be added, but it deteriorates the harmonic compensation level. This dissertation presents active power filters (APFs) based on interleaved buck (IB) converter. Compared to traditional shunt active power filters, the presented IB APFs have enhanced reliability with no shoot-through phenomenon.

The instantaneous active and reactive power (p-q) scheme and instantaneous active and reactive current component (i_d-i_q) control scheme has been implemented to mitigate the source current harmonics. Type-1 and Type-2 fuzzy logic controller with different membership functions (MFs) viz. Triangular, Trapezoidal and Gaussian have been implemented for the optimal harmonic compensation by controlling the dc-link voltage and minimizing the undesirable losses occurred inside the APF. Additionally, the adaptive hysteresis band current controller (AHBCC) is being implemented to get the nearly constant switching frequency. The performance of the control strategies and controllers for the presented IB APF topologies has been evaluated in terms of harmonic mitigation and dc-link voltage regulation under sinusoidal, unbalanced sinusoidal and non-sinusoidal voltage source condition.

This dissertation is concerned with the different topologies of 3-phase 4-wire IB APFs viz. split capacitor (2C) topology, 4-leg (4L) topology, transformer based full-bridge IB APF or single capacitor based FB IB APF (1C 3 FB IB APF) and full-bridge IB APF (FB IB APF) for low to medium power application. Moreover, APF topology is now being

expanded to multilevel VSIs for high power application. Thanks to flexible modular design, transformerless connection, extended voltage and power output, less maintenance and higher fault tolerance, the cascade inverters are good candidates for active power filters with the utility of high power application. The cascaded FB IB APF is modelled with no shoot-through phenomenon by using multicarrier phase shifted PWM scheme.

Extensive simulations have been carried out in the MATLAB / Simulink environment and also verified in the OPAL-RT LAB using OP5142-Spartan 3 FPGA to support the feasibility of presented IB APF topologies, control strategies and controllers during steady and dynamic condition. The performance shows that IB-APF topologies bring the THD of the source current well below 5% adhering to IEEE-519 standard. A comparison has also been made, based on SDP (switch device power) between the IB-APF topologies.

Keywords: Shoot-through phenomenon; IB APF; p-q and i_d-i_q control strategy; Fuzzy1, Fuzzy2, SDP rating, OPAL-RT

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Acronyms

PQ	Power Quality
IEEE	Institute of Electrical and Electronics Engineers
THD	Total Harmonic Distortion
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CSI	Current Source Inverter
VSI	Voltage Source Inverter
APF	Active Power Filter
UPQC	Unified Power Quality Conditioner
IB	Interleaved Buck
IB APF	Interleaved Buck Active Power Filter
HB IB APF	Half Bridge Interleaved Buck Active Power Filter
FB IB APF	Full Bridge Interleaved Buck Active Power Filter
2C IB APF	Capacitor Midpoint Split Capacitor Interleaved Buck Active Power Filter
p-q theory	Instantaneous Active and Reactive Power Theory
i_d-i_q theory	Instantaneous Active and Reactive Current Theory
LPF	Low Pass Filter
HPF	High Pass Filter
PI	Proportional Integral Controller
FLC	Fuzzy Logic Controller
T1FLC	Type-1 Fuzzy Logic Controller
T2FLC	Type-2 Fuzzy Logic Controller
MF	Membership Function
UMF	Upper Membership Function
LMF	Lower Membership Function

LOM	Largest (Absolute) Value of Maximum
MOM	Mean value of Maximum
FIS	Fuzzy Inference System
BOA	Bisector of Area
COA	Centroid of Area
FOU	Foot Point of Uncertainty
NB	Negative Big
NM	Negative Medium
NS	Negative Small
ZE	Zero
PB	Positive Big
PM	Positive Medium
PS	Positive Small
4L IB APF	4-Leg Interleaved Buck Active Power Filter
1C 3FB IB APF	Single Capacitor Three Full Bridge Interleaved Buck Active Power Filter
FB IB APF	Full Bridge Interleaved Buck Active Power Filter
PWM	Pulse Width Modulation
IPD PWM	In-phase Disposition Pulse Width Modulation
POD PWM	Phase Opposition Disposition Pulse Width Modulation
APOD PWM	Alternate Phase Opposition Disposition Pulse Width Modulation
PS PWM	Phase Shifted Pulse Width Modulation
RTDS	Real Time Digital Simulator
HDL	Hardware Description Language
HIL	Hardware-in-the-Loop
FPGA	Field-Programmable Gate Array
JTAG	Joint Test Action Group
CPLD	Complex Programmable Logic Device
PCIe	Peripheral Component Interconnect Express
I^2C	Inter Integrated Circuit
EEPROM	Electrically Erasable Programmable Read Only Memory
DSO	Data Storage Oscilloscope
RT-XSG	Real-Time Xilinx System Generator

Notations

A	Type-1 fuzzy set
$\tilde{A}$	Type-2 fuzzy set
v_a, v_b, v_c	Source voltage (Phase)
v_0	Zero-axis reference voltage
i_a, i_b, i_c	Source current (Phase)
i_n	Source neutral current
i_{La}, i_{Lb}, i_{Lc}	Load current of phase a,b and c
i_{Ln}	Load neutral current
$i_{L\alpha}, i_{L\beta}$	α and β-axis reference load current
i_{Ld}, i_{Lq}	d and q-axis reference load current
$\bar{\imath}_{Ld}, \bar{\imath}_{Lq}$	dc component of d and q-axis load current
$\tilde{\imath}_{Ld}, \tilde{\imath}_{Lq}$	ac component of d and q axis load current
i^+_{Ld1h}, i^+_{Lq1h}	Transformed dc quantity of first harmonic current of positive sequence
i_{Ldnh}, i_{Lqnh}	ac component of current must be injected by the active power filter
i_{L0}	Zero-axis load current
i_{ca}, i_{cb}, i_{cc}	Compensating current/filter current of phase a, b and c
i_{cn}	Neutral compensating current
$i^*_{ca}, i^*_{cb}, i^*_{cc}$	Reference compensating current of phase a, b and c
i^*_{c0}	Zero-axis compensating current
v_α, v_β	α and β - axis reference phase voltage
$i^*_{c\alpha}, i^*_{c\beta}$	α and β - axis reference compensating current
i^*_{c0}	Zero-axis reference compensating current
p, q	Instantaneous active and reactive power
p_0	Zero-axis instantaneous active power

$\bar{p}, \tilde{p}$	Average and oscillating component of instantaneous active power
$\Delta\bar{p}$	Additional average power
$\bar{p}_0$	Average zero sequence power
$\bar{p}_{loss}$	Losses occurred inside the voltage source inverter
V_{dc}	dc-link voltage
V_{dc}^*	Reference dc-link voltage
E	Error
ΔE	Change in error
σ	Width
$\mu_A(x)$	Type-1 membership function
$\tilde{\mu}_A(x,u)$	Type-2 membership function
X	Universe of discourse

Chapter 1

Introduction

The advances in power electronics have increased the harmonic contamination in the line current which has encouraged the development of active power filter that are intended to block all non-fundamental current. One of the main concerns in the research of active power filter is reliability. The “shoot-through” phenomenon occurs in the conventional inverter circuit decreases the reliability of the active power filter. To overcome shoot-through, various investigations have been done, out of which, interleaved buck (IB) inverter topology is exceptional and suits to be utilized in the application with the requirement of high reliability and harmonic compensation.

In addition to harmonics, other problems such as unbalanced source current and excessive current flowing through the neutral conductor due to the unbalancing of loads must be considered in the power system. The excessive zero sequence current due to unbalanced load can possibly lead to the damage of the neutral conductor. Hence, various topologies of 4-wire active power filters (APFs) came into the arena of research. The various conventional shunt active power filter topologies have been presented and they are split capacitor (2C) APF, 3-phase 4-leg APF, 3-bridge 4-wire APF, 3-Level H-Bridge APF and multilevel cascaded H-bridge/Full-bridge APF. The 2C topology and 3-phase 4-leg (4L) topology is usually used for low power application. The voltage that appears across split capacitor and 3-phase 4-leg inverter topology is the three phase voltage (400 V), therefore the required dc-link voltage increased, which raises the rating of the inverter (particularly switching device voltage rating). For the medium power application, there will be increased rating demand of the switches, which limits the installation of the split capacitor (2C) and 3-phase 4-leg topology. Likewise, the topologies used for the medium power applications are 3-bridge 4-wire APF and 3-level H-bridge/Full-bridge APF. In these APF

topologies, single phase voltage (230 V) appears across each H-bridge/Full-bridge inverter of the corresponding phases. The dc-link voltage requirement in full bridge inverter is reduced by a factor of $\sqrt{3}$, as compared to split capacitor (2C) and 3-phase 4-leg APF resulting in reduction of required switching device's voltage rating. Moreover, APF topology is now being expanded to multilevel VSIs for high power application.

Currently, various control strategies have been developed, out of which the p-q control scheme has gained well recognition, but gives imprecise harmonic compensation in non-ideal supply conditions. The i_d-i_q control strategy without PLL is found to be the most suitable, because several synchronization problems can be evaded with non-ideal supply voltages and with better harmonic compensation. Additionally, the adaptive hysteresis band current controllers have been introduced with the establishment of an attractive feature that the hysteresis band is being encoded as a function of the supplied parameters of the source and load to enhance the PWM performance, which results in the reduction of switching losses in the inverter power switch with nearly constant switching frequency.

The researchers are also worried to maintain the dc-link voltage constant as one of the key aspect to the harmonic compensation performance of the APFs. So different controllers have been used like Proportional- Integral (PI) controller and fuzzy logic controller (FLC). The fuzzy logic controller is found to be a better replacement for PI controller as no accurate mathematical model is needed, can work with imprecise inputs and handles non-linearity. With the development of Type-2 fuzzy logic controller having the ability to handle uncertainty, more attention has been given in recent years. The Type-2 fuzzy sets are the extension of ordinary fuzzy sets or Type-1 fuzzy sets. The Type- 2 fuzzy set is being characterized by three dimensional features. Again, in the interval Type-2 FLC, the third dimension value is same everywhere and hence it is ignored.

In this dissertation, various types of three-phase four-wire (3-phase 4-wire) and cascaded H-bridge/Full-bridge interleaved buck converter based active power filter (IB APF) have been modeled for higher reliability and efficiency; that can be used in the three phase distribution lines for harmonic current compensation.

This chapter is being outlined as: Section 1.1 gives the idea about the efforts that has been done in this dissertation as literature survey. Section 1.2 describes the power quality issues and gives the brief description about the most dominant PQ problem, harmonics. Section 1.3 provides the information about the different solution for mitigation of harmonics.

Section 1.4 gives the classification and topologies of active power filter based on the supply system. Section 1.5 depicts the multilevel inverter based active power filter for high power application in brief. Section 1.6 describes about the "shoot-through" phenomenon and its elimination which are the basis of this dissertation. Section 1.7 describes the various control strategies used for active power filters. Section 1.8 summarizes the motivations and objectives and finally section 1.9 clearly outlined the dissertation structure.

1.1 Research Background

Since 1980s, the active power filter latches increasing researches and implementation due to its outstanding performance. But, in the past two decades only, the researchers are worried about the reliability of the conventional voltage source inverter (VSI) and conventional VSI based active power filter. However, with the requirement of high reliability in the application, the conventional inverter based active power filter would suffer from perilous "shoot-through" phenomenon.

To avoid this perilous shoot-through phenomenon, dead time could be introduced to the drive signals. However, the dead-time control scheme provides error in the output voltage; affecting the compensation performance. An enormous number of researches have been performed to overcome the dead- time effects. The different kinds of compensators used to compensate the dead time, anyway achieve the good theoretical results, but not the practical application because of the used delay circuits.

Furthermore, these used methods did not able to avoid the shoot-through phenomenon radically. The researchers mainly focused on the elimination of the dead time effects, but the control methods are complex and hence cannot eliminate the dead time profoundly. The interleaved buck converter is one of the inverter circuits which can eliminate the shoot-through phenomenon without dead time effect [1-2].

1.2 Electrical Power System Quality

The term power quality (PQ) can be broadly defined as to assess and maintain a good quality of power with nearly sinusoidal bus voltage at the level of generation, transmission, distribution and utilization of electrical energy to the load at rated magnitude and frequency [3]. In addition the energy supplied to the consumer must be without interference or interruption from the reliability point of view. Since the power quality

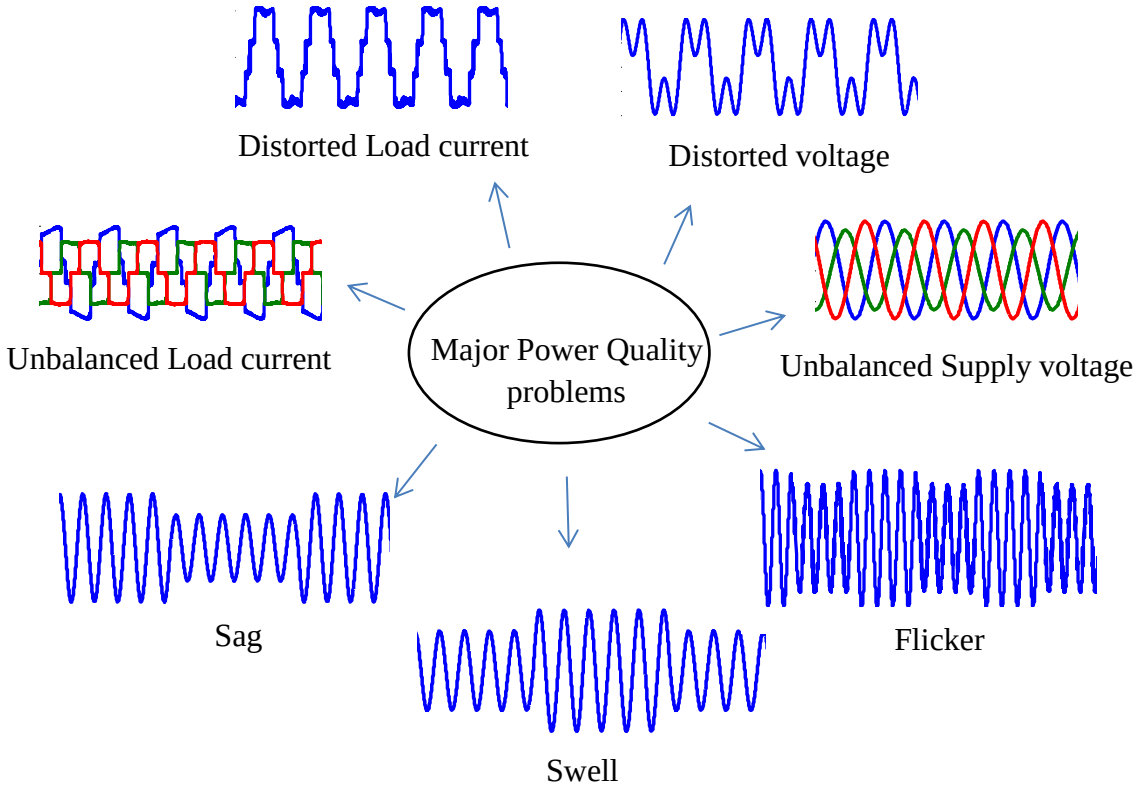


Figure 1.1: Major power quality problems

issues are much more prominent at the utilization level, the researchers give more attention to the distribution system. The main causes of PQ issues are power system faults, switching transients, lightning, non-linear load, adjustable speed drives (ASDs), traction drives, starting of large motor loads, etc. We are so much concerned about the PQs problems because of the economic value. The economic impacts are mainly on the utility, their customers and load equipment suppliers. The PQ problems can be classified as a short duration voltage variation, long duration voltage variation, voltage flicker, voltage notching, transient and harmonic distortion. The short duration voltage variations are referred for the voltage variation in time less than 1 min. The main reasons for short voltage variation are fault conditions, large load energization which requires high starting current, intermittent loose connection in power wiring. The PQ problems called temporary voltage drop (sag), voltage rise (swell) or complete loss of voltage (interruption) occurred depends on the system condition and fault location. The long duration voltage variation is termed for more than 1 min. This may be under voltage and overvoltage. The other PQ problems associated with the power system are voltage unbalance, transient disturbance, voltage flicker, voltage notching and harmonic distortion. The power quality terminologies associated with the distribution level of the power system are below with a short description:

i. Interruption: An interruption may be very short type or sustained interruption. The very short type interruption may be defined when the rms value of voltage decreases to less than 0.1 pu for less than 1 min. The causes of short interruption are power system faults, the equipment failure and control malfunctions. Similarly, the sustained interruption may be defined as the loss of voltage for more than 1 min. This terminology is more specific regarding the absence of voltage for long periods.

ii. Transient: This terminology is defined as the undesirable momentary deviation in terms of impulsive and oscillating nature of the supply voltage and current. The impulsive transient is termed as the sudden, non-fundamental supply frequency change in the steady change of voltage, current or both and is unidirectional (either positive or negative polarity) in nature. Similarly, the oscillating transient is a sudden change, non-fundamental supply frequency change in the steady state but in both polarities.

iii. Voltage sags (dips): The voltage sags (dips) may be defined as the voltage decrease to between 0.1 to 0.9 pu in rms value at rated frequency for 5 cycles to 1 min. The voltage sags are usually from system faults, energization of heavy loads and starting of large motors.

iv. Voltage swells: The voltage swells may be defined as the rise in rms value of voltage in between 1.1 pu to 1.8 pu for the duration of 5 cycles to 1 min. The voltage swell is usually due to the system fault, but are less common than sags. The temporary voltage swell may occur in the unfaulted phases during the single-line-to-ground fault.

v. Under voltage: This terminology may be defined as the decrease in the rms value of voltage to in between 0.8-0.9 pu. for the period of more than 1 min. The under voltage prevails mainly due to the switching events that may be load switching on or capacitor switching off. The over loaded circuits can also cause under voltage phenomenon.

vi. Over voltage: The over voltage may be defined as the increase in the rms voltage at rated frequency to more than 1.1 pu. for more than 1 min. of time period. The over voltage also prevails in the power system due to the switching events, but are opposite to the events to cause undervoltage. The usual switching events that cause over voltage are switching off the large load and energizing of the capacitor bank.

vii. Voltage flicker: The terminology voltage flicker may be defined as the very rapid change in the supply voltage. It is being derived from the voltage fluctuation impact on the lamps that perceived by the human eye as flicker. This is caused by the usage of arc furnace.

viii. Voltage/current imbalance: The voltage/current imbalance may be defined as the inequality in the magnitude of voltage/current of the three phases. There even may not be equal displacement in time of the phases. This is rigorously defined in terms of symmetrical components. The primary source is the single phase load with the three phase distribution circuit. The other source as the blown fuses of one phase in the three phase capacitor bank. The severe imbalance occurs due to the single phasing.

ix. Frequency deviation: This terminology can be defined as a deviation in the fundamental frequency of the supply system. The fundamental frequency is directly related to the rotational speed of generators used to supply the system. The frequency shift and duration depend on the load characteristics and the response of the generation control system during the load changes.

x. Waveform distortion: This waveform distortion can be defined as the steady state deviation from the ideal sinusoidal waveform of rated frequency and characterized by the spectral content of deviation. The chief waveform distortions are dc offset, Harmonics, interharmoinics, notching and noise.

Some of the significant power quality problems are depicted in Figure 1.1. Out of the various PQ problems, harmonic is one of the major issues in the distribution system.

1.2.1 Harmonics

Harmonics can be defined as the integral multiple of the fundamental frequency found in the sinusoidal voltages or currents [4]. When these integral multiple of the fundamental frequency is added with fundamental frequency altogether, a distorted waveform is generated containing harmonics. Figure 1.2 illustrates the effect of 3^{rd} (150 Hz), 5^{th} (250 Hz), 7^{th} (350 Hz), 9^{th} (450 Hz) and 11^{th} (550 Hz) order harmonics of the fundamental waveform producing a resultant distorted waveform [36-40]. The term T HD (Total Harmonic Distortion) is the effective value of the harmonic content in a distorted voltage or current waveform; hence it is defined as the ratio between the RMS values of the

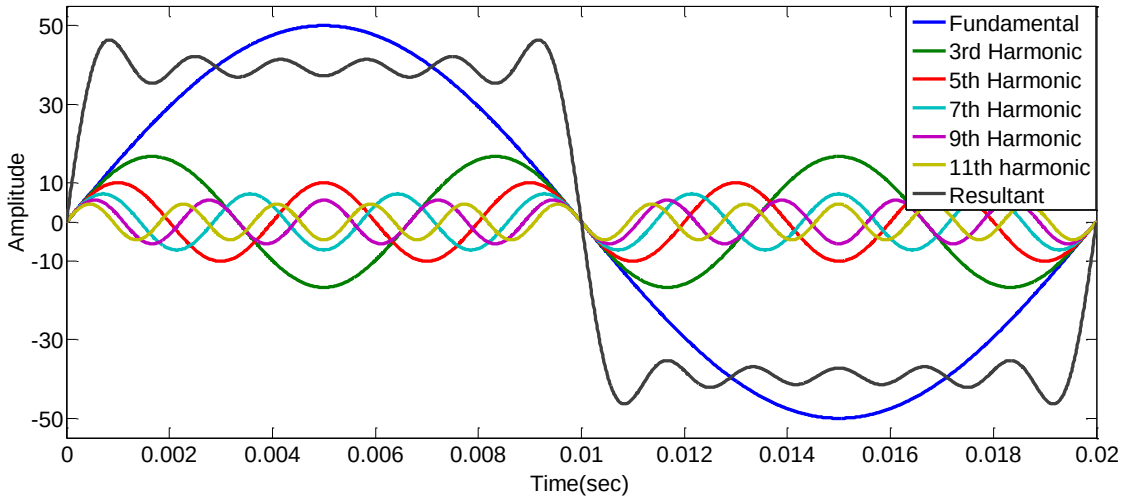


Figure 1.2: Harmonics

harmonic content to the RMS value of the fundamental quantity. It is the potential heating value of the harmonics relative to the fundamental.

The mathematical representation of the voltage and current THD can be depicted in (1.1) and (1.2) respectively as follows:

$$THD_i = \frac{\sqrt{\sum_{n=2}^{\infty} i_n^2}}{i_1} \tag{1.1}$$

where i_1=RMS value of fundamental component of current, i_n= RMS value of the n^{th} order harmonic component of current.

$$THD_v = \frac{\sqrt{\sum_{n=2}^{\infty} v_n^2}}{v_1} \tag{1.2}$$

Where, v_1= RMS value of the fundamental component of voltage, v_n=RMS value of the n^{th} order harmonic component of voltage.

1.2.2 Harmonic Sources

Most of the load on the earlier distribution network were dominated by non-polluting loads and concerned with reactive power only [5]. The developments of modern power electronics equipment, switching devices have completely changed the load characteristics.

The main sources of harmonics are the power electronics devices associated with non-linear characteristics. The switch mode power supply (SMPS), current regulator, frequency converters, dimmers, low power consumption lamps, arc welding machines, adjustable speed drives (ASDs) etc. are some of the vast power electronic devices.

The usage of these loads polluted the modern distribution system. Basically, there are two types of harmonic sources, current source nonlinear load (CSNL) and voltage source nonlinear load (VSNL).

However, the dissertation is concerned about the current harmonics. Although the generators developed nearly perfect sinusoidal voltage, the current passing the system impedance may develop a variety of disturbances to the voltage.

Ultimately, the current harmonics are responsible for the voltage harmonics. The categorization of loads which produces current harmonics are as follows:

i. Harmonics sources from commercial loads: Single phase power supplies, fluorescent lighting, adjustable speed drives for HVAC and elevators.
ii. Harmonic sources from industrial loads: Three phase power converters used in ac and dc drives, arcing devices and saturable devices.
iii. Harmonic sources from domestic loads: Computer systems and other single phase electronic equipment.

1.2.3 Effects of Harmonic Distortion

Harmonic currents produced by the non-linear loads can interact adversely with the power system equipment [6], most notably as follows:

i. Increased losses in the power system
ii. Increased in the rms current resulting high conductor losses, eddy current losses and hysteresis losses; hence overheating of transformers
iii. Overheating of motors
iv. Poor power factor and efficiency
v. Impact on the telecommunications by creating interference with the communication circuits sharing a common path.
vi. Nuisance tripping of protective relays and thermal protection
vii. The harmonic current indicates that the system is in resonance and capacitor bank is involved.
viii. Impact on the accuracy of energy and demand metering
ix. Overloaded and overheated neutral conductors
x. Vibration in rotating machines

1.2.4 Standards of Harmonics

In order to maintain good power quality, many international agencies such as IEEE 519-1992, IEEE 519-2014, IEC 1000-3-2 and IEC 1000-3-4 have released standards and guidelines [7-11]. These guidelines specify the limits of the magnitudes of harmonic currents at various harmonic orders. Both IEC 61000-3-2 and 61000-3-4 define limits for harmonic current emission from equipment drawing input current of upto and including 16 A per phase and larger than 16 A per phase, respectively. These standards are aimed at limiting harmonic emissions from equipment connected to the low-voltage public network so that compliance with the limits ensures that the voltage in the public network satisfies the compatibility limits defined in IEC 61000-2-2. IEEE Standard 519-2014 represents a consensus of guidelines and recommended practices by the utilities and their customers in minimizing and controlling the impact of harmonics generated by non-linear loads for general power system. The harmonic current limits of the general distribution power system with IEEE 519-2014 standard are shown in Table 1.1

Table 1.1: IEEE 519-2014 Standard for harmonic current limits for general distribution systems (120–69,000 V)

Maximum harmonic current (% of I_L)	Individual harmonic order (Odd Harmonics)					
I_{sc}/I_L	<11	11 ≤ n < 17	17 ≤ n < 23	23 ≤ n < 35	35 ≤ n	TDD
< 20*	4.0	2.0	1.5	0.6	0.3	5.0
20-50	7.0	3.5	2.5	1.0	0.5	8.0
50-100	10.5	4.5	4.0	1.5	0.7	12.0
100-1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

where,

I_L: Maximum demand load current at PCC, I_{sc} : Maximum short circuit current at PCC; TDD: Total demand distortion. All power generation equipment are limited to these values of current distortion, regardless of actual $\left(\frac{I_{sc}}{I_L}\right)$.

1.3 Devices for controlling Harmonic Distortion

Harmonics are always present in the power system to some degree. Fundamentally, it is necessary to control only when it creates any problem in the system.

The basis options that can be used to control harmonics are:

i. Add filter either to block the harmonic currents or to siphon the harmonic currents of the system or compensate the harmonic currents produced by the non-linear load.
ii. Modify the frequency response of the system by using inductors, capacitors and filters.

There are various devices available to control the harmonic distortion. The devices may be as simple as capacitor bank or line reactor or as complex as active power filter [12]. This dissertation focused on the harmonic filters that compensate the harmonic distortion produced by the non-linear load so that the IEEE standards can meet. The two general classes of harmonic filters are passive filters and active filters. The former filters are based on the passive elements, and the later filters are based on the power electronics devices.

1.3.1 Passive Power Filter

The inductance, capacitance and resistance are being configured to form passive power filters and tuned to control the harmonics [13-15]. The passive power filters are employed either to shunt the harmonic currents off the line by providing the low impedance path, or to block the flow of harmonic currents in between the parts of the system by tuning the elements to create a resonance at the selected frequency. Usually they are custom designed for a particular frequency, but may be tuned to a frequency between two prevalent harmonics to attenuate both the frequencies. The parameters used to find out the filter inductance, capacitance and resistance are reactive power at nominal voltage, tuning frequencies and quality factor.

The basic types of shunt passive power filters are depicted in Figure 1.3 on per phase basis. The most common type of basic shunt passive filter is the single-tuned filter. This filter is the most economic and is frequently sufficient for the application. The single-tuned filter is connected in parallel with the power system and series tuned to provide a low impedance path to a particular harmonic current. The double tuned passive filters are tuned for dual frequencies. The single tuned and double tuned shunt passive filters come under the band pass filters and are used to filter the lower order harmonics like 5^{th}, 7^{th}, 11^{th}, 13^{th}, etc. The high pass filter constitutes the 1^{st}, 2^{nd}, and 3^{rd} order passive power filters used to filter the

higher order harmonics for a wide range of frequencies. The C-type filter is a special type of high pass filter which can attenuate wide range of steady state, time varying and interharmonics. It also provides reactive power and evades parallel resonance [16-17].

Unlike the shunt passive filters, the series passive filters are connected in series with the load. As can be seen from Figure 1.4a, the inductor and capacitor are connected in parallel and are tuned to high impedance path at a selected high frequency. This high impedance then blocks the harmonic current at tuned frequency only. This series circuit is basically used for blocking single harmonic component and expedient for single phase circuits

Often in practical application, multiple stages of series and parallel passive filters are required to block multiple frequencies. Figure 1.4b depicted the low pass broadband filter which provides the ideal application to block multiple harmonic frequencies. Current with frequency component below the cutoff frequency can pass, however, current component above cut off frequency filtered out.

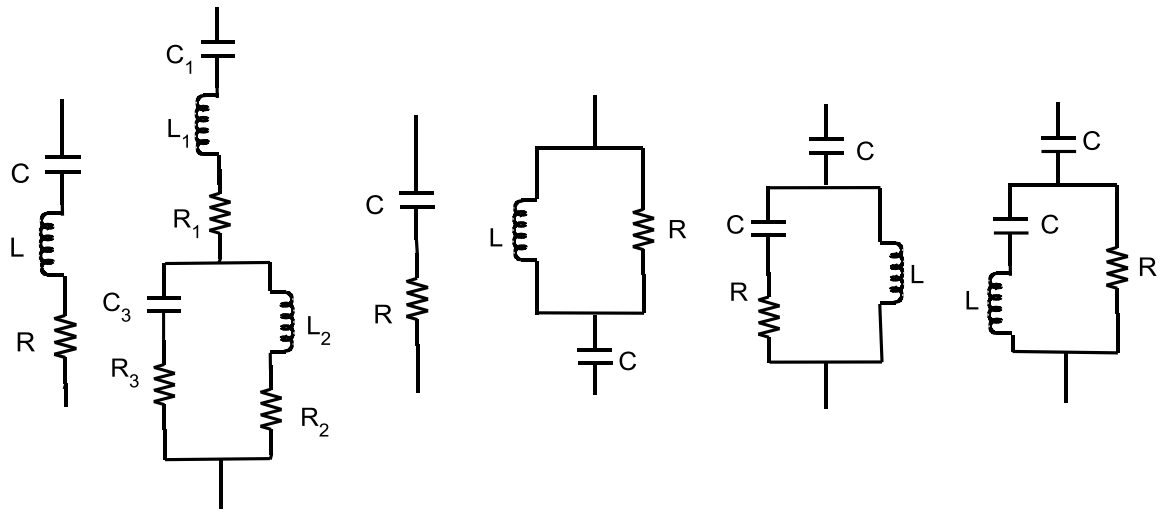


Figure 1.3: Common Shunt passive filter configurations (a) Single tuned (b) Double tuned (c) 1st order high pass filter (d) 2nd order high pass filter (e) 3rd order high pass filter (f) C-type filter

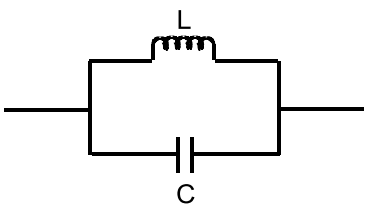


Figure 1.4a: Series passive filter configuration

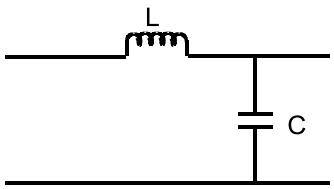


Figure 1.4b: Low pass broadband filter

The passive power filters are commonly used and less expensive as compared to other modes used for harmonic elimination. Again, the passive power filters have an added value of power factor correction for inductive loads. However, they have the disadvantage of potentially interacting adversely with the power system; hence it is necessary to check all possible interaction when being designed.

The drawbacks associated with the passive power filters are the sensitivity to the power system impedance and frequency variation of the utility; high risk of forming a resonance with the system parameters; poor flexibility with the reason of selective harmonic compensation; ineffective for harmonic frequency variation and heavy and bulky.

1.3.2 Active Power Filter

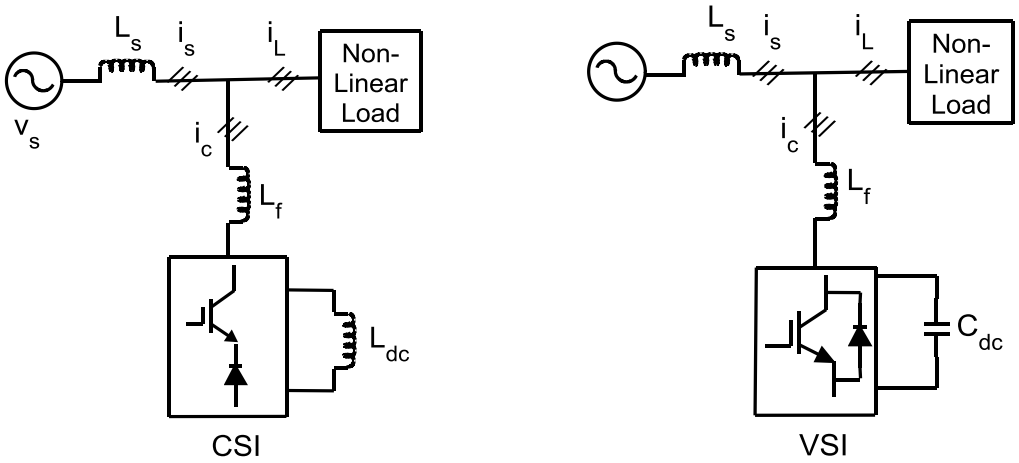
With the advent of solid state devices, varying configuration and control strategies, the active power filters evolved [17]. The active power filters are used to compensate voltage and current harmonics, reactive power and neutral current. APFs are also used to improve voltage unbalance; to regulate the terminal voltage; and to suppress the voltage flicker.

The advantages associated are superior filtering action when the frequency changes randomly; smaller in size; more flexible in application as compared to inductors, capacitors and resistors based passive filters. However the disadvantages associated are the high cost and less efficiency as compared to passive filters [18-27].

The basic power circuits being applicable for active power filters are voltage source inverter (VSI) and current source inverter (CSI). These inverter circuits use the PWM control techniques and Insulated Gate Bipolar transistor (IGBT) or Gate turn-off thyristor (GTO) power devices [28]. The current source and voltage source active power filters are depicted in Figure 1.5 (a) and (b) respectively. The system consisted of the nonlinear load supplied by the source voltage, v_s. The inductance L_s and L_f represents the source and filter impedance respectively. Similarly, the load current, compensating current and source current are represented by i_L, i_c and i_s respectively.

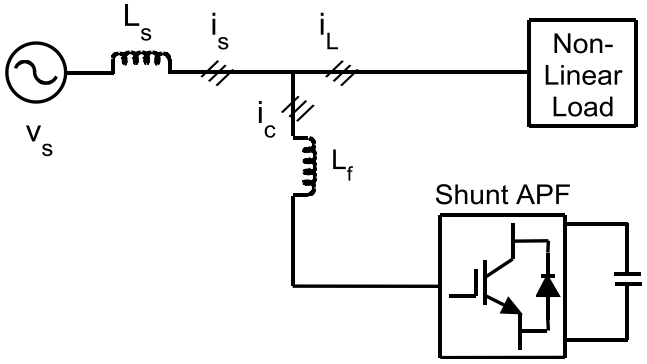
The current source inverter acts as the nonsinusoidal current source to meet the required harmonic current produced by the nonlinear load. A diode is being used with the IGBT for reverse voltage blocking. These CSI based active power filters are to be considered as sufficiently reliable but cannot be used for multilevel application for higher rating performance.

The voltage source inverter based active power filter has self-supporting dc bus provided by the large dc capacitor. VSI based active power filters are more dominant, since it is cheaper, lighter, and expandable to multilevel configurations and to enhance the performance with lower switching frequency.

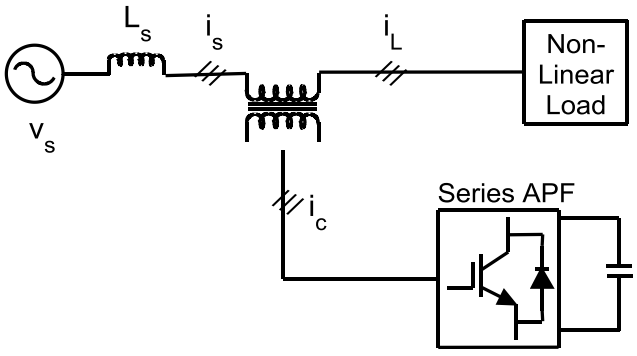


(a) (b)

Figure 1.5: (a) Current source inverter (CSI) based APF (b) Voltage source inverter (VSI) based APF



(a)



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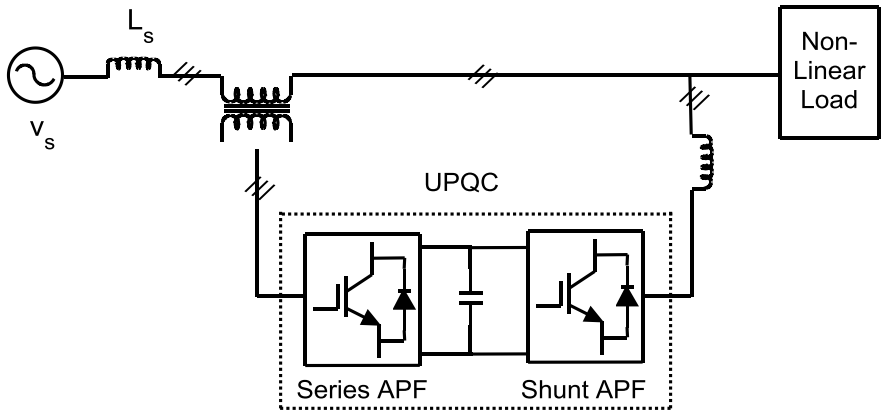
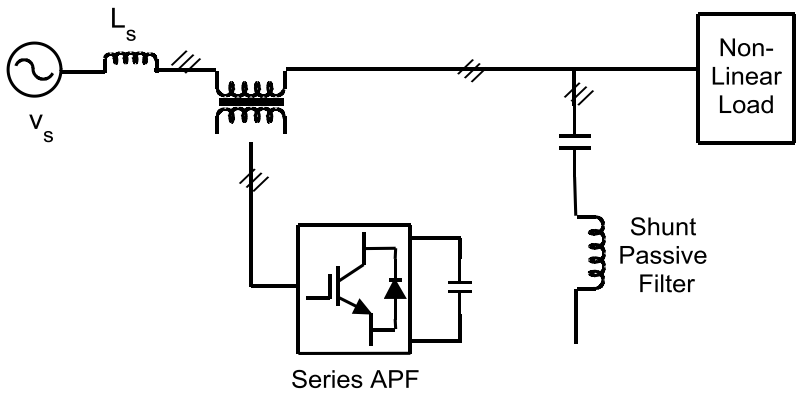


(c)

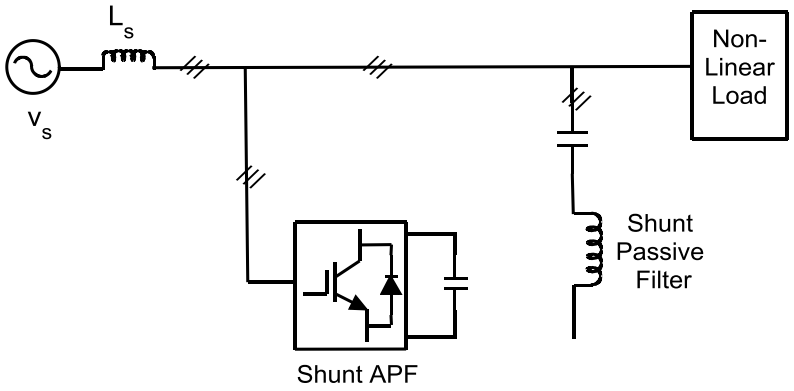
Figure 1.6: (a) Shunt active power filter (b) Series active power filter (c) Unified power quality conditioner (UPQC)

Further, the active power filters can be classified as a shunt or series active power filter and unified power quality conditioner. Figure 1.6 (a) and (b) depicted the shunt and series active power filter respectively. The shunt active power filter compensates the harmonic current produced by the non linear load by injecting equal and opposite harmonic current at the point of connection with a phase shift of 180°. The series active power filter is connected in series before the non linear load through a matching transformer to eliminate voltage harmonics; to regulate and balance the terminal voltage of the line. It has been installed by the utilities in order to damp out the harmonic propagation caused by the resonance produced by the passive filter components and the line impedances [29-31]. Figure 1.6 (c) depicts the unified power quality conditioner (UPQC), is a combination of both series and shunt active power filter. The dc-link storage element, either inductor or capacitor is shared between the current source and voltage source inverter operating as the series and shunt active power filter. UPQC is considered to be an ideal filter as it compensates both current and voltage harmonics and enable to provide clean power to the critical and harmonic prone loads. The others usage is to regulate and balance the terminal voltage and to eliminate the negative sequence current due to unbalancing. The drawbacks associated with are high cost, requirement of complex control and more number of solid state devices. The combination of series filters (either active or passive) and shunt filters (either active or passive) are known as hybrid power filters and can achieve greater benefits in some applications. The various combinations shown in the Figure 1.7 are series active power filter and shunt passive filter, shunt active power filter and shunt passive power filter and series active power filter in addition to shunt passive filter. It becomes popular due to

reduced size of the solid state devices used for the active filter circuit and major passive filters are made of L-C filter used to eliminate the lower order harmonics. These hybrid filters have the capability to filter both the voltage and current harmonics at reasonable cost [32-34].



(a)



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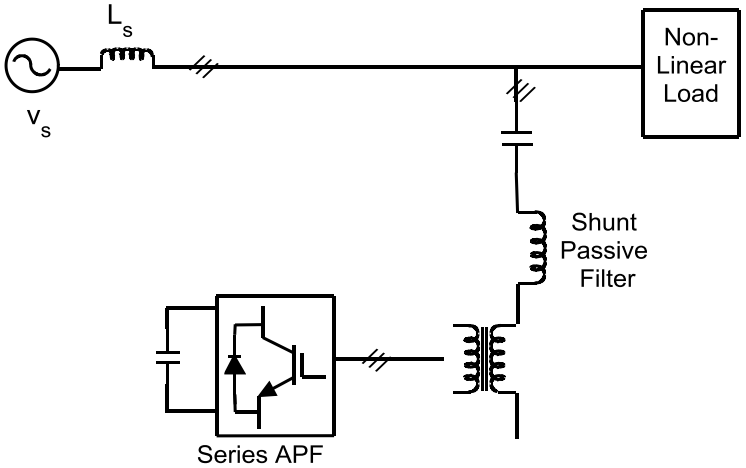


(c)

Figure 1.7: Hybrid filters (a) Series active power filter and shunt passive filter (b) shunt active power filter and shunt passive filter (c) Series active power filter and shunt passive filter

The APFs can also be classified on the basis of compensation and are reactive power compensation, harmonic compensation, balancing of three phase system and multifarious compensation. However, the shunt active power filter can well compensate the multiple power quality issues such as harmonic current, reactive power and unbalanced loading. This dissertation mainly focused on the shunt active power filter as current harmonic is one of the key issues of power quality problems.

1.4 Shunt Active Power Filter configurations

Supply system based shunt active power filter configurations are single phase active power filter, three-phase three-wire and three-phase four-wire active power filter [35]. This dissertation is more concerned about the three-phase four-wire shunt active power filter (3-phase 4-wire APF) due to additional advantage of neutral current compensation.

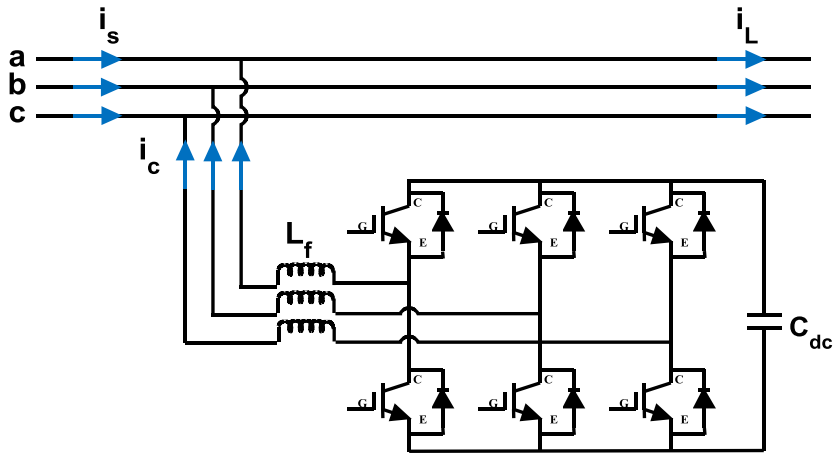


Figure 1.8: Three-phase three-wire shunt active power filter

The single phase shunt active power has the application mainly in the area of electric traction and rolling stock. Also, it is limited to low power application and used for domestic appliances. The three-phase three-wire nonlinear loads such as adjustable speed drives (ASDs) are major applications of solid state converter and hence the three-phase three-wire active power filter became more popular.

The three-phase three-wire shunt active power filter is depicted in Figure 1.8. The power converters that are mostly used in power conditioning in 3- phase system are voltage source converters. The three-phase three-wire active power filters are used mainly to deal with the harmonics produced by the three phase nonlinear load. On the other hand, the three phase four wire system is considered as one of the vulnerable system for various power quality issues [36]. In this three-phase four-wire (3-phase 4-wire) system, single phase supply is

provided to the customer through one of the phases and the neutral conductor. Due to the phase-to-neutral connected load along with three-phase non-linear loads, the four wire three-phase system suffers from load current unbalancing, thus resulting in a net current flowing through the neutral conductor [37].

Again, the unbalancing in the load current produces the presence of negative sequence and zero sequence component of the current. These negative and zero sequence of current may produce excessive heating in the neutral wire, undesirable operation of the electronic equipment, and heating of the electrical machine. This unbalancing is not only the reason for neutral current, the single-phase nonlinear power electronics based equipment even perfectly balanced in 3-phase 4-wire system can also result in significant neutral current. The vector sum of the balanced, nonsinusoidal, three-phase currents does not necessarily provide zero resultant neutral current. In a balanced three-phase system also with non-linear load, the triplen harmonics of the load current component contribute to the neutral current.

However, the development of four wire three phase active power filter has made possible to compensate the multiple power quality issues such as the harmonic, neutral current power and active power compensation at a certain level [38].

A variety of 3-phase 4-wire shunt active power filter topologies have been developed with its unique advantages and disadvantages such as 3-phase 4-wire capacitor midpoint APF topology (2C APF), 3- phase four- leg APF topology (4L APF), 3-phase 4-wire single capacitor 3 H-bridge/Full-bridge APF topology (1-C 3 H-bridge APF) and 3-phase 4-wire H-bridge/Full-bridge APF topology. All these topologies may be good choice for low to medium power application, due to the fewer number of switching devices. However, with the increase in demand for high power application, the researchers are heading towards the multilevel topologies [39-47].

1.4.1 Three-phase four-wire capacitor mid-point APF (2C APF) topology

The 3-phase 4-wire capacitor mid-point active power filter (2C APF) is more efficient and economical active power filters for low power applications. It utilizes the voltage source inverter (VSI) having only six switching devices as depicted in Figure 1.9. The distinguishing feature of this topology is the division of the dc-link bus capacitor into two capacitors. The midpoint of the capacitors is used for the neutral current return path to flow and therefore the whole neutral current flow through the two capacitors. In this

topology, it is very important to maintain the two dc-link voltages same and it is really a difficult part to perform in its control strategy. Hence two voltage control loops are used to maintain the reference dc-link voltage across the voltage source inverter. The difference between the two dc-link voltages may generate the circulating current, affecting the overall performance of compensation. Additionally, there is no direct control on the neural load current compensation, as it gets compensated by the algebraic difference of the currents injected by the phases [31].

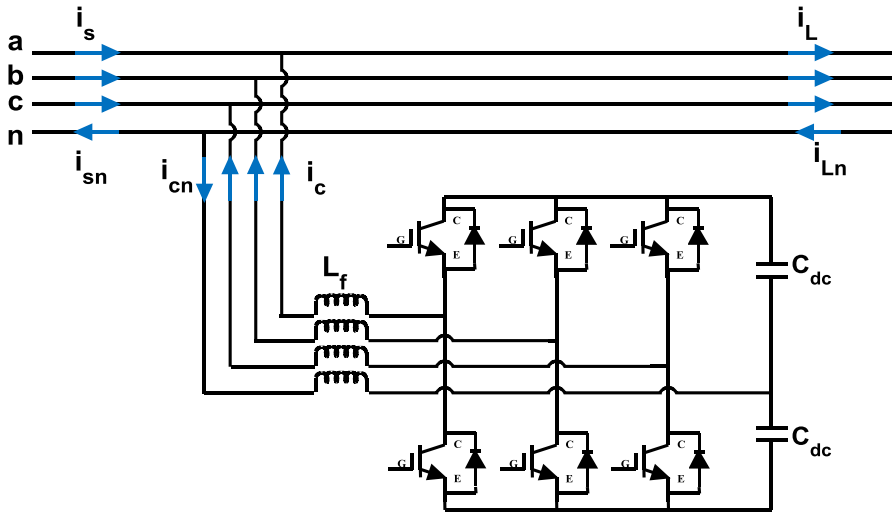


Figure 1.9: Three-phase four-wire capacitor midpoint shunt active power filter

1.4.2 Three-phase four-leg APF (4L APF) topology

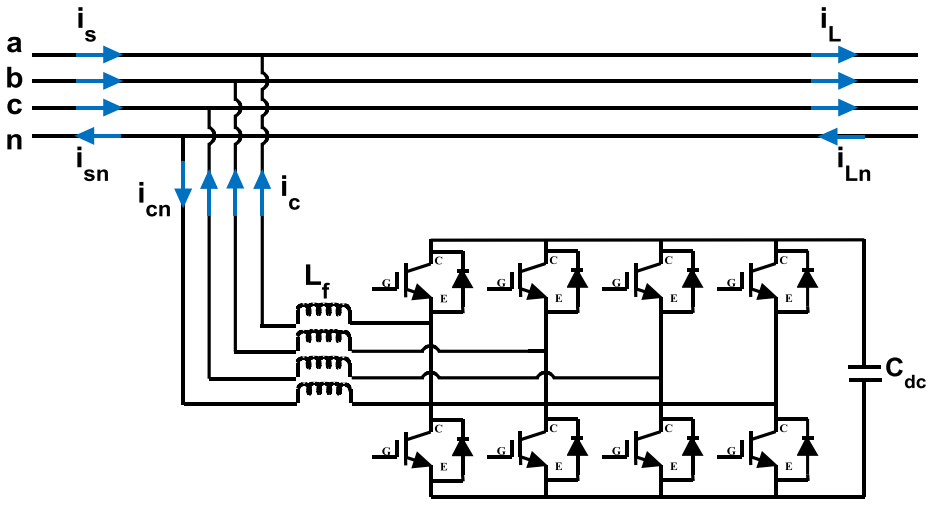


Figure 1.10: Three-phase four-leg shunt active power filter

The 3-phase 4-leg shunt active power filter is illustrated in Figure 1.10. It consists of an additional leg, which is solely added for the load neutral current compensation. This

topology has direct control over the neutral current and hence assured of better neutral current compensation as compared to 2C topology [35,39].

It consists of only one dc-link capacitor and hence easier to maintain the reference dc-link voltage across the four-leg voltage source inverter. Additionally, the sensing of load neutral current through the neutral current sensor is required for the generation of neutral compensation current. The reference for neutral current on the source side, which necessarily ought to be zero. However, the reference neutral compensation current is being made by the addition of the individual phase's reference compensating currents. The disadvantages associated with this topology are increased cost due to the additional two switches and their corresponding control circuitries. This topology is also used for low power application.

1.4.3 1-C, 3 H-bridge/Full-bridge APF topology

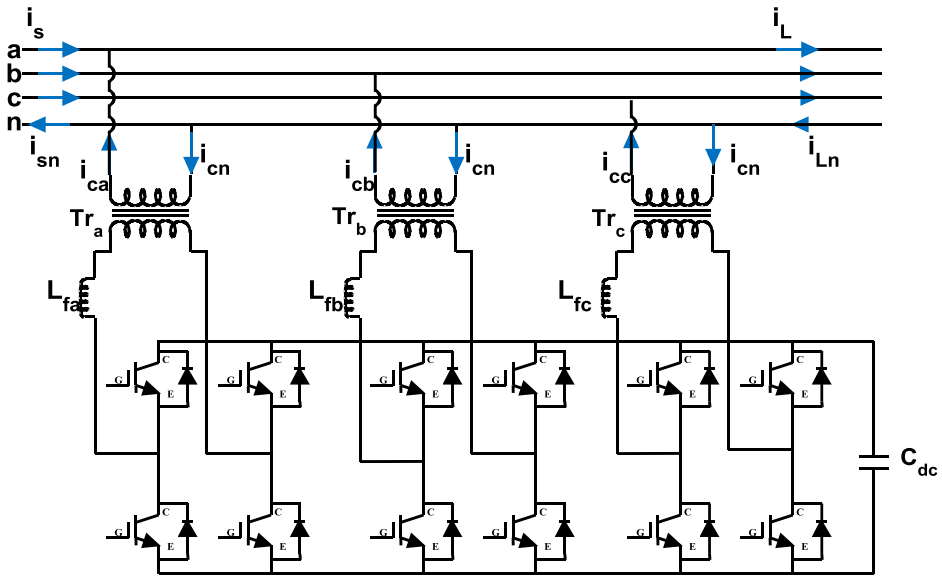


Figure 1.11: Three-phase four-wire 3 H-bridge/ Full-bridge active power filter with single dc- link capacitor

Three phase four wire 3 H-bridge/Full-bridge active power filter having single dc-link capacitor, 1C 3FB APF is illustrated in Figure 1.11. It consists of three numbers of single phase H-bridge/Full-bridge inverter with single dc-link capacitor and is connected to the system through the corresponding single phase isolation transformers [39-40]. The main advantage associated with this topology is the dc-link reference voltage reduction by $\sqrt{3}$ times as compared to 2C and 4-leg topology. Again, as it consists of only one dc-link capacitance, hence the corresponding control strategy is simple. The cost due to more

number of switching devices used by this topology can be compensated by the lower rating of the switching devices as compared to 2C and 4-leg topology. In the 1-C, 3 FB APF topology, the load neutral current is being compensated indirectly same as 2C topology.

1.4.4 Three-phase four-wire H-bridge/Full-bridge APF topology

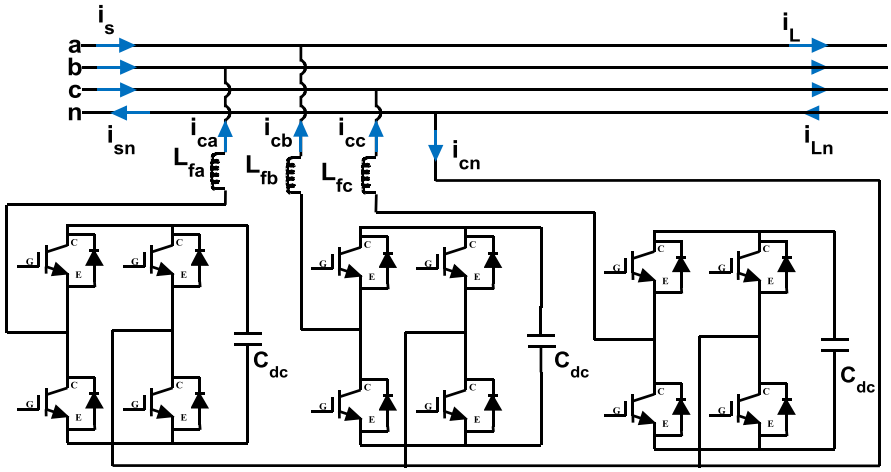


Figure 1.12: Three-phase four-wire H-bridge/Full-bridge active power filter

The 3-phase 4-wire H-bridge/Full-bridge active power filter is presented in Figure 1.12; consists of three single-phase full bridge voltage source inverter. This topology consists of modular structure of the H-bridge and hence the manufacturing process is simple, quick and cheap. The H-bridge voltage source converter of the corresponding phases can connect directly to the 3-phase 4-wire distribution lines without the requirement of isolation transformer [39, 47]. Here also the dc-link reference voltage is being decreased by $\sqrt{3}$ times, as the voltage across the H-bridge inverter is single phase voltage and not the three phase voltage like 2C and 4 leg topology.

As can be seen from the Figure 1.12, there is no direct control over the neutral current like 2C and 1C, 3 FB APF topologies. Though both 1C, 3 FB APF and 3-phase 4-wire H-bridge/Full-bridge APF topology consists of twelve numbers of switching devices, still 3-phase 4-wire H-bridge active power filter has less cost, as it does not necessitate any isolation transformer.

1.5 Multilevel Inverter based Shunt Active Power Filter

The multilevel was first surfaced with the introduction of 3-level neutral-point clamped inverter that generated a three-level quasi-square waveform. Following this development, various multilevel topologies came in the research field.

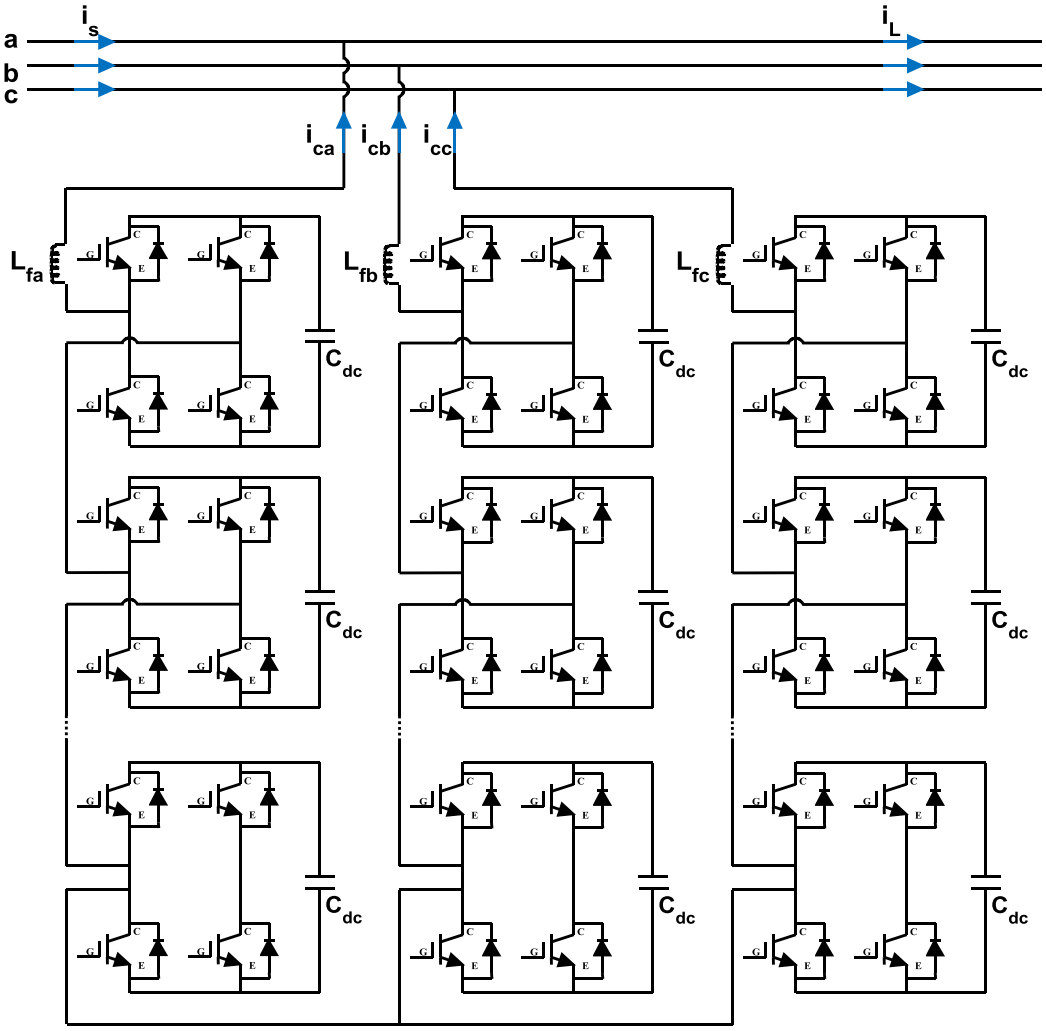


Figure 1.13: Multilevel cascaded H-bridge/Full-bridge active power filter

The multilevel inverters (MLI) based APF are being mainly devised for high power application, owing to higher voltage operating ability, lower dv/dt and better sinusoidal output [48-50]. One of the major disadvantages associated with MLI is the voltage unbalance problems encountered in higher level converters. The basic types of MLIs classified under the topology and principle of generation of multilevel output voltage are neutral point clamped inverter, flying capacitor inverter and Cascaded H-bridge inverter. Out of various multilevel topologies, the cascaded H-bridge/Full-bridge is particularly used for very high power application as shown in Figure 1.13 [51-57]. The other advantages associated with this topology as compared to neutral point clamped and flying capacitor inverter are: the number of possible output voltages is more than the twice of the number of the dc sources; the component requirement is less and modularized H-bridge makes the topology cheap and manufacturing process quick [55]. The various PWM schemes used for this cascaded H-bridge are discussed in [58-60].

1.6 Shoot-through Phenomenon

The power transistor voltage source inverter phase leg is being analyzed to determine the magnitude of current impulse that causes catastrophic effects, shown in Figure 1.14. This shoot-through phenomenon with extensively high current, takes place during the time when the switches are being switched from the same leg of the bridge inverter circuit [61-63]. Usually, this catastrophic phenomenon results from the unequal switching time i.e. turn-on and turn-off time of the transistor.

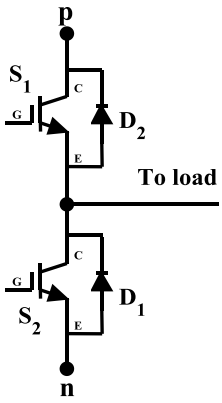


Figure 1.14: Generic phase leg of voltage source inverter

When the transistor switches of the same leg are being switched, a short circuit current may flow by the rapid turn on of one transistor and the delayed turn off of the other transistor, connected in series. This particular current of concern is called as shoot-through phenomenon. The switching time differs mainly due to the charge stored within the base region of the transistors during the conduction period. These stored charges must be removed from the transistor before the transistor ceases conduction. The inequality in the switching time varies even for a given type transistor according to the production and fabrication variables. The time difference may vary from a few tenths of microsecond for the high speed transistor switches to the several microseconds for medium and slower speed transistor switches.

The unequal switching time characteristics of the transistors is troublesome in circuit applications which results in excessively very high short circuit current spikes through the transistors. This shoot-through current may follow for nanoseconds, but frequent occurrence of shoot-through results in the unreliable operation of the inverters with a high current stress in the conventional inverter switches. Shoot-through phenomenon has few distinct disadvantages like; it introduces typical ringing, increases temperature rise in power switches, causes higher Electromagnetic Interference (EMI) and reduces the

reliability and efficiency of the circuit. Various techniques were developed to circumvent the shoot-through phenomenon; to improve the reliability and efficiency of the conventional bridge inverter circuit and are discussed in the later part.

1.6.1 Dead time

Dead time introduction in the switching scheme is one of the ways to eliminate the shoot-through phenomenon in the voltage source inverter. Dead time is defined as the small interval during which both the upper and lower switches in a phase leg are off, is introduced in the standard switching pulse as depicted in Figure 1.15. However, the blanking time can cause output voltage distortion and fundamental voltage loss, especially, when the output voltage is low. In practice, the dead time varies with the gate drive path propagation delay, device characteristics and output current, as well as temperature, which makes the compensation less effective, especially at low output current, low frequency and zero current crossing. Several switching strategies have been proposed to minimize the dead time effect. A dead- time minimization algorithm was also discussed in [66] to improve the inverter output performance and presented an IGBT gate driver circuit to eliminate the dead-time effect in VSIs. [67] proposed a phase leg configuration topology which is not appropriate for high power inverters since the upper device gate turn-off voltage reversely clamped by a diode turn on voltage.

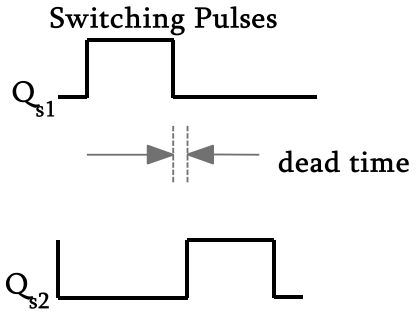
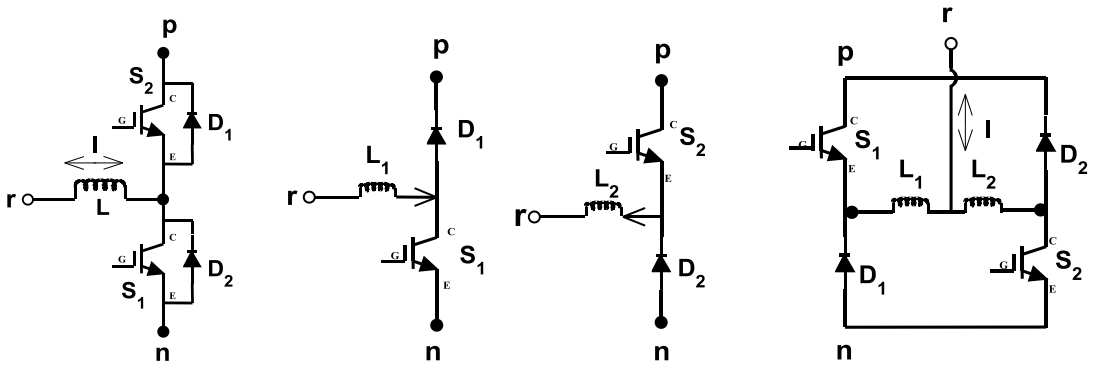


Figure 1.15: Dead time in the normal gate switching signal

High-power inverters usually need longer dead-time than those low-power counterparts. Also, due to complicated structures and severe parasitic parameter variations, in practice, the dead-time for high-power inverters necessitates specific adjustment and/or compensation, and this process is time consuming. For general applications, inevitably eliminating dead-time by gate drive technology is a desired and complete solution. Dead time introduction has also some limitation, cannot go for too long or too short. Too short dead time can cause shoot-through and it again gives complexity. The inclusion of the dead

time state creates an innate nonlinearity in the output voltage and current and this behavior does not give good harmonic compensation. However, the dead time introduction cannot give full assurance about the elimination of shoot-through phenomenon and hence the researchers thought of different circuit topologies.

1.6.2 Interleaved Buck Converter and Active Power Filter



(a) (b) (c)

Figure 1.16: (a) Conventional inverter phase (b) Equivalent circuit cells of conventional inverter phase limb (c) Interleaved buck bridge cell

By the combination of the equivalent circuit cells as shown in Figure 1.16, a circuit is shaped that is known as an interleaved buck (IB) bridge cell, Figure 1.16c in which no shoot-through failure occurs with any dead time effect. This IB bridge cell works on the principle of parallel combinational of two buck converters [1, 68]. So the interrogation must not arise that dead time is not required for either a high side power switch cell or low side power switch cell because both switch cells are aligned with a controllable switch in series with an uncontrollable diode. The disadvantage is that, it needs more inductors as compared to conventional inverter circuits. The advantage of this interleaved buck converter is the requirement of discrete diodes whereas the conventional inverter has the diodes assimilated with the switches. In addition, the reliability of the inverter is greatly improved because the shoot-through phenomenon is eliminated and hence the lifetime of the inverter circuit is prolonged [69-72]. The basic classification of the interleaved buck converter is classified as a half-bridge interleaved buck inverter (HB-IB inverter) and full-bridge interleaved buck inverter (FB-IB inverter) like conventional inverter. Again, the input voltage utilization rate of full bridge interleaved buck inverter is twice of the half bridge interleaved buck inverter. Hence less voltage stress across the full bridge interleaved buck inverter power switches [73]. Hereafter, several researches have been carried out on

interleaved buck (IB) switch cell based active power filter and suits to be used in the application with the requirement of high reliability and harmonic compensation [74-75].

1.7 Control Schemes of APF

In recent years, various control strategies have been proposed like instantaneous active and reactive power (p-q) theory, unity power factor (UPF) scheme, perfect harmonic cancellation (PHC), instantaneous active and reactive current component (i_d-i_q) method, generalized integral, Delay less filtering using artificial neural network (ANN), adaptive linear neuron (ADALINE), wavelet transform, fast Fourier transform (FFT), recursive discrete Fourier transform (RDFT) theory with the development of active power filter [76-95]. Mainly the control schemes can be categorized into time domain and frequency domain. The time domain is preferred here due to its various advantages like the fast response during the fast change in the power system, easy implementation with less memory equipment and less computational burden unlike frequency domain control schemes. Along with, the other disadvantages associated with it in the increased number of calculations for increased order of harmonics to be eliminated and resulting in longer time response. The ANN and ADALINE have also some shortcomings. The number of ADALINE required is equal to the number of harmonic orders considered in the load current. Hence slower down the convergence. The input vector $X = [\cos \omega t\,, \sin \omega t \ldots \cos n\omega t\,, \sin n\omega t]^T$ generation is difficult and also a tedious process. However, from the various control schemes, the p-q and i_d-i_q control strategies have been used in this dissertation for the reference current generation.

i. p-q control strategy

A complete paper of p-q control strategy with experimental verifications published in 1984 by Akagi. et. al. The p-q control strategy has gained more popularity to become a viable solution for active power filter control scheme in time domain. This control strategy offers a precise reference compensating current and allows a clear difference between the active and reactive power components. This topology is applicable to both the three-phase system with or without the neutral conductor and valid for steady as well as dynamic state [80-84]. On contrary to other control scheme, this scheme deal with the three-phase system at a time as a unite system and not the three-phase system treating three single phase circuits. This scheme is based on the Clarke's transformation, which transform the voltage and current component from abc frame to $\alpha\beta 0$ frame. However, this topology is being criticized

during the unbalanced and non-sinusoidal voltage source condition. With the non-ideal voltage source conditions, the harmonic content in calculated active and reactive power gets increased due to multiplication of distorted load current and distorted/unbalanced supply voltage.

ii. i_d-i_q control strategy

In 2000, Soares. et. al. published a paper on the i_d-i_q control strategy, reporting that it is better than the p-q control strategy. It is also named by synchronous reference frame (SRF) method [85-91]. With this, the load current harmonics can be mitigated in all kinds of supply system such as sinusoidal, unbalanced sinusoidal and non-sinusoidal. Here the dq reference frame components are calculated from the $\alpha\beta$.

1.7.1 Conventional PI controller for dc-link voltage regulation

In the steady state condition, the supplied real power is equal to the demand of the load plus the losses due to inductors and switching devices of the active power filter. Thus the dc-link voltage remains constant. But during the load variation, the difference of real power between the source and load; and in this situation, the charging/discharging of capacitor required to maintain the dc-link voltage reference. If the dc-link voltage is recovered to attain the reference voltage, the real power supplied by the source again becomes equal to the real power required by the load. Active power filter control strategy uses a PI controller for minimizing the undesirable losses occurring inside the active power filter itself [92-98]. For maintaining a constant dc-link capacitor voltage, the flow of active power in the filter needs to be controlled. If the active power flowing into the filter is controlled and it is equal to the losses in the filter, the dc-link voltage may be maintained at the desired value.

1.7.2 Implementation of Fuzzy logic controller for dc-link voltage regulation

Only just, fuzzy logic controllers have acknowledged a great deal of attention in regards to their application to active power filters (APFs) control strategy. The advantages of fuzzy logic controllers over PI controllers are that they do not necessitate any precise linear mathematical models, can handle non-linearity with inaccurate inputs, and are more robust. Out of Sugeno and Mamdani type of fuzzy controllers, the Mamdani type controller gives a better result for the control of an active power filter (APF), but it has the drawback of a large number of fuzzy sets and rules [99-161].

1.8 Research Motivations and Objectives

1.8.1 Motivations

i. **Harmonic Mitigation by filters**

The problems of harmonics are most serious with the proliferation of power electronic equipment ensuing in harmful consequences. Both passive and active filters can be used for compensation of the harmonics, but due to smaller in size, superior filtering performance, and more flexible in application, active power filters are superior to passive harmonic filters.

ii. **Optimum converter for active power filter**

Out of voltage and current source inverter, voltage source inverter is more in application because it is more efficient, lower in cost, and smaller in physical size (particularly in terms of comparison between the dc capacitor and dc inductor).

iii. Reliability of voltage source inverter used in the active power filter

The shoot-through phenomenon is one of the most dangerous failure mode encountered in the conventional inverter circuit which decreases the reliability of the APF. To eliminate shoot-through, dead time introduction is one of the methods, but still it has some drawbacks. The interleaved buck converter has been taken for the elimination of shoot-through current and hence decreasing power loss by increasing the reliability of the APF.

iv. Compensation of neutral current during unbalanced load condition

The unbalanced source current can be due to many reasons, such as unequal distribution of single phase load, unbalanced three phase loads, etc. At the same time, an excessive zero sequence current can possibly lead to damage the neutral conductor and hence the four-wire active power filters have been attempted.

v. Optimal control strategies

Most of the control strategies found in the literature are incompetent during the non-ideal supply condition. The p-q control strategy yields acceptable THDs results only under sinusoidal source voltage condition. The i_d-i_q is chosen because it is frequency

independent and hence many synchronization problems evaded. This control strategy works excellent in sinusoidal, unbalanced sinusoidal as well as in nonsinusoidal voltage source condition.

vi. Optimized switching frequency

From various research papers, it can be concluded that, the conventional hysteresis band current controller does not provide optimized switching frequency. For nearly constant witching frequency, adaptive hysteresis band current controller (AHBCC) can be utilized resulting in reduced switching losses.

vii. DC side controller

The researchers have been working on a traditional PI controller for controlling the dc-link voltage of inverter as it is the key aspect of the harmonic compensation performance of the APFs. A lot of deficiencies have been observed in traditional PI controller and they are; the requirement of precise linear mathematical models, which are difficult to attain, and fails to react under parameter variations, nonlinearity, load disturbance, etc. The PI controller drawbacks can be normalized by using the fuzzy logic controller (FLC) or Type-1 fuzzy logic controller (T1FLC). Again, the Type-2 fuzzy logic controller (T2FLC) sets and systems generalize the Type-1 fuzzy logic controller, so that more uncertainty can be handled. Additionally, the different membership functions has the impact on dc-link voltage controller and source current THD. So analysis has been done on this part also.

viii. Various topologies of 3-phase 4-wire IB APFs for low to medium power application

As various conventional APFs reported in the literature, but suffers from the shoot-through phenomenon. Hence various topologies of interleaved buck active power filter (IB APFs) needs to be modelled with high reliability for low and medium power application.

ix. IB APF for high power application

Among various multilevel voltage source inverters, the neutral point clamped inverter; flying capacitor and cascaded H-bridge are commonly used and commercially available. Out of which, the cascaded H-bridge or full-bridge has been considered here. The benefits and limitations of cascaded inverter are as follows:

i. With flexible, modular design, transformerless connection, extended voltage and power output, less maintenance and higher fault tolerance, the cascaded inverters are good candidates for high power application.

ii. The cascaded types of inverter are capable of reaching higher output voltage level by using commercially standard lower voltage devices and components, and it features the modular design concept which makes the maintenance less burdensome.

iii. However, because of cascaded inverters are based on a series connection of several single voltage source inverters (VSI) with two active devices in one leg, it still faces shoot-through problems, the most dominating failures of VSI. So, cascaded FB-IB APF is being come to the focus of research.

Several PWM techniques have been studied. Cascaded full-bridge inverters are usually being controlled by the multi carrier PWM, and are phase shifted PWM (PS-PWM) and level shifted (LS-PWM), which includes Phase Disposition (PD-PWM), Phase Opposition Disposition (POD-PWM), and Alternate Phase Opposition Disposition (APOD-PWM).

x. Validation of the proposed topologies, control strategies and controllers

The power conditioning devices have become very much essential to test and validate the engineering design process. Hence, to find out the effectiveness of various topologies using different control schemes in real time, the MATLAB/Simulink designed model needs to validate by the real time simulator. Here OPAL-RT real time digital simulator has been used for result validation.

1.8.2 Objectives

i. To overcome “shoot-through” phenomenon and “dead time” in active power filter by using interleaved buck (IB) inverter.

ii. To model interleaved buck active power filter (2C IB APF) for 3-phase 4-wire power application system using p-q and i_d-i_q control strategy.

iii. Comparison of conventional hysteresis and adaptive hysteresis band current controller based 3-phase 4-wire IB APF (2C IB APF) in terms of switching frequency and source current THD.

iv. Modelling and Real-time implementation (OPAL-RT) of 3-phase 4-wire IB-APF (2C IB APF) using Type-1 Fuzzy logic controller (T1FLC) for different membership functions viz. Triangular, Trapezoidal and Gaussian.

v. Modelling and real time implementation (OPAL-RT) of 3-phase 4-wire IB APF (2C IB APF) using Type-2 Fuzzy logic controller (T2FLC) for different membership functions viz. Triangular, Trapezoidal and Gaussian.

vi. Comparison of IB APFs performance employing the PI controller, Type-1 Fuzzy logic controller (T1FLC) and Type-2 Fuzzy logic controller (T2FLC)

vii. Performance analysis of various topologies of 3-phase 4-wire interleaved buck active power filter (IB APF) viz. (a) Split capacitor (2C) IB APF topology, (b) Four leg (4L) IB APF topology, (c) 3-full bridge IB APF topology with single dc-link capacitor (1C 3FB IB APF) and (d) Full bridge interleaved buck active power filter (FB IB APF) topology for low to medium power application followed by the Real time implementation (OPAL-RT).

viii. Comparison of IB APF topologies based on the switch device power rating.

ix. Performance analysis of cascaded full-bridge IB APF topology followed by Real-time implementation (OPAL-RT).

1.9 Dissertation Layout

After the introduction presented in this chapter, chapter 2 deals with the performance analysis of 3-phase 4-wire split capacitor interleaved buck active power filter (2C IB APF) with different control schemes. It can also be known as 3-phase 4-wire half-bridge interleaved buck active power filter (HB IB APF). The p-q and i_d-i_q control scheme is followed by the dc-link voltage regulation by PI controller. Finally a comparison has been done between the two control strategies, by performing in a MATLAB/Simulink environment. These control strategies used for generation of reference compensating current are evaluated under different voltage source condition, and finally the performance of the control strategies has been assessed in terms of the harmonic mitigation percentage, dc-link voltage regulation, neutral current for unbalanced load current in three-phase four wire system. Again, adaptive hysteresis band current controller has been implemented to get the nearly constant switching frequency and good harmonic compensation. To validate

the proposed interleaved buck active power filter with different control schemes, the presented research is implemented by OPAL-RT real time simulator.

Chapter 3 deals with the Type-1 and Type-2 fuzzy logic controller based adaptive hysteresis i_d-i_q control strategy for further improvement in performance of conventional methods. Type-2 FLC is an extended concept of Type-1 fuzzy logic controller and they are useful where it is difficult to find the exact membership function for a fuzzy set. Hence, with this Type-2 FLC approach, the compensation capability became extremely good. Different fuzzy membership functions (triangular, trapezoidal and Gaussian) have considered for finding the reference compensating current and are compared by evaluating their performance under different voltage source condition for unbalanced load current. Detailed simulation and OPAL-RT real time simulator results are presented for validation of the proposed research.

Chapter 4 deals with the different topologies of 3-phase 4-wire interleaved buck active filter. The different 3-phase 4-wire IB APF is named as split capacitor interleaved buck active power filter (2C IB APF), four-leg interleaved buck active power filter (4L IB APF), 3 full-bridge interleaved buck active filter with single capacitor (1C, 3 FB IB APF) and full-bridge interleaved buck active power filter (FB IB APF). These all presented topologies have their own advantages. Basically 2C IB APF and 4L IB APF can be used for low power application and 1C, 3 full-bridge IB APF and 3-phase 4-wire full-bridge IB-APF can be used for low to medium power application. Again, the dc-link capacitor requirement by each topology is different. Adaptive hysteresis i_d-i_q control strategy has been used and tested for both the PI and Type-1 fuzzy logic controller with different voltage source conditions with unbalanced load. The switch device power rating (SDP) of IB APFs has been evaluated to have a comparison between the low and medium power IB APF topologies. MATLAB/SIULINK and OPAL RT real-time implementation have been applied to evaluate and validate the performance in terms of harmonic mitigation, component requirements and areas of application.

Chapter 5 deals with the cascaded full-bridge-bridge multilevel interleaved buck active power filter. Higher order multilevel inverters are avoided in the three-phase four-wire application. Due to the various advantages of multilevel cascaded full-bridge active power filter, here multilevel cascaded full-bridge IB APF has been proposed and followed by

multicarrier modulation techniques and i_d-i_q control strategy for generation of reference compensating current.

Chapter 6 concludes the dissertation major distribution along with the future work. Following this, the conclusions drawn from this dissertation are enumerated.

Chapter 2

Performance Analysis of Interleaved Buck Shunt Active Power Filter with p-q and i_d-i_q control schemes

2.1 Introduction

This chapter comes to the modelling of 3-phase 4-wire active power filter (APF) based on interleaved buck (IB) dc-to-ac converter with control schemes as p-q and i_d-i_q. This interleaved buck (IB) dc-to-ac converter is an augmented version of the conventional phase leg configuration and is innately immune to "shoot-through" phenomenon, with the elimination of special protection features required in conventional inverter circuits. A comparison has been made between the compensation capabilities of the 3-phase IB-APF with the PI based p-q and i_d-i_q control strategy under different supply voltage conditions. The performance of the control strategies has been evaluated in terms of harmonic mitigation and dc-link voltage regulation. Extensive simulations have been carried out in the MATLAB/Simulink environment and also implemented Real-Time Digital Simulator Hardware (OPAL-RT Hardware) for verification. This chapter is being labelled as: Section 2.2 represents the working principle of the half-bridge interleaved buck converter and interleaved buck converter based active power filter. In Section 2.3, the control schemes applied to the 3-phase 4-wire interleaved buck active power filter, i.e. p-q and i_d-i_q have been enumerated in detail. Section 2.4 describes the PI controller based dc-link voltage regulation scheme. Section 2.5 refers to conventional and adaptive hysteresis band current controller being used for the generation of gating pulse for the inverter power

switches. Section 2.6 provides the information about the tools used for the analysis of the various models of this dissertation. Section 2.7 depicts the 3-phase 4-wire IB APF system performance using p-q and i_d-i_q control strategy. The results presented for control strategies are being designed with dc side PI controller and hysteresis PWM for generating the gating pulse. In Section 2.8, there is a detailed summarization.

2.2 Half Bridge Interleaved Buck Converter based Active Power Filter

An active power filter is implemented to draw /supply the compensating current in order to make the source current sinusoidal, which flows from/to the load by removing the higher order harmonics than the fundamental with the injection of same but opposite in phase harmonic components [35]. Here the shunt active power filter acts as a current source injecting the harmonic components generated by the load with a phase shift of 180^{o}. This principle is valid for all non-linear load which generates harmonic components.

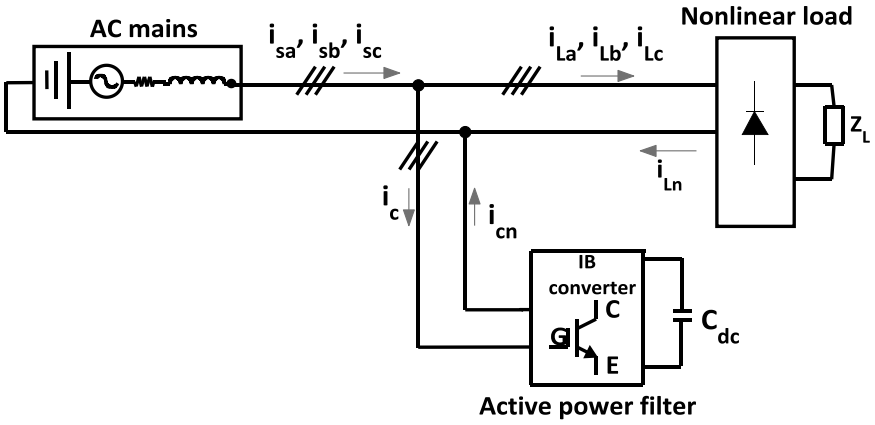


Figure 2.1: Basic configuration of Shunt IB APF system

The shunt active power filter is intended to perform the harmonic compensation in the power system to assure sinusoidal and balanced current that flows through the source to the load. The basic principle of shunt active power filter is figured out in Figure 2.1, i.e. to inject opposite phase harmonic current equal to the amount of harmonics present in the current flowing from the source to the load.

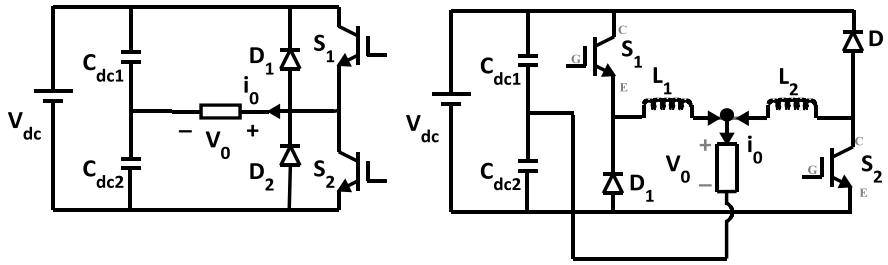
The equation that can be defined the active power filter harmonic compensation in given by (2.1)

$$i_{s\,abc}(t) - i_{L\,abc}(t) = i_{c\,abc}(t) \tag{2.1}$$

Where $i_{s\,abc}(t)$, $i_{L\,abc}(t)$ and $i_{c\,abc}(t)$ represents the phase source current, load current and compensating current for a,b, and c phase respectively.

Here, 3-phase 4-wire active power filter has been developed using the interleaved buck inverter. The most common 3-phase 4-wire APF topology has been worked in this chapter i.e. the 2C IB APF topology. This proposed topology eliminated the shoot-through phenomenon with good harmonic and neutral current compensation. The interleaved buck converter and the proposed 3-phase 4-wire interleaved buck active power filter has been discussed elaborately in the next subsections respectively.

2.2.1 Half-Bridge Interleaved Buck Converter



(a) (b)

Figure 2.2: (a) Conventional half-bridge converter (b) Half bridge interleaved buck converter

Figure 2.2 shows the single phase conventional and interleaved buck converter. Both the topologies may be categorized as half bridge type. The phase leg including the pair of switching device of the conventional inverter, Figure 2.2a are alternately operated to connect the junction between the devices to the voltage source, thereby producing an alternating output at the load. These power switches of the conventional inverter are not the ideal devices and hence do not have an equal switching (turn on and turn off) characteristic. This deviation in switching characteristic time is chiefly ascribable to the "shoot-through" phenomenon in the course of switching conduction.

As the branch switches operated alternately, a short circuit across the power source is created between the rapid turn on time of one transistor and the delayed turn off time of the other.

The short circuit current may reach an exceptionally high level and greatly exceeds the safe maximum current ratings. This may lead to cataclysmic transistor failure, which decreases the reliability of the conventional inverter circuit. In another aspect, the conventional

inverter has the diodes assimilated with the switches. The power loss is high due to the poor characteristics of these assimilated diodes.

Figure 2.2b shows the single phase half-bridge interleaved buck converter and is formed by the decomposition of the generic phase leg of the conventional inverter circuit into the basic switching leg configured with a controllable switch in series with a diode and with coupling inductors [1,73]. The interleaved buck converter can also be described as two buck converter connected in parallel. The single phase half-bridge interleaved buck converter consists of two IGBTs, S_1 and S_2, two diodes D_1 and D_2 and two coupling inductors L_1 and L_2. In addition, the reliability of the inverter is greatly improved because the shoot-through phenomenon is eliminated and the lifetime of the inverter circuit is prolonged. This shoot-through current may flow for a nanosecond, but the recurrent occurrence of shoot-through affects the operation of the inverter with a high current stress in the conventional inverter switches. Hence, the current stress can also be eliminated by the use of an interleaved buck converter. The disadvantage associated with the interleaved buck converter is the requirement of more inductors as compared to conventional, but it can be compensated by special protection features required in conventional inverter circuits.

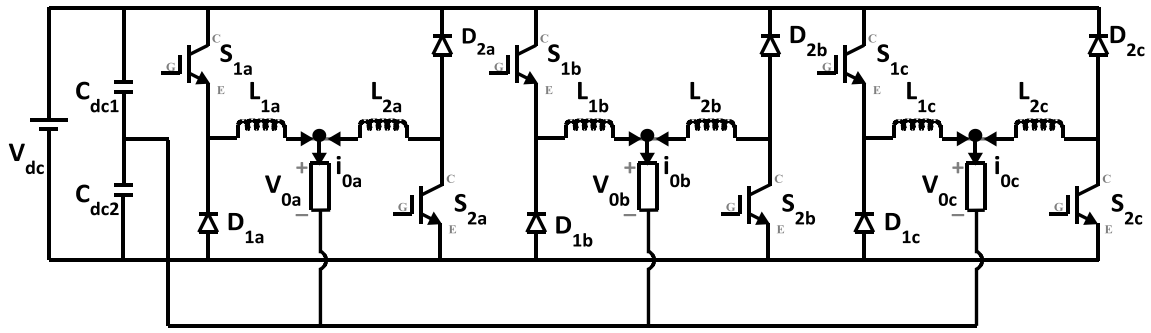


Figure 2.3: Three-phase half bridge interleaved buck converter

By the combination of three single-phase interleaved buck converter the 3-phase half-bridge interleaved buck (HB IB) converter can be formed as shown in Figure 2.3 and hence no shoot-through phenomenon. The 3-phase interleaved buck converter consists of six power switches i.e. IGBTs (S_1-S_6), 6 diodes (D_1-D_6) and 6 coupling inductors (L_1-L_6) [75]. The IB converter features numerous advantages such as the elimination of shoot-through current, high reliability and no requirement of dead time. A comparison of the interleaved buck converter with conventional divulges that:

(i) The Shoot-through phenomenon gets eliminated in the IB converter.

(ii) As the shoot-through phenomenon is being eliminated, the reliability of the IB converter circuit gets increased.

(iii) As there is no shoot-through current between the two series connected phase switches, the voltage and current stresses get reduced in the particular switch of the IB converter.

(iv) As the voltage and current stress get reduced, the cost of the devices gets reduced and also the cost of snubber circuit/ production circuit get reduced.

The critical issues related to conventional and interleaved buck inverter are listed in Table 2.1 below.

Table 2.1: Comparison of conventional and interleaved buck inverter

Critical Issues	Conventional Inverter	Interleaved buck Inverter
Shoot-through phenomenon	Present	Eliminated
Reliability	Less	More
Voltage and current stress on the switch	More	Less
Cost of switches and snubber circuit/ production circuit	More	Less

2.2.2 Three-phase four-wire Interleaved Buck Converter based Active Power Filter

For explaining the working principle of interleaved buck converter based active power filter the single phase topology has been considered [73]. Figure 2.4 depicts the single phase half-bridge interleaved buck converter and its working modes. The basic mind behind the working principle is defined as; positive current deals with power switch S_2, diode D_2 and coupling inductor L_2, as can be seen in the mode I and mode II. Similarly the negative current deals with power switch S_1, diode D_1 and coupling inductor L_1 being described in mode III and mode IV. In another way, the two buck converter connected in parallel supplies the whole compensating current [1,74].

The operating principle can be described as:

If $i_c > 0$;

Mode I: $\frac{di_c}{dt} > 0$: S_2 ON and C_2 supplies power.

Mode II: $\frac{di_c}{dt} < 0$: D_2 ON and C_2 works on the charging mode

i. If $i_c < 0$;

Mode III: $\frac{di_c}{dt} > 0$: S_1 ON and C_1 supplies power

Mode IV: $\frac{di_c}{dt} < 0$: D_1 ON and C_1 works on the charging mode

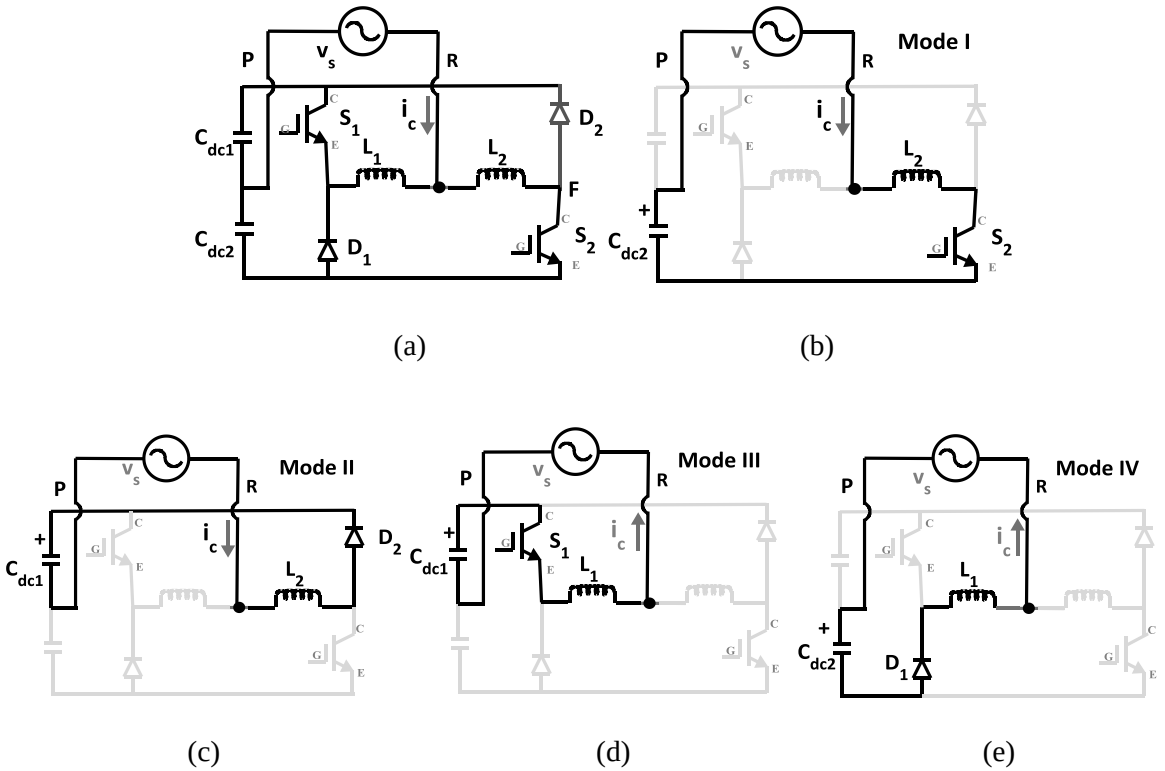


Figure 2.4: Single phase half-bridge interleaved buck converter based APF and its working modes

For the 3-phase 4-wire split capacitor interleaved buck active power filter (2C IB APF) depicted in Figure 2.5, the following equations are valid:

$$\begin{aligned} i_{sa} + i_{sb} + i_{sc} &= i_{sn} \\ i_{La} + i_{Lb} + i_{Lc} &= i_{Ln} \\ i_{ca} + i_{cb} + i_{cc} &= i_{cn} \end{aligned} \tag{2.2}$$

where, i_{sa}, i_{sb}, i_{sc} and i_{sn} represent the corresponding source phase currents and source neutral current. Similarly, the phase load currents and neutral current are represented by i_{La}, i_{Lb}, i_{Lc} and i_{Ln} and the compensating phase currents and neutral current are signified by i_{ca}, i_{cb}, i_{cc} and i_{cn} respectively.

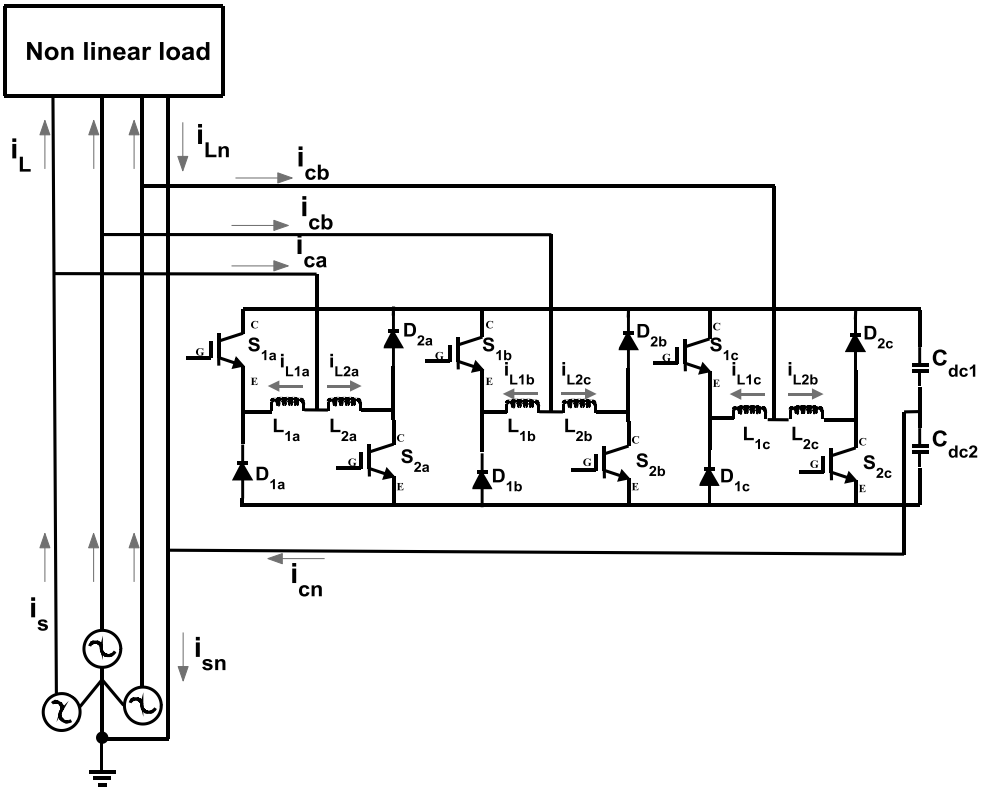


Figure 2.5: 3-phase 4-wire split capacitor interleaved buck active power filter

Again the compensating current can be depicted as the sum of the two coupling inductors current for each phase and are as follows:

$$\begin{aligned} i_{ca} &= i_{L1a} + i_{L2a} \\ i_{cb} &= i_{L1b} + i_{L2b} \\ i_{cc} &= i_{L1c} + i_{L2c} \end{aligned} \tag{2.3}$$

Where i_{L1a}, i_{L2b}, i_{L1b}, i_{L2b}, i_{L1c} and i_{L1c} are the corresponding phase coupling inductors current.

The minimum dc-link voltage required by this 3-phase 4-wire split capacitor interleaved buck active power filter (2C IB APF) [39] can be determined by the mathematical relationship.

$$V_{dc\,min} = \frac{\sqrt{3} \times \sqrt{2}}{0.87} V_{s,rms} = 2.815 \times V_{s,rms}$$

$$\text{hence, } V_{dc\,min} = 2.815 * 230 = 647.45\,V \tag{2.4}$$

The three-phase interleaved buck converter with split capacitor configuration suffers from following shortcomings:

i. The control circuit is somewhat complex due to the split capacitor configuration.

ii. The voltages of the two capacitors of a split capacitor need to be properly balanced. 3-phase interleaved inductor needs discrete diodes whereas the conventional inverter has the diodes assimilated with the switches and also it needs more output inductors as compared to conventional.

2.3 Control schemes for three-phase four-wire Interleaved Buck Active Power Filter

For accurate compensation of the harmonic current, it is very much difficult to choose the appropriate control strategies. The basic harmonic compensation scheme has been elaborated in Figure 2.6 using the close loop control system. On the other hand, the mains voltages at the PCC (Point of Common Coupling) can be unbalanced and nonsinusoidal due to current harmonics. Therefore, it is very considerable to study the behavior of active power filter under such voltage source conditions and determine the most suitable control strategy to attain the current compensation. The various control strategies like unity power factor (UPF), instantaneous reactive power theory (p-q), instantaneous active and reactive current component (i_d-i_q) method etc. are found in the literature. These control strategies forced the actual filter/compensating current to follow the reference compensating current.

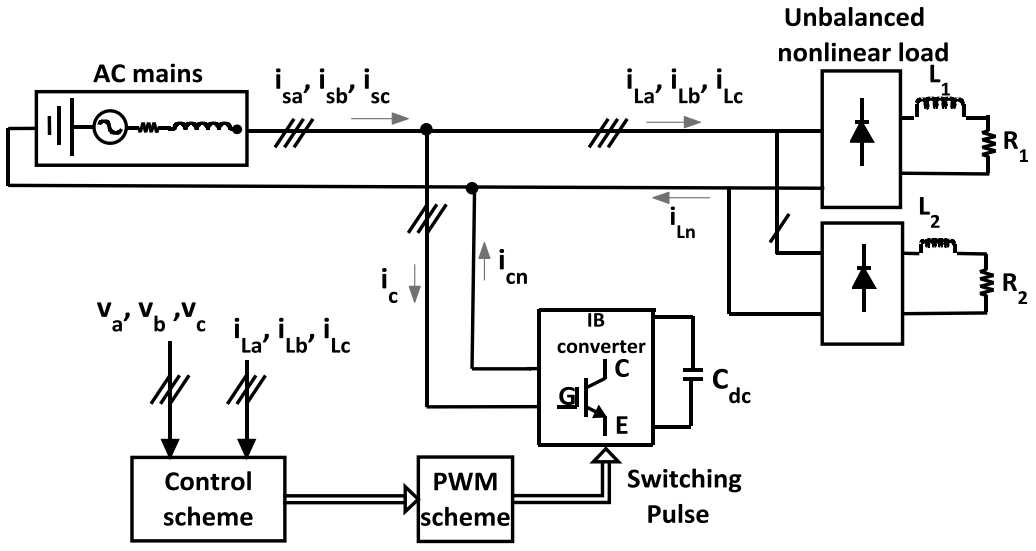


Figure 2.6: Basic harmonic compensation principle of interleaved buck shunt active power filter

For perfect harmonic compensation, the controller must be capable of.

i. Extracting or injecting of load harmonic current.
ii. Maintaining the dc-link voltage constant.

iii. Avoiding the absorption or generation of reactive power with fundamental frequency.

Finally, to generate the switching pattern, the hysteresis band current controller has been used. Again for less deviation in the range of the switching frequency, adaptive hysteresis band current controller has been applied. The researchers have been working on the traditional PI controller used on the dc side of for controlling the dc bus voltage of inverter as it is the key aspect of the harmonic compensation performance of the APFs.

2.3.1 Instantaneous Active and Reactive Power (p-q) Control Scheme

Though there are various control strategies proposed in the literature, p-q method is popular among them [83]. Some interesting features of this scheme are namely: it is a three phase system and can be applied to balanced or unbalanced system, and is based on the instantaneous values. The calculations are relatively small and include only algebraic expressions, allow two control strategies i.e. constant instantaneous supply power and sinusoidal supply current. The p-q control scheme used for reference current generation as shown in Figure 2.7 elucidate by Clarke's transformation using the three phase supply voltage and load current [84]. The general equations for the real power (p_L), reactive power (q_L) and the zero sequence power (p_0) in terms of α-β-0 reference is represented in matrix form as:

$$\begin{bmatrix} p_0 \\ p_L \\ q_L \end{bmatrix} = \begin{bmatrix} v_0 & 0 & 0 \\ 0 & v_\alpha & v_\beta \\ 0 & -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_{L0} \\ i_{L\alpha} \\ i_{L\beta} \end{bmatrix} \tag{2.5}$$

The instantaneous active, reactive and zero sequence power have average and oscillating component and are alluding to:

$$p_L = \overline{p_L} + \widetilde{p_L} \tag{2.6}$$

$$q_L = \overline{q_L} + \widetilde{q_L} \tag{2.7}$$

$$p_0 = \overline{p_0} + \widetilde{p_0} \tag{2.8}$$

The $\bar{p}$ is the only desirable power for p-q control strategy, other i.e. $\tilde{p}$, q and p_0 have to be compensated. The oscillating measure consists of active power p̃, and the average fragment of the zero sequence power $\overline{p_0}$ is get separated from the total active and zero sequence power for the calculation of reference compensating current in α-β frame and illustrates as:

$$\begin{bmatrix} i_{c\alpha}^* \\ i_{c\beta}^* \end{bmatrix} = \frac{1}{v_\alpha^2+v_\beta^2} \begin{bmatrix} v_\alpha & -v_\beta \\ v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} \widetilde{p_L} + \Delta\bar{p} \\ -q_L \end{bmatrix} \quad (2.9)$$

Where $\Delta\bar{p}$ represents the average real power absorbed by the voltage source inverter from α-β axis to attain the energy balance within the active power filter, when it deliveries p_0 to the load.

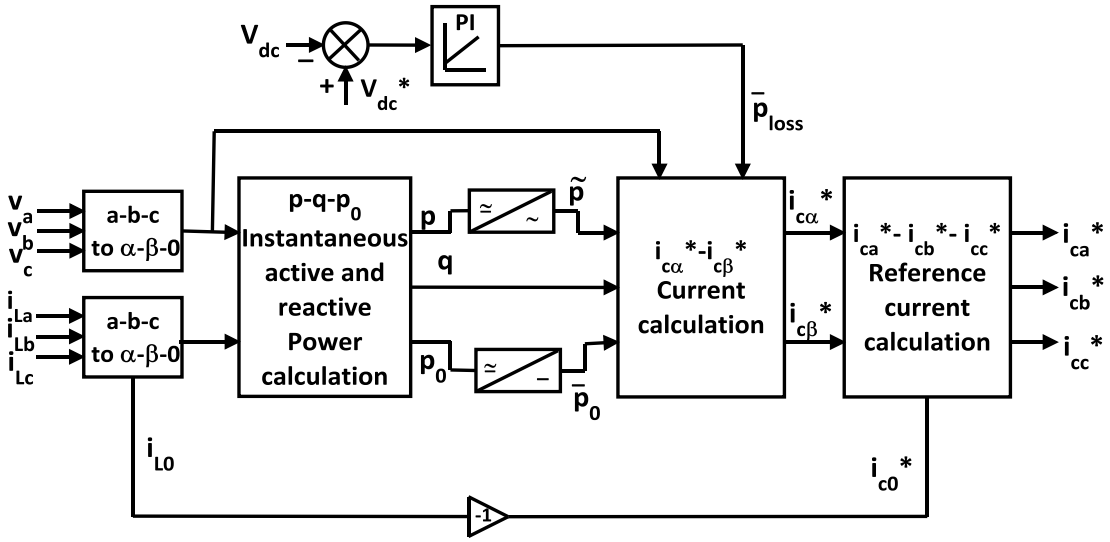


Figure 2.7: Control block diagram of p-q control strategy used for 2C IB APF

The additional average power required by the split capacitor interleaved buck converter is

$$\Delta\bar{p} = \overline{p_0} + \bar{p}_{loss} \quad (2.10)$$

Where $\overline{p_0}$ is the average load zero sequence power that has to be recompensed from the active power filter and $\bar{p}_{loss}$ is the losses occurred inside the voltage source inverter. $\bar{p}_{loss}$ is attained by the dc-link voltage regulator as output of the PI controller as can be defined as

$$\bar{p}_{loss} = K_p \Delta V_{dc} + K_i \int \Delta V_{dc} \, . \, dt \quad (2.11)$$

Where K_p, K_i are PI controller proportionality constant and ΔV_{dc} is the error voltage i.e. $V_{dc} - V_{dc}^*$.

The zero sequence reference compensating current i_{c0}^* should be same and opposite to the harmonic content in the zero sequence load current and hence provides the required zero sequence compensating current. The valid equation is;

$$i_{c0}^* = i_{L0} \quad (2.12)$$

To end with the reference compensating current equation for the p-q control strategy as;

$$\begin{bmatrix} i_{ca}^* \\ i_{cb}^* \\ i_{cc}^* \end{bmatrix} = \sqrt{2/3} \cdot \begin{bmatrix} 1 & 0 & 1/\sqrt{2} \\ -1/2 & \sqrt{3}/2 & 1/\sqrt{2} \\ -1/2 & -\sqrt{3}/2 & 1/\sqrt{2} \end{bmatrix} \cdot \begin{bmatrix} i_{c\alpha}^* \\ i_{c\beta}^* \\ i_{c0}^* \end{bmatrix} \quad (2.13)$$

In this method, the calculation of active power and reactive power by multiplying the instantaneous source voltage and instantaneous load current leads to the amplification in the harmonic content.

Due to the increased harmonic content, it does not able to provide precise harmonic compensation under non sinusoidal and unbalanced supply voltage condition.

2.3.2 Instantaneous Active and Reactive Current Component (i_d-i_q) Control Scheme

The i_d-i_q control strategy [85] used for reference compensating current generation, as shown in Figure 2.8 explain by Clarke's and Park's transformation using the three phase supply voltage and load current is as follows:

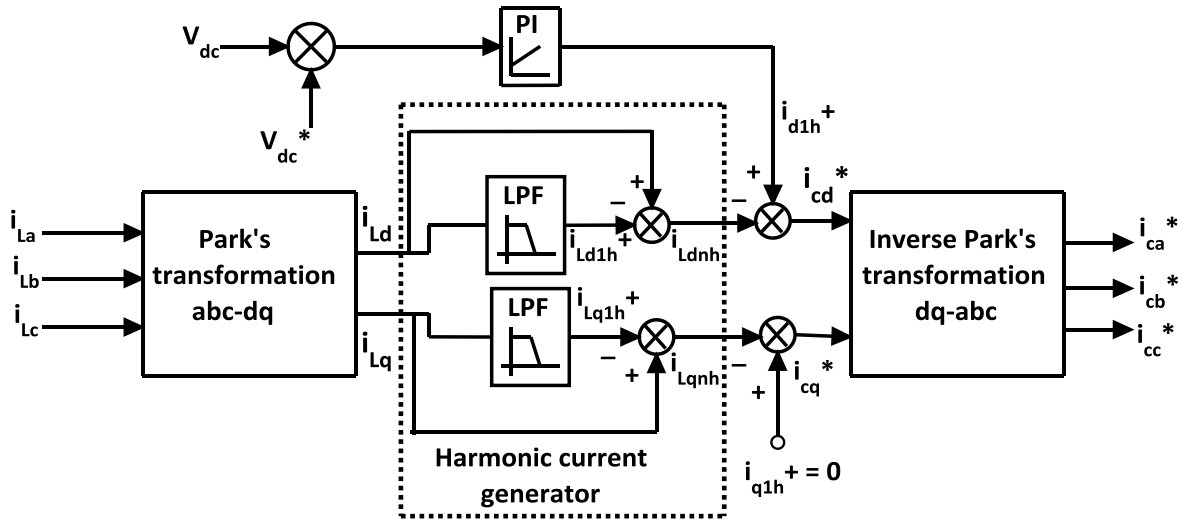


Figure 2.8: Control block diagram of i_d-i_q control strategy used for 2C IB APF

For the source voltages v_a, v_b, v_c, it is possible to acquire the αβ transformation as in (2.14) gives:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{2/3} \cdot \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \cdot \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (2.14)$$

Similarly, the transformation of the instantaneous load current in αβ0 frame, i.e.

$$\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \\ i_{L0} \end{bmatrix} = \sqrt{2/3} \cdot \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \cdot \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \quad (2.15)$$

Where, v_a, v_b, v_c and i_{La}, i_{Lb}, i_{Lc} are the respective phase source voltage and phase load current.

Again, it is possible by applying the Park's transformation, the equivalence calculation for the active, reactive and zero sequence current (i_{Ld}, i_{Lq}, i_{L0}) is as,

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \\ i_{L0} \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta & 0 \\ -\sin\theta & \cos\theta & 0 \\ 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \\ i_{L0} \end{bmatrix}, \theta = \tan^{-1}\left(\frac{v_\beta}{v_\alpha}\right) \quad (2.16)$$

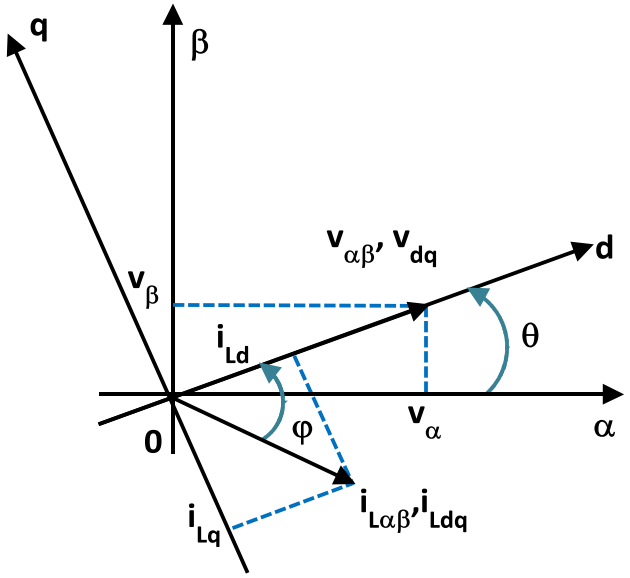


Figure 2.9: Instantaneous voltage and current vectors

Where, θ signifies the instantaneous voltage vector as shown in Figure 2.9. The equation (2.16) can be rewritten in terms of v_α and v_β with the value of direct voltage component as $v_d = |\bar{v}_{dq}| = |\bar{v}_{\alpha\beta}| = \sqrt{v_\alpha^2 + v_\beta^2}$ and q axis voltage being always zero.

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \\ i_{L0} \end{bmatrix} = \frac{1}{\sqrt{v_\alpha^2 + v_\beta^2}} \cdot \begin{bmatrix} v_\alpha & v_\beta & 0 \\ -v_\beta & v_\alpha & 0 \\ 0 & 0 & v_{\alpha\beta} \end{bmatrix} \cdot \begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \\ i_{L0} \end{bmatrix} \quad (2.17)$$

The instantaneous active load current i_{Ld} and reactive load current i_{Lq} has average component as well as oscillating component and are alluding to,

$$i_{Ld} = \bar{\imath}_{Ld} + \tilde{\imath}_{Ld} \tag{2.18}$$

$$i_{Lq} = \bar{\imath}_{Lq} + \tilde{\imath}_{Lq} \tag{2.19}$$

In the condition of ideal sinusoidal voltage source, the first harmonic positive sequence of load current is transmuted to average term, i_{Ld1h}^{+} and i_{Lq1h}^{+}, that must be well-kept in the mains. The remaining oscillating component (i_{Ldnh} and i_{Lqnh}) of the load current (i_{Ld} and i_{Lq}) desires to be injected by the IB APF. The ac quantities can get filtered out by using high pass filter, but here an alternative high pass filter has been conceded. The alternative high pass filter arrangement is nothing but with the use of low pass filter to have the average or dc component as output, which gets subtracted from the total load current component to have the ac component, that is clarified as from the Figure 2.9,

$$i_{dnh} = i_{Ld} - i_{Ld1h}^{+} \tag{2.20}$$

$$i_{Lqnh} = i_{Lq} - i_{Lq1h}^{+} \tag{2.21}$$

Here, the low pass Butterworth filter has been used, having a cut-off frequency of 25 Hz. Finally, to obtain the phase reference compensating current, another component of current is required that is i_{d1h}^{+}, first harmonic direct current of positive sequence and that can be obtained from the dc-link voltage regulation system by using PI controller. The input of the PI controller is $V_{dc}^{*} - V_{dc}$, whereas the output is i_{d1h}^{+} and is considered as the first harmonic direct current of positive sequence, which is responsible to regulate active power flow within the voltage source interleaved buck inverter and hence the dc-link voltage V_{dc}.

Here, the primary aim is the harmonic mitigation of the source current, hence the first harmonic of quadrature current of positive sequence (i_{q1h}^{+}) is tuned to zero. For the compensation of reactive power, the reactive power flow to the IB inverter may be controlled by i_{q1h}^{+}. After getting the active reference compensating current (i_{cd}^{*}) and reactive reference compensating current (i_{cq}^{*}) by considering the first harmonic of direct current of positive sequence by using PI, applied inverse Park's and Clarke's transformation to extract the reference compensating current in terms of a, b and c.

So by following the inverse Park's and Clarke's transformation the reference compensating current matrix equations are as follows,

$$\begin{bmatrix} i_{c\alpha}^{*} \\ i_{c\beta}^{*} \\ i_{c0}^{*} \end{bmatrix} = \frac{1}{\sqrt{v_{\alpha}^{2}+v_{\beta}^{2}}} . \begin{bmatrix} v_{\alpha} & -v_{\beta} & 0 \\ v_{\beta} & v_{\alpha} & 0 \\ 0 & 0 & v_{\alpha\beta} \end{bmatrix} . \begin{bmatrix} i_{cd}^{*} \\ i_{cq}^{*} \\ i_{c0}^{*} \end{bmatrix} \tag{2.22}$$

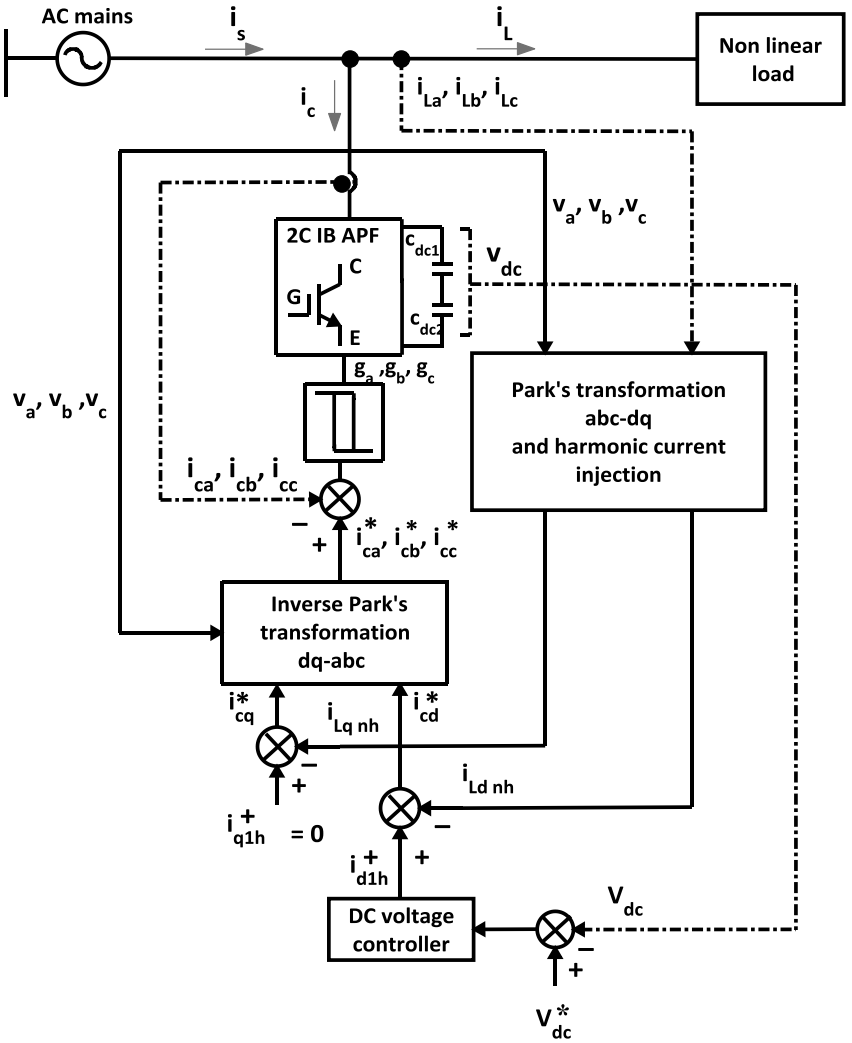


Figure 2.10: Harmonic compensation scheme of 2C IB APF using i_d-i_q control strategy

$$\begin{bmatrix} i_{ca}^* \\ i_{cb}^* \\ i_{cc}^* \end{bmatrix} = \sqrt{2/3} \cdot \begin{bmatrix} 1 & 0 & 1/\sqrt{2} \\ -1/2 & \sqrt{3}/2 & 1/\sqrt{2} \\ -1/2 & -\sqrt{3}/2 & 1/\sqrt{2} \end{bmatrix} \cdot \begin{bmatrix} i_{c\alpha}^* \\ i_{c\beta}^* \\ i_{c0}^* \end{bmatrix} \tag{2.23}$$

The i_{c0}^* signifies the zero sequence reference compensating current which has to be exactly recompensed the zero sequence of the load current and hence can be equated as:

$$i_{c0}^* = i_{L0} \tag{2.24}$$

The harmonic compensation scheme of the proposed split capacitor interleaved buck active power filter using i_d-i_q control strategy is illustrated in Figure 2.10. The reference compensating current is being compared with the actual compensating current of the 2C IB APF in hysteresis band current controller to generate the switching pattern for the interleaved buck converter power switches.

In comparison to p-q control strategy, i_d-i_q control strategy works very well in unbalanced and non-sinusoidal voltage source condition [85]. As the Park's transformation gives sureties for the power invariance, a comparison can be made between the two control strategies. This comparison can be understood by considering active and reactive power. In ideal sinusoidal voltage source condition, the oscillatory component of voltage $\widetilde{v_d}$ is null, hence the compensating power $p_{c1}$and q_{c1} for the p-q control strategy is equivalent to the compensation power p_{c2} and q_{c2} by the i_d-i_q control strategy. But, for unbalanced and non-sinusoidal voltage source condition, the voltage oscillatory component $\widetilde{v_d}$ is to be considered and hence the p-q control strategy constitutes additional disturbances as compared to i_d-i_q control strategy. As can be seen from equation (2.25), the additional disturbance contributed significantly owing to the product between the oscillatory component of voltage and average component of load current.

$$\begin{bmatrix} p_{c1} \\ q_{c1} \end{bmatrix} - \begin{bmatrix} p_{c2} \\ q_{c2} \end{bmatrix} = -\widetilde{v_d} \begin{bmatrix} I_{Ld} \\ -I_{Lq} \end{bmatrix} \tag{2.25}$$

Thus, it can be concluded that, under ideal sinusoidal voltage source condition, both the control strategies work very well and have nearly same performance; but in case of unbalanced and nonsinusoidal voltage source condition, the average and oscillatory power gets disturbed and hence the compensation performance gets degraded by the p-q control strategy.

2.4 DC-link voltage regulator with PI controller

In the steady state condition, the real power supplied by the source is equal to the power demand of the load and the small power required for the switching loss compensation occurred in the IB APF. Hence the dc-link capacitor voltage may be maintained constant. But during the dynamic condition, i.e. whenever there is a change in the load, the real power balanced gets disturbed between the source and load. This real power variance can be supplied by the charging/discharging of dc-link capacitor and hence the dc-link capacitor gets disturbed. However, if the dc-link voltage gets recovered, and attains the reference voltage; the real power flow from the source becomes equal to the consumed power by the load. The high quality of IB APF performance mainly depends on the dc-link voltage control.

For regulating and maintaining the dc-link capacitor voltage constant [20], the active power flowing into the active filter needs to be controlled. If the active power flowing into

the filter can be controlled equal to the losses inside the filter, the dc-link voltage can be maintained at the desired value. The quality and performance of the shunt active power filter depend mainly on the method implemented to generate the compensating reference current. In order to maintain dc-link voltage constant, here a PI controller branch is added to the d-axis in d–q frame to control the active current component. The PI controls this small amount of active current and then the current controller regulate this current to maintain the dc-link capacitor voltage.

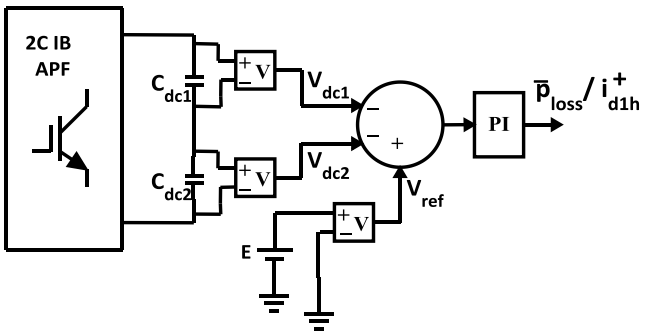


Figure 2.11: DC-link voltage controller block diagram using PI controller

The design of the dc-link capacitor is governed by the instantaneous power flow, whereas the value of the dc-link capacitor may be based on the reduction of the dc-link voltage ripple. Thus, the defining equation that can be used for the calculation of C_{dc} is as [92];

$$C_{dc} = \frac{\pi \times I_{cr}}{\sqrt{3}\,\omega\; V_{dc\,ripple,p\_p}} \tag{2.26}$$

Where, I_{cr} represents the rated filter current and $V_{dc\,ripple,p\_p}$ represents the peak-peak value of the dc-link voltage ripple

Again, the dc-link voltage must be more than the peak value of the utility source voltage, i.e. to force the IB APF output current under the command of reference compensating current. If the dc-link voltage opts less than the peak of the utility source voltage, then the performance level of active power filter degrades; whereas, opting for higher voltage, the THD decreases but the settling time increases. Most important, if the dc-link voltage is chosen very high, more voltage stress occurs in the power switches and hence more rated power switches and dc-link capacitor.

The dc-link capacitor performing as the energy source retains the balance of energy inside the IB APF. The component of reference compensating current i_{d1h}^{+} / average power $\bar{p}_{loss}$ to reinstate the energy in the dc-link capacitor is being calculated based on the energy

balance. The nominal stored energy e_{dc}^* equation for the dc-link capacitor of APF can be depicted as;

$$e_{dc}^* = \frac{1}{2} C_{dc}(V_{dc}{}^*)^2 \tag{2.27}$$

But, the actual energy e_{dc} stored in the dc-link capacitor with the actual dc-link capacitor voltage V_{dc} is;

$$e_{dc} = \frac{1}{2} C_{dc} (V_{dc})^2 \tag{2.28}$$

The energy loss in IB APF can be found from the equation;

$$\Delta e_{dc} = e_{dc}^* - e_{dc} = \frac{1}{2}\{(V_{dc}{}^*)^2 - (V_{dc})^2\} \tag{2.29}$$

Where V_{dc} and $V_{dc}{}^*$ are actual and reference dc-link capacitor voltage. This energy difference Δe_{dc} is being supplied by means of the dc-link voltage regulator.

The PI controller used for the control of dc-link capacitor voltage is shown in Figure 2.11. The peak value of the reference current is estimated by adjusting the dc-link voltage. The actual capacitor voltage value is compared with the set reference dc voltage value. The error signal is then processed through a PI controller, which contributes to the zero steady state error in tracking the reference current signal. The output of the PI controller is responsible for the active power flow control to the active power filter and thus the dc-link voltage regulation. The design of the PI controller needs precise linear mathematical model. Here, the tuning of PI controller has been done by Ziegler-Nichols method [95].

2.5 Conventional and Adaptive Hysteresis Band Current Controller

Hysteresis PWM scheme is intended to be used by the active power filter for the instantaneous harmonic compensation. The actual filter current is forced to follow the reference compensating current path being obtained by any of the control strategies. The continually tracked actual compensating currents (i_{ca}, i_{cb}, i_{cc}) are compared with the reference compensating current ($i_{ca}^*, i_{cb}^*, i_{cc}^*$) using the conventional hysteresis band current controller for generating the switching pulses as shown in Figure 2.12. The conventional hysteresis band current controller has been proven to be the most appropriate for generating the switching signal for shunt active power filter [96]. The conventional hysteresis controller may be considered as a simple control strategy with the characterization of fast response during the transient. The other characteristic incorporated

with it is the inherent stability with good accuracy. The phase pulse width modulated (PWM) current and voltage waveforms are shown in Figure 2.13. The conventional HBCC used in IB APF composed of a hysteresis around the reference compensating current i_c^*.

The switching pattern of the power switches decides by the hysteresis band current controller and is formulated as:

i. If $i_{ca} < (i_{ca}^* - HB)$, the upper power switch is OFF and lower power switch is ON of the phase IB cell

ii. If $i_{ca} > (i_{ca}^* + HB)$, the upper power switch is ON and lower power switch is OFF of the phase IB cell

However, this conventional hysteresis control scheme exhibits a quite lot of demerits, such as more variation in switching frequency, extra switching losses and likely to produce resonance [97-98]. Due to above demerits here adaptive hysteresis band current controller has been considered as shown in Figure 2.14 by which the switching frequency becomes nearly constant.

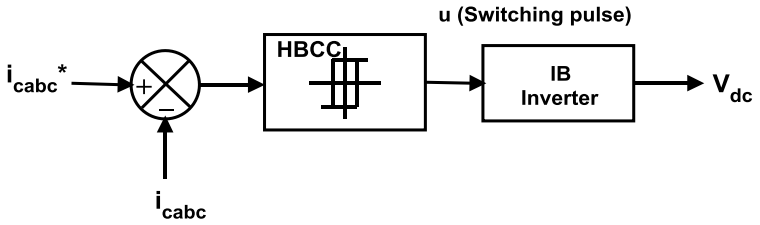


Figure 2.12: Hysteresis band current controller PWM scheme for the generation of switching pulses

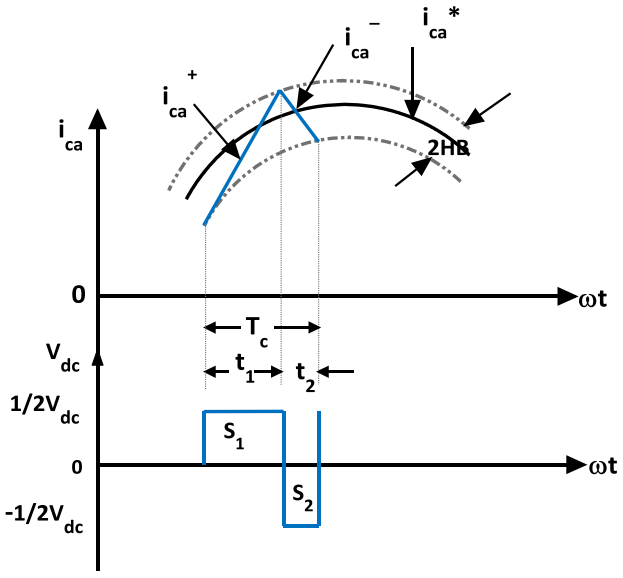


Figure 2.13: Hysteresis band current controller PWM scheme current and voltage waveforms

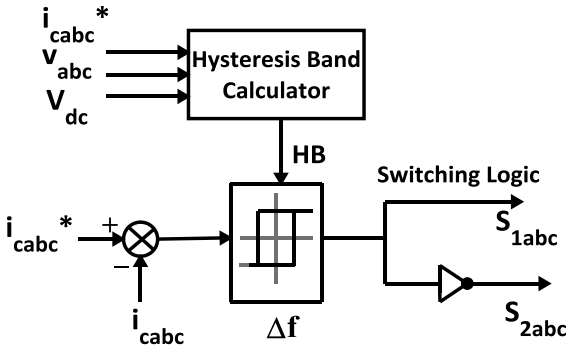


Figure 2.14: Adaptive hysteresis band current controller (AHBCC)

For nearly constant switching frequency, the hysteresis band is being managed as:

$$HB_j = \frac{V_{dc}}{8 f_m L}\left[1 - \frac{4L^2}{V_{dc}^2}\left(\frac{V_s(t)}{L} + \frac{di_{cj}^*}{dt}\right)^2\right], \text{ j=a, b, c phase} \qquad (2.30)$$

The equation (2.30) depicts the hysteresis band of the adaptive hysteresis band current controller where f_m represents the modulation frequency, i_{cj}^* defined the compensating reference current and $\frac{di_{cj}^*}{dt}$ denotes its slope, L stands for the coupling inductance of the 2C-IB APF, V_{dc} signifies dc-link voltage and $v_s(t)$ to be the supply voltage. At any instant of time, in full bridge interleaved buck inverter, two coupling inductors come into the picture, and hence both the inductors have the effect on the hysteresis band, that is $L_{1x} + L_{2x}$, where x represent for a, b and c phase. The switching frequency generated here is a maximum of 10 KHz.

2.6 Analysis Tools

Now a day, major studies on modern power system needs very fast, flexible and scalable real time simulators. The latest real time simulator works with the field programmable gate array (FPGA) integrated circuit [162].

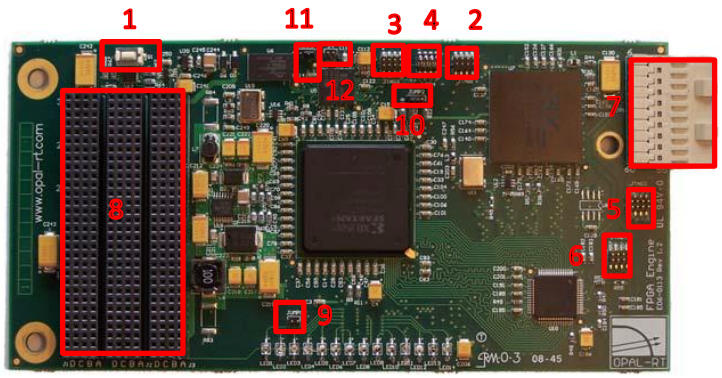


Figure 2.15: OP5142 Reconfigurable Board indicating components

Table 2.2: Components Description of OP5142 Reconfigurable Board

#	Name	Description	#	Name	Description
1	S1	FPGA Engine manual reset	7	JP1	PCIe synchronization bus and power supply
2	JTAG1	FPGA JTAG interface	8	J1/J2/J3	Backplane data, ID and I^2C interface
3	JTAG2	CPLD JTAG interface	9	JUMP1	Identification EEPROM write protection
4	JUMP4	JTAG Architecture selection	10	JUMP2	FPGA configuration mode selection
5	JTAG3	PCIe Bridge JTAG interface	11	JUMP3	Flash memory write protection
6	JTAG4	SerDes JTAG interface	12	J4	Flash memory forced programmation voltage

FPGA-Field Programmable Gate Array, JTAG-Joint Test Action Group, CPLD-Complex Programmable Logic Device, PCIe-Peripheral Component Interconnect Express, SerDes-Serializer/Deserializer, I^2C-Inter-Integrated Circuit, EEPROM-Electrically Erasable Programmable Read Only Memory.

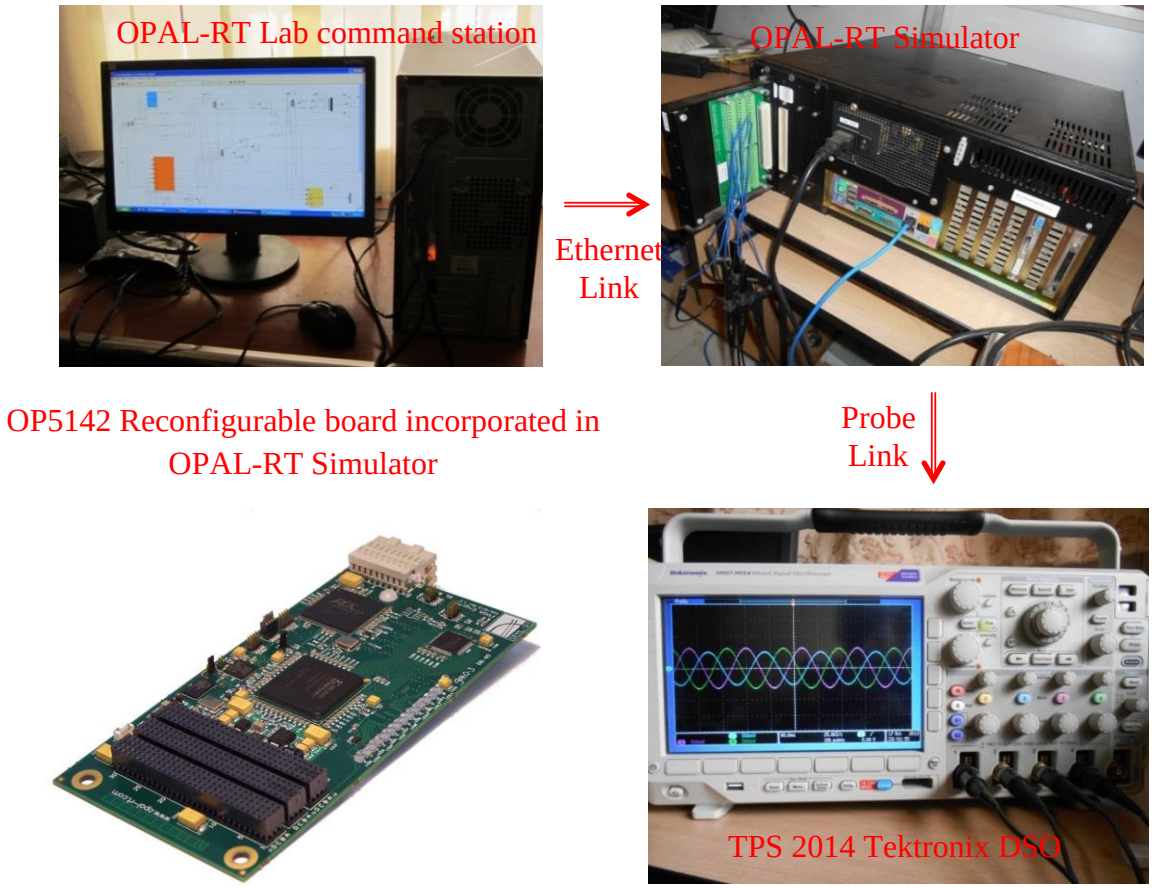


Figure 2.16: OPAL-RT LAB Setup

Based on this, OPAL-RT is designed and is defined as the open Real-Time simulation software environment which has modernised the way Model-based design is performed and is fully incorporated with MATLAB/Simulink.

This OPAL-RT simulator permits real-time simulations of Simulink models with hardware in the loop in a very fast response at a low cost. It is flexible enough to handle most complex Simulink model either, it is a real time hardware in the loop or to speed up model execution, control and test [98,115].

The OP5142 (Figure 2.16) is the key building blocks in the modular OP5000 I/O system from OPAL-RT technologies. The Field programmable gate array (FPGA) technology is incorporated in RT-LAB simulation cluster for distributed execution of hardware description language (HDL) functions and high speed, high density digital I/O in real time models. Based on the highest density Xilinx Spartan-3 FPGAs, the OP5142 can be attached to the backplane of an I/O module of either a Wanda 3U or Wanda 4U-based OPAL-RT simulation system. It communicates with the target PC via a Peripheral Component Interconnect (PCI)-Express ultra-low-latency real time bus interface. The key features are as follows:

i. Reconfigurability

The OP5142 platform FPGA device can be configured exactly as required by the user. Integration with Simulink, the system generator for DSP toolbox from Xilinx and RT-XSG from OPAL-RT technologies allow the transfer of Simulink submodes to the OP5142FPGa processor for distributed processing.

In addition, standard and user developed functions can be stored in the on-board Flash memory for instant start up. The OP5142 board is configurable on-the- fly using the PCIe bus interface and the RT-LAB /Live lab design environments

ii. Performance

OP5142 series products enable update rates of 100 MHz, providing the capability to perform time stamped capture and generation of digital events for high precision switching of items such as PWM I/O signaling up to very high frequencies, as I/O scheduling is performed directly on the OP5142 board

iii. Required skills and knowledge

The user must be familiar with hardware description language Simulink. With the help of a Xilinx system generator for DSP tool box, only minimal programmable technical

knowledge is needed to use the OP5142 board. This blockset is used to translate the Simulink design built using particular library blocks into HDL. The translated design is used by OPAL-RT tools to give access to I/O interfaces and debugging facilities. Real-time Xilinx System Generators (RT-XSG) uses Simulink to define models that will be executed by the reconfigurable platform. So it is expected that the user has a clear understanding of Simulink operation, particularly regarding the model definition and simulation parameters.

iv. Software and Hardware requirements

The OP5142 PCIe Reconfigurable platform needs the software such as Microsoft Windows XP (32- bit version), Xilinx ISE design suitev10.1, Xilinx system generator for DSP v10.1 and Mat lab R2007b or R2008a in order to able to generate a programming file for the reconfigurable device and to perform the platform.

Similarly, the minimal requirement of hardware requirements are RT-LAB compatible Wanda 3U or Wanda 4U target computer with a free PCIe bus slot, a Wanda Backplane Adapter as an interface between the OP5142 board and the target PC I/O module, a PCI-Express board and cable as an interface between the OP5142 board and the target PC PCIe bus, and refer to third party software documentation for host computer minimal configuration.

Technical specification of OPAL-RT

i. Digital I/O

No of channels-256 input/output configurable in 1to 32 bit groups, compatibility- 3.3 V, power on state- high impedance.

ii. FPGA

Device- Xilinx Spartan 3, I/O package- fg676, Embedded RAM available- 216 Kbytes, Clock-100 MHz, Platform options- XC3S5000, Logic slices- 33,280, Equivalent Logic cells- 74880, available I/o Lines- 489.

iii. Bus

Dimensions (not including connectors) - PCI Express x1, Data transfer-2.5 Gbit/s.

As shown in Figure 2.16 the Simulink model is performed on the personal computer (PC) with OPAL-RT software loaded. The PC is connected to the OPAL-RT simulator via Ethernet and the output result is taken by the Data Storage Oscilloscope (DSO) connected to the simulator.

2.7 System Performance of p-q and i_d-i_q control strategies with PI controller using Hysteresis PWM

At first, extensive investigations were performed on the three-phase conventional inverter and interleaved buck inverter circuit to acquire the shoot-through result. Shoot-through current in the conventional inverter circuit is very difficult to measure because this fault current persists for only a few ns. The 3-phase conventional and interleaved buck inverter has been modelled in MATLAB/Simulink environment with R-L load and the switch current has been captured. Here, the MATLAB simulation results are presented for both the conventional and interleaved buck three-phase inverter. Again the conventional hysteresis band current controller (HBCC) and adaptive hysteresis band current controller (AHBCC) has been applied with i_d-i_q control strategy to verify the switching frequency of the split capacitor interleaved buck active power filter (2C IB APF) and are presented in the results section.

Else, the proposed 2C IB-APF has been implemented in real time OPAL-RT hardware with conventional hysteresis PWM based p-q and i_d-i_q control strategy by using the PI controller for unbalanced three-phase and single-phase non-linear loads. Again the i_d-i_q based 2C IB APF topology has been tested for adaptive hysteresis during the dynamic condition. Investigations are carried out under different supply voltage conditions, i.e. balanced sinusoidal, unbalanced sinusoidal and non-sinusoidal.

The simulation and real-time digital simulator results presented in later shows the 3-phase source voltage, load current, compensating current, source current, load neutral current, source neutral current and dc-link capacitor voltage for each supply mains condition. The detailed parameters used by the Simulink models are showcased on Table 2.3. The degree of three phase IB-APF is measured in terms of compensation abilities with dc voltage regulation. From the results it can be seen that, the neutral current get cancelled after compensation.

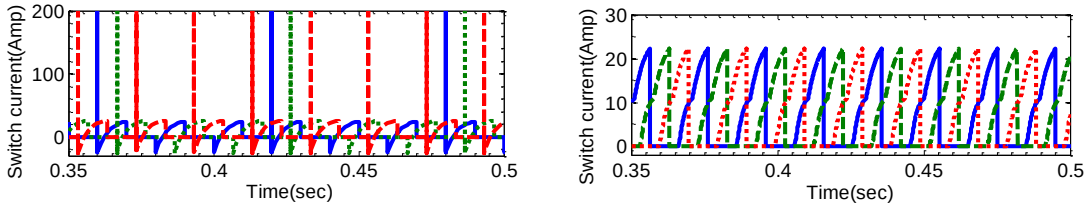
2.7.1 Steady State performance discussion with MATLAB and OPAL-RT Results

Table 2.3 depicts the values used by both the simulation and OPAL-RT lab for steady state performance of p-q and i_d-i_q control strategy for unbalanced load current.

Table 2.3 Simulation condition parameters for steady state analysis of 2C IB APF

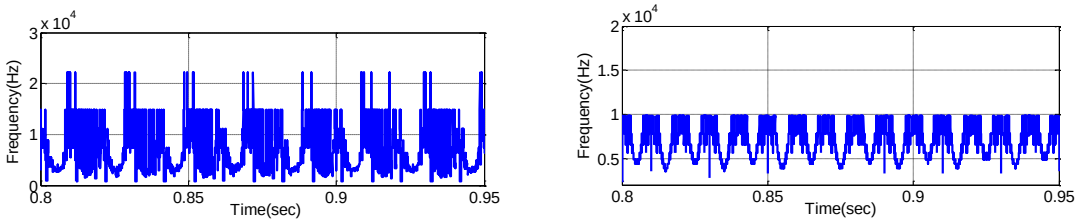
System parameters	FB-IB APF value
Supply Voltage (RMS)	Vs = 400 V (Line voltage)
Supply Frequency	fs = 50Hz
dc-link capacitance	C_{dc} = 1500 µF
dc-link capacitor voltage	V_{dc} = 800 V
APF coupling inductor	L = 600 µH
Non-linear load value	3-phase non-linear load R_1 = 16 Ω and L_1=50 mH 1-phase non-linear load R_2 = 16 Ω and L_2 = 50 mH

The conventional 3-phase half bridge inverter and interleaved buck inverter circuit have been simulated to investigate the "shoot-through" phenomenon for R-L load and from the simulation results, it is clarified that in conventional inverter circuit, the high shoot-through current is conducted through the IGBTs which decreases the reliability and in the dual buck inverter, the shoot-through current has been eliminated. The 3-phase conventional and interleaved buck inverter switch current have been illustrated in Figure 2.17a and 2.17b. The elimination of shoot-through current greatly improves the inner reliability of the active power filter.



(a) (b)

Figure 2.17: Switch current for R-L load in (a) conventional 3 -phase half- bridge inverter with shoot-through current (b) 3 -phase half - bridge inverter with no shoot-through current



(c) (d)

Figure 2.18: Switching frequency of the power switches using (c) conventional hysteresis band current controller (d) adaptive hysteresis band current controller based i_d-i_q control strategy during steady state condition

Steady state performance of 2C-IB APF under unbalanced load with PI controller using HBCC p-q control strategy

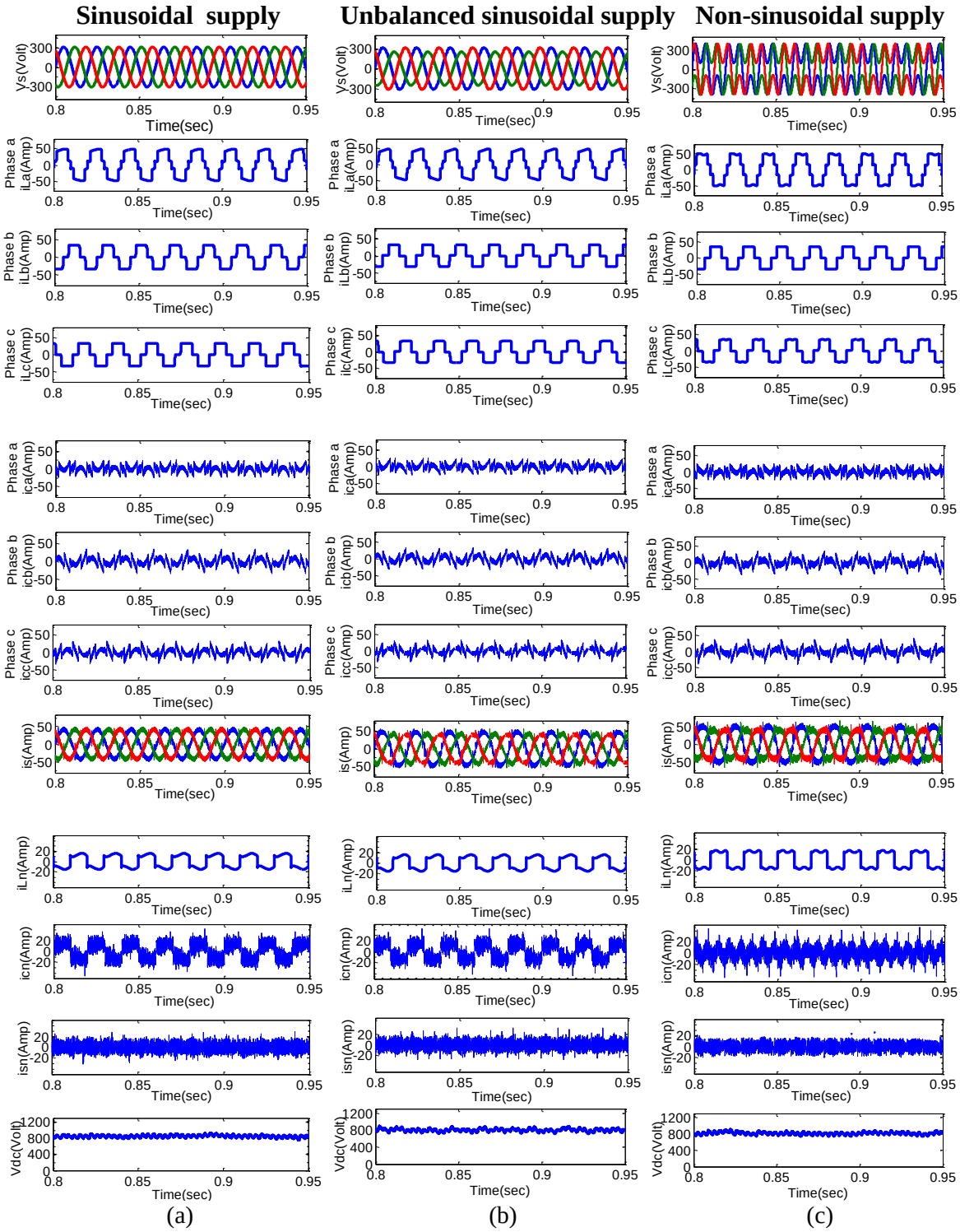


Figure 2.19: Steady state simulation results of 2C IB APF with unbalanced load using HBCC p-q control strategy for load current (i_L), filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}), under (a) ideal sinusoidal voltage supply, (b) unbalanced sinusoidal voltage supply, and (c) non-sinusoidal voltage supply

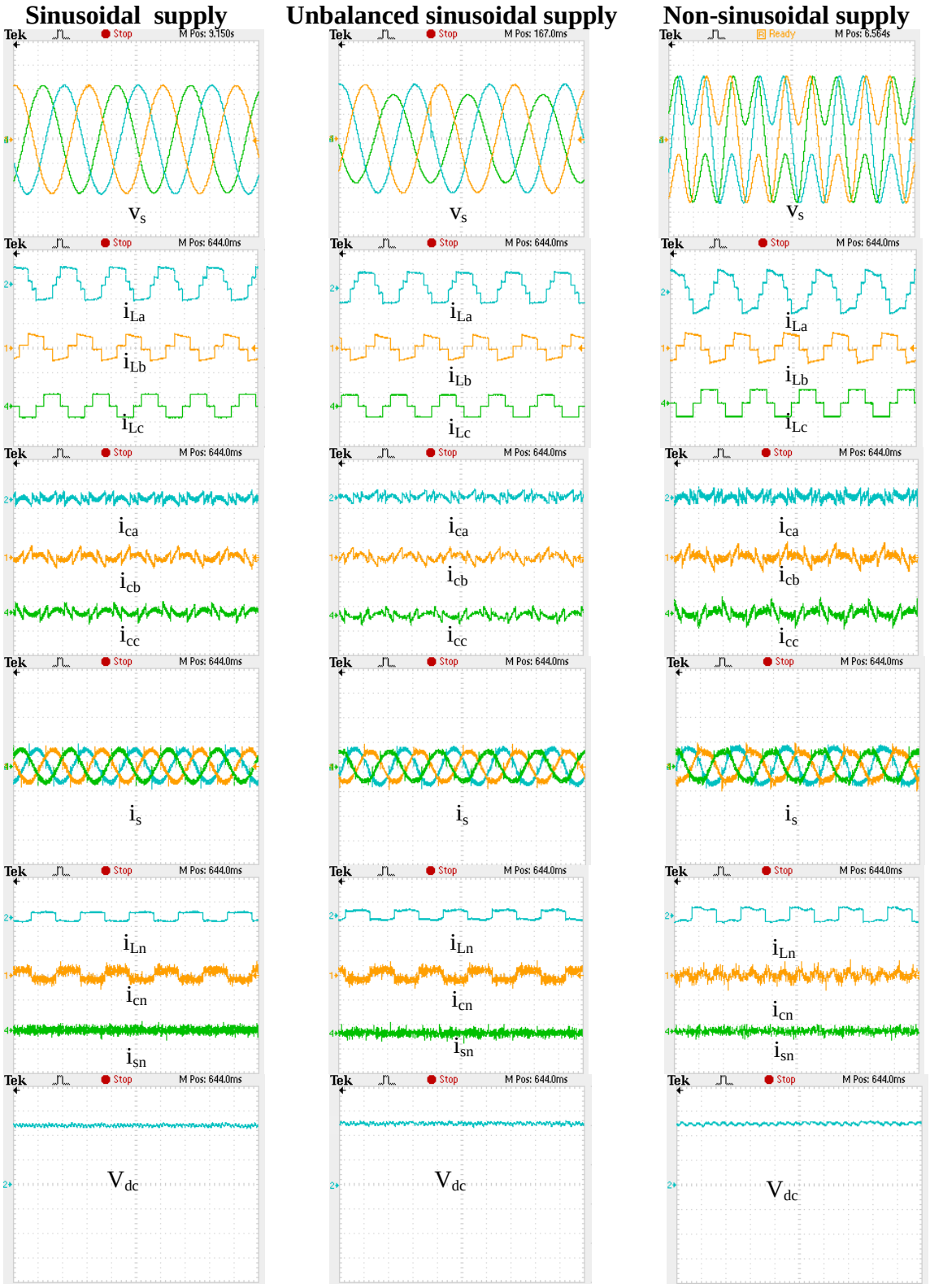


Figure 2.20: Steady state OPAL-RT results of 2C IB APF with unbalanced load using HBCC p-q control strategy for load current (i_L), filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}), under (a) ideal sinusoidal voltage supply, (b) unbalanced sinusoidal voltage supply, and (c) non-sinusoidal voltage supply

Steady state performance of 2C-IB APF under unbalanced load with PI controller using HBCC i_d-i_q control strategy

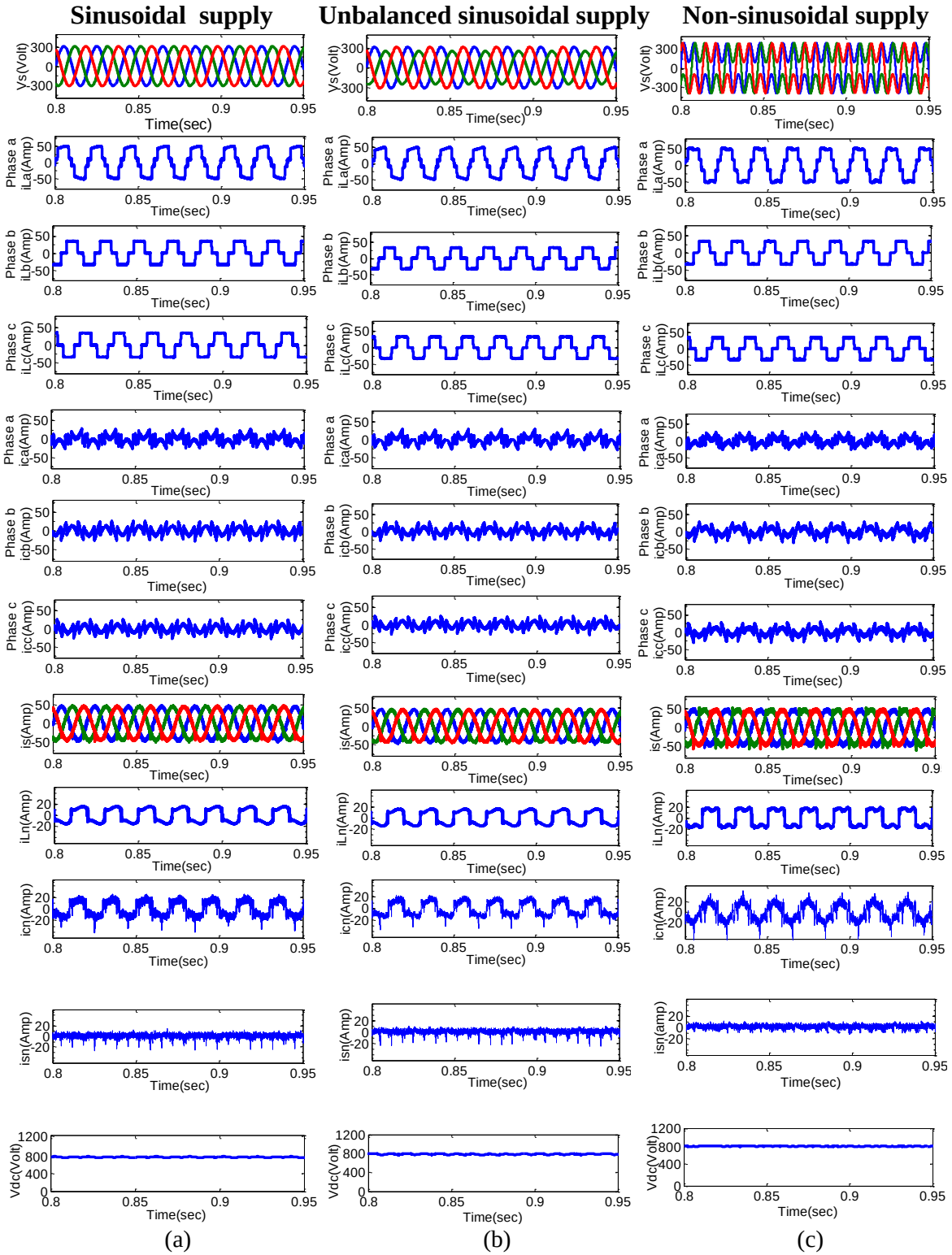


Figure 2.21: Steady state simulation results of 2C IB APF with unbalanced load using HBCC i_d-i_q control strategy for load current (i_L), filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}), under (a) ideal sinusoidal voltage supply, (b) unbalanced sinusoidal voltage supply, and (c) non-sinusoidal voltage supply

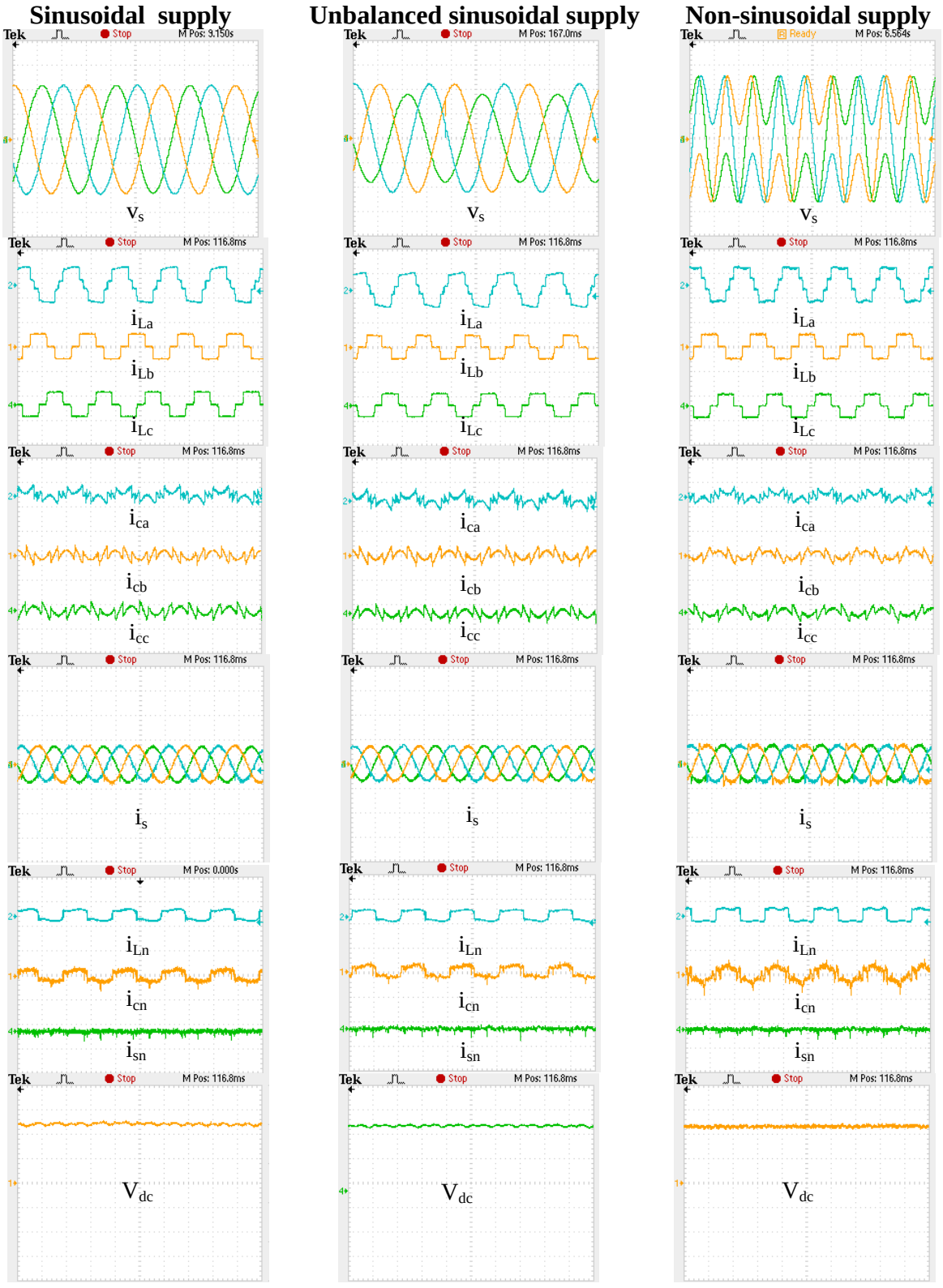


Figure 2.22: Steady state OPAL-RT results of 2C IB APF with unbalanced load using HBCC i_d-i_q control strategy for load current (i_L), filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}), under (a) ideal sinusoidal voltage supply, (b) unbalanced sinusoidal voltage supply, and (c) non-sinusoidal voltage supply

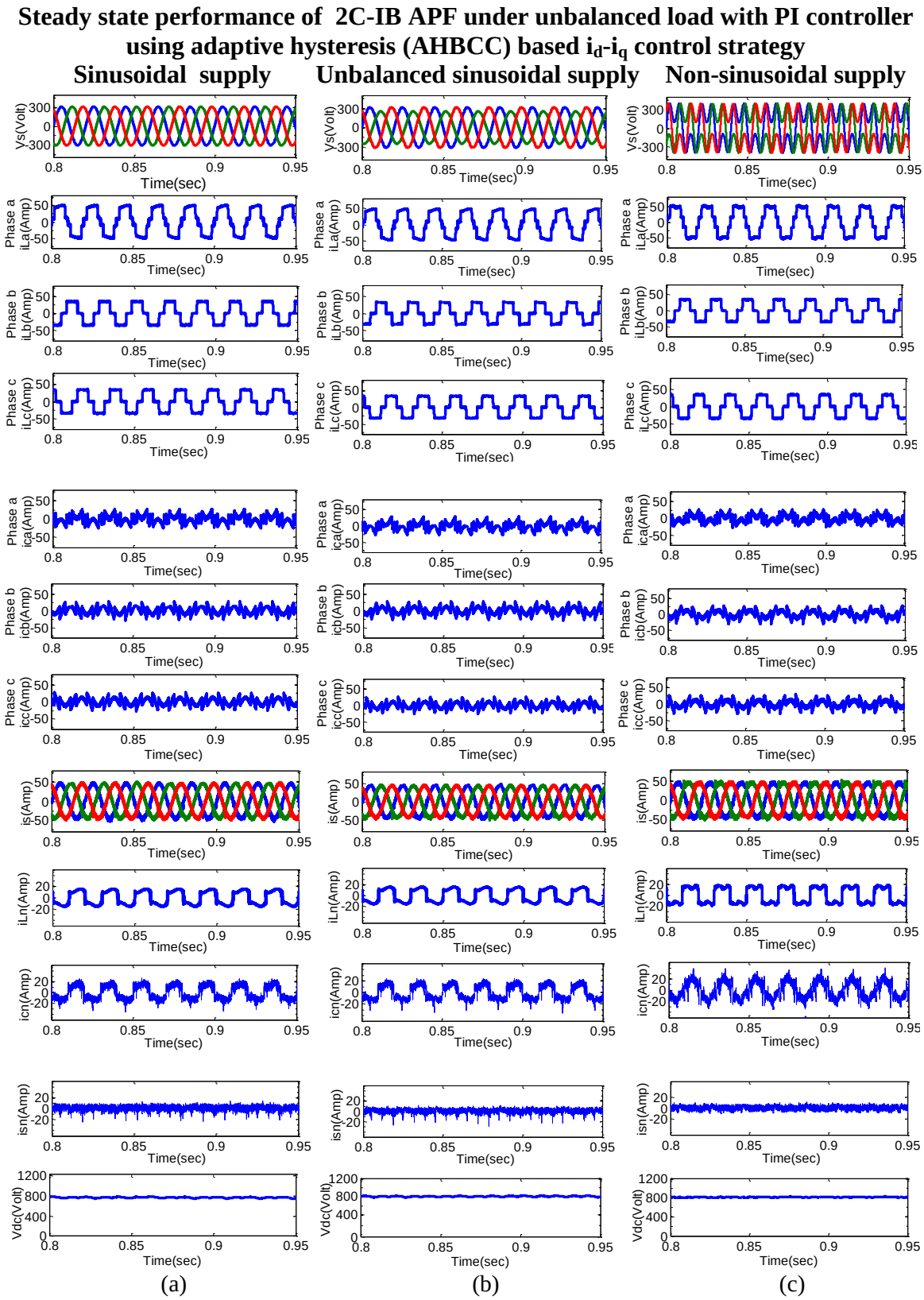


Figure 2.23: Steady state simulation results of 2C IB APF with unbalanced load using AHBCC i_d-i_q control strategy for load current (i_L), filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutralcurrent (i_{sn}), and capacitor voltage (V_{dc}), under (a) ideal sinusoidal voltage supply, (b) unbalanced sinusoidal voltage supply, and (c) non-sinusoidal voltage supply

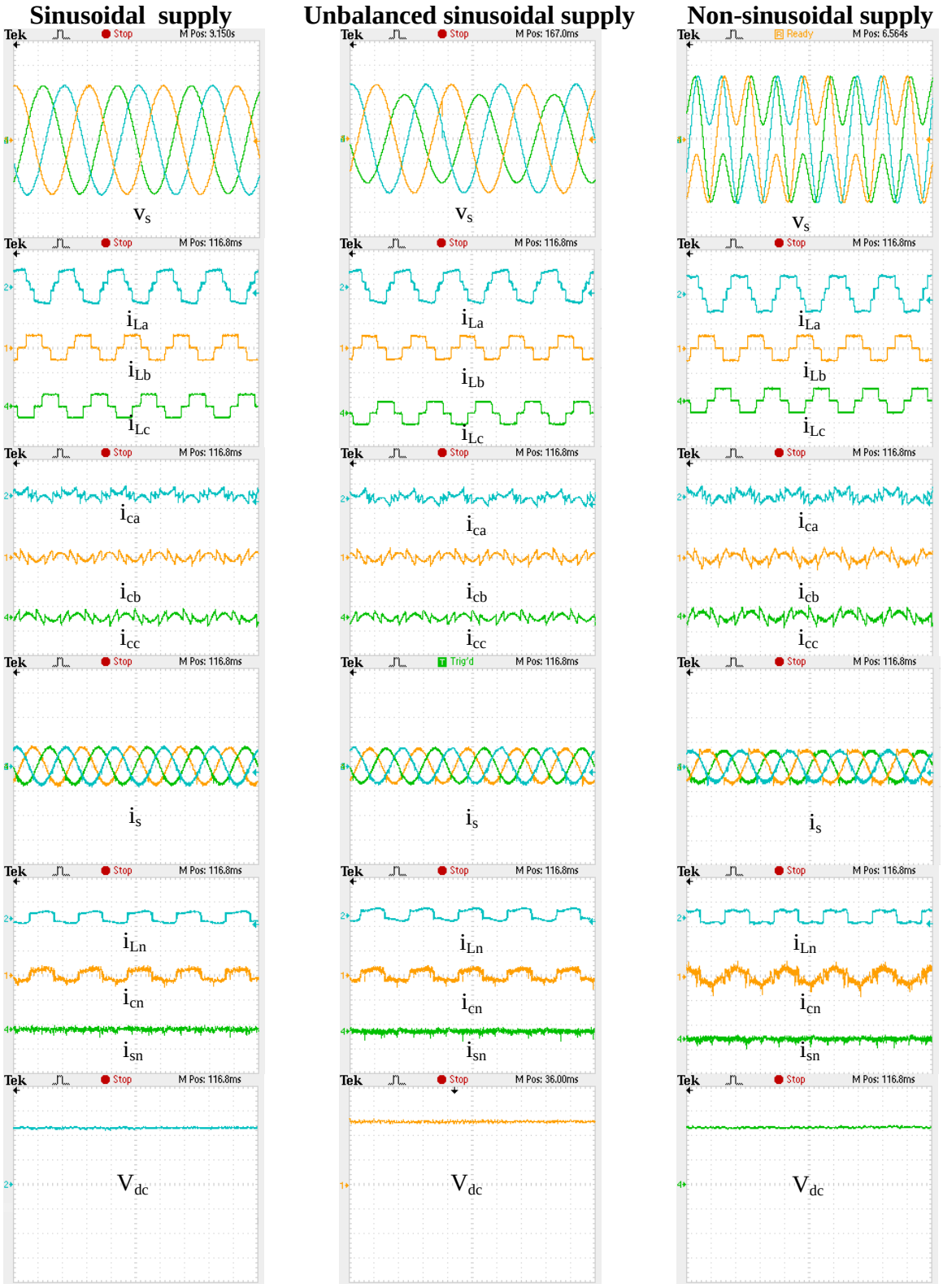


Figure 2.24: Steady state OPAL-RT results of 2C IB APF with unbalanced load using AHBCC i_d-i_q control strategy for load current (i_L), filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}), under (a) ideal sinusoidal voltage supply, (b) unbalanced sinusoidal voltage supply, and (c) non-sinusoidal voltage supply

Table 2.4: Source current THD using conventional hysteresis band current controller (HBCC) p-q control strategy

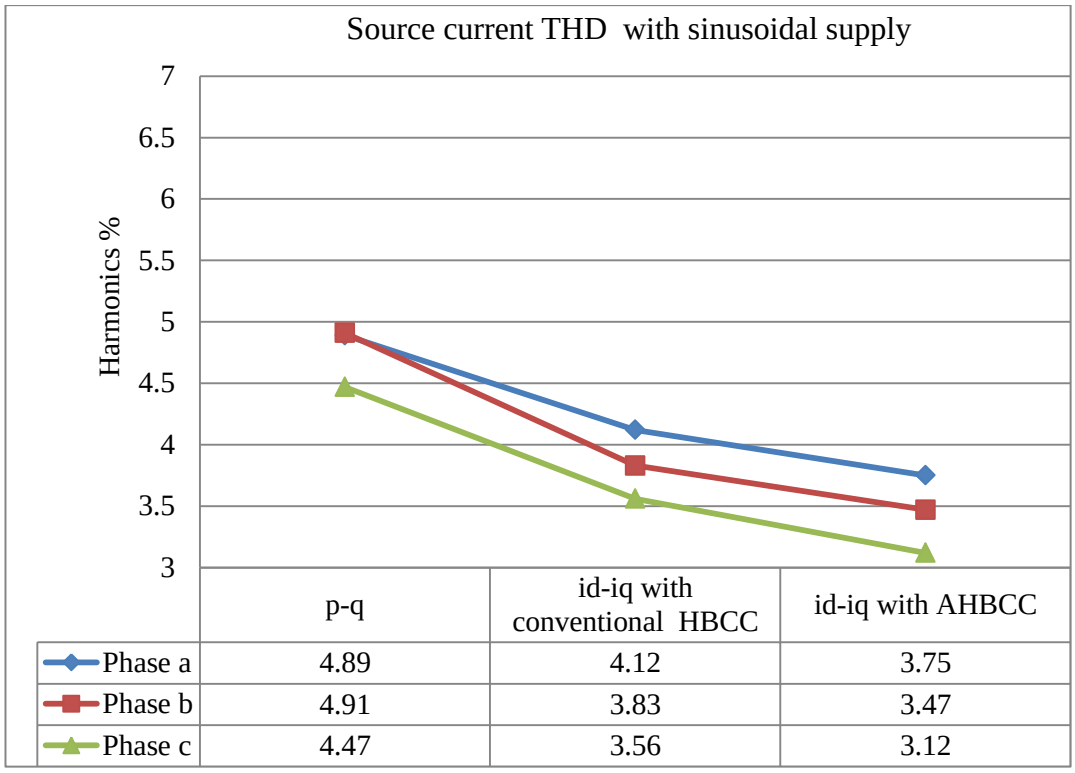
Supply voltage condition	Without APF (THD %)			2C-IB APF (THD %)		
	Ph-a	Ph-b	Ph-c	Ph-a	Ph-b	Ph-c
Sinusoidal supply	20.64	30.66	30.66	4.89	4.91	4.47
Unbalanced sinusoidal supply	21.48	33.36	28.92	6.74	6.63	6.776
Non-sinusoidal supply	22.12	30.96	30.96	8.38	10.16	9.98

Table 2.5: Source current THD using conventional hysteresis band current controller (HBCC) based i_d-i_q control strategy

Supply voltage condition	Without APF (THD %)			2C-IB APF (THD %)		
	Ph-a	Ph-b	Ph-c	Ph-a	Ph-b	Ph-c
Sinusoidal supply	20.63	30.68	30.68	4.12	3.83	3.56
Unbalanced sinusoidal supply	21.44	33.38	28.89	4.75	4.21	3.71
Non-sinusoidal supply	22.13	30.94	30.95	5.69	6.00	5.49

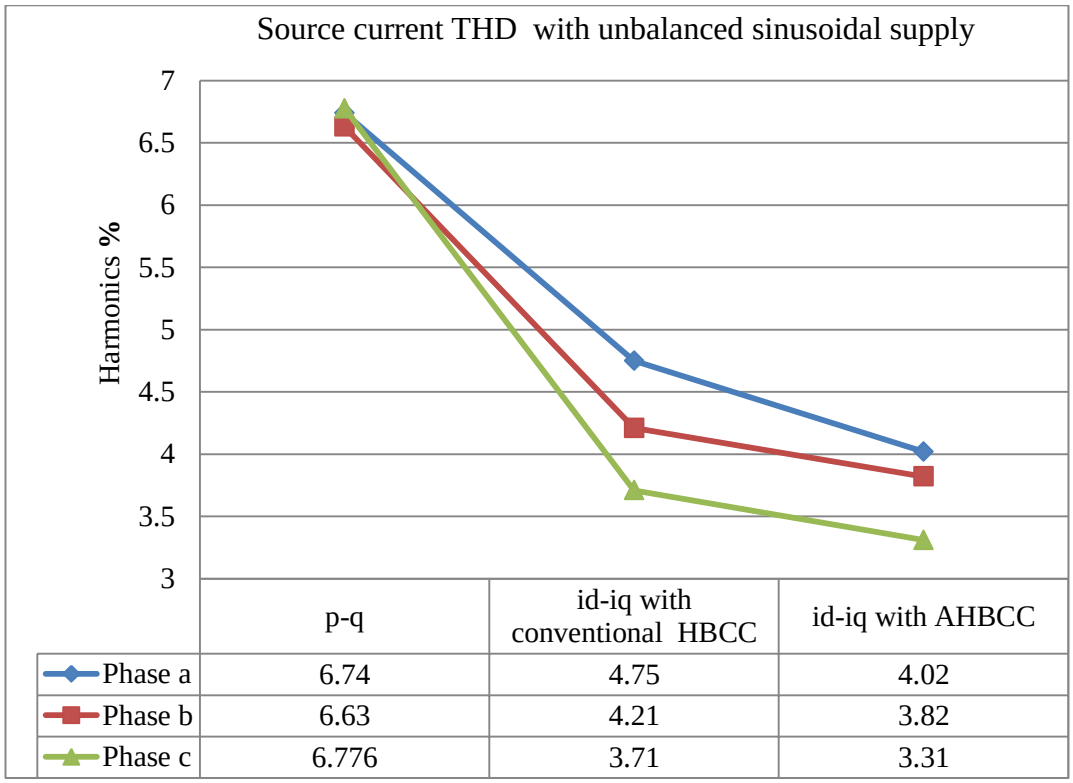
Table 2.6: Source current THD using adaptive hysteresis band current controller (AHBCC) based i_d-i_q control strategy

Supply voltage condition	Without APF (THD %)			2C-IB APF (THD %)		
	Ph-a	Ph-b	Ph-c	Ph-a	Ph-b	Ph-c
Sinusoidal supply	20.65	30.71	30.67	3.75	3.47	3.12
Unbalanced sinusoidal supply	21.49	33. 37	28.91	4.02	3.82	3.31
Non-sinusoidal supply	22.12	30.95	30.97	4.76	4.91	4.42



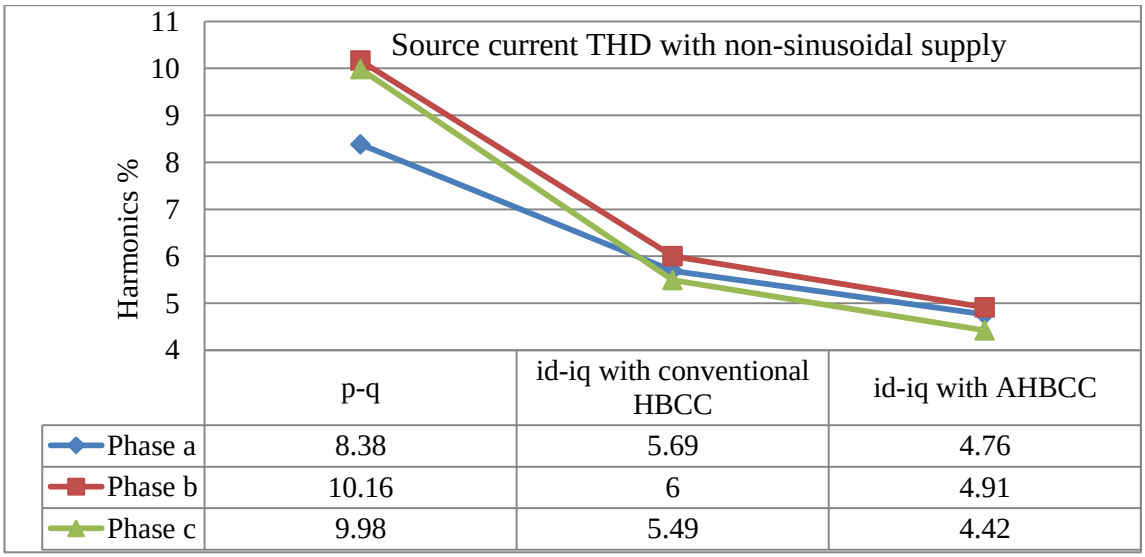
	p-q	id-iq with conventional HBCC	id-iq with AHBCC
Phase a	4.89	4.12	3.75
Phase b	4.91	3.83	3.47
Phase c	4.47	3.56	3.12

Figure 2.25: Chart showing the THD comparison of source current for p-q, i_d-i_q with conventional HBCC and i_d-i_q with AHBCC for sinusoidal voltage source condition



	p-q	id-iq with conventional HBCC	id-iq with AHBCC
Phase a	6.74	4.75	4.02
Phase b	6.63	4.21	3.82
Phase c	6.776	3.71	3.31

Figure 2.26: Chart showing the THD comparison of source current for p-q, i_d-i_q with conventional HBCC and i_d-i_q with AHBCC for unbalanced sinusoidal voltage source condition



	p-q	id-iq with conventional HBCC	id-iq with AHBCC
Phase a	8.38	5.69	4.76
Phase b	10.16	6	4.91
Phase c	9.98	5.49	4.42

Figure 2.27: Chart showing the THD comparison of source current for p-q, i_d-i_q with conventional HBCC and i_d-i_q with AHBCC for non-sinusoidal voltage source condition

Figure 2.18 represents the switching frequency of the 2C IBF power switches (IGBTS) for the adaptive hysteresis band current controller based i_d-i_q control strategy. Figure 2.19 and Figure 2.20 shows the simulation and OPAL-RT lab results for 2C IB APF topology using p-q control strategy with PI controller and conventional hysteresis band current controller PWM scheme respectively for unbalanced load current. Similarly, Figure 2.21 and 2.22 represent the simulation and OPAL-RT lab results for 2C IB APF using i_d-i_q control strategy with the same PI controller and conventional hysteresis band current controller PWM scheme respectively. Figure 2.23 and Figure 2.24 represent the 2C IB APF using PI and adaptive hysteresis band current controller based i_d-i_q control strategy simulation and OPAL-RT lab results respectively. In p-q control strategy with PI and conventional HBCC, the THD of the source currents are well below 5%, according to the IEEE 519 standard after compensation but for unbalanced and non sinusoidal, the source current THDs are below the recommending IEEE standard as can be seen from Table 2.4. The source current THD of 2C IB APF using i_d-i_q control strategy with PI and conventional HBCC in Table 2.5 are well below 5 % for sinusoidal and unbalanced sinusoidal voltage source condition but unable to meet the IEEE 519 recommendations limit during the non-sinusoidal voltage source condition after compensation. Table 2.6 represents the source current THDs after compensation using id-iq control strategy using HBCC; the THDs of the source current are well below in all all the voltage source conditions i.e. sinusoidal, unbalanced sinusoidal voltage source conditions. Finally, the chart presented in Figure 2.25,2.26 and 2.27 describes about the compensation

performance of p-q, i_d-i_q with HBCC and i_d-i_q with AHBCC for sinusoidal, unbalanced sinusoidal and non-sinusoidal voltage source conditions for phase-a, phase b and phase c source currents respectively.

2.7.2 Dynamic State performance discussion with MATLAB and OPAL-RT Results

To realize the dynamic performance of 2C IB APF using i_d-i_q control strategy, for both the conventional HBCC and AHBCC, the following parameters in Table 2.7 has been used in the MATLAB/Simulink and OPAL-RT lab model.

Table 2.7: Simulation condition parameters for dynamic state analysis of 2C IB APF

System parameters	FB-IB APF value
Supply Voltage (RMS)	Vs = 400 V (Line voltage)
Supply Frequency	fs = 50Hz
dc-link capacitance	C_{dc} = 1500 µF
dc-link voltage	V_{dc} = 800 V
APF coupling inductor	L = 600 µH
Non-linear load value	Two 3-phase non-linear load R_1 = 16 Ω and L_1=50 mH connected in parallel and one 1-phase non-linear load R_2 = 16 Ω and L_2 = 50 mH connected with phase-a

Figure 2.28 provides the simulation result of the switching frequency of the IB APF power switches during the dynamic condition. It can be seen that the maximum switching frequency is nearly around 10 kHz. Figure 2.29 and 2.30 shows the simulation and OPAL-RT lab dynamic condition results respectively, of 2C IB APF using conventional HBCC based i_d-i_q control strategy during sinusoidal, unbalanced-sinusoidal and non-sinusoidal voltage source conditions. The simulation and OPAL-RT lab dynamic condition results for 2C IB APF using adaptive hysteresis band current controller has been shown in Figure 2.31 and 2.32 respectively, for sinusoidal, unbalanced sinusoidal and non-sinusoidal voltage source conditions.

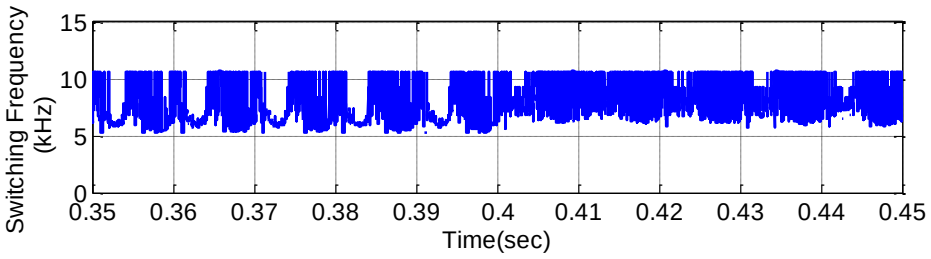
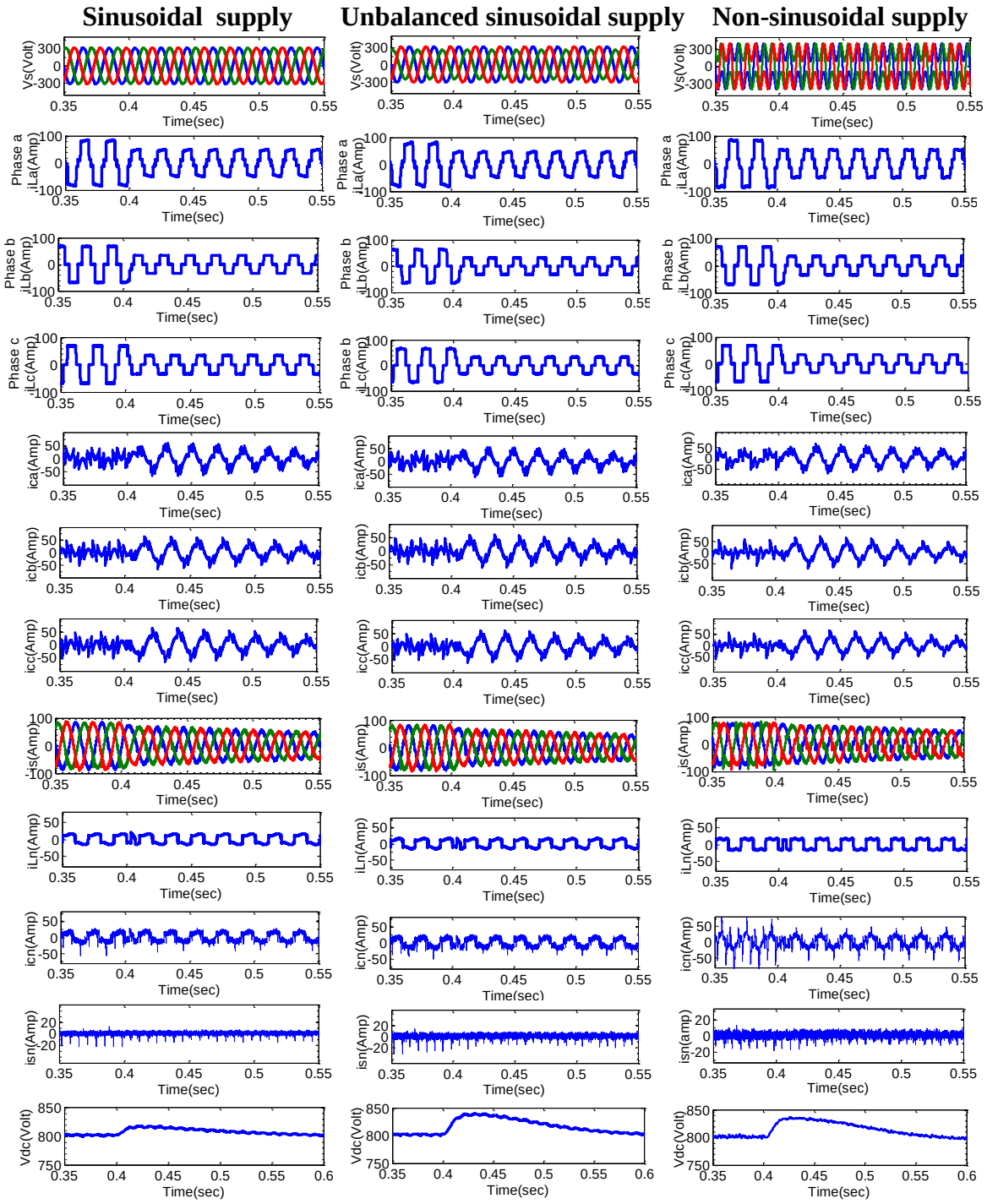


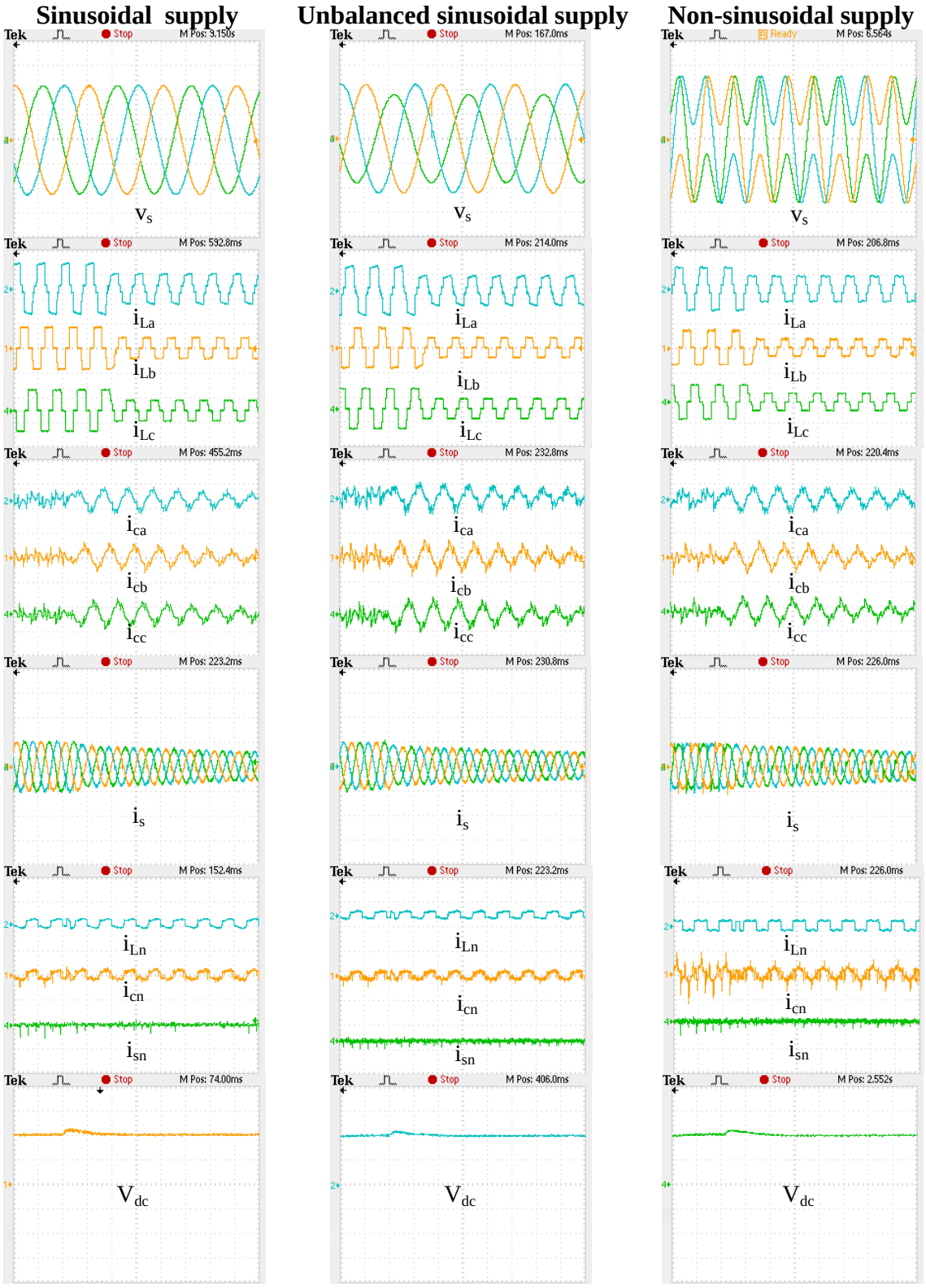
Figure 2.28: Switching frequency of the power switches using adaptive hysteresis band current controller based i_d-i_q control strategy during dynamic state condition

Dynamic Performance of 2C-IB APF under unbalanced load with PI controller and conventional hysteresis band current controller (HBCC) based i_d-i_q control strategy



(a) (b) (c)

Figure 2.29: Dynamic state simulation results of 2C IB APF with unbalanced load using HBCC i_d-i_q control strategy for load current (i_L), filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}), under (a) ideal sinusoidal voltage supply, (b) unbalanced sinusoidal voltage supply, and (c) non-sinusoidal voltage supply



(a) (b) (c)

Figure 2.30: Dynamic state OPAL-RT results of 2C IB APF with unbalanced load using HBCC i_d-i_q control strategy for load current (i_L), filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}), under (a) ideal sinusoidal voltage supply, (b) unbalanced sinusoidal voltage supply, and (c) non-sinusoidal voltage supply

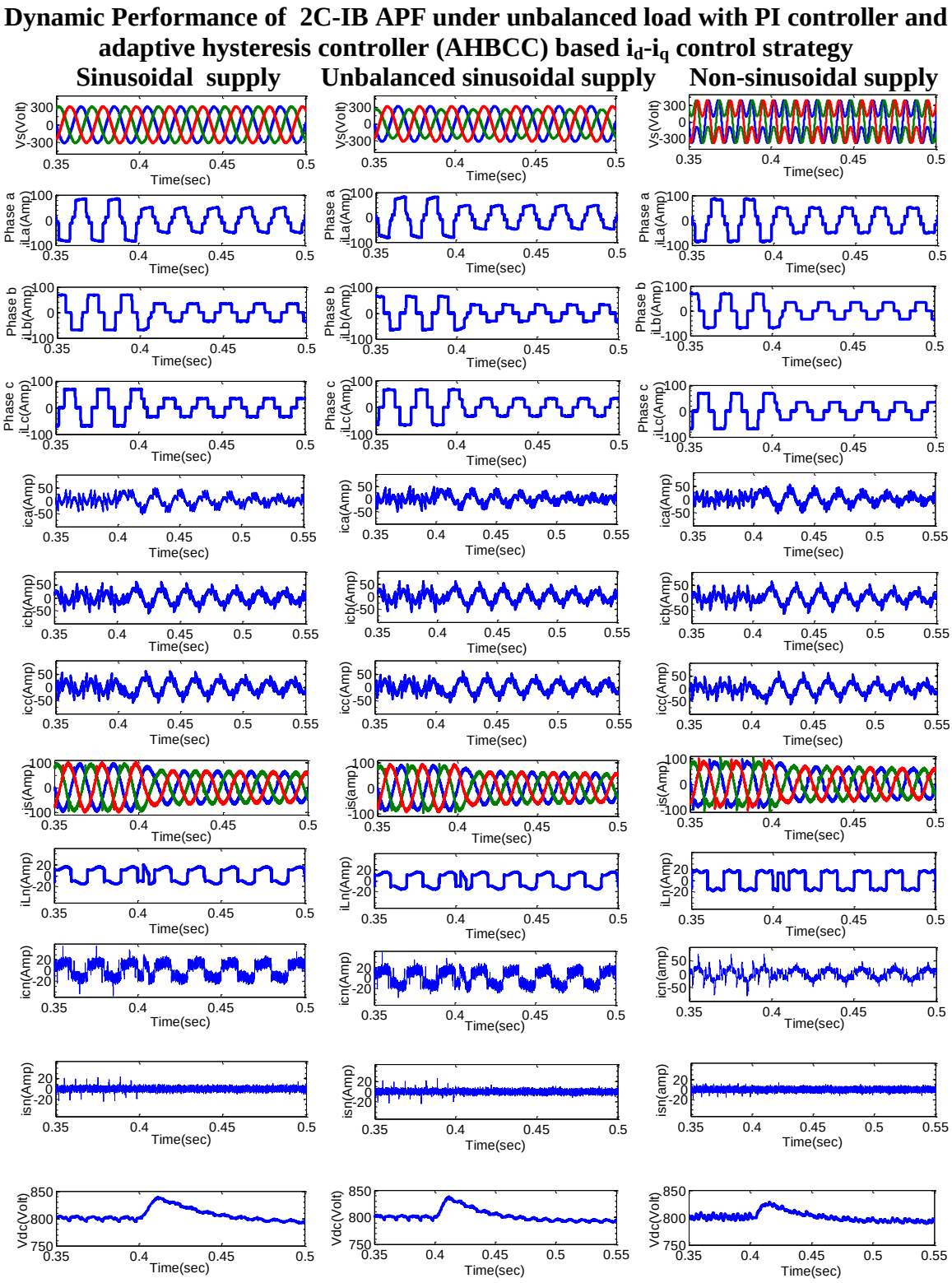
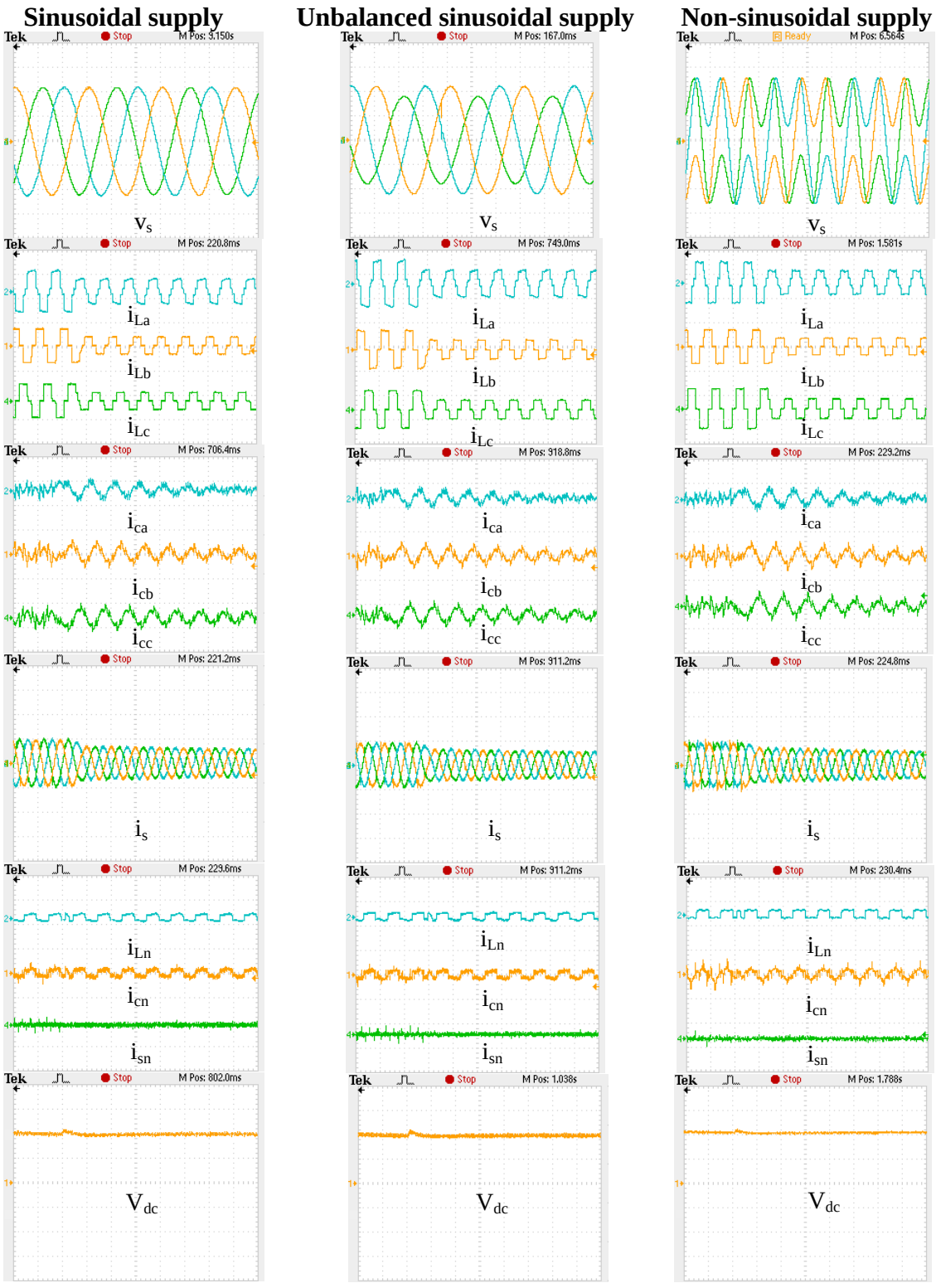


Figure 2.31: Dynamic state simulation results of 2C IB APF with unbalanced load using AHBCC i_d-i_q control strategy for load current (i_L), filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}), under (a) ideal sinusoidal voltage supply, (b) unbalanced sinusoidal voltage supply, and (c) non-sinusoidal voltage supply



(a) (b) (c)

Figure 2.32: Dynamic state OPAL-RT results of 2C IB APF with unbalanced load using AHBCC i_d-i_q control strategy for load current (i_L), filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}), under (a) ideal sinusoidal voltage supply, (b) unbalanced sinusoidal voltage supply, and (c) non-sinusoidal voltage supply

Table 2.8: Source current THD using conventional hysteresis band current controller (HBCC) based i_d-i_q control strategy during dynamic condition

Supply voltage condition	Without APF (THD%)			2C-IB APF (THD%)		
	Ph-a	Ph-b	Ph-c	Ph-a	Ph-b	Ph-c
Sinusoidal supply	20.37	28.77	28.56	4.16	4.63	3.57
Unbalanced sinusoidal supply	20.37	31.41	26.95	4.29	4.87	4.06
Non-sinusoidal supply	20.96	28.89	28.74	8.67	10.67	9.41

Table 2.9: Source current THD using adaptive hysteresis band current controller (AHBCC) based i_d-i_q control strategy during dynamic condition

Supply voltage condition	Without APF (THD%)			2C-IB APF (THD%)		
	Ph-a	Ph-b	Ph-c	Ph-a	Ph-b	Ph-c
Sinusoidal supply	20.44	28.79	28.44	3.53	4.15	3.18
Unbalanced sinusoidal supply	20.86	31.39	26.34	3.77	4.20	3.96
Non-sinusoidal supply	20.63	28.83	28.82	5.12	6.98	5.22

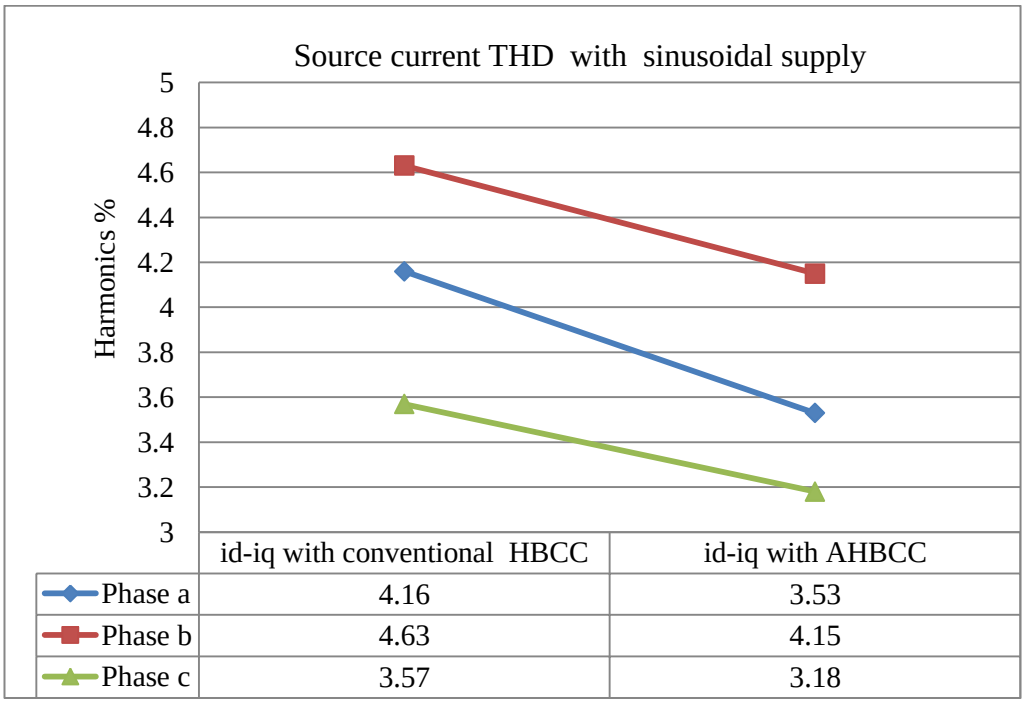
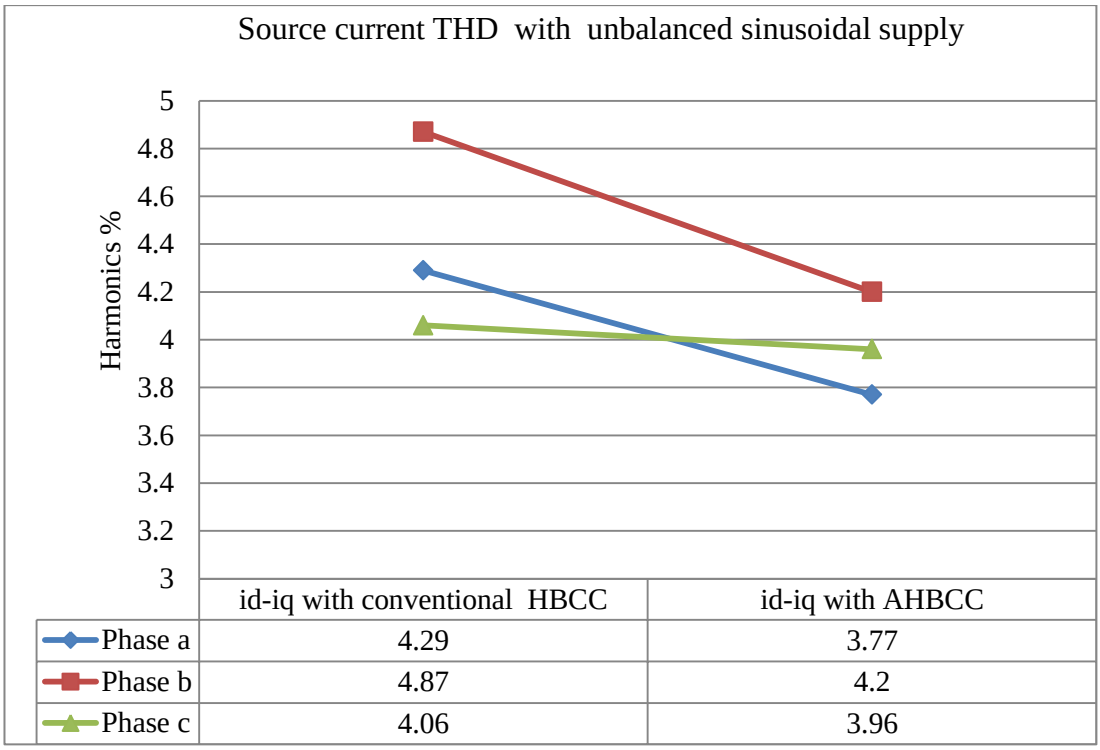
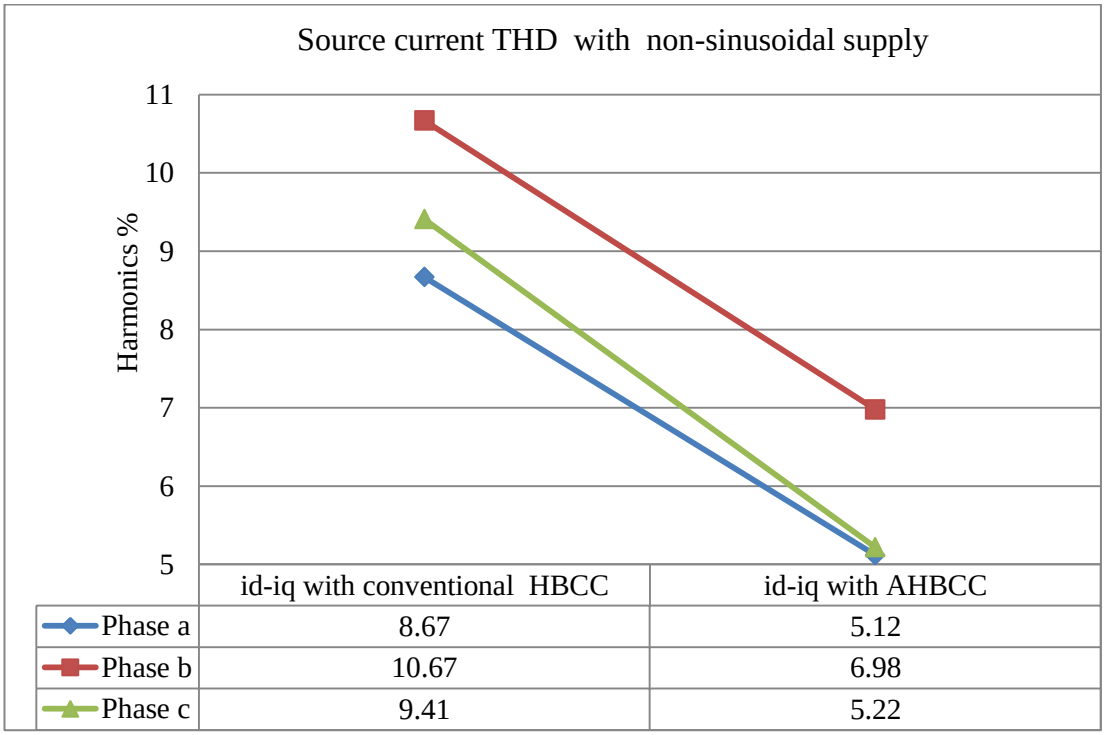


Figure 2.33: Chart showing the THD comparison of source current for i_d-i_q with conventional HBCC and i_d-i_q with AHBCC for sinusoidal voltage source condition



	id-iq with conventional HBCC	id-iq with AHBCC
Phase a	4.29	3.77
Phase b	4.87	4.2
Phase c	4.06	3.96

Figure 2.34: Chart showing the THD comparison of source current for i_d-i_q with conventional HBCC and i_d-i_q with AHBCC for unbalanced sinusoidal voltage source condition



	id-iq with conventional HBCC	id-iq with AHBCC
Phase a	8.67	5.12
Phase b	10.67	6.98
Phase c	9.41	5.22

Figure 2.35: Chart showing the THD comparison of source current for i_d-i_q with conventional HBCC and i_d-i_q with AHBCC for unbalanced nonsinusoidal voltage source condition

The unbalanced load current has been decreased at 0.4 sec. It can be observed that the dc-link voltage as well as the source current and compensating current have less settling time during dynamic condition in case of conventional HBCC as compared to AHBCC controller as can be seen from the simulation results. The disturbance has been created at 0.4 sec and the dc-link voltage is getting settled down at nearly more than 0.6 sec in the conventional HBCC controller where as in case of AHBCC, the dc-link voltage has been settled down at nearly 0.48 sec. with sinusoidal voltage source condition. The similar effects can be seen from the simulation and OPAL-RT result of unbalanced and nonsinusoidal voltage source condition. From results, it can be seen that, the neutral load current is also well compensated and it is better in AHBCC based i_d-i_q control strategy.

The THD of the source current before and after compensation are being tabulated in Table 2.8 and Table 2.9 for 2C IBAPF using i_d-i_q with HBCC and AHBCC for the unbalanced dynamic load condition during various voltage source conditions. The chart illustrated in Figure 2.33, 2.34 and 2.35 shows the dynamic compensation performance of 2C IB APF using i_d-i_q control strategy with conventional HBCC and AHBCC for sinusoidal, unbalanced-sinusoidal and non-sinusoidal voltage source conditions respectively. The adaptive hysteresis band current controller based i_d-i_q control strategy used for 2C IBAPF has better harmonic compensation performance as can be seen from the charts presented for sinusoidal, unbalanced-sinusoidal and non-sinusoidal voltage.

2.8 Summary

In this chapter, an extensive simulation and RTDS hardware analysis of 3-phase 4-wire 2C IB-APF has been done focusing on the inherent elimination of shoot-through current with a good harmonic compensation to the disturbances generated by the non-linear loads. The proposed module contributes the elimination of shoot-through path to improving the reliability of the system. Even though both of the presented control strategies are capable to compensate the harmonics, it is concluded that i_d-i_q has a better performance over p-q control strategy.

Under the sinusoidal supply voltage condition, both the control strategy can provide good compensation, but in non-sinusoidal supply voltage condition p-q control strategy fails to have that much of good compensation. Simulation results show that the “shoot-through”

problem does not exist and dead time can be eliminated in the interleaved buck converter. Thus, some of the important features of the IB APF active filter include:

i. The Shoot-through phenomenon gets eliminated in the interleaved buck converter.
ii. As the shoot-through phenomenon is being eliminated, the reliability of the converter circuit gets increased.
iii. As there is no short circuit current between the two series connected phase switches, the voltage and current stresses get reduced in the particular switch.
iv. As the voltage and current stresses get reduced, the cost of the devices gets reduced and also the cost of snubber circuit/ power circuit get reduced.
v. Further the THD of the source current has been maintained within IEEE-519 standard.

Chapter 3

Performance Analysis of Interleaved Buck Shunt Active Power Filter with Type-1 and Type-2 Fuzzy Logic controller

3.1 Introduction

In Ch-2, development of 2C IB APF and its control strategies p-q and i_d-i_q with PI controller have been discussed for sinusoidal, unbalanced sinusoidal and non-sinusoidal voltage source condition for unbalanced load current. It is concluded that, the PI controller is inefficient for mitigation of harmonics during the unbalanced and non-sinusoidal voltage source condition.

The PI controller used in the 2C IB APF is based on the linearized model and hence unable to react well in dynamic response. Hence, the Fuzzy logic concept comes with the advantage over PI to process the improbable, uncertain and imprecise data and information.

Fuzzy concept mimics the human control logic and designed with mathematical form to represent the vagueness and uncertainty of linguistic problems, thereby obtaining the tools to solve. Intelligent system based on fuzzy logic is the fundamental tool to work with nonlinear complex system modeling.Here, in this chapter, various Type-1 and Type-2 fuzzy membership functions have been tested for the dynamic response of 2C IB APF topology using i_d-i_q control strategy. The various membership functions that have been tested are trapezoidal, triangular and Gaussian and finally evaluated the performance parameters for sinusoidal, unbalanced sinusoidal and non-sinusoidal voltage source condition with unbalanced non-linear load current.

Essentially, the performance parameters have been evaluated in terms of THD compensation and dc-link voltage regulation. The detailed simulation results have been presented using MATLAB/Simulink environment to support the feasibility of the 2C IB APF topology using fuzzy based i_d-i_q control strategy. Again for validation, the system is also implemented on OPAL-RT real time digital simulator and sufficient results are taken for the verification.

This chapter is being organized as: Section 3.2 provides the details of the Type-1 fuzzy logic controller; Section 3.3 gives the details about the Type-2 fuzzy logic controller. Section 3.4 and 3.5 represent the simulation and OPAL –RT Lab results for Type-1 and Type-2 fuzzy logic controller with different membership functions.

3.2 Type-1 Fuzzy Logic Controller (T1FLC)

The fuzzy logic concept was acquainted with by Prof. Lotfi Zadeh [99] in 1965 and soon after [100-127], it becomes an excellent choice for many control system applications as the capability to mimic human logic [101]. A fuzzy controller converts a linguistic control strategy into an automatic control strategy, and fuzzy rules are constructed either by expert or with a knowledge database [93]. Figure 3.1 represents the fuzzy based i_d-i_q control strategy used for 2C IB APF for generating the reference compensating current. The inputs of the fuzzy logic controller are error (E) and change in error (ΔE) which has been deduced from actual dc-link voltage, V_{dc} and reference dc-link voltage, V_{dc}^{*}; whereas the output is i_{d1h}^{+} and is considered as the first harmonic direct current of positive sequence, which is responsible to regulate active power flow within the voltage source interleaved buck inverter and hence the dc-link voltage, V_{dc}.

The following seven fuzzy levels or sets are chosen for better result: NB (negative big), NM (negative medium), NS (negative small), ZE (zero), PS (positive small), PM (positive medium), and PB (positive big) [115]. The fuzzy inference system is a popular computing framework based on the concepts of fuzzy set theory. The fuzzy sets used may be more or less than this particular set (7x7). But here, for this topology (7x7) fuzzy sets have been chosen for excellent regulation in dc-link voltage as related to other sets like (5x5) and (3x3). The (7x7) sets of fuzzy logic controller give the perfect current tracking capability. The more subdivision (9x9) fuzzy sets can also be used, but has the disadvantage to deal with large number of rules and hence the complexity in the design part occurs.

So here the Mamdani fuzzy inference type based FLC characteristics comprise of seven fuzzy sets for each of the two inputs, i.e. error and change in error, seven fuzzy sets for the output with trapezoidal, triangular and Gaussian membership function have been used. The fuzzification gives the corresponding universe of discourse (UOD) of the crisp input variables, performing a scale mapping, implication using the "min" operator, aggregation using the "max" operator, defuzzification using the "centroid of area (COA)" method.

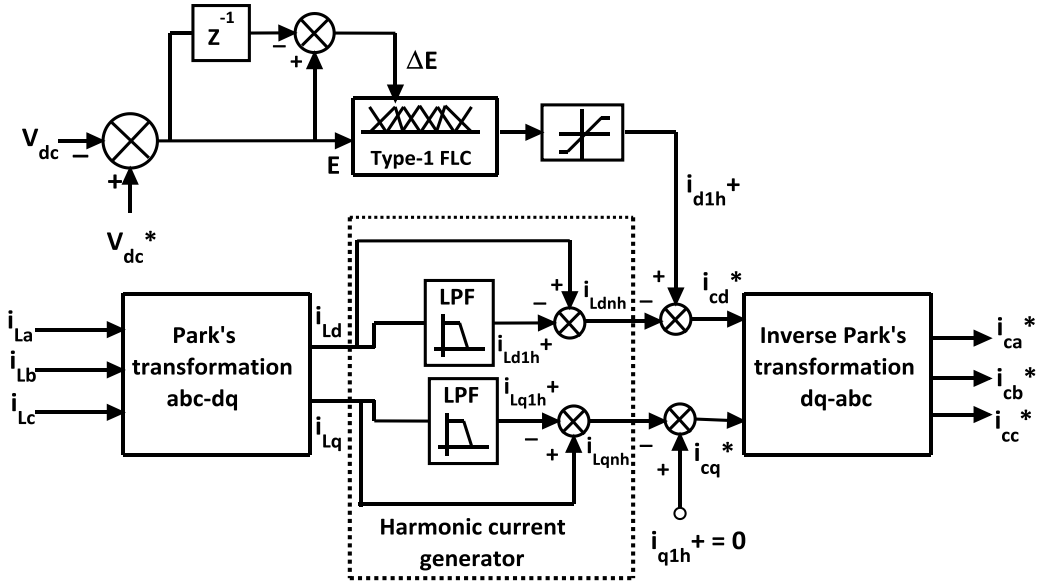


Figure 3.1: Reference current extractions with i_d-i_q method using Type-1 fuzzy logic controller

The control scheme as shown above in Figure 3.1 consists of fuzzy logic controller with a limiter for the generation of reference currents and switching signals [102]. The peak value of the reference current is estimated by adjusting the dc-link voltage. The actual capacitor voltage is compared with the set reference dc voltage. The error signal is then processed through a fuzzy controller, which contributes to the zero steady state error in tracking the reference current signal.

The fuzzy logic block diagram is illustrated in Figure 3.2. This block diagram functions is mainly categorized into the following [104]:

i. Fuzzification
ii. Knowledge base
iii. Fuzzy inference system (FIS)
iv. Defuzzification

A fuzzy system typically consisted of knowledge base and inference system besides the fuzzification and defuzzification as can be seen from the Figure 3.2.

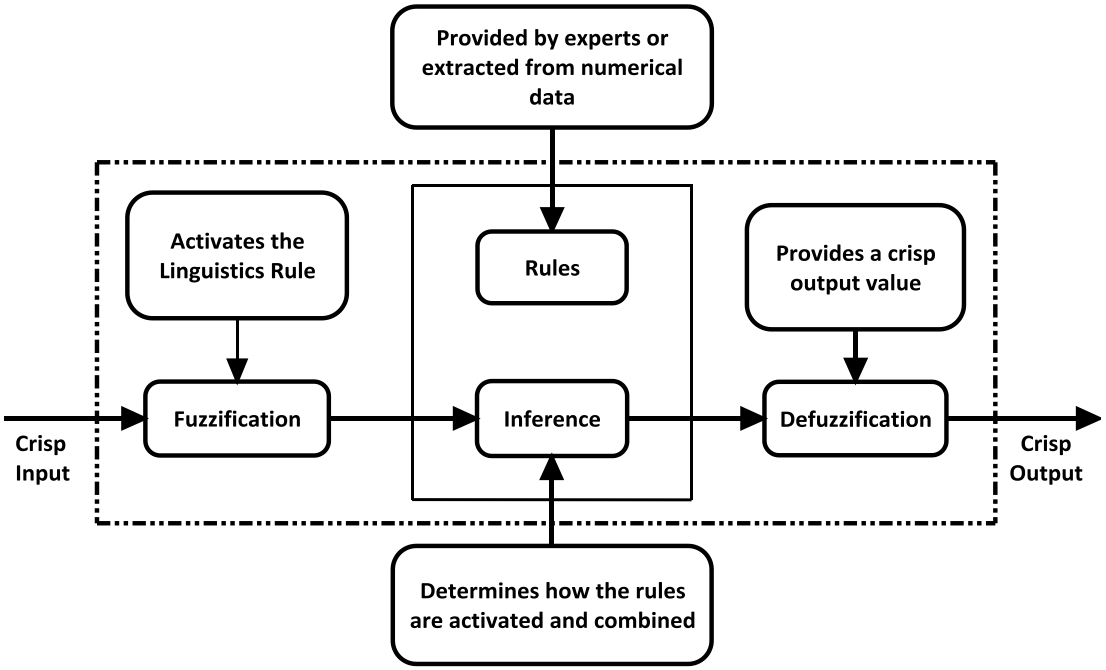


Figure 3.2: Fuzzy logic controller block diagram

The fuzzy data base that comprehends the definitions of the attributes/variables in terms of fuzzy sets and the set of rules which defines the problem, form the knowledge base. The inference system develops the outputs of the system by using the knowledge base and the inputs.

3.2.1 Fuzzification

The fuzzification is considered as the first step in the fuzzy inference system. The fuzzification involves the process of converting the crisp (real) set into fuzzy (linguistic) numbers. In other way, it can be defined as the mapping process of crisp input values to fuzzy sets in the universe of discourse of that input [103]. Again the fuzzy sets can be represented by various membership function curves, but triangular and/or trapezoidal are the most common.

3.2.2 Fuzzy Inference System

The fuzzy inference system (FIS) can be considered as a popular computational framework used by the fuzzy sets [105]. The types of fuzzy inference system are known as Mamdani, Sugeno etc.

Out of Sugeno and Mamdani types of fuzzy controllers, the Mamdani type controller gives a better result for the control of an active power filter (APF), but it has the drawback of a

large number of fuzzy sets and rules [121]. However, the Mamdani fuzzy inference has been used.

Fuzzy inference system (FIS) uses the fuzzy set theory to map the inputs (features in case of fuzzy classification) to the outputs (classes in case of fuzzy classification).

The fuzzy inference process consists of following five steps [110]. They are fuzzification; application of fuzzy operator in the antecedent part of the rule; implication from the antecedent to the consequent; aggregation of the consequents across the rules and finally defuzzification. The linguistic variables of the antecedent part are known as the feature and the consequent part is termed as the class. The typical classification rule that can be applied to fuzzy is expressed in IF E is A_1 and ΔE is B_1 THEN out is C_1 as can be seen in Figure 3.3.

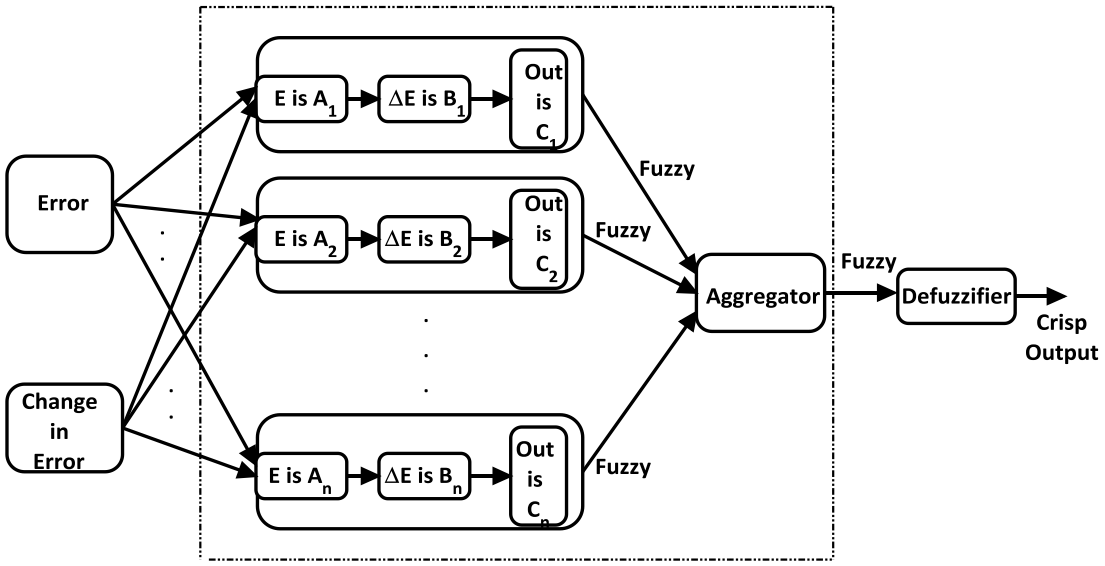


Figure 3.3: A two input Mamdani fuzzy inference system

In Mamdani fuzzy inference system, the following steps have to be followed:

i. Determining of a set of fuzzy rules
ii. Fuzzifying the inputs by using the membership function
iii. Combining the fuzzified inputs according to the rule base for establishing a rule strength
iv. Finding the consequence of the rule, by combining the rule strength and the output membership function
v. Combining the consequences to get the output distribution
vi. Defuzzifying the output distribution if crisp out is required

Fuzzy implications have a great impact on the fuzzy reasoning, allowing for the modeling of intelligent system by plausible inference in the same way as the human reasoning. Again, the Mamdani fuzzy implication models are being used for the assessment of the individual rules. The main two types of implication method, are being used by the fuzzy rules are Mamdani max-min inferencing composition method and Mamdani max-prod inferencing composition method [114].

3.2.2.1 Mamdani max-min Inferencing Composition Method

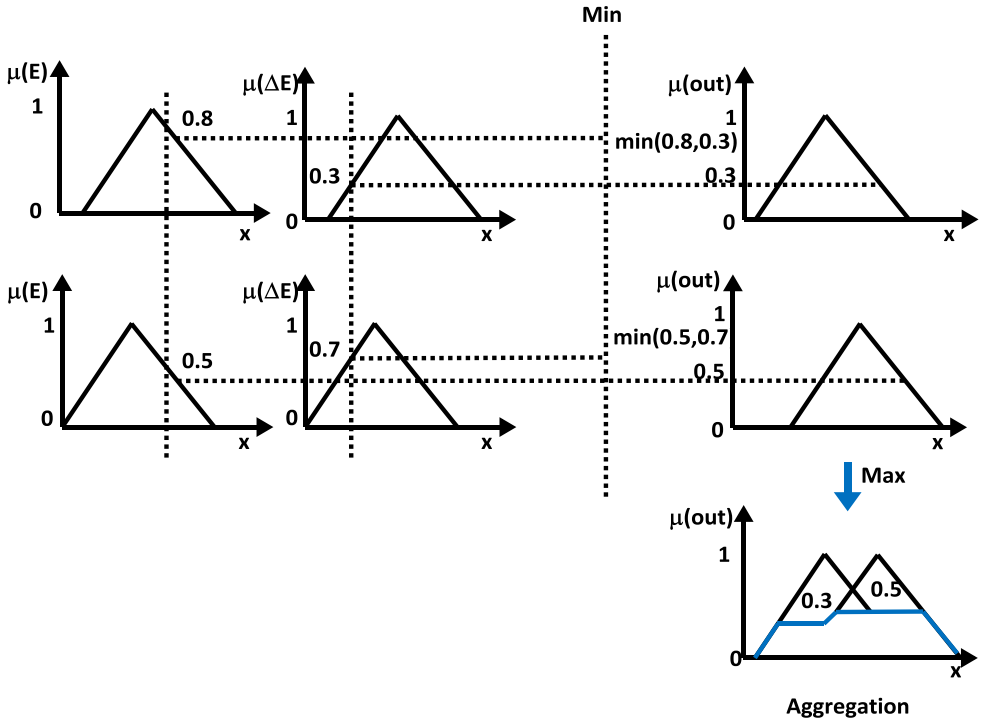


Figure 3.4: A two input Mamdani fuzzy max-min inference system

The Mamdani max-min fuzzy inferencing method is being depicted in Figure 3.4. The fuzzy implication along with aggregation has been used by max-min inferencing method of approximate reasoning. Here aggregation and implication used are maximum operation and minimum operation respectively.

3.2.2.2 Mamdani max-prod Inferencing Composition Method

The Mamdani max-prod fuzzy inferencing composition method is being illustrated in Figure 3.5 [113]. Here the aggregation of maximum operation and the product operation for implication have been used.

The main differences between the Mamdani max-min and prod-max lays with their fuzzy rules and hence in aggregation, and accordingly differ.

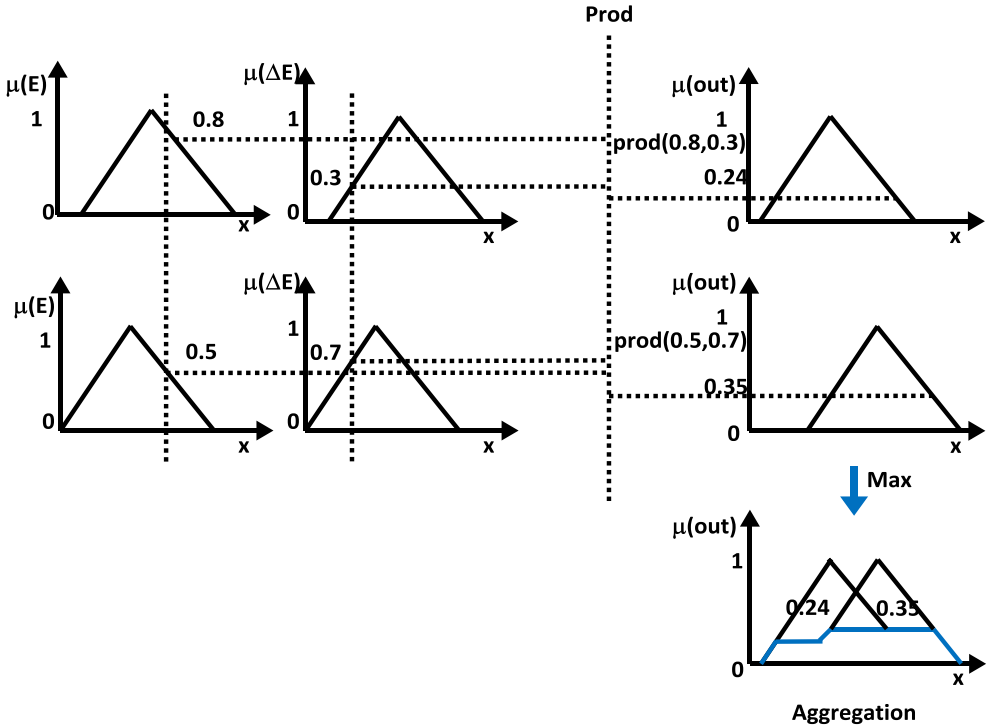


Figure 3.5: A two input Mamdani fuzzy max-prod inference system

3.2.2.3 Aggregation

Hence the implication step evaluates the consequent part of a rule and the contributions are represented in the right of Figure 3.4 and Figure 3.5. When the fuzzy rule base becomes compounded by various rules, then there is a need for aggregation. These individual outputs are aggregated or compounded to get the fuzzy result as shown in the bottom right of the above mentioned figures i.e. Figure 3.5 and 3.6.

3.2.3 Defuzzification

However, followed by the implication and aggregation the output of the fuzzy rules is fuzzy in nature, but according to the real world requirement, the fuzzy output to be crispy and can be defined as;

$$\mu_A(x) = defuzz(x, mf, type) \tag{3.1}$$

Where defuzz$(x, mf, type)$ evaluates the defuzzified or the crispy output of a membership function positioned on an associated variable value x from the aggregated final fuzzy output, followed by the implication method. The various defuzzification methods used to evaluate the crispy output are [114]:

i. Center of Area (COA),

ii. Bisector of Area (BOA),

iii. Mean value of maximum (MOM),

iv. Smallest (absolute) value of maximum (SOM) and

v. Largest (absolute) value of maximum.

In Figure 3.6, the shaded solid area represents the fuzzy aggregated output and the dot represents the defuzzified crisp output. The various defuzzification methods [116] are depicted in Figure 3.7 and are explained in detail in the following sections.

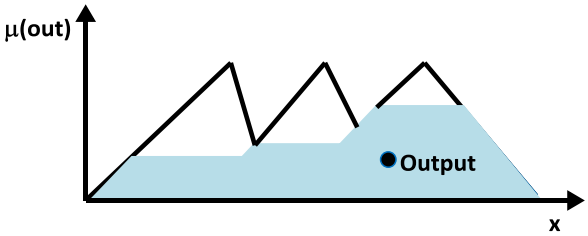


Figure 3.6: Defuzzification

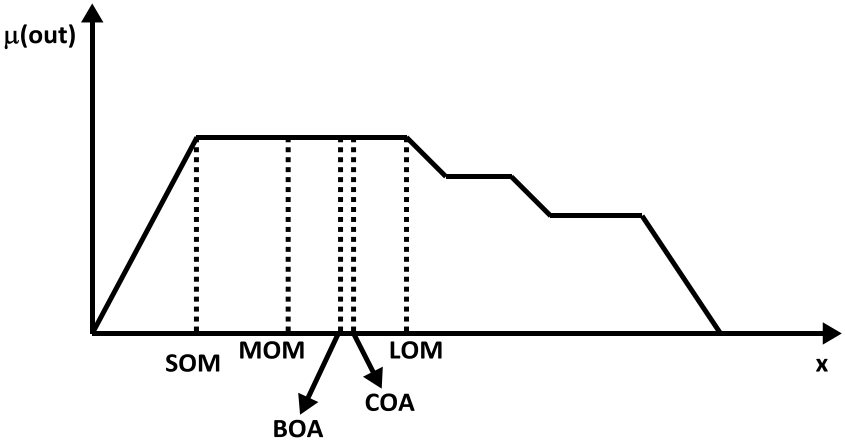


Figure 3.7: Defuzzification methods

3.2.3.1 Center of Area method

The Center of Area (COA) method is also termed as the Center of gravity [117]. This method is very well-known and is often used in spite of a certain amount of complexity in the calculation part. The mathematical formula used for the calculation of crisp value using COA as:

$$COA = \frac{\int_a^b x\, \mu_A(x) dx}{\int_a^b \mu_A(x)\, dx} \tag{3.2}$$

Where *x* variable is defined to be the geometric center of the aggregated fuzzy output or output variable and $\mu_A(x)$ is being made by the unions of all the contributions of the fuzzy rules or aggregated membership functions.

With a discretized universe of discourse (UOD), the COA expression can be denoted as:

$$COA = \frac{\int_a^b x_i \, \mu_A(x_i) dx}{\int_a^b \mu_A(x_i) \, dx} \tag{3.3}$$

It is to be noted in this method that, the overlapping areas of two or more contributing rules after aggregation are counted once.

3.2.3.2 Bisector of Area method

The Bisector of Area (BOA) method represented as the bisector line which gives the division of two sub regions having equal area. The bisector line sometimes coincident with the center line of COA, but not always. The mathematical expression that defines the BOA method is represented as:

$$\int_{\alpha}^{X_{BOA}} \mu_A(x) dx = \int_{X_{BOA}}^{\beta} \mu_A(x) dx \tag{3.4}$$

3.2.3.3 Mean, Smallest and Largest of Maximum methods

The mean of maximum (MOM) defuzzification method computes the average of those aggregated fuzzy output values that have the highest degrees [118].

One of the shortcomings of the MOM method is that, it does not consider the entire shape of the aggregated output membership function, and only consider the highest degree points in that membership function. The expression for the defuzzification, by using the mean of maximum (MOM) as:

$$X_{MOM} = \frac{\int_{X'} x \, dx}{\int_{X'} dx} \tag{3.5}$$

Where $X' = \{ x; \ \mu_A(x) = \mu^* \}$

The other two methods, i.e. smallest of maximum (SOM) and largest of maximum (LOM) along with mean of maximum (MOM), key off the maximum value assumed by the aggregate MF. In case of unique maximum by the aggregate MF, then MOM, SOM, and LOM takes the same value only.

The fuzzy logic controller used in the proposed topology is characterized as following

i. Seven fuzzy sets of input and output
ii. Fuzzification using continuous universe of discourse (UOD)
iii. Implication using Mamdani's min operator
iv. Defuzzification using centroid of area (COA)

3.2.4 Design of Control Rules

The rule base is being constructed to control the output variable of the fuzzy logic controller [119]. The fuzzy rule is nothing but the if-then rule by a condition and a conclusion. Hence followed by the inference system with rule base, output membership function is calculated. The rule design of fuzzy logic controller involves the process to relate the input variables by the model output properties. The design of the FLC is principally based on the intuitive feelings and the process experience; as FLC is not dependent on the system model [120]. The rules are expressed in a language like English with linguistic variables. The syntax used in the rule design process as, IF {X is error, E and Y is change in error, ΔE} THEN {Z is control output}.

To have better performance control, finer fuzzy petitioned subspaces are used [122,123]. The finer petitioned subspaces in the fuzzy, that have used in the modelled topology are zero (Z), negative small (NS), positive small (PS), negative medium (NM), positive medium (PM), negative big (NB) and positive big (PB). These seven membership functions are valid for the error, E and change in error ΔE input variables as well for the output variable and are being characterized for triangular, trapezoidal and Gaussian membership function [103].

A membership function (MF) is a curve that defines how the values of a fuzzy variable in a certain region are mapped to a membership value or (degree of membership) between 0 and 1. The used MFs are described elaborately in the following subsections. The variables universe of discourse (UOD) is expressed in per unit values.

Fuzzy sets have been chosen based on the error of the dc-link capacitor voltage. The other possible membership function like 3×3 or 5×5 can also be used in the dc-link voltage regulation, but unable to meet dc-link voltage constant and hence error develops with the reference dc-link voltage. Due to this dc-link voltage error difference, there may not be good harmonic compensation by the control strategy [56]. With the use of 7×7 MFs, the shunt active power filter is capable of maintaining the constant dc-link voltage nearly equal to the reference dc-link voltage.

3.2.4.1 Trapezoidal Membership Function

The trapezoidal curve [115] shown in Figure 3.8 can be represented as the function of x and four scalar vectors a, b, c and d;

$$\mu_A(x) = \begin{Bmatrix} 0 & if\ x \le a \\ \frac{x-a}{b-a} & if\ a \le x \le b \\ 1 & if\ b \le x \le c \\ \frac{c-x}{c-b} & if\ c \le x \le d \\ 0 & if\ x \ge d \end{Bmatrix} \quad (3.6)$$

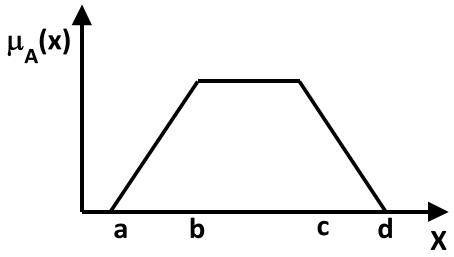


Figure 3.8: Trapezoidal membership function

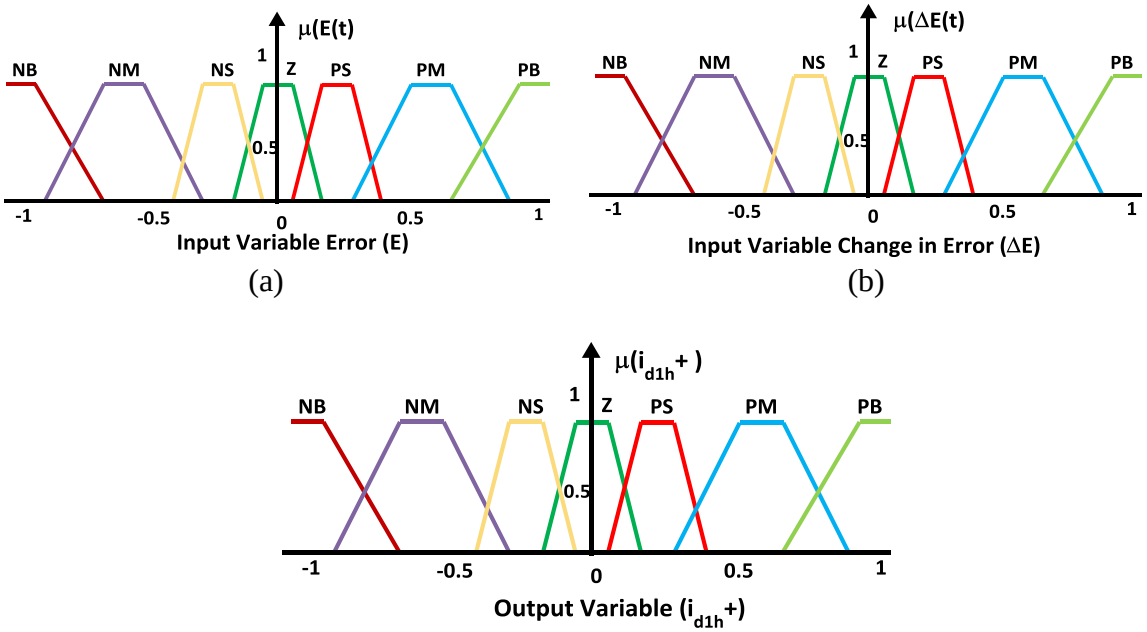


Figure 3.9: Normalized trapezoidal membership function for dc-link voltage control (a) Input variable error, E (b) Input variable change in error, ΔE (c) Output variable, i_{d1h}^{+}

The trapezoidal membership can also be expressed as:

$$\mu_A(x) = max\left(min\left(\frac{x-a}{b-a}, 1, \frac{d-x}{d-c}\right), 0\right) \quad (3.7)$$

where the parameters a and d trace the "foot" and the points b and c trace the "shoulders of the trapezoid. Figure 3.9 depicted the 7×7 normalized trapezoidal membership function for input variable error, E, change in error, ΔE of dc-link voltage and output variable, i_{d1h}^{+}, first harmonic direct current of positive sequence.

3.2.4.2 Triangular Membership Function

An MF can have different shapes and out of them, triangular MF is simplest and, most commonly used as shown in Figure 3.10.

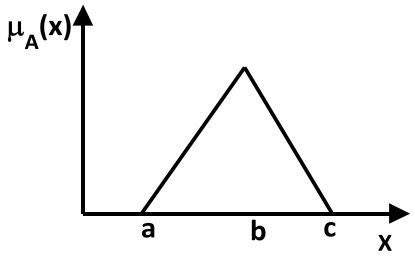


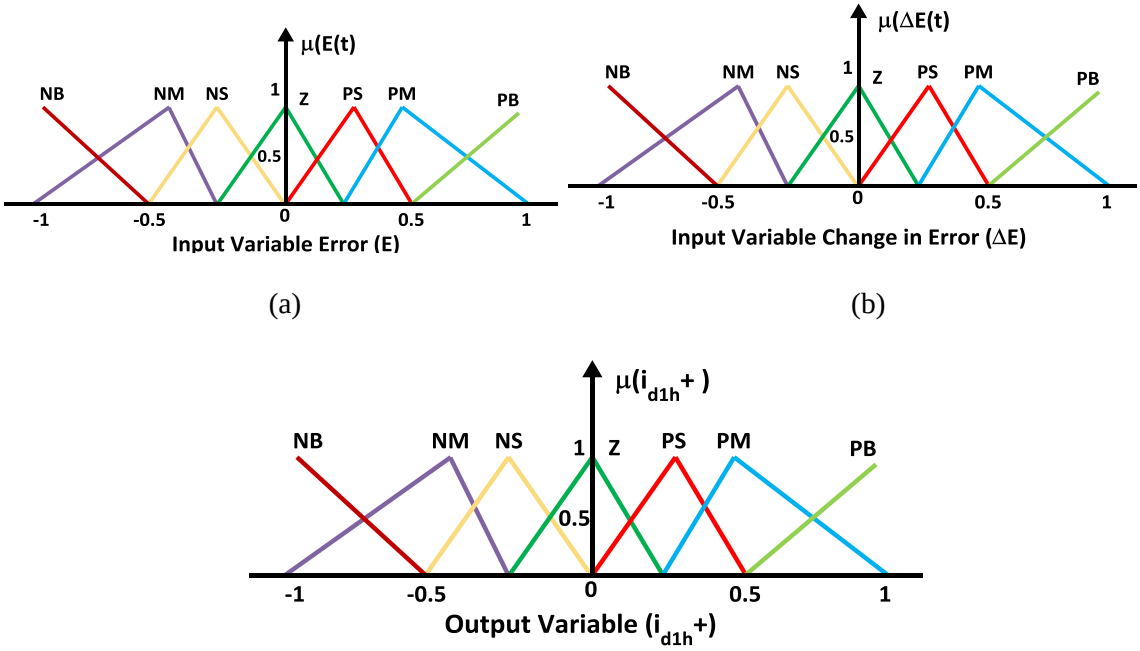
Figure 3.10: Triangular membership function

The triangular curve is a function of a vector, x, and depends on three scalar parameters a, b, and c, as given by

$$\mu_A(x) = \begin{cases} 0 & if\ x \le a \\ \frac{x-a}{b-a} & if\ a \le x \le b \\ \frac{c-x}{c-b} & if\ b \le x \le c \\ 0 & if\ x \ge c \end{cases} \tag{3.8}$$

The triangular membership function can also be depicted as:

$$\mu_A(x) = max\left(min\left(\frac{x-a}{b-a}, \frac{c-x}{c-b}\right), 0\right) \tag{3.9}$$



(a) (b)

(c)

Figure 3.11: Normalized triangular membership function for dc-link voltage control (a) Input variable error, E (b) Input variable change in error, ΔE (c) Output variable, i_{d1h}^{+}

Figure 3.11 shows the normalized triangular membership functions used for the reference current generation where the inputs are error, E and change in error, ΔE of dc-link voltages and the output i_{d1h}^{+}, first harmonic direct current of positive sequence.

3.2.4.3 Gaussian Membership Function

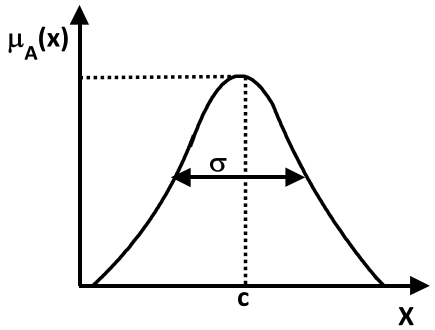


Figure 3.12: Gaussian membership function

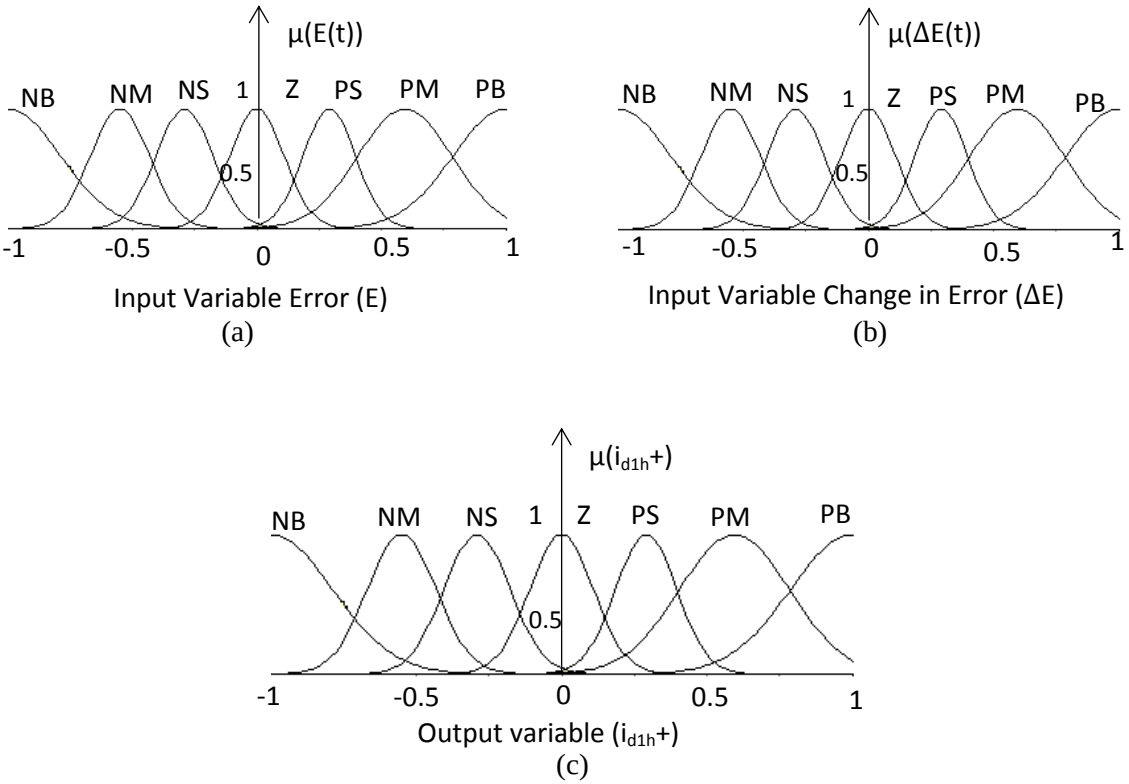


Figure 3.13: Normalized Gaussian membership function for dc-link voltage control (a) Input variable error, E (b) Input variable change in error, ΔE (c) Output variable, i_{d1h}^{+}

Figure 3.12 illustrates the Gaussian membership function. This membership curve is a function of vector x and three scalar parameters c, center, σ, width and m, the fuzzification factor. Hence, by taking these parameters, the Gaussian membership function can be defined as:

$$\mu_A(x,c,s,m) = exp\left[-\frac{1}{2}\left|\frac{x-c}{\sigma}\right|\right]^m \quad (3.10)$$

Figure 3.13 shows the normalized Gaussian membership functions

3.2.4.4 Rule Base

As there are seven membership functions chosen for inputs as error, E and change in error, ΔE, and hence 7×7=49 matrix rules are possible. Based on this, the elements of the rule table are obtained as shown in Table 3.1

Table 3.1: Rule base

ΔE / E	NB	NM	NS	Z	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	Z
NM	NB	NB	NB	NM	NS	Z	PS
NS	NB	NB	NM	NS	Z	PS	PM
Z	NB	NM	NS	Z	PS	PM	PB
PS	NM	NS	Z	PS	PM	PB	PB
PM	NS	Z	PS	PM	PB	PB	PB
PB	Z	PS	PM	PB	PB	PB	PB

The Type-1 fuzzy inference result by MATLAB/Simulation for dc-link voltage regulation is presented in Figure 3.14, 3.15 and 3.16 for trapezoidal, triangular and Gaussian membership functions respectively. The major five graphical tools to build, edit and observe fuzzy inference systems in a fuzzy logic tool box are:

i. Fuzzy inference system (FIS) editor,
ii. Membership function (MF) editor,
iii. Rule editor,
iv. Rule viewer and
v. Surface viewer

The FIS editor gives the information about having the numeral of inputs and output variable with the description of their name. The shapes for all the MF of each variable are defined by the membership function editor. It controls over the change of name, type, and parameters (shape) of each MFs.

Once the rule matrix is governed, it is fairly easy to form the rules by rule editor and the rules can be edited as desired. Out of various logical connectives of rules that is AND, OR, and NOT, here AND has been implemented.

The rule viewer and surface viewer are read only tool [104,115]. The rule viewer shows the contribution of each rule and also gives information about the total fuzzy output with the corresponding defuzzified output. Once the fuzzy algorithm is developed, the surface viewer permits to see the mapping relation between the input and output variables in two or three dimensional form.

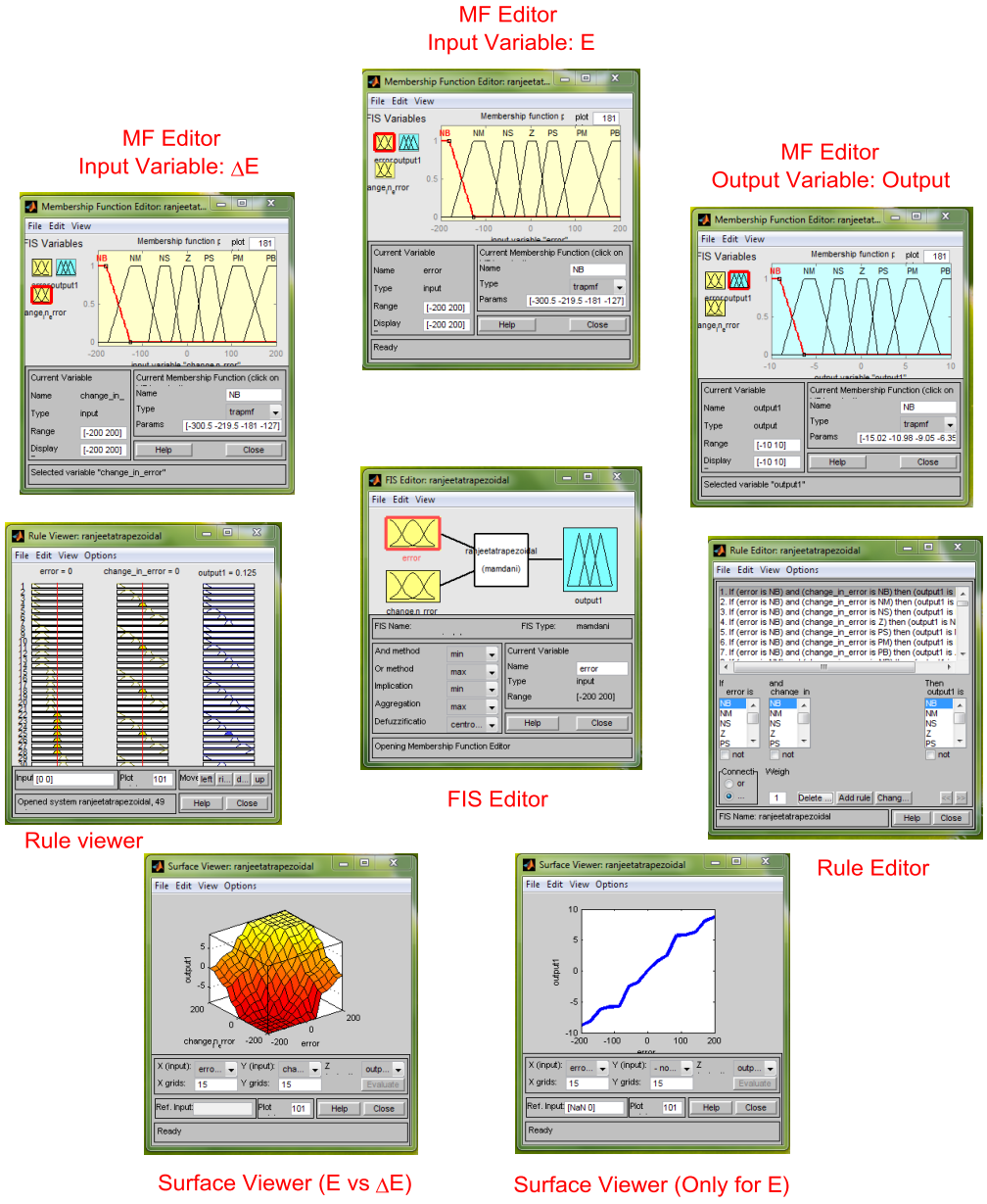


Figure 3.14: Matlab based Type-1 fuzzy inference system with trapezoidal membership function

One of the main issues in fuzzy set is the determination of the membership functions. The membership functions define the fuzzy set and may take any form, but some common examples are there in real applications. The users may choose the membership functions arbitrarily or depending on their experiences, perspectives, etc., or may apply the machine learning methods like genetic algorithm or neural network.

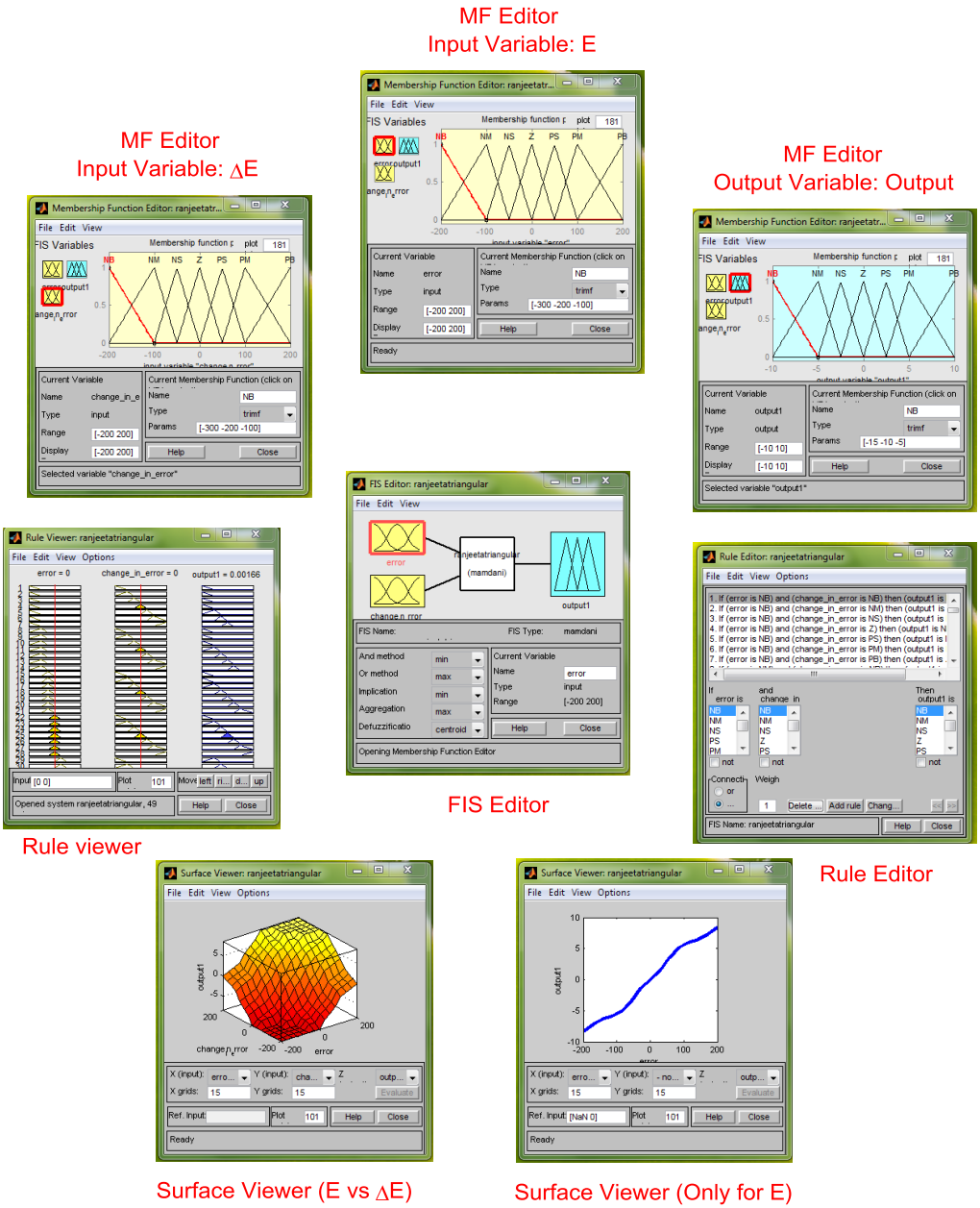


Figure 3.15: Matlab based Type-1 fuzzy inference system with triangular membership function

The numerous membership functions are available like triangular, trapezoidal, Gaussian, bell shaped and etc. Here trapezoidal, triangular, and Gaussian MFs have been considered in the analysis of the proposed 3-phase 4-wire i_d-i_q based split capacitor (2C) interleaved buck active power filter.

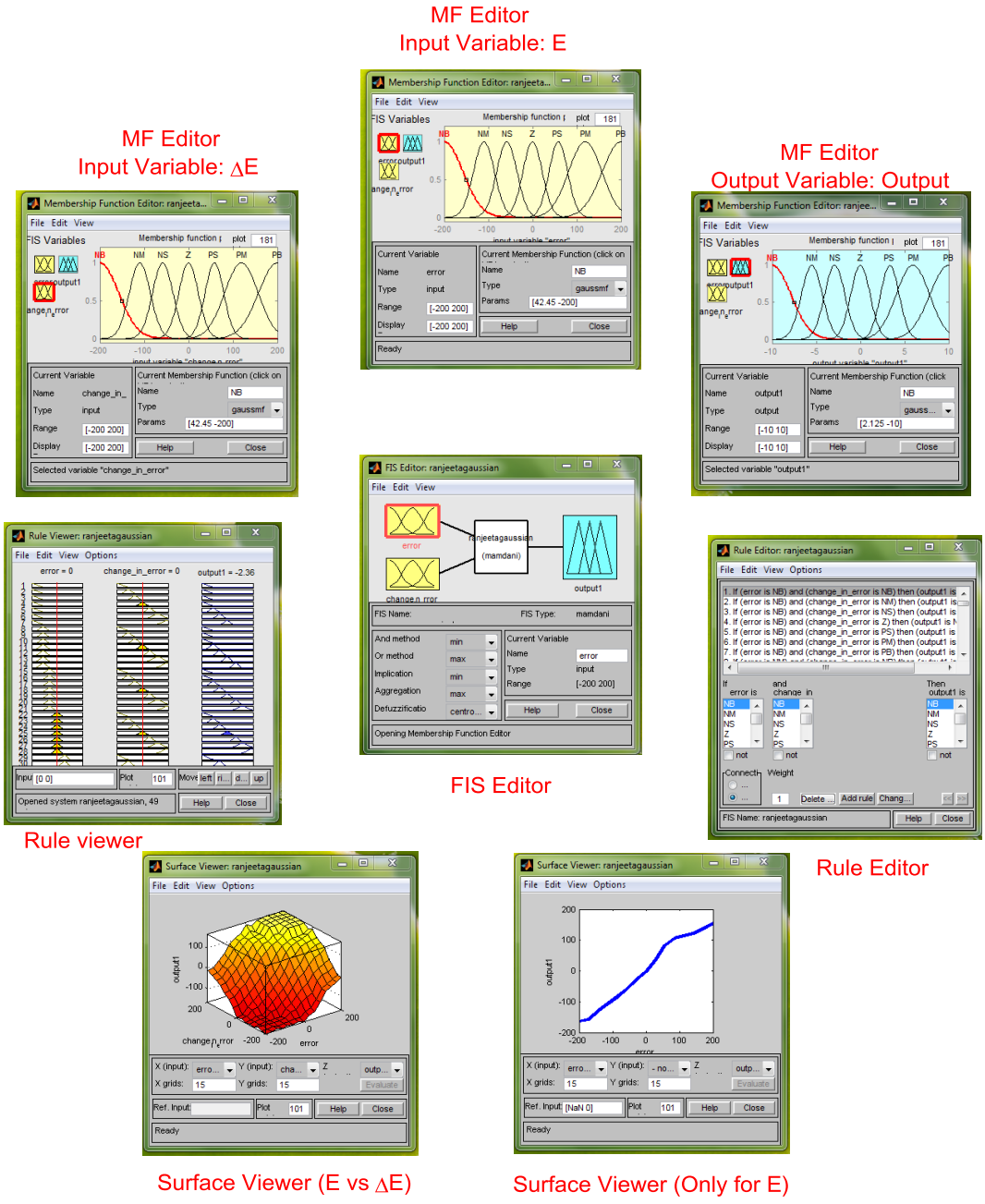


Figure 3.16: Matlab based Type-1 fuzzy inference system with Gaussian membership function

3.3 Type-2 Fuzzy Logic Controller (T2FLC)

The concept of Type-2 fuzzy logic controller (T2FLC) was also introduced by Lotfi A. Zadeh as an extension to Type-1 fuzzy logic controller (T1FLC) [128]. With the introduction of T2FLC of the capability for handling uncertainty, the use of T2FLC has attracted the researchers much significance in the latest years. The Type-2 fuzzy set is defined by the grades of fuzzy membership function, that is grade of each element of membership function is also a fuzzy set characterized in [0,1]; unlike the Type-1 fuzzy

logic controller where the grade of the membership function is a crisp number in [0,1] [107]. The Type-2 fuzzy set membership functions are three-dimensional, including the foot-print of uncertainty, FOU which is the third dimension of the fuzzy sets. This foot-print of uncertainty provides an additional degree of freedom to handle the uncertainties of the model [124-131]. During the evaluation process, the various sources of uncertainty are found [132] and the five sorts of uncertainty emerging by the imprecise natural state are as follows:

i. Uncertainty of measurement: This is the error taking place on the observed quantities.
ii. Uncertainty of process: This uncertainty of process is the dynamic randomness
iii. Uncertainty of Model: This is due to the wrong specification in the model structure
iv. Uncertainty of estimate: This uncertainty of estimate appears due to any of the previous uncertainties or by their combination and known as the imprecision or inexactness.
v. Uncertainty of implementation: This is being due to the variability resulting from sorting politics that is the inability to meet the exact strategic objective.

However, it has recently been given away that, the additional degree of freedom in Type-2 fuzzy controller due to FOU to produce output is not possible with the same number of Type-1 membership functions. Each T2FLC input and output fuzzy sets are embedded by a large number of Type-1 fuzzy sets and the use of large numbers of Type-1 fuzzy sets give a detailed description of the analytical control surface. The additional levels of classification provide greatly smooth control surface with good response [135-140].

3.3.1 Structure of Type-2 Fuzzy Logic Controller (T2FLC)

From Figure 3.18, it is clear that structurally T2FLC is very similar to T1FLC shown in Figure 3.17, and also consists of the components as: fuzzifier, rule base, inference system and output processing unit which comprises of type reducer and defuzzifier. Similar to Type-1 FLC, the fuzzifier maps the crisp input into Type-2 fuzzy sets [149-150].

The type reducer produces the Type-1 fuzzy sets and the defuzzifier gives the crisp output. Usually, the T2FLC has been characterized by intense computation due to the high computational loads at the type reducing phase. To simplify the computation, the secondary MFs may be set 0 or 1and is known as Interval Type-2 fuzzy logic controller [109].

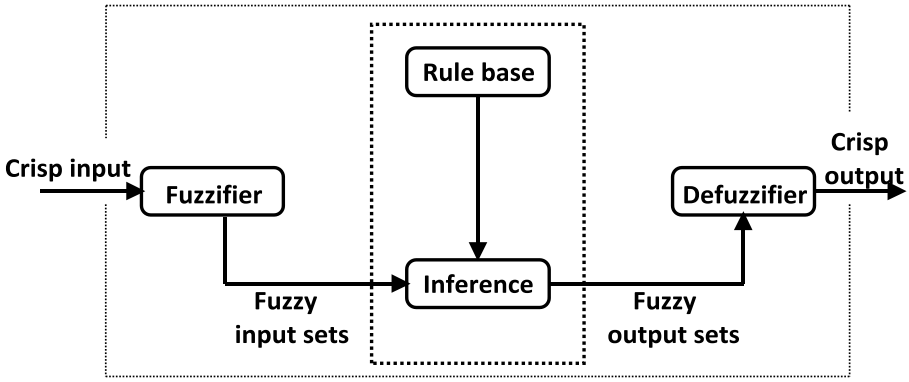


Figure 3.17: Type-1 fuzzy logic controller architecture

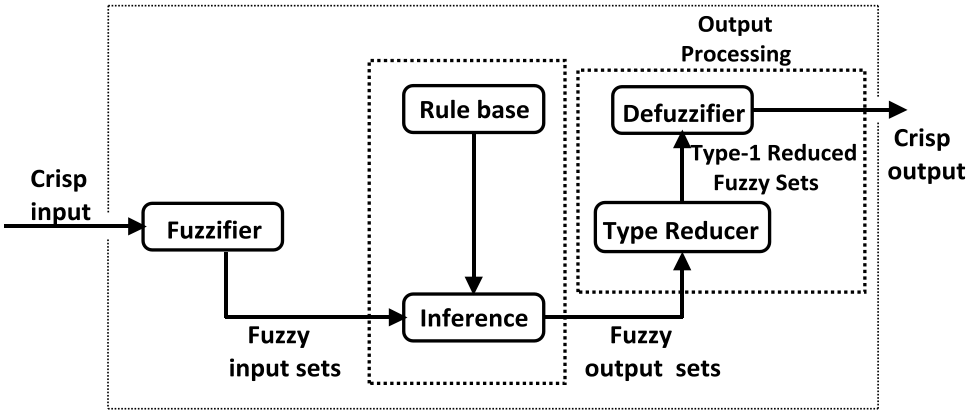


Figure 3.18: Type-2 fuzzy logic controller architecture

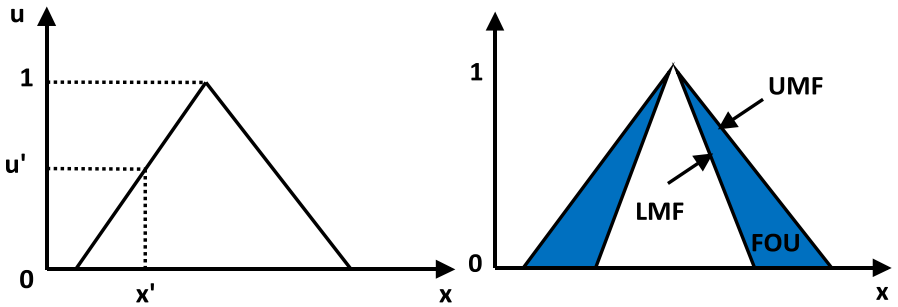


Figure 3.19: (a) Type-1 fuzzy logic membership function (b) Type-2 fuzzy logic membership function

The Type-1 fuzzy sets based on the fact that the membership function is crisp and means the degrees of the MF is fully crisp not the fuzzy [151]. Hence, the membership grade of each element in the Type-1 fuzzy set is crisp number in [0,1], as depicted in Figure 3.19a. The Type-2 fuzzy membership function shown in Figure 3.19b is characterized by three dimension membership with a foot-print of uncertainty, FOU.

For Type-2 FLC design, the similar configuration has been chosen as that of Type-1 FLC [153]. The number of inputs is two i.e. error, E and change in error, ΔE and one output variable with seven membership functions for each input/output. Here, the Mamdani fuzzy inference system has been implemented. The operation is same as a Type-1 fuzzy system; however, in the Type-2 fuzzy system, the operation is implemented at two Type-1 membership functions [154,155], and limiting the FOU, between the lower membership function (LMF) and upper membership function (UMF) [156, 157].

It is worth to be noted that the Type-2 fuzzy sets are being embedded by large numbers of Type-1 fuzzy sets [150]. The Type-1 fuzzy set is represented by A and the membership grade of x∈X in A is $\mu_A(x)$, and is a crisp number in [0, 1]; the Type-2 fuzzy set is $\tilde{A}$ in the set X with the membership grade [152] of x∈X is $\mu_{\tilde{A}}(x)$, which is a Type-1 fuzzy set in [0,1].

The Type-2 fuzzy set is represented by $\tilde{A}$ is being characterized by the Type-2 membership function and is represented by $\mu_{\tilde{A}}(x,u)$, in which x∈X and u $\in J_x \subseteq$ [0,1], that is,

$$\tilde{A} = \left\{\left((x,u), \mu_{\tilde{A}}(x,u)\right) \middle| \forall\, x \in X, \forall u \in J_x \subseteq [0,1]\right\} \tag{3.11}$$

where, $0 \leq \mu_{\tilde{A}}(x,u) \leq 1$

The $\tilde{A}$ can also be uttered as

$$\tilde{A} = \int_{x\in X} \int_{u\in J_x} \mu_{\tilde{A}}(x,u)/(x,u) \qquad J_x \subseteq [0,1] \tag{3.12}$$

In the equation (3.12), the $\iint$ signifies union over all acceptable *x* and *u*. The same can be represent for discrete universe of discourse, by replacing the $\int$ into $\sum$.

$\tilde{A}$ can be reuttered as:

$$\tilde{A} = \int_{x\in X} \mu_{\tilde{A}}(x)/(x) = \int_{x\in X} \left[\int_{u\in J_x} f_x(u)/u\right]/x \qquad J_x \subseteq [0,1] \tag{3.13}$$

The internal structure of the control strategy Type-2 fuzzy based i_d-i_q control strategy used for the 3-phase 4-wire split capacitor interleaved buck active power filter (2C IB APF) is depicted in Figure 3.20. The control scheme consists of Type-2 Fuzzy logic controller to control the dc-link voltage which is very much essential to get the harmonic compensation in a well manner. Here also, the analysis has been done for triangular, trapezoidal and Gaussian membership function.

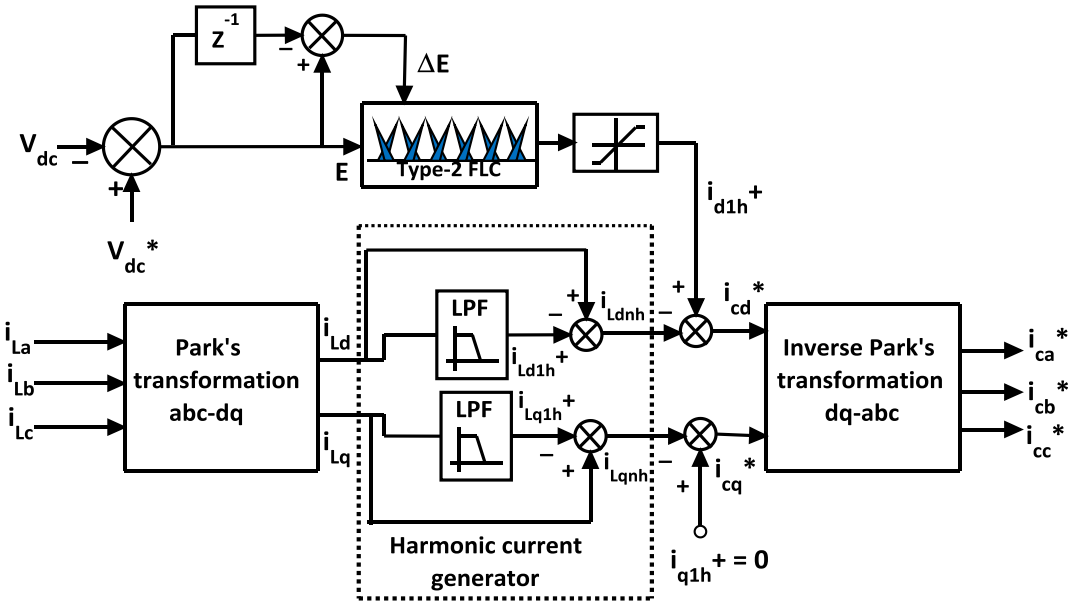


Figure 3.20: Reference current extractions with i_d-i_q method using Type-2 fuzzy logic controller

3.3.2 Fuzzy Inference System of Type-2 FLC

The Type-2 fuzzy inference system (T2FIS) is represented by:

i. Type-2 fuzzy inference system editor
ii. Type-2 fuzzy membership function editor
iii. Type-2 fuzzy rule editor
iv. Type-2 fuzzy rule viewer
v. Type-2 fuzzy reduced surface viewer

The Matlab based Type-2 fuzzy inference system for different membership functions that have been used with the i_d-i_q control strategy for reference compensating current generation [150]. The various Type-2 fuzzy inference system implementing trapezoidal, triangular and Gaussian membership functions is depicted in Figure 3.21, 3.22 and 3.23 respectively.

The design description of the Type-2 fuzzy inference system is given as:

i. Two input variables (error, E and change in error, ΔE) one output variable
ii. Membership function type (trapezoidal, triangular and Gaussian etc.)
iii. Seven membership function for each variable
iv. 7×7= 49 fuzzy inference rules
v. Implication method (Mamdani max-min method)
vi. Defuzzification method (Centre of area)

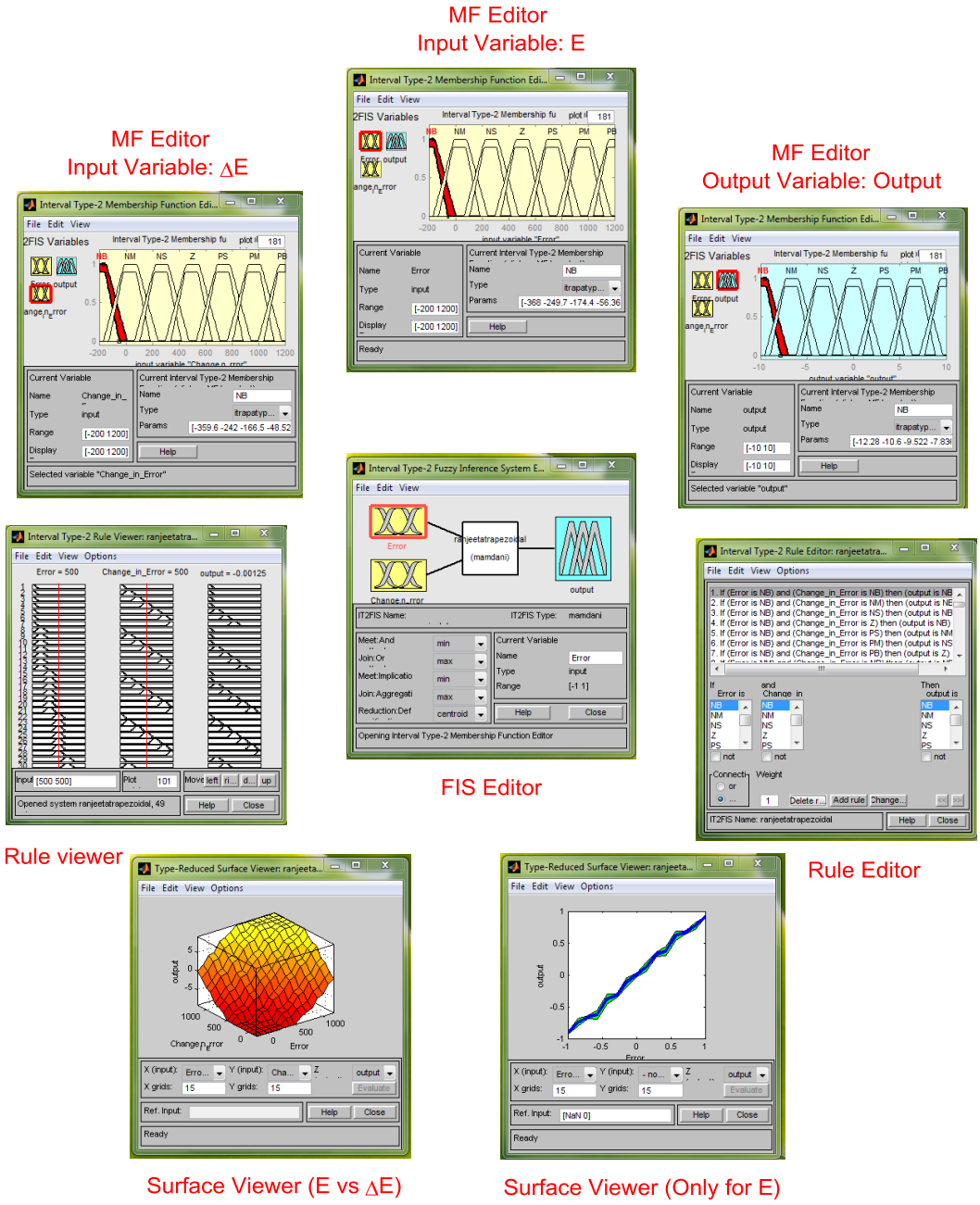


Figure 3.21: Matlab based Type-2 fuzzy inference system with trapezoidal membership function

The Type-2 fuzzy inference system editor handles the high level issues like the number of input and output variables, their names. However, there is no limitation on the number of inputs; it is only managed by the available memory of the personal computer (PC). But, if the number of input or number of MF is too large, then it may be difficult to analyse the Type-2 FIS by other GUI tools.

The Type-2 membership function editor defines the shape of membership functions of each particular variable. The Type-2 rule editor is used to edit the rules and hence gives the behaviour of the systems.

The Type-2 rule viewer and reduced surface viewer are only for looking purpose. These are not editable and they are strictly read-only-tools. The rule viewer is a Matlab based display and may be used as a diagnostic, which gives the information about the active rules and the effect of individual membership function's shape on the results.

The surface viewer displays the dependency of any output towards the one or two of the inputs by the plot of the output surface map of the system as shown in Figure 3.21, 3.22 and 3.23.

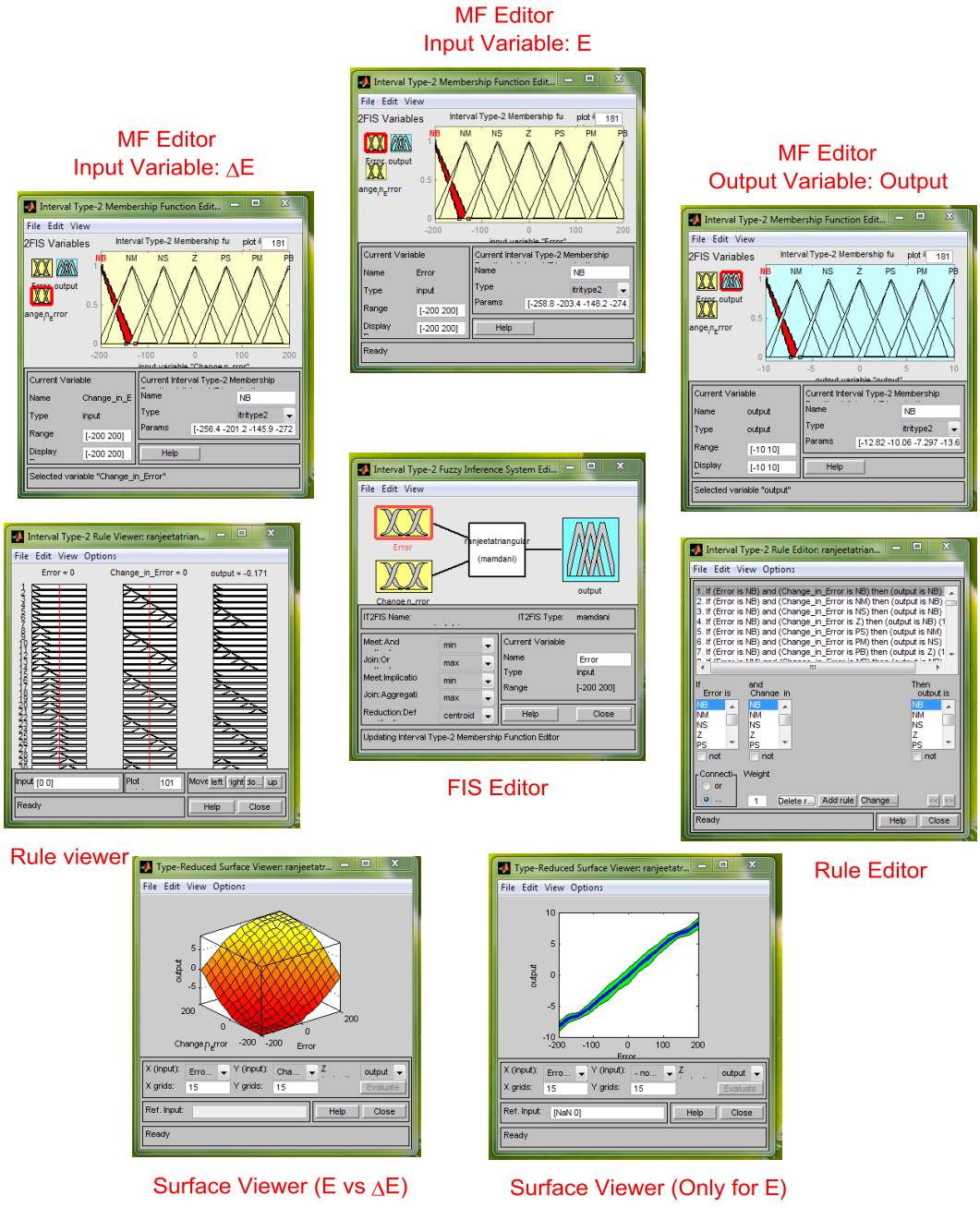


Figure 3.22: Matlab based Type-2 fuzzy inference system with triangular membership function

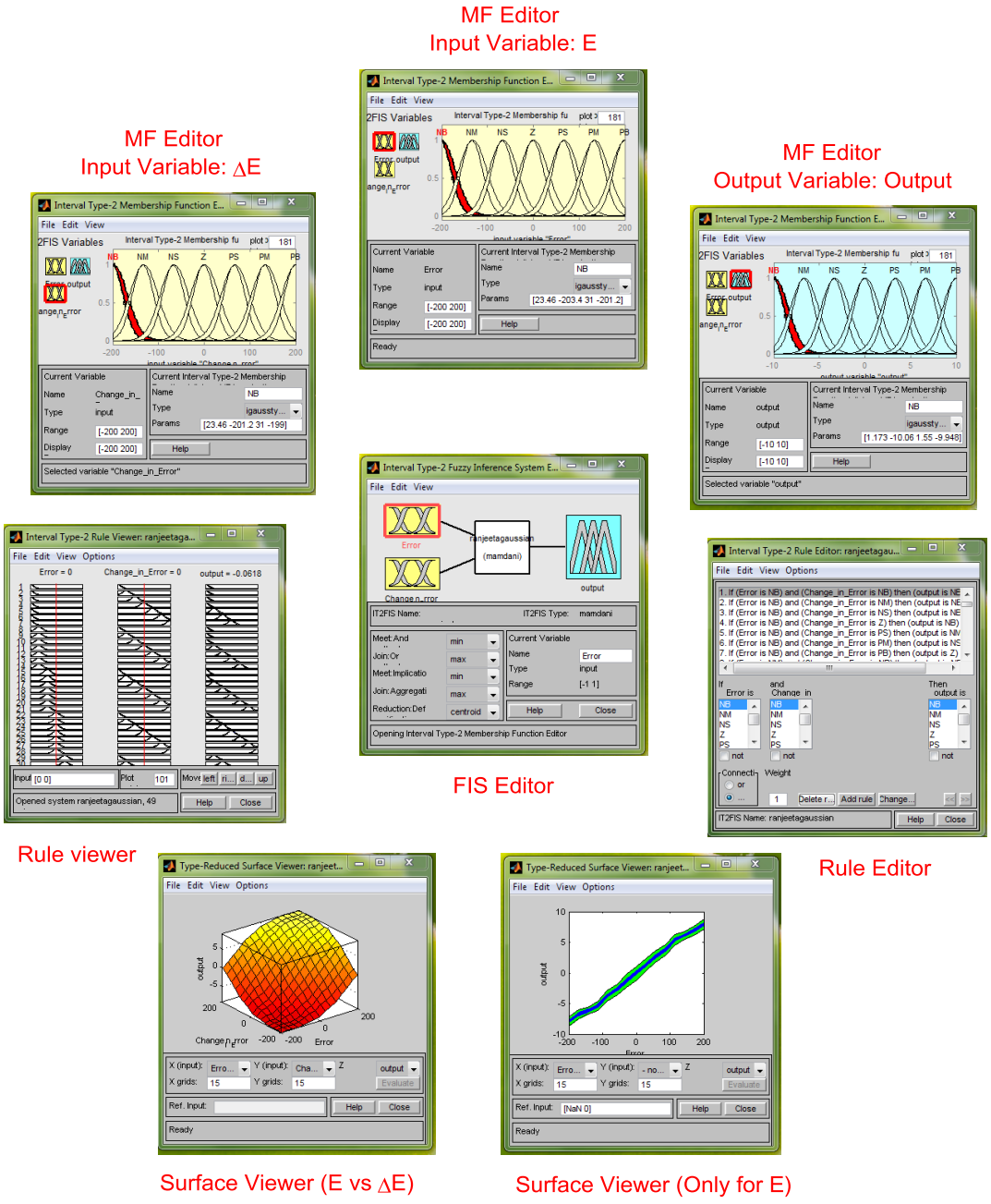


Figure 3.23: Matlab based Type-2 fuzzy inference system with Gaussian membership function

3.4 2C IB APF using FLC based i_d-i_q control strategy

Figure 3.24 shows the 3-phase 4-wire split capacitor interleaved buck active power filter (2C IB APF) and Figure 3.25 shows the fuzzy (Type-1 and Type-2) and adaptive hysteresis based i_d-i_q control strategy used for 2C IB APF.

Extensive simulations have been taken out to find the effectiveness of adaptive hysteresis based i_d-i_q control based 2C IB APF with above discussed Type-1 and Type-2 fuzzy logic

controller for different membership functions such as trapezoidal, triangular and Gaussian under different supply voltage conditions.

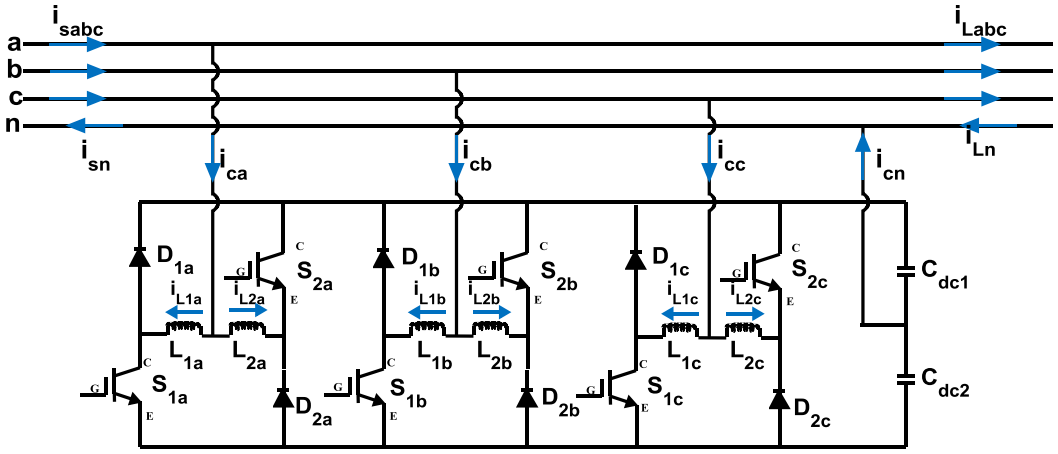


Figure 3.24: 3-phase 4-wire split capacitor interleaved buck active power filter (2C IB APF)

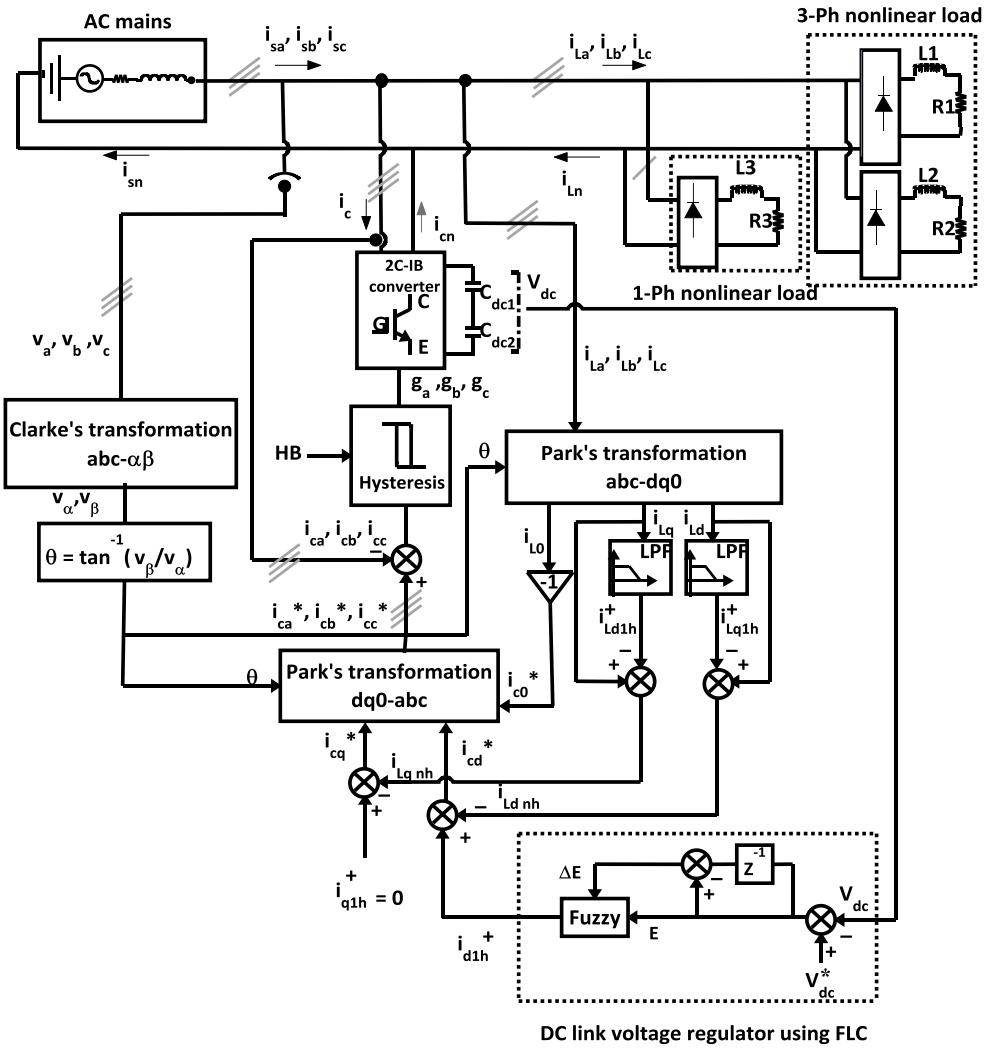


Figure 3.25: 3-phase 4-wire split capacitor interleaved buck active power filter (2C IB APF) using fuzzy and adaptive hysteresis based i_d-i_q control strategy

The system configuration along with the three-phase and single-phase non-linear load is depicted in Figure 3.25. Values for simulation and real time implementation parameters of 2C IB APF using fuzzy and adaptive hysteresis based i_d-i_q control strategy is depicted in Table 3.2 very clearly.

The main purpose of this chapter is to give the improved harmonic compensation with good dc-link voltage regulation as compared to the conventional PI controller based i_d-i_q control strategy. Here also 2C IB APF has been used to have the comparison with the previous chapter. However, here the analysis has been done on 2C IB APF for different Type-1 and Type-2 fuzzy membership functions for harmonic compensation and dc-link voltage regulation for dynamic state.

Table 3.2: Parameters value of simulation and real time implementation

System parameters	2C IB APF value
Supply Voltage (RMS)	Vs = 400 V (Line voltage)
Supply Frequency	fs = 50Hz
dc-link capacitance	C_{dc} = 1500 µF
dc- link capacitor voltage	V_{dc} = 800 V
APF coupling inductor	L = 600 µH
Non-linear load value	Two 3-phase non-linear load R_1 = 16 Ω and L_1=50 mH One 1-phase non-linear load R_2 = 16 Ω and L_2 = 50 mH connected with phase-a

Table 3.3: Mamdani fuzzy design parameters

Mamdani fuzzy parameters	Information
Type	Type-1 and Type-2
Input	2
Output	1
Number of MFs	7
Number of rules	49
Fuzzification	Continuous Universe of Discourse
Implication	Mamdani's min operator
Defuzzification	Centroid of area

3.5 System Performance of Type-1 FLC based i_d-i_q control strategy with different fuzzy MFs

Dynamic performance of 2C IB APF under unbalanced load condition with Type-1 fuzzy Logic Controller for sinusoidal voltage source condition

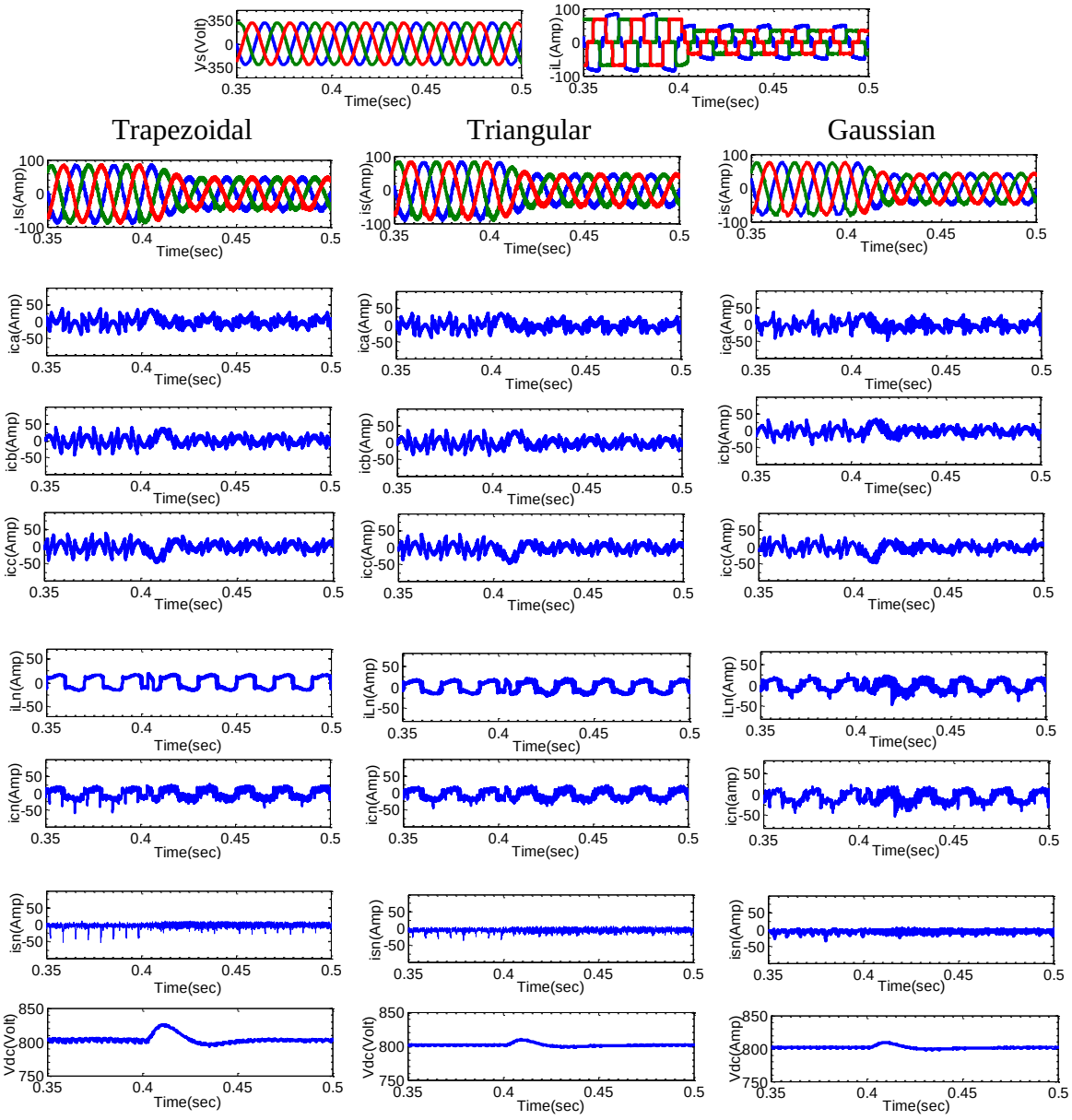


Figure 3.26: Simulation results of 2C IB APF with unbalanced load using Type-1 fuzzy logic controller for load current (i_L), filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}) by (a) Trapezoidal MF, (b) Triangular MF, and (c) Gaussian MF under sinusoidal voltage source condition

Dynamic performance of 2C IB APF under unbalanced load condition with Type-1 fuzzy logic controller for sinusoidal voltage supply

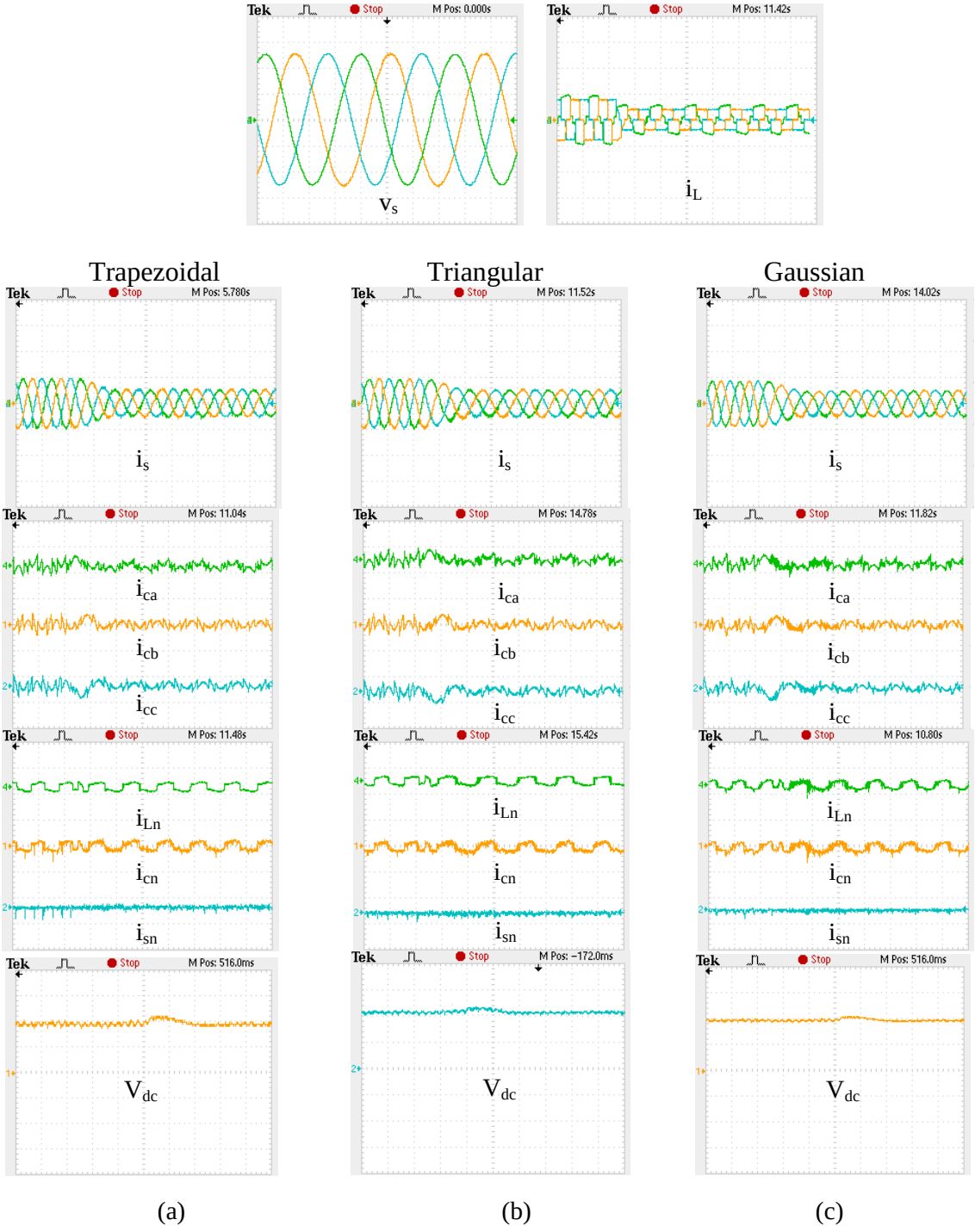


Figure 3.27: OPAL-RT lab results of 2C IB APF with unbalanced load using Type-1 fuzzy logic controller for load current (i_L), filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}) by (a) Trapezoidal MF, (b) Triangular MF, and (c) Gaussian MF under sinusoidal voltage source condition

Dynamic performance of 2C IB APF under unbalanced load condition with Type-1 fuzzy logic controller for unbalanced sinusoidal voltage source condition

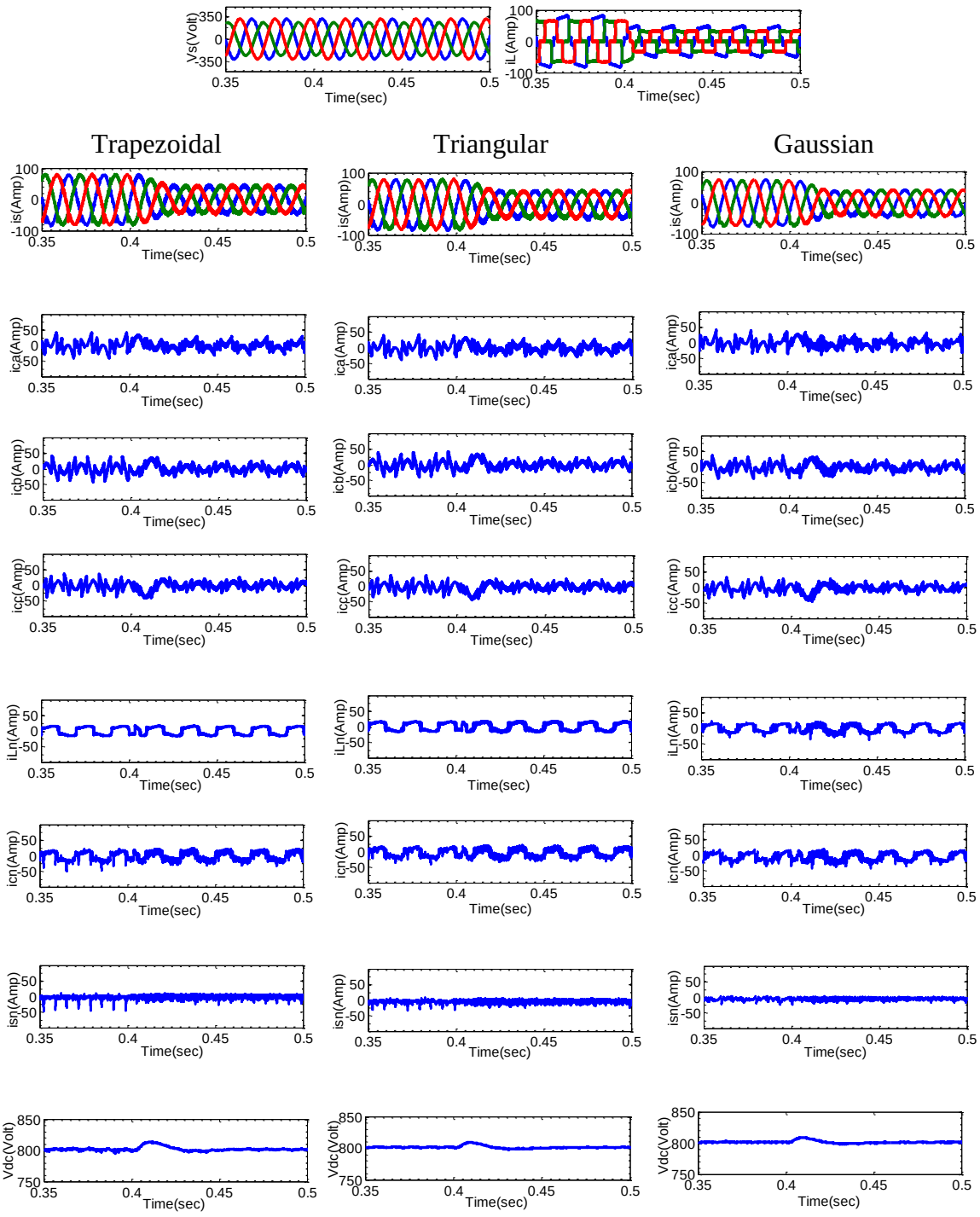


Figure 3.28: Simulation results of 2C IB APF with unbalanced load using Type-1 fuzzy logic controller for load current (i_L), filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}) by (a) Trapezoidal MF, (b) Triangular MF, and (c) Gaussian MF under unbalanced sinusoidal voltage source condition

Dynamic performance of 2C IB APF under unbalanced load condition with Type-1 fuzzy logic controller for unbalanced sinusoidal voltage source condition

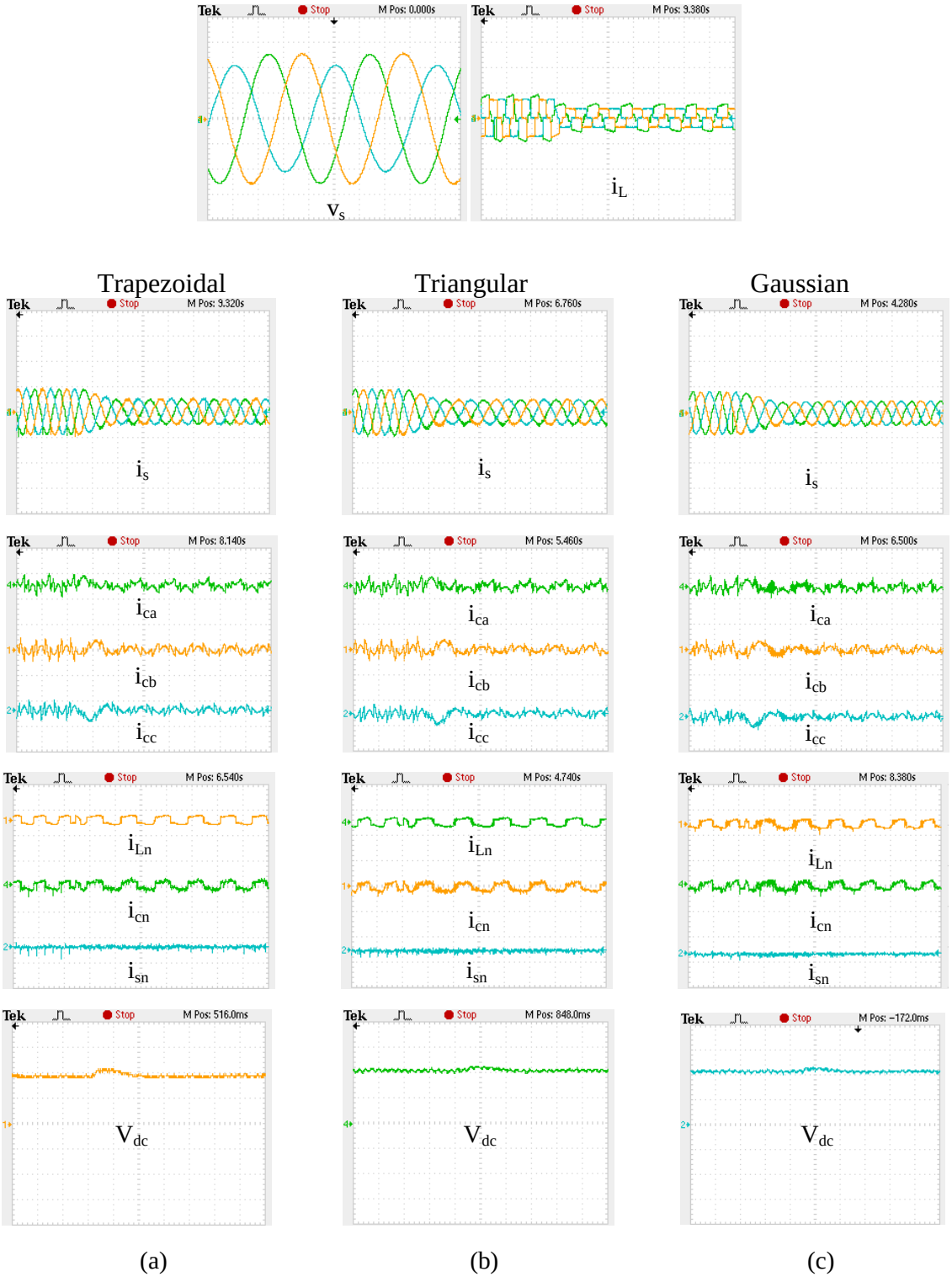


Figure 3.29: OPAL-RT results of 2C IB APF with unbalanced load using Type-1 fuzzy logic controller for load current (i_L), filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}) by (a) Trapezoidal MF, (b) Triangular MF, and (c) Gaussian MF under unbalanced sinusoidal voltage source condition

Dynamic performance of 2C IB APF under unbalanced load condition with Type-1 fuzzy logic controller for non-sinusoidal voltage source condition

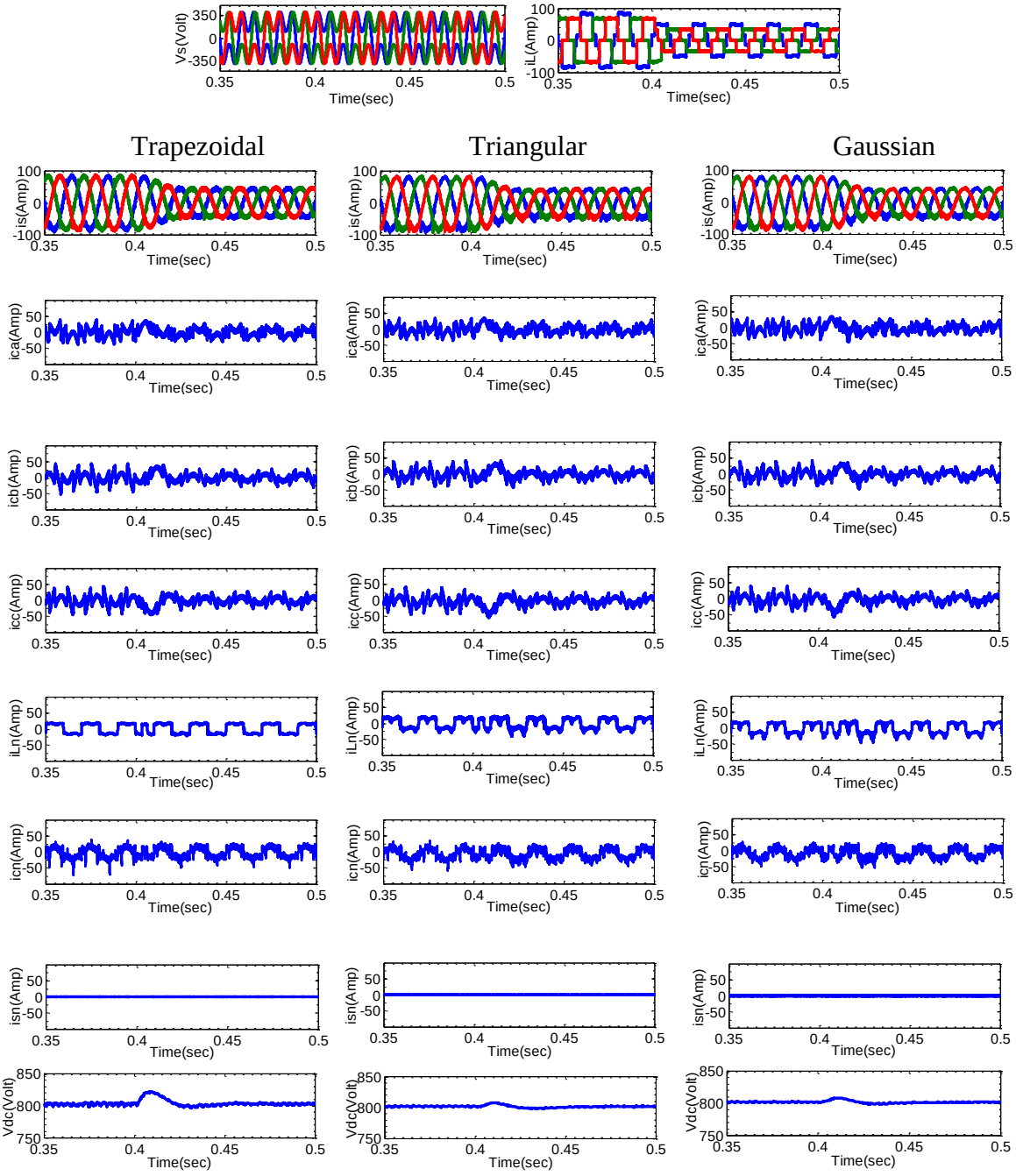


Figure 3.30: Simulation results of 2C IB APF with unbalanced load using Type-1 fuzzy logic controller for load current (i_L), filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}) by (a) Trapezoidal MF, (b) Triangular MF, and (c) Gaussian MF under non-sinusoidal voltage source condition

Dynamic performance of 2C IB APF under unbalanced load condition with Type-1 fuzzy logic controller for non-sinusoidal voltage source condition

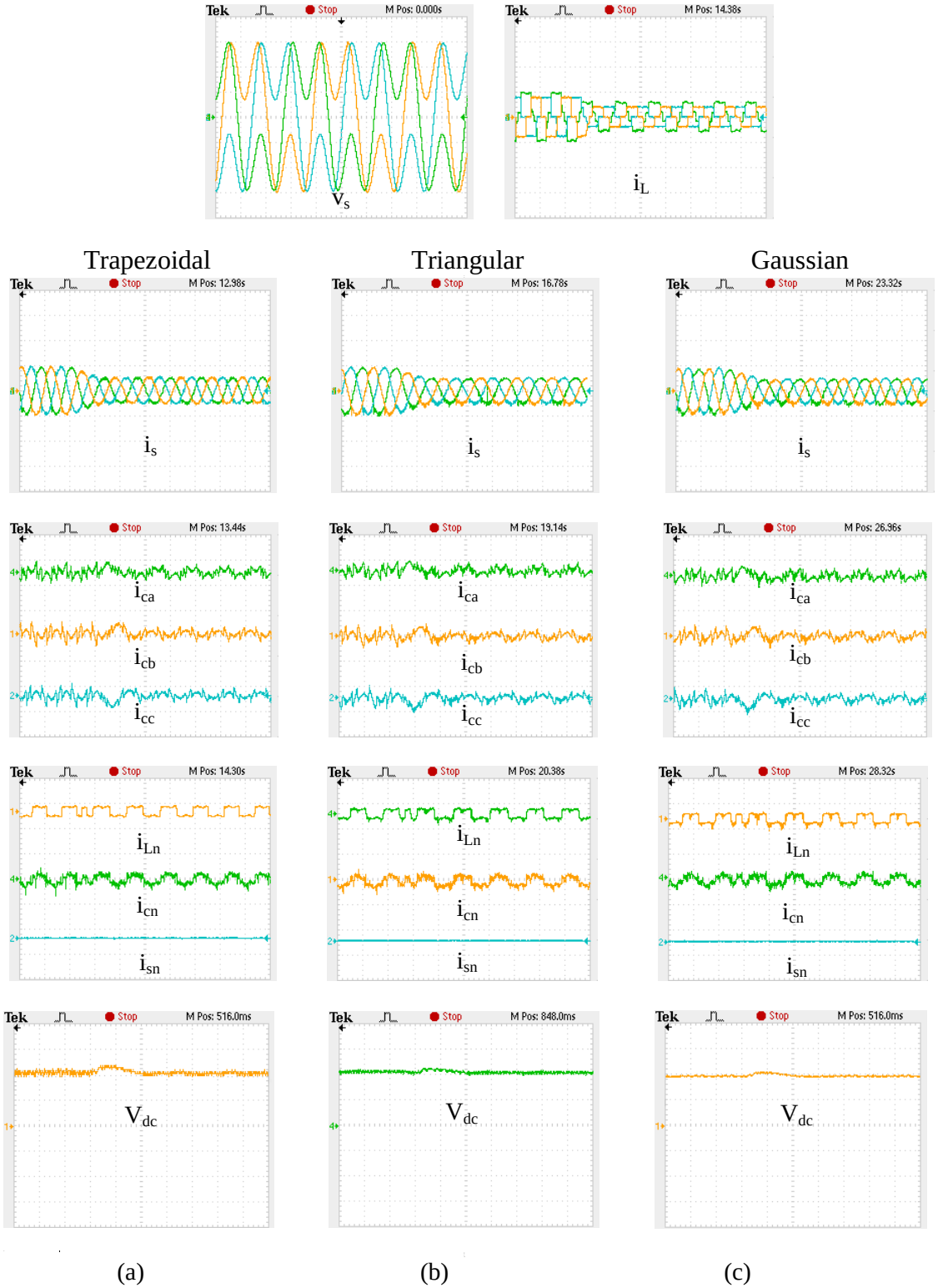


Figure 3.31: OPAL-RT results of 2C IB APF with unbalanced load using Type-1 fuzzy logic controller for load current (i_L), filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}) by (a) Trapezoidal MF, (b) Triangular MF, and (c) Gaussian MF under nonsinusoidal voltage source condition.

3.5.1 Results Discussion

Table 3.4: Source current THD using Type-1different fuzzy MFs

Supply voltage	Without 2C IB APF (% THD)			Type-1 Fuzzy MF	With 2C IB APF (% THD)		
	Ph-a	Ph-b	Ph-c		Ph-a	Ph-b	Ph-c
Sinusoidal	19.12	28.25	28.99	Trapezoidal	3.36	3.68	3.29
				Triangular	2.26	2.84	2.41
				Gaussian	2.03	2.71	2.29
Unbalanced sinusoidal	20.96	31.41	27.65	Trapezoidal	4.31	4.18	3.44
				Triangular	2.68	3.19	2.47
				Gaussian	2.17	2.97	2.30
Non-sinusoidal	21.92	28.46	28.64	Trapezoidal	4.62	4.98	4.41
				Triangular	4.15	4.38	3.98
				Gaussian	3.01	4.01	3.2

Figure 3.26 and 3.27 shows the Simulation and OPAL-RT real-time hardware results of 2C IB APF with unbalanced load using Type-1 fuzzy controller for load current (i_L), filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}) for trapezoidal MF, triangular MF, and Gaussian membership functions for sinusoidal voltage source condition. Similarly, Figure 3.28 and 3.29 shows the simulation and OPAL-RT results for unbalanced sinusoidal supply; and Figure 3.30 and 3.31 shows for non-sinusoidal voltage source conditions. Table 3.4 depicted the THDs of the source current with and without the compensation using trapezoidal, triangular and Gaussian MF for sinusoidal, unbalanced sinusoidal and non-sinusoidal voltage source conditions. It can be seen that, in all the voltage source conditions, Type-1 Gaussian membership functions give the better harmonic compensation. Here the simulation and OPAL-RT results have been shown for dynamic state and as can be seen that the settling time for dc-link voltage is also nearly only 0.025 sec; whereas the load current change has been made at 0.4 sec and the dc-link capacitor voltage has been settled down nearly 0.425 sec. Again, from the previous chapter, the dc-link voltage settling time is nearly 0.08 sec. in case of sinusoidal voltage source condition with PI controller. Hence, it can be concluded that, Gaussian MFs compensates well enough in any voltage conditions.

3.6 System Performance of Type-2 FLC based i_d-i_q control strategy with different Fuzzy MFs

Dynamic performance of 2C IB APF under unbalanced load condition with Type-2 fuzzy logic controller for sinusoidal voltage source condition

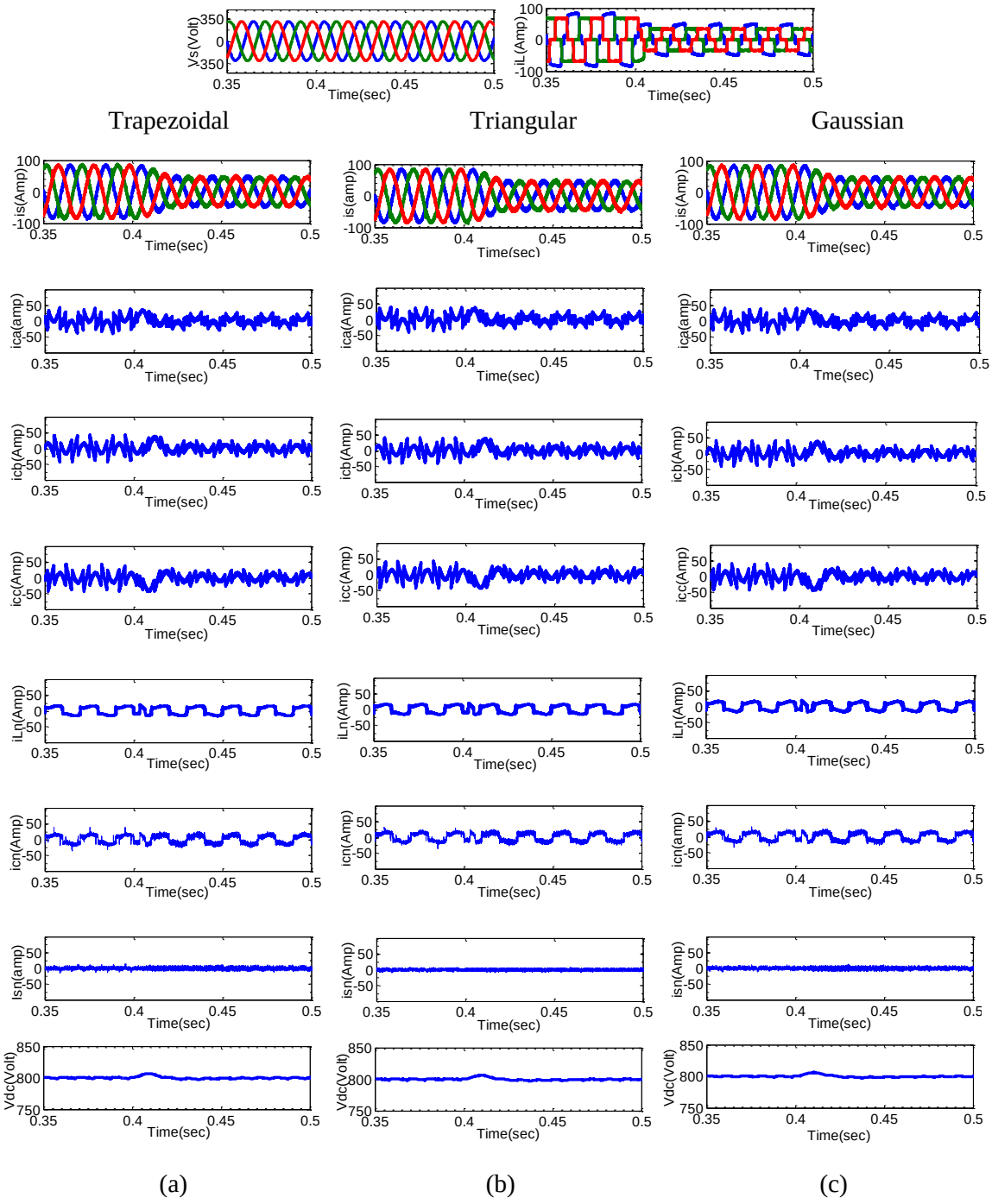


Figure 3.32: Simulation results of 2C IB APF with unbalanced load using Type-2 fuzzy logic controller for load current (i_L), filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}) by (a) Trapezoidal MF, (b) Triangular MF, and (c) Gaussian MF under sinusoidal voltage source condition

Dynamic performance of 2C IB APF under unbalanced load condition with Type-2 fuzzy logic controller for sinusoidal voltage source condition

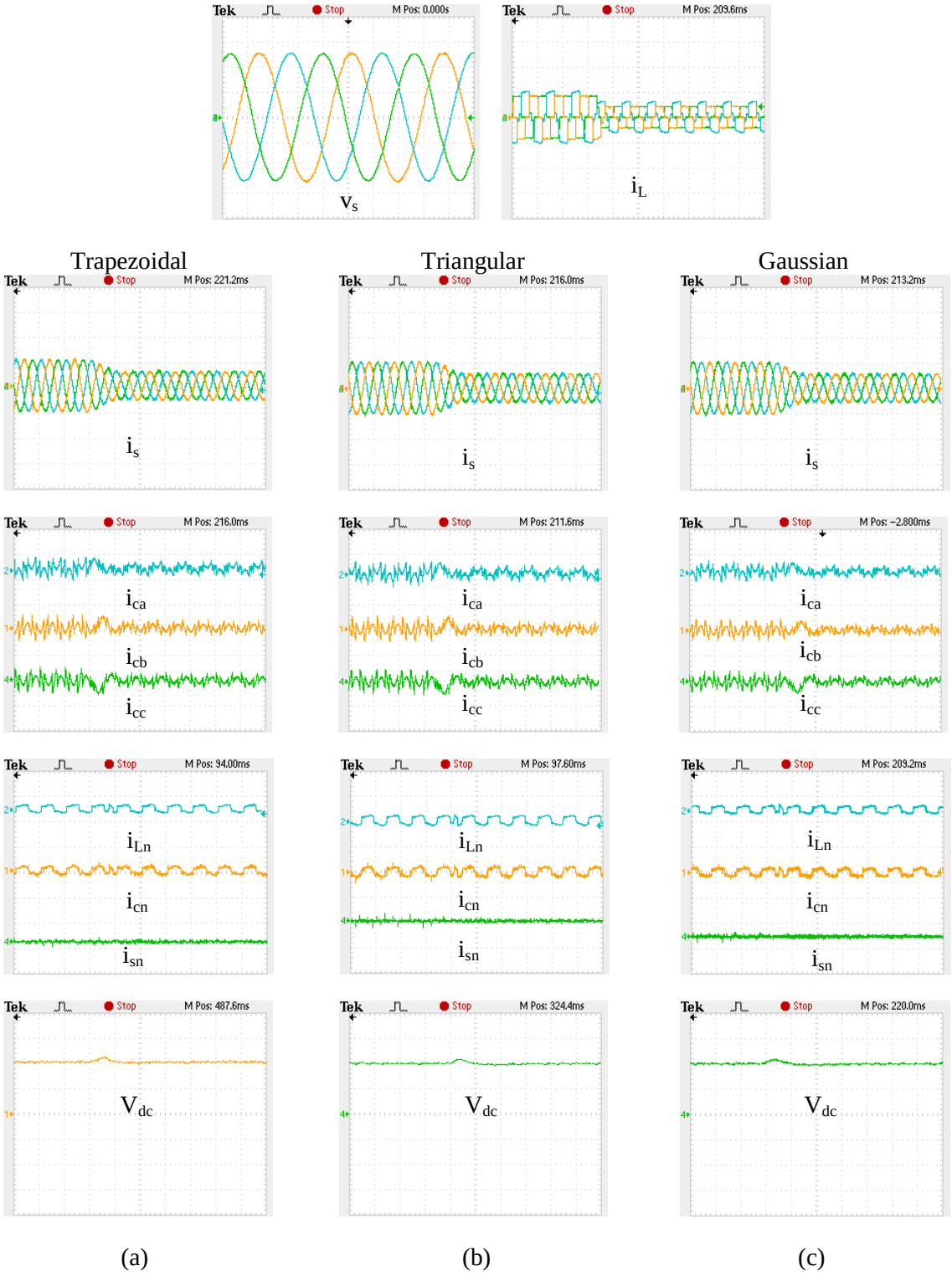


Figure 3.33: OPAL-RT results of 2C IB APF with unbalanced load using Type-2 fuzzy logic controller for load current (i_L), filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}) by (a) Trapezoidal MF, (b) Triangular MF, and (c) Gaussian MF under sinusoidal voltage source condition

Dynamic performance of 2C IB APF under unbalanced load condition with Type-2 fuzzy logic controller for unbalanced sinusoidal voltage source condition

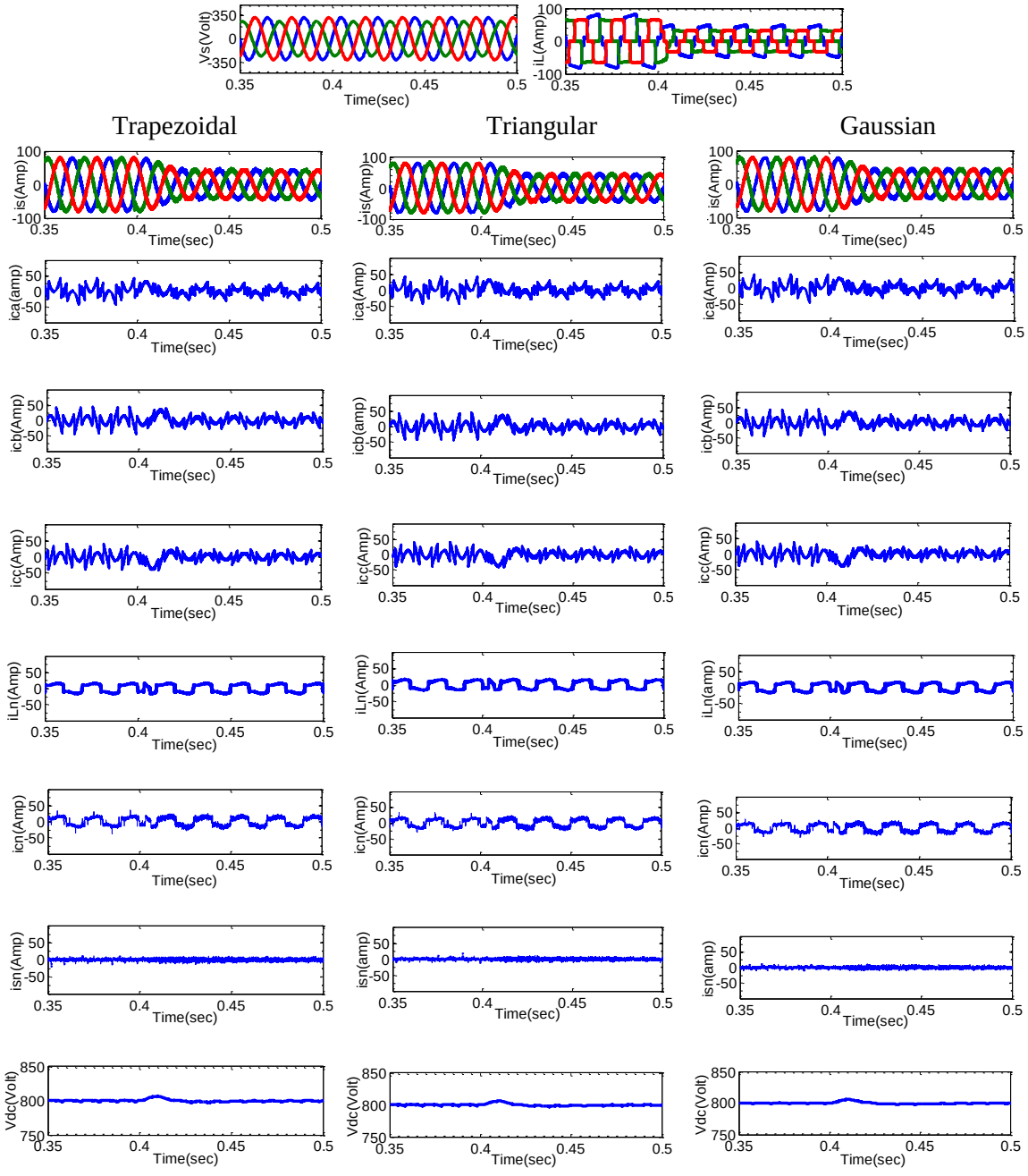
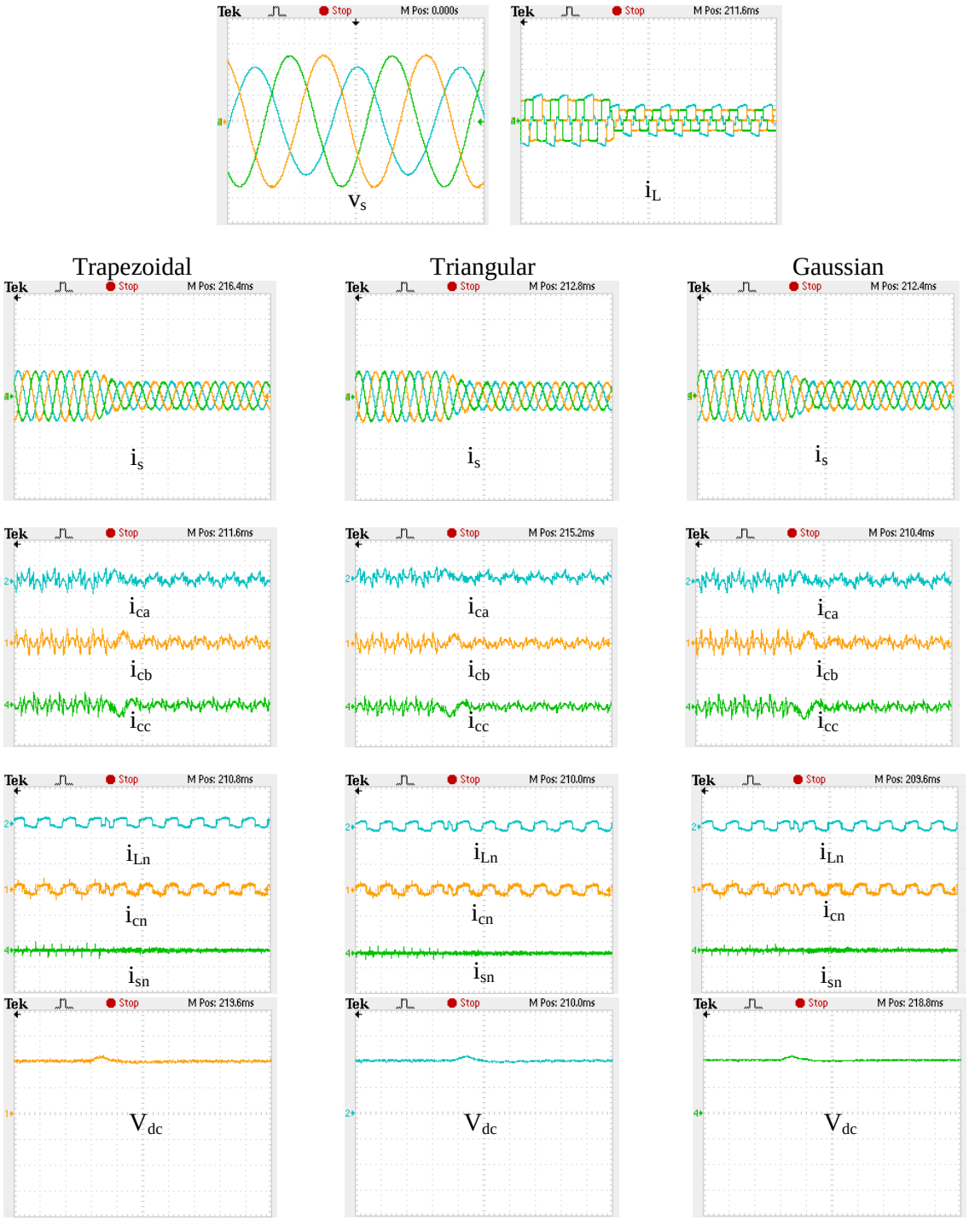


Figure 3.34: Simulation results of 2C IB APF with unbalanced load using Type-2 fuzzy logic controller for load current (i_L), filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}) by (a) Trapezoidal MF, (b) Triangular MF, and (c) Gaussian MF under unbalanced sinusoidal voltage source condition

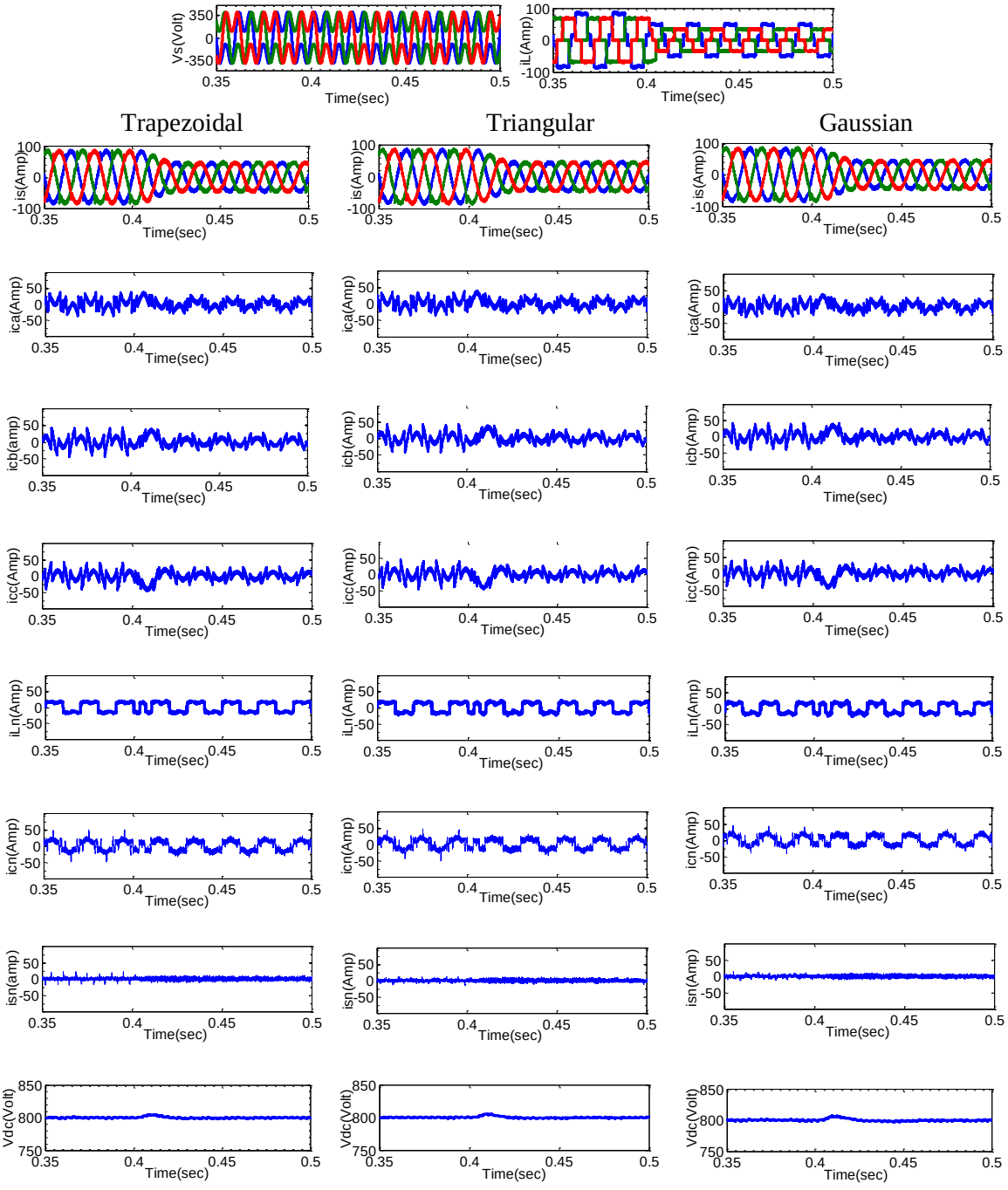
Dynamic performance of 2C IB APF under unbalanced load condition with Type-2 fuzzy logic controller for unbalanced sinusoidal voltage source condition



(a) (b) (c)

Figure 3.35: OPAL-RT results of 2C IB APF with unbalanced load using Type-2 fuzzy logic controller for load current (i_L), filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}) by (a) Trapezoidal MF, (b) Triangular MF, and (c) Gaussian MF under unbalanced sinusoidal voltage source condition

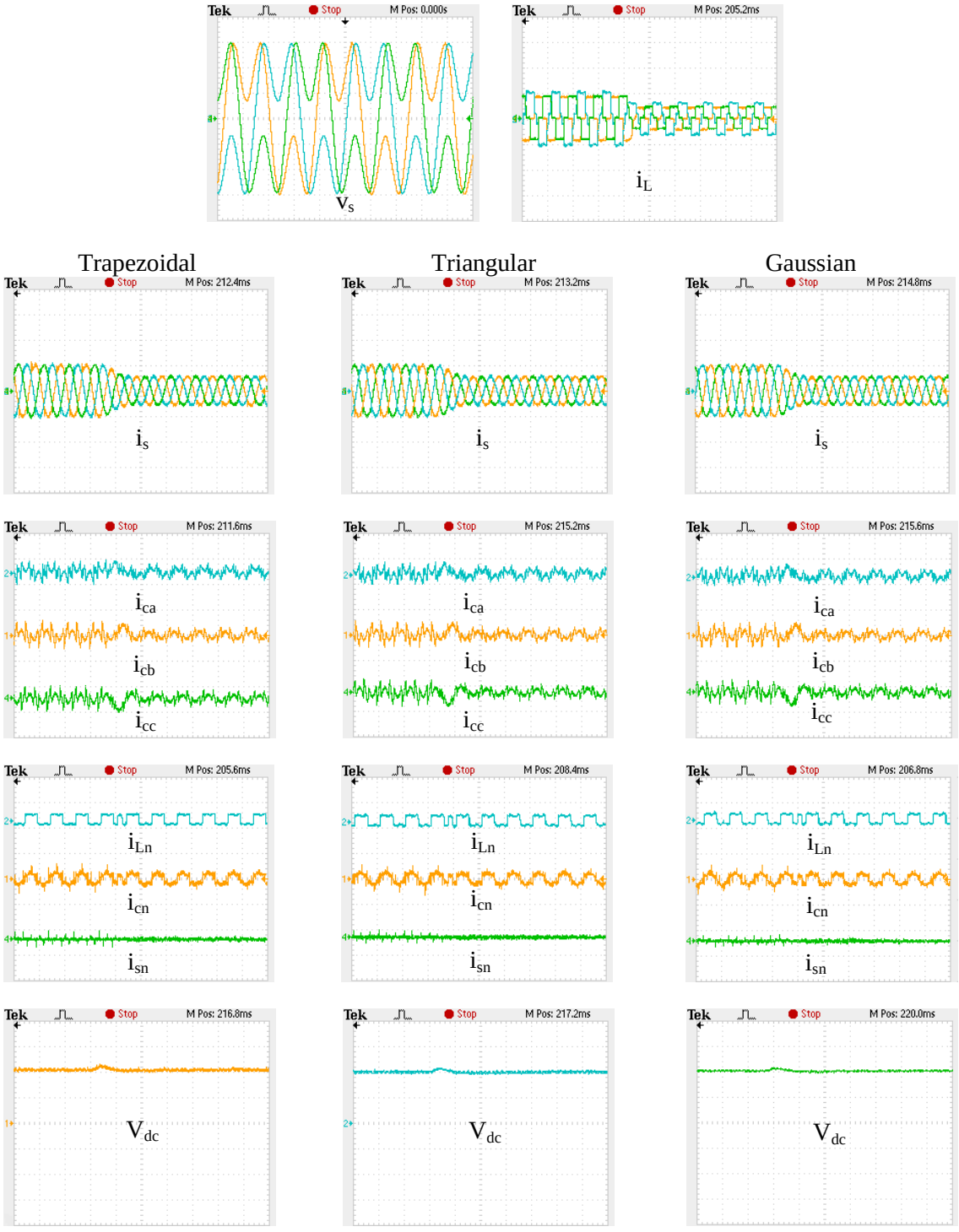
Dynamic performance of 2C IB APF under unbalanced load condition with Type-2 fuzzy logic controller for non-sinusoidal voltage source condition



(a) (b) (c)

Figure 3.36: Simulation results of 2C IB APF with unbalanced load using Type-2 fuzzy logic controller for load current (i_L), filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}) by (a) Trapezoidal MF, (b) Triangular MF, and (c) Gaussian MF under non-sinusoidal voltage source condition

Dynamic performance of 2C IB APF under unbalanced load condition with Type-2 fuzzy logic controller for non-sinusoidal voltage source condition



(a) (b) (c)

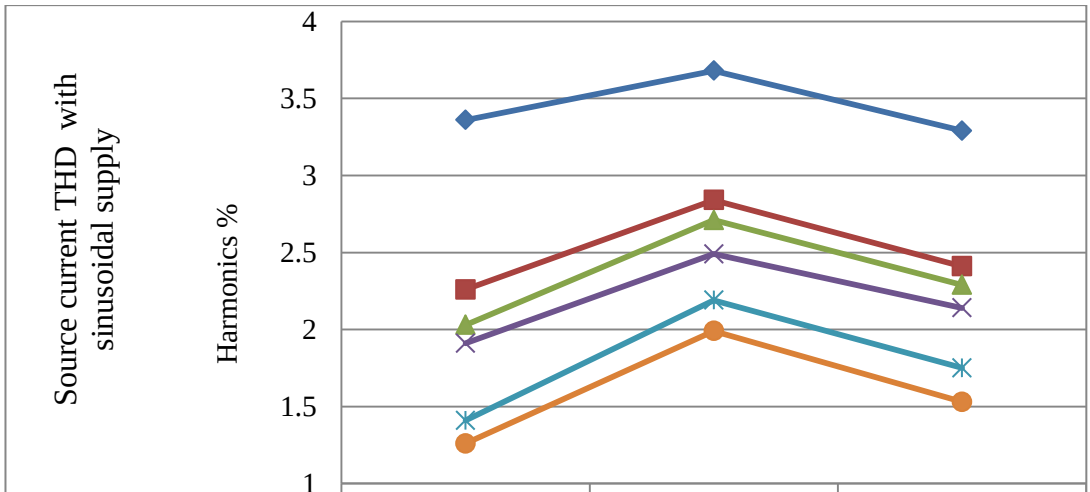
Figure 3.37: OPAL-RT results of 2C IB APF with unbalanced load using Type-2 fuzzy logic controller for load current (i_L), filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}) by (a) Trapezoidal MF, (b) Triangular MF, and (c) Gaussian MF under non-sinusoidal voltage source condition

3.6.1 Results Discussion

Table 3.5: Source current THD using Type-2 different fuzzy MFs

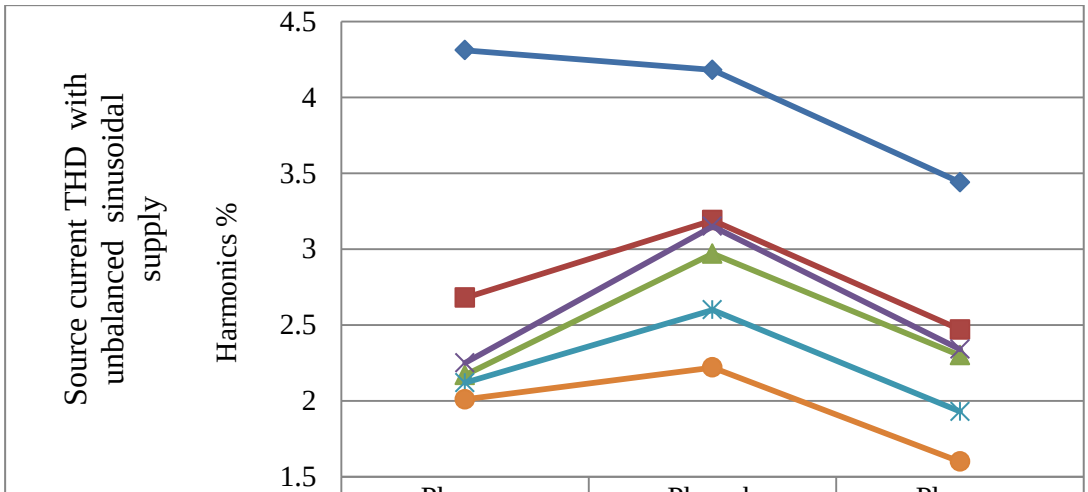
Supply voltage	Without 2C IB APF (% THD)			Type-2 Fuzzy MF	With 2C IB APF		
	Ph-a	Ph-b	Ph-c		Ph-a	Ph-b	Ph-c
Sinusoidal	19.48	28.04	27.66	Trapezoidal	1.91	2.49	2.14
				Triangular	1.41	2.19	1.75
				Gaussian	1.26	1.99	1.53
Unbalanced sinusoidal	20.30	30.70	26.12	Trapezoidal	2.25	3.15	2.34
				Triangular	2.12	2.60	1.93
				Gaussian	2.01	2.22	1.60
Non-sinusoidal	20.62	28.35	27.98	Trapezoidal	2.51	3.76	3.04
				Triangular	2.21	3.29	2.50
				Gaussian	2.06	3.18	2.19

Figure 3.32 and 3.33 represents the Type-2 fuzzy controller for membership functions, trapezoidal, triangular and Gaussian simulation and OPAL-RT real time results for sinusoidal voltage source condition. The simulation and OPAL-RT results are depicted for load current (i_L), filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}) of 2C IB APF. Similarly 3.34 and 3.35 gives the simulation and OPAL-RT results for unbalanced sinusoidal and Figure 3.36 and 3.37 depicts the simulation and OPAL-RT results for non-sinusoidal voltage source condition. As can be seen from the Table 3.5, all the MFs can meet the IEEE 519 harmonic compensation standard, but, Type-2 Gaussian membership functions give the better harmonic compensation in all the voltage source conditions. The dc-link capacitor voltage also settles down in less time as compared to Type-1 fuzzy logic controller a can be seen from the simulation results. Finally, as Type-2 fuzzy logic controller can handle more uncertainty, hence the harmonic compensation is better than the Type-1 fuzzy logic controller as can be seen from Table 3.4 and 3.5. Figure 3.38, 3.39 and 3.40 shows the chart diagram of the THD comparisons.



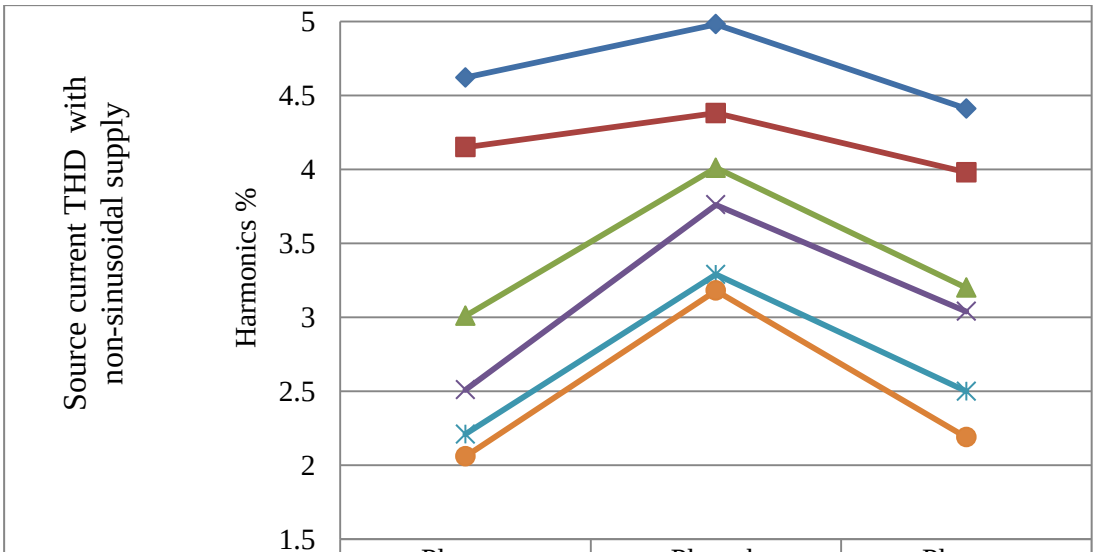
	Phase a	Phase b	Phase c
Type-1 Trapezoidal	3.36	3.68	3.29
Type-1 Triangular	2.26	2.84	2.41
Type-1 Gaussian	2.03	2.71	2.29
Type-2 Trapezoidal	1.91	2.49	2.14
Type-2 Triangular	1.41	2.19	1.75
Type-2 Gaussian	1.26	1.99	1.53

Figure 3.38: Chart showing the THD comparison of source current using Type-1 and Type-2 trapezoidal, triangular, and Gaussian membership function for sinusoidal voltage source condition



	Phase a	Phase b	Phase c
Type-1 Trapezoidal	4.31	4.18	3.44
Type-1 Triangular	2.68	3.19	2.47
Type-1 Gaussian	2.17	2.97	2.3
Type-2 Trapezoidal	2.25	3.15	2.34
Type-2 Triangular	2.12	2.6	1.93
Type-2 Gaussian	2.01	2.22	1.6

Figure 3.39: Chart showing the THD comparison of source current using Type-1 and Type-2 trapezoidal, triangular, and Gaussian membership function for unbalanced sinusoidal voltage source condition



	Phase a	Phase b	Phase c
Type-1 Trapezoidal	4.62	4.98	4.41
Type-1 Triangular	4.15	4.38	3.98
Type-1 Gaussian	3.01	4.01	3.2
Type-2 Trapezoidal	2.51	3.76	3.04
Type-2 Triangular	2.21	3.29	2.5
Type-2 Gaussian	2.06	3.18	2.19

Figure 3.40: Chart showing the THD comparison of source current using Type-1 and Type-2 trapezoidal, triangular, and Gaussian membership function for non-sinusoidal voltage source condition

3.7 Summary

In this chapter, Type-1 and Type-2 fuzzy logic controller based split capacitor interleaved buck active power filter using adaptive hysteresis i_d-i_q control strategy with different membership functions has been used for the mitigation of harmonics. The performance of the 2C IB APF topology has been evaluated in terms of harmonic compensation, dc-link voltage regulation and neutral current compensation for unbalanced non-linear load condition during the dynamic state. Type-2 fuzzy logic controller performance is superior to Type-1 fuzzy logic controller in all the supply conditions, i.e. sinusoidal, unbalanced sinusoidal and non-sinusoidal voltage source conditions. The Type-2 based 2C IB APF able to eliminate the uncertainty of the system and provides outstanding performance of harmonic compensation. The detailed simulation and OPAL-T real time hardware results have been depicted in order to prove the feasibility of the proposed topology. The simulation results depicted that, even in the non-sinusoidal voltage source condition, Type-2 Gaussian membership function with i_d-i_q control strategy gives the best result as

compared to Type-1 with all MFs and Type-2 trapezoidal and triangular. This Type-1 and Type-2 control approach has also compensates the neutral current and well maintained dc-link voltage in all supply conditions. The settling time of dc-link voltage is also less in Type-2 based i_d-i_q control strategy as compared to PI and Type-1 based i_d-i_q control strategy. The presented results prove that, in all conditions, the 2C IB APF with fuzzy has been found to meet the IEEE 519-1992 standard recommendation on harmonic limits and hence can be adaptable for severe constraints like unbalanced and highly distorted voltage supply conditions.

Chapter 4

Performance Analysis of 4-Leg IB APF, 1C 3FB IB APF and FB IB APF topologies for 3-phase 4-wire system

4.1 Introduction

In this chapter various topologies of 3-phase 4-wire interleaved buck active power filter has been modelled. In chapter-2 and chapter-3, three-phase four-wire split capacitor (2C) IB-APF with i_d-i_q control scheme using PI, Type-1 and Type-2 fuzzy logic controller has been presented in detail. However, this 2C IB-APF can be used for low power application and less prone to neutral current. To overcome these limitations as well as taking other accounts, different new 3-phase 4-wire interleaved buck active power filter topologies have been modelled here for 3-phase 4-wire distribution system.

The various interleaved buck converter based four-wire shunt active power filter topologies discussed in this chapter are split capacitor (2C) interleaved buck APF (2C IB APF), 3-phase 4-leg interleaved buck APF (4L IB APF), single capacitor full bridge interleaved buck active power filter (1C 3FB IB APF), and 3-phase 4-wire full bridge interleaved buck active power filter (FB IB APF) with their various pros and cons. The neutral compensation, dc-link voltage utilization, power handling capacity of the active power filter is the main reasons for the development of various topologies. Again, all the 3-phase 4-wire IB APF topologies are of high reliability, as these are free from the shoot-through phenomenon.

In Chapter-2 already discussed about the advantages of mitigation of shoot-through current in the interleaved buck inverter circuit used as the main part of the active power

filter. Here, various, 3-phase 4-wire interleaved buck active power filter topologies are modelled with Proportional-Integral (PI) and Type-1 fuzzy logic controller (T1FLC) based i_d-i_q control strategy and compared; their performance is evaluated under various voltage source conditions i.e. sinusoidal, unbalanced and non-sinusoidal for unbalanced load condition. The most commonly used membership functions (MFs) are triangular as to various membership functions. Hence triangular MF has been used in all the proposed topologies and the same design parameters, as given in Table 3.3 are being applied to this Mamdani based Type-1 fuzzy logic controller. The unbalanced load taken here comprised of the combination of three-phase and single-phase harmonic producing nonlinear load. The thorough simulation results have been presented for all the 3-phase 4-wire IB APFs topologies for PI and T1FLC. For validation, the modelled topologies are implemented in real time OPAL-RT simulator and sufficient results are depicted for its verification.

The topologies 2C IB APF and 4-leg IB APF are enumerated in Section 4.2 and 4.3 respectively. A description of FB IB converter and its working modes are presented in 4.4. Again, 1C 3FB IB APF and FB IB APF are enumerated in detail in Section 4.5 and 4.6 respectively. Section 4.7 represents the detailed simulation and OPAL-RT hardware results for all the proposed 3-phase 4-wire IB APF topologies. Finally, a comparison of SDP has been laid out in Section 4.8 and summarizes in Section 4.9.

4.2 Split Capacitor Interleaved Buck Active Power Filter (2C IB APF)

In previous chapters, there is already a detailed description of this split capacitor interleaved buck active power filter (2C IB APF) but for comparison purpose, again this topology has been depicted here. This topology can also be called as a half bridge interleaved buck active power filter (HB IB APF), because it consists of three numbers of half bridge interleaved buck inverter with split capacitor arrangement [74]. The presented 3-phase 4-wire split capacitor IB APF is designed for harmonic, unbalanced load current compensation with an end to shoot-through phenomenon. The midpoint of the two capacitors is utilized for the neutral current path, and thus, the entire neutral current flows through the dc bus capacitors. In this topology, voltages of the two capacitors need to be properly balanced. A difference between these two voltages may cause a dc circulating current to flow, affecting the overall compensation. Figure 4.1 and 4.2 shows the 2C IB APF and dc-link voltage regulation system respectively. .

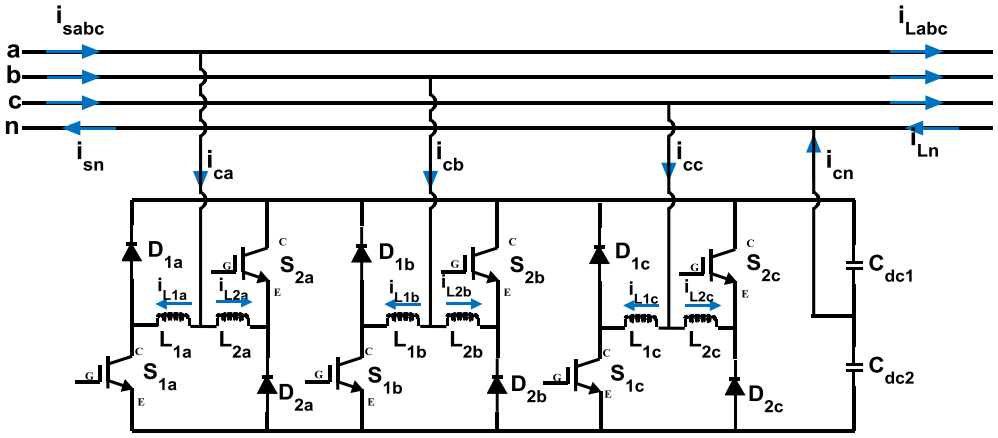


Figure 4.1: Split capacitor interleaved buck active power filter (2C IB APF)

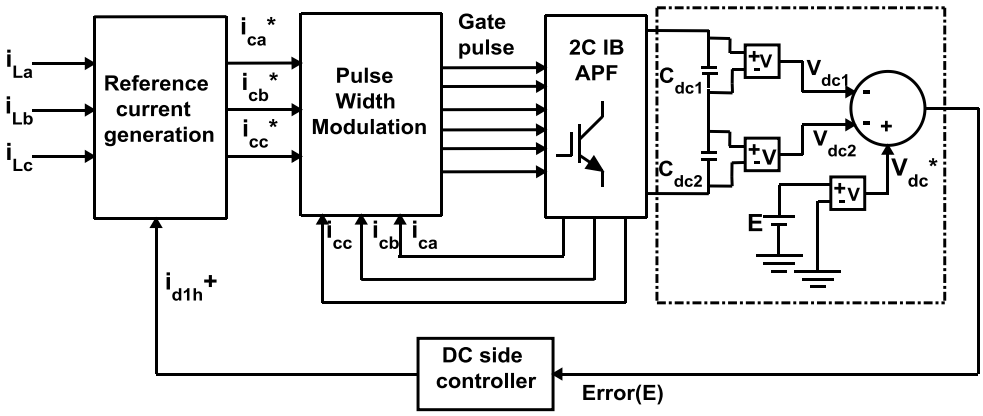


Figure 4.2: Block diagram of dc-link voltage regulation in 2C IB APF

The voltage that appears across 3-phase 4-wire split capacitor interleaved buck active power is the three phase voltage (400 V) and not the single phase voltage [39]. Hence, the required minimum dc-link capacitor voltage can be calculated from the following equation:

$$V_{dc,min} = \frac{\sqrt{3}\times\sqrt{2}}{0.87} V_{s,rms} = 2.815 \times V_{s,rms} \quad (4.1)$$

The rating of the inverter (particularly switching device voltage rating) depends very much on dc-link voltage [12].

The voltage across the DC-link capacitors, C_{dc1} be V_{dc1} and C_{dc2} be V_{dc2} respectively. The 2C IB APF can be considered as the single phase half bridge interleaved buck active power filter when the midpoint of the split capacitor is being grounded. Let's say the filter current, i_{ca} for the corresponding phase a. The rate of rise of the voltage V_{dc1} and V_{dc2} depends on the rate of rise of the filter current, i.e. di_{ca}/dt. The C_{dc1} capacitor voltage V_{dc1} increases and C_{dc2} capacitor voltage V_{dc2} decreases, for $i_{ca} > 0$. Similarly, the V_{dc1},

capacitor voltage across C_{dc1} and V_{dc2}, capacitor voltage across C_{dc2} decreases and increases respectively, for $i_{ca} < 0$. Though, the rise and fall of the dc-link capacitor voltage are not same due to different rate of rise of filter current, there may be a voltage difference between $V_{dc1}$and V_{dc2}; which may result in a circulating current. The equation defined for the differential voltage between the $V_{dc1}$and V_{dc2} as:

$$\Delta V_{dc} = \frac{1}{C}\int_0^t (i_{C1} + i_{C2})dt = \frac{1}{C}\int_0^t \left(\frac{V_{dc1}+V_{dc2}}{V_{dc}} i_n\right) dt = -\frac{1}{C}\int_0^t i_n dt \quad (4.2)$$

Where i_{C1} and i_{C2} are designated by the upper and lower dc bus capacitor current, and i_n represents as neutral current.

The dc-link voltage regulation is different from all other topologies discussed in the following subsections. The all other discussed 3-phase 4-wire IB APF topologies have to deal with only one dc-link bus voltage. Hence, the voltage difference between the dc-link capacitor voltage and the pre-specified reference dc voltage needs to be minimized as per the requirement by the i_d-i_q control strategy, shown in Figure 4.2 for the effective compensation.

The dc-link voltage error that necessarily be the input to the dc side controller (PI or T1FLC) as can be seen from Figure 4.2, is given as:

$$\Delta V_{dc} = (V_{dc1} + V_{dc2}) - V_{dc}^* \quad (4.3)$$

The 2C IB IBF challenges with the complexity of dc-link voltage regulation. Additionally, there is no direct control over the neutral current compensation, rather the algebraic difference of all the injected phase compensating currents is responsible for the neutral current compensation; hence does not require any neutral current sensor. However, the 2C IB APF topology is used for lower power rating applications as less number of switching devices.

4.3 Four-leg Interleaved Buck Active Power Filter (4L IB APF)

This topology shown in Fig. 4.3 represents the 4-leg interleaved buck active power filter and the corresponding interleaved buck converter consists of an additional IB cell as compared to 2C IB APF inverter [1,75]. The fourth IB cell is solely added to compensate

the load neutral current. A direct, and thus a better, control over neutral current is assured because of the additional interleaved buck (IB) cell.

However, this topology requires an additional neutral current sensor, to track the load neutral current. The neutral reference compensating current can be calculated by the formula as:

$$i_{cn}^{*} = i_{ca}^{*} + i_{cb}^{*} + i_{cc}^{*} \tag{4.4}$$

Considering the economical aspect, the cost involved for an extra bridge leg and their corresponding control circuitries can be a disadvantage of this topology. In this topology also, the three-phase voltage (400 V) exists across the interleaved buck inverter.

The minimum requirement of dc-link voltage by the 4-leg IB APF is given by the calculation as follows:

$$V_{dc,min} = \sqrt{3} \times \sqrt{2} \times V_{s,rms} \tag{4.5}$$

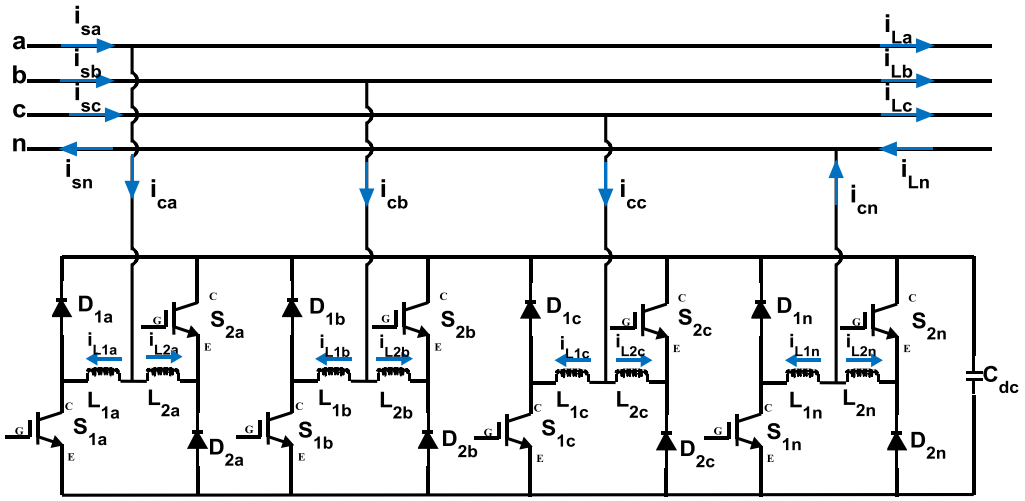


Figure 4.3: Four-leg interleaved buck active power filter (4L IB APF)

Here, only one capacitor voltage needs to be tracked as required by the i_d-i_q control strategy for reference current generation. The 4L IB APF requires comparatively a small value of capacitor as compared to split capacitor interleaved buck active power filter topology (2C IB APF) and can be justified by equation 4.1 and 4.3. The control scheme is also very easy to implement due to one dc-link capacitor. However, the extra cost due to an additional interleaved buck inverter cell and corresponding control circuitries for switching pulse generation are the disadvantages associated with this 4L IB APF topology. As same as the 2C IB APF topology, it is being used for the low power application, and

many researchers have chosen this topology as the proficient alternative topology in 3-phase 4-wire distribution system to be employed on shunt APFs [54,80, 84].

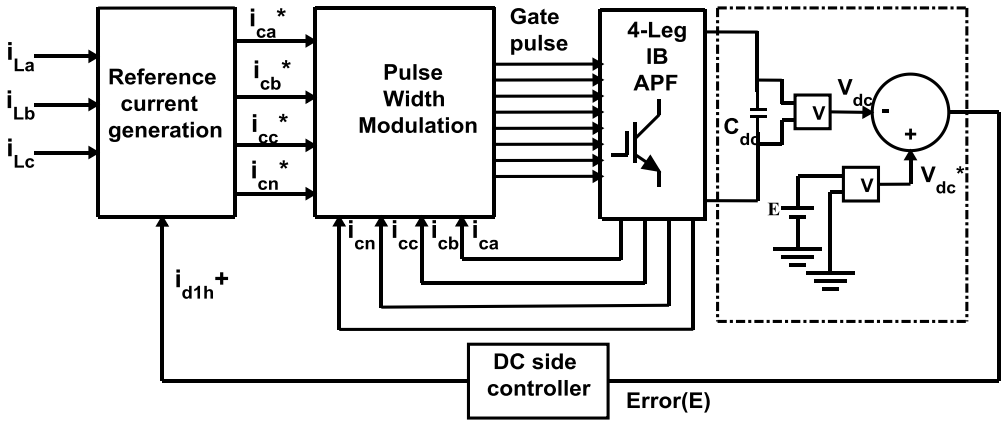


Figure 4.4: Block diagram of dc-link voltage regulation in four-leg interleaved buck active power filter (4L IB APF)

The dc-link voltage regulation is simpler as compared to as can be seen from the Figure 4.4. But, additional two switching pulses are needed to generate for an extra IB cell, which again makes the control strategy complex, but provides better neutral current compensation.

The dc-link error voltage input needs to be minimized as per the requirement by using the dc side controller, either Proportional-Integral (PI) or Type-1 fuzzy logic controller (T1FLC) and can be depicted as:

$$\Delta V_{dc} = V_{dc} - V_{dc}^{*} \tag{4.6}$$

The other description of this i_d-i_q control strategy used by the 4L IB APF is same as the 2C IB APF control strategy, which has already been discussed in Chapter 2.

4.4 Full-bridge Interleaved Buck Converter based Active Power Filter

As the application goes for higher ratings, there will be increased rating demand of the switches, which limits the installation of the above discussed 3-phase 4-wire interleaved buck active power filter topologies. The 2C IB APF topology is based on the half-bridge interleaved buck inverter and the detailed description and working principle has been presented in previous chapters. The further discussed 3-phase 4-wire interleaved buck active power filter topologies are based on the full-bridge interleaved buck inverter [73,

75]. The input voltage utilization rate of full bridge interleaved buck inverter is twice of the half bridge interleaved inverter and less voltage stress across the power switches [71]. Hence, the single-phase full bridge interleaved buck active power filter has been studied, followed by its working modes.

4.4.1 Working modes of Full-Bridge Interleaved Buck Active Power Filter

Figure 4.5a depicts the single phase conventional full bridge inverter which is used as an active power filter [38]. Further, it is to be noted that the two switches which comprise each inverter leg must operate in a complementary fashion. That is, one switch must be conducted at all times, and both switches are prohibited from conducting at the same time. If somehow, the two power transistors of the same leg gets turned on at the same time, a short circuit current (shoot- through current) flows.

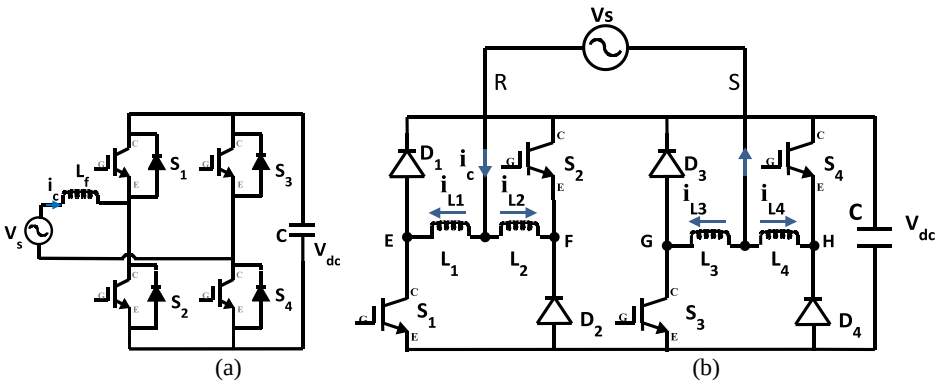


Figure 4.5: (a) Single phase conventional full bridge converter (b) Single phase full bridge interleaved buck (IB) converter

Figure 4.5b shows the single phase full-bridge interleaved buck converter based active power filter [72] and is formed by the decomposition of the generic phase leg of the conventional inverter into the basic switching leg configured with a controllable switch in series with a diode and with coupling inductors L_1, L_2, L_3, and L_4 of same value. By using this topology shoot-through can be eliminated without dead time effect. The concluded equation for the filter current is:

$$i_c = i_{L1} + i_{L2} = -i_{L4} + -i_{L3} \tag{4.7}$$

For modeling, all power switches and diodes have been assumed as ideal devices. From Figure 4.5b, the positive filter current i_c, as assumed is flowing with the circuit elements

S_1, S_4 (power switches), D_1, D_4 (discrete diodes) and L_1, L_4 (coupling inductors). For analyzing the working principle, the considerations are $L_1 = L_4 = L$ and $i_{L1} = -i_{L4}$.

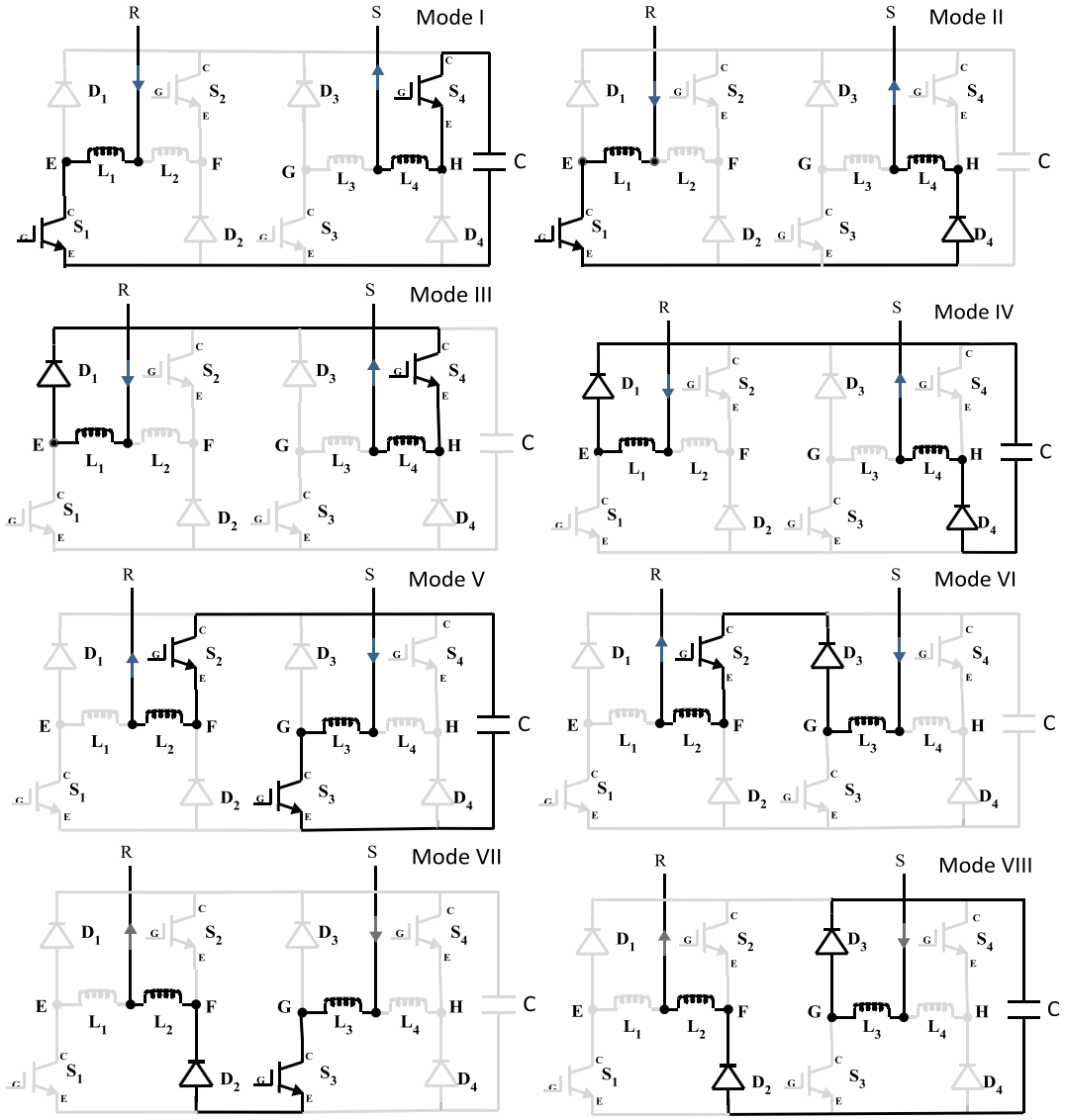


Figure 4.6: Working stages of full-bridge interleaved buck converter based active power filter

When transistors S1 and S4 are turned on simultaneously, the equation for the positive compensating/filter current is

$$L_1 \frac{di_{L1}}{dt} - V_{dc} - L_4 \frac{di_{L4}}{dt} = v_s$$

$$L_1 \frac{di_{L1}}{dt} - L_4 \frac{di_{L4}}{dt} = V_{dc} + v_s$$

$$L \frac{di_{L1}}{dt} + L \frac{di_{L1}}{dt} = V_{dc} + v_s; (\text{as } i_{L1} = -i_{L4} \text{ and } L_1 = L_4 = L) \quad (4.8)$$

$$2L \frac{di_{L1}}{dt} = V_{dc} + v_s$$

Similarly for negative filter current i_c, the associated circuit elements are S_2, S_3 (power switches), D_2, D_3 (discrete diodes) and L_2, L_3 (coupling inductors). The analysis of the negative compensating current is same and hence not described to any further extent. It can be seen from the Figure 4.5b that the diode is connected in reverse series with the power transistors and hence no shoot-through phenomenon. The working stages with positive and negative compensation current are shown in Figure 4.6. The below Table 4.1 give a brief description of the figured working stages.

Table 4.1: Brief description of the single-phase full-bridge IB APF working modes

Filter current	Mode 1	Mode 2	Mode 3	Mode 4
$i_c > 0$	S_1, S_4	S_1, D_4	D_1, S_4	D_1, D_4
Filter current	Mode 5	Mode 6	Mode 7	Mode 8
$i_c < 0$	S_2, S_3	S_2, D_3	D_2, S_3	D_1, D_3

So, by using this full-bridge interleaved buck active power filter, the following 3-phase 4-wire single capacitor full bridge interleaved buck active power filter, 1C 3 FB IB APF and full bridge interleaved buck active power filter, FB IB APF have been modelled.

4.5 Single capacitor, three full-bridge Interleaved Buck Active Power Filter (1C 3FB IB APF)

The voltage, that appears across the split capacitor interleaved buck active power filter, 2C IB APF is the three phase voltage (400 V) and therefore the required dc-link bus voltage increases, which raises the rating of the inverter (particularly power device voltage rating).

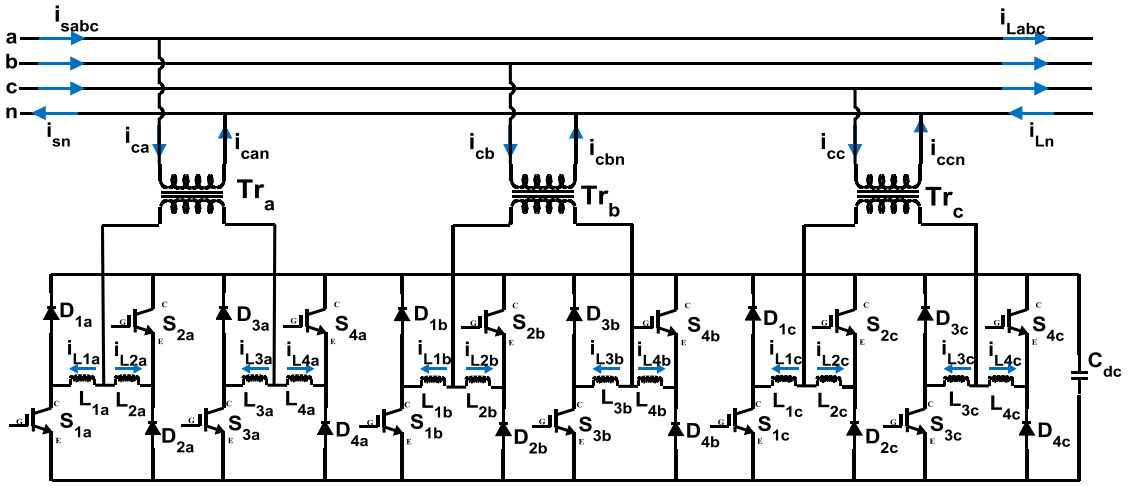


Figure 4.7: Single capacitor, three full-bridge interleaved buck active power filter (1C 3FB IB APF)

At the same time, 230 V appears across each interleaved buck full bridge inverter of this modelled single capacitor full bridge interleaved buck active power filter in Figure 4.7, as three single phase interleaved-buck full bridge inverters connect with a common dc bus to the respective phase of 3-phase 4-wire distribution system. Hence the dc-link voltage requirement is less with low voltage stress on the switches.

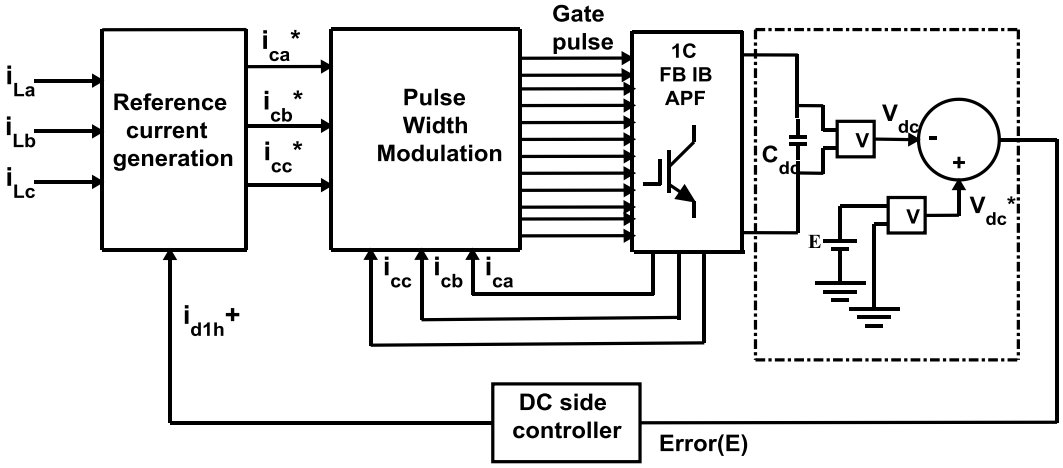


Figure 4.8: Block diagram of dc-link voltage regulation in single capacitor, three full-bridge interleaved buck active power filter (1C 3FB IB APF)

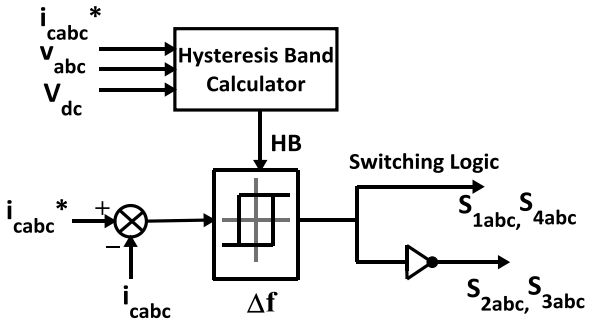


Figure 4.9: Switching pulse generation

This concludes that, low voltage rating of the power device can be used for same power application as compared to the 2C IB APF. Due to the use of low voltage rated power switches in the proposed topology, this can be used for increased power application. In addition, the control strategy is very simple as three interleaved buck full bridge inverter connected to the three phase distribution system is being controlled by a single dc–link capacitor. Here only one voltage sensor is required to track the dc-link voltage for the modelled topology performance. The eminent features of this topology are; the high utilization of dc-link voltage, low voltage stress and simple control. The disadvantages concerned with this proposed topology are more number of switches, more coupling

inductances and usage of isolation transformer as compared to the 2C IB APF. This all can be partly counterbalanced by relatively less rating of the power device.

In this configuration, in all, 12 power IGBTs, 12 discrete diodes, 12 coupling inductors is taken to realize the single capacitor interleaved buck full-bridge inverter based active power filter. These three full-bridge interleaved buck inverters are connected with the 3-phase 4-wire distribution system with their individual single phase isolation transformer.

The advantages of the proposed 1C 3FB IB APF over 3-phase 4-wire 2C IB APF are:

i. The dc-link bus voltage is decreased by $\sqrt{3}$ times, resulting in the reduction of the inverter rating mainly the IGBTs power switch voltage rating and hence the low voltage stress on the power switches.
ii. As the dc-link voltage decreases by $\sqrt{3}$ times in the proposed topology, the same can be used for greater power application.
iii. Simple control as only one dc-link voltage has to be considered for reference compensating current generation.

In single capacitor full-bridge interleaved buck active power filter topology (1C FB IB APF), the neutral current gets compensated indirectly. The following equations are valid for single capacitor full-bridge interleaved buck shunt active power filter (1C FB IB APF):

$$\begin{aligned} i_{sa} + i_{sb} + i_{sc} &= i_{sn} \\ i_{La} + i_{Lb} + i_{Lc} &= i_{Ln} \\ i_{ca} + i_{cb} + i_{cc} &= i_{cn} \end{aligned} \tag{4.9}$$

where, i_{sa}, i_{sb}, i_{sc} and i_{sn} represents the corresponding source phase currents and source neutral current. Similarly, the phase load currents and load neutral current is represented by i_{La}, i_{Lb}, i_{Lc} and i_{Ln} and the compensating phase currents and compensating neutral current are signified by i_{ca}, i_{cb}, i_{cc} and i_{cn} respectively. Again the compensating current can be depicted as the sum of the two coupling inductor current for each phase and are as follows [72]:

$$\begin{aligned} i_{ca} &= i_{L1a} + i_{L2a} = -i_{L3a} - i_{L4a} \\ i_{cb} &= i_{L1b} + i_{L2b} = -i_{L3b} - i_{L4b} \\ i_{cc} &= i_{L1c} + i_{L2c} = -i_{L3c} - i_{L4c} \end{aligned} \tag{4.10}$$

The minimum dc-link voltage required by this three interleaved-buck full-bridge active power filter can be determined by the mathematical relationship [40] as:

$$V_{dc\,min} = \sqrt{2}V_{s\,rms} = \sqrt{2} * 230 = 325\ V \quad (4.11)$$

Here the dc-link bus voltage has been chosen as 450 V for good performance. However, this topology can be used for more power rating system as compared to 2C IB APF and 4L IB APF.

Figure 4.8 shows the closed loop block diagram of the dc-link voltage regulation and can be seen that only one capacitor voltage needs to be track of the reference compensating current generation. Here, twelve switching pulses are required to generate by the i_d-i_q control scheme for the 1C 3-phase full bridge interleaved buck inverter. The adaptive hysteresis current controlled pulse width modulation technique has been used for the generation of switching pulse to the power devices and is represented in Figure 4.9.

4.6 Three-phase four-wire Full-Bridge Interleaved Buck Active Power Filter (FB IB APF)

Here also, in the FB IB-APF topology, 12 power switches are being used to realize the 3-phase 4-wire system, i.e. 4 power switches in each phase [73, 47]. In this topology, three single phase full bridge interleaved buck inverter is being connected with each particular phase and neutral. This configuration has also the advantage of reduced voltage stress across the switches, i.e. only the single-phase voltage appear across the switches and hence the reference dc-link voltage needed is reduced as compared to 3-phase 2C interleaved buck converter APF topology.

Again, in this topology only one capacitor voltage is essential for reference current generation by i_d-i_q control strategy, out of the three individual phase FB IB converter capacitor for harmonic compensation of source current and hence decreases the complexity of voltage regulation. More important, the requirements of isolation transformers get eliminated with this topology.

The adaptive hysteresis pulse width modulation technique [86] has been used for the generation of the switching pattern to the full bridge interleaved buck inverter power switches and is same as 1C 3FB IB APF switching generation scheme demonstrated in Figure 4.9.

Both proportional integral (PI) and Type-1 fuzzy logic controller have been taken for error voltage minimization in the dc-link voltage regulation scheme as can be seen in Figure 4.11.

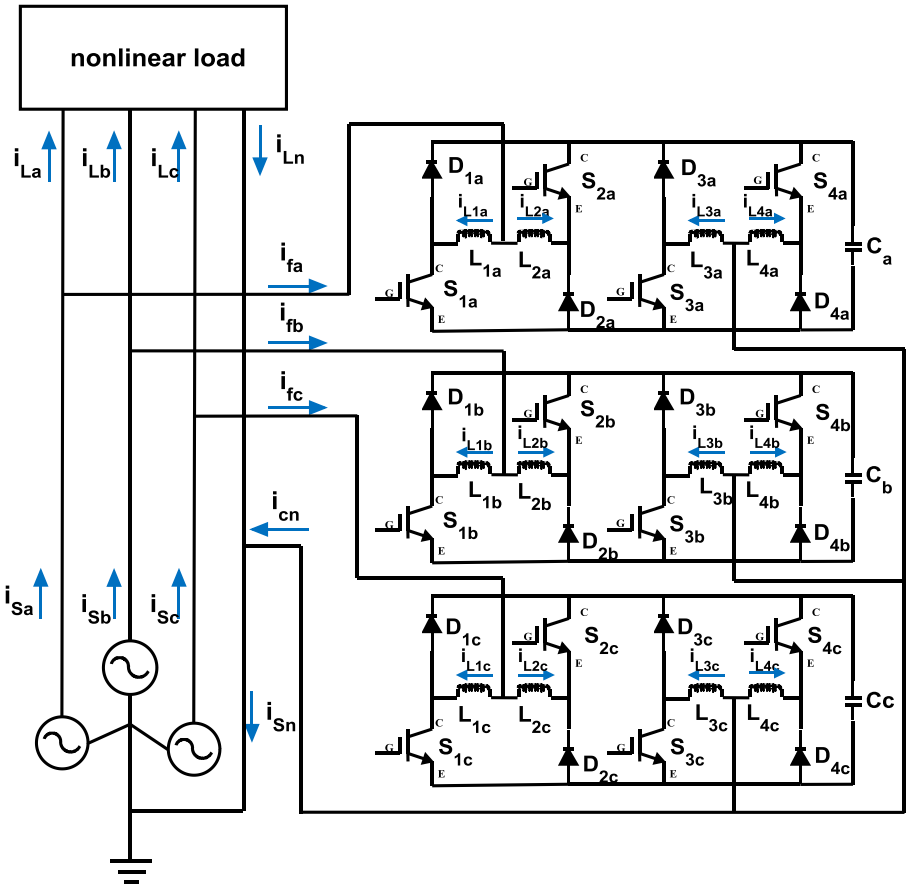


Figure 4.10: 3-phase 4-wire full-bridge interleaved buck active power filter (FB IB APF)

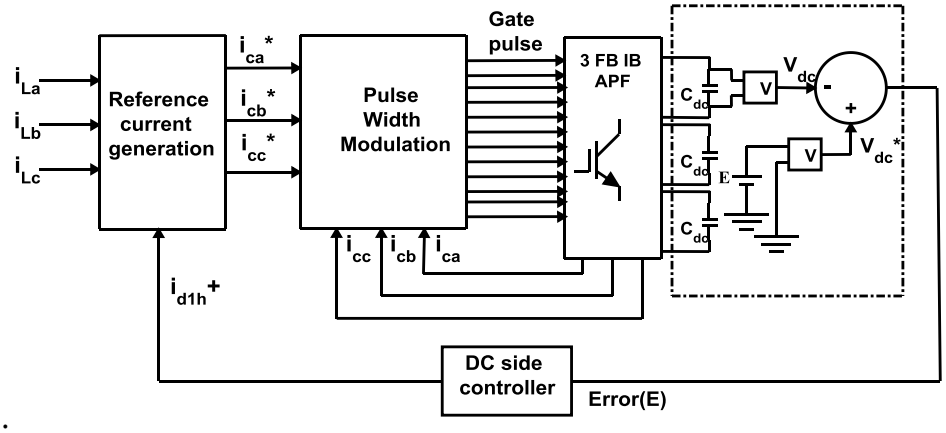


Figure 4.11: Block diagram of dc-link voltage regulation in 3-phase 4-wire full-bridge interleaved buck active power filter (3-phase 4-wire FB IB APF)

For the 3-phase 4-wire FB IB-APF, the following equations are valid as same as 1C 3FB IB APF:

$$\begin{aligned} i_{sa} + i_{sb} + i_{sc} &= i_{sn} \\ i_{La} + i_{Lb} + i_{Lc} &= i_{Ln} \\ i_{ca} + i_{cb} + i_{cc} &= i_{cn} \end{aligned} \tag{4.12}$$

where, i_{sa}, i_{sb}, i_{sc} and i_{sn} are the corresponding source phase currents and source neutral current, i_{La}, i_{Lb}, i_{Lc} and i_{Ln} are the corresponding phase load currents and load neutral current and i_{ca}, i_{cb}, i_{cc} and i_{cn} are the corresponding compensating phase currents and compensating neutral current. Again the compensating current can be depicted as the sum of the two coupling inductors current for each phase [75] and are as follows:

$$\begin{aligned} i_{ca} &= i_{L1a} + i_{L2a} = -i_{L4a} - i_{L3a} \\ i_{cb} &= i_{L1b} + i_{L2b} = -i_{L4b} - i_{L3b} \\ i_{cc} &= i_{L1c} + i_{L2c} = -i_{L4c} - i_{L3c} \end{aligned} \tag{4.13}$$

In conclusive, the additional distinguished features of 3-phase 4-wire FB IB-APF are same as 1C 3FB IB APF with the additional advantages and are followed:

i. Only one dc-link capacitor voltage is being used out of three for reference current generation by i_d-i_q control strategy and hence simple control as compared to 2C IB-APF.
ii. This topology has a flexible, modular design, transformerless connection, less maintenance and higher fault tolerance.

Nearly all the advantages of 1C 3FB IB APF are featured in this 3-phase 4-wire FB IB APF except the last point of the above distinguished features, which makes the use of 3-phase 4-wire FB IB APF more compatible with the distribution system. The high cost of the proposed 3-phase 4-wire FB IB-APF owing to the more numbers of inductors used as compared to 3-phase 4-wire split capacitor interleaved buck active power filter topology [9], can be counterbalanced with the cost of less rated switching devices and snubber circuit.

Most importantly, it can be used for higher power application as compared to 2C IB APF and 4L IB APF. Since lower rated switches and other accessories are used, the proposed inverter topology is cost effective for higher power application. Again, as this topology becomes free from the transformer, the weight is less as compared to the 1C 3FB IB APF.

Table 4.2 epitomises a clear idea about the different features viz. no. of power devices, no. of diodes, no. of coupling inductors, extra sensor requirement, necessity of coupling transformers and about the neutral current compensation of the various 3-phase 4-wire IB APFs.

Table 4.2: Comparison of various features of 3-phase 4-wire IB APF topologies

Features	2C IB APF	4L IB APF	1C 3FB IB APF	FB IB APF
No. of power devices	6	8	12	12
No of diodes	6	8	12	12
No of coupling inductors	6	8	12	12
dc bus capacitors	2	1	1	1
Extra sensor requirement	1 more dc bus voltage sensor	1more neutral current sensor	None	None
Necessity of coupling transformers	Not required	Not required	3	Not required
Neutral current compensation	Indirect	Direct and hence better neutral current compensation	Indirect	Indirect

4.7 System Performance of 2C IB APF, 4-Leg IB APF, 1C 3FB IB APF and FB IB APF topologies by i_d-i_q control strategy with PI and T1FLC for sinusoidal, unbalanced sinusoidal and non-sinusoidal voltage source condition

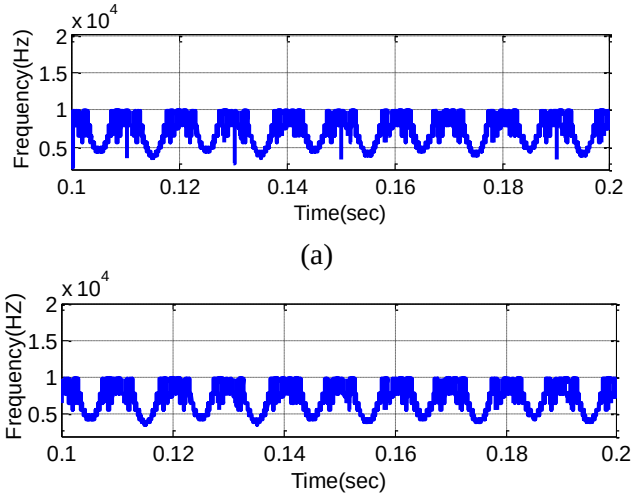


Figure 4.12: Simulation result of switching frequency for (a) adaptive hysteresis current controller with PI controller (b) adaptive hysteresis current controller with Type-1 fuzzy logic controller

Sinusoidal voltage source condition with unbalanced load

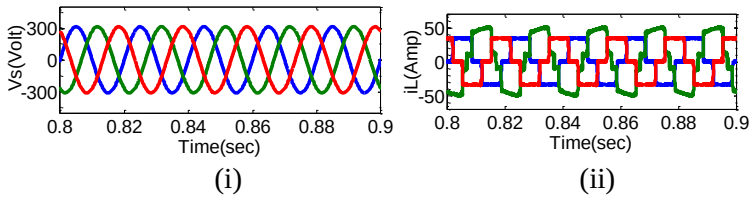


Figure 4.13a: (i) Sinusoidal source voltage, v_s (ii) Unbalanced load current, i_L

Split capacitor 3-phase 4-wire IB-APF (2C IB APF) using PI controller

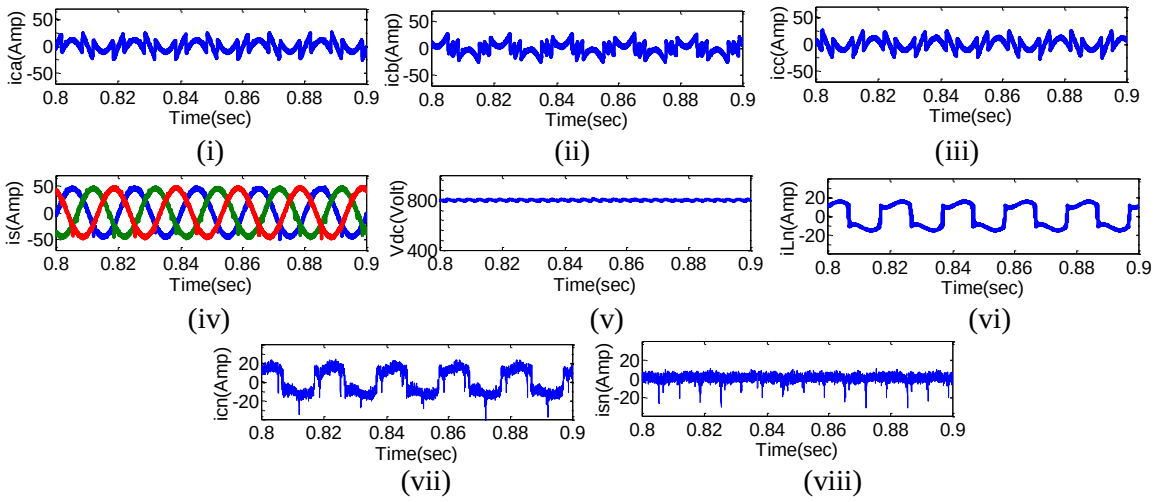


Figure 4.13b: Simulation results of (i) phase *a* filter current, i_{ca} (ii)) phase *b* filter current, i_{cb} (iii) phase *c* filter current, i_{cc} (iv) source current, i_s (v) capacitor voltage, V_{dc} (vi) load neutral current, i_{Ln} (vii) filter neutral current, i_{cn} and (viii) source neutral current i_{sn} for 2C IB APF using PI controller under sinusoidal volatge source condition.

Split capacitor 3-phase 4-wire IB-APF (2C IB APF) using Type-1 fuzzy controller

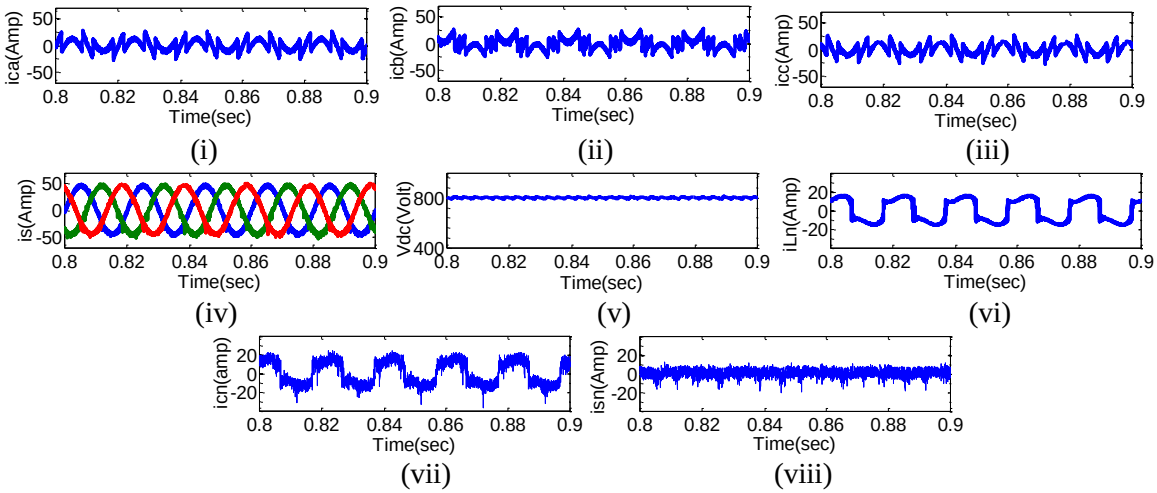


Figure 4.13c: Simulation results of (i) phase *a* filter current, i_{ca} (ii) phase *b* filter current, i_{cb} (iii) phase *c* filter current, i_{cc} (iv) source current, i_s (v) capacitor voltage, V_{dc} (vi) load neutral current, i_{Ln} (vii) filter neutral current, i_{cn} and (viii) source neutral current i_{sn} for 2C IB APF using Type-1 fuzzy logic controller (T1FLC) under sinusoidal volatge source condition.

Simulation results of 4-Leg IB APF, 1C FB IB APF and 3FB IB APF using PI controller

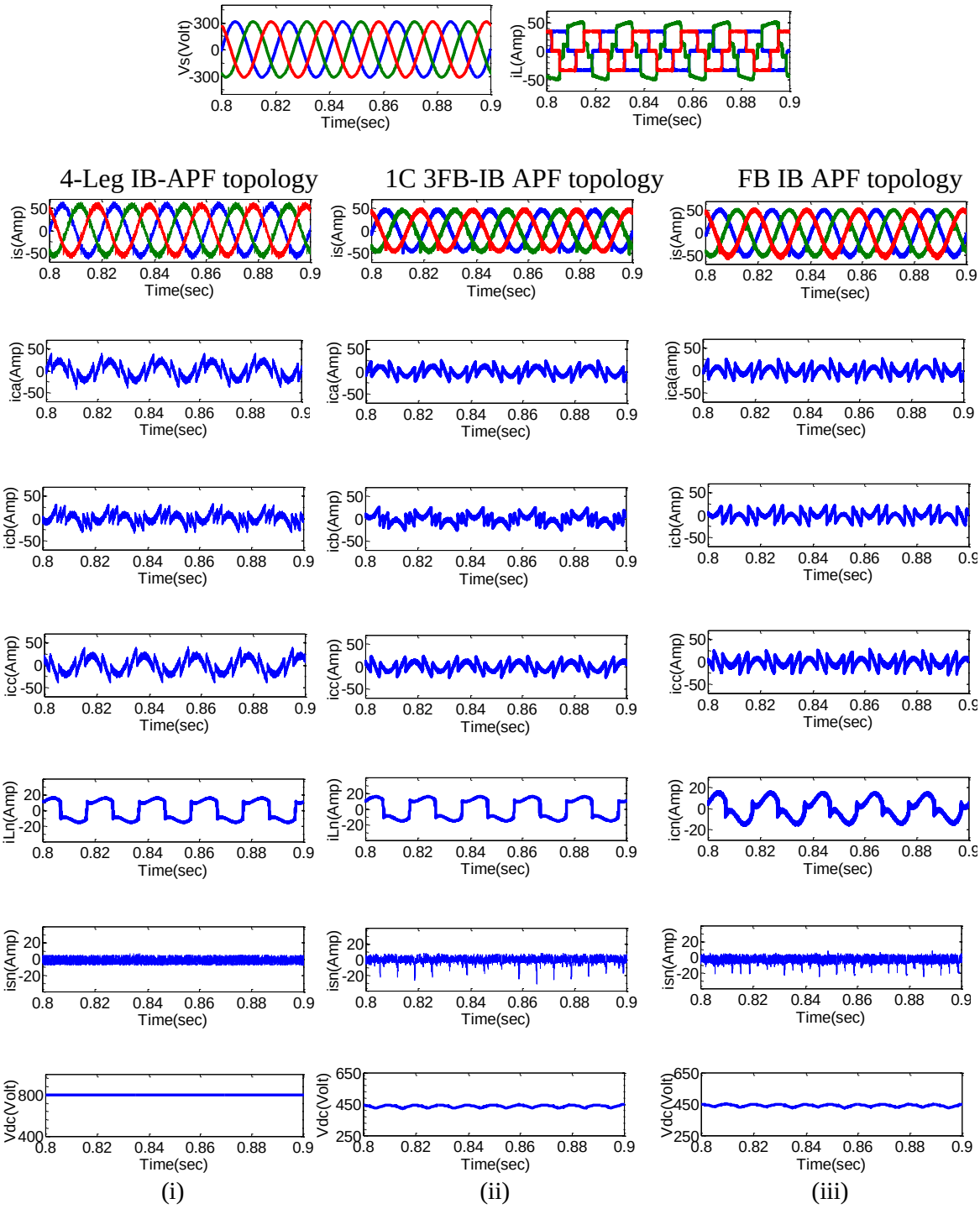


Figure 4.14: Simulation results of source voltage (v_s), load current (i_L), phase filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}) using PI controller under sinusoidal voltage source condition for (i) four-leg interleaved buck active power filter, 4L IB APF (ii) single capacitor three full bridge interleaved buck active power filter, 1C 3FB IB APF and (iii) 3-phase 4-wire full bridge interleaved buck active power filter, FB IB APF

Simulation results of 4-Leg IB APF, 1C 3FB IB APF and FB IB APF using Type-1 fuzzy logic controller

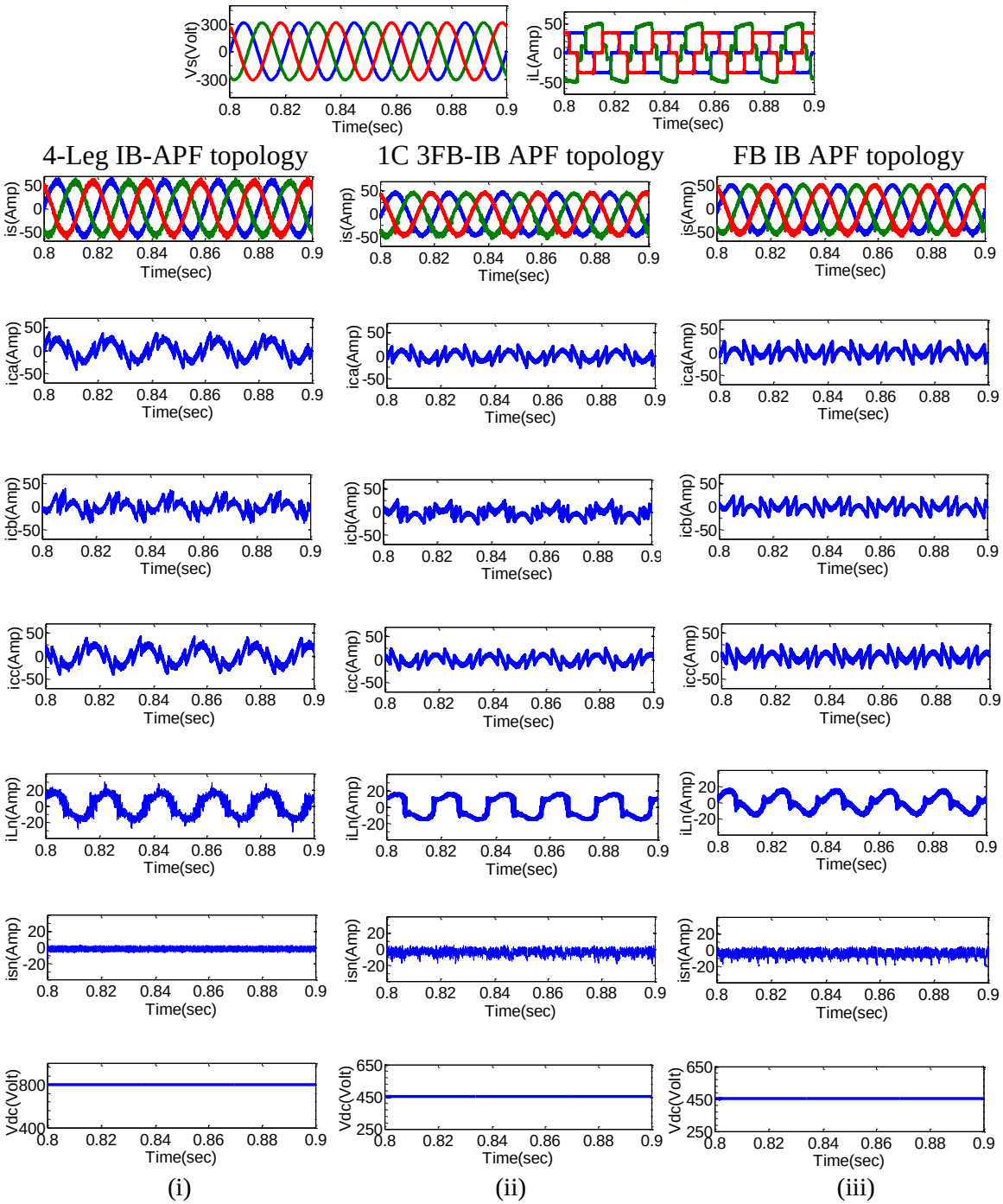


Figure 4.15: Simulation results of source voltage (v_s), load current (i_L), source current (i_s), phase filter current (i_c), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}) using Type-1 fuzzy logic controller (T1FLC) under sinusoidal voltage source condition for (i) four-leg interleaved buck active power filter, 4L IB APF (ii) single capacitor three full bridge interleaved buck active power filter, 1C 3FB IB APF and (iii) 3-phase 4-wire full bridge interleaved buck active power filter, FB IB APF

OPAL-RT results of 2C IB APF, 4-Leg IB APF, 1C 3FB IB APF and FB IB APF using PI controller

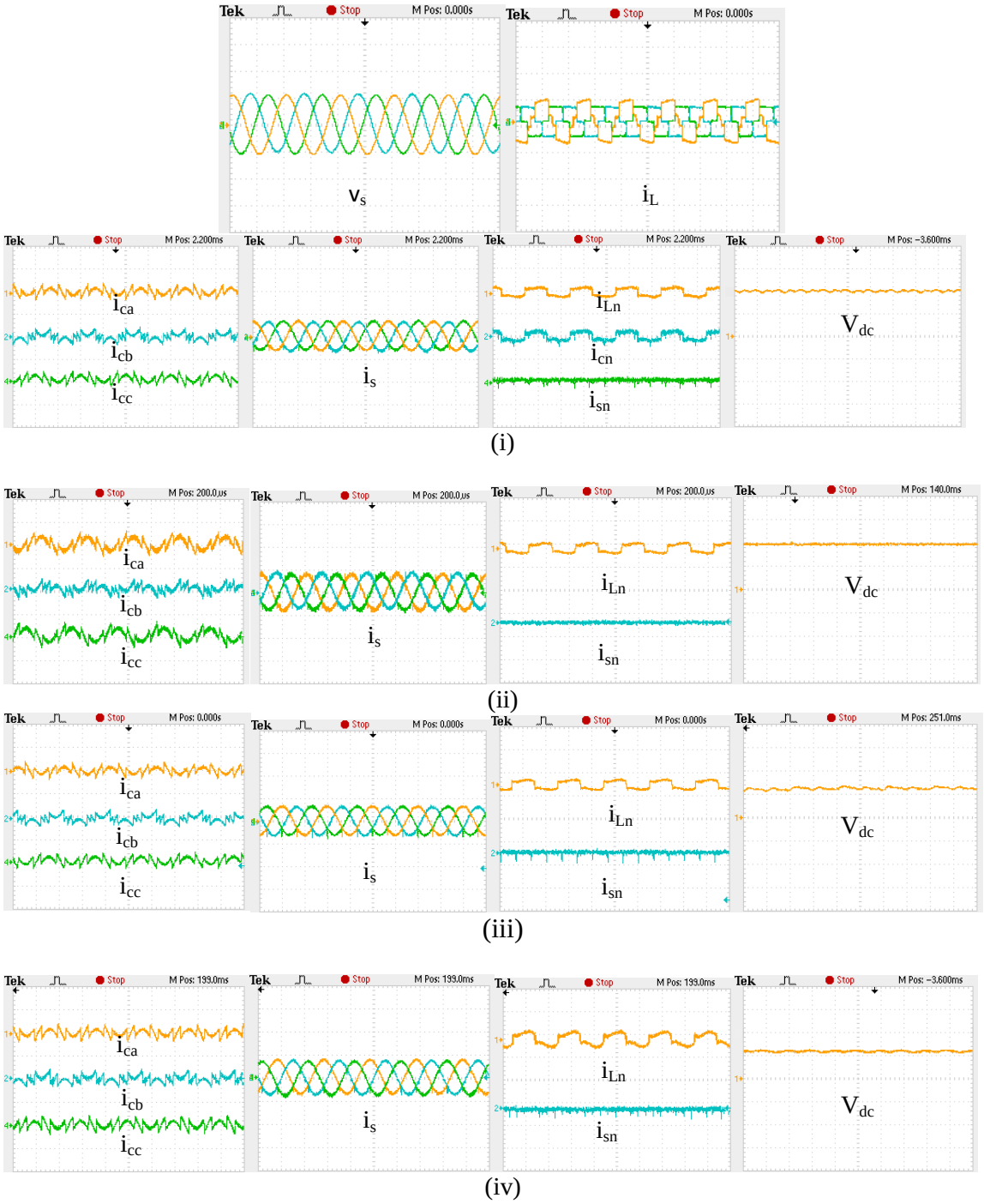
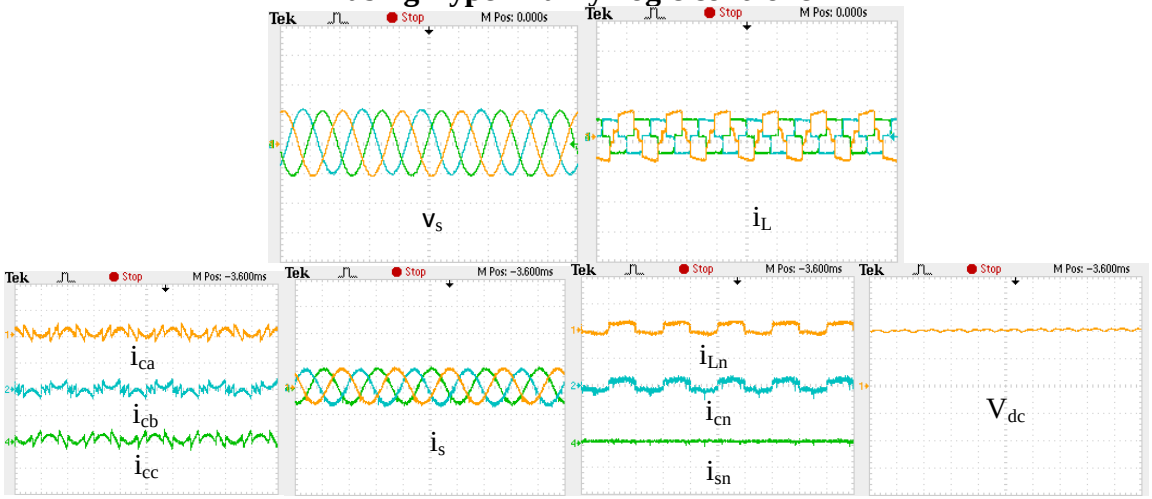
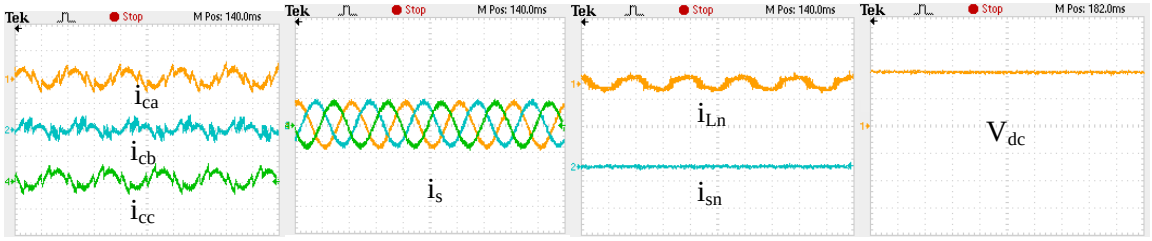


Figure 4.16: OPAL-RT results of source voltage (v_s), load current (i_L), phase filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}) using PI controller under sinusoidal voltage source condition for (i) split capacitor interleaved buck active power filter, 2C IB APF (ii) four-leg interleaved buck active power filter, 4L IB APF (iii) single capacitor three full bridge interleaved buck active power filter, 1C 3FB IB APF and (iv) 3-phase 4-wire full bridge interleaved buck active power filter, FB IB APF

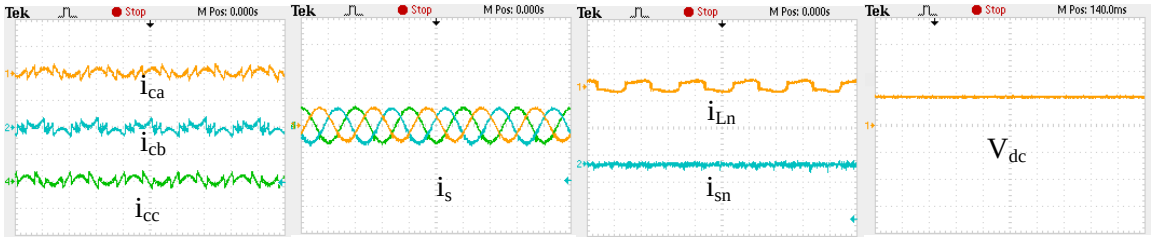
OPAL-RT results of 2C IB APF, 4-Leg IB APF, 1C 3FB IB APF and FB IB APF using Type-1 fuzzy logic controller



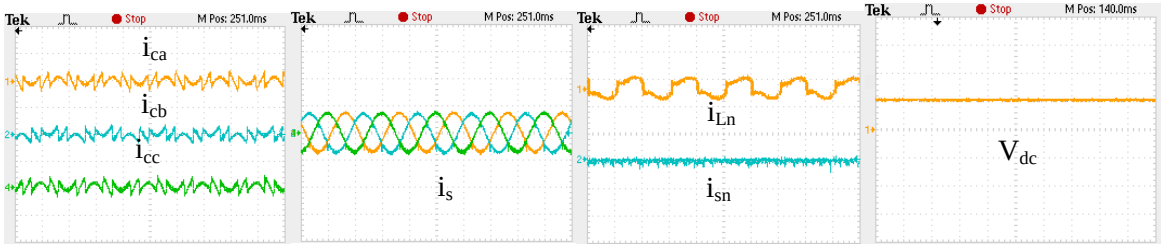
(i)



(ii)



(iii)



(iv)

Figure 4.17: OPAL-RT results of source voltage (v_s), load current (i_L), phase filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}) using Type-1 fuzzy logic controller (T1FLC) under sinusoidal voltage source condition for(i) split capacitor interleaved buck active power filter, 2C IB APF (ii) four-leg interleaved buck active power filter, 4L IB APF (iii) single capacitor three full bridge interleaved buck active power filter, 1C 3FB IB APF and (iv) 3-phase 4-wire full bridge interleaved buck active power filter, FB IB APF

Unbalanced sinusoidal voltage source condition with unbalanced load

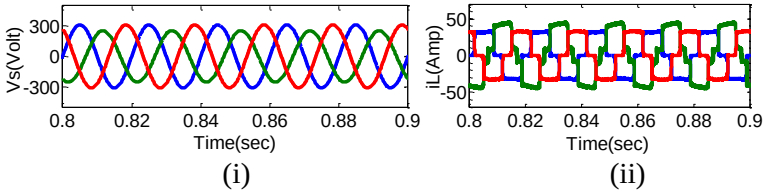


Figure 4.18a: (i) Sinusoidal source voltage, v_s (ii) Unbalanced load current, i_L

Split capacitor 3-phase 4-wire IB-APF (2C IB APF) using PI controller

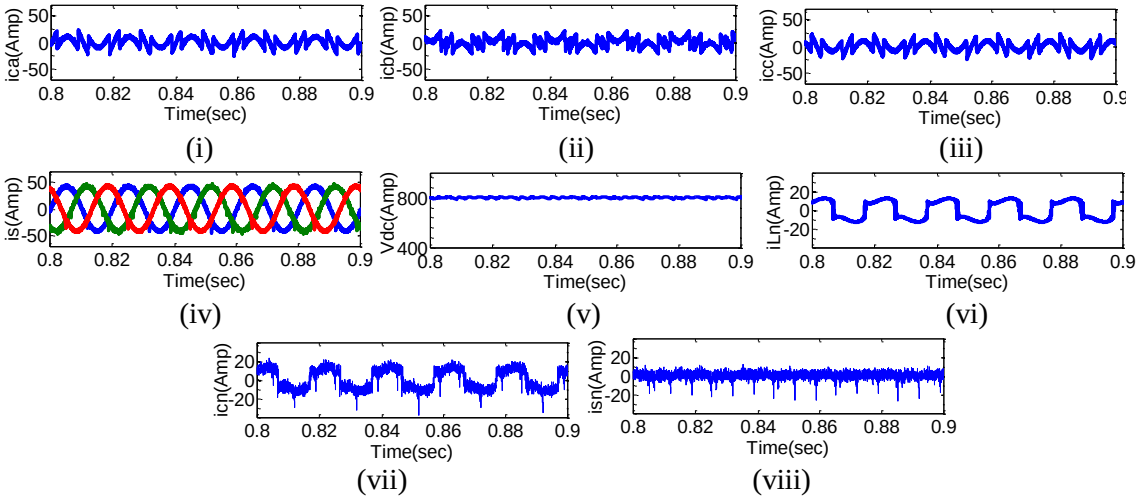


Figure 4.18b: Simulation results of (i) phase *a* filter current, i_{ca} (ii)) phase *b* filter current, i_{cb} (iii) phase *c* filter current, i_{cc} (iv) source current, i_s (v) capacitor voltage,V_{dc} (vi) load neutral current, i_{Ln} (vii) filter neutral current, i_{cn} and (viii) source neutral current i_{sn} for 2C IB APF using PI controller under unbalanced sinusoidal volatge source condition.

Split capacitor 3-phase 4-wire IB-APF (2C IB APF) using Type-1 fuzzy logic controller

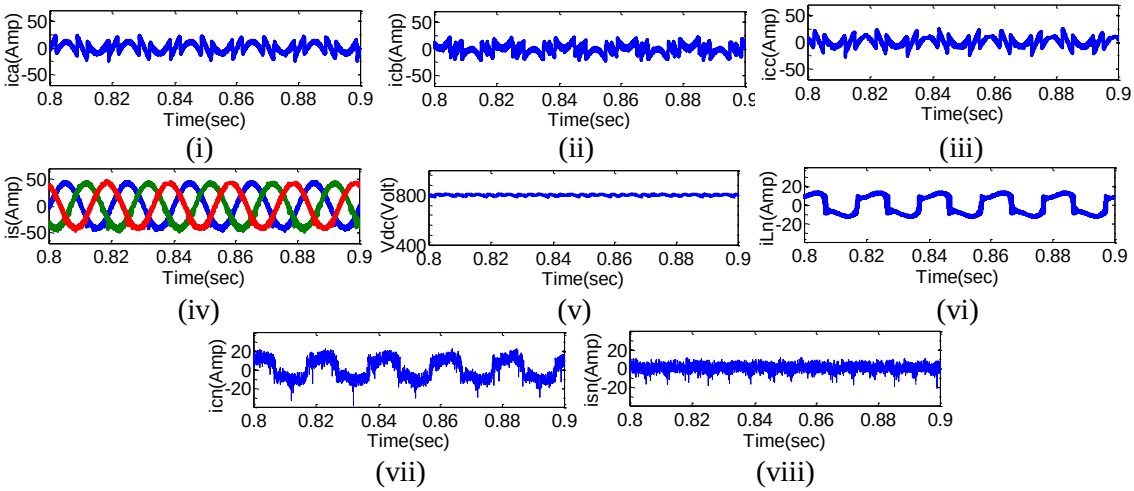


Figure 4.18c: Simulation results of (i) phase *a* filter current, i_{ca} (ii)) phase *b* filter current,i_{cb} (iii) phase *c* filter current, i_{cc} (iv) source current, i_s (v) capacitor voltage,V_{dc} (vi) load neutral current, i_{Ln} (vii) filter neutral current, i_{cn} and (viii) source neutral current i_{sn} for 2C IB APF using Type-1 fuzzy logic controller (T1FLC) under unbalanced sinusoidal volatge source condition.

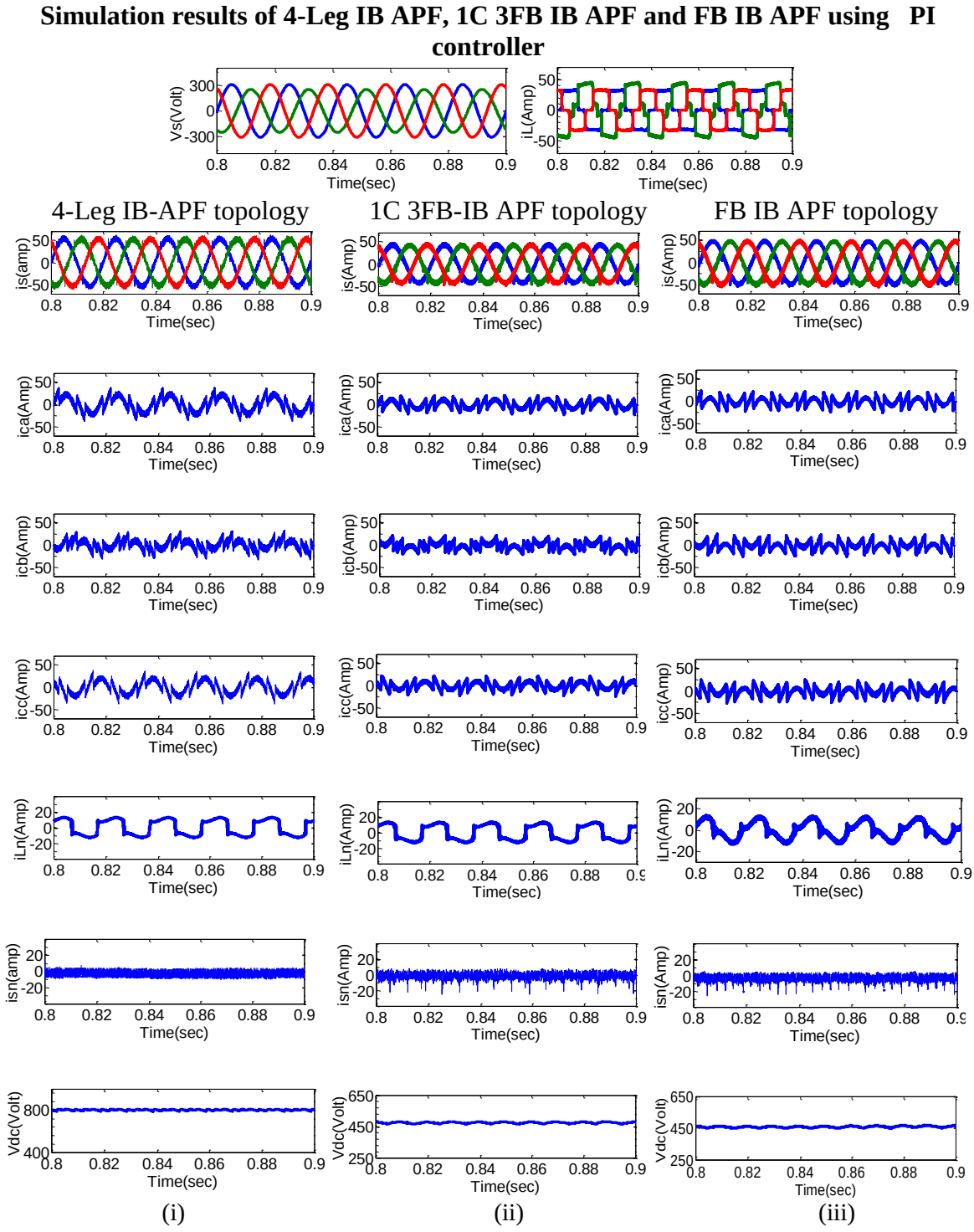


Figure 4.19: Simulation results of source voltage (v_s), load current (i_L), phase filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}) using PI controller under unbalanced sinusoidal voltage source condition for (i) four-leg interleaved buck active power filter, 4L IB APF (ii) single capacitor three full bridge interleaved buck active power filter, 1C 3FB IB APF and (iii) 3-phase 4-wire full bridge interleaved buck active power filter, FB IB APF

Simulation results of 4-Leg IB APF, 1C 3FB IB APF and FB IB APF using Type-1 fuzzy logic controller

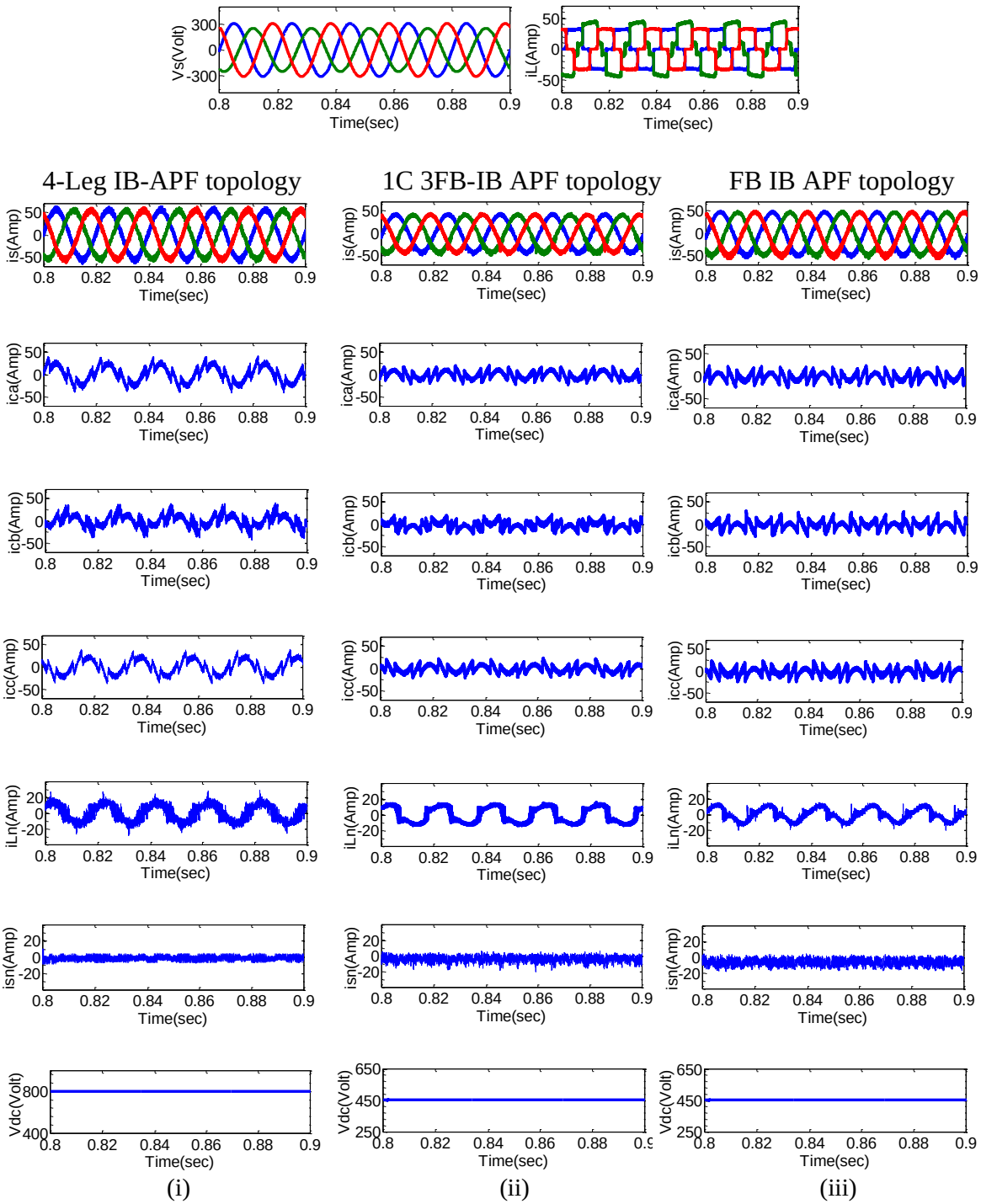
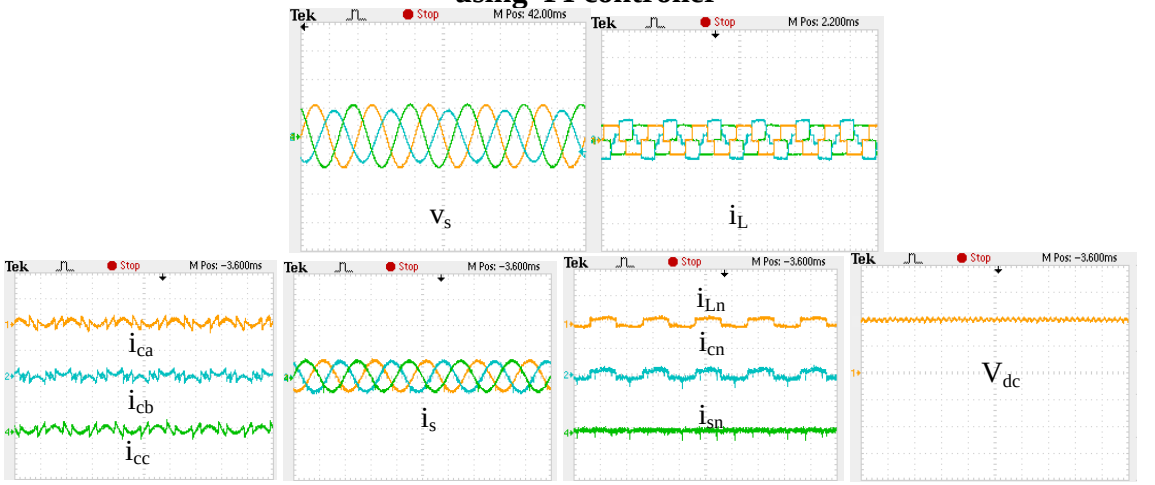
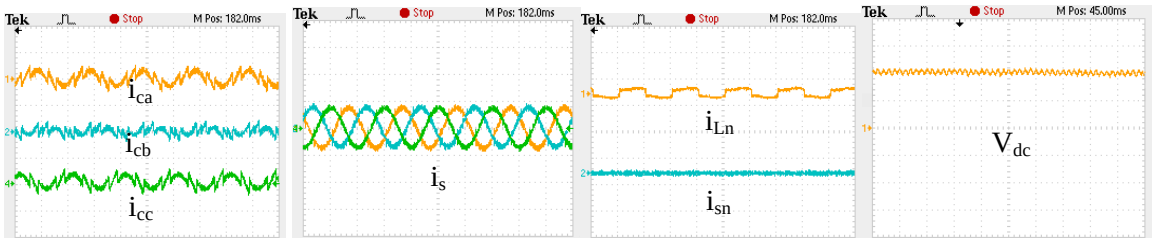


Figure 4.20: Simulation results of source voltage (v_s), load current (i_L), phase filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}) using Type-1 fuzzy logic controller (T1FLC) under unbalanced sinusoidal voltage source condition for (i) four-leg interleaved buck active power filter, 4L IB APF (ii) single capacitor three full bridge interleaved buck active power filter, 1C 3FB IB APF and (iii) 3-phase 4-wire full bridge interleaved buck active power filter, FB IB APF

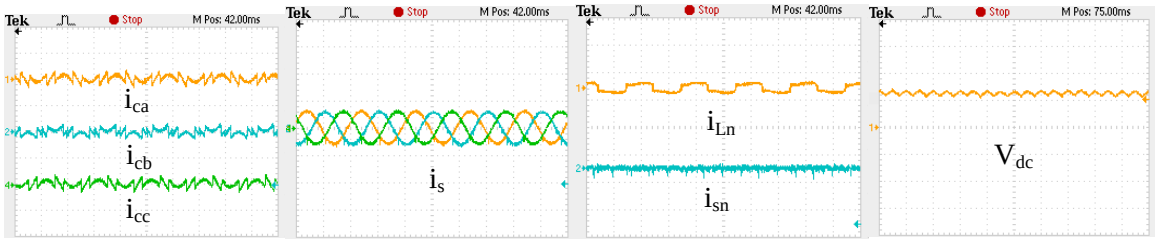
OPAL-RT results of 2C IB APF, 4-Leg IB APF, 1C 3FB IB APF and FB IB APF using PI controller



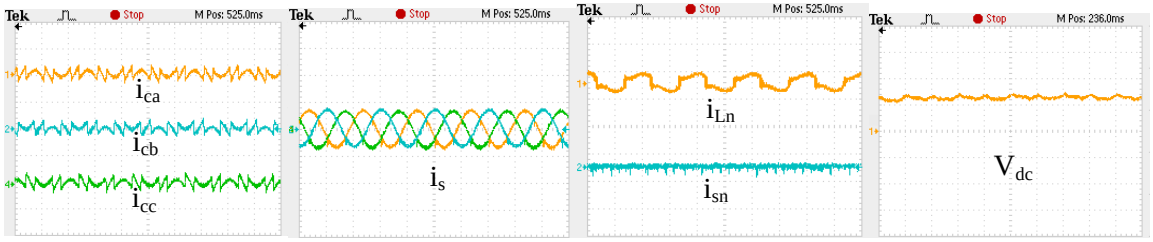
(i)



(ii)



(iii)



(iv)

Figure 4.21: OPAL-RT results of source voltage (v_s), load current (i_L), phase filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}) using PI controller under unbalanced sinusoidal voltage source condition for (i) split capacitor interleaved buck active power filter, 2C IB APF (ii) four-leg interleaved buck active power filter, 4L IB APF (iii) single capacitor three full bridge interleaved buck active power filter, 1C 3FB IB APF and (iv) 3-phase 4-wire full bridge interleaved buck active power filter, FB IB APF

OPAL-RT results of 2C IB APF, 4-Leg IB APF, 1C 3FB IB APF and FB IB APF using Type-1 fuzzy logic controller

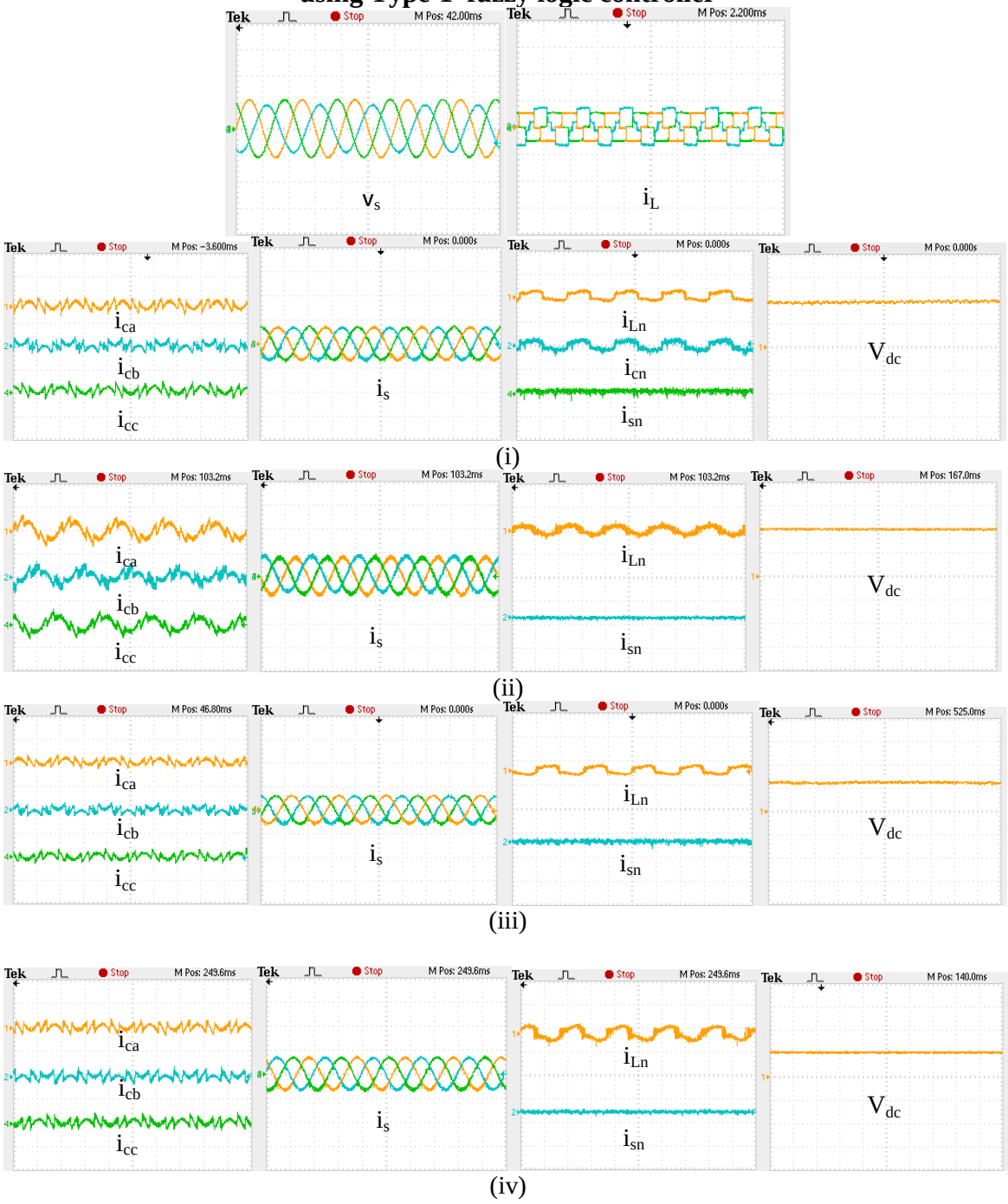


Figure 4.22: OPAL-RT results of source voltage (v_s), load current (i_L), phase filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}) using Type-1 fuzzy logic controller (T1FLC) under unbalanced sinusoidal voltage source condition for (i) split capacitor interleaved buck active power filter, 2C IB APF (ii) four-leg interleaved buck active power filter, 4L IB APF (iii) single capacitor three full bridge interleaved buck active power filter, 1C 3FB IB APF and (iv) 3-phase 4-wire full bridge interleaved buck active power filter, FB IB APF

Non-sinusoidal voltage source condition with unbalanced load

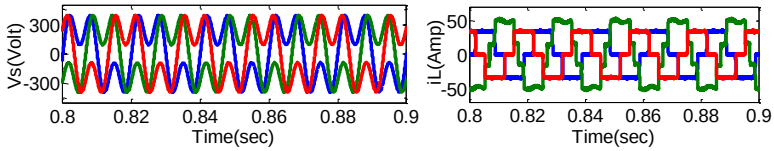


Figure 4.23a: (i) Sinusoidal source voltage, v_s (ii) Unbalanced load current, i_L

Split capacitor 3-phase 4-wire IB-APF (2C IB APF) using PI controller

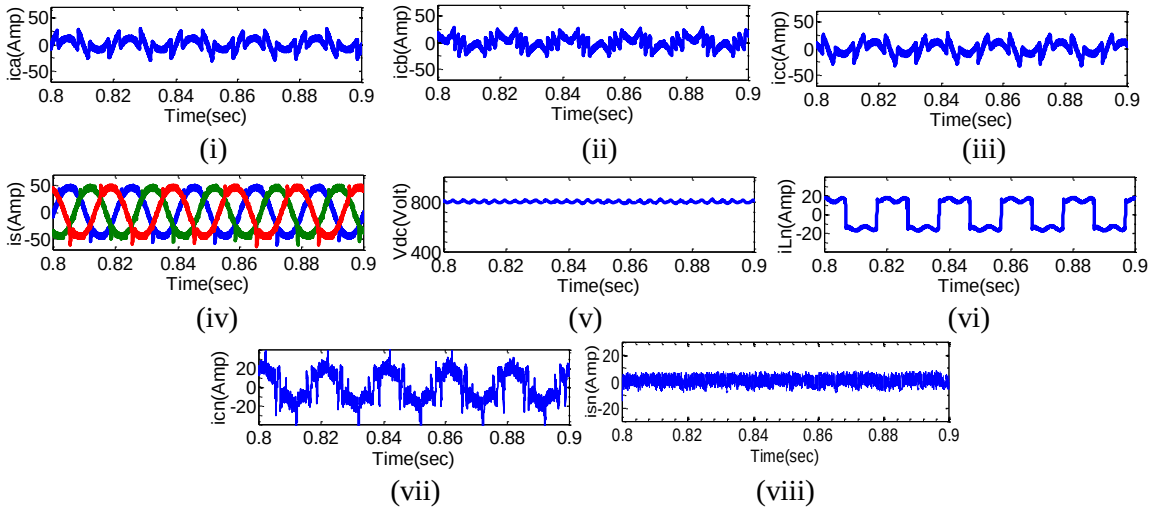


Figure 4.23b: Simulation results of (i) phase *a* filter current, i_{ca} (ii) phase *b* filter current, i_{cb} (iii) phase *c* filter current, i_{cc} (iv) source current, i_s (v) capacitor voltage,V_{dc} (vi) load neutral current, i_{Ln} (vii) filter neutral current, i_{cn} and (viii) source neutral current, i_{sn} for 2C IB APF using PI controller under non-sinusoidal volatge source condition

Split capacitor 3-phase 4-wire IB-APF (2C IB APF) using Type-1 fuzzy logic controller

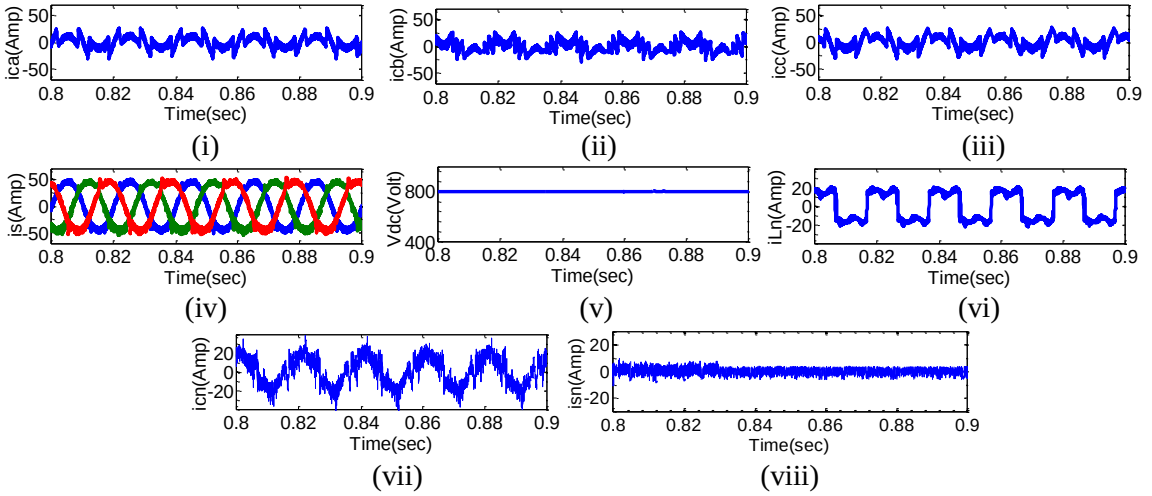
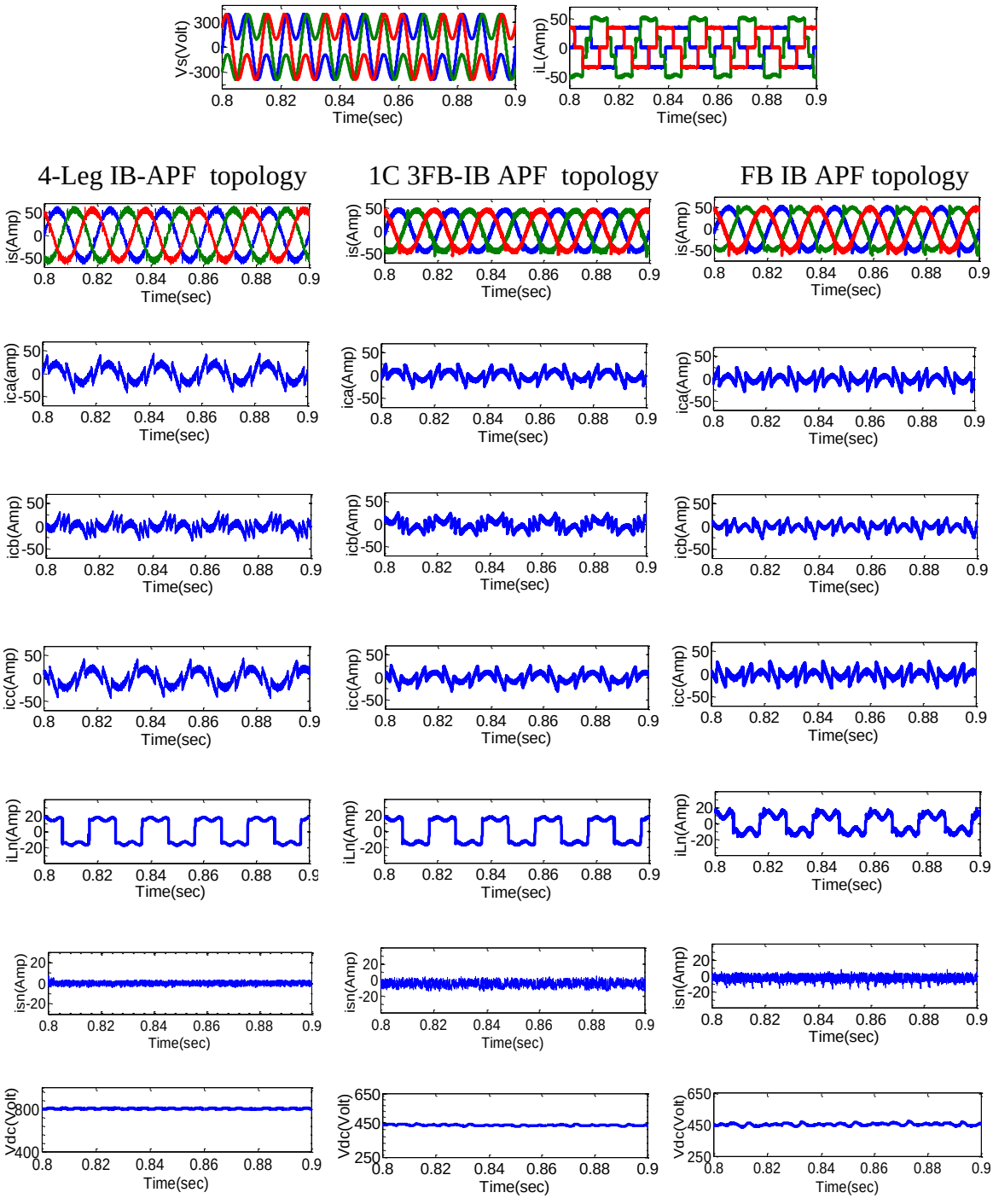


Figure 4.23c: Simulation results of (i) phase *a* filter current, i_{ca} (ii) phase *b* filter current,i_{cb} (iii) phase *c* filter current, i_{cc} (iv) source current, i_s (v) capacitor voltage,V_{dc} (vi) load neutral current, i_{Ln} (vii) filter neutral current, i_{cn} and (viii) source neutral current i_{sn} for 2C IB APF using Type-1 fuzzy logic controller (T1FLC) under non-sinusoidal volatge source condition

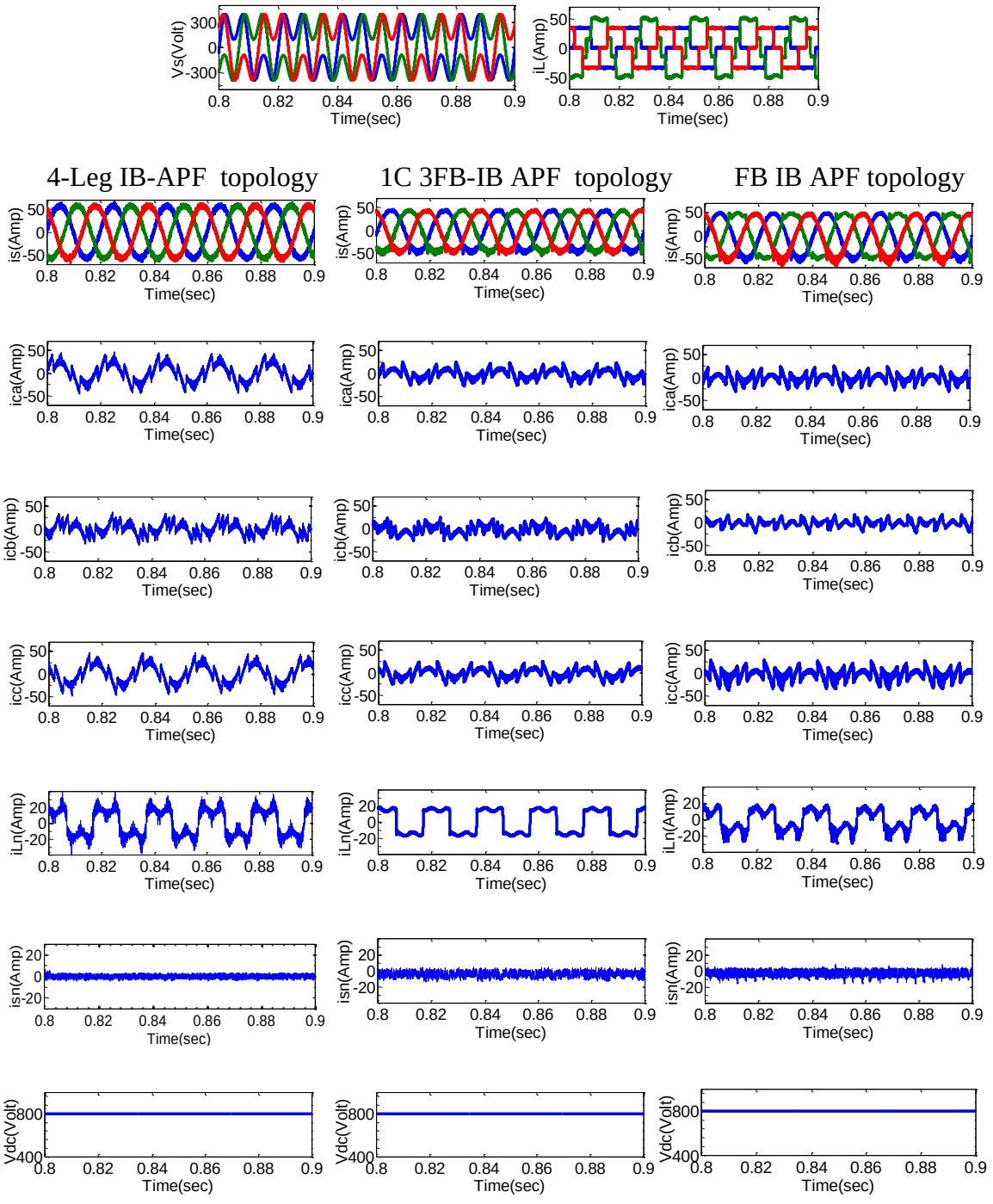
Simulation results of 4-Leg IB APF, 1C 3FB IB APF and FB IB APF using PI controller



(i) (ii) (iii)

Figure 4.24: Simulation results of source voltage (v_s), load current (i_L), phase filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}) using PI controller under non-sinusoidal voltage source condition for (i) four-leg interleaved buck active power filter, 4L IB APF (ii) single capacitor three full bridge interleaved buck active power filter, 1C 3FB IB APF and (iii) 3-phase 4-wire full bridge interleaved buck active power filter, FB IB APF

Simulation results of 4-Leg IB APF, 1C 3FB IB APF and FB IB APF using Type-1 fuzzy logic controller



(i) (ii) (iii)

Figure 4.25: Simulation results of source voltage (v_s), load current (i_L), phase filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}) using Type-1 fuzzy logic controller (T1FLC) under non sinusoidal voltage source condition for (i) four-leg interleaved buck active power filter, 4L IB APF (ii) single capacitor three full bridge interleaved buck active power filter, 1C 3FB IB APF and (iii) 3-phase 4-wire full bridge interleaved buck active power filter, FB IB APF

OPAL-RT results of 2C IB APF, 4-Leg IB APF, 1C 3FB IB APF and FB IB APF using PI controller

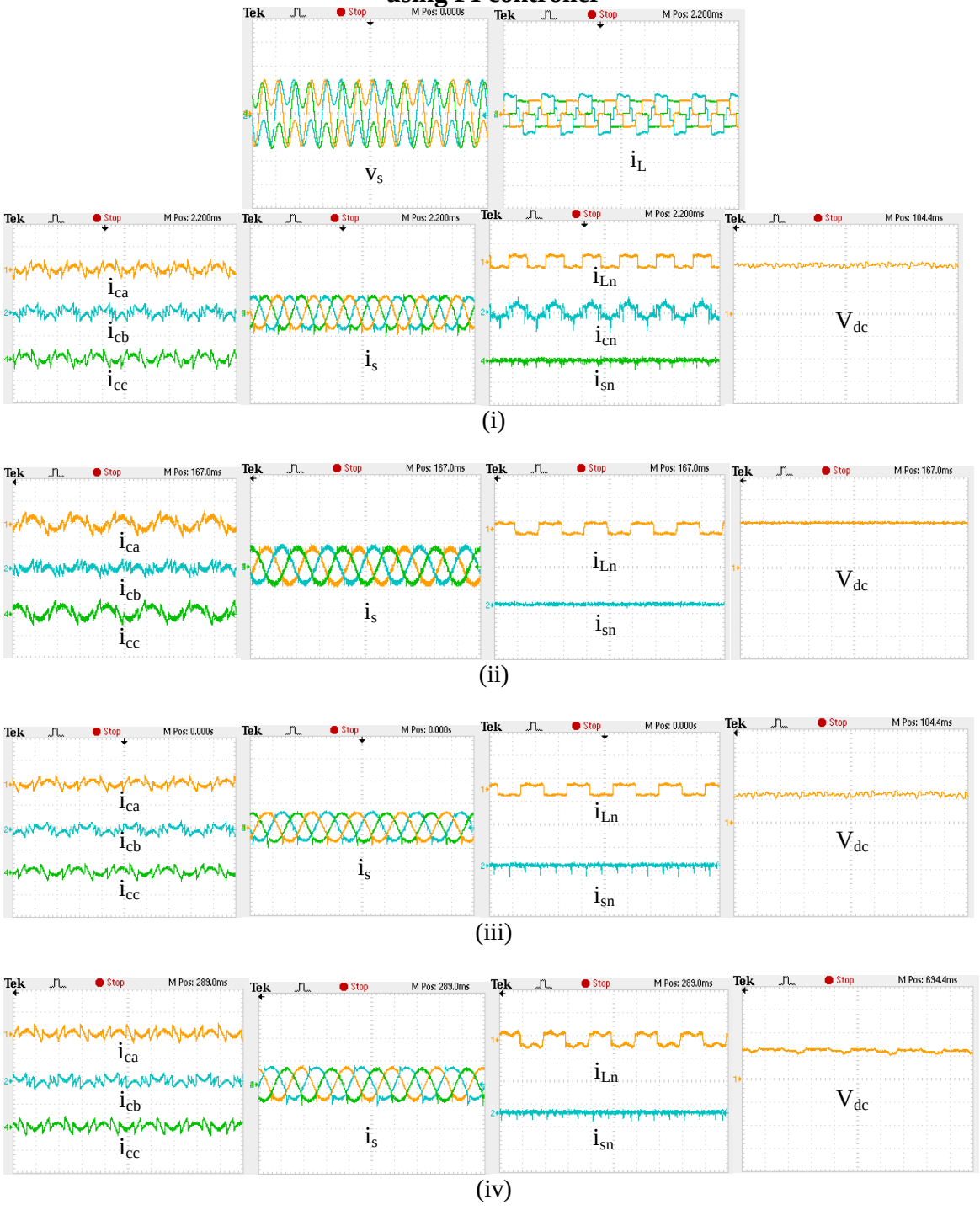


Figure 4.26: OPAL-RT results of source voltage (v_s), load current (i_L), phase filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}) using PI controller under non-sinusoidal voltage source condition for (i) split capacitor interleaved buck active power filter, 2C IB APF (ii) four-leg interleaved buck active power filter, 4L IB APF (iii) single capacitor three full bridge interleaved buck active power filter, 1C 3FB IB APF and (iv) 3-phase 4-wire full bridge interleaved buck active power filter, FB IB APF

OPAL-RT results of 2C IB APF, 4-Leg IB APF, 1C 3FB IB APF and FB IB APF using Type-1 fuzzy logic controller

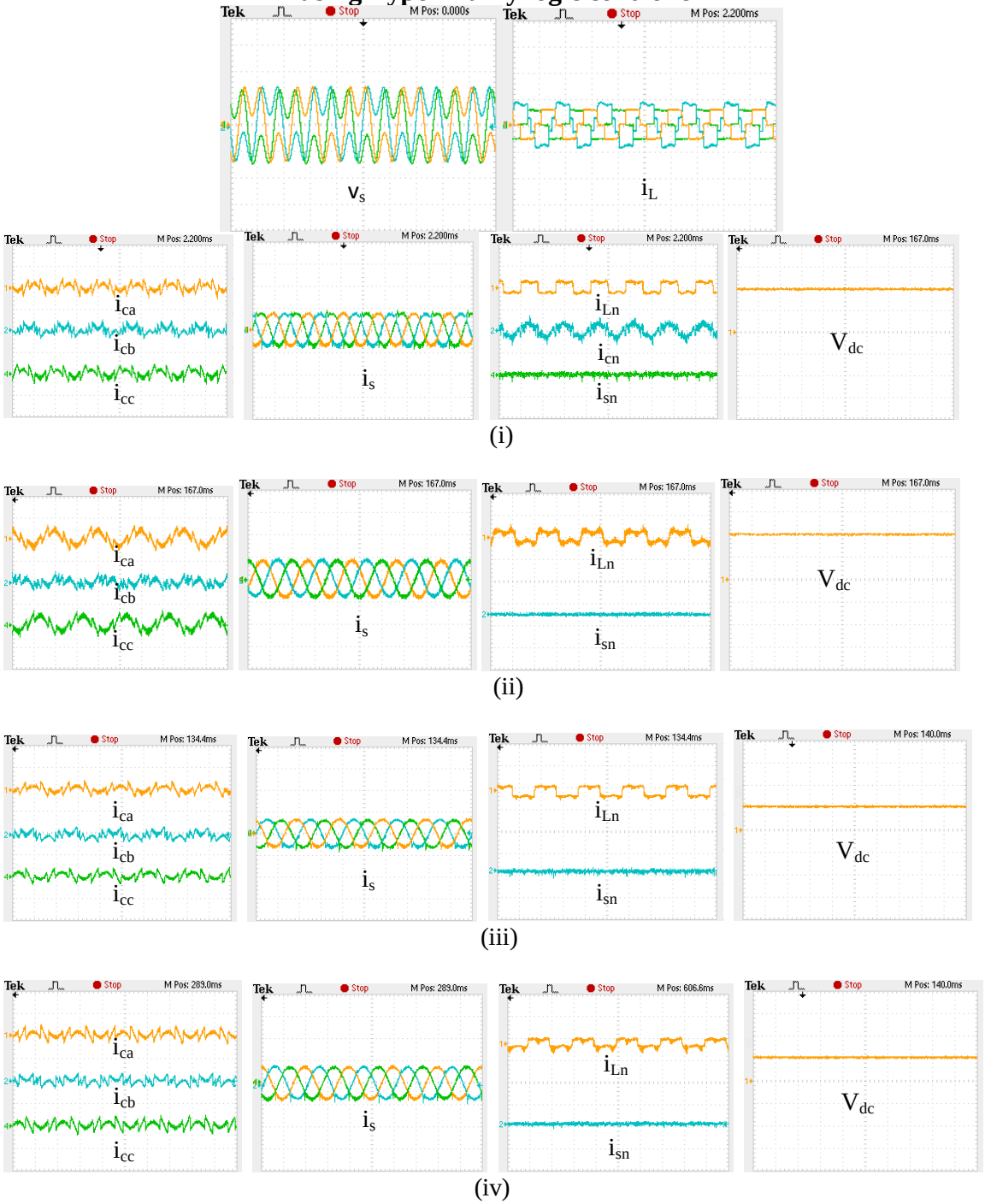


Figure 4.27: OPAL-RT results of source voltage(v_s), load current (i_L), phase filter current (i_c), source current (i_s), load neutral current (i_{Ln}), source neutral current (i_{sn}), and capacitor voltage (V_{dc}) using Type-1 fuzzy logic controller (T1FLC) under non-sinusoidal voltage source condition for (i) split capacitor interleaved buck active power filter, 2C IB APF (ii) four-leg interleaved buck active power filter, 4L IB APF (iii) single capacitor three full bridge interleaved buck active power filter, 1C 3FB IB APF and (iv) 3-phase 4-wire full bridge interleaved buck active power filter, FB IB APF

4.7.1 Results Discussion

The parameters used for the simulation circuit for the various 3-phase 4-wire IB APF by i_d-i_q control strategy using PI and Type-1 fuzzy logic controller (T1FLC) has been given in Table 4.3.

The switching frequency of IB APF has been shown in Figure 4.12a, 4.12b using adaptive hysteresis band current controller with PI, dc side controller and adaptive hysteresis band current controller with Type-1 fuzzy logic (T1FLC), dc side controller respectively. The T1FLC based adaptive hysteresis band current controller provides the best optimized switching and can be seen from the simulation results. The variation of the switching frequency variation is more in PI as compared to T1FLC.

The simulation results of 2C IB APF, 4L IB APF, 1C 3FB IB APF and FB IB APF for nonlinear unbalanced load under sinusoidal voltage source condition has been shown in Figure 4.13, 4.14 and 4.15 using PI and T1FLC based i_d-i_q control strategy. For validation, the OPAL-RT results have shown in Figure 4.16 and 4.17 for the same. Similarly, the simulation results are depicted in Figure 4.18, 4.19 and 4.20 for both PI and T1FLC controller in Figure 4.18, 4.19 and 4.20 and the same OPAL-RT results in Figure 4.21 and 4.22 of the 2C IB APF, 4L IB APF, 1C 3FB IB APF and FB IB APF under unbalanced sinusoidal and non-sinusoidal voltage source condition respectively. The THD of source current have been tabulated without and with compensation properties in the following tables of Table 4.4, 4.5, 4.6 and 4.7 for 2C IB APF, 4L IB APF, and 1C 3FB IB APF and FB IB APF topology using PI and T1FLC based i_d-i_q control strategy respectively. Figure 4.28, 4.29, 4.30, and 4.31 represents the chart diagram of the THD comparisons.

Table 4.3: Parameters value used for various 3-phase 4-wire IB APFs

3-phase 4-wire APF topologies	Coupling inductor value	dc-link capacitor value	dc-link capacitor bus voltage
2C IB APF	600 µH	(1500+1500) µF	800 V
4-Leg IB APF	600 µH	2800 µF	800 V
Transformer based 3 FB IB-APF (1C 3FB IB APF)	500 µH	3000 µF	450 V
FB IB-APF	500 µH	1000 µF for each phase inverter	450 V

Table 4.4: Source current THD before and after compensation using 2C IB APF

Supply voltage condition	Controller	Without APF (THD%)			2C-IB APF (THD%)		
		Ph-a	Ph-b	Ph-c	Ph-a	Ph-b	Ph-c
Sinusoidal supply	PI	27.71	18.25	27.77	2.57	3.65	2.94
	T1FLC	27.69	18.81	27.78	2.36	3.07	2.54
Unbalanced sinusoidal supply	PI	27.73	19.10	26.34	3.30	3.98	3.99
	T1FLC	27.75	19.02	26.60	2.15	2.65	2.23
Non-sinusoidal supply	PI	28.70	20.97	28.78	5.57	4.78	6.34
	T1FLC	28.71	20.94	28.80	3.97	4.01	4.58

Table 4.5: Source current THD before and after compensation using 4-Leg IB APF

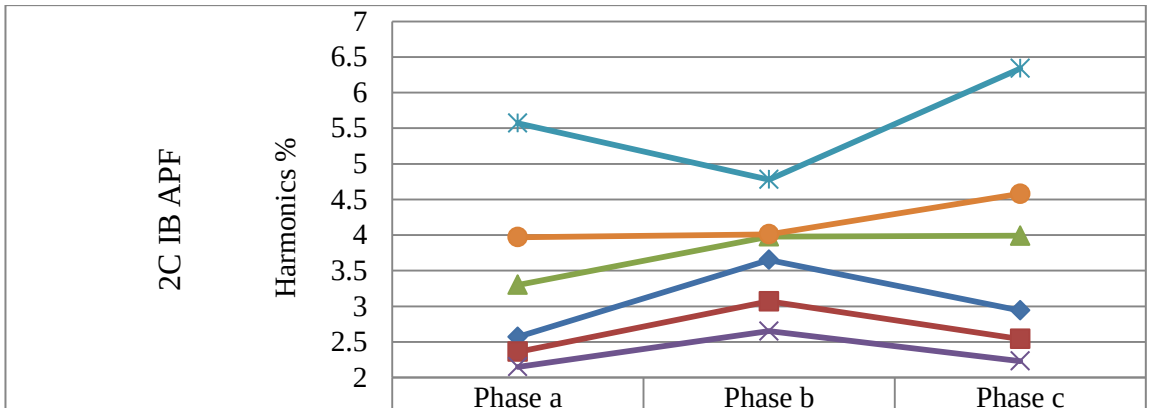
Supply voltage condition	Controller	Without APF (THD%)			4-Leg IB APF (THD%)		
		Ph-a	Ph-b	Ph-c	Ph-a	Ph-b	Ph-c
Sinusoidal supply	PI	29.72	19.83	29.64	3.81	3.84	3.94
	T1FLC	29.81	19.79	29.68	2.08	2.18	2.17
Unbalanced sinusoidal supply	PI	29.36	20.43	28.03	3.61	3.62	3.65
	T1FLC	29.42	20.38	27.99	2.11	2.08	2.12
Non-sinusoidal supply	PI	29.60	21.45	29.64	4.28	4.24	4.44
	T1FLC	29.62	21.5	28.7	3.16	3.39	3.83

Table 4.6: Source current THD before and after compensation using 1C 3FB IB APF

Supply voltage condition	Controller	Without APF (THD%)			1C 3FB IB APF (THD%)		
		Ph-a	Ph-b	Ph-c	Ph-a	Ph-b	Ph-c
Sinusoidal supply	PI	28.76	19.24	28.73	3.78	3.89	3.92
	T1FLC	28.82	19.10	28.81	2.77	2.81	3.01
Unbalanced sinusoidal supply	PI	27.56	19.16	26.28	3.49	3.34	3.50
	T1FLC	27.49	19.04	26.35	2.98	3.01	2.78
Non-sinusoidal supply	PI	28.34	20.83	28.40	4.33	5.55	4.98
	T1FLC	28.39	20.69	28.57	3.96	4.08	3.89

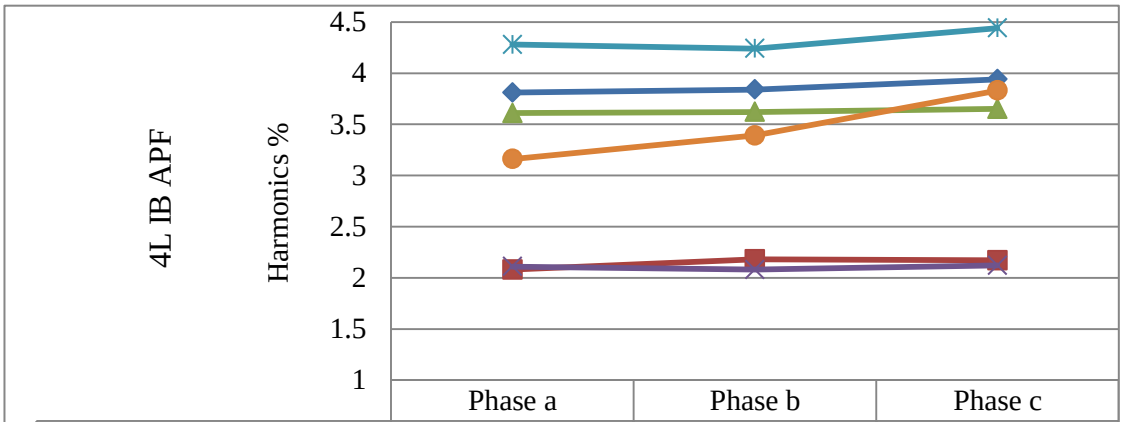
Table 4.7: Source current THD before and after compensation using FB IB APF

Supply voltage condition	Controller	Without APF (THD%)			FB IB APF (THD%)		
		Ph-a	Ph-b	Ph-c	Ph-a	Ph-b	Ph-c
Sinusoidal supply	PI	27.72	22.12	27.64	2.75	3.09	2.59
	T1FLC	27.73	22.08	27.65	2.07	2.10	2.01
Unbalanced sinusoidal supply	PI	27.40	24.22	25.97	3.37	2.73	2.78
	T1FLC	27.48	24.16	25.99	2.42	2.57	2.36
Non-sinusoidal supply	PI	27.75	22.13	28.09	4.32	5.03	4.94
	T1FLC	27.80	22.01	28.12	3.81	4.02	3.56



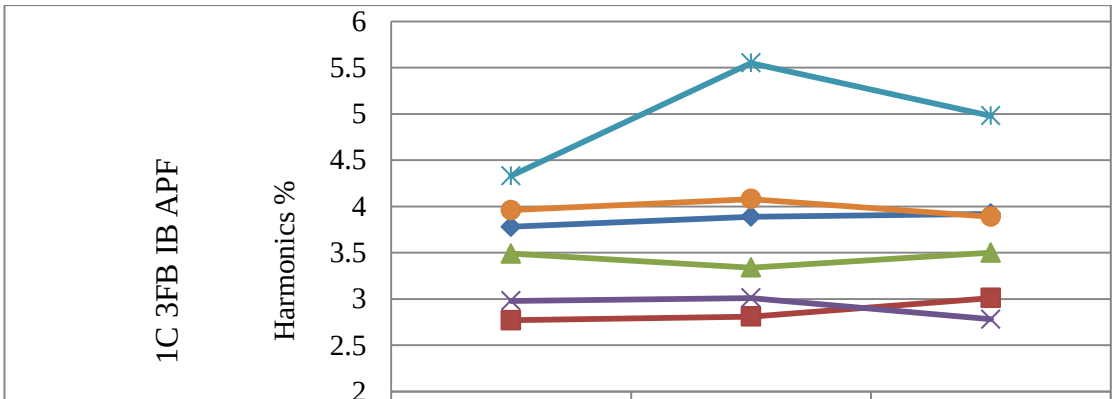
	Phase a	Phase b	Phase c
Sin PI	2.57	3.65	2.94
Sin T1FLC	2.36	3.07	2.54
Unbalanced sin PI	3.3	3.98	3.99
Unbalanced sin T1FLC	2.15	2.65	2.23
Non-sin PI	5.57	4.78	6.34
Non-sin T1FLC	3.97	4.01	4.58

Figure 4.28: Chart showing the source current THD comparison after compensation using 2C IB APF topology with PI and Type-1 fuzzy logic controller (T1FLC) for sinusoidal, unbalanced sinusoidal and non-sinusoidal voltage source condition



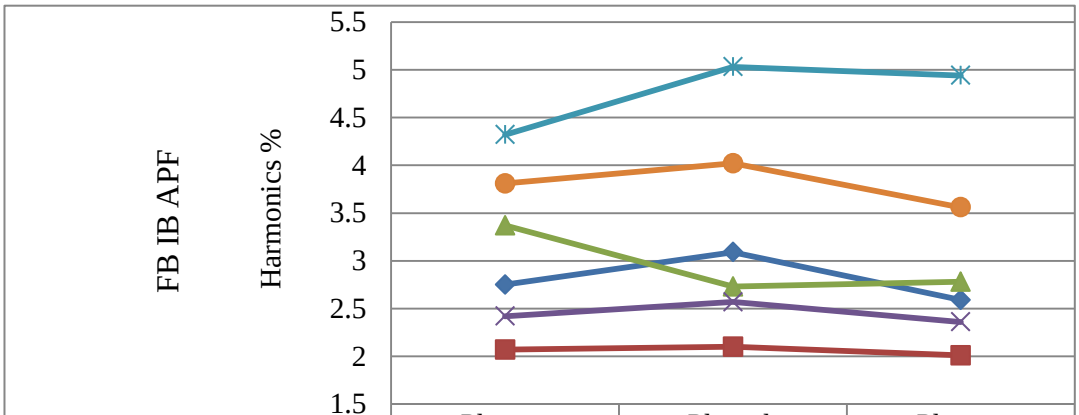
	Phase a	Phase b	Phase c
Sin PI	3.81	3.84	3.94
Sin T1FLC	2.08	2.18	2.17
Unbalanced sin PI	3.61	3.62	3.65
Unbalanced sin T1FLC	2.11	2.08	2.12
Non-sin PI	4.28	4.24	4.44
Non-sin T1FLC	3.16	3.39	3.83

Figure 4.29: Chart showing the source current THD comparison after compensation using 4L IB APF topology with PI and Type-1 fuzzy logic controller (T1FLC) for sinusoidal, unbalanced sinusoidal and non-sinusoidal voltage source condition



	Phase a	Phase b	Phase c
Sin PI	3.78	3.89	3.92
Sin T1FLC	2.77	2.81	3.01
Unbalanced sin PI	3.49	3.34	3.5
Unbalanced sin T1FLC	2.98	3.01	2.78
Non-sin PI	4.33	5.55	4.98
Non-sin T1FLC	3.96	4.08	3.89

Figure 4.30: Chart showing the source current THD comparison after compensation using 1C 3 FB IB APF topology with PI and Type-1 fuzzy logic controller (T1FLC) for sinusoidal, unbalanced sinusoidal and non-sinusoidal voltage source condition



	Phase a	Phase b	Phase c
Sin PI	2.75	3.09	2.59
Sin T1FLC	2.07	2.1	2.01
Unbalanced sin PI	3.37	2.73	2.78
Unbalanced sin T1FLC	2.42	2.57	2.36
Non-sin PI	4.32	5.03	4.94
Non-sin T1FLC	3.81	4.02	3.56

Figure 4.31: Chart showing the source current THD comparison after compensation using FB IB APF topology with PI and Type-1 fuzzy logic controller (T1FLC) for sinusoidal, unbalanced sinusoidal and non-sinusoidal voltage source condition

The steady state THD has been evaluated and it is observed that the performance is quite satisfactory in terms of %THD in the source current. The Type-1 fuzzy logic controller (T1FLC) performance is always better either ideal or non-ideal voltage source condition for all the proposed topologies. Here the non-linear load is designed with a three-phase load and a single phase load to generate unbalanced load condition. The THDs table give the THD value of the unbalanced load current for both before and after compensation. In conclusion all the proposed topologies have the ability to bring down the THDs well below the 5%, according to IEEE 519 standard recommendations. In previous chapters, the single phase load has been connected with the phase-a of the 3-phase 4-wire distribution system for making the system unbalanced. But, here the single-phase load has been connected with the phase-b in the 4-wire distribution system to have the unbalancing system.

4.8 SDP (switch device power) of IB-APFs

The SDP (switch device power) for the proposed 3-phase 4-wire FB IB-APF and 2C IB-APF topologies have been calculated and presented in the Table 4.7 and 4.8.

Table 4.8: Comparative study of 2C IB APF and FB IB-APF for various parameters

Voltage source	IB APFs	Supply voltage	V_{dc}	I_L	I_s	I_c
Sinusoidal	2C IB APF	230	800	29.52	29.02	8.321
	FB IB APF	230	450	29.96	28.79	8.17
Unbalanced sinusoidal	2C IB APF	Ph-a 230 Ph-b 180 Ph-c 230	800	27.93 25.79 27.73	27.43 27.14 27.5	7.74 8.553 7.355
	FB IB APF	Ph-a 230 Ph-b 180 Ph-c 230	450	27.6 25.69 27.8	26.92 27.02 27.72	7.606 8.228 7.083
Non-sinusoidal	2C IB APF	269.4	800	28.59	27.42	8.211
	FB IB APF	269.4	450	28.63	27.41	8.133

For minimalism, the balanced 3-phase non-linear load has been considered with R= 16 Ω and L=50 mH. Table 4.8 and 4.9 provides the information of the supply phase voltage (V_{phase}), capacitor voltage (V_{dc}), load current (I_L), source current (I_s), compensating current (I_c), switch voltage (V_{switch}), switch current (I_{switch}), diode voltage (V_{diode}), diode current

(I_{diode}), and device power (KVA) ratings in RMS values. A comparison has been made for sinusoidal, unbalanced sinusoidal and nonsinusoidal voltage source conditions. For unbalanced sinusoidal voltage source condition, the corresponding phase switches KVA rating analysis has been done separately

Table 4.9: Comparative study of SDP rating for 2C IB APF and FB IB-APF

Voltage source	IB APFs	Supply voltage	V_{switch}	I_{switch}	V_{diode}	I_{diode}	SDP, KVA	
							Switch	Diode
Sinusoidal	2C IB APF	230	562.8	6.32	554.4	6.53	3.556	3.62
	FB IB APF	230	303.9	6.37	304.7	6.19	1.935	1.866
Unbalanced sinusoidal	2C IB APF	Ph-a 230	561.5	5.633	556.1	6.212	3.162	3.454
		Ph-b 180	562.9	6.368	552.1	7.171	3.584	3.959
		Ph-c 230	561.5	6.128	556.1	5.98	3.44	3.325
	FB IB APF	Ph-a 230	303.9	5.425	304.2	6.01	1.648	1.828
		Ph-b 180	313.7	6.213	314.6	7.054	1.949	2.219
		Ph-c 230	303.7	5.59	304.5	5.55	1.697	1.689
Non-sinusoidal	2C IB APF	269.4	567.6	6.698	556.3	7.759	3.801	4.316
	FB IB APF	269.4	318.7	6.1	319.2	7.195	1.944	2.296

It is to be noted that the DC link voltage required for the proposed 3-phase 4-wire full bridge interleaved buck active power filter (FB IB-APF) topology is 450 V and for the previous 3-phase 4-wire split capacitor (2C) interleaved buck active power topology is 800 V. Therefore the ratings of the devices are drastically reduced, which can be observed from the Table 4.9 (SDP, KVA) section.

4.9 Summary

Here in this chapter an extensive simulation analysis of various 3-phase 4-wire IB APF topologies focusing on the inherent elimination of shoot-through current with a good harmonic compensation to the disturbances generated by the non-linear loads has been presented. For non-linear unbalanced load drawing a high THD current without an APF,

has been drastically brought down to less than 5% by using the proposed topologies, thereby following the IEEE-519 standard recommendations on harmonic limits. The proposed module contributes the elimination of shoot-through path, improving the reliability of the system. Although the 1C 3FB-IB APF and FB IB APF topologies use surplus switches, but can be used for greater power application, as compared to 2C-IB APF and 4-leg IB-APF which can be an eye-catching factor. Additionally, the i_d-i_q method enables a frequency independent operation as a result a large number of synchronization problems can be avoided. The fuzzy controller gives better harmonic compensation in all proposed topologies as compared to PI controller. From the Table 4.8, it can be concluded that, the maximum switch and diode KVA rating are 3.801 and 4.316 respectively, for 2C IB-APF and the maximum KVA rating of the switch and diode for the proposed 3-phase 4-wire FB IB-APF are 1.949 and 2.296 respectively. Thus, it is proved that the KVA ratings of the FB IB-APF switch and diode have been reduced by nearly $\sqrt{3}$ times.

Chapter 5

Performance Analysis of Cascaded Full-Bridge Interleaved Buck Shunt Active Power Filter

5.1 Introduction

The demand for high power applications is the motivation for extending research on cascaded full-bridge multilevel inverter based shunt active filter. The concept of multilevel inverter (MLI) is being first developed by Nabae et. al. in 1975 [43]. Out of various multilevel topologies, the cascaded full-bridge is particularly used for very high power application. Amongst the different multilevel level voltage source inverters, the most commonly used are neutral point clamped inverter, flying capacitor and cascaded H-bridge inverter [48].

The cascaded inverters are adept for a higher level of output voltage by the use of the commercially available standard lower rated voltage devices and components. Thanks to the flexible modular design of cascaded H-bridge with advantages as; transformerless connection, protracted voltage and power output with less maintenance and higher fault tolerance. As these conventional cascaded full-bridge are unite of multi cell converter and each modular converter cell consists of two active devices in one leg, hence still faces the shoot-through phenomenon with decreased reliability. Here in this chapter, the cascaded full bridge active power filter utilizing the multi carrier phase shifted PWM scheme has been modelled using full bridge interleaved buck converter with no shoot-through phenomenon.

Multilevel inverter when used in the active power filter may reduce the additional harmonics generated by it, as compared to the traditional voltage source inverters. By

increasing the number of levels of multi-level inverter, the quality of the output voltage can be improved. The more the number of levels in the output voltage and is more near to the sinusoidal. Therefore, the interleaved buck multilevel inverter and based active power has been merely discussed in this chapter.

This chapter deals with the modelling of the cascaded interleaved buck inverter on single dual-buck inverter topology to better issued the shoot-through problem. Already discussed in the previous chapters, there are no worries of shoot-through problem with this interleaved buck inverter topology and hence enhanced reliability. As no shoot-through problem in each building block cascade interleaved buck inverter, there is copious improved in the reliability as compared with other cascade inverters. Additionally, there is no necessity of dead time introduction of conventional cascade based inverters that can easily push the duty cycle theoretical limit and hence fully transfers the energy to load through the total pulse width modulation (PWM). Already discussed, the single unit interleaved buck inverter has two basic arrangements and they are half bridge interleaved buck inverter and full bridge interleaved buck inverter. The half bridge interleaved buck active power filter suffers complicacy in the dc-link voltage regulation as it consists of two dc-link capacitors. Hence cascaded full bridge interleaved buck inverter has been used for the interleaved buck active power filter for higher power application.

The various Sections of this chapter are depicted as: Section 5.2 deals with the cascaded full-bridge interleaved buck converter, Section 5.3 gives the idea about the control analysis of cascaded full-bridge interleaved buck converter, Section 5.4 describes the cascaded full-bridge IB APF with i_d-i_q control strategy, Section 5.5 and 5.6 represents the system performance of cascaded FB IB converter and based APF followed by results discussion in Section 5.7 and being summarized in Section 5.8.

5.2 Cascaded Full-Bridge Interleaved Buck converter

Figure 5.1 shows the single-phase full-bridge interleaved buck inverter [71]. The current ripple of i can be derived as follows:

$$\Delta i = \frac{(V_{dc} - v_0) D_s T_s}{L} \tag{5.1}$$

where L is the sum of L_1+L_2, and $T_s = \frac{1}{f_s}$, f_s is the switching frequency of the power devices.

Figure 5.2a shows the basic circuit diagram of the cascaded full bridge interleaved buck multilevel (9-level) inverter with capacitors acting as the dc sources. Each dc-link capacitor is connected to each single-phase full bridge interleaved buck inverter. A cascaded m-level consists of $\frac{m-1}{2}$ number of full-bridge inverters [71,1].

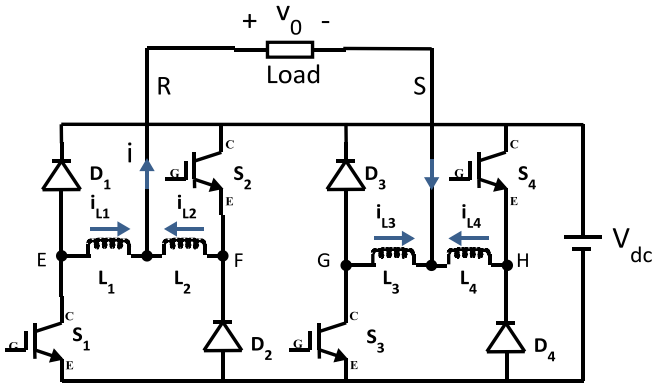
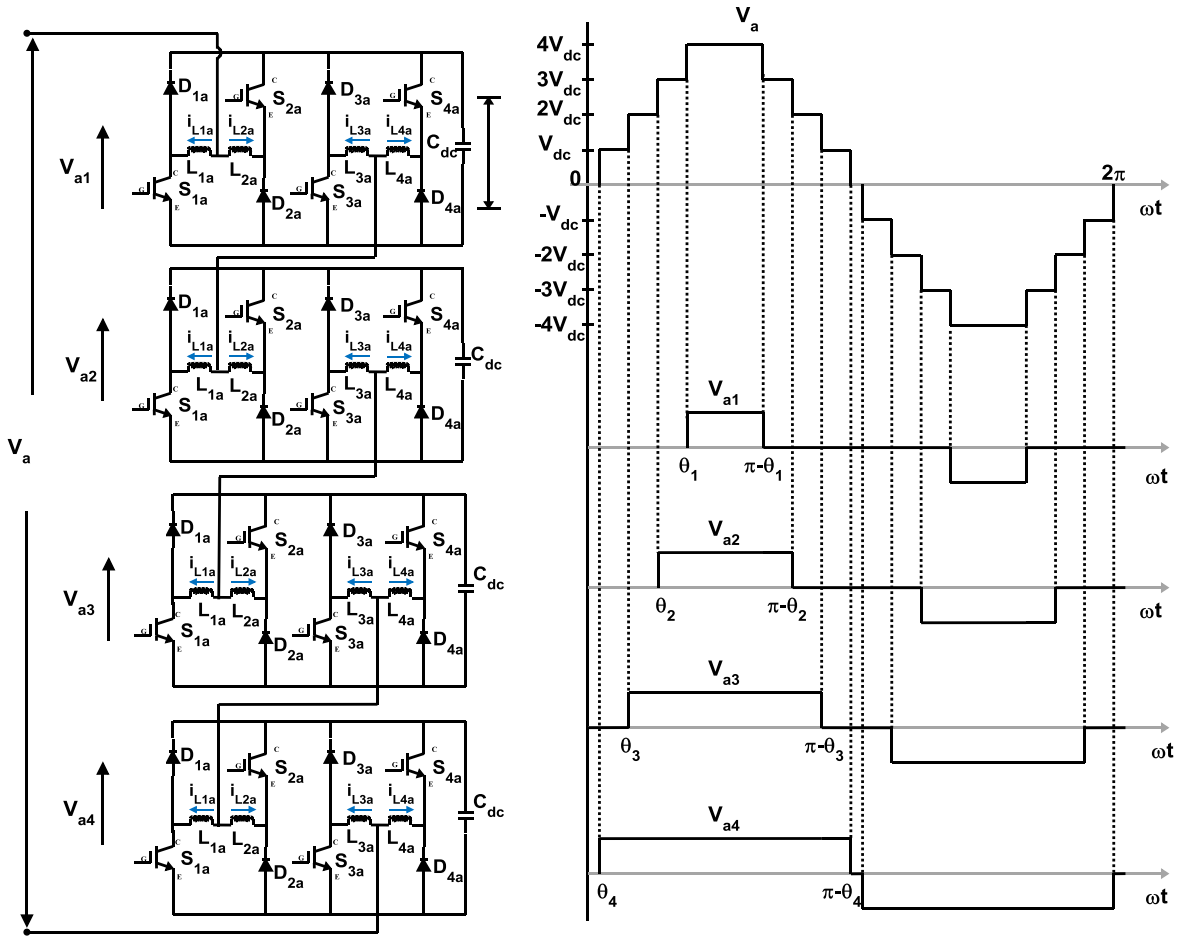


Figure 5.1: Circuit diagram of full bridge interleaved buck converter



(a) (b)

Figure 5.2: (a) Circuit diagram and (b) Output phase voltage of 9-level cascaded full-bridge interleaved buck inverter

Each H-bridge/Full-bridge produces the quasi square wave output voltage with the amplitude -$V_{dc,}$ 0 and V_{dc}. These voltages sum produce the phase voltage $V_{a,}$ since the ac terminal voltages, V_{al},V_{a2}, …$V_{a(m\text{-}1/2\text{-}1)}$, $V_{a(m\text{-}1/2)}$ are connected in series.

The phase output voltage is defined as the sum of each individual single-phase full bridge interleaved buck inverter voltage [51] and is:

$$V_a = V_{a1} + V_{a2} + \cdots + V_{a(m-1/2-1)} + V_{a(m-1/2)} \quad (5.2)$$

The phase voltage waveforms for a single-phase 9-level multilevel cascaded full bridge interleaved buck inverter are depicted in Figure 5.2b.

5.3 Control Analysis of Cascaded Full-Bridge Interleaved Buck converter

The cascaded multilevel full bridge interleaved buck inverter can be worked with both fundamental and high switching frequencies, hence can be broadly divided into two types based on the switching frequency [55-58]. Figure 5.3 shows the switching schemes classification for the multilevel cascaded inverter.

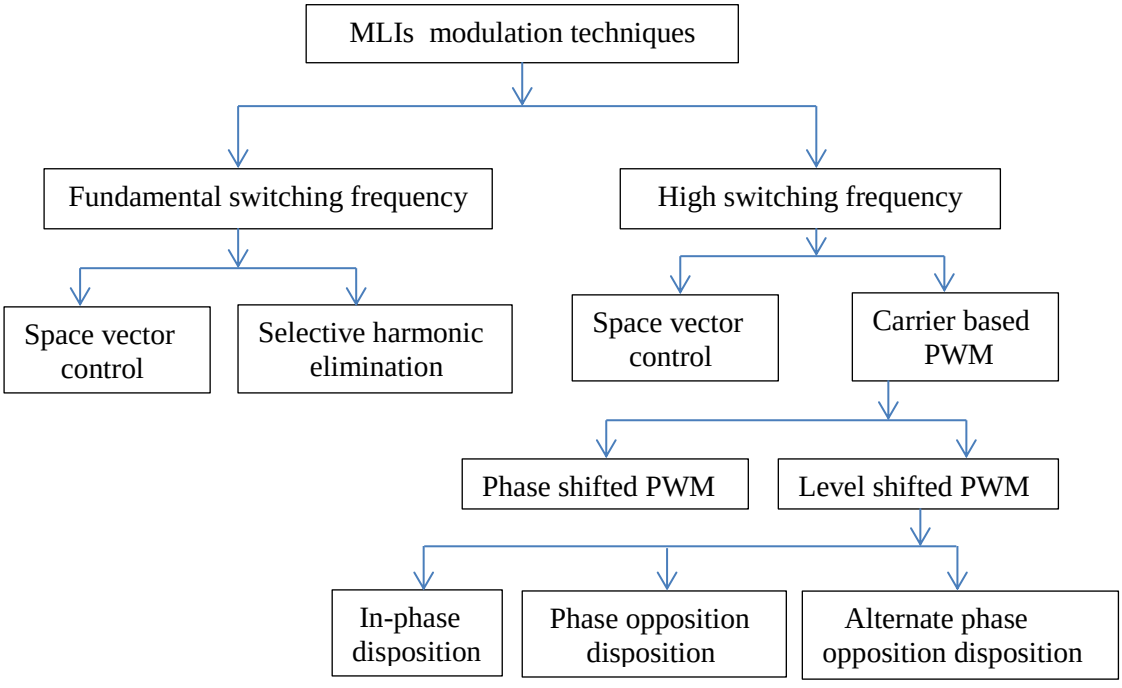


Figure 5.3: Classification of multilevel inverter (MLI) modulation techniques

Fundamental switching schemes implicate one or two commutations by the switching devices per cycle of the fundamental output voltage. However, the high frequency

switching schemes may involve numerous commutations within a cycle of the output voltage. The fundamental switching schemes comprised of space vector control and selective harmonic elimination (SHE). However, the carrier based pulse width modulation scheme prevails under the high switching frequency type of modulation.

5.3.1 Space Vector Modulation (SVM)

Space vector modulation (SVM) is very commonly used in two-level voltage source inverter. The SVM for multi-level inverter is the extended version of the two-level inverter SVM. It follows the α-β transformation of voltage signal and is represented in the form of space vectors, maintaining the impedances and total power becomes unchanged.

As per the switching positions of two level voltage source inverter, there are eight states of switching and six sectors. The state matrix becomes very much complex as the number of the output voltage level goes on increasing for multilevel cascaded inverter. This finds the high computational burden during the switching pulses generation process. Therefore, this SVM finds its application only for some lower level multilevel inverter.

5.3.2 Selective Harmonic Elimination (SHE)

Think through a MLI having 's' number of full bridge interleaved buck inverter and $s = (m-1)/2$, where m represents the number of levels in the output voltage. The Fourier series expansion of this stepped output voltage can be represented as follows:

$$V(\omega t) = \frac{4V_{dc}}{\pi}\sum_{n}[cos(n\theta_1) + cos(n\theta_2) + \cdots + cos(ns)] \times \frac{\sin(n\omega t)}{n} \tag{5.3}$$

where n = 1,3,5,7… represents for the 1st, 3rd, 5th, 7th … , odd order harmonics. $\theta_1, \theta_2, \ldots, \theta_s$ represents the switching angles of 's' individual full bridge inverter of the multilevel cascaded topology as depicted in Figure 4.1b.with the condition that $0 < \theta_1 < \theta_2 < \theta_s < \frac{\pi}{2}$.

The Fourier series coefficients when being normalized with V_{dc} are being given by:

$$H(n) = \frac{4}{n\pi}[cos(n\theta_1) + cos(n\theta_2) + \cdots + cos(ns)] \tag{5.4}$$

Here the angles $\theta_1, \theta_2, \ldots, \theta_s$ are set for such values that the THD can be decreased of the synthesized output values and the condition is that, the output voltage should be:

$$V(\omega t) = V_1 \sin(\omega t) \tag{5.5}$$

where, V_1 is the desired fundamental voltage. The switching angles are selected in the way that, the dominated lower order harmonics are to be eliminated. The number of lower order harmonics that can be eliminated by the selective harmonic elimination pulse width modulation (SHE PWM) scheme is $(s-1)$ with $'s'$ number of separate DC sources in multilevel cascaded inverter. Consider 11-level multilevel cascaded inverter having $s = 5$, then $(s-1) = 4$ numbers of dominant harmonic orders can be eliminated. For eliminating the 5th, 7th, 11th and 13th order of harmonics the reduced following equations considering the mathematical conditions of 4.2 are as given as:

$$\begin{gathered}
\frac{4V_{dc}}{\pi}[\cos\theta_1 + \cos\theta_1 + \cos\theta_1 + \cos\theta_1] = V_1 \\
[\cos 5\theta_1 + \cos 5\theta_1 + \cos 5\theta_1 + \cos 5\theta_1] = 0 \\
[\cos 7\theta_1 + \cos 7\theta_1 + \cos 7\theta_1 + \cos 7\theta_1] = 0 \\
[\cos 11\theta_1 + \cos 11\theta_1 + \cos 11\theta_1 + \cos 11\theta_1] = 0 \\
[\cos 13\theta_1 + \cos 13\theta_1 + \cos 13\theta_1 + \cos 13\theta_1] = 0
\end{gathered} \tag{5.6}$$

After eliminating the dominant lower order harmonics by the help of switching scheme, the higher order harmonics can easily be filtered out from the output voltage of the multilevel inverter. Hence the output voltage using this SHE-PWM gives better output voltage as compared to other PWM schemes, but suffers with the drawbacks of large computation and requirement large memory unit.

5.3.3 Multicarrier based Pulse Width Modulation

The multicarrier based pulse width modulation scheme can be essentially divided into two types and are phase shifted and level shifted PWM [50-52].

5.3.3.1 Phase shifted PWM scheme

The phase shifted pulse width modulation scheme necessitates $(m-1)$ number of carrier signal for the generation of m level output voltage. The carrier signal are triangular in nature devouring of the same amplitude and frequency, but being shifted by an angle φ_{cr}, is given as:

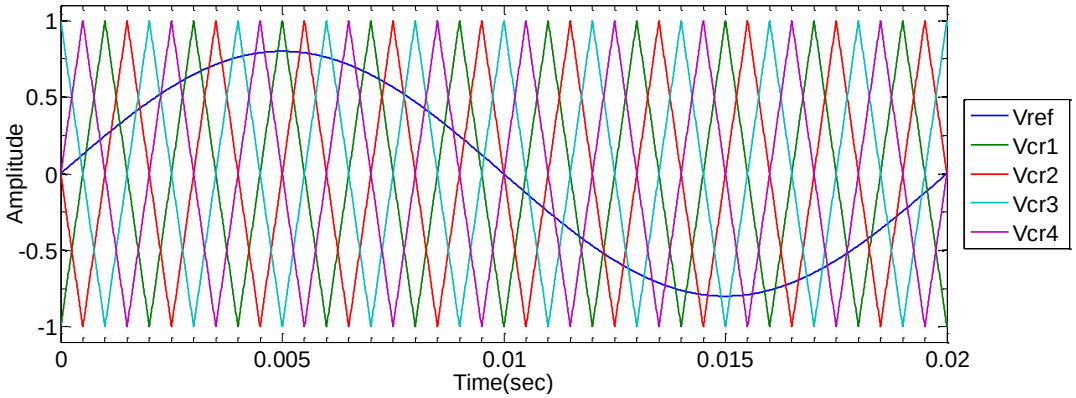


Figure 5.4: Phase shifted PWM scheme for 5-level multilevel cascaded inverter

$$\varphi_{cr} = \frac{360^{\circ}}{m-1} \tag{5.7}$$

The modulating signal is sinusoidal in nature. The above Figure 5.4 depicts the phase shifted PWM scheme for 5 level multilevel cascaded inverter. The carrier signal signals and reference/modulating signal are represented by $V_{cr1}, V_{cr2}, V_{cr3}, V_{cr4}$ and V_{ref} in the above figure respectively.

5.3.3.2 Level Shifted PWM scheme

For level shifted pulse width modulation scheme also requires the same number of carrier signal as phase shifted i.e. $(m-1)$. The frequency and amplitude are also same for all the carrier signals, but are vertically disposed with respect to each other so that the adjacent band can be occupied by them to become level shifted waveform. The level shifted modulation can be classified according to the nature of the carrier signal and are given as:

i. In-phase disposition PWM scheme (IPD PWM): In this scheme all the carrier signals are disposed in the same phase
ii. Phase opposition disposition PWM scheme (POD PWM): In this scheme, the carrier signals are arranged in the same phase above the zero reference but opposition to the carrier signal below the zero reference signal.
iii. Alternate opposition disposition PWM scheme (APOD PWM): Here in this method the carrier signals are oppositely disposed alternately.

Figure 5.5a, 5.5b and 5.5c shows the IPD, POD and APOD pulse width modulation scheme for 5-level cascaded inverter respectively for one cycle of frequency supply i.e. 50 Hz. The signals $V_{cr1}, V_{cr2}, V_{cr3}, V_{cr4}$ represents the carrier signal waveform and V_{ref} represents for reference/modulating signal.

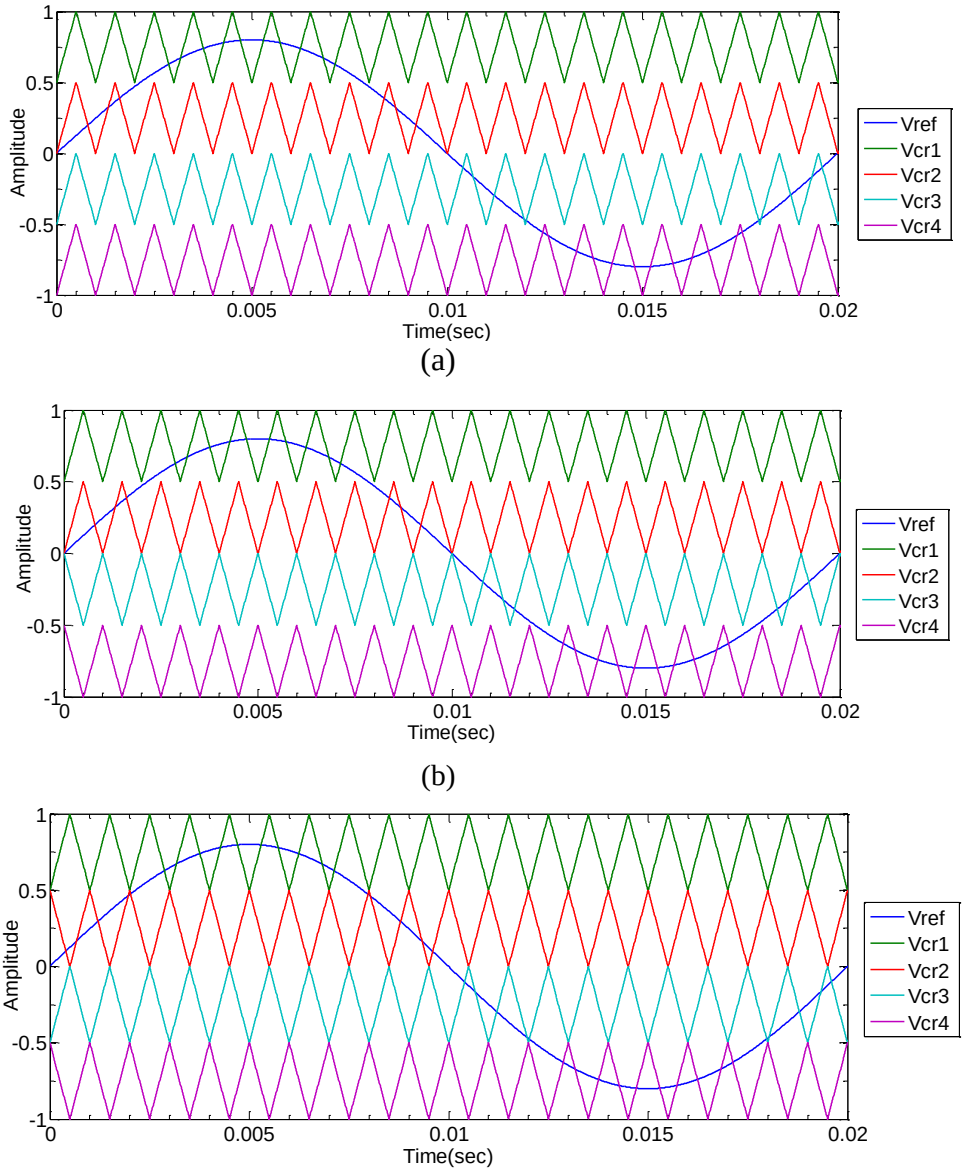


Figure 5.5: (a) In-phase disposition PWM (IPD PWM) (b) Phase opposition disposition PWM (POD PWM) (c) Alternate phase opposition disposition PWM (APOD PWM) scheme for 5-level multilevel cascaded inverter

Again, a general comparison has been made between the phase shifted and level shifted PWM by taking the following features:

i. Modulation indices

The frequency modulation index can be given by

$$m_f = \frac{f_c}{f_m} \tag{5.8}$$

where f_c and f_m represents the carrier and reference/modulating signal frequency respectively. This frequency modulation index formula is same for both the phase shifted and level shifted PWM scheme.

Further, the amplitude modulation index m_a for phase shifted is defined as:

$$m_a = \frac{A_m}{A_c} \tag{5.9}$$

which is not same for the level shifted PWM and is defined by,

$$m_a = \frac{A_m}{A_c(m-1)} \tag{5.10}$$

where A_m and A_c represents the peak amplitude of modulating and each carrier signal respectively. The amplitude modulation index values exist in the range of 0 to1 for both phase shifted and level shifted PWM.

ii. Device and inverter switching frequencies

The device switching frequency (f_{device}) of MLI by the use of phase shifted PWM scheme is same as the frequency of the carrier signal (f_c), given as:

$$f_{device} = f_c \tag{5.11}$$

Whereas, the inverter switching frequency by phase shifted PWM is

$$f_{inverter} = (m-1)f_{device} \tag{5.12}$$

On the contrary, the inverter switching frequency of a level shifted carrier type MLI is same as carrier frequency:

$$f_{inverter} = f_c \tag{5.13}$$

And the device switching frequency with level shifted PWM scheme is given as:

$$f_{device} = \frac{f_{inverter}}{(m-1)} \tag{5.14}$$

iii. Device conduction period

The device conduction time for each device is same for phase shifted PWM scheme, whereas conduction time becomes different for in case of level shifted PWM scheme.

iv. Necessity of carrier rotation

There is an uneven distribution of power in each full bridge inverter cell of multilevel cascaded inverter topology in level shifted PWM scheme, resulting high harmonic input current. This disadvantage can be eliminated by the rotation carrier scheme and hence uniform power distribution among each full-bridge inverter cells used by the MLI. Further, the phase shifted MLI does not suffer from the uneven power distribution problem.However, the level shifted PWM scheme always give better results as compared to phase shifted PWM, which has been proven and can be seen in the later section of this chapter.

5.4 Cascaded Full-Bridge Interleaved Buck Converter based Active Power Filter with i_d-i_q control strategy

Figure 5.6 shows the 3-phase multilevel cascaded full bridge interleaved buck active power filter [54,72]. In this chapter, only 3-phase 5-level cascaded full bridge interleaved buck active power filter has been focused. In 5-level cascaded full bridge interleaved buck active power filter, only two units of full bridge inverter needs to be used. The Non-linear load has been taken and drawing the i_{La}, i_{Lb} and i_{Lc} respectively phase load current.

The source current i_{sa}, i_{sb} and i_{sc} from the utility can be exactly same as the load current without active power filter and can be related as:

$$\begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} = \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{5.15}$$

The compensating current injected by the active power filter is precisely the same magnitude but 180° out of phase to the harmonic content of the load current. This injected compensating current makes the source current purely sinusoidal and the relation between the source current i_{sa}, i_{sb}, i_{sc}, load current i_{La}, i_{Lb}, i_{Lc} with compensating current i_{ca}, i_{cb} i_{cc} can be depicted as:

$$\begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} = \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} + \begin{bmatrix} i_{ca} \\ i_{cb} \\ i_{cc} \end{bmatrix} \tag{5.16}$$

The cascaded inverter output voltage contains less switching frequency ripple as equated to two-level inverter and hence lower value coupling inductor can be used [53]. Again, in the cascaded inverter structure more number of dc sources are required as compared to 2-level inverter. The dc-link voltage required by the cascaded inverter can be defined as:

$$C_{dc} = \frac{\Delta Q}{\Delta V_{dc}}$$

$$\text{And } \Delta Q = \int_{\pi-\theta_i}^{\theta_i} \sqrt{2} I \cos\theta \, d\theta = 0 \tag{5.17}$$

where, $i = 1,2,\ldots,(m-1)/2$; $[\theta_i, \pi - \theta_i]$ denotes the time interval during which dc capacitor connects to the ac side, and I represents the rms value of line current. An added advantage of cascaded inverter is that it boosts the voltage and hence low dc-link capacitor voltage required.

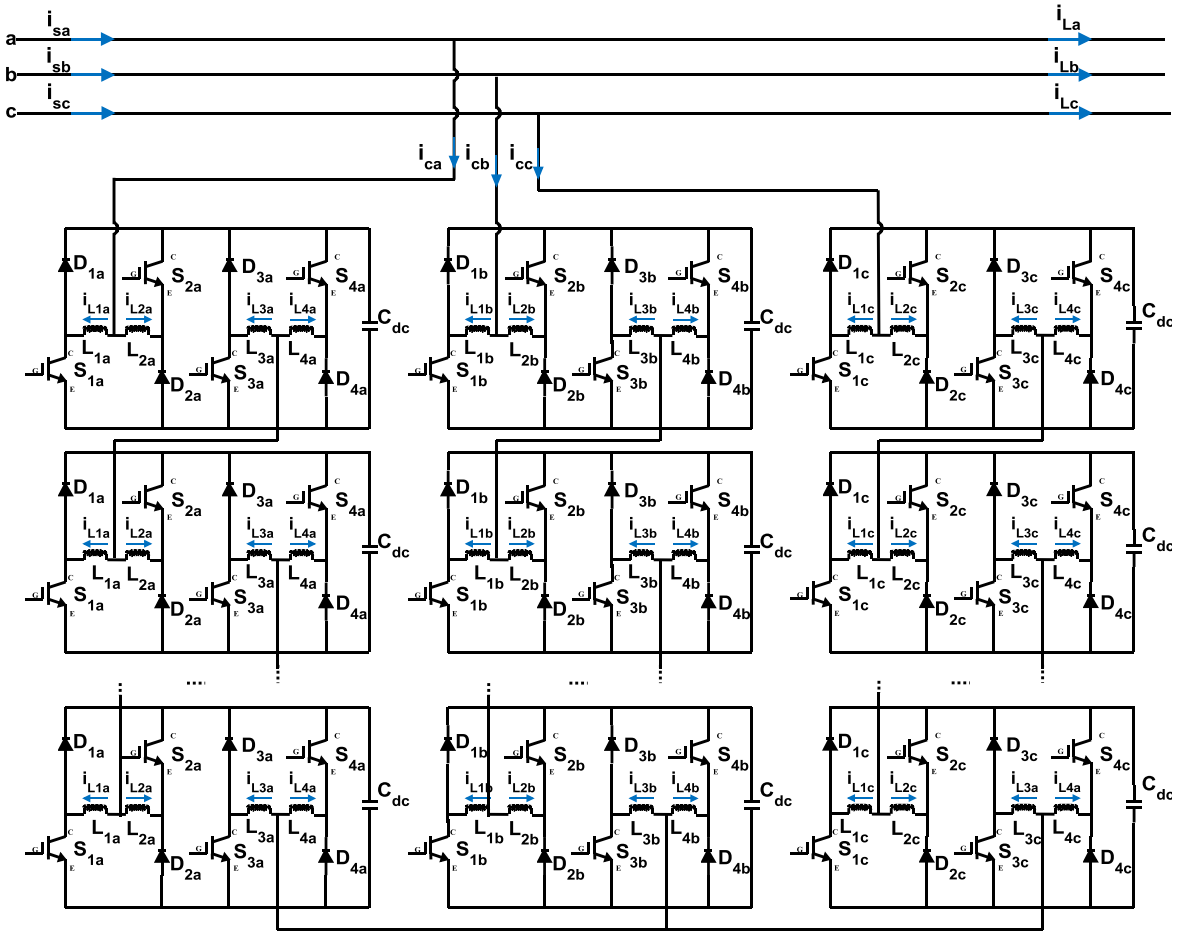


Figure 5.6: Multilevel 3-phase *m*–level cascaded full bridge interleaved buck active power filter

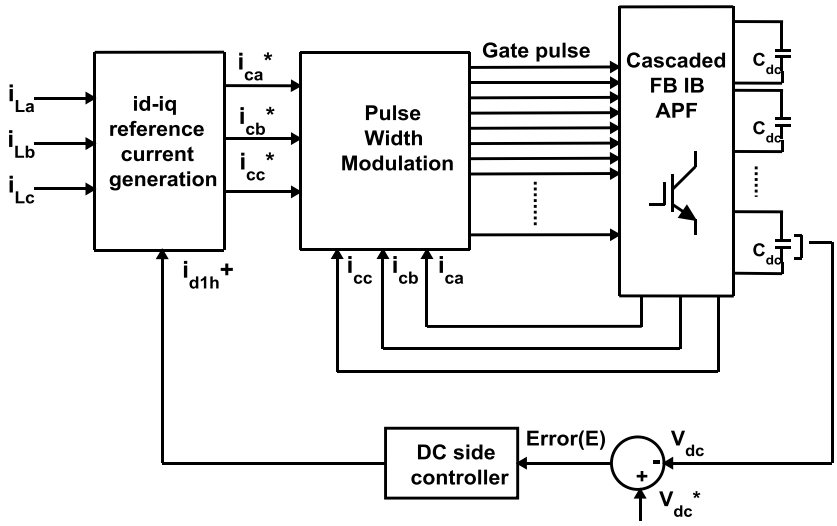
For the 5-level cascaded full-bridge interleaved buck converter based active power filter the T1FLC based i_d-i_q control strategy has been used for the evaluation of reference compensating current as shown in Figure 5.7a.

In order to regulate the dc-link voltages of all the dc-link capacitors used in the cascaded interleaved buck full-bridge inverter only one dc-link capacitor voltage needs to be tracked required by the i_d-i_q control scheme for reference current generation [53]. Hence, the dc-link voltage regulation system becomes very simple and reliable.

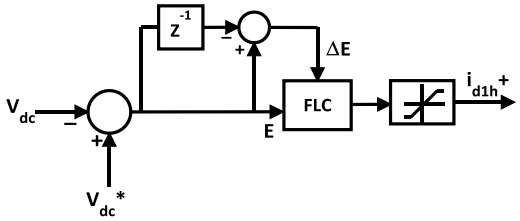
The dc-link voltage regulator system using the Type-1 fuzzy logic controller has been depicted in Figure 5.7b. The error (E) and change in error (ΔE) calculated from the dc-link voltage (V_{dc}) and (V_{dc}^*) becomes the input of the Type-1 fuzzy logic controller.

$$E = V_{dc} - V_{dc}^* \tag{5.18}$$

$$\Delta E = \Delta(V_{dc} - V_{dc}^*) \tag{5.19}$$



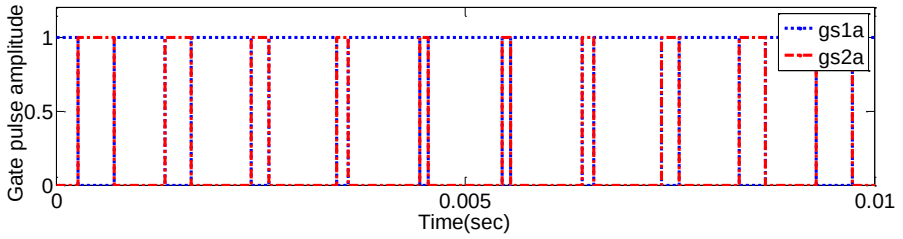
(a)



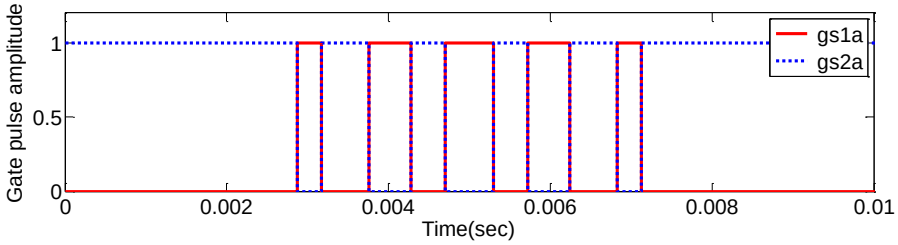
(b)

Figure 5.7: (a) Block diagram of reference current generation using i_d-i_q control scheme for m-level interleaved buck active power filter (b) dc- link voltage controller using Type-1 fuzzy logic controller (T1FLC)

5.5 System Performance of Cascaded Full-Bridge Interleaved Buck Converter



(a)



(b)

Figure 5.8: Switching pulse for the same leg power devices by (a) phase shifted PWM (b) level shifted PWM

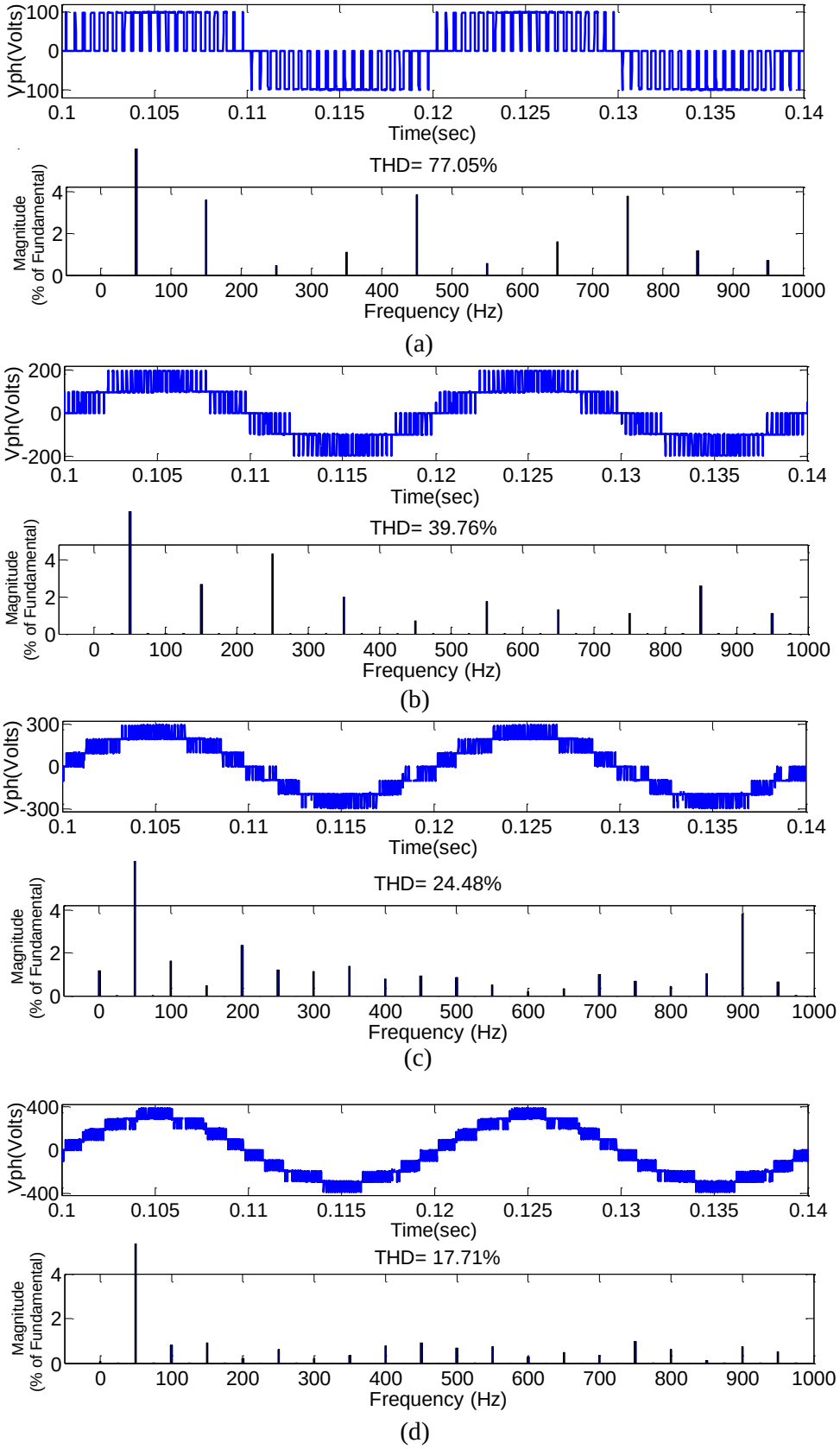


Figure 5.9: Phase voltage and THDs for (a) Level-3 (b) Level-5 (c) Level-7 (d) Level-9 cascaded full-bridge IB inverter using Phase shifted PWM scheme

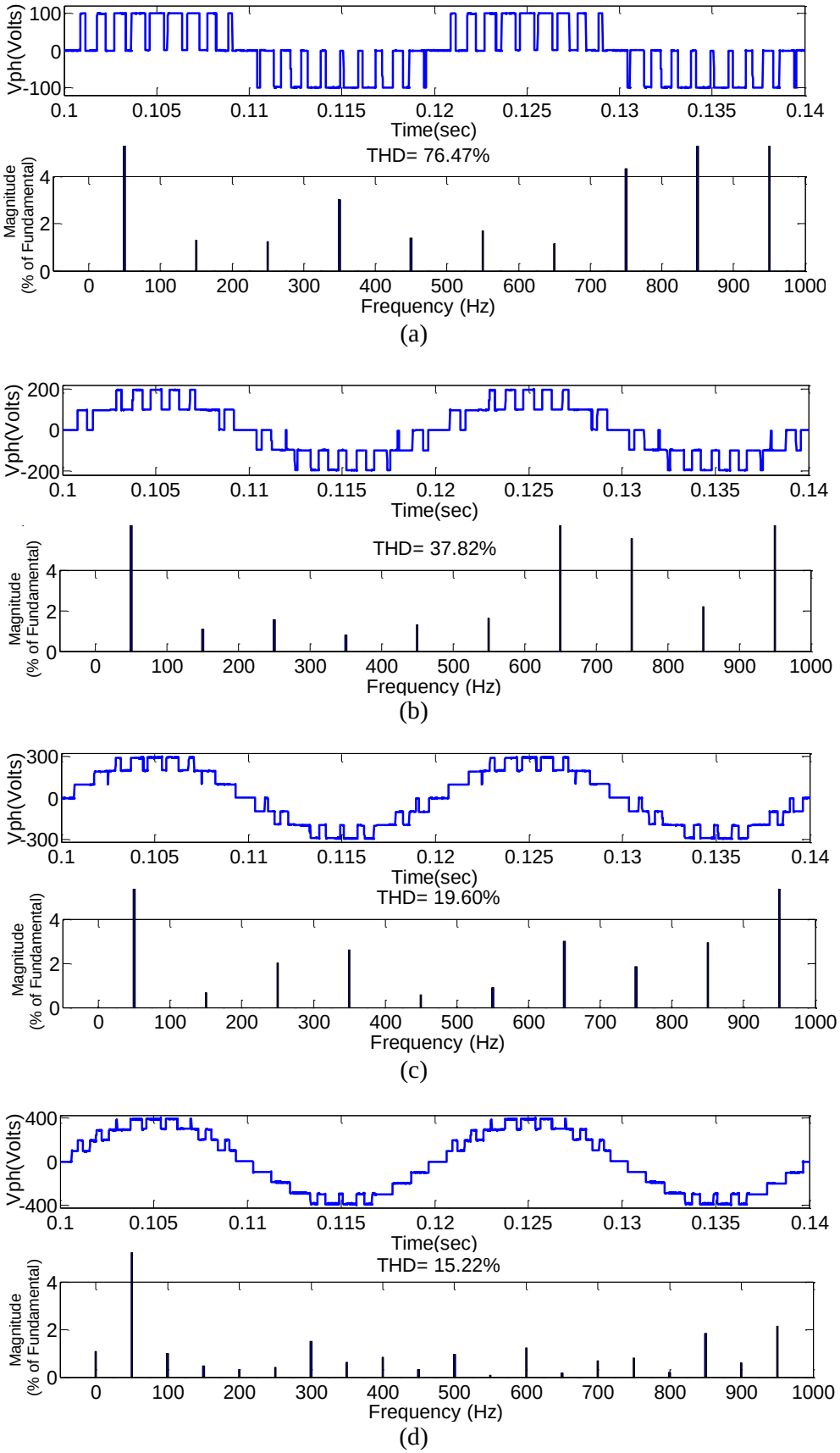
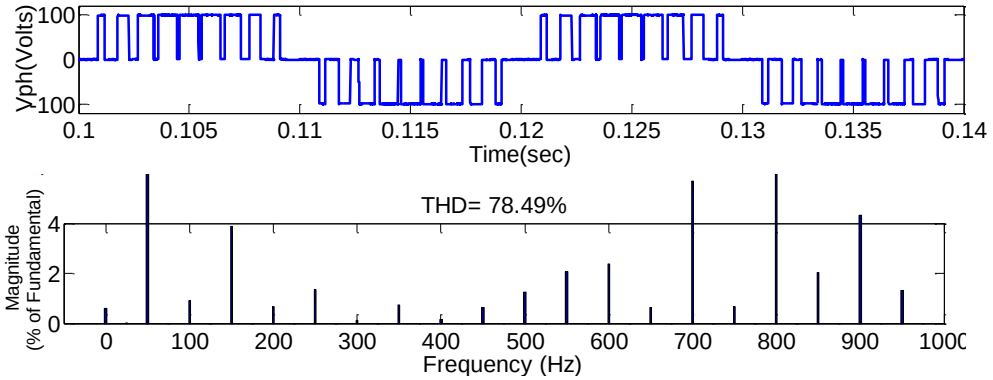
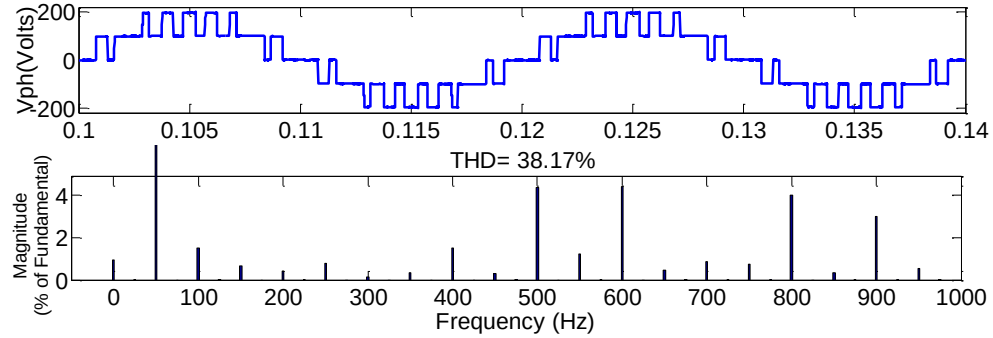


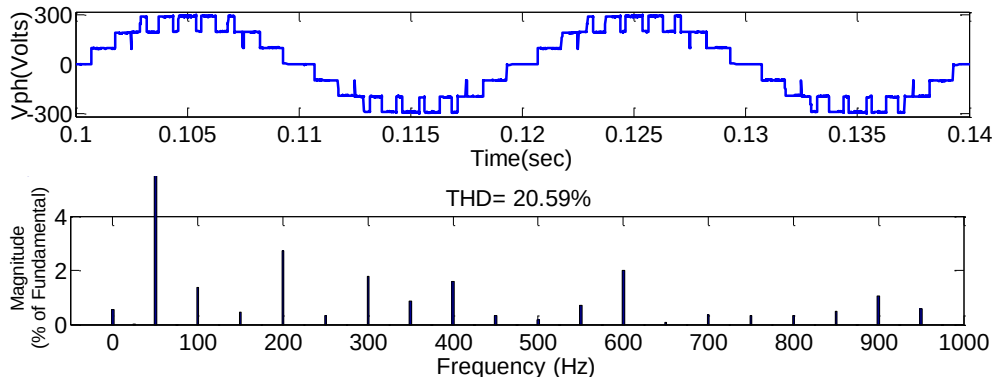
Figure 5.10: Phase voltage and THDs for (a) Level-3 (b) Level-5 (c) Level-7 (d) Level-9 cascaded full-bridge IB inverter using In phase Disposition (IPD) PWM scheme



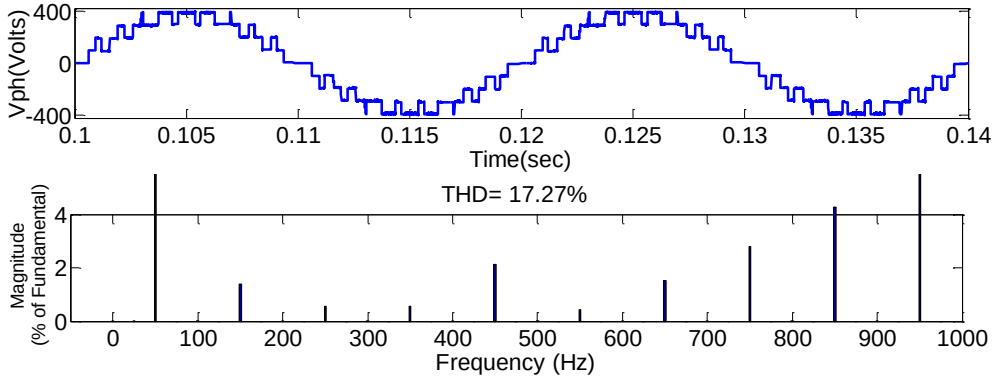
(a)



(b)



(c)



(d)

Figure 5.11: Phase voltage and THDs for (a) Level-3 (b) Level-5 (c) Level-7 (d) Level-9 cascaded full-bridge IB inverter using Phase Opposition Disposition (POD) PWM scheme

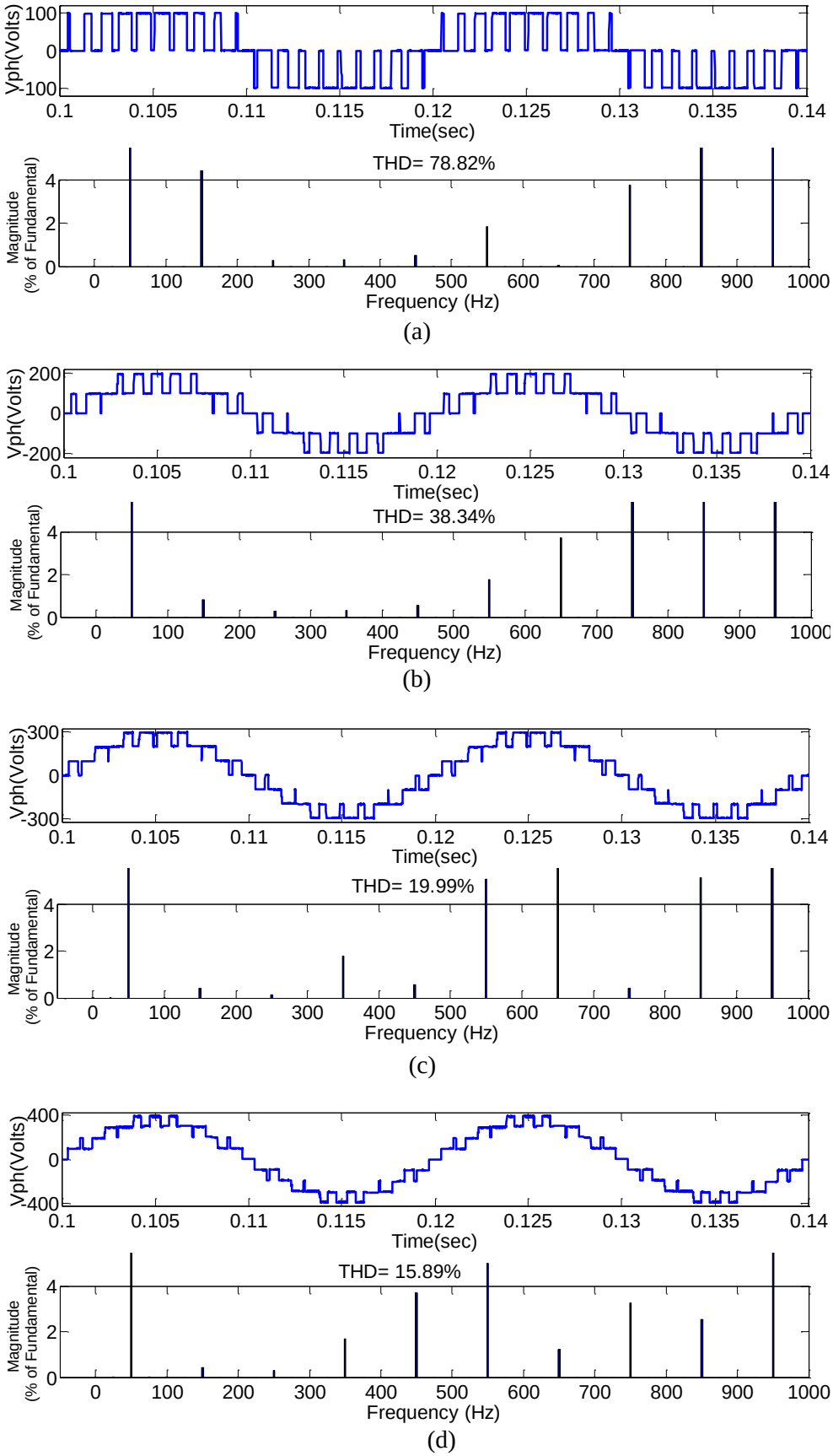


Figure 5.12: Phase voltage and THDs for (a) Level-3 (b) Level-5 (c) Level-7 (d) Level-9 cascaded full-bridge IB inverter using Alternate Phase Opposition Disposition (APOD) PWM scheme

5.6 System Performance of Cascaded Full-Bridge Interleaved Buck converter based Active Power Filter

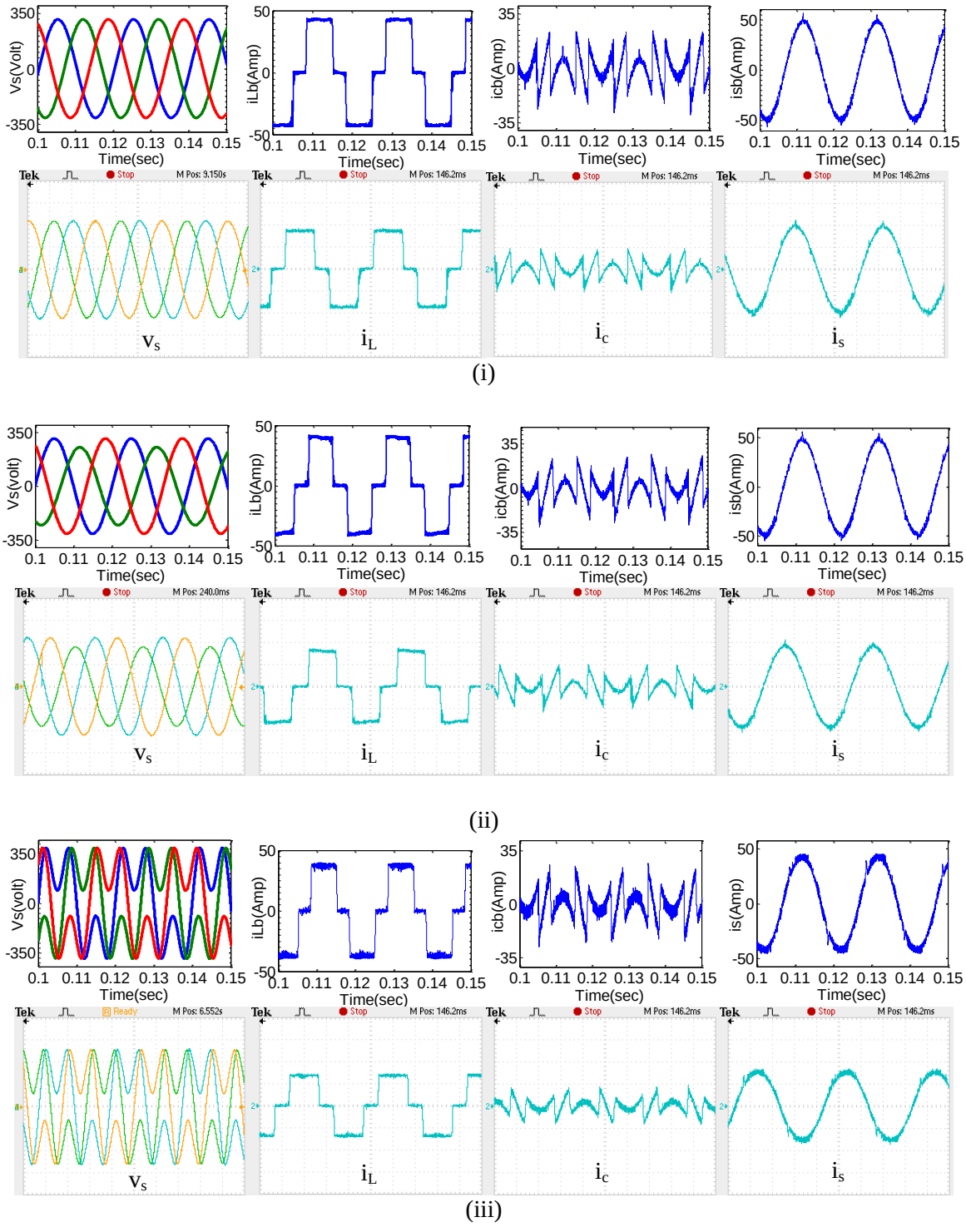


Figure 5.13: Simulation and OPAL-RT results of source voltage (v_s), load current (i_L), compensating current (i_c) and source current (i_s) for 5-level 3-phase cascaded full-bridge interleaved buck active power filter under (i) sinusoidal (ii) unbalanced sinusoidal (iii) non-sinusoidal voltage source condition

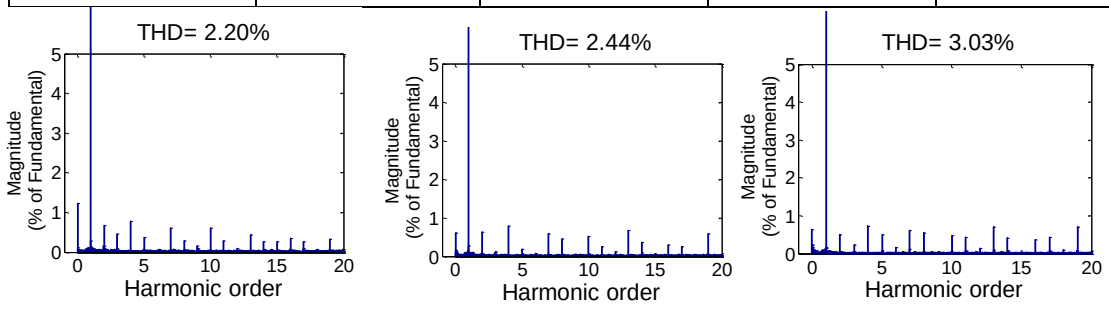
5.7 Results Discussion

Figure 5.8a and 5.8b shows the switching gate pulse for the power switches on the same leg, with the application of phase shifted and level shifted PWM scheme. It can be seen that from Figure 5.8, at the same time one power switch is getting turned on and another is getting turned off rising the shoot-through phenomenon in conventional cascaded inverter.

Figure 5.9 shows the simulation results of phase voltage and THDs for Level-3, Level-5, Level-7 and Level-9 cascaded full-bridge IB converter using Phase shifted PWM scheme. Similarly, 5.10, 5.11 and 5.12 represents the Level-3, Level-5, Level-7 and Level-9 for IPD, POD and POD PWM scheme respectively. However, from the Table 5.1 it can be proved that the level shifted PWM scheme provides better output phase voltage than phase shifted. Again, IPD level shifted PWM scheme provides the best THDs as compared to others. Hence, here IPD PWM scheme has been utilized for the cascaded full-bridge interleaved buck active power filter.

Table 5.1: THD of the phase voltage of the Level-3, Level-5, Level-7 and Level-9 cascaded interleaved buck full-bridge inverter

Cascaded MLI	Phase-shifted PWM	Level-shifted PWM		
		IPD	POD	APOD
Level - 3	77.05%	76.47%	78.49%	78.82%
Level - 5	39.76%	37.82%	38.17%	38.34%
Level - 7	24.48%	19.60%	20.59%	19.99%
Level - 9	17.71%	15.22%	17.27%	15.89%



(a) (b) (c)

Figure 5.14: THDs of the source current after compensation using cascaded 5-level FB IB converter based APF for (a) sinusoidal (b) unbalanced sinusoidal and (c) non-sinusoidal voltage source condition

An analysis has been done on the cascaded full bridge interleaved buck active power filter. Extensive simulation results have been shown for 5-level cascaded full-bridge interleaved buck active power filter. Figure 5.13 shows the simulation and OPAL-RT results for the performance analysis of the cascaded 5-level full-bridge interleaved buck active power filter for sinusoidal, unbalanced sinusoidal and non-sinusoidal voltage source condition respectively. The THD of the source current is 28.01% before compensation and had been decreased to 2.20, 2.44, 3.03 for balanced, unbalanced and non-sinusoidal voltage source condition respectively after compensation as shown in Figure 5.14.

5.8 Summary

Here, in this chapter, the cascaded interleaved buck active power filter has been considered with its various advantages for distribution network with no shoot-through phenomenon. Besides, a major purpose the MLI serves is reduction of stresses across the semiconductor switching devices. A comparison between APFs employing cascaded 5-level interleaved buck full bridge active power filters are realized under ideal, distorted and unbalanced supply voltage conditions. The reference compensation filter currents for three-phases are extracted using $i_d - i_q$ scheme and multilevel carrier based IPD-PWM is carried out to generate switching signals for MLI. The THDs has been decreased to below 5 % as per the IEEE 519 limits with shoot-through elimination.

Chapter 6

Major Contributions, General Conclusions and Scope for Future Research

6.1 Major Contributions

1) Elimination of shoot-through current in the modeled IB APF topology.
2) Performance analysis of 2C IB APF using p-q and i_d-i_q control strategy.
3) Comparison of source current compensation capabilities of p-q control strategy and i_d-i_q control strategy for 3-phase 4-wire 2C IB APF under sinusoidal, unbalanced sinusoidal and non-sinusoidal voltage source condition.
4) Comparison of switching frequency and source current THD of conventional hysteresis band current controller and adaptive hysteresis current band controller for 3-phase 4-wire 2C IB APF using i_d-i_q control strategy.
5) Performance analysis of 2C IB APF using Type-1 and Type-2 fuzzy logic controller for different fuzzy membership functions (MFs) viz. Triangular, Trapezoidal and Gaussian MF.
6) Performance analysis of various topologies of 3-phase 4-wire IB APFS for distribution system and they are
   i. 2C IB APF topology
   ii. 4L IB APF topology
   iii. Single capacitor 3 full bridge IB APF, 1C 3 FB IB APF
   iv. 3-phase 4-wire FB IB APF with three discrete FB cell, FB IB APF

7) Comparison of switch device power rating of the 2C IB APF and FB IB APF
8) Performance analysis of cascaded full-bridge interleaved buck converter and based active powe filter.

6.2 General Conclusions

The following are the important findings of the research work:

1) Shoot-through current gets eliminated hence the reliability of the modeled IB APFs topology improved. p-q control strategy does not provide good harmonic compensation of the source current in case of unbalanced and non sinusoidal voltage source condition.
2) The i_d-i_q control strategy is better as compared to p-q control strategy under a wide variety of voltage source condition. Load compensation has been dropped down satisfactorily to below 5 % satisfying the IEE519 standards of harmonic compensation. Additionally, it compensates the neutral current during unbalanced load condition.
3) The adaptive hysteresis provides the optimum switching frequency of the power switches resulting in the reduced switching losses. The source current compensation is also better here.
4) The Type-2 fuzzy logic controller provides best dc-Link voltage regulation during load changing condition and also a good source harmonic compensation as compared to PI and Type-1 fuzzy logic controller.
5) The simulation results show best source current THD by using Gaussian membership function in both Type-1 and Type-2 fuzzy logic controllers.
6) Comparative analysis of 3-phase 4-wire IB APF topologies: 2C IB APF, 4L IB APF, 1C FB IB APF and 3-phase 4-wire 3 FB IB APF. The 4L with an additional leg as compared to 2C IB APF topology, is a better one for superior compensation of neutral current and source current compensation. Similarly, the 3-phase 4-wire FB IB APF is a better choice for distribution system power application as there is no requirement of isolation transformer as in the case of 1C FB IB APF.
7) The SDP of the 1C FB IB APF and FB IB APF has been drastically reduced by $\sqrt{3}$ times as compared to 2C IB APF topology.

6.3 Scope for future research

1) Modeling of higher level of cascaded full-bridge interleaved buck converter based active power filter.

2) The voltage required by dc-link capacitor of the IB APF topologies may be provided by various renewable energy sources.

3) Development of distributed active power filters by using interleaved buck converters

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