Modeling and Simulation of Subthreshold Characteristics of Short-Channel Fully-Depleted Recessed-Source/Drain SOI MOSFETs

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This is to certify that the work presented in the dissertation entitled "*Modeling and Simulation of Subthreshold Characteristics of Short-Channel Fully-Depleted Recessed-Source/Drain SOI MOSFETs*" submitted by "*Gopi Krishna Saramekala"*, Roll Number: *512EC1015*, is a record of original research carried out by him under my supervision and guidance in partial fulfillment of the requirements for the degree of *Doctor of Philosophy* in *Electronics and Communication Engineering*. Neither this dissertation nor any part of it has been submitted earlier for any degree or diploma to any institute or university in India or abroad.

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Dedicated to My teachers, family, and friends

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Declaration of Originality

I, Gopi Krishna Saramekala, Roll Number 512EC1015 hereby declare that this dissertation entitled "*Modeling and Simulation of Subthreshold Characteristics of Short-Channel Fully-Depleted Recessed-Source/Drain SOI MOSFETs*" presents my original work carried out as a doctoral student of NIT Rourkela and, to the best of my knowledge, contains no material previously published or written by another person, nor any material presented by me for the award of any degree or diploma of NIT Rourkela or any other institution. Any contribution made to this research by others, with whom I have worked at NIT Rourkela or elsewhere, is explicitly acknowledged in the dissertation. Works of other authors cited in this dissertation have been duly acknowledged under the section "Reference". I have also submitted my original research records to the scrutiny committee for evaluation of my dissertation.

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Abstract

Non-conventional metal-oxide-semiconductor (MOS) devices have attracted researchers' attention for future ultra-large-scale-integration (ULSI) applications since the channel length of conventional MOS devices approached the physical limit. Among the non-conventional CMOS devices which are currently being pursued for the future ULSI, the fully-depleted (FD) SOI MOSFET is a serious contender as the SOI MOSFETs possess some unique features such as enhanced short-channel effects immunity, low substrate leakage current, and compatibility with the planar CMOS technology. However, due to the ultra-thin source and drain regions, FD SOI MOSFETs possess large series resistance which leads to the poor current drive capability of the device despite having excellent short-channel characteristics. To overcome this large series resistance problem, the source/drain area may be increased by extending S/D either upward or downward. Hence, elevated-source/drain (E-S/D) and recessed-source/drain (Re-S/D) are the two structures which can be used to minimize the series resistance problem. Due to the undesirable issues such as parasitic capacitance, current crowding effects, etc. with E-S/D structure, the Re-S/D structure is a better choice. The FD Re-S/D SOI MOSFET may be an attractive option for sub-45nm regime because of its low parasitic capacitances, reduced series resistance, high drive current, very high switching speed and compatibility with the planar CMOS technology. The present dissertation is to deal with the theoretical modeling and computer-based simulation of the FD SOI MOSFETs in general, and recessed source/drain (Re-S/D) ultra-thin-body (UTB) SOI MOSFETs in particular. The current drive capability of Re-S/D UTB SOI MOSFETs can be further improved by adopting the dual-metal-gate (DMG) structure in place of the conventional single-metal-gate-structure. However, it will be interesting to see how the presence of two metals as gate contact changes the subthreshold characteristics of the device. Hence, the effects of adopting DMG structure on the threshold voltage, subthreshold swing and leakage current of Re-S/D UTB SOI MOSFETs have been studied in this dissertation. Further, high-*k* dielectric materials are used in ultra-scaled MOS devices in order to cut down the quantum mechanical tunneling of carriers. However, a physically thick gate dielectric causes fringing field induced performance degradation. Therefore, the impact of high-*k* dielectric materials on subthreshold characteristics of Re-

S/D SOI MOSFETs needs to be investigated. In this dissertation, various subthreshold characteristics of the device with high-*k* gate dielectric and metal gate electrode have been investigated in detail. Moreover, considering the variability problem of threshold voltage in ultra-scaled devices, the presence of a back-gate bias voltage may be useful for ultimate tuning of the threshold voltage and other characteristics. Hence, the impact of back-gate bias on the important subthreshold characteristics such as threshold voltage, subthreshold swing and leakage currents of Re-S/D UTB SOI MOSFETs has been thoroughly analyzed in this dissertation. The validity of the analytical models are verified by comparing model results with the numerical simulation results obtained from ATLAS™, a device simulator from SILVACO Inc.

Keywords*: *recessed-source/drain (Re-S/D) SOI MOSFET, drain-induced barrier lowering (DIBL), hot-carrier effects (HCEs), dual-metal-gate (DMG), high-k gate dielectric, and back-gate

CONTENTS

Chapter 2

SOI MOSFETs: A General Review

Chapter 3

Analytical Modeling and Simulation of Subthreshold Characteristics of Short-Channel Dual-Metal-Gate Fully-Depleted Recessed-Source/Drain SOI MOSFET

List of Figures

List of Tables

List of Abbreviations

WSTS	World semiconductor trade statistics
Si	Silicon
s-Si	Strained silicon
Ge	Germanium
Ga	Gallium
JFET	Junction field effect transistor
MOSFET	Metal-oxide-semiconductor field effect transistor
BJT	Bipolar junction transistor
TFT	Thin-film transistor
nFET	n-channel field effect transistor
pFET	p-channel field effect transistor
Re-S/D	Recessed- source/drain
E-S/D	Elevated- source/drain
IC	Integrated circuit
CMOS	Complementary metal-oxide-semiconductor
RAM	Random-access memory
SOI	Silicon-on-insulator
s-SOI	Strained Silicon-on-insulator
SOIAS	Silicon-on-insulator with active substrate
BOX	Buried oxide
DMG	Dual-metal-gate
ASD	Asymmetric source/drain
SSD	Symmetric source/drain
DSSB	Dopant segregated schottky barrier
TRIMAGS	Tri-material-gate stacks
MuGFETs	Multi-gate field effect transistors
ITRS	International technology roadmap for semiconductors
VLSI	Very large scale integration
ULSI	Ultra-large scale integration

DIBL	Drain-induced barrier-lowering
GIDL	Gate-induced drain leakage
RILC	Radiation-induced leakage current
SISP	Substrate induced surface potential
LOCOS	Local oxidation of silicon
FIPOS	Full isolation by porous oxidized silicon
SWCVD	Selective tungsten chemical vapor deposition
SIMOX	**S**eparation by implantation of oxygen
SOS	Silicon-on-sapphire
HCEs	Hot-carrier effects
HOT	Hybrid orientation technology
SCEs	Short-channel effects
QMEs	Quantum mechanical effects
UTB	Ultra-thin body
FD	Fully-depleted
PD	Partially-depleted
DD	Drift-diffusion
IR	Internet resource
RF	Radio frequency
FOMs	Figures-of-merits

List of Symbols

ε_{si}	Permittivity of Si (F cm^{-1})
ε_{ox}	Permittivity of SiO_2 (F cm^{-1})
ε_{k}	Permittivity of High-*k* dielectric (F cm^{-1})
t_{Si}	Silicon channel thickness (nm)
t_{ox}	Oxide thickness (nm)
t_{box}	Buried oxide thickness (nm)
t_{rsd}	Recessed source/drain thickness (nm)
t_{sp}	Spacer thickness (nm)
d_{box}	Lengths of source/drain overlap (nm)
$L_1 : L_2$	Ratio of control gate length to screen gate length
L	Channel length (nm)
W_d	Depletion layer width (nm)
$\phi(x,y)$	Potential in channel region (V)
q	Charge of electron ($1.6e^{-19}$ C)
N_a	Acceptor doping concentration of channel (cm^{-3})
N_d	Source/drain doping concentration (cm^{-3})
N_{sub}	Substrate doping concentration (cm^{-3})
V_{fb}	Flat-band voltage (V)
ϕ_M	Gate material work function (eV)
χ_{si}	Electron affinity of Si (eV)
E_g	Silicon energy band gap (eV)
V_T	Thermal voltage (V)
n_i	Intrinsic carrier density (cm^{-3})
$\phi_f(x)$	Front channel surface potential (V)

$\phi_b(x)$	Back channel surface potential (V)
V_{GS}	Gate to source voltage (V)
V_{DS}	Drain to source voltage (V)
V_{BG}	Back-gate voltage (V)
V_{bi}	Built in voltage (V)
λ	Characteristic length (nm)
k	Boltzmann's constant ($1.38e^{-23}$ JK^{-1})
T	Temperature (300K)
C_{bot}	Bottom fringing capacitance (fF)
C_{ox}	Gate oxide capacitance (fF)
C_{rsd}	Recessed source/drain capacitance (fF)
C_{box}	Buried-oxide capacitance (fF)
C_{Si}	Channel capacitance (fF)
V_{th}	Threshold voltage (V)
$\phi_{S\,min}$	Minimum surface potential (V)
ϕ_{vc}	Virtual cathode potential (V)
E	Electric field (V cm^{-1})
I_s	Subthreshold current (A/um)
S	Subthreshold swing (mV/Dec.)
μ	Mobility of the free carrier ($cm^2V^{-1}sec^{-1}$)
W	Width of the device along Z-axis (nm)
J	Charge density (C/cm^3)

Chapter 1

Introduction

1.1 Introduction

The semiconductor industry has grown enormously since 1960 and today it is one of the world's largest industries. Such a phenomenal growth was never seen before in any sector in the history of mankind. World Semiconductor Trade Statistics (WSTS) forecast its 2016 global semiconductor sales growth to $355.3 billion, which is 3.1% higher from 2015 sales. Moreover, the growth of the semiconductor industry has not been monotonous but has a great impact on other industries like communication, transportation, healthcare, security and surveillance, smart buildings and homes, and space etc. A semiconductor material is one whose electrical conductivity lies in between those of insulators and good conductors which are classified as intrinsic (pure) and extrinsic (impure) semiconductors. Even though, some pure elements and several compounds exhibit semiconductor properties, silicon (Si), germanium (Ge), and compounds of gallium (Ga) are the most commonly used in electronic devices. Further, depending upon the used impurity, extrinsic semiconductors are sub-divided into two classes which are *n*-type semiconductors and *p*-type semiconductors. Application of the semiconductors has been expanding day by day widely from radio in the 1960s to almost every electronic device that has an on-off switch in 2016. Semiconductor devices have been rigorously pursued targeting performance improvement in terms of higher speed, lower power consumption, higher efficiency with much functionality. The continuous need of performance improvement has been the motivating force behind the invention of new semiconductor devices and makes this field really fascinating as well as challenging.

1.2 History and Perspective of Transistors

A transistor (**tran**sfer + re**sistor**) is a semiconductor device which can amplify or switch electrical signals. It was invented in the mid-1940s by a team of scientists namely William Shockley, John Bardeen, and Walter Brattain [Brinkman *et al.* (1997)]. This solid state option of the vacuum tubes revolutionized the field of electronics and led to smaller and cheaper radios, calculators, and computers, among other things. The idea of 'field-effect transistor (FET)' was presented and patented by Lilienfeld in 1926 and 1930, respectively [Lilienfeld (1930)]. Shockley proposed a 'junction field-effect transistor (JFET)' in 1952 [Shockley (1952)] based on the unipolar concept with three terminals. In 1960, Kahng and Atalla [Kahng *et al.* (1960)] presented one of the most essential unipolar transistors called the metal-oxide-semiconductor field-effect transistor (MOSFET) with four terminals including a substrate for controlling the transport property more effectively. Even after the MOSFETs' invention, the BJT remained the transistor of choice for several analog circuits due to its superior electrical properties and ease of manufacturing.

In 1952, a technique to integrate a variety of electronic components onto a monolithic semiconductor crystal was invented [Internet Resource (IR1)]. In 1957, Jack Kilby [Kilby (1964)] developed an integrated circuit (IC) comprises of transistors, resistors, and capacitors, and received the Noble Prize in physics in the year 2000. Further, in 1959, a monolithic chip made of silicon material was presented by Robert Noyce, where metal vaporization technique was used to create interconnects. The major breakthrough in the improvement of the integration level onto the chip was marked in 1963, when the complementary-metal-oxide-semiconductor (CMOS) technology was invented [Wanlass *et al.* (1963)]. A CMOS circuit is designed with both *n*-channel and *p*-channel MOSFETs on a single substrate [Wanlass *et al.* (1963)]. Using the CMOS technology, researchers have been able to integrate hundreds of millions of transistors on a single chip which can even operate at room temperature [Taur *et al.* (1998)]. Today, the CMOS technology is the leading semiconductor technology and has been used for the fabrication of microcontrollers, microprocessors, static RAM, and other digital logic circuits because of

high packing density. Fig. 1.1 gives a sketch of the major milestone events in the development of CMOS technology.

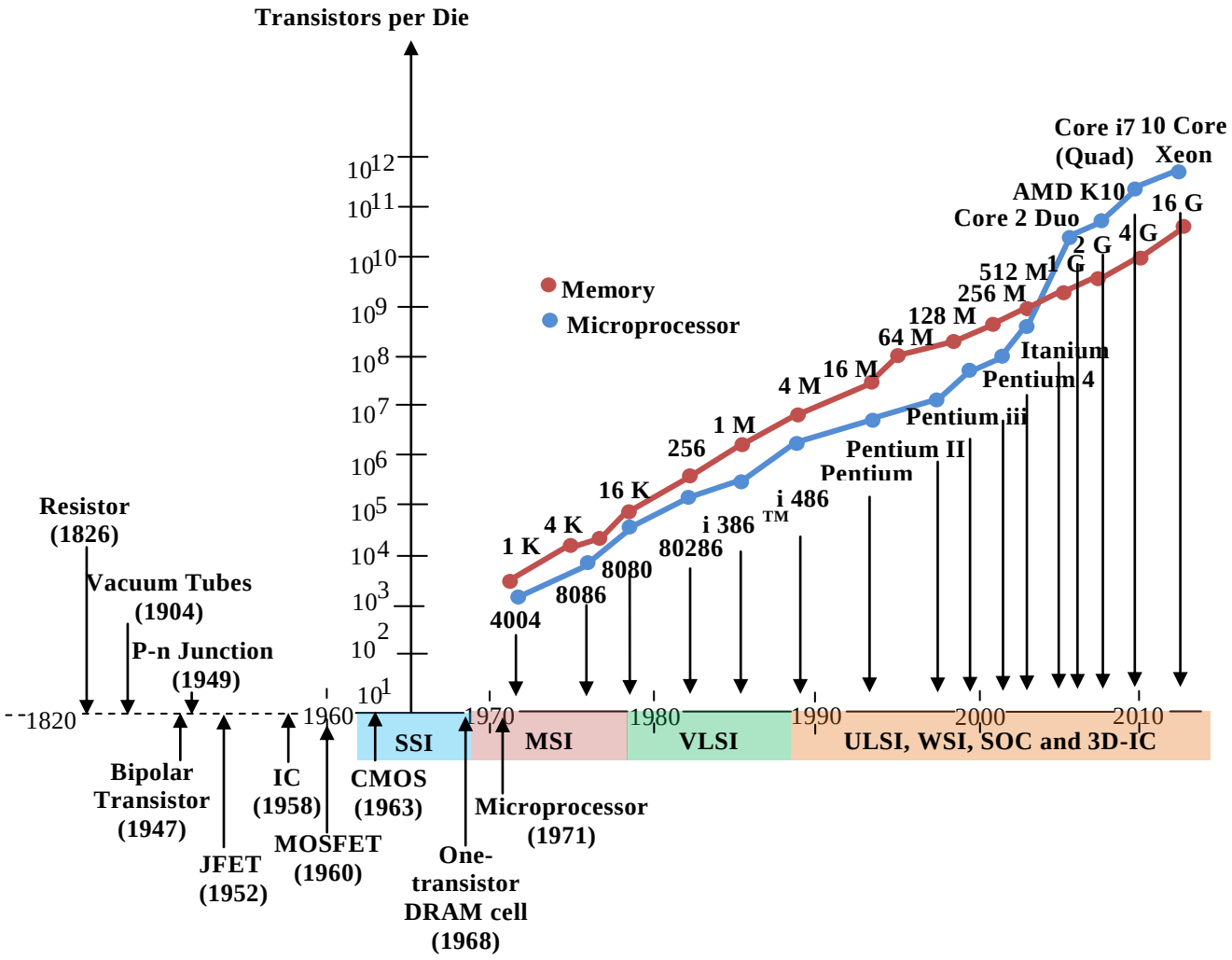


Fig. 1.1: A brief timeline of the major milestones in the development of CMOS integration [Taur *et al.* (1998)]

Moore's law, proposed by Intel's co-founder Gordon Moore in 1965, states that the number of transistors per square inch on an integrated circuit will get double in every 18 months [Moore (1965), Thompson (2006)]. Moore's law has been an important guideline in developing the technology for the semiconductor industry since 1965. Semiconductor industry witnessed two important milestones in the year 1989 and 2005. The million and billion transistors were fabricated onto a chip for the first time in the year 1989 and 2005, respectively [Clarke (2005)]. Thus, ultra-large-scale integration (ULSI) was possible in

the year 2005 because of the MOSFET scalability and advanced manufacturing technology.

1.3 MOSFET Technology Scaling

Scaling of CMOS transistors below 32nm technology node causes severe short-channel effects (SCEs) such as subthreshold swing roll-up and threshold voltage roll-off [Wong (2002)]. It also increases the standby power dissipation worsening the switching characteristics and offers lower Ion/Ioff ratio. Hence, the suppression of the SCEs up to the tolerable level is of significant importance of the MOSFET scaling to continue the IC technology scaling trend.

The first scaling theory proposed by Dennard *et al.* [Dennard *et al.* (1974)] is known as 'constant-field scaling' theory. The principle of this theory is to scale the supply voltage and device dimensions (both horizontal and vertical) by the same scaling factor $S > 1$, in order to keep electric field unchanged. As a result, the circuit speeds up by the same factor S, and reduces the power dissipation per circuit by a factor of S^2. The other important scaling schemes are constant-voltage scaling and generalized scaling. The scaling rules for various device parameters and circuit performance factors of constant-field, constant-voltage, and generalized scaling are shown in Table 1.1

Several attempts have been made to find out the alternative ways to follow Moore's law [Ieong *et al.* (2006), Thompson *et al.* (2006), Colinge (2008)]. As a result of these efforts, several kinds of techniques and alternative materials have been proposed for CMOS performance improvement [Chang *et al.* (2003), Ieong *et al.* (2006)]. Apart from introducing new materials for the manufacturing of transistors to improve the functionality per unit area, new transistor structures are also finding significance in the microelectronics industry to keep the scaling alive [Chang *et al.* (2003), Ieong *et al.* (2006)]. Further, new materials, structures, and technologies that have been adopted by the semiconductor industry to combat the increasing leakage power and other scaling issues are discussed in section 1.4.

Device Parameters		Multiplication Factor, $S>1$ Scaling parameter, α			
		Constant -field Rules	**Constant -voltage Rules**	**Generalized Rules**	
Scaling assumptions	Device dimensions (t_{ox}, L, W)	$1/S$	$1/S$	$1/S$	
	Doping concentration (N_a, N_d)	S	S^2	αS	
	Voltage (V)	$1/S$	1	α/S	
Derived scaling behavior of device parameters	Electric field (E)	1	S	α	
	Depletion-layer width (W_d)	$1/S$	$1/S$	$1/S$	
	Capacitance ($C=\varepsilon A/t$)	$1/S$	$1/S$	$1/S$	
	Inversion/ layer charge density(Q_1)	1	S	1	
				Long Channel	**Velocity Saturation**
	Carrier velocity (v)	1	S	α	1
	Drift current (I)	$1/S$	S	α^2/S	α/S
	Channel resistance (R_{ch})	1	$1/S$	α^2/S	α/S
Derived scaling behavior of circuit parameters	Circuit delay time ($\tau \approx CV/I$)	$1/S$	$1/S^2$	$1/\alpha S$	$1/S$
	Power dissipation per circuit ($\tau \approx CV/I$)	$1/S^2$	S	α^3/S^2	α^2/S^2
	Power density (P/A)	1	S^3	α^3	α^2
	Power-delay product per circuit ($\tau \approx CV/I$)	$1/S^3$	S	α^2/S^3	

Table 1.1: Scaling of device dimensions and circuit parameters [Taur (1998)]

1.4 CMOS Technology Boosters

As discussed in the previous section, the main challenge faced by the CMOS scaling is the presence of excess short-channel effects, when the device channel length enters in sub-100nm regime. CMOS technology boosters such as strained channel, hybrid-orientation-technology (HOT), high-*k* dielectric, multi-gate, back-gate and non-conventional MOS structures help to continue CMOS scaling in sub-100nm regime. Few CMOS technology boosters are discussed below.

1.4.1 Strained-Silicon (s-Si) Technology

Strained-Si technology has been adopted by the microelectronics industry as a performance booster for mainstream ULSI since the introduction of 32nm technology

node [Takagi (2007)]. Basically, strained-Si technology modifies the lattice constant of the material by a lattice deformation, which changes its energy band structure to trap carriers through the well formation and enhances mobility.

One of the techniques to generate the strain in the silicon channel is to grow a thin silicon epitaxial layer on the silicon-germanium ($Si_{1-x}Ge_x$) substrate [Barraud *et al.* (2005)], where, *x* is the mole fraction of germanium in the silicon-germanium compound. The mole fraction *x* can be varied in order to introduce different amount of strain in the silicon film. In strained Si film, the 6-fold degenerate valley in the conduction band splits into a 2-fold non-planar and 4-fold planar degenerate valleys [Chaudhry *et al.* (2010)]. In the same way, the valence band also splits into two bands consisting of light and heavy holes respectively [Chaudhry *et al.* (2010)]. The carriers then prefer the lower energy valley, while occupying them, resulting in the reduction of inter-valley scattering and effective mass of the carrier [Chaudhry *et al.* (2010)]. By increasing the Ge concentration in the relaxed $Si_{1-x}Ge_x$ substrate, the amount of biaxial strain increases and, therefore, a higher magnitude of the mobility enhancement can be achieved. The lattice structure strained-Si which grows on SiGe is shown in Fig. 1.2

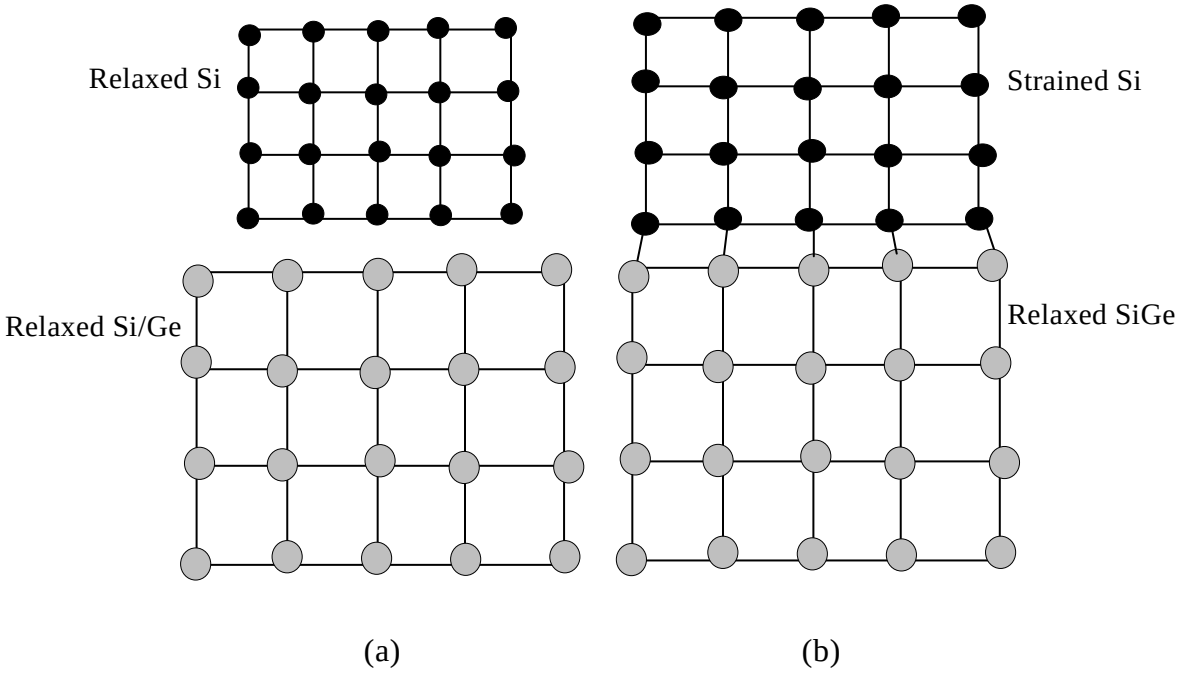


Fig. 1.2: Lattice structure of (a) unstrained Si and SiGe (b) strained Si on relaxed SiGe

1.4.2 Hybrid-Orientation-Technology (HOT)

Hybrid-Orientation-Technology (HOT) improves carriers' mobility in Si CMOS devices [Yang *et al.* (2003)]. Properties that are exploited for mobility enhancement are surface orientation and tensile strain. To take full advantage of the carrier mobility dependence on surface orientation, nFETs should be fabricated on the (100) silicon surface and pFETs on the (110) silicon surface [Yang *et al.* (2006)]. The *n*-channel FET is formed in (100) orientation layer due to low oxide-interface charge density and highest electron mobility. The *p* channel FET is formed in (110) orientation layer in which the atom density is higher compared to (100) orientation layer, as can be observed from the Fig. 1.3. Mixing these two orientations on a single substrate is done by **Hybrid-Orientation-Technology** (HOT). It provides a way of reducing the current drive imbalance between *n*-type and *p*-type channels [Sheraw *et al.* (2005)]. The technological processes that fabricate these hybrid surface layers are membrane transfer and overgrowth. HOT has received considerable attention by researchers since its introduction due to its fabrication processes compatibility with the current VLSI technology [Yang *et al.* (2003), Sheraw *et al.* (2005)].

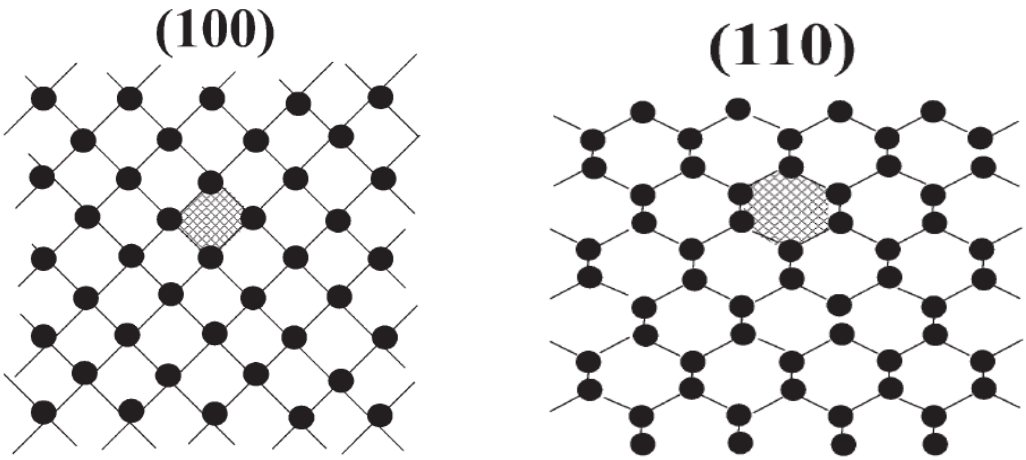


Fig. 1.3: Schematic images of silicon (100) and (110) surfaces. (Shadowed areas are the channel areas indicating that the channeling effect of implanted ions is larger on the (110) surface) [Yang *et al.* (2006)]

1.4.3 High-*k* Dielectric Materials in MOS Transistors

When the device channel length is scaled down below 32nm, an ultra-thin gate oxide, i.e., less than 1nm~five atomic layers becomes a necessity [Andresa *et al.* (2007)]. However, this very thin layer of gate oxide tends to leak a lot of current which leads to excess power consumption and a build-up of heat. Hence, to cut down the gate-leakage current, a physically thicker gate dielectric without compromising the gate-channel electrostatics coupling is required. In other words, the dielectric material needs to be physically thick but electrically thin [Internet Resource (IR2)]. The physical thickness of a high-*k* dielectric gate oxide is given by $t_k = t_{ox}\left(\frac{\varepsilon_{SiO_2}}{\varepsilon_k}\right)$, where, ε_{SiO_2} is the permittivity of silicon dioxide, ε_k is the permittivity of high-*k* dielectric material and t_{ox} is the effective gate oxide thickness of the device. Researchers have found some suitable high-*k* dielectric materials to control both short-channel effects and gate-leakage current simultaneously. Materials like HfO_2 (relative permittivity, k =22), ZrO_2 (k =25) and Ta_2O_5 (k =26), $HfSiO_4$ (k =27), are strong contenders to replace SiO_2 when the channel length is scaled down below 32nm [Park *et al.* 2015, Robertson (2004)].

1.4.4 Dual-Metal-Gate (DMG) MOSFETs

Dual-Metal-Gate (DMG) structure which was proposed by Long *et al.* [Long *et al.* 1999] is one of the prominent CMOS technology boosters today. The cross-sectional view of dual-metal-gate (DMG) FET is shown in Fig. 1.4. The gate electrode of a DMG FET is made of two different materials which are termed as control and screen gates with work function ϕ_{M_1} and ϕ_{M_2} respectively. The work function of the control gate (ϕ_{M_1}) is higher than that of screen gate (ϕ_{M_2}) i.e. $\phi_{M_1} > \phi_{M_2}$ for an *n*-channel MOSFET and vice versa for a *p*-channel MOSFET [Long *et al.* (1999)]. A device with DMG structure is found to be superior than a conventional one as it possesses excellent short-channel effects (SCEs) immunity, lower hot-carrier effects (HCEs) and drain-induced barrier lowering (DIBL) [Long *et al.* (1999), Chaudhry *et al.* (2004), Kumar *et al.* (2004), Jin *et al.* (2010)].

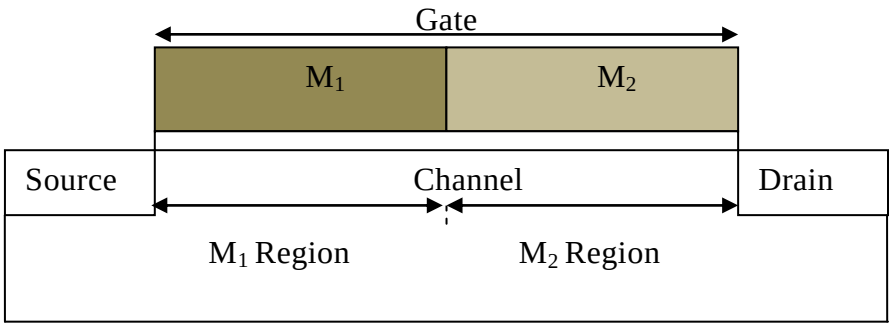
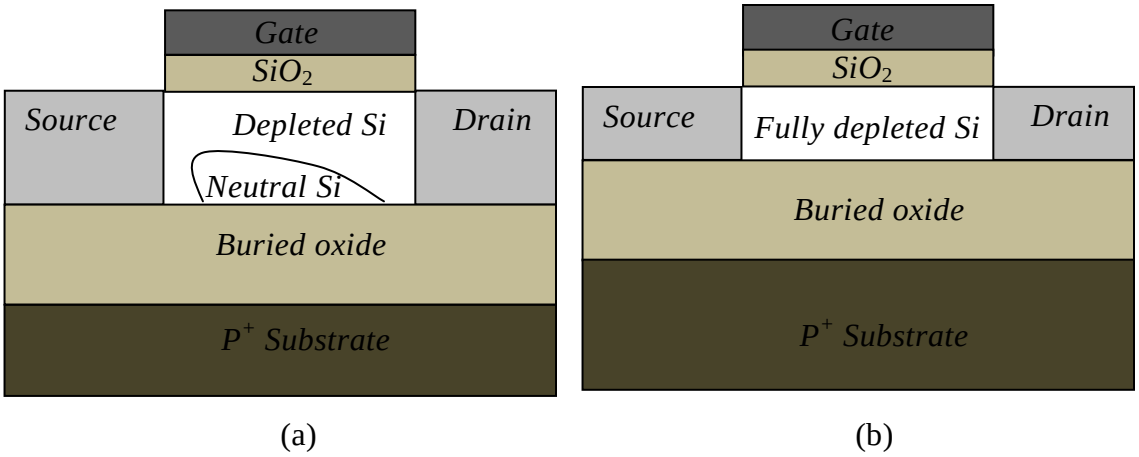


Fig. 1.4: Cross-sectional view of a dual-metal-gate (DMG) FET [Long *et al.* (1999)]

1.4.5 Non-Conventional MOSFETs

Beyond 32nm technology node, non-conventional MOS structures have been pursued relentlessly in order to continue the scaling of MOS structures. Non-conventional MOSFETs may be classified into following two broad categories (i) planar silicon-on-insulator (SOI) MOSFETs, and (ii) non-planar multi-gate MOSFETs. In SOI MOSFETs, a thin Si channel is grown on a thick buried-oxide (BOX) insulator which is grown on a Si substrate. The thin Si channel on BOX causes the reduced parasitic capacitances, improved electrical isolation, better immunity to radiation-induced leakage current (RILC) and diminished latch-up effect. SOI MOSFETs can be categorized into partially-depleted (PD) SOI MOSFETs and fully-depleted (FD) SOI MOSFETs. In the PD devices, the silicon film is made to be much thicker than the maximum gate depletion width so that a neutral body region exists below the gate depletion boundary as shown in Fig. 1.5 (a). On the other hand, the silicon channel thickness of fully-depleted SOI MOSFETs is made to be thin enough so that the entire film is depleted under the zero-bias condition of the device. The schematic structure of a FD SOI MOSFET is shown in Fig. 1.5 (b).

It may be mentioned that unlike the bulk MOSFETs, the body of PD-SOI devices is not tied to the ground. In other words, the body can be floated to different potentials depending on the applied drain and gate voltages. When the device operates under large drain bias conditions, carriers of the same type as that of the neutral body may be generated by impact-ionization near the drain and get stored in the neutral region of the device. The stored charges may alter the body potential and hence the threshold voltage of the device leading to an adverse phenomenon called the floating body effect of the SOI MOSFETs [Yoshimi *et al.* (1989)].



(a) (b)

Fig. 1.5: Schematic structure of (a) partially-depleted (PD) SOI MOSFET (b) fully-depleted (FD) SOI MOSFET

The SOI MOSFETs have a number of advantages over the bulk MOSFETs. The advantages of ultra-thin SOI MOSFETs include reduced junction capacitance, improved electrical isolation, the possibility of optimal operation with relatively light channel doping, better immunity to radiation-induced leakage current and diminished latch-up effect [Colinge (2004), Celler *et al.* (2003), Markov *et al.* (2012)]. Further, SOI devices have lower SCEs than the bulk devices. The buried-oxide (BOX) cuts off most of the leakage current path for a MOSFET fabricated on it. Another important merit of SOI technology is that it provides the base for new device structures such as multi-gate field-effect transistors (MuGFETs) as shown in Fig. 1.6. The MuGFETs may be classified as double-gate planar SOI transistor, double-gate non-planar FinFET, tri-gate FET, quadruple-gate FET, gate-all-around (or surrounding-gate) FET and nanowire FET [Park *et al.* (2001), Yang *et al.* (2002), Colinge (2004), Jiménez *et al.* (2004), Manoj *et al.* (2008), Bangsaruntip *et al.* (2009), Huang *et al.* (2010), Kuhn (2012)]. The MuG MOS structures provide extra gate control over the channel region. Hence, effective suppression of the off-state leakage current and SCEs can be achieved [Colinge (2008)]. Additionally, multi-gate MOS structures have the flexibility that they may be controlled by a single-gate electrode, wherein the multiple-gate surfaces act electrically a single-gate, or by independent-gate electrodes [Ferain *et al.* (2011)].

However, several technological problems of MuGFETs must be solved before, to use MuGFETs in VLSI circuits. Some of these problems are discussed below.

- The design and fabrication process of non-planar structures (MuGFETs) are more complicated than the planar structures (SOI MOSFETs). MuGFETs require more advanced fabrication techniques such as improved etching accuracy and reliability [Pacha *et al.* (2006), Masahara *et al.* (2009)].

- MuGFETs exhibits a very undesirable characteristic known as corner-effect which occurs due to the electrostatic coupling between two adjacent gates at the corners. This effect degrades the device performance by increasing the off-state leakage current [Zhao (2006), Yu *et al.* (2007)].

- Another important challenge associated with the performance and reliability of MuGFETs is that in order to retain the desired values for threshold voltage, subthreshold current and subthreshold swing, the width of the fin needs to be decreased as gate length is decreased [Masahara *et al.* (2009)]. This imposes a difficult challenge on the fabrication process.

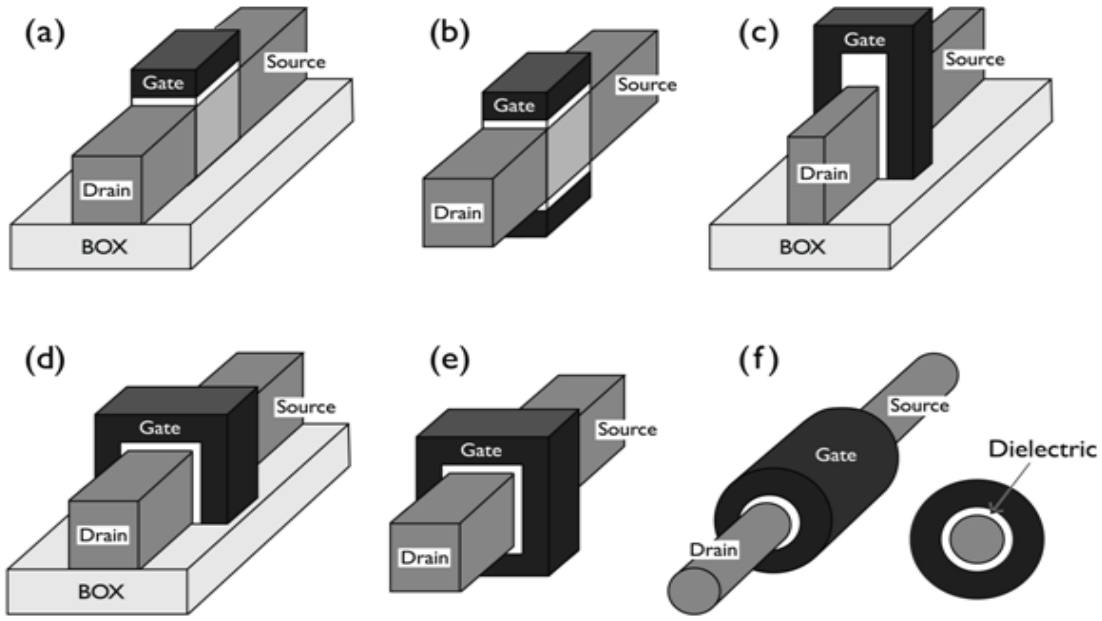


Fig. 1.6: Various SOI device: (a) single-gate SOI transistor, (b) double-gate planar SOI transistor, (c) double-gate non-planar FinFET, (d) tri-gate FET, (e) quadruple-gate (or gate-all-around) FET, (f) gate-all around (or surrounding gate) FET (nanowire FET). [Kim (2010)]

1.4.6 Back-Gated SOI MOSFETs

SOI MOSFETs are very attractive for low power applications because of many reasons including lower junction capacitance, steeper subthreshold slope, and higher short-channel effect immunity [Kumar *et al.* (2008)]. In addition, back-gate of SOI MOSFETs may be used to control the threshold voltage of the structure. The cross-sectional view of a fully-depleted SOI MOSFETs with back-gate control is shown in Fig. 1.7. The front-gate can be used to switch the device, whereas the back-gate can be used to set the correct threshold voltage.

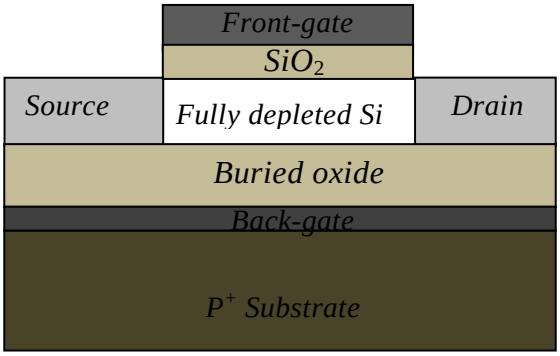


Fig. 1.7: Cross-sectional view of a fully-depleted SOI MOSFETs with back-gate control

1.5 SOI MOSFET

In SOI-based CMOS technology, the conventional silicon substrate of a bulk MOSFET is replaced by a layered silicon-insulator (i.e. SiO_2 or sapphire)-silicon substrate to reduce parasitic device capacitances. The top layer of the SOI substrate which is used as the channel of the device is usually a very thin layer of crystalline silicon. The thin silicon layer is electrically isolated from the substrate by a thick (typically 100nm or more) buried-oxide layer. Many techniques have been developed for producing a film of single crystal silicon on an insulator [Colinge (2004)]. Silicon-on-insulator structure can be produced from a bulk silicon wafer by isolating a thin silicon layer from the substrate through the Full isolation by porous oxidized silicon (FIPOS) or through the ion beam synthesis of a buried insulator layer separation by implanted oxygen (SIMOX) [Colinge (2004)]. Moreover, there is another layer transfer technique in which the smart-cut has enabled the

"peeling-off" of a thin silicon layer from a wafer and its transfer onto an oxidized wafer. The approaches for making SOI wafers have been discussed in section 1.5.1.

1.5.1 SOI Manufacturing Technologies

- **SOS (Silicon-on-Sapphire)**

Silicon-on-sapphire (SOS) is obtained by an epitaxial growth of a thin layer of silicon on a sapphire (Al_2O_3) wafer. SOS is used for manufacturing of high-frequency and high-power CMOS integrated circuits in satellite communication systems, cellular telephones, and others [Internet resource (IR3)]. In the early days, SOS faced many difficulties in the commercial manufacturing of small-scale transistors. Later, various techniques including solid-phase epitaxial and regrowth (SPEAR), double solid-phase epitaxial (DSPE), were developed to reduce the problem associated with the fabrication of SOS based transistors [Paul *et al.* (2004)]. The SOS wafer fabrication process is illustrated in Fig. 1.8.

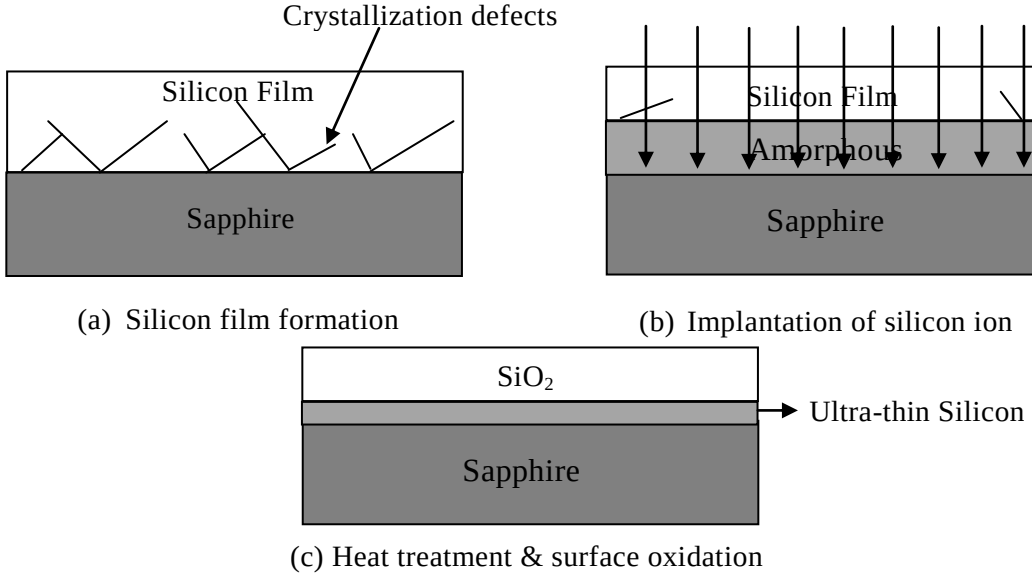


Fig. 1.8: SOS wafer fabrication flow

- **SIMOX (Separation by Implanted Oxygen)**

In SIMOX technique, oxygen atoms are implanted into Si wafer in order to synthesise SiO_2. The formation of SiO_2 by O_2-ion implantation into Si wafer was first reported by Watanabe and Tooi in 1966 [Watanabe *et al.* (1966)]. Later, in 1978, K. Izumi *et al.* [Izumi (1978)] invented a new SIMOX technique and fabricated a 19-stage CMOS ring

oscillator using a buried SiO_2 layer formed by O_2-ion ($^{16}O^+$) implantation into silicon. The SIMOX process is shown in Fig. 1.9.

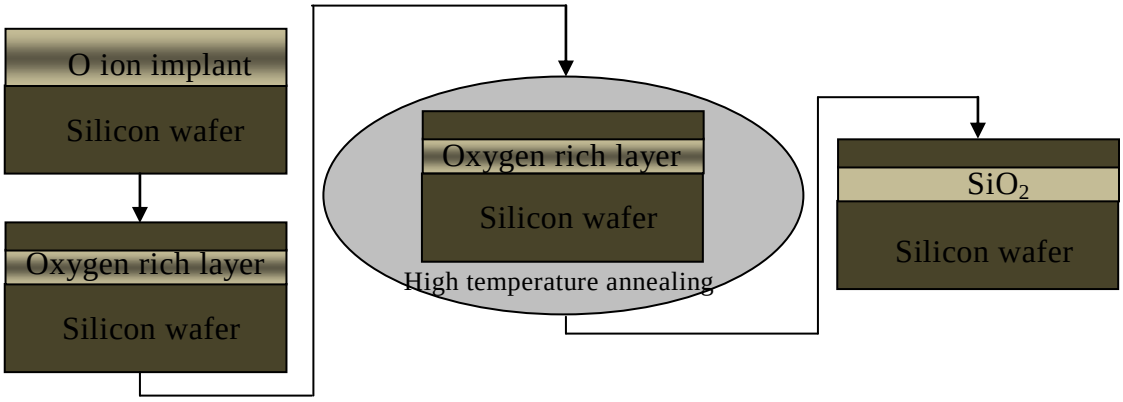


Fig. 1.9: SIMOX process

- **Smart-Cut**

Using smart-cut technique, a very thin surface layer of crystalline silicon material is transferred onto the insulating substrate. In 1995, Michel Bruel invented the smart-cut process [Bruel *et al.* (1995)]. This process contains three major steps which are: implantation of H^+ ions, bonding to a stiffener, and thermal annealing [Colinge (2004)]. The wafers which are fabricated by the smart-cut process are called as UNIBOND wafers [Colinge (2004)]. The sequence of graphics given in Fig. 1.10 describes the process of SOI wafer fabrication using the smart cut technology.

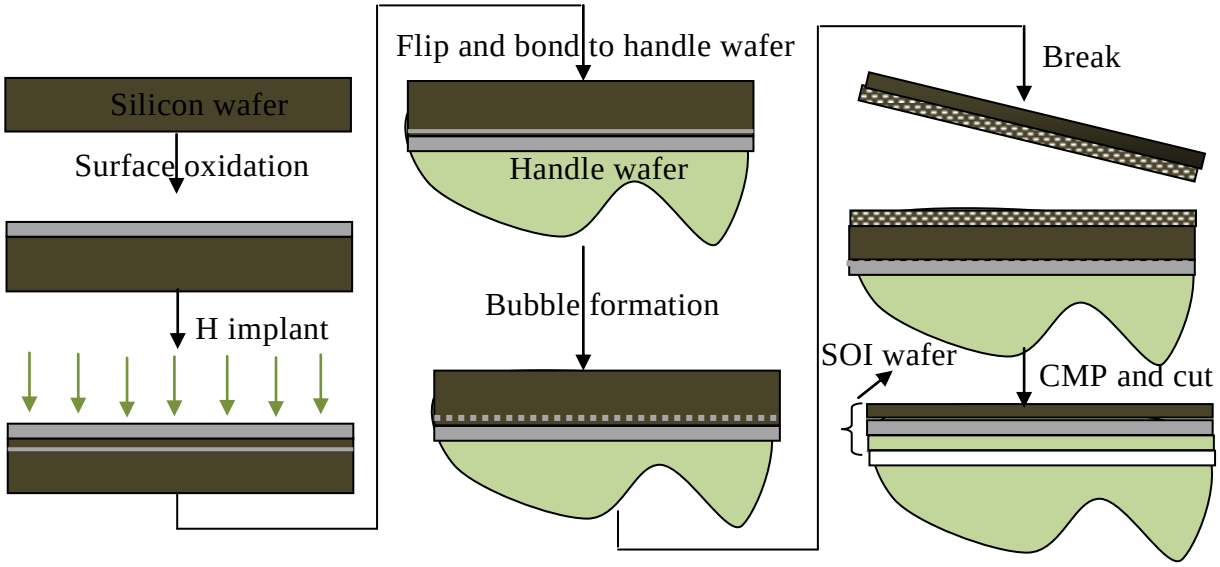


Fig. 1.10: Smart-cut process

1.5.2 Salient Features of SOI MOSFETs

SOI MOSFETs offer several advantages over bulk silicon CMOS such as high speed, low power dissipation, low drain/source junction capacitances, low leakage currents, high short-channel effects immunity, high subthreshold voltage swing, and better manufacturing compatibility with the existing bulk silicon CMOS technology [Colinge *et al.* (2004), Kumar *et al.* (2008)]. Some of the advantages of SOI MOSFET are discussed below.

- **Low Drain Junction Capacitance:**

In bulk MOSFETs, the parasitic capacitance at the drain junction consists of two components: Capacitance between the drain/substrate junction and the capacitance between the drain and the channel stop implant under the field oxide as shown in Fig 1.11(a). As scaling the MOSFETs to nanometer regime, highly doped substrate regions are inevitable which leads to high junction capacitances. On the other hand, SOI MOSFETs mainly contains only one parasitic capacitance which exits between the buried oxide and the silicon substrate. This capacitance is typical much lower when compared to the capacitance of bulk MOSFETs [Colinge (2004)]. Thus, reduced parasitic capacitances in SOI MOSFETs contribute to the high performance. In addition, the buried oxide thickness does not necessarily to be scaled down with device miniaturization.

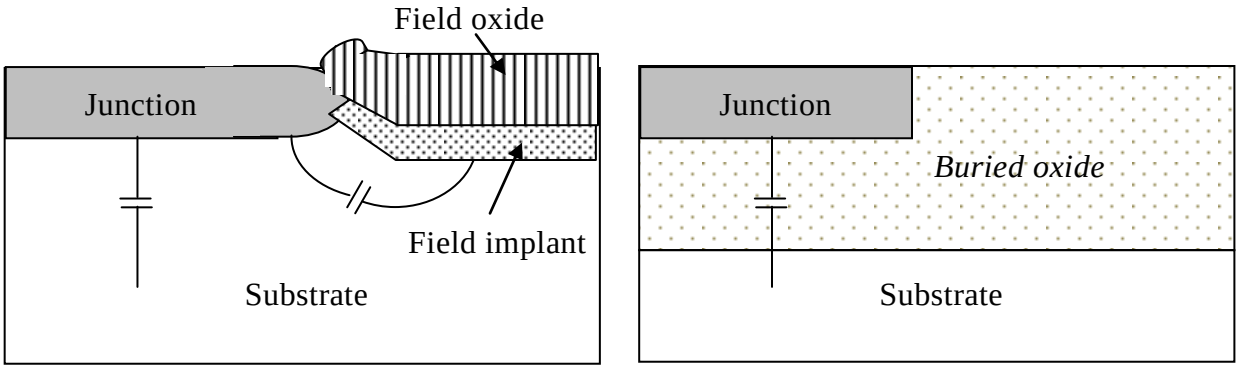


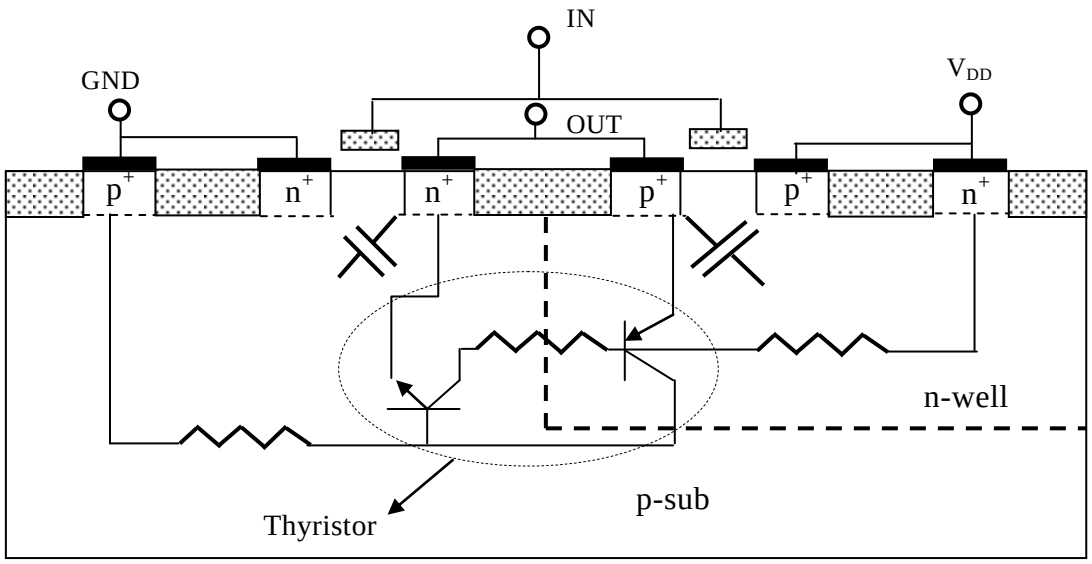
Fig. 1.11: Junction capacitances [Colinge (2004)]

- **Reduced Short-Channel Effects (SCEs) :**

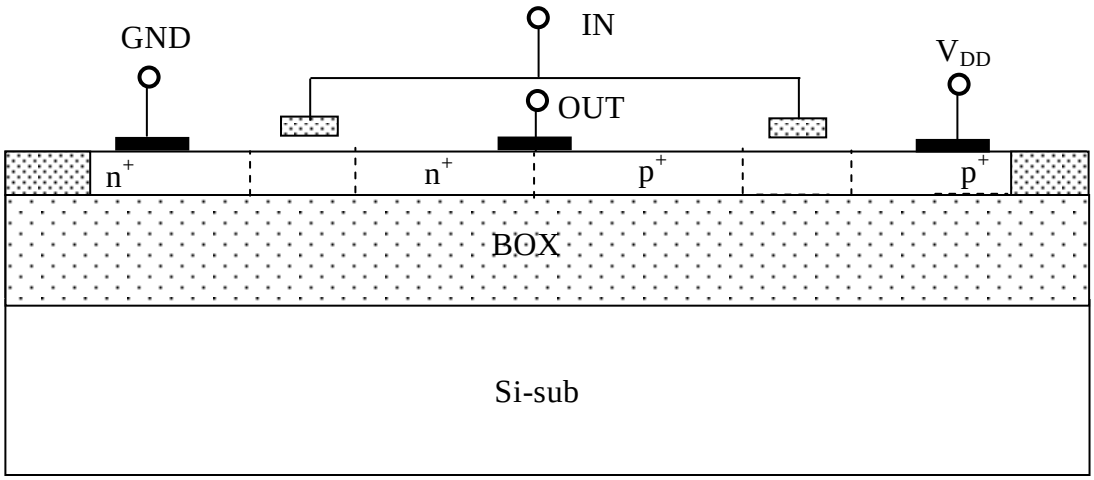
In SOI MOSFETs, SCEs such as threshold voltage roll-off and DIBL are mainly influenced by the channel thickness, buried oxide thickness, substrate doping and channel doping concentration. The threshold voltage roll-off occurs at the smaller gate voltages in SOI MOSFETs than in bulk MOSFETs, by using ultra-thin SOI film the threshold voltage roll off can be reduced. Another SCE, DIBL occurs due to the charge sharing between the gate and the S/D junctions. However, in ultra-thin SOI MOSFETs, the channel region prohibits drain to take control of channel charges. [Colinge (2004)].

- **No Latch-Up :**

Latch-up is an unwanted condition occurs in bulk CMOS devices as shown in Fig. 12 (a). The triggering of inherent PNPN thyristor structure formed by the Bi-polar transistors in bulk CMOS devices lead to severe problems in device performance. However in SOI CMOS devices, the latch-up problem is ruled out as there is electrically isolated thick buried oxide layer between the devices as shown in Fig 1.12(b) [Matloubian (1989), Kushwaha (2011)].



(a)



(b)

Fig. 1.12: Cross-sectional view of (a) bulk CMOS (b) SOI CMOS

1.5.3 Challenges and Remedies

Although SOI technology is already a mature technology, there are still some serious challenges exist. Primary challenges include fabrication of ultra-thin film, thin box, excellent thickness uniformity and lower defect content [Colinge (2004)]. Further, due to the ultra-thin source and drain regions, FD SOI MOSFETs possess large series resistance which leads to the poor current drive capability of the device despite having excellent short-channel characteristics [Zhang *et al.* (2004)]. Furthermore, interconnects are essential to be a minimum of sub-10nm in diameter in order to connect extremely small devices [Li *et al.* (2009)]. As the interconnect wires diameter scale downs to the mean free path of electrons, the surface scattering and boundary scattering would delay the electronic conduction in wires, [Li *et al.* (2009)]. Therefore, the circuit operation becomes slower and it is not promising to attain performance enhancement from scaling [Li *et al.* (2009)]. Hence, the FD SOI MOSFET structure needs some structural modifications to overcome these problems. The modification can be done in two possible ways (i) by elevating S/D regions upward (ii) by recessing S/D regions deeper into the buried oxide. Based on these, two different kinds of FD SOI MOSFET structures have been proposed as follows:

- **Elevated Source/Drain (E-S/D) SOI MOSFETs**

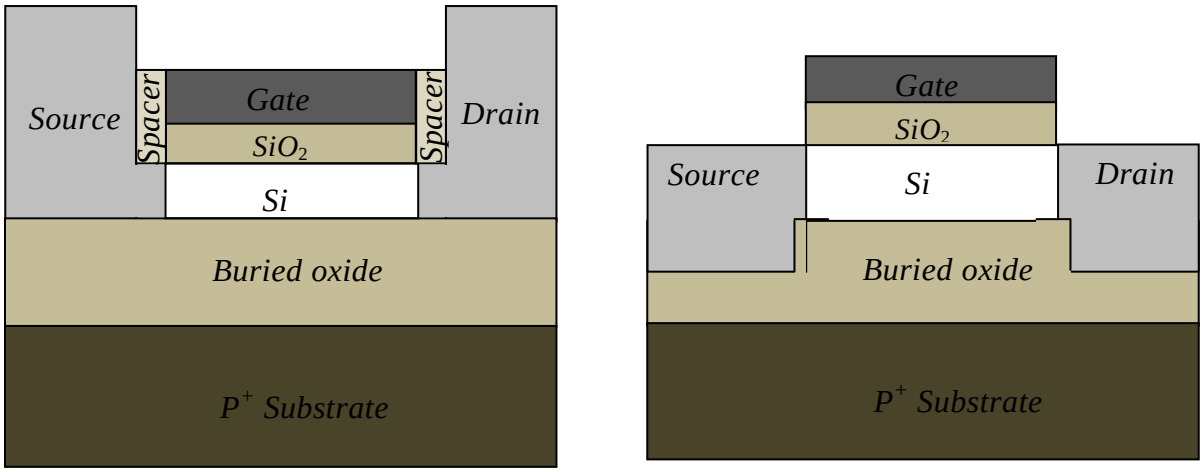
The elevated source/drain (E-S/D) MOSFET was proposed and fabricated by Wong *et al.* [Wong *et al.* (1984)]. In Fig. 1.13 (a), the elevated source/drain (E-S/D) regions are created by growing selective epitaxial silicon at the top of source/drain regions. In E-S/D SOI MOSFET, the elevated source/drain regions are separated from the gate electrode by gate spacers. As a result, a parasitic capacitance (Miller capacitance) coming from the coupling between the gate and the elevated source/drain regions [Zhang *et al.* (2004)]. Further, E-S/D regions are affected with current crowding effects which form a non-homogenous distribution of current density through a semiconductor, especially at the surrounding area of the contacts and over the PN junctions and leads to localized overheating and formation of thermal hot spots [Thean *et al.* (2006)]. Moreover, due to the elevated source/drain regions in E-S/D SOI MOSFET, the device structure loses its planar nature. Hence, E-S/D may not be compatible with planar CMOS technology.

- **Recessed-Source/Drain (Re-S/D) SOI MOSFETs**

In Re-S/D SOI MOSFET, the large series resistance is cut down by extending the source and drain regions deeper into the buried-oxide (BOX) [Hanafi *et al.* (2005), Ahn *et al.* (2004), Ahn *et al.* (2006), Wu *et al.* (2015)]. The Re-S/D ultra-thin body (UTB) SOI MOSFET was designed and fabricated by Zhang *et al.* [Zhang *et al.* (2004)]. The cross-sectional view of Re-S/D SOI MOSFET is shown in Fig. 1.13 (b). By using the wet etching process two trenches have been created at both edges of thin SOI film to remove the thin Si film and BOX for the formation of source/drain and Re-S/D regions. The formed trenches will be filled with the amorphous silicon to act as the S/D and Re-S/D regions. The filled amorphous silicon is planarised up to the gate oxide region by using the chemical mechanical planarization (CMP) technique. Further, to form the p^+ S/D and p^+ Re-S/D regions, the amorphous silicon regions have been heavily doped with the arsenic material. Finally, the back-end steps like contact hole etching, metal deposition, and metal patterning steps are performed to complete the process.

In case of Re-S/D SOI MOSFET, the capacitance coupling between the gate and source/drain regions are almost eliminated. Further, Re-S/D SOI MOSFETs are free from

current crowding effect [Thean *et al. (*2006)]. Moreover, unlike an E-S/D SOI MOSFET, the Re-S/D SOI MOSFET is a planar structure. Thus, the Re-S/D SOI MOSFET seems to be an excellent device structure which is compatible with planar CMOS process technology.



(a) (b)

Fig. 1.13: Schematic cross-sections of UTB SOI MOSFETs with (a) recessed source/drain (Re-S/D) structure and (b) elevated source/drain (E-S/D) structure

1.6 Dissertation Motivation

In the era of sub-100nm device dimensions, continuing conventional MOSFET scaling and keeping up with the ITRS roadmap are proved to be more difficult than ever. This is attributed to the severe SCEs in the shrinking nanometer order. In the conventional MOSFET, as the channel length diminishes, the gate control over the channel gets reduced due to the increased source/drain capacitances. Various alternative MOS structures have been pursued in order to further continue the scaling. Among all of them, SOI MOSFET is one of the alternative CMOS devices that can be scaled more aggressively than the bulk silicon MOSFET. The device offers diminished SCEs, smaller subthreshold swing, smaller mobility degradation and higher on-to-off current ratio compared to the conventional MOS devices [Colinge (2004), Kumar *et al.* (2008)]. Being three-dimensional structures, multi-gate FETs (MuGFETs) have several technological problems such as fabrication complexity, corner effect and fabrication of thin silicon (fin) etc. Hence, a planar fully-depleted (FD)

SOI MOSFETs could be the best option as the device offers almost equivalent on-off current ratio.

An ultra-thin-body (UTB) is used in FD SOI MOSFETs in order to improve the short-channel effects immunity. However, the UTB gives rise to a large series resistance and contact formation problems which lead to the poor current drive capability of the device despite having excellent short-channel characteristics. Since, an UTB is required to diminish the SCEs, the source/drain area may be increased by extending S/D either upward or downward. Thus, two schemes discussed in the last section can be employed in FD SOI MOSFETs to counter the large series resistance and contact problem by elevating or recessing source/drain regions. By keeping in mind the issues associated with E-S/D SOI MOSFETs, the Re-S/D SOI MOSFETs have been pursued rigorously to address the large series resistance problem.

Recessing source and drain deeper into buried oxide ensures high drive current and avoid the contact formation problem. However, the recessed source and drain may deteriorate the subthreshold characteristics, including threshold voltage, subthreshold current and subthreshold swing of the transistor owing to a strong coupling between the recessed source/drain and the back surface of the channel. It may happen that the strong coupling between recessed source/drain and back of the channel activates the channel at the back surface before the gate voltage does the same on the front-surface. If it happens, the device will show an anomalous subthreshold behavior.

In light of above-mentioned facts, an attempt has been made to analyze the subthreshold behavior of Re-S/D SOI MOSFETs. Theoretical models of the threshold voltage, subthreshold current and subthreshold swing have been developed for Re-S/D SOI MOSFETs. The impact of various device parameters on the subthreshold characteristics of Re-S/D SOI MOSFETs has been analyzed through the developed theoretical models.

Further, CMOS performance boosters such as high-*k* dielectric, multi-gate and back-gate etc. help to improve the on-current of FD Re-S/D SOI MOSFETs. Therefore, these performance boosters have been employed in the Re-S/D SOI MOSFETs in order to investigate their impact on the subthreshold characteristics of the device.

1.7 Scope of Dissertation

The main objective of this dissertation is to present a detailed modeling & simulation - based study of the subthreshold characteristics of short-channel fully-depleted (FD) recessed-source/drain (Re-S/D) SOI MOSFETs. The dissertation consists of six chapters, including the present one as Chapter 1. The contents of the remaining chapters of the dissertation are outlined as follows:

Chapter 2 presents a detailed review of the modeling and simulation of SOI MOSFETs in detail and Re-S/D SOI MOSFET in particular. The state-of-the-art works reported on the threshold voltage, subthreshold swing and subthreshold current of Re-S/D SOI MOSFETs have been discussed in this chapter. Finally, some major observations from the literature have been summarized at the end of the chapter to justify the motivations behind the research works carried out in the following three chapters of the present dissertation.

Chapter 3 includes the analytical modeling and simulation of the threshold voltage, subthreshold current and subthreshold swing of short-channel dual-metal-gate (DMG) recessed-source/drain (Re-S/D) SOI MOSFETs. The formulated models are derived considering the appropriate physics of the device operation. The model results are analyzed with wide variations in the device parameters. The validity of the present models is confirmed by comparing the model results with the numerical simulation results.

Chapter 4 presents the analytical modeling and simulation of the threshold voltage, subthreshold current and subthreshold swing of Re-S/D SOI MOSFETs with the high-*k* dielectric material. The two-dimensional (2D) Poisson's equation is solved in the channel region in order to obtain the surface potential under the assumption of the parabolic potential profile in the transverse direction of the channel with appropriate boundary conditions. Subsequently, threshold voltage, subthreshold current and subthreshold swing models are presented by considering the influence of the fringing field in terms of bottom plate capacitance C_{bot} which is formed between bottom edge of the gate electrode and the source/drain regions. Following which, all the developed models are tested by

varying the different device parameters. Model results are also compared with the 2D numerical simulation results in order to show their validity.

Chapter 5 presents the analytical modeling of subthreshold characteristics of Re-S/D SOI MOSFETs with back-gate control. The impact of back-gate on the subthreshold characteristics of Re-S/D SOI MOSFETs has been analyzed in detail. Again, to confirm the validity of presented models, 2D numerical simulations are carried out.

Chapter 6 includes the summary and conclusions of the present dissertation. The major findings of the entire dissertation have been summarized in this chapter. In addition, suggestions to future the work in this thesis is presented at the end of this chapter.

Chapter 2

SOI MOSFETs: A General Review

2.1 Introduction

MOSFET miniaturization has enabled amazing improvement in the switching speed [Critchlow (2007)], density [Taur *et al.* (1998)], functionality [Iwai (2009)] and cost of microprocessors [Cavin *et al.* (2012)]. However, the problems associated with miniaturization of the conventional MOS transistors have increased with the increasing transistor density in integrated circuits (ICs) [Ieong *et al.* (2006)]. The CMOS performance boosters, which were discussed in Chapter 1, are very useful in order to counter the problems associated with miniaturization [Takagi (2007), Yang *et al.* (2006), Chaudhry *et al.* (2004), Kumar *et al.* (2004), Bangsaruntip *et al.* (2009), Kuhn (2012), Amlan *et al.* (2009)]. In Chapter 1, it was also discussed that the Fully depleted (FD) silicon-on-insulator (SOI) MOSFET is one of the potential CMOS devices that can be scaled down to a greater extent compared to the bulk silicon MOSFET because of their outstanding short-channel effects (SCEs) controlling capability [Taur *et al.* (1997), Colinge (2008)]. However, owing to the ultra-thin source and drain regions, FD SOI MOSFETs exhibit large series resistance problem which results in the diminished current drive capability of the device despite possessing excellent short-channel characteristics [Chaudhry *et al.* (2004)]. In order to reduce the effect of this large series resistance problem, Zhang *et al.* [Zhang *et al.* (2004)] proposed and fabricated a recessed-source/drain (Re-S/D) ultra-thin body (UTB) SOI MOSFET. In the Re-S/D UTB SOI MOSFETs, source and drain regions are extended deeper into the buried oxide (BOX) to mitigate the effects of large source and drain resistances.

The objective of this dissertation is to perform the modeling and simulation of the subthreshold characteristics of some SOI MOSFET structures. Since, the future trends in research, in any area can only be predicted by having a thorough knowledge of the state-of-the-art research in that particular field of interest, the present chapter is dedicated to discuss a detailed review of the state-of-the-art-work on various aspects of SOI MOSFETs in general, and recessed-source/drain SOI MOSFETs in particular, in order to validate the scope of the dissertation outlined in the previous chapter.

The layout of the chapter is as follows. Sections 2.2 and 2.3 include the review of FD SOI MOSFETs. Some state-of-the-art works on the modeling and simulation of the subthreshold characteristics of SOI MOSFETs have been briefly discussed in section 2.4. Finally, some major findings of the literature review have been summarized in section 2.5.

2.2 SOI MOSFETs

Fully depleted (FD) SOI MOSFETs beat the conventional MOSFETs in various aspects like ability to operate in critical environment such as high temperature [Francis *et al.* (1992)], SCEs immunity [Colinge *et al.* (2004)], high drive current capability [Chaudhry *et al.* (2004)], as well as low parasitic capacitances and leakage currents [Markov *et al.* (2012)]. In addition, the SCEs in a FD SOI MOSFET can be suppressed by using a thinner silicon body and BOX [Ghanatian *et al.* (2009)]. Further, the FD SOI MOSFET with a BOX thickness of less than 5nm may be treated as a double-gate device structure on SOI substrate [Ghanatian *et al.* (2009)]. In contrast to BOX thickness scaling, the silicon film thickness scaling is more feasible from a technology point of view [Trivedi *et al.* (2005)], which generates a great deal of interest in ultra-thin body FD SOI MOSFETs.

However, as the film thickness decreases, the source/drain resistance increases and can attain significantly high value to degrade circuit speed performance [Chaudhry *et al.* (2004)]. The source/drain resistance of the device can be pulled down by various techniques such as silicidation of source/drain, tungsten clad, schottky source/drain,

elevated-source/drain (E-S/D), and recessed-source/drain (Re-S/D) etc. [Chen *et al.* (2007), Zan *et al.* (2003), Ieong *et al.* (1998), Wong *et al.* (1984), Zhang *et al.* (2004)].

2.2.1 Source and Drain Silicides

Formation of a low-resistance silicide layer on the source/drain is one of the common techniques to reduce source and drain resistance of the device [Chen *et al.* (2007)]. For this low-barrier silicide formation, firstly, metal is deposited on a silicon substrate and then it is energized by thermal heating or laser irradiation or ion beam mixing. The metal reacts with silicon at the interface, leaving a silicide there. This process is depicted in Fig. 2.1 [Chen *et al.* (2007)]. The commonly used silicides are titanium silicide ($TiSi_2$), cobalt silicide ($CoSi_2$), platinum silicide (PtSi) and nickel silicide (NiSi). Schematic view of an SOI MOSFET with low-barrier silicide layer above the source and drain regions is shown in Fig. 2.2 [Colinge *et al.* (2004)].

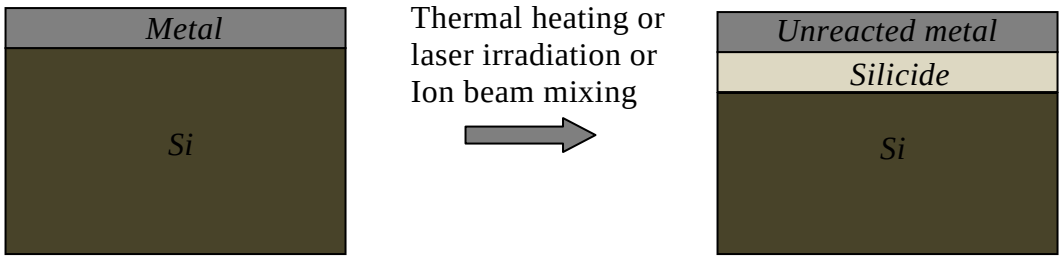


Fig. 2.1: Silicide formation

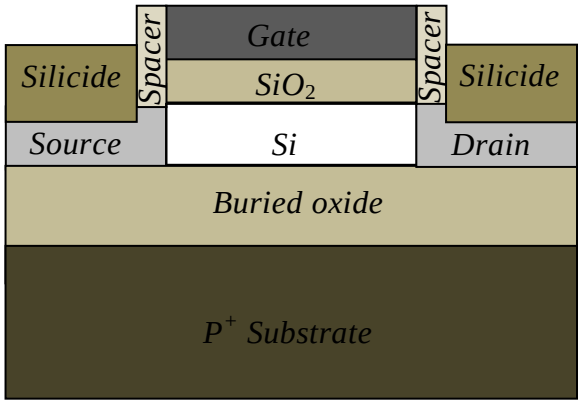


Fig. 2.2: Schematic view of an SOI MOSFET with silicide layer above the source and drain regions

Deng *et al.* [Deng *et al.* (1997)] calculated the source/drain sheet resistance (R_s) against the thickness of the deposited titanium. They observed that the sheet resistance decreased from 300 Ω/square to 2 Ω/square with the increase in titanium thickness from 0nm to 45nm respectively. But, silicon possesses a tendency to diffuse into a titanium silicide. Hence, the silicon in the source/drain and channel region starts diffusing into silicides forming Kirkendall voids [Tu *et al.* (2005)] under the gate edges. This may lead to failure of the device. Therefore, the thinner silicide layer, which gives rise to comparatively lower resistance than the conventional SOI MOSFET, is used in practice.

2.2.2 Tungsten Clad

For the first time, the ultra-thin-channel poly-silicon thin-film transistor (TFT) with tungsten-clad source/drain (W-TFT) was proposed by Zan *et al.* [Zan *et al.* (2003)] to reduce S/D resistance by selective tungsten chemical vapor deposition (SWCVD) technology. SWCVD is one of the best ways to reduce source/drain resistance because of its small silicon consumption. The schematic cross-sectional view of W-TFT is shown in Fig. 2.3 [Zan *et al.* (2003)]. The W-deposition on silicon film can be done by CVD (chemical vapor deposition) process, where SiH_4 chemically reduces WF_6 to W at 250^0C followed by a rapid thermal annealing at 550^0C temperature. Zan *et al.* [Zan *et al.* (2003)] also compared the output characteristics of conventional TFT and W-TFT and they reported that the output characteristics of W-TFTs are better than those of the conventional TFTs.

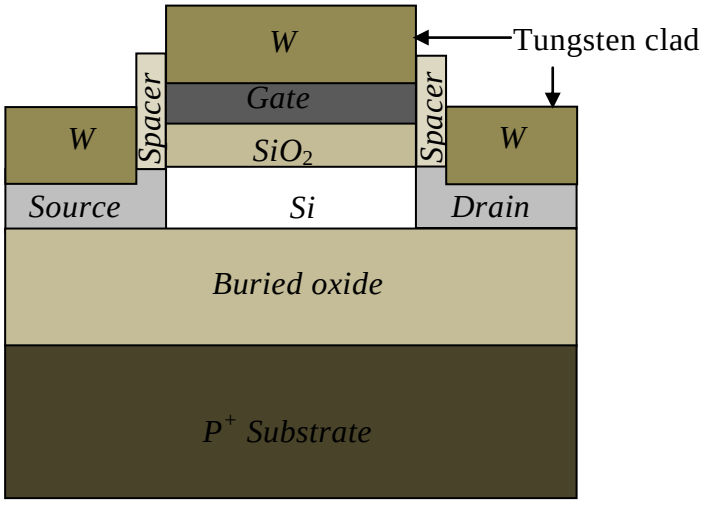


Fig. 2.3: Schematic cross-sectional view of the W-TFT. [Zan *et al.* (2003)]

2.2.3 Schottky Source and Drain

The source/drain resistance can be decreased as well by using Schottky source and drain [Ieong *et al.* (1998)]. The Schottky source/drain gives rise to lower sheet resistance, but leads to a higher contact resistance because of its finite Schottky barrier height. Hence, a material with lower barrier height must be used as a contact in order to reduce contact resistance [Ieong *et al.* (1998)]. It had been reported that in short-channel devices, if a very small or negative Schottky barriers developed, then both the source/drain resistance and contact resistance were significantly reduced [Larson *et al.* (2006)]. For a p-channel and n-channel devices, platinum silicide (PtSi) and **e**rbium silicide ($ErSi_{1.7}$) have been used for Schottky junction respectively [Ieong *et al.* (1998)]. Ieong *et al.* [Ieong *et al.* (1998)] analyzed I-V characteristics of a Schottky source/drain MOSFET for various Schottky barrier heights and observed that the drive current severely degrades with higher Schottky barrier height, but increases substantially with a decrease in barrier height due to decreased contact resistance.

2.2.4 Elevated source and drain (E-S/D) regions

An elevated source and drain regions can also cut down the series resistance of a MOS device. In this, an ultra-thin Si film is used in the channel region along with a thicker Si film for source and drain regions as shown in Fig. 1.13 (a) of Chapter 1 [Wong *et al.* (1984)]. This can be done in either of the two ways, i.e. (1) by adopting elevated source and drain technique [Colinge (2004)], or (2) by adopting the local oxidation of silicon (LOCOS) technique [Colinge (2004)]. In the former approach, firstly an ultra-thin Si film is used and then, a selective epitaxial growth (SEG) is carried out to increase the thickness of source/drain regions [Colinge (2004)]. In the latter approach, a thicker Si film is used first and then, the channel region is thinned using a LOCOS technique [Colinge (2004)].

2.2.5 Recessed-Source/Drain (Re-S/D)

Recessing of source and drain regions diminishes the large series resistance of a MOS device [Zhang *et al.* (2004)]. The cross-sectional view and fabrication process of the

Re-S/D SOI MOSFET have already been presented in section 1.5.4 of Chapter 1. Zhang *et al.* [Zhang *et al.* (2004)] designed and fabricated a self-aligned Re-S/D UTB SOI MOSFET. The comparison of series resistances/parasitic capacitances of E-S/D and Re-S/D structures were presented by Zhang *et al.* (2004). It was found that the E-S/D structure offers an extra parasitic capacitance which is called as a gate to source/drain Miller capacitance. However, increasing the spacer thickness between the gate and the E-S/D can reduce the gate to S/D Miller capacitance, but it also increases the series resistance. Hence, in case of an E-S/D structure, a compromise among series resistance or Miller capacitance is inevitable [Zhang *et al.* (2004)]. Further, in case of Re-S/D structure, there is no spacer adjacent to the gate as in the E-S/D MOSFET, therefore, a fall of 25% miller capacitance is attained in Re-S/D structure [Zhang *et al.* (2004)]. Furthermore, E-S/D regions are also affected by current crowding effects and planarity which were discussed in section 1.5.3 of Chapter 1.

2.3 Earlier Works Related to SOI MOSFETs

The first SOI transistor was fabricated by Mueller *et al.* in the year 1964 [Mueller *et al.* (1964)]. Most of the early SOI MOSFETs were fabricated with SOS (silicon-on-sapphire) wafer technology. SOI technology was advocated enormously by J. P. Colinge in 1980's [Colinge (1991)]. Introducing a BOX in conventional MOS structure delivers a lot of improved characteristic such as excellent isolation [Colinge (1996)], less leakage current [Markov *et al.* (2012)], enhanced SCEs immunity [Colinge (2004)], improved latch-up free condition [Narayanan *et al.* (2013)], enhanced switching speed due to less drain-body capacitance [Markov *et al.* (2012)] and radiation hardness [Chan *et al.* (1994)]. The SOI CMOS technology emerged as an alternative to planar CMOS technology for deep sub-micron CMOS. It appeared to be one of the best options for low-power electronics [Colinge (2004)]. SOI MOSFETs attracted a number of researchers [Colinge (1986), Young *et al.* (1989), Yan *et al.* (1991), Joachim *et al.* (1993), Yan *et al.* (1992), Wong *et al.* (1998), Kumar *et al.* (2005), Reddy *et al.* (2005), Pal *et al.* (2014), Mohapatra *et al.* (2003), Kumar *et al.* (2007), Lu *et al.* (2011), Zhang *et al.* (2004), Ke *et al.* (2007), Svilicic *et al.* (2009)] due to their several advantages over conventional MOSFETs.

In 1986, J. P. Colinge [Colinge (1986)] presented a subthreshold slope model of thin-film SOI MOSFETs. One-dimensional (1D) Poisson's equation was solved in the channel region using the suitable boundary conditions to model the electrostatic behavior of SOI MOSFETs. A subthreshold slope of 62 mV/decade, which is almost equivalent to the ideal subthreshold slope of 60 mV/decade, was observed in a long-channel undoped FD SOI device [Colinge (1986)]. However, the near-ideal subthreshold slope cannot be obtained in short-channel FD SOI MOSFETs with thick BOX due to the lateral field coupling into the channel through the BOX [Colinge (1986)].

Young [Young (1989)] derived a two-dimensional (2D) potential distribution equation of FD SOI MOSFETs in the silicon thin film by assuming a simple parabolic function perpendicular to the channel region. It was found that the vertical field through the depleted film strongly influences the lateral field across the source and drain regions. It was obsereved that the SCEs were found to be decreased with decreasing silicon film thickness. [Young (1989)]. In the early 90's, R. H. Yan [Yan *et al.* (1991)] also derived a 2D channel potential for SOI MOSFETs following K.K. Young's approach [Young *et al.* (1989)]. However, both Young and Yan assumed the electric field inside the thick BOX to be zero in order to simplify the problem. Therefore, these models did not show BOX thickness dependency [Joachim *et al.* (1993)]. Joachim *et al.* [Joachim *et al.* (1993)], however, specified that 2D effects in the BOX region could not be neglected for short-channel devices [Joachim *et al.* (1993)]. Joachim *et al.* [Joachim *et al.* (1993)] modified the boundary condition at the bottom of the SOI layer to account for the nonlinear potential distribution inside the BOX. They [Joachim *et al.* (1993)] found that in a FD SOI MOSFET, the subthreshold slope is improved by increasing the channel doping concentration.

Yan *et al.* [Yan *et al.* (1992)], in year 1992, introduced natural length scale (λ) as a scaling parameter for several SOI devices such as (a) conventional, (b) gate-all-around, and (c) ground plane, which are shown in Fig. 2.4. It was mentioned that in a deep-submicrometer regime, to achieve better subthreshold leakage control, heavily doped devices were essential, but high channel doping leads to undesirable large junction

capacitance and degraded mobility. Hence, Yan *et al.* [Yan *et al.* (1992)] rigorously studied about the scaling of FD SOI devices and found that the horizontal leakage due to short-channel effects could be very less in non-planar structures. It was observed that the gate length of the device needed to be lengthier than λ for obtaining better subthreshold characteristics [Yan *et al.* (1992)]. The minimum scalable channel length of a FD SOI device could be simply projected by its scale length [Yan *et al.* (1992)]. Yan *et al.* [Yan *et al.* (1992)] reported that the minimum channel length of gate-all-around could be scaled by 30% shorter than the conventional SOI MOSFET with good subthreshold characteristics. It was also reported that the ground-plane structure shows an improvement in λ about 75% over the conventional SOI and a 20% over the gate-all-around structure respectively.

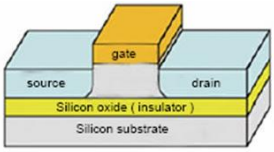
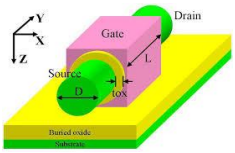
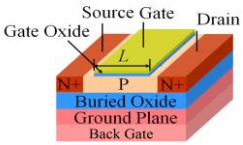
Structure	**Conventional**	**Gate-All-Around**	**Ground Plane**
Schematic			
Scaling	$\lambda = \frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{Si} t_{ox}$	$\lambda = \frac{\varepsilon_{Si}}{2\varepsilon_{ox}} t_{Si} t_{ox}$	$\lambda = \frac{\varepsilon_{Si}}{2\varepsilon_{ox}} \frac{t_{Si} t_{ox}}{\left[1 + \frac{\varepsilon_{Si} t_{ox}}{\varepsilon_{ox} t_{Si}}\right]}$

Fig. 2.4: Various SOI structures: (a) conventional (b) gate-all-around (c) ground plane. **[**Yan *et al.* (1992), Sasaki *et al.* (2015), Chena *et al.* (2016)**]**

Wong *et al.* [Wong *et al.* (1998)] investigated the severity of SCEs in 25nm FD SOI, ground-plane and double-gate (DG) MOSFETs based on 2D simulations. It was observed that the FD SOI MOSFET does not provide adequate short-channel immunity for 25 nm channel length devices even though the channel potential control was increased. Further, in ground-plane MOSFETs, bottom gate insulator must be kept thin to allow effective tuning of the threshold voltage by a bottom gate voltage not exceeding the power supply voltage. However, the thickness of back-gate insulator was considered to be 1.5 times than that of top gate insulator thickness. The design space for the oxide thickness (t_{ox}) and the channel thickness (t_{Si}) were also studied [Wong *et al.*

(1998)]. The obtained models were validated with the simulation results which were obtained from the device simulators FIELDAY program from IBM [Wong *et al.* (1998)].

Kranti *et al.* [Kranti *et al.* (2010)] investigated the analog/radio-frequency (RF) performance of sub-100nm SOI MOSFETs with gate-source/drain underlap channel for low voltage applications. It was reported that the use of underlap source/drain architecture over conventional one enhances the analog/RF performance. [Kranti *et al.* (2010)]. It was, further, claimed that the underlap channel design possesses high voltage gain up to 30 dB and cutoff frequency up to 100 GHz.

Patil *et al.* [Patil *et al.* (2013)] proposed the asymmetric source/drain (ASD) underlap channel dopant-segregated schottky barrier (DSSB) SOI MOSFET and compared the performance with the same of the symmetric S/D (SSD) overlap and underlap structures. The fabrication steps of the ASD underlap structure were also specified in detail [Patil *et al.* (2013)]. The RF figures-of-merits (FoMs) of the considered structures were extracted using H and Y parameters found by carrying out the small-signal AC analysis [Patil *et al.* (2013)]. It was reported that ASD underlap structure (where the source side and drain side were considered to be overlapped and underlapped, respectively) reduced the gate-induced-drain-leakage (GIDL) and improved the analog figures of merit such as transconductance (g_m) and cutoff frequency (f_T) [Patil *et al.* (2013)]. Further, the optimization study revealed that the mixed-signal circuit performance of the ASD underlap device, however, degraded significantly beyond certain underlap length at drain side [Patil *et al.* (2013)].

In 1999, Long *et al.* [Long *et al.* (1999)] proposed a novel structure named as dual-material gate (DMG) FET, where the two gate materials were cascaded such that the source side gate metal (M_1) had a relatively higher work function than the drain side metal (M_2). The DMG structure provides the benefits of high electron velocity and enhanced source side electric field resulting in increased carrier transport efficiency in the channel region [Long *et al.* (1999)]. Long *et al.* [Long *et al.* (1999)] observed a step-like channel potential profile which ensured screening of the minimum potential

point from drain voltage fluctuations. Hence, the metal gate M_2 behaves as the screen gate and the metal M_1 behaved as the control gate.

In 2005, for the first time, Reddy *et al.* [Reddy *et al.* (2005)] developed an analytical threshold voltage model for a double-material double-gate (DMDG) SOI MOSFET. The front-gate and back-gate surface potentials of the DG and DMDG SOI MOSFETs were compared along the channel region [Reddy *et al.* (2005)]. It was observed that the DMDG SOI MOSFET illustrated a step-like profile in the surface potential at both the surfaces [Reddy *et al.* (2005)]. It was reported that in case of an asymmetrical DG SOI MOSFET the surface potential at the back-gate dominates in determining the threshold voltage (V_{th}).

Pal *et al.* [Pal *et al.* (2014)] recently developed an analytical threshold voltage model for the dual-material surrounding-gate MOSFET (DMSG). The threshold voltage (V_{th}) variations were compared for DMSG and SG MOSFETs [Pal *et al.* (2014)]. It was observed that the DMSG MOSFETs offer higher efficiency to V_{th} roll-off compared to SG MOSFETs [Pal *et al.* (2014)]. It was reported that in gate-engineered MOSFETs, due to the electric field discontinuities in the channel, the increased drain to source potential is absorbed by the screen gate.

In 2010, the concept of DMG was invoked in strained-silicon-on-insulator (s-SOI) MOSFETs by Jin *et al.* [Jin *et al.* (2010)]. It was analytically demonstrated that the significant improvements in the SCEs such as DIBL, HCEs, and carrier transport efficiency could be obtained in strained-SOI MOSFETs [Jin *et al.* (2010a)](2010)].

By utilizing the concepts of the straddle-gate structure of the MOSFETs [Tiwari *et al.* (1998)] and the electrically induced shallow junction MOSFETs [Han *et al.* (2001)], Goel *et al.* [Goel *et al.* (2006)] presented a new structure called tri-material gate-stack (TRIMAGS) MOSFET in 2006. The gate dielectric of their proposed structure consisted of a gate oxide layer on the substrate, followed by a high-*k* dielectric layer. The polysilicon at the gate-electrode was replaced by laterally connected three different materials with three different work functions placed in such a way that the materials

with the highest and lowest work functions were at the source side and drain side respectively.

Chiang [Chiang *et al.* (2009)] reported a subthreshold current model for a tri-material gate-stack (TRIMAGS) SOI MOSFET using evanescent mode analysis. The two-dimension (2D) Poisson's equation was solved in the channel region using suitable boundary conditions to obtain channel potential which was finally used to derive the subthreshold current model of the device. It was observed that a thin effective stack-gate oxide, a thin silicon body and large $L_1 : L_2$ ratio were required to deliver better subthreshold behavior, where, L_1 and L_2 be the lengths of control and screen gates respectively [Chiang *et al.* (2009)].

As per the device scaling rule [Dennard *et al.* (1985)], an ultra-short-channel length device should have a very thin gate oxide in order to diminish the unwanted short-channel effects. But, through the ultra-thin gate oxide, quantum mechanical tunneling of the charge carrier is inevitable [Basak *et al.* (2015)]. Therefore, the gate dielectric material (SiO_2) should be replaced by a high-*k* gate dielectric material (HfO_2, Ta_2O_5 and ZrO_2) which offers large physical thickness and small electrical thickness [Tripathi *et al.* (2012)]. However, the high-*k* dielectric material induces fringing field lines, which influence the channel electrostatic potential; hence, it is very important to examine the subthreshold characteristics of the device in the presence of the high-*k* dielectric material. Several attempts have been made in the past, to model the capacitance associated with the bottom edge of the gate electrode and the source and drain regions for different CMOS devices [Kumar *et al.* (2007), Mohapatra *et al.* (2003), Liu *et al.* (2002)].

Mohapatra *et al.* [Mohapatra *et al.* (2003)] presented parasitic capacitance models of MOS transistors with high-*k* dielectric material, as shown in Fig. 2.5. It was reported that three types of parasitic capacitances might affect the device: the first one is C_{side}, the sidewall fringing capacitance between gate and source/drain regions (through high-*k*); the second one is C_{pp}, the parallel plate capacitance between gate and source/drain electrodes and the last one is C_{top}, the top fringing capacitance between top surface of

the gate and source/drain electrodes through the first layer of passivation dielectrics [Mohapatra *et al.* (2003)]. Mohapatra *et al.* [Mohapatra *et al.* (2003)] used the developed model to study the dependence of parasitic capacitance on different parameters such as channel length, gate dielectric constant, gate electrode thickness, gate dielectric thickness, and spacer thickness.

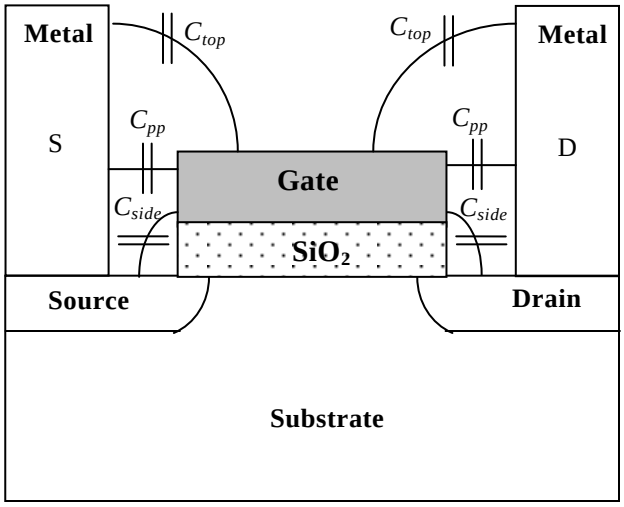


Fig. 2.5: Cross-sectional view of a MOS transistor with various capacitance components [Mohapatra *et al.* (2003)]

Further, Kumar *et al.* [Kumar *et al.* (2006)] presented a parasitic capacitance model for high-*k* gate dielectric SOI MOSFETs by considering the effect of the parasitic internal fringe capacitance allied with the bottom edge of the gate electrode and the source and drain regions. A threshold voltage model including the effect of fringing capacitance was also presented by Kumar *et al.* [Kumar *et al.* (2006)]. It was observed that there is a significant threshold voltage drop because of fringing field lines from the bottom edge of the gate electrode to the source/drain region for high-*k* dielectric. In addition, it was also mentioned that this significant threshold voltage drop might degrade the device characteristics and performance considerably.

Considering the variability problem of threshold voltage owing to the random dopant fluctuation in the doped channel, the back-gate biasing is one of the unique features of MOSFET devices for ultimate tuning of threshold voltage even after the device has been fabricated [Yang *et al.* (2013)]. Hence, one approach to control the threshold voltage

fluctuation is to apply an appropriate back-gate bias voltage with low doped substarte [Yang *et al.* (2013)]. Thus, the threshold voltage of FD SOI MOSFETs can be controlled by three parameters, the gate work function (ϕ_M), the channel doping (N_a), and the back-gate voltage, (V_{BG}) [Numata *et al.* (2004)].

Yang *et al.* [Yang *et al.* (1995)] presented a novel SOI device called FD silicon-on-insulator-with-active substrate (SOIAS) MOSFET structure in which an oxide-isolated polysilicon back-gate electrode was formed beneath the channel and back-gate was used to control the threshold voltage of the device. The fabrication of SOIAS MOSFET using bonded SIMOX and BE (bond and etch-back) -SOI processes was presented in detail [Yang *et al.* (1995)]. It was reported that a dynamic threshold voltage control scheme was needed for high-performance and low-power requirements [Yang *et al.*].

Lu *et al.* [Lu *et al.* (2011)] presented an analytical threshold voltage model for FD SOI MOSFETs in which the front-gate and back-gate were independently biased. Lu *et al.* [Lu *et al.* (2011)] considered the non-ideal effects such as short-channel effects (SCEs), quantum effects, leakage currents, field dependent mobility, and parasitic effects to model the characteristics of a real device. The threshold voltage (V_{th}) versus back-gate voltage (V_{BG}) for both symmetric and asymmetric double-gate (DG) MOSFETs were compared. The derived model was validated with the simulation results which were obtained from the device simulator TCAD.

Ultra-thin-body (UTB) SOI MOSFETs exhibit excellent short-channel characteristics such as low parasitic capacitances and leakage currents; but suffer from poor contacts and source/drain resistances because of ultra-thin source/drain regions [Chaudhry *et al.* (2004)]. As discussed in section 2.2, Re-S/D SOI MOSFETs not only facilitates better contacts but also possesses smaller source/drain resistances. Further, the Re-S/D SOI MOSFET fabrication process steps are almost similar to those of CMOS. Hence, due to the above advantages of Re-S/D SOI MOSFETs, researchers have developed an interest towards it.

Ke *et al.* [Ke *et al.* (2007)] performed a comprehensive study on the Re-S/D UTB SOI MOSFET in detail using a commercial simulator ISE 7.0. The Re-S/D structure offer

significantly reduced source/drain series resistance than the E-S/D structure [Ke *et al.* (2007)]. Further, it was also observed that the E-S/D SOI MOSFETs show degraded SCEs immunity than that of Re-S/D SOI MOSFETs. The design guidelines and design window were also proposed for the Re-S/D SOI MOSFETs by Ke *et al.* [Ke *et al.* (2007)]. It was claimed that the Re-S/D SOI MOSFETs were capable of scaling down to 10nm node [Ke *et al.* (2007)].

Zhang *et al.* [Zhang *et al.* (2004)] presented a drain current characteristic of the Re-S/D SOI MOSFET with a reasonably good on and off current ratio of 3.8×10^{7}. The step by step procedure for the fabrication of UTB Re-S/D SOI MOSFET was given by Zhang *et al.* [Zhang *et al.* (2004)]. Zhang *et al.* [Zhang *et al.* (2004)] compared the performance of E-S/D and Re-S/D SOI structures. It was reported that the UTB Re-S/D SOI MOSFET had many advantages over UTB E-S/D SOI MOSFET, such as lesser source/drain series resistance and reduced Miller capacitance [Zhang *et al.* (2004)].

Svilicic *et al.* [Svilicic *et al.* (2009)] developed an analytical threshold voltage model for Re-S/D SOI MOSFETs. It was pointed out that in case of Re-S/D SOI MOSFET, the front-channel got inverted just like the conventional SOI MOSFET for lower recessed S/D length, but as the recessed source/drain thickness was increased, the source/drain coupling with the back-channel dominated over the gate coupling with the front-channel, which lead to an early inversion in the back-channel [Svilicic *et al.* (2009)]. The back-channel barrier height found to be smaller compared to the front-channel [Svilicic *et al.* (2009)]. Since the back inverted channel remained too far from the front-gate, and also under the control of source and drain, poor subthreshold characteristics of the device were inevitable.

2.4 Subthreshold Characteristic Models of SOI MOSFETs

Moreover, many attempts have also been made to model and investigate the subthreshold characteristics of SOI MOSFETs [Lee *et al.* (1989), Woo *et al.* (1990), Banna *et al.* (1995), Suziki *et al.* (1995), Svilicic *et al.* (2009), Kumar *et al.* (2014), Yeh *et al.* (1995), Yan *et al.* (1992), Kumar *et al.* (2013), Ding *et al.* (2011), Chen *et al.*

(2011), Dey *et al.* (2008)]. Few of these attempts are summarized in forthcoming sections.

2.4.1 Threshold Voltage Models of SOI MOSFETs

The threshold voltage (V_{th}) of a MOSFET is defined as the gate-to-source voltage at which the conduction of current begins. The role of V_{th} has become increasingly important in designing of VLSI circuits and systems targeting low-voltage, low-power, and high-speed applications [Schrom *et al.* (1996), Giustolisi *et al.* (2003)]. A number of attempts have been made to model the threshold voltage of SOI MOSFETs [Lee *et al.* (1989), Woo *et al.* (1990), Banna *et al.* (1995), Suziki *et al.* (1995), Svilicic *et al.* (2009), Kumar *et al.* (2014)].

Lee *et al.* [Lee *et al.* (1989)] presented a numerical study of the threshold voltage of a long-channel lightly doped ultra-thin SOI MOSFET, where Si-film was assumed to be thin enough so that complete depletion of the film could take place at the threshold condition. The results obtained by Lee *et al.* [Lee *et al.* (1989)] were limited only to the conditions at which the back channel was neither accumulated nor inverted enough to cause significant floating body effects or leakage current. It was found that the classical definition of the threshold voltage condition (i.e. $\phi_{sf} = 2\phi_B$, where ϕ_{sf} was the front-surface potential and $\phi_{f_{Si}}$ was the Fermi potential of the film) of the conventional bulk CMOS device could not be considered for SOI MOSFETs [Lee *et al.* (1989)]. Instead, Lee *et al.* [Lee *et al.* (1989)] assumed that the electron concentration of the front-surface must reach a critical value η_T at the threshold condition and accordingly, front-surface potential was approximated as $\phi_{sf} = \phi_{f_{Si}} + \phi_o$ [Lee *et al.* (1989), Chen (2003)] where $\phi_o = \phi_{f_{Si}}$ if $N_a > \eta_T$ or $\phi_o = \frac{kT}{q}\ln\left(\frac{\eta_T}{n_i}\right)$ if $N_a < \eta_T$, $-q$ was the electron charge, N_a was the channel doping concentration, n_i was the intrinsic carrier concentration, k was the Boltzmann's constant, and T was the temperature. Based on the simulation results, Lee *et al.* [Lee *et al.* (1989)] concluded that high-performance sub-micrometer complementary MOSFETs could be achieved by using lightly doped or near-intrinsic

ultra-thin SOI films, gate materials with an appropriate work function, and back-gate biasing of the SOI MOSFET. Further, Balestra *et al.* [Balestra *et al.* (1987)] discovered an important physical phenomenon 'volume-inversion' in DG SOI MOSFETs in the year 1987. Volume inversion is a phenomenon which appears in thin-film multi-gate SOI MOSFETs. As per volume inversion concept, the inversion carriers are not confined near the Si-channel/SiO2 interface, but somewhat at the center of the film [Balestra *et al.* (1987)].

In year 1995, Banna *et al.* [Banna *et al.* (1995)] developed a threshold voltage model for FD SOI MOSFET using a quasi-2D approach in the sub-μm regime. It was observed that the threshold voltage roll-off in FD SOI MOSFET was lesser than that of conventional MOSFET for the same effective channel length. Banna *et al.* [Banna *et al.* (1995)] used experiential fitting parameter 'η' while finding the characteristic length of FD SOI MOSFET. The obtained model was validated with the simulation results which were obtained from MINIMOS5 and found to be in excellent agreement.

Suzuki *et al.* [Suziki *et al.* (2003)] presented an analytical threshold voltage model for FD single-gate SOI MOSFETs by assuming the 2D effects in both silicon film and BOX. This model is valid for both long and short-channel SOI MOSFETs. However, Suzuki *et al.* [Suziki *et al.* (2003)] limited their investigation to the highly doped base substrates only. It was stated that the lightly doped substrates gives negative V_{th} in most cases.

Zhang *et al.* [Zhang *et al.* (2008)] derived an analytical 2D model of the threshold voltage of a FD SOI MOSFET with vertical Gaussian doping profile by considering the 2D effects in both SOI and BOX [Zhang *et al.* (2008)]. Zhang *et al.* [Zhang *et al.* (2008)] limited their analysis with an approximation that the lateral channel doping concentration was assumed uniform and the vertical doping concentration be non-uniform distribution (Guassian profile). The resulted characteristic lengths of the model was in agreement with Suzuki *et al.* [Suziki *et al.* (2003)] uniformly doped FD SOI MOSFETs model, when $\sigma_p << R_p$; where, R_p and σ_p were the projected range and straggle of the Gaussian doping profile.

In the year 2014, our group [Kumar *et al.* (2014)] presented a threshold voltage model of short-channel Re-S/D UTB SOI MOSFETs considering the substrate induced surface potential (SISP) effects. Kumar *et al.* [Kumar *et al.* (2014)] derived the surface potential expression of the front-surface and the back- surface of the channel region using the evanescent mode analysis method. It was observed that the recessed thickness (t_{rsd}) is an important parameter to decide the threshold voltage of the device and the threshold voltage is switched from back surface dominance to the front-surface dominance of the channel as channel doping (N_a) is increased [Kumar *et al.* (2014)].

2.4.2 Subthreshold Current Models of SOI MOSFETs

Since the subthreshold current plays key role in determining the static power dissipation of any MOS device, an accurate subthreshold current model of an SOI MOSFET could be an extreme concern for researchers for the optimization of the power dissipation in short-channel FD SOI MOSFET based VLSI/ULSI circuits [Yeh *et al.* (1995)]. Various attempts have been made to model the subthreshold current of FD SOI MOS devices [Yeh *et al.* (1995), Yan *et al.* (1992), Kumar *et al.* (2013)].

Yeh *et al.* [Yeh *et al.* (1995)] presented a physical subthreshold current model of FD SOI MOSFETs in a sub-micrometer regime considering that the diffusion current is dominant in the subthreshold regime of device operation. The effect of substrate charge (under source/drain regions) was included in the model [Yeh *et al.* (1995)].

Analytical models of the subthreshold current and subthreshold slope of asymmetric three-terminal (3-T) and four-terminal (4-T) DG MOSFETs were presented by Dey *et al.* [Dey *et al.* (2008)] using the evanescent mode analysis method to solve the 2D Poisson's equation in the channel region. Dey *et al.* [Dey *et al.* (2008)] used the models to study the subthreshold characteristics of a DG MOSFET with asymmetry in gate oxide thickness, gate voltage, and gate material work function.

Luan *et al.* [Luan *et al.* (2009)] presented a subthreshold current model of DMG SOI nMOSFETs with a single halo (DMGH) near the source region. The parabolic potential approximation was considered in the channel region and the current of the device was

obtained by utilizing the drift-diffusion theory [Luan *et al.* (2009)]. To obtain a fully analytical model for subthreshold current, a piecewise approximation was employed to the surface potential [Luan *et al.* (2009)].

2.4.3 Subthreshold Swing Models of SOI MOSFETs

Subthreshold swing (S) is one of the important parameters of a device as it determines the switching characteristics. It is defined as the amount of gate voltage required to change the output current by one decade. Since the subthreshold swing has vital implications in device scaling, it is important to develop analytical models to study the subthreshold swing characteristics of the SOI MOSFETs. Various theoretical models for the subthreshold swing of SOI MOSFETs have been reported in the literature [Chen *et al.* (2011), Svilicic *et al.* (2010), Kumar *et al.* (2013)].

Chen *et al.* [Chen *et al.* (2011)] developed an analytical subthreshold swing model for FD SOI MOSFETs with vertical Gaussian-like doping profile in the channel region. It was reported that the subthreshold swing decreases with increasing peak doping concentration [Chen *et al.* (2011)].

In 2010, an analytical subthreshold swing model for a Re-S/D UTB SOI MOSFET was developed by Svilicic *et al.* [Svilicic *et al.* (2010)]. Svilicic *et al.* [Svilicic *et al.* (2010)] used the developed model to analyze the dependence of subthreshold swing on various device parameters, such as channel length, channel thickness, gate material, gate oxide thickness, BOX material, and Re-S/D thickness.

Kumar *et al.* [Kumar *et al.* (2013)] presented a subthreshold swing model of the strained-Si on silicon-germanium-on-insulator (SGOI) MOSFETs for different gate lengths. It was reported that the subthreshold swing increases with the increase in strain (Ge mole fraction (x)). For an increase in the Ge mole fraction from 0 to 30%, the subthreshold swing is found to be increased by 14.73% for 30nm gate length, 2.94% for 50nm gate length and 0.8% for 70nm gate length [Kumar *et al.* (2013)]. The switching characteristics were observed to be degraded with the increased strain and decreased gate length of the device.

2.5 Summary and Conclusion

Based on the literature survey presented in above sections, Chapter 2 can be summarized under some important observations as follows:

- The FD UTB SOI MOSFET can beat the conventional MOSFETs in various aspects like ability to operate in critical environment such as high temperature [Francis *et al.* (1992)], enhanced SCEs immunity [Colinge *et al.* (2004)], high drive current capability [Chaudhry *et al.* (2004)], enhanced effective carrier mobility [Chu *et al.* (2009)], enhanced transconductance [Lim *et al.* (2009)], low parasitic capacitances and leakage currents [Markov *et al.* (2012)], and high scalability [Colinge *et al.* (2004)]. Above mentioned advantages of FD UTB SOI MOSFETs make it suitable for a number of applications like subthreshold logic operation, low-power analog circuits, RF applications, memory applications, systems-on-a-chip (SOC) applications [Trivedi *et al.* (2005)].

- In FD UTB SOI MOSFETs, the ultra-thin source and drain regions offer large series resistance and contact formation problems which lead to the poor current drive capability of the device despite having excellent short-channel characteristics [Chaudhry *et al.* (2004)]. Hence, it was observed from the literature that the large series resistance and contact formation problems could be reduced by implementing various techniques such as silicide source/drain, tungsten clad, schottky source/drain, elevated-source/drain (E-S/D), recessed-source/drain (Re-S/D) etc. [Chen *et al.* (2007), Zan *et al.* (2003), Ieong *et al.* (1998), Wong *et al.* (1984), Zhang *et al.* (2004)]. Among these aforementioned techniques, Re-S/D is the viable option [Zhang *et al.* (2004), Svilicic *et al.* (2009)]. Further, the Re-S/D SOI MOSFETs offer several advantages over the conventional SOI MOSFETs such as (i) higher drive current capability (ii) reduced parasitic resistances (iii) enhanced transconductance (iv) higher scalability [Zhang *et al.* (2004), Cheng *et al.* (2003), Kuchipudi and Mahmoodi (2007)].

- It was observed from the literature that CMOS performance boosters such as dual-metal-gate, high-*k* dielectric, and back-gate etc. help to improve the ‘on’ current

drive capability, reduce the subthreshold leakage current, and reduce the threshold voltage roll-off of FD Re-S/D SOI MOSFETs. Therefore, an investigation is required for subthreshold characteristics of Re-S/D SOI MOSFETs with CMOS performance boosters [Takagi (2007), Yang *et al.* (2006), Chaudhry *et al.* (2004), Kumar *et al.* (2004), Bangsaruntip *et al.* (2009), Kuhn (2012), Amlan *et al.* (2009)].

- Threshold voltage modeling of short-channel Re-S/D SOI MOSFETs has drawn the significant attention of the researchers because of its better scalability features over the conventional CMOS devices [Kumar *et al.* (2014)]. Various models [Kumar *et al.* (2014), Svilicic *et al.* (2009),] have been developed to estimate the SCEs by inspecting the sensitivity of threshold voltage (V_{th}) towards channel length (L), channel thickness (t_{Si}), and oxide thickness (t_{ox}). The impact of performance boosters on threshold voltage characteristics have yet to be investigated on Re-S/D FD SOI MOSFETs.

- Subthreshold current is another important characteristic of a Re-S/D SOI MOSFET as it decides the standby power dissipations and on-off current ratio which is an important parameter for characterizing the switching performance of a device. A number of subthreshold current models for SOI MOSFETs were presented based on surface potential expression [Yeh *et al.* (1995), Yan *et al.* (1992), Kumar *et al.* (2013)]. However, to the best of our knowledge, no subthreshold current models for Re-S/D SOI MOSFETs as well as Re-S/D FD SOI MOSFETs with CMOS performance boosters have been reported yet. Thus, it is very important to analytically analyze the subthreshold current for both the Re-S/D SOI MOSFETs as well as Re-S/D FD SOI MOSFETs with CMOS performance boosters.

- A long-channel SOI MOSFET is an ideal candidate for subthreshold logic circuits targeting ultra-low-power applications, since it provides an ideal value of subthreshold swing, i.e 60 mV/Decade [Yeh *et al.* (1995)]. But with reduced channel lengths, the subthreshold swing of short-channel SOI MOSFET increases

continuously, thereby degrading the switching performance of the device. Thus, it is very important to search for the new techniques for improving the switching performance of the device. Further, various subthreshold swing models for SOI MOSFETs were presented [Chen *et al.* (2011), Dey *et al.* (2008)]. However, only one model is available for Re-S/D SOI MOSFETs [Svilicic *et al.* (2010)]. Hence, there is an ample scope of work in modeling of subthreshold swing for Re-S/D FD SOI MOSFETs with CMOS performance boosters.

- Further, it was observed from the literature that recessing source and drain may deteriorate the subthreshold characteristics including threshold voltage, subthreshold current and subthreshold swing of the structure due to a strong coupling between recessed source/drain and the back surface of the channel. It may happen that the strong coupling between Re-S/D and back of the channel activates the channel at back surface before the gate voltage does the same on the front-surface. If it happens the device will show an anomalous subthreshold behavior. However, CMOS boosters such as multi-gate, high-*k* dielectric, and back-gate etc. are expected to improve the subthreshold behavior of the Re-S/D SOI MOSFETs. Therefore, modeling of subthreshold characteristics of Re-S/D SOI MOSFETs with CMOS boosters becomes requisite.

In brief, there is a lot of opportunity in the modeling and simulation of the subthreshold characteristics of Re-S/D SOI MOSFETs. The scope of the dissertation outlined in Chapter 1 is based on the observations discussed above.

Chapter 3

Analytical Modeling and Simulation of Subthreshold Characteristics of Short-Channel Dual-Metal-Gate Fully-Depleted Recessed-Source/Drain SOI MOSFET

3.1 Introduction

As discussed in Chapters 1 and 2, a dual-metal-gate (DMG) MOS structure can be used for improving both the hot-carrier effects (HCEs) and drain-induced barrier lowering (DIBL) simultaneously [Kumar *et al.* (2004)]. The structure provides the benefits of high electron velocity and enhanced source side electric field resulting in increased carrier transport efficiency in the channel region [Reddy *et al.* (2005)]. The DMG structure creates a step-like channel potential profile which ensures the screening of the minimum potential point from drain voltage fluctuations. It may be noted that the DMG concept has already been implemented in the conventional silicon-on-insulator (SOI) MOSFETs and significant improvements have been observed in terms of enhanced short-channel effects (SCEs) and hot-carrier effects (HCEs) [Kumar *et al.* (2004)]. However, it can be observed from Chapter 2 that no significant work has been reported on the modeling of the subthreshold characteristics of the short-channel DMG Re-S/D SOI MOSFET. Hence, in this chapter, an attempt has been made to evaluate the impact of DMG on subthreshold characteristics of the Re-S/D UTB SOI MOSFET.

The layout of the present chapter is as follows. Section 3.2 describes the modeling of the two-dimensional (2D) surface potential function. Using the results of section 3.2,

the short-channel threshold voltage model of the device is presented in section 3.3. Analytical models for the subthreshold current and subthreshold swing are presented in sections 3.4 and 3.5 respectively. Results and discussion related to the developed models are presented in section 3.6. Finally, the present chapter is concluded in section 3.7.

3.2 Modeling of Two-Dimensional (2D) Surface Potential

A cross-sectional view of a dual-metal-gate (DMG) Re-S/D UTB SOI MOSFET which is used in our modeling and simulation is shown in Fig. 3.1. The entire Si channel is considered to be fully depleted to avoid the floating body effect. The position along the channel length is represented by the x- axis, whereas the channel depth is represented by the y- axis as shown in the Fig. 3.1. Two different metals for control and screen gates with work functions ϕ_{M1} and ϕ_{M2}, respectively, divide the entire channel into two virtual regions which are named as region I and region II. The region I is defined within $0 < x < L_1$ and $0 < y < t_{Si}$ while the region II is within $L_1 < x < L_1 + L_2$ and $0 < y < t_{Si}$; where L_1 and L_2 are lengths of the control gate and screen gate respectively, t_{Si} is silicon channel thickness. Thus, the total channel length is $L = L_1 + L_2$. The potential distributions of regions I and II are taken as $\phi_1(x, y)$ and $\phi_2(x, y)$ respectively. The symbols t_{ox} and t_{box} represent the thicknesses of the gate oxide and the BOX. The source and the drain regions penetrate into the buried oxide by a thickness t_{rsd}, which is also known as the recessed thickness. The symbol d_{box} is the length of the source/drain overlap over the buried-oxide. The channel region is assumed to be lightly doped with a doping concentration of N_a while source and drain regions are considered to be heavily doped with a doping concentration of N_d each. The source/drain to channel junction is assumed to be abrupt. The substrate doping concentration is N_{sub}. The MOSFET is biased by the gate voltage of V_{GS}, drain voltage of V_{DS} and substrate voltage as V_{sub} keeping the source voltage at $V_S = 0$. The notations and parameter values used in modeling and simulation are given in Table 3.1.

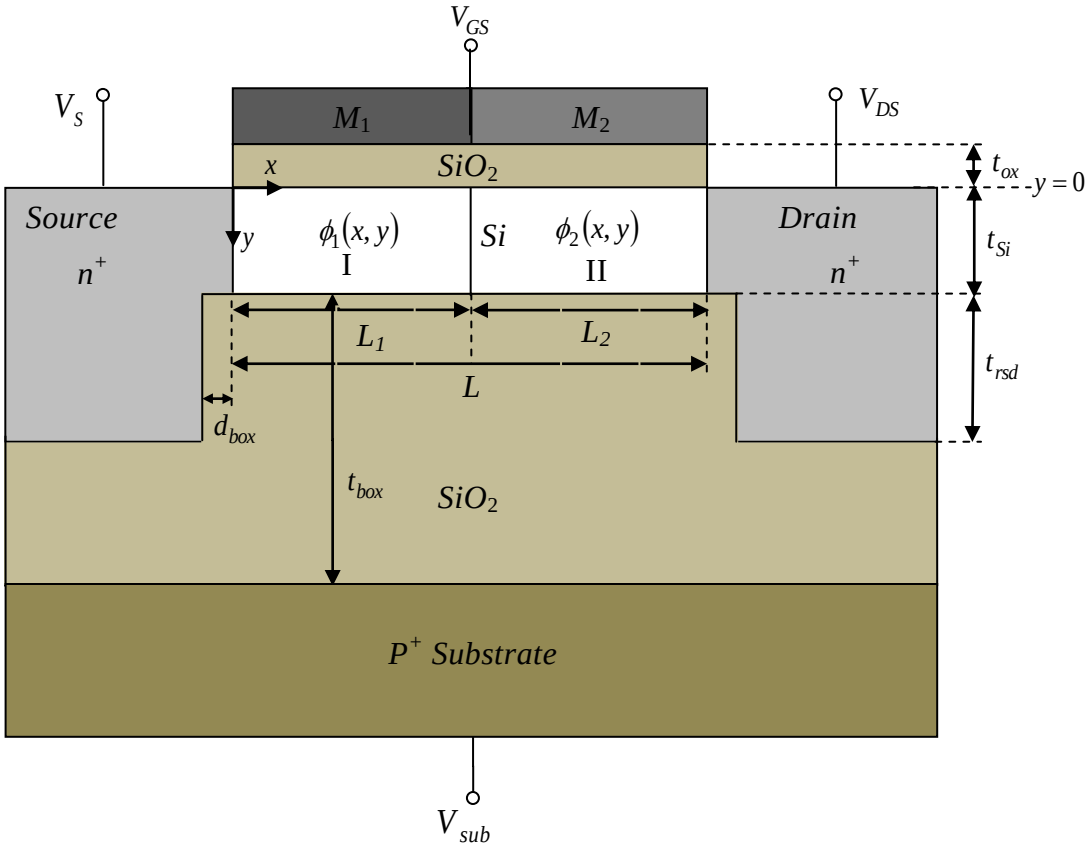


Fig. 3.1: Cross-sectional view of dual-metal-gate (DMG) Re-S/D UTB SOI MOSFET

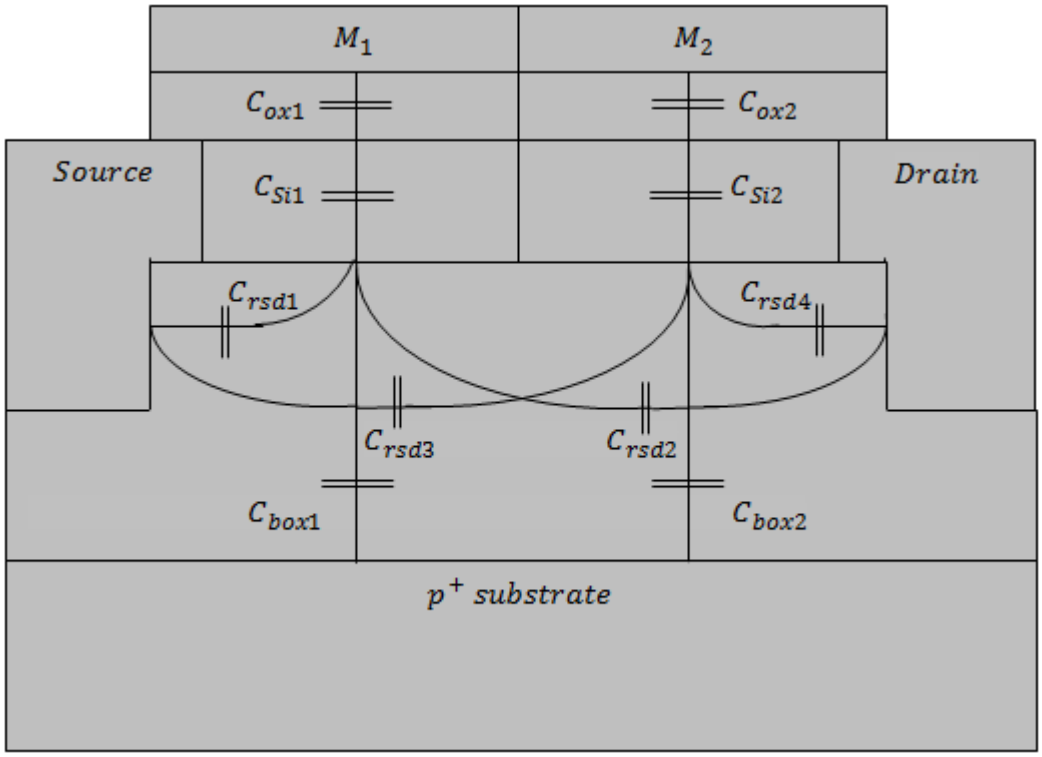


Fig. 3.2: The DMG Re-S/D UTB SOI MOSFET with dominant intrinsic capacitance components

Device Parameters (Notation)	**Value and Units**
Control gate work function, ϕ_{M_1}	4.8eV
Work function of screen gate, ϕ_{M_2}	4.4eV - 4.6eV
Channel doping, N_a	10^{15}cm^{-3}
Source/ drain doping, N_d	10^{20}cm^{-3}
Substrate doping, N_{sub}	10^{18}cm^{-3}
Front-channel oxide thickness, t_{ox}	1.5nm - 3nm
Buried oxide thickness, t_{box}	100nm - 300nm
Silicon thickness, t_{Si}	6nm-10nm
Substrate thickness, t_{sub}	300nm
Length of the source/drain overlap over the buried-oxide, d_{box}	3nm
Control gate to screen gate length ratio, $L_1 : L_2$	1:2, 1:1, 2:1
Channel length, L	30nm - 300nm

Table 3.2: Device parameter values used for modeling and simulation of a DMG Re-S/D UTB SOI MOSFET

The two-dimensional (2D) potential distribution in the channel region of a DMG Re-S/D UTB SOI MOSFET before the onset of strong inversion can be obtained by solving following Poisson's equation [Young *et al.* (1989)]

$$\frac{\partial^2 \phi_i(x,y)}{\partial x^2} + \frac{\partial^2 \phi_i(x,y)}{\partial y^2} = \frac{qN_a}{\varepsilon_{Si}} \quad \text{, where } i = 1, 2 \text{ for region I and II} \tag{3.1}$$

where, N_a, q and ε_{Si} are the doping concentration of channel region, electronic charge and the permittivity of Si film respectively. The 2D electrostatic potential distribution in regions I and II are approximated by following parabolic polynomials [Young *et al.* (1989)]

$$\phi_i(x,y) = \phi_{fi}(x) + C_{i1}(x)y + C_{i2}(x)y^2 \tag{3.2}$$

where, i = 1 stands for region I, and i = 2 for region II, $\phi_{fi}(x)$ be the front-surface potential at SiO_2/Si interface under both metals M_1 and M_2. The coefficients $C_{i1}(x)$ and $C_{i2}(x)$ are the functions of x only and can be determined by using following boundary conditions:

1) The electric flux at SiO_2/Si interface is assumed to be continuous in the device. Therefore, it can be written as [Svilicic *et al.* (2009)]:

$$\left[\frac{\partial \phi_1(x,y)}{\partial y}\right]_{y=0} = \frac{C_{ox1}}{\varepsilon_{Si}} \frac{\phi_{f1}(x) - (V_{GS} - V_{FB1})}{L_1} \tag{3.3}$$

$$\left[\frac{\partial \phi_2(x,y)}{\partial y}\right]_{y=0} = \frac{C_{ox2}}{\varepsilon_{Si}} \frac{\phi_{f2}(x) - (V_{GS} - V_{FB2})}{L_2} \tag{3.4}$$

where, V_{GS} is the applied gate to source voltage. C_{ox1}, C_{ox2} are the front-gate oxide capacitances per unit length under metals M_1 and M_2, respectively and are given by

$$C_{ox1} = \frac{\varepsilon_{ox} L_1}{t_{ox}}, \tag{3.5}$$

$$C_{ox2} = \frac{\varepsilon_{ox} L_2}{t_{ox}} \tag{3.6}$$

where, ε_{ox} is the permittivity of gate oxide material.

V_{FB1} and V_{FB2} are the flat-band voltages for the control and screen gates and are given by

$$V_{FB1} = \phi_{M1} - \phi_{Si} \tag{3.7}$$

$$V_{FB2} = \phi_{M2} - \phi_{Si} \tag{3.8}$$

where, ϕ_{M_1} and ϕ_{M_2} are the metal work functions of the control gate and the screen gate respectively, ϕ_{Si} is the silicon work function given by

$$\phi_{Si} = \frac{\chi_{Si}}{q} + \frac{E_g}{2q} + \phi_{f,Si} \tag{3.9}$$

where, χ_{Si} and E_g are the electron affinity and energy band gap of the silicon respectively, $\phi_{f,Si}$ is the Fermi level potential

$$\phi_{f,Si} = V_T \ln\left(\frac{N_a}{n_i}\right) \tag{3.10}$$

where, n_i is the intrinsic carrier concentration of the silicon.

2) The electric flux at the Si / BOX interface should also be continuous in the device. Therefore, it can be written as [Svilicic *et al.* (2009)]:

$$\left[\frac{\partial \phi_1(x,y)}{\partial y}\right]_{y=t_{Si}} = \frac{C_{rsd1}}{\varepsilon_{Si}}\frac{V_S - V_{FB3} - \phi_{b1}(x)}{L_1} + \frac{C_{rsd2}}{\varepsilon_{Si}}\frac{V_D - V_{FB3} - \phi_{b1}(x)}{L_1} + \frac{C_{box1}}{\varepsilon_{Si}}\frac{V_{sub} - V_{FB4} - \phi_{b1}(x)}{L_1} \tag{3.11}$$

$$\left[\frac{\partial \phi_2(x,y)}{\partial y}\right]_{y=t_{Si}} = \frac{C_{rsd3}}{\varepsilon_{Si}}\frac{V_S - V_{FB3} - \phi_{b2}(x)}{L_2} + \frac{C_{rsd4}}{\varepsilon_{Si}}\frac{V_D - V_{FB3} - \phi_{b2}(x)}{L_2} + \frac{C_{box2}}{\varepsilon_{Si}}\frac{V_{sub} - V_{FB4} - \phi_{b2}(x)}{L_2} \tag{3.12}$$

where, V_S, V_{sub}, and V_D are source voltage, substrate voltage and drain voltage respectively. $\phi_{bi}(x) = \phi_i(x, y = t_{Si})$ is the channel potential at the channel/BOX interface and named as back-surface potential. C_{rsd1}, C_{rsd2}, C_{rsd3} and C_{rsd4} are recessed source/drain- back channel capacitances per unit length as shown in Fig. 3.2 and are given by [Svilicic *et al.* (2009)]

$$C_{rsd1} = \begin{cases} \dfrac{\varepsilon_{ox}}{\frac{\pi}{2} + \frac{\pi}{2}\sec h\left(\frac{t_{rsd}}{d_{box}}\right)} \ln\left(1 + \dfrac{L_1}{d_{box}}\right), & \text{for } L_1 < t_{rsd} \\ \dfrac{\varepsilon_{ox}}{\frac{\pi}{2} + \frac{\pi}{2}\sec h\left(\frac{t_{rsd}}{d_{box}}\right)} \ln\left(1 + \dfrac{t_{rsd}}{d_{box}}\right), & \text{for } L_1 > t_{rsd} \text{ or } t_{rsd} = 0 \end{cases} \tag{3.13}$$

$$C_{rsd2} = \begin{cases} \dfrac{\varepsilon_{ox}}{\frac{\pi}{2} + \frac{\pi}{2}\sec h\left(\frac{t_{rsd}}{(d_{box} + L_2)}\right)} \ln\left(1 + \dfrac{L_1}{(d_{box} + L_2)}\right), & \text{for } L_1 < t_{rsd} \\ \dfrac{\varepsilon_{ox}}{\frac{\pi}{2} + \frac{\pi}{2}\sec h\left(\frac{t_{rsd}}{(d_{box} + L_2)}\right)} \ln\left(1 + \dfrac{t_{rsd}}{(d_{box} + L_2)}\right), & \text{for } L_1 > t_{rsd} \text{ or } t_{rsd} = 0 \end{cases} \tag{3.14}$$

$$C_{rsd3}=\begin{cases}\dfrac{\varepsilon_{ox}}{\dfrac{\pi}{2}+\dfrac{\pi}{2}\sec h\left(\dfrac{t_{rsd}}{(d_{box}+L_1)}\right)}\ln\left(1+\dfrac{L_2}{(d_{box}+L_1)}\right), \text{for } L_2<t_{rsd}\\ \dfrac{\varepsilon_{ox}}{\dfrac{\pi}{2}+\dfrac{\pi}{2}\sec h\left(\dfrac{t_{rsd}}{(d_{box}+L_1)}\right)}\ln\left(1+\dfrac{t_{rsd}}{(d_{box}+L_1)}\right), \text{for } L_2>t_{rsd} \text{ or } t_{rsd}=0\end{cases} \tag{3.15}$$

$$C_{rsd4}=\begin{cases}\dfrac{\varepsilon_{ox}}{\dfrac{\pi}{2}+\dfrac{\pi}{2}\sec h\left(\dfrac{t_{rsd}}{(d_{box})}\right)}\ln\left(1+\dfrac{L_2}{d_{box}}\right), \text{for } L_2<t_{rsd}\\ \dfrac{\varepsilon_{ox}}{\dfrac{\pi}{2}+\dfrac{\pi}{2}\sec h\left(\dfrac{t_{rsd}}{(d_{box})}\right)}\ln\left(1+\dfrac{t_{rsd}}{d_{box}}\right), \text{for } L_2>t_{rsd} \text{ or } t_{rsd}=0\end{cases} \tag{3.16}$$

C_{box1} and C_{box2} are the buried oxide capacitances per unit length in the regions which are under the influence of metals M_1 and M_2, respectively and are given by

$$C_{box1}=\frac{\varepsilon_{ox}L_1}{t_{box}} \tag{3.17}$$

$$C_{box2}=\frac{\varepsilon_{ox}L_2}{t_{box}} \tag{3.18}$$

C_{Si1} and C_{Si2} are the channel capacitances per unit length under metals M_1 and M_2, respectively given as

$$C_{Si1}=\frac{\varepsilon_{Si}L_1}{t_{Si}} \tag{3.19}$$

$$C_{Si2}=\frac{\varepsilon_{Si}L_2}{t_{Si}} \tag{3.20}$$

C_{ox1} and C_{ox2} are the front-gate oxide capacitances per unit length in the regions under the metals M_1 and M_2, respectively given by

$$C_{box1}=\frac{\varepsilon_{ox}L_1}{t_{box}} \tag{3.21}$$

$$C_{box2} = \frac{\varepsilon_{ox} L_2}{t_{box}} \tag{3.22}$$

V_{FB3} and V_{FB4} are the source/drain-back channel flat-band voltage and substrate back channel flat-band voltage, respectively and are given by

$$V_{FB3} = \frac{kT}{q} ln\left(\frac{N_a N_d}{n_i^2}\right) \tag{3.23}$$

$$V_{FB4} = \frac{kT}{q} ln\left(\frac{N_{sub}}{N_a}\right) \tag{3.24}$$

where, N_a, N_d and N_{sub} are the channel, source/drain and substrate doping concentration respectively.

3) The potential at the source end is

$$\phi_1(0, y) = V_{bi} \tag{3.25}$$

where, $V_{bi} = \frac{kT}{q} ln\left(\frac{N_a N_d}{n_i^2}\right)$ is the built in potential across the source/drain and Si junction.

4) The potential at the drain end is

$$\phi_2(L, y) = V_{bi} + V_{DS} \tag{3.26}$$

where, V_{DS} is the applied source/drain bias voltage.

The coefficients $C_{11}(x), C_{12}(x)$, $C_{21}(x)$ and $C_{22}(x)$ of Eq. (3.2) are obtained by utilizing boundary conditions of Eqs. (3.3), (3.4), (3.11) and (3.12) in Eq. (3.2) and can be written as

$$C_{11}(x) = \frac{C_{ox1}}{C_{Si1} t_{Si}} \left(\phi_{f1}(x) - \left(V_{GS} - V_{FB1}\right)\right) \tag{3.27}$$

$$\begin{aligned} C_{12}(x) = {} & \frac{C_{rsd1} + C_{rsd2}}{2 C_{Si1} t_{Si}^{\,2}} \left(V_{DS} - 2V_{FB3} - 2\phi_{b1}(x)\right) \\ & + \frac{C_{box1}}{C_{Si1} t_{Si}^{\,2}} \left(V_{sub} - 2V_{FB4} - \phi_{b1}(x)\right) - \frac{C_{ox1}}{C_{Si1} t_{Si}^{\,2}} \left(\phi_{f1}(x) - \left(V_{GS} - V_{FB1}\right)\right) \end{aligned} \tag{3.28}$$

$$C_{21}(x)=\frac{C_{ox2}}{C_{Si2}t_{Si}}\left(\phi_{f2}(x)-\left(V_{GS}-V_{FB2}\right)\right) \tag{3.29}$$

$$\begin{aligned}C_{22}(x)=&\frac{C_{rsd3}+C_{rsd4}}{2C_{Si2}{t_{Si}}^2}\left(V_{DS}-2V_{FB3}-2\phi_{b2}(x)\right)\\&+\frac{C_{box2}}{{C_{Si2}t_{Si}}^2}\left(V_{sub}-2V_{FB4}-\phi_{b2}(x)\right)-\frac{C_{ox2}}{{C_{Si2}t_{Si}}^2}\left(\phi_{f2}(x)-\left(V_{GS}-V_{FB2}\right)\right)\end{aligned} \tag{3.30}$$

Thus, the expressions for $\phi_1(x,y)$ and $\phi_2(x,y)$ are obtained by substituting the values of $C_{11}(x)$, $C_{12}(x)$, $C_{21}(x)$ and $C_{22}(x)$ into Eq. (3.2). Now, by utilizing Eq. (3.2) in the expressions of $\phi_1(x,y)$ and $\phi_2(x,y)$, potential $\phi_i(x,y)$ can be written in terms of front- and back- surface potential separately as follows

$$\begin{aligned}\phi_1(x,y)=\phi_{f1}(x)&\left[1+\frac{C_{ox1}}{C_{Si1}t_{Si}}y-\frac{C_{ox1}}{{C_{Si1}t_{Si}}^2}y^2-\left(2C_{Si1}+C_{ox1}\right)z_1y^2\right]\\&+\left(V_{GS}-V_{FB1}\right)\left[-\frac{C_{ox1}}{C_{Si1}t_{Si}}y+\frac{C_{ox1}}{2{C_{Si1}t_{Si}}^2}y^2-\left(C_{ox1}\right)z_1y^2\right]\\&+\left(V_{DS}-2V_{FB3}\right)\left[\frac{C_{rsd1}+C_{rsd2}}{2{C_{Si1}t_{Si}}^2}y^2+\left(C_{rsd1}+C_{rsd2}\right)z_1y^2\right]\\&+\left(V_{sub}-V_{FB4}\right)\left[\frac{C_{box1}}{2{C_{Si1}t_{Si}}^2}y^2+\left(C_{box1}\right)z_1y^2\right]\end{aligned} \tag{3.31}$$

where, $z_1=\left(\frac{2\left(C_{rsd1}+C_{rsd2}\right)+C_{box1}}{2{C_{Si1}t_{Si}}^2\left(2C_{Si1}+2\left(C_{rsd1}+C_{rsd2}\right)+C_{box1}\right)}\right)$ (3.32)

$$\begin{aligned}\phi_2(x,y) = \phi_{f2}(x)&\left[1+\frac{C_{ox2}}{C_{Si2}t_{Si}}y-\frac{C_{ox2}}{C_{Si2}t_{Si}^{\,2}}y^2-\left(2C_{Si2}+C_{ox2}\right)z_2y^2\right]\\&+(V_{GS}-V_{FB2})\left[-\frac{C_{ox2}}{C_{Si2}t_{Si}}y+\frac{C_{ox2}}{2C_{Si2}t_{Si}^{\,2}}y^2-\left(C_{ox2}\right)z_2y^2\right]\\&+(V_{DS}-2V_{FB3})\left[\frac{C_{rsd3}+C_{rsd4}}{2C_{Si2}t_{Si}^{\,2}}y^2+\left(C_{rsd3}+C_{rsd4}\right)z_2y^2\right]\\&+(V_{sub}-V_{FB4})\left[\frac{C_{box2}}{2C_{Si2}t_{Si}^{\,2}}y^2+\left(C_{box2}\right)z_2y^2\right]\end{aligned} \tag{3.33}$$

$$\text{where } z_2=\left(\frac{2\left(C_{rsd3}+C_{rsd4}\right)+C_{box2}}{2C_{Si2}t_{Si}^{\,2}\left(2C_{Si2}+2\left(C_{rsd3}+C_{rsd4}\right)+C_{box2}\right)}\right) \tag{3.34}$$

$$\begin{aligned}\phi_1(x,y) = \phi_{b1}(x)&\left[\left(\frac{2C_{Si1}+2\left(C_{rsd1}+C_{rsd2}\right)+C_{box1}}{2C_{Si1}+C_{ox1}}\right)z_3-\right.\\&\left.\left(\frac{C_{rsd1}+C_{rsd2}}{C_{Si1}t_{Si}^{\,2}}+\frac{C_{box1}}{2C_{Si1}t_{Si}^{\,2}}\right)y^2\right]\\&+(V_{GS}-V_{FB1})\left[-\frac{C_{ox1}}{C_{Si1}t_{Si}}y+\frac{C_{ox1}}{C_{Si1}t_{Si}^{\,2}}y^2+\left(\frac{C_{ox1}}{2C_{Si1}+C_{ox1}}\right)z_3\right]\\&+(V_{DS}-2V_{FB3})\left[\frac{C_{rsd1}+C_{rsd2}}{C_{Si1}t_{Si}^{\,2}}y^2-\left(\frac{C_{rsd1}+C_{rsd2}}{2C_{Si1}+C_{ox1}}\right)z_3\right]\\&+(V_{sub}-V_{FB4})\left[\frac{C_{box1}}{C_{Si1}t_{Si}^{\,2}}y^2-\left(\frac{C_{box1}}{2C_{Si1}+C_{ox1}}\right)z_3\right]\end{aligned} \tag{3.35}$$

$$\text{where, } z_3=\left(1+\frac{C_{ox1}}{C_{Si1}t_{Si}}y-\frac{C_{ox1}}{2C_{Si1}t_{Si}^{\,2}}y^2\right) \tag{3.36}$$

$$\phi_2(x,y)=\phi_{b2}(x)\left[\left(\frac{2C_{Si2}+2\left(C_{rsd3}+C_{rsd4}\right)+C_{box2}}{2C_{Si2}+C_{ox2}}\right)z_4-\left(\frac{C_{rsd3}+C_{rsd4}}{C_{Si2}t_{Si}^{\,2}}+\frac{C_{box2}}{2C_{Si2}t_{Si}^{\,2}}\right)y^2\right]$$
$$+(V_{GS}-V_{FB2})\left[-\frac{C_{ox2}}{C_{Si2}t_{Si}}y+\frac{C_{ox2}}{C_{Si2}t_{Si}^{\,2}}y^2+\left(\frac{C_{ox2}}{2C_{Si2}+C_{ox2}}\right)z_4\right] \quad (3.37)$$
$$+(V_{DS}-2V_{FB3})\left[\frac{C_{rsd3}+C_{rsd4}}{C_{Si2}t_{Si}^{\,2}}y^2-\left(\frac{C_{rsd3}+C_{rsd4}}{2C_{Si2}+C_{ox2}}\right)z_4\right]$$
$$+(V_{sub}-V_{FB4})\left[\frac{C_{box2}}{C_{Si2}t_{Si}^{\,2}}y^2-\left(\frac{C_{box2}}{2C_{Si2}+C_{ox2}}\right)z_4\right]$$

where, $z_4=\left(1+\frac{C_{ox2}}{C_{Si2}t_{Si}}y-\frac{C_{ox2}}{2C_{Si2}t_{Si}^{\,2}}y^2\right)$ (3.38)

Further, by substituting $\phi_1(x,y)$and $\phi_2(x,y)$in Eq. (3.1) and putting $y=0$ and $y=t_{Si}$ respectively, the following differential equations of front- and back-surface potential are obtained

$$\frac{d^2\phi_{fi}(y)}{dx^2}-\alpha_{fi}\phi_{fi}(y)=\beta_{fi},\ i=1,2 \quad (3.39)$$

$$\frac{d^2\phi_{bi}(y)}{dx^2}-\alpha_{bi}\phi_{bi}(y)=\beta_{bi},\ i=1,2 \quad (3.40)$$

where,

$$\alpha_{f1}=2\frac{1+\frac{C_{ox1}\left(C_{Si1}+C_{rsd1}+C_{rsd2}+C_{box1}\right)}{C_{Si1}\left(C_{rsd1}+C_{rsd2}+C_{box1}\right)}}{t_{Si}^{\,2}\left(1+\frac{2C_{Si1`}}{C_{rsd1}+C_{rsd2}+C_{box1}}\right)} \quad (3.41)$$

$$\alpha_{f2}=2\frac{1+\frac{C_{ox2}\left(C_{Si2}+C_{rsd3}+C_{rsd4}+C_{box2}\right)}{C_{Si2}\left(C_{rsd3}+C_{rsd4}+C_{box2}\right)}}{t_{Si}^{\,2}\left(1+\frac{2C_{Si2}}{C_{rsd3}+C_{rsd4}+C_{box2}}\right)} \quad (3.42)$$

$$\beta_{f1}=\left[\frac{qN_a}{\varepsilon_{Si}}-(V_{GS}-V_{FB1})\frac{2\dfrac{C_{ox1}(C_{Si1}+C_{rsd1}+C_{rsd2}+C_{box1})}{C_{Si1}(C_{rsd1}+C_{rsd2}+C_{box1})}}{t_{Si}^{\,2}\left(1+\dfrac{2C_{Si1}}{C_{rsd1}+C_{rsd2}+C_{box1}}\right)}\right.$$
$$-(V_{DS}-2V_{FB3})\frac{\dfrac{C_{rsd1}+C_{rsd2}}{C_{rsd1}+C_{rsd2}+C_{box1}}}{t_{Si}^{\,2}\left(1+\dfrac{2C_{Si1}}{C_{rsd1}+C_{rsd2}+C_{box1}}\right)} \tag{3.43}$$
$$\left.-(V_{sub}-V_{FB4})\frac{\dfrac{2C_{box1}}{C_{rsd1}+C_{rsd2}+C_{box1}}}{t_{Si}^{\,2}\left(1+\dfrac{2S_{Si1}}{C_{rsd1}+C_{rsd2}+C_{box1}}\right)}\right]$$

$$\beta_{f2}=\left[\frac{qN_a}{\varepsilon_{Si}}-(V_{GS}-V_{FB2})\frac{2\dfrac{C_{ox2}(C_{Si2}+C_{rsd3}+C_{rsd4}+C_{box2})}{C_{Si2}(C_{rsd3}+C_{rsd4}+C_{box2})}}{t_{Si}^{\,2}\left(1+\dfrac{2C_{Si2}}{C_{rsd3}+C_{rsd4}+C_{box2}}\right)}\right.$$
$$-(V_{DS}-2V_{FB3})\frac{\dfrac{C_{rsd3}+C_{rsd4}}{C_{rsd3}+C_{rsd4}+C_{box2}}}{t_{Si}^{\,2}\left(1+\dfrac{2C_{Si2}}{C_{rsd3}+C_{rsd4}+C_{box2}}\right)} \tag{3.44}$$
$$\left.-(V_{sub}-V_{FB4})\frac{\dfrac{2C_{box2}}{C_{rsd3}+C_{rsd4}+C_{box2}}}{t_{Si}^{\,2}\left(1+\dfrac{2C_{Si2}}{C_{rsd3}+C_{rsd4}+C_{box2}}\right)}\right]$$

$$\alpha_{b1}=2\frac{1+\dfrac{C_{ox1}(C_{Si1}+C_{rsd1}+C_{rsd2}+C_{box1})}{C_{Si1}(C_{rsd1}+C_{rsd2}+C_{box1})}}{t_{Si}^{\,2}\left(1+\dfrac{2C_{Si1`}}{C_{ox1}}\right)} \tag{3.45}$$

$$\alpha_{b2}=2\frac{1+\dfrac{C_{ox2}(C_{Si2}+C_{rsd3}+C_{rsd4}+C_{box2})}{C_{Si2}(C_{rsd3}+C_{rsd4}+C_{box2})}}{t_{Si}^{\,2}\left(1+\dfrac{2C_{Si2}}{C_{ox2}}\right)} \tag{3.46}$$

$$\beta_{b1}=\left[\frac{qN_a}{2\varepsilon_{Si}}-\frac{2\left(V_{GS}-V_{FB1}\right)}{t_{Si}^{\,2}\left(1+2\dfrac{C_{Si1}}{C_{ox1}}\right)}\right.$$
$$\left.-2\left(V_{DS}-2V_{FB3}\right)\frac{\left(\dfrac{C_{rsd1}}{C_{ox1}}+\dfrac{C_{rsd2}}{C_{Si1}}\right)}{t_{Si}^{\,2}\left(1+2\dfrac{C_{Si1}}{C_{ox1}}\right)}-2\left(V_{sub}-V_{FB4}\right)\frac{\left(\dfrac{C_{box1}}{C_{ox1}}+\dfrac{C_{box1}}{C_{Si1}}\right)}{t_{Si}^{\,2}\left(1+2\dfrac{C_{Si1}}{C_{ox1}}\right)}\right] \tag{3.47}$$

$$\beta_{b2}=\left[\frac{qN_a}{2\varepsilon_{Si}}-\frac{2\left(V_{GS}-V_{FB2}\right)}{t_{Si}^{\,2}\left(1+2\dfrac{C_{Si2}}{C_{ox2}}\right)}\right.$$
$$\left.-2\left(V_{DS}-2V_{FB3}\right)\frac{\left(\dfrac{C_{rsd3}}{C_{ox2}}+\dfrac{C_{rsd4}}{C_{Si2}}\right)}{t_{Si}^{\,2}\left(1+2\dfrac{C_{Si2}}{C_{ox2}}\right)}-2\left(V_{sub}-V_{FB4}\right)\frac{\left(\dfrac{C_{box2}}{C_{ox2}}+\dfrac{C_{box2}}{C_{Si2}}\right)}{t_{Si}^{\,2}\left(1+2\dfrac{C_{Si2}}{C_{ox2}}\right)}\right] \tag{3.48}$$

Now, the following equations of front- and back-surface potentials, $\phi_{fi,bi}(x)$, are obtained by solving the differential Eqs. (3.39) and (3.40) with the help of boundary conditions of Eqs. (3.25)-(3.26)

$$\phi_{f1,b1}(x)=\frac{\psi_{fd1,bd1}\sinh\left(\lambda_{f1,b1}x\right)-\psi_{fs1,bs1}\sinh\left(\lambda_{f1,b1}\left(x-L_1\right)\right)}{\sinh\left(\lambda_{f_{1,b1}}L_1\right)}-\sigma_{f1,b1} \tag{3.49}$$

$$\phi_{f2,b2}(x)=\frac{\psi_{fd2,bd2}\sinh\left(\lambda_{f2,b2}\left(x-L_1\right)\right)-\psi_{fs2,bs2}\sinh\left(\lambda_{f2,b2}\left(x-L\right)\right)}{\sinh\left(\lambda_{f_{2,b2}}L_2\right)}-\sigma_{f2,b2} \tag{3.50}$$

where,

$$\lambda_{f_i}=\sqrt{\alpha_{fi}} \tag{3.51}$$

$$\lambda_{b_i}=\sqrt{\alpha_{bi}} \tag{3.52}$$

$$\sigma_{fi}=\frac{\beta_{fi}}{\alpha_{fi}} \tag{3.53}$$

$$\sigma_{bi} = \frac{\beta_{bi}}{\alpha_{bi}}, \tag{3.54}$$

$$\psi_{fs1} = V_{bi} + \sigma_{f1} \tag{3.55}$$

$$\psi_{fd1} = V_{fp} + \sigma_{f1} \tag{3.56}$$

$$\psi_{fs2} = V_{fp} + \sigma_{f2} \tag{3.57}$$

$$\psi_{fd2} = V_{bi} + V_{DS} + \sigma_{f2} \tag{3.58}$$

$$\psi_{bs1} = V_{bi} + \sigma_{b1} \tag{3.59}$$

$$\psi_{bd1} = V_{bp} + \sigma_{b1} \tag{3.60}$$

$$\psi_{bs2} = V_{bp} + \sigma_{b2} \tag{3.61}$$

$$\psi_{bd2} = V_{bi} + V_{DS} + \sigma_{b2} \tag{3.62}$$

$$V_{fp} = \frac{\psi_{f,d2}\, cos\, ech(\lambda_f L_2) + \psi_{f,s1}\, cos\, ech(\lambda_f L_1) - \sigma_{f1}\, coth(\lambda_f L_2) - \sigma_{f2}\, coth(\lambda_f L_2)}{coth(\lambda_f L_1) + coth(\lambda_f L_2)} \tag{3.63}$$

$$V_{bp} = \frac{\psi_{b,d2}\, cos\, ech(\lambda_b L_2) + \psi_{b,s1}\, cos\, ech(\lambda_b L_1) - \sigma_{b1}\, coth(\lambda_b L_1) - \sigma_{b2}\, coth(\lambda_b L_2)}{coth(\lambda_b L_1) + coth(\lambda_b L_2)} \tag{3.64}$$

where, $\lambda_{f_i} = \lambda_f$ and $\lambda_{b_i} = \lambda_b$ are the characteristic lengths associated with the front-surface potential and back-surface potential, respectively.

The position (x_{min}) of the front- and back-surface minimum potential value (virtual cathode) lies under the control gate and is estimated by solving $\left.\frac{d\phi_{f1,b1}(x)}{dx}\right|_{(x_{min})} = 0$ which yields

$$(x_{min})_{f1,b1} = \frac{1}{2\lambda_{f,b}} ln\left(\frac{b_{f1,b1}}{a_{f1,b1}}\right) \tag{3.65}$$

Now the front- and back- channel minimum surface potential, $\phi_{f1min,b1min}$, under the control gate region can be obtained by putting Eq. (3.65) into Eq. (3.49) and its value is found to be

$$\phi_{f1min,b1min} = 2\sqrt{a_{f1,b1} b_{f1,b1}} - \sigma_{f1,b1}, \tag{3.66}$$

where,

$$a_{f1,b1} = \frac{-1}{2\sinh(\lambda_{f,b}L_1)}\left[\psi_{fs1,bs1}e^{-\lambda_{f1,b1}L_1} - \psi_{fd1,bd1}\right] \tag{3.67}$$

$$b_{f1,b1} = \frac{-1}{2\sinh(\lambda_{f,b}L_1)}\left[-e^{\lambda_{f1,b1}L_1}\psi_{fs1,bs1} + \psi_{fd1,bd1}\right] \tag{3.68}$$

Here, it is worth mentioning that ϕ_{f1min} and ϕ_{b1min} are two important parameters which determine the source-channel barrier heights at front and back surfaces of the channel respectively. The condition $\phi_{f1min} > \phi_{b1min}$ indicates that the source-channel barrier height at the front-surface of the channel is lower compared to the same at the back channel. And, as a result the inversion layer is formed at the front-surface of the channel when gate voltage is raised up to the threshold voltage level. Similarly, the condition $\phi_{f1min} < \phi_{b1min}$ facilitates the inversion layer to be formed at the back surface of the channel under suitable gate bias condition. In a conventional SOI MOSFET, the condition $\phi_{f1min} > \phi_{b1min}$ holds generally true because the back surface of the channel remains far away from the front-gate. Further, the weak source/drain-back channel coupling also does not help much. However, in case of Re-S/D SOI MOSFETs, both conditions (i.e $\phi_{f1min} > \phi_{b1min}$ or $\phi_{f1min} < \phi_{b1min}$) may hold true depending upon the device parameters [Kumar *et al.* (2014)]. For example, if the channel region is highly doped or the device channel length is considerably large, the Re-S/D SOI MOSFET behaves as a conventional SOI MOSFETs [Kumar *et al.* (2014)]. However, in case of a short-channel undoped/lightly doped Re-S/D SOI MOSFET, a strong electrostatics coupling between source/drain and back surface of the channel builds up, and the condition $\phi_{f1min} < \phi_{b1min}$ is found to be exist. This strong coupling may lead the back surface of the channel to the inversion.

Now, we derive the following equation of the so-called virtual cathode potential $\phi_{vc}(y)$ [Chen *et al.* (2003)] ($\phi_{vc}(y) = \phi_1(x,y)\big|_{x=x_{min}}$,where $x = x_{min}$ is the position where minima of front-/back-surface potential exists). The obtained virtual cathode potential $\phi_{vc}(y)$which is a function of the minimum value of the front-surface potential is

$$\begin{aligned}\phi_{vc}(y)=\phi_{f1min}&\left[1+\frac{C_{ox1}}{C_{Si1}t_{Si}}y-\frac{C_{ox1}}{C_{Si1}t_{Si}^{\,2}}y^2-\left(2C_{Si1}+C_{ox1}\right)z_1y^2\right]\\&+(V_{GS}-V_{FB1})\left[-\frac{C_{ox1}}{C_{Si1}t_{Si}}y+\frac{C_{ox1}}{2C_{Si1}t_{Si}^{\,2}}y^2-\left(C_{ox1}\right)z_1y^2\right]\\&+(V_{DS}-2V_{FB3})\left[\frac{C_{rsd1}+C_{rsd2}}{2C_{Si1}t_{Si}^{\,2}}y^2+\left(C_{rsd1}+C_{rsd2}\right)z_1y^2\right]\\&+(V_{sub}-V_{FB4})\left[\frac{C_{box1}}{2C_{Si1}t_{Si}^{\,2}}y^2+\left(C_{box1}\right)z_1y^2\right]\end{aligned}\tag{3.69}$$

Similarly, another equation of the so-called virtual cathode potential which is a function of the minimum value of the back surface potential can also be obtained

$$\begin{aligned}\phi_{vc}(y)=\phi_{b1min}&\left[\left(\frac{2C_{Si1}+2\left(C_{rsd1}+C_{rsd2}\right)+C_{box1}}{2C_{Si1}+C_{ox1}}\right)z_3-\left(\frac{C_{rsd1}+C_{rsd2}}{C_{Si1}t_{Si}^{\,2}}+\frac{C_{box1}}{2C_{Si1}t_{Si}^{\,2}}\right)y^2\right]\\&+(V_{GS}-V_{FB1})\left[-\frac{C_{ox1}}{C_{Si1}t_{Si}}y+\frac{C_{ox1}}{C_{Si1}t_{Si}^{\,2}}y^2+\left(\frac{C_{ox1}}{2C_{Si1}+C_{ox1}}\right)z_3\right]\\&+(V_{DS}-2V_{FB3})\left[\frac{C_{rsd1}+C_{rsd2}}{C_{Si1}t_{Si}^{\,2}}y^2-\left(\frac{C_{rsd1}+C_{rsd2}}{2C_{Si1}+C_{ox1}}\right)z_3\right]\\&+(V_{sub}-V_{FB4})\left[\frac{C_{box1}}{C_{Si1}t_{Si}^{\,2}}y^2-\left(\frac{C_{box1}}{2C_{Si1}+C_{ox1}}\right)z_3\right]\end{aligned}\tag{3.70}$$

Here, it should be noted that either of Eqs. (3.69) or (3.70) can be utilized for the formulation of the subthreshold charge carrier density at virtual cathode position.

3.3 Threshold Voltage Formulation

The threshold voltage V_{th} of a MOSFET is defined as that value of the gate voltage V_{GS} at which a number of minority carriers at the channel surface equals the majority carrier concentration in the bulk. In other words, in a conventional MOSFET, the threshold voltage is taken to be that value of the gate-source voltage at which the virtual cathode potential becomes equal to the twice of the Fermi potential (i.e. $\phi_{f1min,,b1min}=2\phi_{f,Si}$

where, $\phi_{f1min,b1min}$ is minimum surface potential) [Svilicic *et al.* (2009)]. However, this definition of the threshold voltage does not hold completely true for a lightly doped or intrinsic SOI MOSFET owing to the volume inversion in the whole channel region, as discussed in Chapter 2. Because of the early inversion of the charge carriers in an intrinsic/lightly doped SOI film, the threshold voltage definition is modified as discussed in section 2.4.1 of Chapter 2. In this chapter, the modified threshold voltage definition of [Chen *et al.* (2003)] is used for threshold voltage formulation. Further, any of the front-channel or back channel may be inverted at first and form a conducting channel between source and drain, threshold voltage associated with front-surface and back-surface of the channel regions have been formulated separately.

3.3.1 Front Channel Threshold Voltage Formulation

The front-channel threshold voltage (V_{thf}) is considered to be the value of the gate voltage at which the minimum of front-channel surface potential ϕ_{f1min} is found to be $2\phi^*_{f,Si}$,

$$\text{i.e. } \phi_{f1min}\big|_{V_G=V_{thf}} = 2\phi^*_{f,Si} = \begin{cases} 2\phi_{f,Si} & for, N_a > n_T \\ \phi_{f,Si} + \dfrac{kT}{q} ln\left(\dfrac{n_T}{n_i}\right) & for, N_a < n_T \end{cases} \tag{3.71}$$

where, q is the electron charge, N_a is the channel doping concentration, n_i is the intrinsic carrier concentration, k is the Boltzmann's constant, and T is the temperature, $\phi_{f,Si}$ is the Fermi potential, n_T is a critical concentration of electron in the channel to turn on the device [Lee *et al.* (1989)]. It should be noted that n_T depends on device parameters like channel thickness and channel length; it has been determined following the method of Chen [Chen (2003), Svilicic *et al.* (2010)].

Thus, solving $\phi_{f1min} = 2\sqrt{a_{f1}b_{f1}} - \sigma_{f1}\big|_{V_{GS}=Vt_{hf}} = 2\phi^*_{f,Si}$ gives the following expression for front-channel threshold voltage, V_{thf}

$$V_{thf} = \frac{-q_f + \sqrt{{q_f}^2 - 4p_f r_f}}{2p_f} \tag{3.72}$$

where, $p_f = v_{f1}v_{f2} - n_f^2$ (3.73)

$$q_f = u_{f1}v_{f2} + u_{f2}v_{f1} - 2n_f l_f \tag{3.74}$$

$$r_f = u_{f1}u_{f2} - {l_f}^2 \tag{3.75}$$

$$u_{f1} = \frac{(V_{fp11} + m_{f1}) - (V_{bi} + m_{f1})exp(-\lambda_f L_1)}{sinh(\lambda_f L_1)} \tag{3.76}$$

$$v_{f1} = \frac{V_{fp12} + (1 - exp(-\lambda_f L_1))n_f}{sinh(\lambda_f L_1)} \tag{3.77}$$

$$u_{f2} = \frac{(V_{bi} + m_{f1})exp(\lambda_f L_1) - (V_{fp11} + m_{f1})}{sinh(\lambda_f L_1)} \tag{3.78}$$

$$v_{f2} = \frac{(exp(\lambda_f L_1) - 1)n_f - V_{fp12}}{sinh(\lambda_f L_1)} \tag{3.79}$$

$$l_f = 2\phi_f + m_{1f} \tag{3.80}$$

$$V_{fp_{11}} = \frac{\begin{aligned}[(V_{bi} + V_{DS})\,cos\,ech(\lambda_f L_2) + (V_{bi})\,cos\,ech(\lambda_f L_1) + m_{b1}(cos\,ech(\lambda_f L_2) - coth(\lambda_f L_2))\\ + m_{f1}(cos\,ech(\lambda_f L_1) - coth(\lambda_f L_1))]\end{aligned}}{coth(\lambda_f L_1) + coth(\lambda_f L_2)} \tag{3.81}$$

$$V_{fp_{12}} = \frac{n_f [cos\,ech(\lambda_f L_2) - coth(\lambda_f L_2) + cos\,ech(\lambda_f L_1) - coth(\lambda_f L_1)]}{coth(\lambda_f L_1) + coth(\lambda_f L_2)} \tag{3.82}$$

$$m_{1f} = \frac{\left[\frac{qN_a}{\varepsilon_{Si}}\left(\alpha_{f2} - \beta_{f1}\frac{C_{ox1}}{C_{rsd1} + C_{rsd2} + C_{box1}}\right) - k\left(\alpha_{f2} + \beta_{f1}\frac{C_{ox1}}{C_{rsd1} + C_{rsd2} + C_{box1}}\right)\right]}{\alpha_{f1}\alpha_{f2} - \beta_{f1}\beta_{f2}} \tag{3.83}$$

$$n_f = \frac{\frac{C_{ox1}C_{Si1}}{t_{Si}^2}\left(\alpha_{f2} - \beta_{f1}\frac{C_{ox1}}{C_{rsd1} + C_{rsd2} + C_{box1}}\right)}{\alpha_{f1}\alpha_{f2} - \beta_{f1}\beta_{f2}} \tag{3.84}$$

3.3.2 Back Channel Threshold Voltage Formulation

Similarly, solving $\phi_{b1min} = 2\sqrt{a_b b_b} - \sigma_{b1}\Big|_{V_{GS}=Vt_{hb}} = 2\phi^*_{f,Si}$ gives the following expression for back-channel threshold voltage, V_{thb}

$$V_{thb} = \frac{-q_b + \sqrt{q_b^{\,2} - 4p_b r_b}}{2p_b} \tag{3.85}$$

where, $p_b = v_{b1}v_{b2} - n_b^2$ (3.86)

$$q_b = u_{b1}v_{b2} + u_{b2}v_{b1} - 2n_b l_b \tag{3.87}$$

$$r_b = u_{b1}u_{b2} - l_b^{\,2} \tag{3.88}$$

$$u_{b1} = \frac{(V_{bp11} + m_{b1}) - (V_{bi} + m_{b1})exp(-\lambda_b L_1)}{sinh(\lambda_b L_1)} \tag{3.89}$$

$$v_{b1} = \frac{V_{bp12} + (1 - exp(-\lambda_c L_1))n_b}{sinh(\lambda_b L_1)} \tag{3.90}$$

$$u_{b2} = \frac{(V_{bi} + m_{b1})exp(\lambda_b L_1) - (V_{bp11} + m_{b1})}{sinh(\lambda_b L_1)} \tag{3.91}$$

$$v_{b2} = \frac{(exp(\lambda_b L_1) - 1)n_b - V_{bp12}}{sinh(\lambda_b L_1)} \tag{3.92}$$

$$l_b = 2\phi_f + m_{b1} \tag{3.93}$$

$$V_{bp_{11}} = \frac{\begin{aligned}&[(V_{bi} + V_{DS})cos\,ech(\lambda_b L_2) + (V_{bi})cos\,ech(\lambda_b L_1)\\ &+ m_{b1}(cos\,ech(\lambda_b L_2) - coth(\lambda_b L_2))m_{f1}(cos\,ech(\lambda_b L_1) - coth(\lambda_b L_1))]\end{aligned}}{coth(\lambda_f L_1) + coth(\lambda_f L_2)} \tag{3.94}$$

$$V_{bp_{12}} = \frac{n_b[cos\,ech(\lambda_b L_2) - coth(\lambda_b L_2) + cos\,ech(\lambda_b L_1) - coth(\lambda_b L_1)]}{coth(\lambda_b L_1) + coth(\lambda_b L_2)} \tag{3.95}$$

$$m_{b1} = \frac{\left[\frac{qN_a}{\varepsilon_{Si}}\left(\alpha_{b1}\frac{C_{ox1}}{C_{rsd1}+C_{rsd2}+C_{box1}}-\beta_{b2}\right)+k\left(\alpha_{b1}\frac{C_{ox1}}{C_{rsd1}+C_{rsd2}+C_{box1}}+\beta_{b2}\right)\right]}{\alpha_{b1}\alpha_{b2}-\beta_{b1}\beta_{b2}} \tag{3.96}$$

$$n_b = \frac{\frac{C_{ox1}C_{Si1}}{t_{Si}^2}\left(\alpha_{b1}\frac{C_{ox1}}{C_{rsd1}+C_{rsd2}+C_{box1}}-\beta_{b2}\right)}{\alpha_{b1}\alpha_{b2}-\beta_{b1}\beta_{b2}} \tag{3.97}$$

As mentioned above, DMG FD Re-S/D SOI MOSFET may have two different threshold voltages associated with the front-surface and back-surface of the channel region, respectively. Hence, the threshold voltage V_{th} of a DMG Re-S/D SOI MOSFET could be determined either by front-surface threshold voltage (V_{thf}) or by the back surface threshold voltage (V_{thb}) depending on the front- and back- minimum surface potential. In this way, the threshold voltage of DMG UTB Re-S/D SOI MOSFET is defined as

$$V_{th} = \begin{cases} V_{thf}, & for \quad \phi_{f,1min} > \phi_{b,1min} \\ V_{thb}, & for \quad \phi_{f,1min} < \phi_{b1,min} \end{cases}. \tag{3.98}$$

3.3.3 Threshold Voltage Modifications due to Quantum Mechanical Effects (QMEs)

The model's accuracy could be improved for ultra-thin body structure by adding following quantum effects induced correction term ΔV_{th} in the threshold voltage model of Eq. (3.98) [Dort *et al.* (1992)].

$$\Delta V_{th} = \Delta E_0\left(1+\frac{\varepsilon_{Si}t_{ox}}{\varepsilon_k t_{Si}+\varepsilon_{Si}t_{box}}\right) \tag{3.99}$$

where, ΔE_0 is the difference between the first discrete energy level and the lowest conduction band energy level which is given as [Dort *et al.* (1992)].

$$\Delta E_0 = \left(\frac{h^2}{2m^*}\right)^{1/3}\left[\frac{9}{8}\pi qE\right]^{2/3} \tag{3.100}$$

where, h is the planks constant, m^* is effective mass of the electron, E is the normal electric field due to the charge in the depletion layer.

3.4 Subthreshold Current Formulation

The diffusion dominant subthreshold current in weak inversion is assumed to be proportional to the carrier concentration at the virtual cathode, $n_{\min}(y)$, and hence, can be defined as [Kumar *et al.* (2013), Dey at al. (2008)]

$$I_{sub} = \int_0^{t_{Si}} J_n(y)dy \tag{3.101}$$

where, $J_n(y) = \frac{qD_n n_{min}(y)}{L_e}\left(1 - exp\left(-\frac{V_{DS}}{V_T}\right)\right)$ (3.102)

D_n is the coefficient of diffusion, L_e is the effective channel length, V_T is the thermal voltage. The electron density at the virtual cathode, $n_{min}(y)$ can be expressed as [Dey at al. (2008)]

$$n_{min}(y) = \frac{n_i^2}{N_a} exp\left(\frac{\phi_{vc}(y)}{V_T}\right) \tag{3.103}$$

where n_i is the intrinsic carrier concentration.

The effective channel length can be expressed as [Dey at al. (2008)]

$$L_e = L - (L_s + L_d) + 2L_D \tag{3.104}$$

where, L_s and L_d represent the source and drain depletion width, L_D be the Debye length, all of which can be formulated as[Yeh *et al.* (1995)]

$$L_s = \frac{2(V_{bi} - \phi_{vc}(y_m))}{\left.\frac{d\phi(x,y)}{dx}\right|_{x=0}} \tag{3.105}$$

$$L_d = \frac{2\left(V_{bi} + V_{ds} - \phi_{vc}\left(y_m\right)\right)}{\left.\frac{d\phi(x,y)}{dx}\right|_{x=L_1+L_2}} \tag{3.106}$$

$$L_D = \sqrt{\frac{\varepsilon_{Si} V_T}{qN_a}} \tag{3.107}$$

where, $\phi_{vc}\left(y_m\right) = \phi_{vc}(y)$ is the value of the minimum surface potential function along the channel thickness at $y = y_m$, where y_m can be obtained by solving

$$\frac{\partial \phi_{vc}(y)}{\partial y} = 0 \text{ and } \phi_{vc}\left(y_m\right) = \phi_{vc}(y)\Big|_{y=y_m} \tag{3.108}$$

Equation (3.101) is a complex equation and cannot be solved analytically. However, an approximate solution of Eq. (3.101) can be obtained by invoking a piecewise linear approximation of the virtual cathode potential equation. For this purpose the channel region may be divided into two parts; region 1 ($0 \le y \le y_m$) contributing current I_F, and region 2 ($y_m \le y \le t_{Si}$) contributing another current I_B. Further, the virtual cathode potential variation is approximated by two straight lines in regions1 and 2. [Yeh *et al.* (1995)]. Finally, the subthreshold current can now be written as

$$\begin{aligned} I_{sub} &= I_F + I_B \\ &= K\left[\int_0^{y_m} \exp\left(\frac{\phi_{vc}(y)}{V_T}\right) dy + \int_{y_m}^{t_{Si}} \exp\left(\frac{\phi_{vc}(y)}{V_T}\right) dy\right] \end{aligned} \tag{3.109}$$

$$\text{where } K = \frac{qD_n V_T n_i^{\,2}}{L_e N_a}\left(1 - exp\left(-\frac{V_{DS}}{V_T}\right)\right) \tag{3.110}$$

Assuming the linear variation of $\phi_{vc}(y)$ in y direction, Eq. (3.109) can be solved as [Dey at al. (2008)]

$$I_{sub} = KV_T\left(\frac{I_f}{E_f} + \frac{I_b}{E_b}\right) \tag{3.111}$$

where,

$$I_f = exp\left(\frac{\phi_{vc}(y=0)}{V_T}\right) - exp\left(\frac{\phi_{vc}(y=y_m)}{V_T}\right) \tag{3.112}$$

$$I_b = exp\left(\frac{\phi_{vc}(y=y_m)}{V_T}\right) - exp\left(\frac{\phi_{vc}(y=t_{Si})}{V_T}\right) \tag{3.113}$$

$$E_f = (\phi_{vc}(y=0) - \phi_{vc}(y=y_m))/y_m \tag{3.114}$$

$$E_b = (\phi_{vc}(y=y_m) - \phi_{vc}(y=t_{Si}))/(t_{Si} - y_m) \tag{3.115}$$

Eqs. (3.114 & 3.115) are the electric fields associated with the front- and back- surfaces of the channel. Eq. (3.111) is the desired expression for subthreshold current derived for DMG Re-S/D FD UTB SOI MOSFET.

3.5 Subthreshold Swing Formulation

The switching property of a MOS device is governed by the subthreshold swing characteristics in the weak inversion region. It is defined as the inverse slope of the $\log(I_D)\ vs V_{GS}$ characteristics in the subthreshold region. The typical value of subthreshold swing is 60mV/dec (at room temperature).

The subthreshold swing of a Re-S/D SOI MOSFETs can be expressed as [Svilicic *et al.* (2010)]

$$S = \begin{cases} V_T(ln10) \times \left(\frac{d\phi_{f1min}}{dV_{GS}}\right)^{-1} & for\ \phi_{f1min} > \phi_{b1min} \\ V_T(ln10) \times \left(\frac{d\phi_{b1min}}{dV_{GS}}\right)^{-1} & for\ \phi_{b1min} > \phi_{f1min} \end{cases} \tag{3.116}$$

Utilising Eq. (3.65) in Eq. (3.116) and after some mathematical calculations, we obtain the following closed form expression of the subthreshold swing of the DMG Re-S/D UTB SOI MOSFET

$$S=\begin{cases} V_T(ln10)\times\left(\dfrac{-1}{2\sqrt{a_{f1}b_{f1}}\sinh(\lambda_f L_1)}\left[\begin{array}{l}\dfrac{K_1}{\alpha_{f1}}\left(e^{-\lambda_f L_1}-1\right)\left(b_f+a_f e^{\lambda_f L_1}\right)\\ +\dfrac{K_2}{\alpha_{f2}}\dfrac{\psi_{f,s1}\left(1-\cosh(\lambda_f L_1)\right)\left(1-\cosh(\lambda_f L_2)\right)}{\sinh(\lambda_f L)}\\ +\dfrac{K_1}{\alpha_{f1}}\dfrac{\psi_{f,s1}\sinh(\lambda_f L_2)\left(1-\cosh(\lambda_f L_1)\right)^2}{\sinh(\lambda_f L_1)\sinh(\lambda_f L)}\end{array}\right]-\dfrac{K_1}{\alpha_{f1}}\right)^{-1} \\ \qquad\qquad for\,\phi_{f1min}>\phi_{b1min} \\ V_T(ln10)\times\left(\dfrac{-1}{2\sqrt{a_{b1}b_{b1}}\sinh(\lambda_b L_1)}\left[\begin{array}{l}\dfrac{K_3}{\alpha_{b1}}\left(e^{-\lambda_b L_1}-1\right)\left(b_b+a_b e^{\lambda_b L_1}\right)\\ +\dfrac{K_4}{\alpha_{b2}}\dfrac{\psi_{b,s1}\left(1-\cosh(\lambda_b L_1)\right)\left(1-\cosh(\lambda_b L_2)\right)}{\sinh(\lambda_b L)}\\ +\dfrac{K_3}{\alpha_{b1}}\dfrac{\psi_{b,s1}\sinh(\lambda_b L_2)\left(1-\cosh(\lambda_b L_1)\right)^2}{\sinh(\lambda_b L_1)\sinh(\lambda_b L)}\end{array}\right]-\dfrac{K_3}{\alpha_{b1}}\right)^{-1} \\ \qquad\qquad for\,\phi_{b1min}>\phi_{f1min} \end{cases} \tag{3.117}$$

where,

$$K_1=-\frac{\dfrac{2C_{ox1}\left(C_{Si1}+C_{rsd1}+C_{rsd2}+C_{box1}\right)}{C_{Si1}\left(C_{rsd1}+C_{rsd2}+C_{box1}\right)}}{t_{Si}^2\left(1+\dfrac{2C_{Si1}}{C_{rsd1}+C_{rsd2}+C_{box1}}\right)} \tag{3.118}$$

$$K_2=-\frac{\dfrac{2C_{ox2}\left(C_{Si2}+C_{rsd3}+C_{rsd4}+C_{box2}\right)}{C_{Si2}\left(C_{rsd3}+C_{rsd4}+C_{box2}\right)}}{t_{Si}^2\left(1+\dfrac{2C_{Si2}}{C_{rsd3}+C_{rsd4}+C_{box2}}\right)} \tag{3.119}$$

$$K_3=-\frac{2}{t_{Si}^2\left(1+\dfrac{2C_{Si1}}{C_{ox1}}\right)} \tag{3.120}$$

$$K_4=-\frac{2}{t_{Si}^2\left(1+\dfrac{2C_{Si2}}{C_{ox2}}\right)} \tag{3.121}$$

3.6 Results and Discussion

In this section, we have analyzed the derived theoretical models of subthreshold characteristics of the DMG Re-S/D UTB SOI MOSFETs. Further, the models have also been validated against the numerical simulation data obtained by a numerical device simulator ATLAS^{TM}. The drift-diffusion model has been used while simulating the carrier transportation in the device. The CVT mobility model has also been used as it is a complete mobility model in which mobility depends on doping density, temperature, lateral and transverse electric field. Fermi-Dirac carrier statistics has been employed to minimize the carrier concentration in the heavily doped regions. Along with this, a quantum transport equation (NEGF) is used to include the quantum effects The numerical threshold voltage has been extracted from the drain current-gate voltage curve by considering the value of that gate voltage at which drain current magnitude is given by $I_d = (W/L)\times 10^{-7}\, A/\mu m$, where W and L are width and length of the channel, respectively [Conde *et al.* (2002)].

3.6.1 Surface Potential

Figure 3.3 shows both front-channel and back-channel surface potential profiles along the channel length direction for a device channel length of $L = 60\text{nm}$ and $t_{rsd} = 30nm$. It may be noticed that the back-channel minimum surface potential is significantly higher than the front-channel minimum surface potential. This implies that just like Re-S/D SOI MOSFET as discussed in section 3.2, the source-channel barrier height is found lower at back surface of the channel in case of DMG Re-S/D SOI MOSFETs. The estimated value of the source channel barrier height associated with the back-channel is lower than that of the front-channel by ~76mV. This leads to a significant inversion at the back channel when gate-source voltage is raised, and the threshold voltage of the device should be determined by the threshold voltage of the back-surface of the channel. Since, we have considered only lightly doped short-channel length devices in this chapter, the status of back surface of the channel will determine the subthreshold characteristics of the device.

Figure 3.4 demonstrates the back-channel surface potential along the channel length direction for different control-gate to screen-gate length ratios $L_1 : L_2$. It should be noted that the control-to-screen gate ratio is varied whereas the total channel length remains fixed to L. As the source side metal gate has higher work function (control gate, ϕ_{M1}=4.8eV) than the drain side metal gate (screen gate, ϕ_{M2}= 4.6eV), the 'virtual cathode' position is found below the control gate and shifted towards the source end when the contribution of screen gate is increased in total channel length. Increasing the contribution of screen gate length from $1/3$ to $2/3$ in the total gate length, the minimum surface potential increases from 0.19 V to 0.27 V. Thus, varying the gate length ratio ($L_1 : L_2$) could modulate the position and magnitude of the minimum surface potential, which in turn could modulate the subthreshold characteristics of the device.

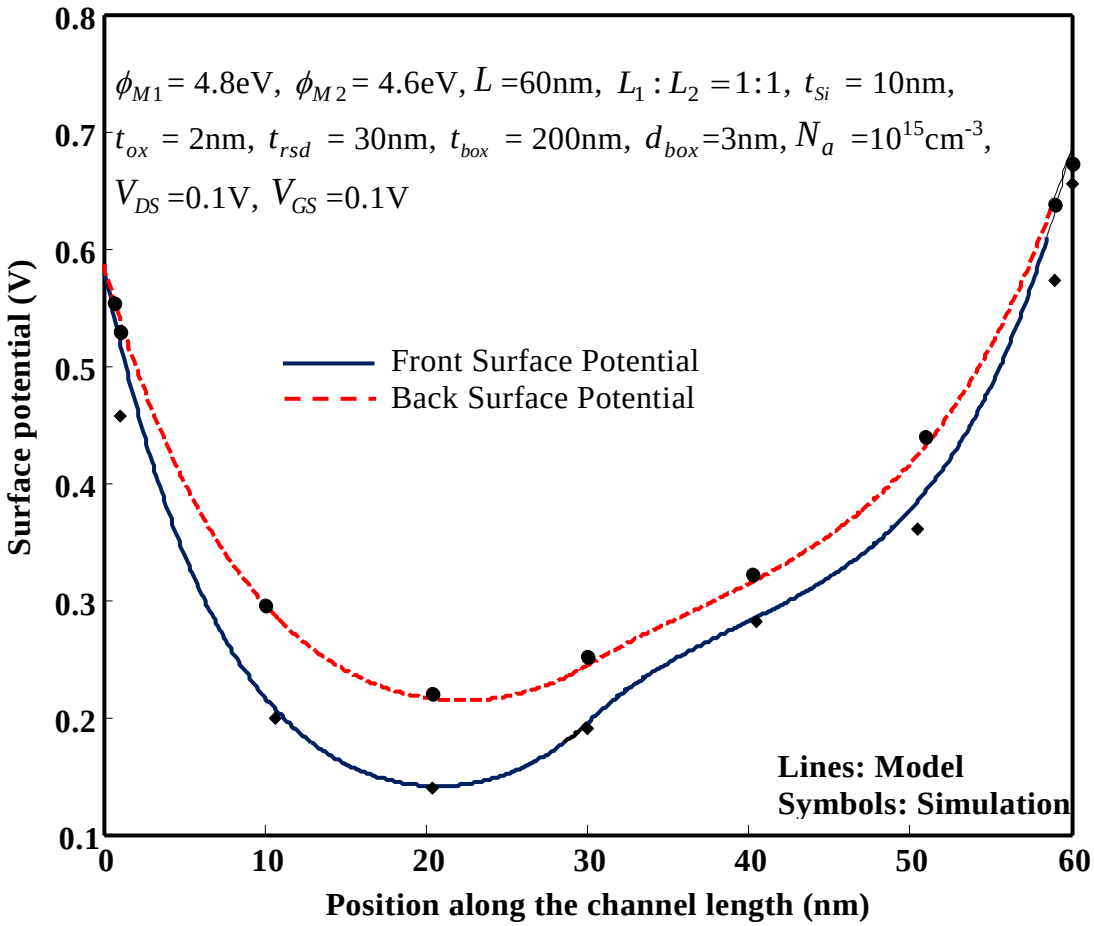


Fig. 3.3: Surface potential along the channel length at front-gate and back-gate

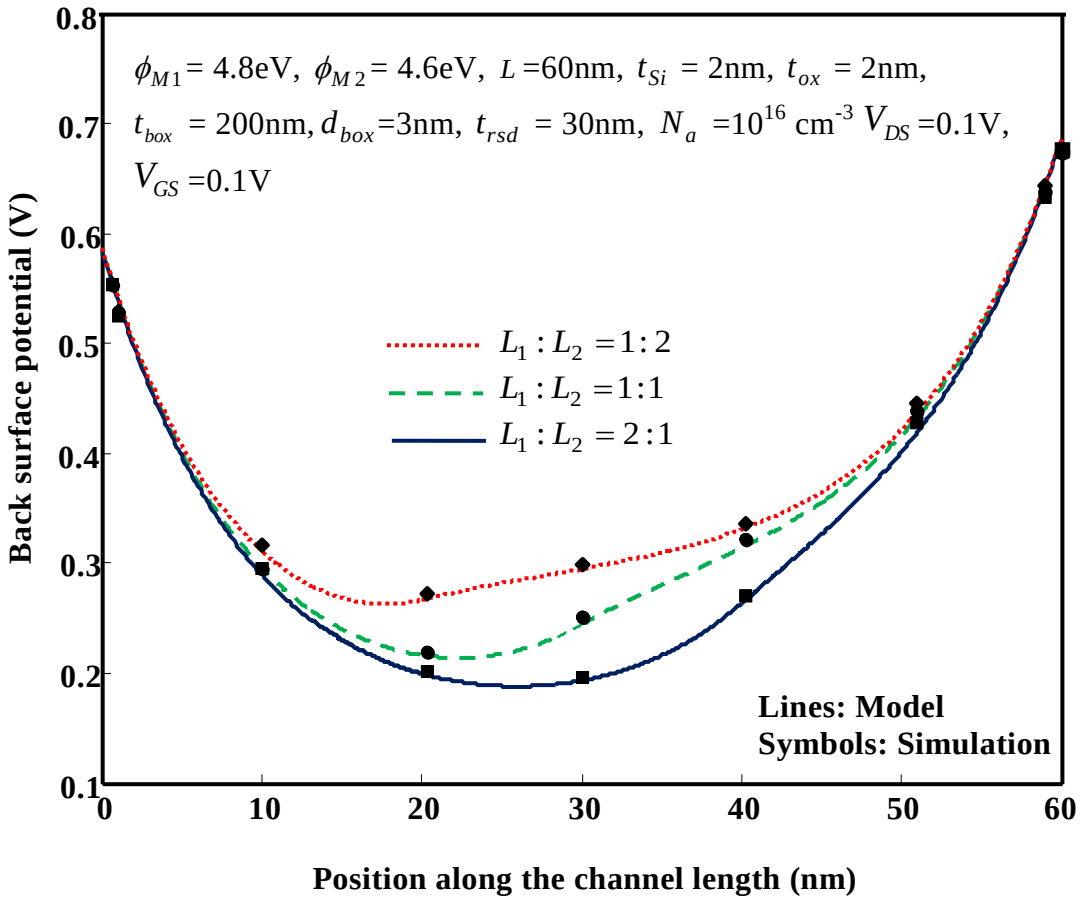


Fig. 3.4: Back surface potential along the channel at different control to screen gate length ratio

3.6.2 Threshold Voltage

Figure 3.5 exhibits the threshold voltage variation against the gate length at different oxide thickness. It is observed from the figure that the threshold voltage remains almost constant irrespective of the oxide thickness variations if the device channel length is selected above 150nm, however, devices with channel length less than 150nm become sensitive to the gate oxide thickness. Further, the threshold voltage of device with channel length less than 150nm is found to be decreased severely when a thicker gate oxide is considered in the device.

Figure 3.6 demonstrates the threshold voltage versus device channel length for different Si film thicknesses. The threshold voltage is found to be increased with the decrease in the thickness of the silicon channel. As the thickness of the channel is increased, the

controllability of the gate over the entire channel region is reduced due to the reduction in the gate electric field at the deeper section of the channel. Therefore, devices with thinner silicon films have higher channel barrier heights and higher threshold voltage. Thus, a thin Si film is preferred as a channel region as it causes a strong coupling between gate and channel region.

Figure 3.7 shows the threshold voltage versus device channel length at different recessed source/drain thicknesses, t_{rsd}. It should be noted that at $t_{rsd} = 0$, the device structure is similar to a conventional SOI MOSFET where the front-gate controls over the channel. As observed, the threshold voltage is found to be decreased with more and more penetration of source/drain in the BOX (larger t_{rsd}). The decrease in the threshold voltage may be attributed to the coupling of the back-surface of the channel region to the extended source and drain through the buried-oxide. Further, Fig. 3.7 proves the accuracy of our model and its applicability, where Re-S/D SOI MOSFET with two different recessed-source/drain thickness as well as conventional SOI MOSFET ($t_{rsd} = 0$) have been compared.

Figure 3.8 plots the threshold voltage versus channel length at different $L_1 : L_2$ ratio keeping the other device parameters constant. The threshold voltage roll-off is found to be decreased gradually with channel length if a higher ratio of $L_1 : L_2$(2:1) is chosen. It may be attributed to better short-channel effects (SCEs) immunity in such devices as the control gate length is larger than the screen gate length which in turn shifts the virtual cathode point away from the source end. As a result, it could be said that varying the ratio $L_1 : L_2$ may be an additional option to control the threshold voltage of the device.

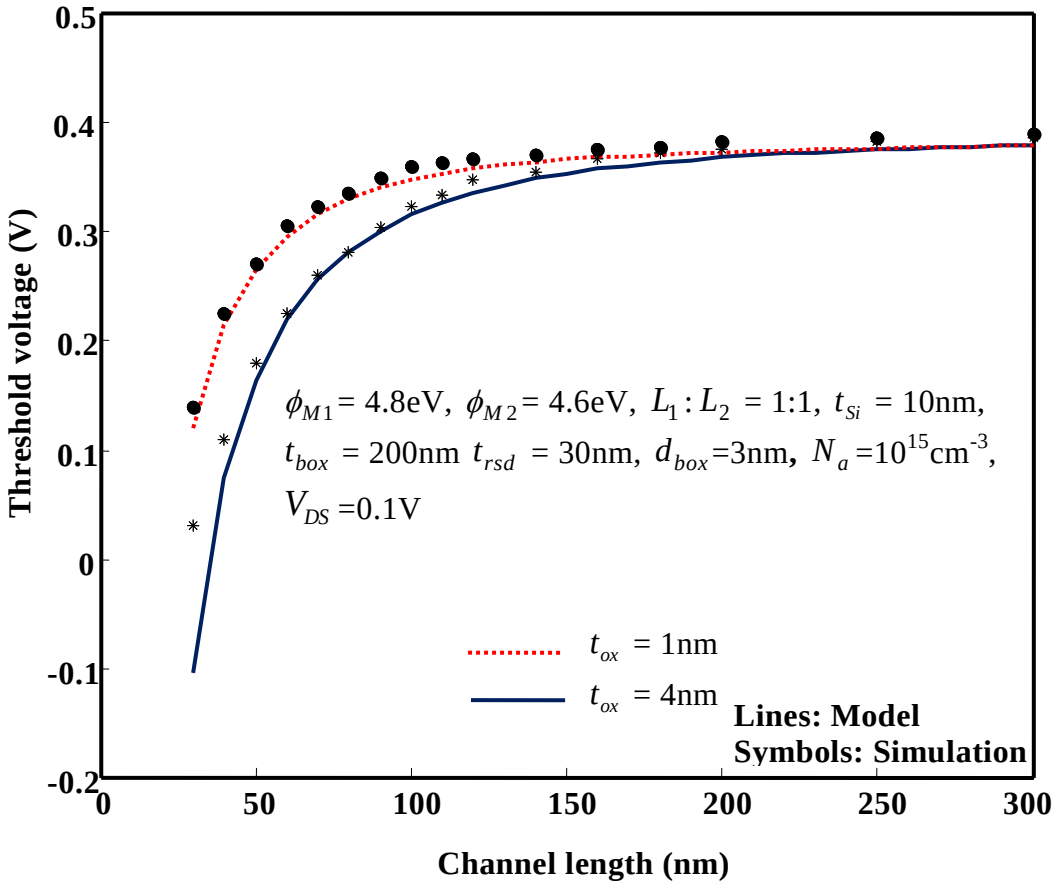


Fig. 3.5: Threshold voltage versus channel length for varying oxide thickness.

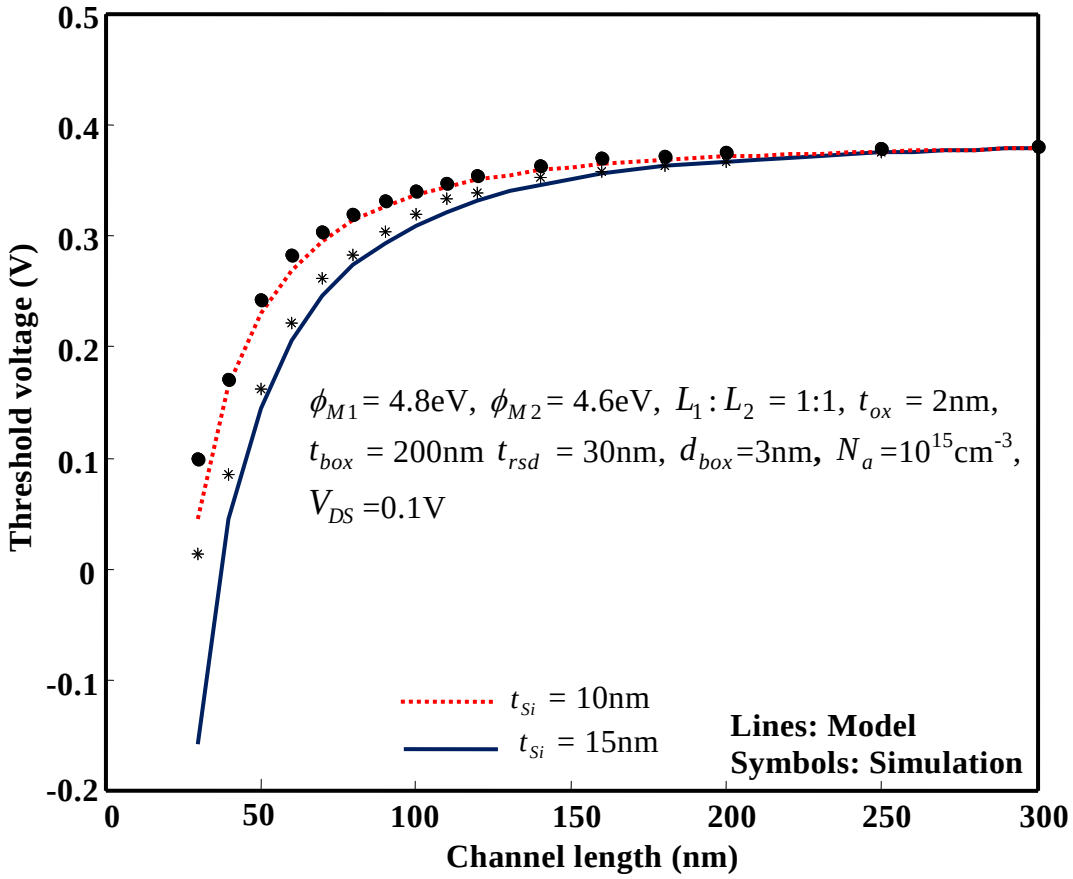


Fig. 3.6: Threshold voltage versus channel length for varying Si film thickness.

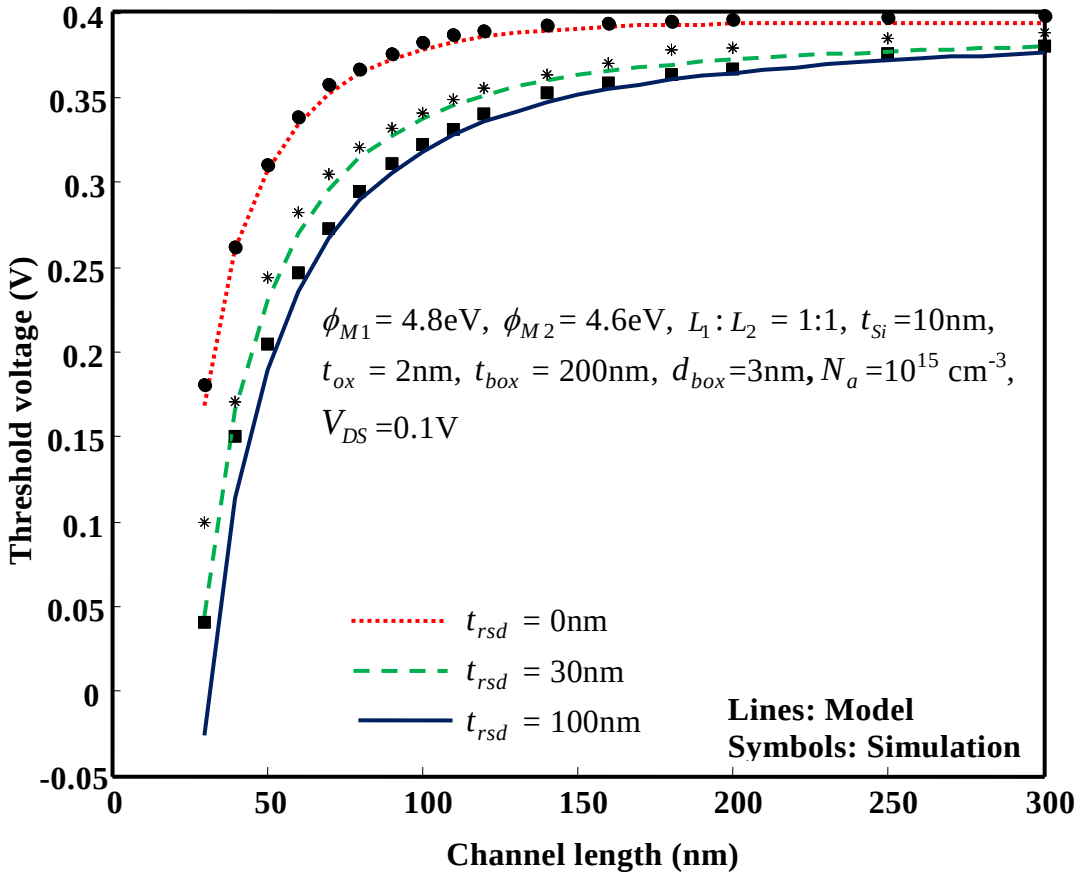


Fig. 3.7: Threshold voltage versus channel length for varying recessed oxide thickness.

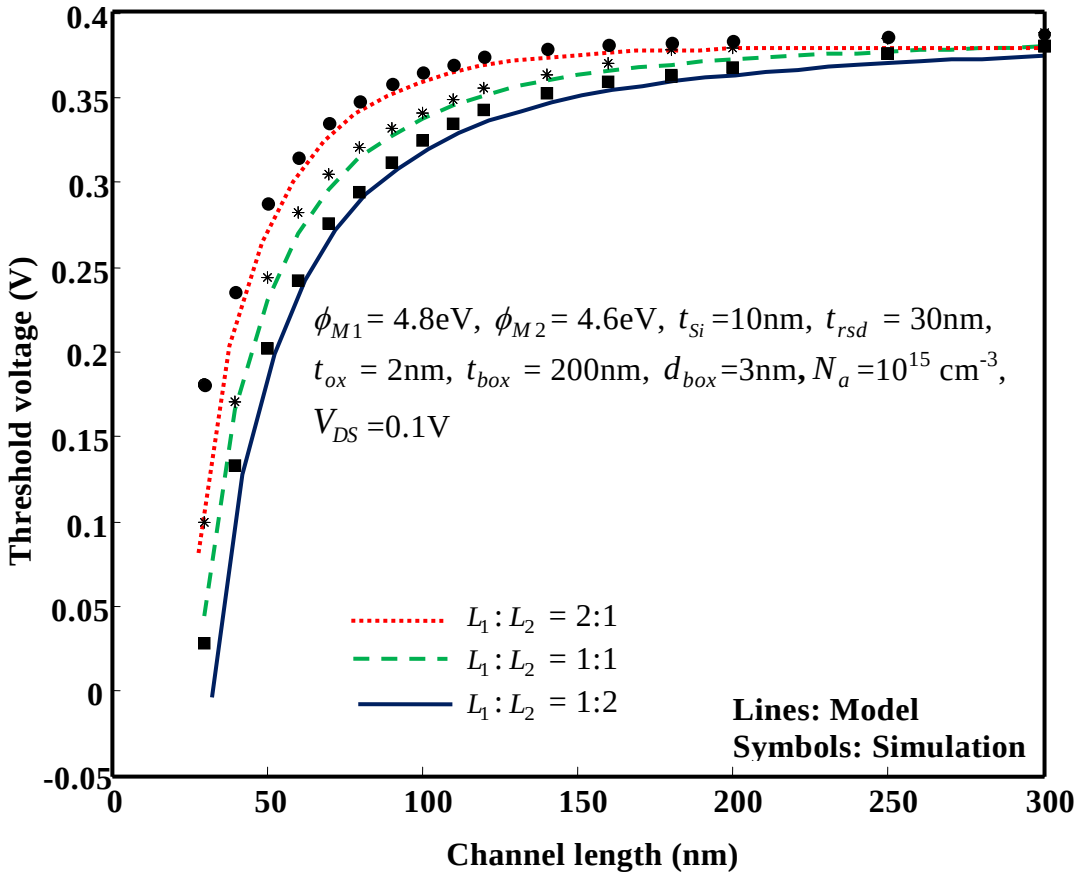


Fig. 3.8: Threshold voltage versus channel length for varying control to screen gate length ratio.

3.6.3 Subthreshold Current

Figure 3.9 plots the subthreshold current against the gate-to-source voltage for different channel lengths keeping other device parameters constant. The higher value of subthreshold current at a shorter channel length for a fixed gate voltage may be attributed to the reduced threshold voltage due to the short-channel effects. The influence of control to screen gate length ratio on subthreshold current characteristics of Re-S/D UTB SOI MOSFETs is investigated in Fig. 3.10. Keeping $L_1 : L_2 = 1:1$ as reference, the subthreshold current can be observed increasing with smaller control gate length (L_1) for $L_1 : L_2 = 1:2$; whereas in case of $L_1 : L_2 = 2:1$, the longer L_1 helps to boost the electrostatics in the channel region rendering reduced leakage current.

In Fig. 3.11, the subthreshold current characteristics are plotted with gate-to-source voltages for two different gate oxide thicknesses. Increasing the gate oxide thickness weakens the penetration power of electric field in the channel, which decontrols the channel. Such relaxation in gate control on channel causes enhanced leakage current in the channel. The effect of Si film thickness on the subthreshold current is examined in Fig. 3.12. It is observed from the figure that the subthreshold current is increased with the silicon channel thickness which is attributed to the fact that in case of a thinner silicon body, both the front-channel and the back channel are under the instant control of the gate and thus, the improved short-channel immunity results in reduced leakage current.

The influence of recessed source/drain thickness on subthreshold current is shown in Fig. 3.13 by keeping all other device parameters constant. It is found that at t_{rsd} = 0nm (conventional SOI with back-gate), subthreshold current is ~ $2*10^{-12}$A/μm and as t_{rsd} increases to 30nm and 100nm, subthreshold current is ~ $9*10^{-12}$A/μm and $1*10^{-11}$A/μm, respectively. It is due to the fact that the thicker recessed source/drain thickness offers higher short-channel effects due to the coupling of recessed source/drain and channel region and thus increasing the subthreshold current. However, a slight increase in subthreshold current is noticed with increasing t_{rsd} above 30nm.

All the theoretical results are well matched with the simulation results obtained from the 2D numerical simulator ATLAS^{TM} [SILVCO Int. (2012)] for a gate voltage below the threshold voltage of the device.

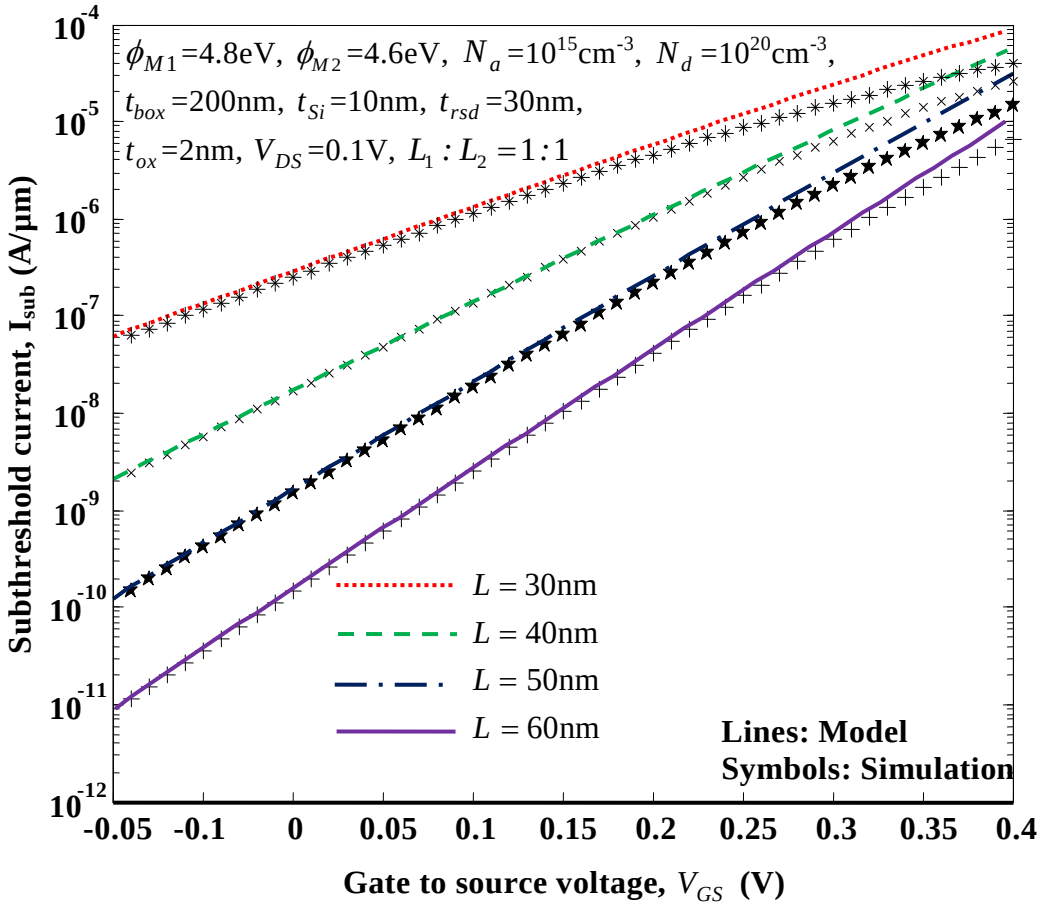


Fig. 3.9: Subthreshold current variation with gate-to-source voltage for different channel lengths

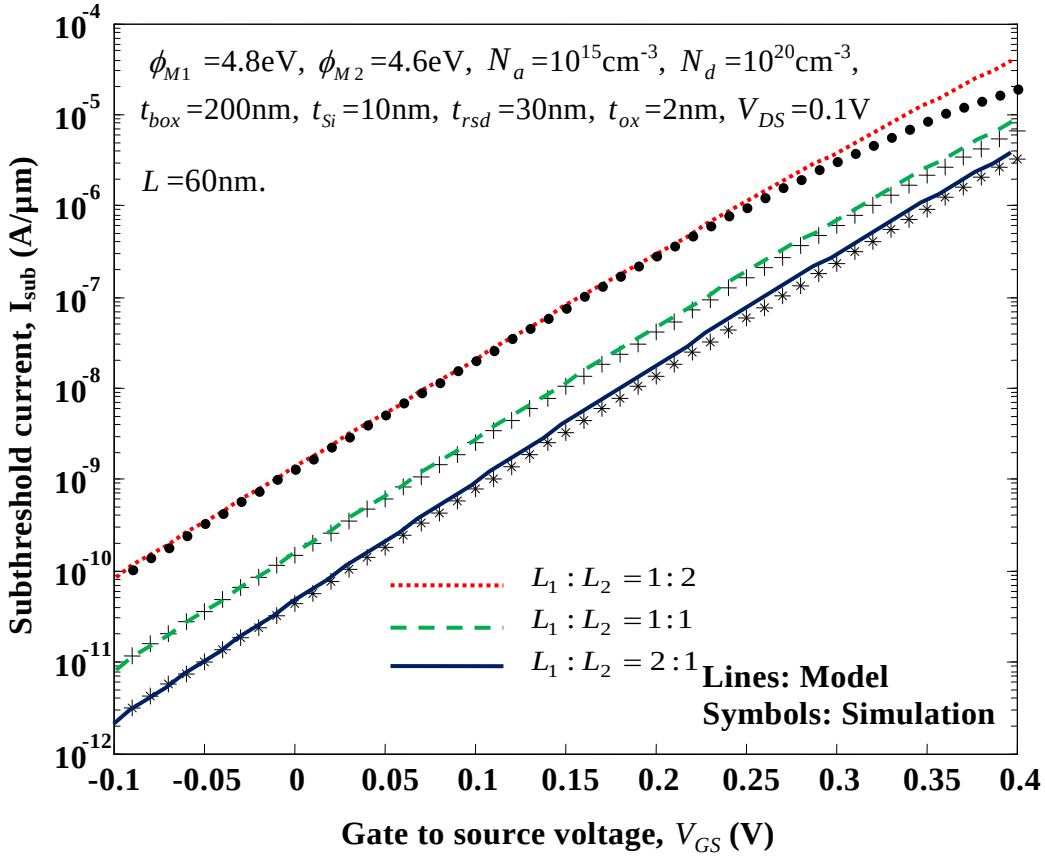


Fig. 3.10: Subthreshold current variation with gate-to-source voltage for different control to screen gate length ratios

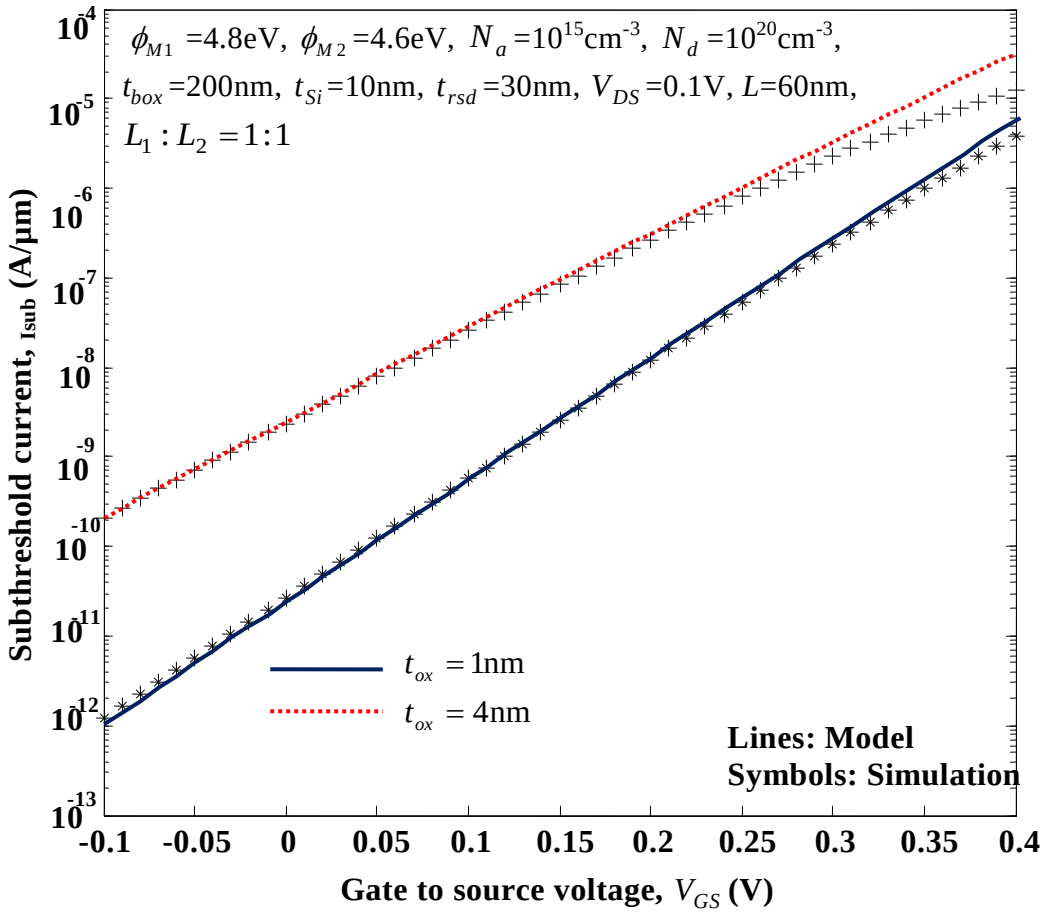


Fig. 3.11: Subthreshold current variation with gate-to-source voltage for different oxide thicknesses

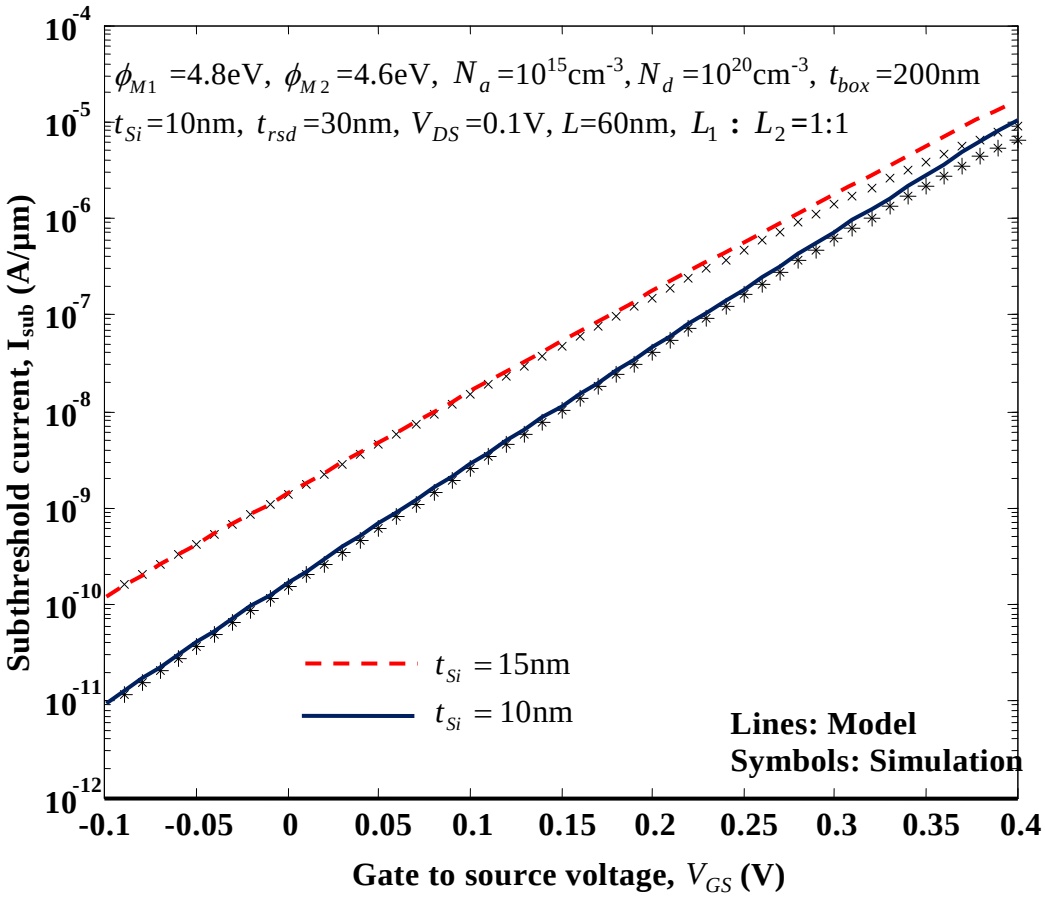


Fig. 3.12: Subthreshold current variation with gate-to-source voltage for different Si film thicknesses

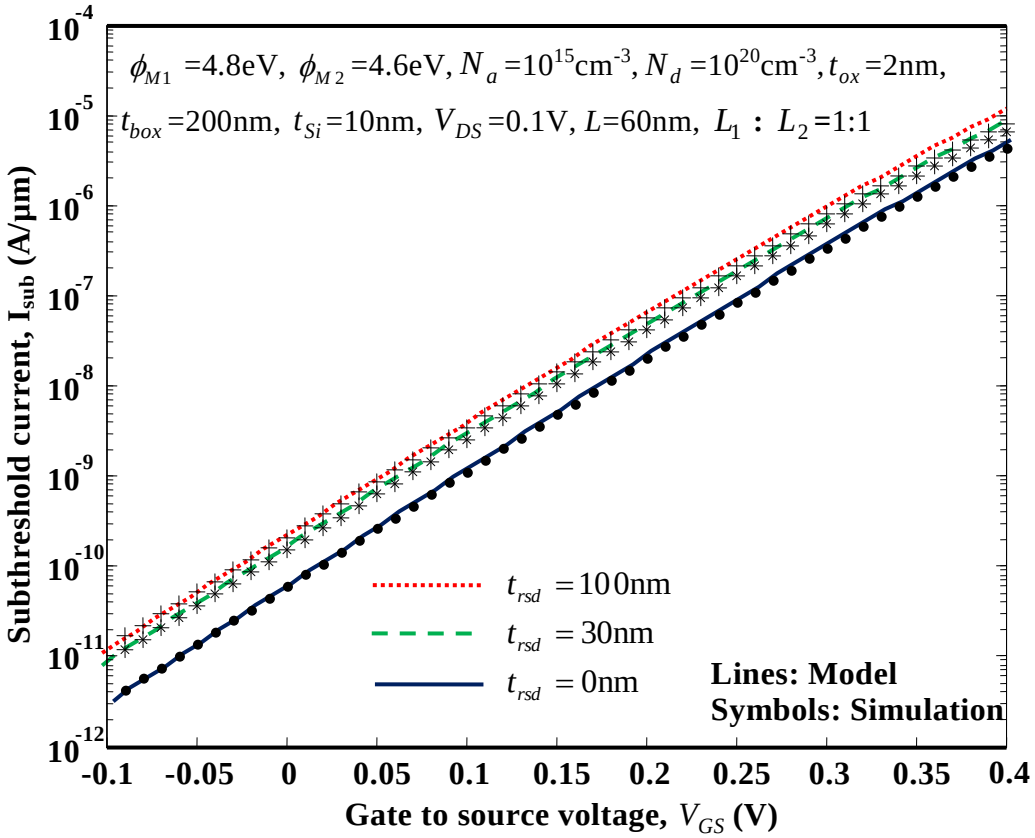


Fig. 3.13: Subthreshold current variation with gate-to-source voltage for different recessed source/drain thicknesses

3.6.4 Subthreshold Swing (*S*)

The results of Fig. 3.9 and Fig. 3.10 are reflected in Fig. 3.14 that demonstrates the subthreshold swing (S) variation against the device channel length (L) for different control to screen gate length ratios (L_1 : L_2). The subthreshold swing is found to be decreased with the increase in the control gate length for a fixed total channel length. The length of the control gate plays important role in determining the device characteristics as devices with longer control gate suffer less with short-channel effects.

The influences of gate oxide thickness and channel thickness on switching characteristics are displayed in Fig. 3.15 and Fig. 3.16 respectively. The subthreshold swing is found to be decreased with the decrease in front-gate oxide thickness and channel thickness for a fixed value channel length. This is due to the fact that a thin

layer of front-gate oxide and silicon channel improves the gate control over the channel by strengthening the vertical electric field across the channel.

Figure 3.17 shows the subthreshold swing variation with the device channel length for different recessed-source/drain thicknesses. It is observed from the figure that the subthreshold swing is found to be increased with increase in recessed-source/drain thickness, which is well expected from the results of Fig. 3.13. In case of $t_{rsd} = 0$ the subthreshold swing is ~ 148mV/Dec., and in case of t_{rsd} =30nm and t_{rsd} =100nm the subthreshold is ~ 160 mV/Dec. and ~ 167 mV/Dec., respectively. This increase is due to back coupling between extended source/drain and back surface of the channel region.

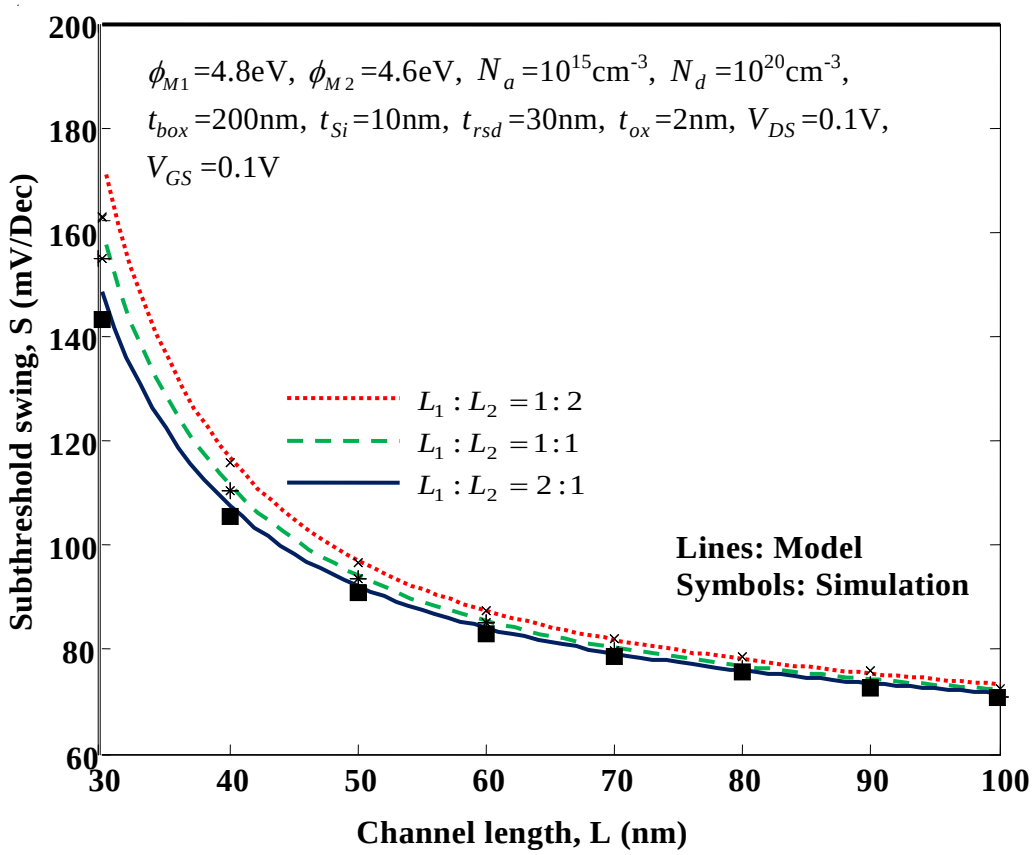


Fig. 3.14: Subthreshold swing variation with device channel length for different control to screen gate length ratios

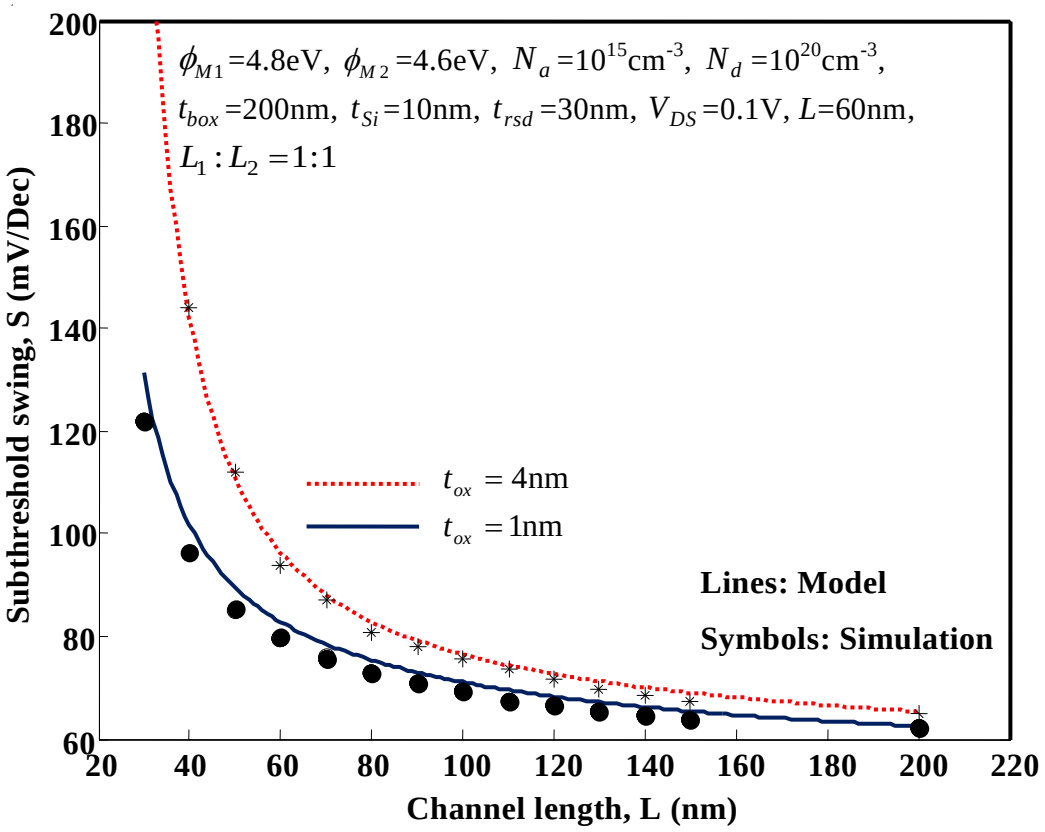


Fig. 3.15: Subthreshold swing variation with device channel length for different oxide thicknesses

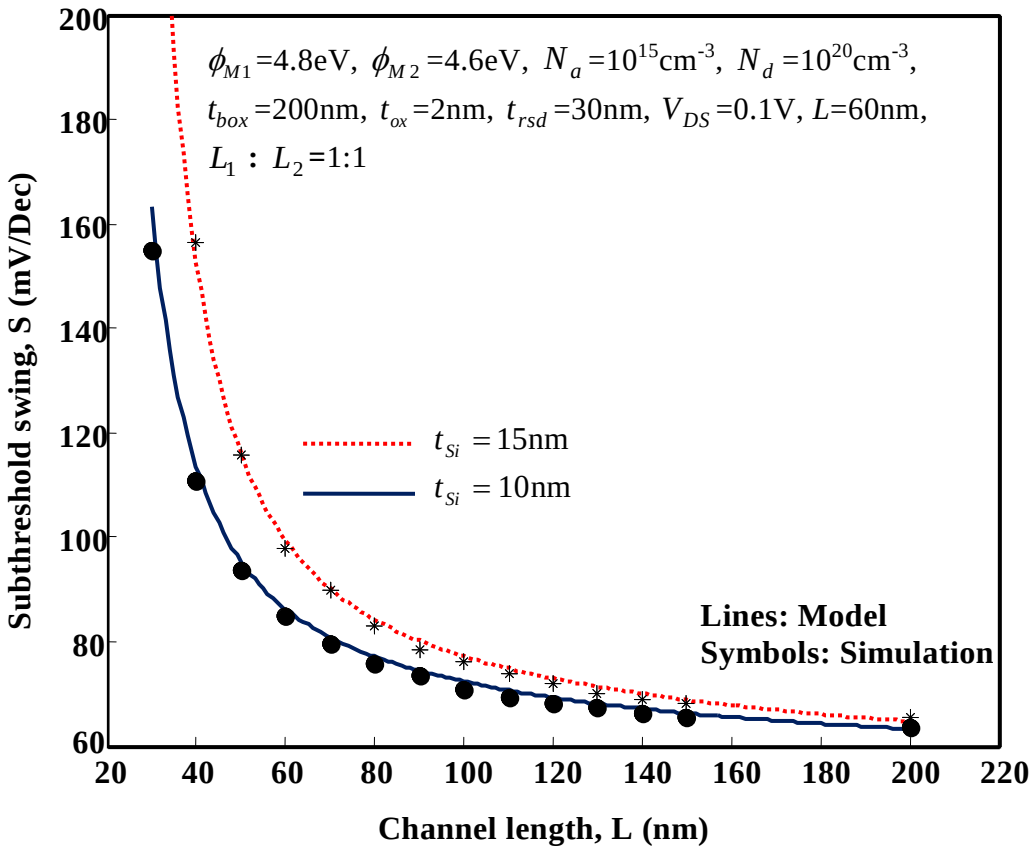


Fig. 3.16: Subthreshold swing variation with device channel length for different Si film thicknesses

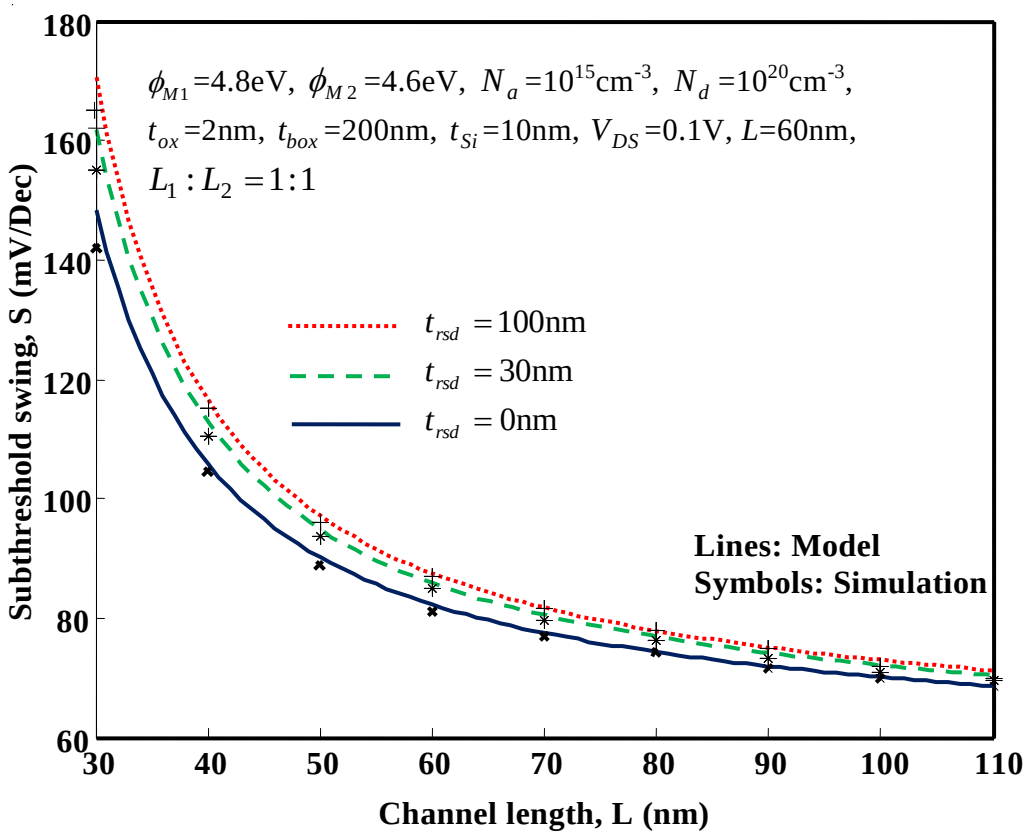


Fig. 3.17: Subthreshold swing variation with device channel length for different recessed source/drain thicknesses

3.7 Summary and Conclusion

Analytical models of threshold voltage, subthreshold current and swing of short-channel dual-metal-gate (DMG) fully-depleted (FD) recessed-source/drain (Re-S/D) SOI MOSFET have been presented in this chapter. An extensive analysis has been carried out to find the impact of the numerous device parameters like gate oxide thickness, Si film thickness, and control gate to screen gate length ratio, and recessed source/drain thicknesses on the threshold voltage, subthreshold current and subthreshold swing characteristics of the device. It is found that in case of a lightly doped short-channel length DMG Re-S/D device, due to a strong electrostatics coupling between source drain and back surface of the channel, inversion occurs at the back channel when gate voltage is increased. Thus, threshold voltage of a Re-S/D SOI MOSFET is that value of the gate voltage at which a conducting channel is formed between source and drain near

the back surface of the channel. Further, it is also concluded that reducing the gate oxide and channel thicknesses effectively curbs down the threshold voltage roll-off. Subthreshold leakage current and swing can also be cut down by selecting thinner gate oxide and silicon film thickness. Thus, the increased threshold voltage roll-off, subthreshold swing and subthreshold current because of recessing source and drain deeper into the BOX can be suppressed by choosing the device parameters judiciously. The control to screen gate length ratio ($L_1 : L_2$) may be an additional controlling parameter which can modulate the subthreshold characteristics of DMG Re-S/D SOI MOSFETs. Further, the ratio $L_1 : L_2$ may be used to optimize the subthreshold behavior of Re-S/D SOI MOSFETs. The proposed models are very general in nature and can predict the subthreshold characteristics of a number of devices including conventional SOI MOSFET (with t_{rsd}=0 and L_2=0), DMG SOI MOSGET with (t_{rsd}=0), Re-S/D SOI MOSFET (with L_2=0) and DMG Re-S/D SOI MOSFETs. The proposed model results are in good agreement with the simulation data obtained by using the commercially available ATLAS^{TM} device simulation software from SILVACO.

Chapter 4

Analytical Modeling and Simulation of Subthreshold Characteristics of Short-Channel Fully-Depleted Recessed-Source/Drain SOI MOSFET with High-*k* Gate-Dielectric Material

4.1 Introduction

The SOI MOSFET is a highly scalable structure. However, an ultra-thin gate oxide (SiO_2) with thickness t_{ox} < 1nm is needed to curb the short-channel effects if the device channel length is scaled down below 32nm [Takeda *et al.* (2010), Ranuarez *et al.* (2006), Chnag *et al.* (2002)]. An ultra-thin gate oxide of thickness less than 1nm causes huge gate-leakage current because of quantum-mechanical direct tunneling of carriers through the gate oxide [Keyes *et al.* (2005), Koh *et al.* (2001)]. Therefore, it has been tried to find out some suitable high-*k* gate-dielectrics with higher physical and lower electrical thickness in order to control both short-channel effects and gate-leakage current simultaneously. HfO_2 (relative permittivity ε_k =22), ZrO_2 (ε_k =25), Ta_2O_5 (ε_k =26) and La_2O_3 (ε_k =27) are found to be showing excellent performance with high permittivity and energy gap [Tripathi *et al.* (2012), Wilk *et al.* (2001)].

It is observed from Chapter 2 that no significant theoretical work has been reported so far in the literature regarding the subthreshold characteristics of the Re-S/D SOI MOSFET with high-*k* gate-dielectric material. Keeping the above facts in view, an attempt has been made in this chapter to present a theoretical and simulation based

study of the potential distribution, threshold voltage, subthreshold swing and subthreshold current of the Re-S/D SOI MOSFETs with high-*k* gate-dielectric material considering the impact of fringing fields. The layout of the present chapter is outlined as follows.

In section 4.2, the 2D surface potential function of the short-channel FD Re-S/D SOI MOSFET device with high-*k* gate-dielectric material is derived by solving the 2D Poisson's equation using the parabolic approximation method. Section 4.3 presents the analytical threshold voltage modeling of the device. The analytical subthreshold current and subthreshold swing models are developed in sections 4.4 and 4.5 respectively. Results and discussion related to the developed models are presented in section 4.6. Finally, the summary and conclusion of the present chapter are presented in section 4.7.

4.2 Modeling of Two-Dimensional (2D) Surface Potential

This section presents the modeling of subthreshold characteristics of Re-S/D UTB SOI MOSFET with high-*k* gate-dielectric material. The schematic structure of the Re-S/D UTB SOI MOSFET device with high-*k* gate-dielectric material used in our modeling and simulation is shown in Fig.4.1. Here, L, W, t_{Si}, t_{gt}, t_{sp}, t_k, t_{box}, t_{rsd} and d_{box} are the gate length, gate width along z axis , channel thickness, thickness of gate, thickness of spacer, gate-dielectric thickness, buried-oxide (BOX) thickness, source/drain penetration in the BOX and length of source/drain overlap over the BOX, respectively. The other parameters used in the analysis of the device of Fig. 4.1 are considered same as those in Fig. 3.1. of Chapter 3. The symbols and values of all the parameters used in modeling and simulation are detailed in Table 4.1.

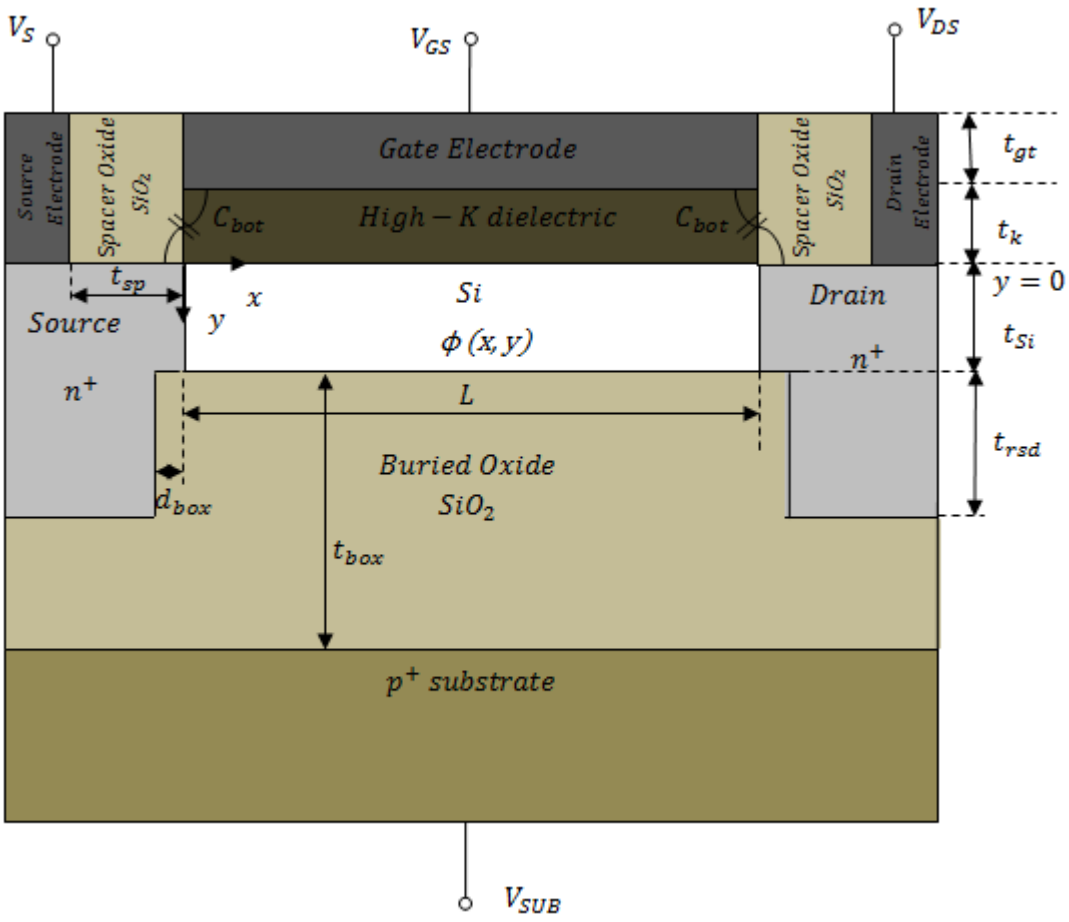


Fig. 4.1: The schematic structure of the Re-S/D FD SOI MOSFET showing the internal parasitic fringe capacitance

Parameters	Symbol	Values
Gate work-function	ϕ_M	4.6, 4.8eV
Channel Doping	N_a	10^{15}cm^{-3}
Source/Drain Doping	N_d	10^{20}cm^{-3}
Substrate Doping	N_{sub}	10^{18}cm^{-3}
Silicon Thickness	t_{Si}	5-8nm
Physical Gate-Dielectric Thickness	t_k	1.5-15nm
Effective Oxide Thickness	t_{ox}	1.5-3nm
Buried-Oxide Thickness	t_{box}	100-200nm
The depth of S/D in the Buried-Oxide	t_{rsd}	30, 100nm
Gate-Thickness	t_{gt}	25nm
Gate-Dielectric Constant	ε_k	3.9, 12, 22, 27
Thickness of the Spacer	t_{sp}	25nm
Gate Width	W	1μm
Length of S/D Overlap	d_{box}	3nm
Channel Length	L	20-300nm
Gate Voltage	V_{GS}	0.1V
Drain Voltage	V_{DS}	0.1V
Substrate Voltage	V_{sub}	-3.0 to 1V

Table 4.1: Device parameter values used for modeling and simulation of Re-S/D FD SOI MOSFET with high-k gate-dielectric material

In the subthrehold regime of the device operation, the 2D Poisson's equation in the channel region of the device, shown in Fig. 4.1, can be written as follows [Young *et al.* (1989)]

$$\frac{\partial^2\phi(x,y)}{\partial x^2}+\frac{\partial^2\phi(x,y)}{\partial y^2}=\frac{qN_a}{\varepsilon_{Si}} \tag{4.1}$$

where, $\phi(x,y)$ is the channel potential and ε_{Si} is permittivity of silicon.

The potential profile in the vertical direction in the channel can be approximated by the following parabolic function [Young *et al.* (1989)]

$$\phi(x,y)=\phi_f(x)+C_1(x)y+C_2(x)y^2 \tag{4.2}$$

The coefficients $C_1(x)$ and $C_2(x)$ are the functions of x only, and $\phi_f(x)=\phi(x,0)$ is the surface potential at gate-dielectric/Si interface. These coefficients are to be determined using the following boundary conditions:

The continuity of electric flux at gate-dielectric/Si interface is as [Svilicic *et al.* (2009)]:

$$\left[\frac{\partial\phi(x,y)}{\partial y}\right]_{y=0}=\frac{C_k}{\varepsilon_{Si}}\frac{\phi_f(x)-(V_{GS}-V_{FB1})}{L} \tag{4.3}$$

The electric flux at Si/BOX interface is also continuous and is given as [Svilicic *et al.* (2009)]:

$$\left[\frac{\partial\phi(x,y)}{\partial y}\right]_{y=t_{Si}}=\frac{C_{rsd}}{\varepsilon_{Si}}\frac{V_S-V_{FB2}-\phi_b(x)}{L}+\frac{C_{rsd}}{\varepsilon_{Si}}\frac{V_D-V_{FB2}-\phi_b(x)}{L}+\frac{C_{box}}{\varepsilon_{Si}}\frac{V_{sub}-V_{FB3}-\phi_b(x)}{L} \tag{4.4}$$

N_d is the source/drain doping concentration, n_i is the intrinsic carrier concentration in the silicon, V_{FB1}, V_{FB2} and V_{FB3} are the gate-front channel flat-band voltage, source/drain-back channel flat-band voltage and substrate-back channel flat-band voltage, respectively and are given by

$$V_{FB1}=\phi_M-\phi_{Si} \tag{4.5}$$

$$V_{FB2}=\frac{kT}{q}\ln\left(\frac{N_aN_d}{n_i^2}\right) \tag{4.6}$$

$$V_{FB3}=\frac{kT}{q}\ln\left(\frac{N_{sub}}{N_a}\right) \tag{4.7}$$

where, ϕ_M is the gate work function, $\phi_{Si}=\chi_{Si}+E_g/2+V_T\ln\left(\frac{N_a}{n_i}\right)$, χ_{Si} and E_g are the electron affinity and energy band gap of the silicon, respectively, and V_T is the thermal

voltage; V_D and V_{GS} are the drain and gate to source bias-voltages, respectively; The potential at channel-BOX interface is $\phi_b(x)=\phi_b(x, y=t_{Si})$, which is named as back surface potential. The symbol V_{sub} refers to the substrate bias voltage.

C_k is the front-channel gate-dielectric capacitance per unit length and it is given by

$$C_k = \frac{\varepsilon_k L}{t_k} \tag{4.8}$$

C_{Si} is the silicon channel capacitance per unit length and it is given by

$$C_{Si} = \frac{\varepsilon_{Si} L}{t_{Si}} \tag{4.9}$$

C_{box} is the buried-oxide capacitance per unit length and it is given by

$$C_{box} = \frac{\varepsilon_{ox} L}{t_{box}} \tag{4.10}$$

C_{rsd} is the recessed-source/drain buried-oxide capacitance per unit length and it is given by [Svilicic et al. (2009)]

$$C_{rsd} = \begin{cases} \dfrac{\varepsilon_{box}}{\theta} \ln\left(1+\dfrac{L}{2d_{box}}\right) for \dfrac{L}{2} < t_{rsd} \\ \dfrac{\varepsilon_{box}}{\theta} \ln\left(1+\dfrac{t_{rsd}}{2d_{box}}\right) for \dfrac{L}{2} > t_{rsd}, t_{rsd} = 0 \end{cases} \tag{4.11}$$

where, d_{box} is the length of source/drain overlap over buried-oxide which should be greater than zero, θ is the effective angle between the two slanted electrodes: channel back-side and source/drain extension; $\theta = \left(\frac{\pi}{2} + \frac{\pi}{2}.\sec h \frac{t_{rsd}}{d_{box}}\right)$, From this equation it can be noticed that θ varies from $\frac{\pi}{2}$ for the Re-S/D SOI MOSFETs to π for the conventional SOI MOSFETs ($t_{rsd} = 0$).

The surface potential at the source end is

$$\phi(0,y)=V_{bi} \tag{4.12}$$

whereas, the surface potential at the drain end is

$$\phi(L,y)=V_{bi}+V_{DS} \tag{4.13}$$

where, V_{bi} is the built-in voltage at the source/drain and Si interface given by $V_{bi}=\frac{kT}{q}ln\left(\frac{N_aN_d}{n_i^2}\right)$,

Now, the coefficients $C_1(x)$and $C_2(x)$ of Eq. (4.2) are determined using the boundary conditions Eq. (4.3) and (4.4) as

$$C_1(x)=\frac{C_k}{t_{Si}.C_{Si}}\left[\phi_f(x)-(V_G-V_{FB1})\right] \tag{4.14}$$

$$C_2(x)=\frac{1}{2t_{Si}{}^2.}\left\{\frac{C_{rsd}}{C_{Si}}\left[V_{DS}-2V_{FB2}-\phi_b(x)\right]+\frac{C_{box}}{.C_{Si}}\left[V_{sub}-V_{FB3}-\phi_b(x)\right]+\frac{C_k}{.C_{Si}}\left[\phi_f(x)-(V_G-V_{FB1})\right]\right\} \tag{4.15}$$

Now, using $C_1(x)$and $C_2(x)$ of Eqs. (4.14) and (4.15) in Eq. (4.2), gives the following equation of 2D channel potential

$$\phi(x,y)=\phi_f(x)+\frac{C_k}{t_{Si}.C_{Si}}\left[\phi_f(x)-(V_G-V_{FB1})\right]y+\frac{1}{2t_{Si}{}^2.}\left\{\frac{C_{rsd}}{C_{Si}}\left[V_{DS}-2V_{FB2}-\phi_b(x)\right]+\frac{C_{box}}{.C_{Si}}\left[V_{sub}-V_{FB3}-\phi_b(x)\right]+\frac{C_k}{.C_{Si}}\left[\phi_f(x)-(V_G-V_{FB1})\right]\right\}y^2 \tag{4.16}$$

Further, the following two differential equations for $\phi_{f,b}$ have been obtained using $\phi(x,y)$ of Eq. (4.16) in Eq. (4.1) at $y=0$ and $y=t_{Si}$ respectively,

$$\frac{d^2\phi_{f,b}(x)}{dx^2} - \alpha_{f,b}\phi_{f,b}(x) = \beta_{f,b} \tag{4.17}$$

where,

$$\alpha_f = 2\frac{1+\left(\frac{C_k\left(C_{Si}+2C_{rsd}+C_{box}\right)}{C_{Si}\left(2C_{rsd}+C_k\right)}\right)}{t_{Si}^2\left(1+2\frac{C_{Si}}{2C_{rsd}+C_k}\right)} \tag{4.18}$$

$$\beta_f = \frac{qN_a}{\varepsilon_{Si}} - 2\frac{\left[\left(V_{GS}-V_{FB1}\right)\left(\frac{C_k\left(C_{Si}+2C_{rsd}+C_{box}\right)}{C_{Si}\left(2C_{rsd}+C_k\right)}\right)+\left(V_{DS}-2V_{FB2}\right)\left(\frac{2C_{rsd}}{2C_{rsd}+C_{box}}\right)\right)}{t_{Si}^2\left(1+2\frac{C_{Si}}{2C_{rsd}+C_k}\right)} \tag{4.19}$$

$$\alpha_b = 2\frac{1+\left(\frac{\left(C_k+C_{Si}\right)\left(2C_{rsd}+C_{box}\right)}{C_kC_{Si}}\right)}{t_{Si}^2\left(1+2\frac{C_{Si}}{C_k}\right)} \tag{4.20}$$

$$\beta_b = \frac{qN_a}{\varepsilon_{Si}} - 2\frac{\left(V_{GS}-V_{FB1}\right)+\left(V_{DS}-2V_{FB2}\right)\left(\frac{C_{rsd}}{C_k}+\frac{C_{rsd}}{C_{Si}}\right)+\left(V_{sub}-V_{FB3}\right)}{t_{Si}^2\left(1+2\frac{C_{Si}}{C_k}\right)} \tag{4.21}$$

By solving the second-order non-homogenous differential equation (4.17), the following expression which is front- and back- surface potential distribution along the channel is obtained

$$\phi_{f,b} = A_{f,b}.e^{\sqrt{\alpha_{f,b}}x} + B_{f,b}.e^{-\sqrt{\alpha_{f,b}}x} - \frac{\beta_{f,b}}{\alpha_{f,b}} \tag{4.22}$$

Now, the boundary conditions of Eqs. (4.12) and (4.13) can be used to determine the coefficients $A_{f,b}$ and $B_{f,b}$ of Eq. (4.22).

where ,

$$A_{f,b} = \frac{\beta_{f,b}\left(e^{\sqrt{\alpha_{f,b}}L} - 1\right) + \alpha_{f,b}\left[V_{bi}\left(e^{\sqrt{\alpha_{f,b}}L} - 1\right) + V_{DS}e^{\sqrt{\alpha_{f,b}}L}\right]}{\alpha_{f,b}\left(e^{2\sqrt{\alpha_{f,b}}L} - 1\right)} \tag{4.23}$$

$$B_{f,b} = \frac{e^{\sqrt{\alpha_{f,b}}L}\left\{\beta_{f,b}\left(e^{\sqrt{\alpha_{f,b}}L} - 1\right) - \alpha_{f,b}\left[V_{bi}\left(1 - e^{\sqrt{\alpha_{f,b}}L}\right) + V_{DS}\right]\right\}}{\alpha_{f,b}\left(e^{2\sqrt{\alpha_{f,b}}L} - 1\right)} \tag{4.24}$$

The positions $\left(x_{min}\right)_{f,b}$ of the front- and back- channel minimum surface potentials (virtual cathode potential, $\phi_{f\min,b\min}$ [Svilicic *et al.* (2009)] can be obtained by solving $\left.\frac{d\phi_{f,b}(x)}{dx}\right|_{(x_{\min})_{f,b}} = 0$ and are determined as

$$\left(x_{\min}\right)_{f,b} = \frac{1}{2}\frac{\ln\left(\frac{B_{f,b}}{A_{f,b}}\right)}{\sqrt{\alpha_{f,b}}} \tag{4.25}$$

The minimum of front- and back- surface potential $\phi_{f\min,b\min}$ could be obtained by substituting $\left(x_{min}\right)_{f,b}$ of Eq. (4.25) into Eq. (4.22) as

$$\phi_{f\min,b\min} = 2\sqrt{A_{f,b}B_{f,b}} - \frac{\beta_{f,b}}{\alpha_{f,b}} \tag{4.26}$$

Further, in order to obtain the surface potential equations including the effect of the fringe capacitance C_{bot}, the potentials $V\left(x,\sigma_1\right)\big|_{source}$ and $V\left(L-x,\sigma_2\right)\big|_{drain}$ due to the induced charges on the source and drain regions, respectively, are added to surface potential $\phi_{f,b}$ and the expression for surface potential of Eq. (4.22) is modified as

$$\phi_{f,b} = A_{f,b}.e^{\sqrt{\alpha_{f,b}}x} + B_{f,b}.e^{-\sqrt{\alpha_{f,b}}x} - \frac{\beta_{f,b}}{\alpha_{f,b}} + \left(V(x,\sigma_1)\big|_{source} + V\left(L-x,\sigma_2\right)\big|_{drain}\right) \tag{4.27}$$

The origin and derivation of potential $V\left(x,\sigma_{1,2}\right)$and fringe capacitance C_{bot} are discussed in section 4.2.1

Now, the modified minimum of front- and back- surface potential could be obtained using Eq. (4.27). However, the direct derivative of Eq. (4.27) may lead us to a very complicated equation of $(x_{min})_{f,b}$ and which in turn gives an implicit equation for threshold voltage. Therefore, assuming that first two terms are varying more rapidly compared to the last two, and the last two terms only modify the minimum values of $\phi_{f\min,b\min}$, following equations for the modified minimum front- and back- surface potential can be obtained as

$$\phi'_{f\min,b\min} = 2\sqrt{A_{f,b}B_{f,b}} - \frac{\beta_{f,b}}{\alpha_{f,b}} + \left(V(x,\sigma_1)\big|_{source} + V(L-x,\sigma_2)\big|_{drain}\right)\Big|_{x=(x_{\min})_{f,b}} \tag{4.28}$$

Now, we derive the following equation of the so-called virtual cathode potential $\phi_{vc}(y)$ [Chen *et al.* (2003)] ($\phi_{vc}(y) = \phi_1(x,y)\big|_{x=(x_{\min})_{f,b}}$,where $x = (x_{\min})_{f,b}$ is the position where minima of front-/back-surface potential exists). The obtained virtual cathode potential $\phi_{vc}(y)$which is a function of the minimum value of the front- surface potential is

$$\begin{aligned}\phi_{vc}(y) = \phi'_{f\min}&\left[1 + \frac{C_k}{C_{Si}t_{Si}}y - \frac{C_k}{C_{Si}t_{Si}^{\,2}}y^2 - (2C_{Si}+C_k)z_1y^2\right]\\ &+ (V_{GS}-V_{FB1})\left[-\frac{C_k}{C_{Si}t_{Si}}y + \frac{C_k}{2C_{Si}t_{Si}^{\,2}}y^2 - (C_k)z_1y^2\right]\\ &+ (V_{DS}-2V_{FB2})\left[\frac{C_{rsd}}{2C_{Si}t_{Si}^{\,2}}y^2 + (C_{rsd})z_1y^2\right]\\ &+ (V_{sub}-V_{FB4})\left[\frac{C_{box}}{2C_{Si}t_{Si}^{\,2}}y^2 + (C_{box})z_1y^2\right]\end{aligned} \tag{4.29}$$

where, $z_1 = \left(\frac{2C_{rsd}+C_{box1}}{2C_{Si1}t_{Si}^{\,2}(2C_{Si}+2C_{rsd}+C_{box})}\right)$ (4.30)

Similarly, another equation of the so-called virtual cathode potential which is a function of the minimum value of the back surface potential can also be obtained

$$\begin{aligned}\phi_{vc}(y) = \phi'_{b\min}&\left[\left(\frac{2C_{Si}+2C_{rsd}+C_{box}}{2C_{Si}+C_k}\right)z_2-\left(\frac{C_{rsd}}{C_{Si1}{t_{Si}}^2}+\frac{C_{box}}{2C_{Si1}{t_{Si}}^2}\right)y^2\right]\\&+(V_{GS}-V_{FB1})\left[-\frac{C_k}{C_{Si}t_{Si}}y+\frac{C_k}{C_{Si}{t_{Si}}^2}y^2+\left(\frac{C_k}{2C_{Si}+C_k}\right)z_2\right]\\&+(V_{DS}-2V_{FB2})\left[\frac{C_{rsd}}{C_{Si1}{t_{Si}}^2}y^2-\left(\frac{C_{rsd}}{2C_{Si}+C_k}\right)z_2\right]\\&+(V_{sub}-V_{FB3})\left[\frac{C_{box}}{C_{Si}{t_{Si}}^2}y^2-\left(\frac{C_{box}}{2C_{Si}+C_k}\right)z_2\right]\end{aligned} \tag{4.31}$$

where, $z_2=\left(1+\frac{C_k}{C_{Si}t_{Si}}y-\frac{C_k}{2C_{Si}{t_{Si}}^2}y^2\right)$ (4.32)

Here, it should be noted that either of Eqs. (4.29) or (4.31) can be utilized for the formulation of the subthreshold charge carrier density at virtual cathode position, as done in Chapter 3.

4.2.1 Derivation of $V(x,\sigma_i)$

The electric field lines that originate from the bottom of the gate and enter into the source and drain through the spacer induce electrostatic charges in source and drain region. The surface charge density, σ_i (i=1 and 2 for source and drain, respectively) due to fringing electric field lines is given as (Fig. 4.2) [Kumar *et al.* (2006)]

$$\sigma_i=\left(\frac{(C_{bot})V_{pi}}{W.t_{sp}}\right)\text{, where } i=1,2 \text{ for source and drain, respectively} \tag{4.33}$$

where, $V_{p1}=V_{bi}-V_{GS}+V_{FB2}$ and $V_{p2}=V_{bi}+V_{DS}-V_{GS}+V_{FB2}$ are the source and drain junction potentials respectively, W is width of the gate along z axis and t_{sp} is the spacer thickness between gate sidewall and source/drain contacts.

Parasitic internal fringe capacitances associated with bottom edge of gate electrode can be calculated as [Kumar *et al.* (2006)]

$$C_{bot} = \frac{(0.3)\varepsilon_{eff} W}{\pi} \tag{4.34}$$

where, $\varepsilon_{eff} = \frac{\varepsilon_k \varepsilon_{sp}^{'}}{\varepsilon_k - \varepsilon_{sp}^{'}} \ln\left(\frac{\varepsilon_k}{\varepsilon_{sp}^{'}}\right), \varepsilon_{sp}^{'} = \left(1 + \frac{t_k}{L}\right)\varepsilon_{sp}$ is the effective permittivity of spacer material, ε_k and ε_{sp} are the permittivity of gate-dielectric and spacer materials respectively, $t_k = t_{ox}\left(\frac{\varepsilon_k}{\varepsilon_{Sio_2}}\right)$ is the physical dielectric thickness, t_{ox} is the effective oxide thickness (EOT), and ε_{Sio_2} is the permittivity of silicon dioxide [Kumar *et al.* (2006)].

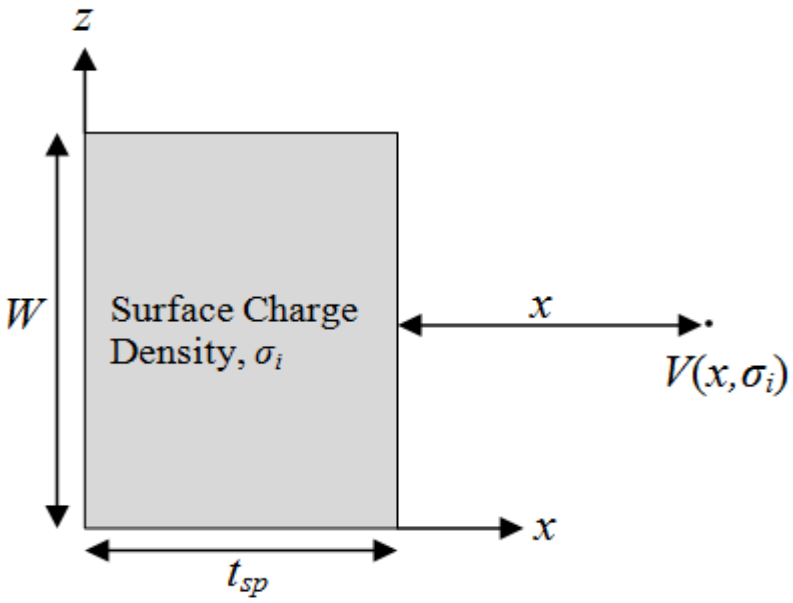


Fig. 4.2: Potential on source and drain due to uniformly charged plate

Now, the potential $V(x,\sigma_i)$ at a distance 'x' from uniformly charged plate as shown in Fig. (4.2) [Kumar *et al.* (2006)]

$$V(x,\sigma_i) = \frac{1}{2}\int_0^{t_{sp}} \int_{-\frac{W}{2}}^{\frac{W}{2}} \frac{\sigma_i dx_1 dx_2}{4\pi\varepsilon_{Si}\sqrt{(x+x_1)^2 + (x_2)^2}} \tag{4.35}$$

By calculating the integral in Eq. (4.35) the expression for $V(x,\sigma_i)$ is obtained as

$$V(x,\sigma_i)=\frac{\sigma_i}{8\pi\varepsilon_{Si}}[U(x)] \tag{4.36}$$

where,

$$U(x)=(x+t_{sp}).ln\left\{\frac{\sqrt{(x+t_{sp})^2+\left(\frac{W^2}{4}\right)}+\left(\frac{W}{2}\right)}{\sqrt{(x+t_{sp})^2+\left(\frac{W^2}{4}\right)}-\left(\frac{W}{2}\right)}\right\}-x.ln\left\{\frac{\sqrt{x^2+\left(\frac{W^2}{4}\right)}+\left(\frac{W}{2}\right)}{\sqrt{x^2+\left(\frac{W^2}{4}\right)}-\left(\frac{W}{2}\right)}\right\}$$
$$+W.ln\left\{\frac{\sqrt{x^2+\left(\frac{W^2}{4}\right)}+t_{sp}+\sqrt{x^2+{t_{sp}}^2+2t_{sp}\sqrt{x^2+\left(\frac{W^2}{4}\right)}}}{\sqrt{x^2+\left(\frac{W^2}{4}\right)}+x}\right\} \tag{4.37}$$

4.3 Threshold Voltage Formulation

The threshold voltage associated with front surface and back surface of the channel could be obtained using [Chen *et al.* (2003)]

$$\phi'_{f\min,b\min}\Big|_{V_G=V_{thf,b,}}=2\phi^*{}_{f,Si}=\begin{cases}2\phi_{f,Si} & for, N_a>n_T\\ \phi_{f,Si}+\frac{kT}{q}\ln\left(\frac{n_T}{n_i}\right) & for, N_a<n_T\end{cases} \tag{4.38}$$

where, q is the electron charge, N_a is the channel doping concentration, n_i is the intrinsic carrier concentration, k is the Boltzmann's constant, and T is the temperature, $\phi_{f,Si}$ is the Fermi potential, n_T is a critical concentration of electrons in channel to turn on the device [Chen *et al.* (2003)]. However, the critical concentration, n_T depends on device parameters like channel thickness and channel length and it has been obtained by following the method of Chen [Chen *et al.* (2003)].

Now, after using Eq. (4.38) in Eq. (4.28), we get the following equations for front and back channel-surface threshold voltages $V_{thf,b}$

$$V_{thf,b}=\frac{-b_{f,b}+\sqrt{{b_{f,b}}^2-4a_{f,b}c_{f,b}}}{2a_{f,b}} \tag{4.39}$$

where,

$$a_{f,b} = u_{f1,b1}u_{f2,b2} - \left(\frac{m'_{f,b}}{2\alpha_{f,b}}\right)^2 \tag{4.40}$$

$$c_{f,b} = v_{f1,b1}v_{f2,b2} - \phi_{f,Si}{}^2 - \left(\frac{n'_{f,b}}{2\alpha_{f,b}}\right)^2 - \frac{n'_{f,b}}{\alpha_{f,b}}\ \phi_{f,Si} \tag{4.41}$$

$$b_{f,b} = u_{f1,b1}v_{f2,b2} + u_{f2,b2}v_{f1,b1} - \frac{m'_{f,b}n'_{f,b}}{2\alpha_{f,b}{}^2} - \frac{m'_{f,b}}{\alpha_{f,b}}\phi_{f,Si} \tag{4.42}$$

$$v_{f1,b1} = \frac{n'_{f,b}\left(e^{\sqrt{\alpha_{f,b}}L} - 1\right) + \alpha_{f,b}\left[V_{bi}\left(e^{\sqrt{\alpha_{f,b}}L} - 1\right) + V_{DS}e^{\sqrt{\alpha_{f,b}}L}\right]}{\alpha_{f,b}\left(e^{2\sqrt{\alpha_{f,b}}L} - 1\right)} \tag{4.43}$$

$$v_{f2,b2} = \frac{e^{\sqrt{\alpha_{f,b}}L}\left\{n'_{f,b}\left(e^{\sqrt{\alpha_{f,b}}L} - 1\right) - \alpha_{f,b}\left[V_{bi}\left(1 - e^{\sqrt{\alpha_{f,b}}L}\right) + V_{DS}\right]\right\}}{\alpha_{f,b}\left(e^{2\sqrt{\alpha_{f,b}}L} - 1\right)} \tag{4.44}$$

$$u_{f1,b1} = \frac{m'_{f,b}\left(e^{\sqrt{\alpha_{f,b}}L} - 1\right)}{\alpha_{f,b}\left(e^{2\sqrt{\alpha_{f,b}}L} - 1\right)} \tag{4.45}$$

$$u_{f2,b2} = \frac{m'_{f,b}e^{\sqrt{\alpha_{f,b}}L}\left(e^{\sqrt{\alpha_{f,b}}L} - 1\right)}{\alpha_{f,b}\left(e^{2\sqrt{\alpha_{f,b}}L} - 1\right)} \tag{4.46}$$

$$m'_{f,b} = m_{f,b} + P_1\alpha_{f,b} \tag{4.47}$$

$$n'_{f,b} = n_{f,b} + P_2\alpha_{f,b} \tag{4.48}$$

$$\beta_{f,b} = m_{f,b}V_{GS} + n_{f,b} \tag{4.49}$$

$$U(x)\big|_{x=x_{min}} + U(x)\big|_{x=L-x_{min}} = P_1V_{GS} + P_2 \tag{4.50}$$

where, P_1 and P_2 are the constants which can be obtained by rearranging the expression $U(x)\big|_{x=x_{min}} + U(x)\big|_{x=L-x_{min}}$

Here, it should be noted that in Re-S/D SOI MOSFETs, the position of inversion layer depends on the device parameters such as channel doping, recessed-source/drain

thickness and channel length as discussed in Chapter 3. Thus, the threshold voltage V_{th} of Re-S/D SOI MOSFETs with high-*k* gate-dielectric material could be given as follows [Kumar *et al.* (2014)]

$$V_{th} = \begin{cases} V_{thf}, & \text{for} \quad \phi_{\text{f,min}} > \phi_{\text{b,min}} \\ V_{thb}, & \text{for} \quad \phi_{\text{f,min}} < \phi_{\text{b,min}} \end{cases} . \tag{4.51}$$

Further, the following quantum effects induced correction term ΔV_{th} is added in the threshold voltage model of Eq. (4.51) [Dort *et al.* (1992)].

$$\Delta V_{th} = \Delta E_0 \left(1 + \frac{\varepsilon_{Si} t'_{ox}}{\varepsilon_k t_{Si} + \varepsilon_{Si} t_{box}} \right) \tag{4.52}$$

where, h is the planks constant, m^* is effective mass of the electron, ΔE_0 can be found out using Eq. (3.98) of Chapter 3.

4.4 Subthreshold Current Formulation

By assuming that the diffusion is the dominant current flow mechanism in the weak inversion regime [Dey *et al.* (2008)], the subthreshold current can be modeled by using the concept of effective channel length. Thus, the expression of subthreshold current density can be written as [Dey *et al.* (2008)]:

$$J_n(y) = \frac{qD_n n_{\min}(y)}{L_e} \left(1 - \exp\left(-\frac{V_{DS}}{V_T} \right) \right) \tag{4.53}$$

D_n is the coefficient of diffusion, L_e is the effective channel length [Dey at al. (2008)], V_T is the thermal voltage. The electron density at the virtual cathode, $n_{\min}(y)$ can be expressed as [Yeh *et al.* (1995), Dey at al. (2008)]

$$n_{min}(y) = \frac{n_i^2}{N_a} exp\left(\frac{\phi_{vc}(y_m)}{V_T} \right) \tag{4.54}$$

where, $\phi_{vc}(y_m)=\phi_{vc}(y)$ is the value of the minimum surface potential function along the channel thickness at $y = y_m$, where y_m can be obtained by solving $\frac{\partial \phi_{vc}(y)}{\partial y} = 0$ and $\phi_{vc}(y_m) = \phi_{vc}(y)\big|_{y=y_m}$

The subthreshold current, I_{sub} can be obtained by integrating Eqn. (4.53) along the silicon film, i.e., from 0 to t_{Si}, as done in Chapter 3.

$$I_{sub} = \int_0^{t_{Si}} J_n(y)dy = \int_0^{t_{Si}} \frac{qD_n n_i^2}{L_e N_a} \exp\left(\frac{\phi_{vc}(y)}{V_T}\right)\left(1-\exp\left(-\frac{V_{DS}}{V_T}\right)\right)dy \tag{4.53}$$

$$I_{sub} = K\int_0^{t_{Si}} \exp\left(\frac{\phi_{vc}(y)}{V_T}\right)dy \tag{4.54}$$

where, $K = \frac{qD_n n_i^2}{L_e N_a}\left(1-\exp\left(-\frac{V_{DS}}{V_T}\right)\right)$ (4.55)

By following the method which is given in section 3.4 of Chapter 3, the above equation has been solved and the obtained final subthreshold current expression is

$$I_{sub} = KV_T\left[\frac{\exp\left(\frac{\phi_{vc}(y=0)}{V_T}\right)-\exp\left(\frac{\phi_{vc}(y=y_m)}{V_T}\right)}{(\phi_{vc}(y=0)-\phi_{vc}(y=y_m))/y_m}\right.$$
$$\left.+\frac{\exp\left(\frac{\phi_{vc}(y=y_m)}{V_T}\right)-\exp\left(\frac{\phi_{vc}(y=t_{Si})}{V_T}\right)}{(\phi_{vc}(y=y_m)-\phi_{vc}(y=t_{Si}))/(t_{Si}-y_m)}\right] \tag{4.56}$$

4.5 Subthreshold Swing Formulation

The subthreshold slope (*S*) of a Re-S/D SOI MOSFET is defined as the reciprocal of the slope of the subthreshold characteristic curve representing the variation of $\log(I_D)$ as a

function of the gate voltage, V_G, where, I_D is the drain current in the subthreshold regime of operation of the device. Thus, the subthreshold swing, *S* of the Re-S/D SOI MOSFET can be written as [Dey *et al.* (2008), Svilicic *et al.* (2010)]

$$S = \begin{cases} V_T(\ln 10) \times \left(\dfrac{d\phi'_{f\min}}{dV_{GS}} \right)^{-1} & for\, \phi'_{f\min} > \phi'_{b\min} \\ V_T(\ln 10) \times \left(\dfrac{d\phi'_{b\min}}{dV_{GS}} \right)^{-1} & for\, \phi'_{b\min} > \phi'_{f\min} \end{cases} \tag{4.57}$$

By substituting the Eq. (4.28) in Eq. (4.57) the following closed form expression of the subthreshold swing of the Re-S/D UTB SOI MOSFET with high-*k* gate-dielectric material is obtained as

$$S = \begin{cases} V_T(ln10) \times \left[\left(1 + \dfrac{C_{Si}\left(2C_{rsd} + C_{box}\right)}{C_K\left(C_{Si} + 2C_{rsd} + C_{box}\right)} \right) \left(\dfrac{1 + e^{\sqrt{\alpha_f} L}}{1 + e^{\sqrt{\alpha_f} L} - e^{\sqrt{\alpha_f} x_{min,f}} - e^{\sqrt{\alpha_f}\left(L - x_{min,f}\right)}} \right) - \dfrac{C_{bot}}{Wt_{sp} 8\pi\varepsilon_{Si}} \left(U_S + U_D\right) \right]^{-1} \\ \qquad for\, \phi'_{f\,min} > \phi'_{b\,min} \\ V_T(ln10) \times \left(\left(1 + \dfrac{\left(C_K + C_{Si}\right)\left(2C_{rsd} + C_{box}\right)}{C_K C_{Si}} \right) \left(\dfrac{1 + e^{\sqrt{\alpha_b} L}}{1 + e^{\sqrt{\alpha_b} L} - e^{\sqrt{\alpha_b} x_{min,b}} - e^{\sqrt{\alpha_b}\left(L - x_{min,b}\right)}} \right) - \dfrac{C_{bot}}{Wt_{sp} 8\pi\varepsilon_{Si}} \left(U_S + U_D\right) \right)^{-1} \\ \qquad for\, \phi'_{b\,min} > \phi'_{f\,min} \end{cases} \tag{4.58}$$

where, $U_S = U(x)\big|_{x=x_{min}}$, $U_D = U(x)\big|_{x=L-x_{min}}$

4.6 Results and Discussion

This section presents some theoretical and ATLAS™ simulation results of the surface potential, threshold voltage, subthreshold current and subthreshold swing of the Re-S/D SOI MOSFETs with high-*k* gate-dielectric material. The high-*k* gate-dielectric material considered for modeling and simulations is HfO_2 with a relative permittivity ε_k =22,

unless stated otherwise. All the results have been plotted by considering the same effective oxide thickness (EOT), however, the physical dielectric thickness varies according to this relation: physical dielectric thickness, $t_k = t_{ox}\left(\frac{\varepsilon_k}{\varepsilon_{Sio_2}}\right)$; t_{ox} is the effective oxide thickness (EOT), and ε_{Sio_2} is the permittivity of silicon dioxide. Further, three types of parasitic capacitances might affect the device performance: the bottom capacitance, C_{bot}, between bottom edge of the gate electrode to the source and drain regions (through high-*k*); C_{pp}, the parallel plate capacitance between gate and source/drain electrodes; and C_{top}, the top fringing capacitance between top surface of the gate and source/drain electrodes through the first layer of passivation dielectrics [Mohapatra *et al.* (2003)]. However, a thick spacer between source and drain is considered in our proposed structure. Thus, the effect of C_{pp} and C_{top} is negligible on the device characteristics. The simulation methodology has been discussed in section 3.6 of Chapter 3.

4.6.1 Surface Potential

The front-channel and back-channel surface potentials of a Re-S/D SOI MOSFET along the channel length direction are displayed in Fig. 4.3 considering HfO_2 (ε_k =22) as a gate- dielectric material. Other device parameters are ϕ_M =4.8eV, L =45nm, N_a =10^{16}cm^{-3}, N_d =10^{20}cm^{-3}, t_{box} =200nm, t_{Si} = 8nm, t_{rsd} = 30nm, t_{ox} =1.5nm, V_{DS} =0.1V, V_{GS} =0.1V. It is noticed from the figure that back-channel minimum surface potential is higher than the front-channel minimum surface potential by 30mV for the selected device dimensions and the channel-doping level. Therefore, the device threshold voltage is mainly under the control of the back-channel rather than the front-channel in contrast to the conventional SOI MOSFETs.

Figure 4.4 demonstrates the back surface potential variation against the channel length for different gate-dielectric constants (ε_k). A material with high dielectric constant as a gate-dielectric raises the minimum value of back surface potential. Figure 4.4

demonstrates the back surface potential variation against the channel length for different gate-dielectric constants (ε_k). A gate-dielectric with high dielectric constant (more fringing fields) raises the minimum value of back surface potential. Thus, results in lowering the source-channel barrier height, which subsequently results in the threshold voltage change. Therefore, the fringing fields due to the bottom capacitance, C_{bot} between bottom edge of the gate electrode to the source and drain regions could considerably modulate the threshold voltage of a Re-S/D SOI MOSFET. In Fig. 4.4, the highest level of minimum surface potential is observed for $\varepsilon_k = 27$ (more fringing fields) .

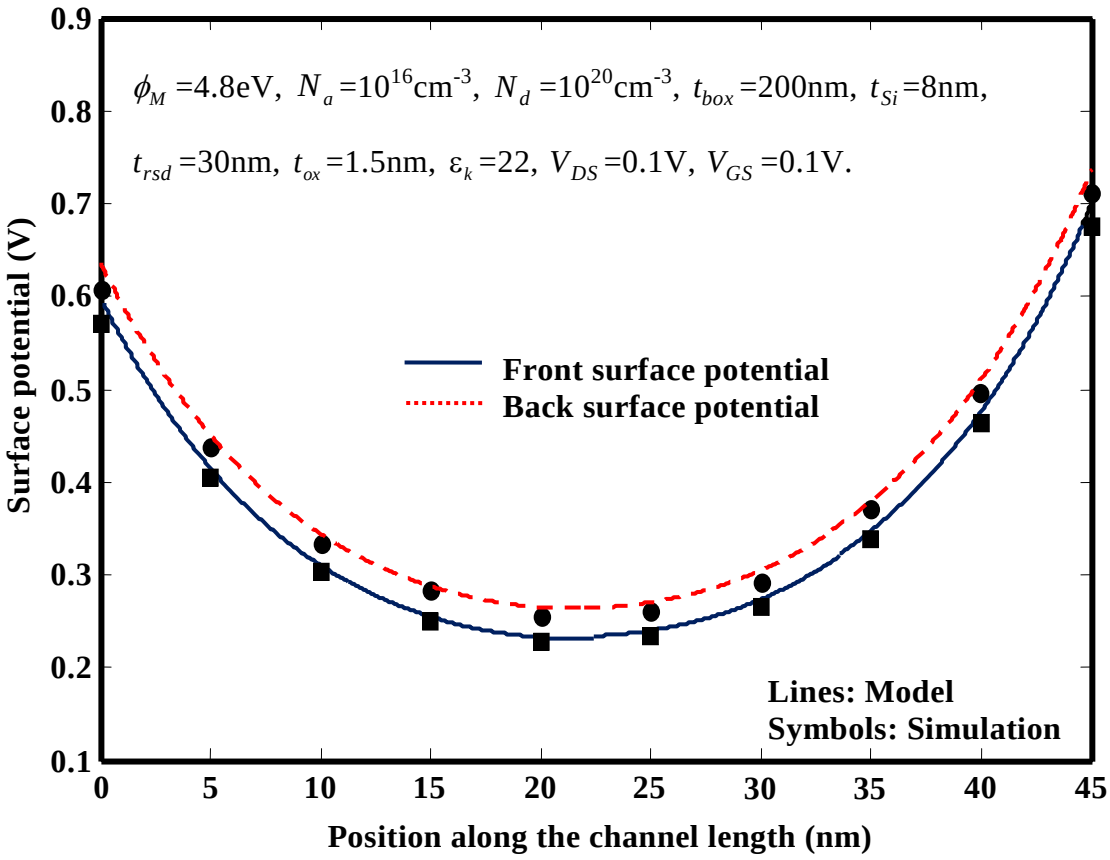


Fig. 4.3: Surface potential along the channel length at front-channel and back-channel

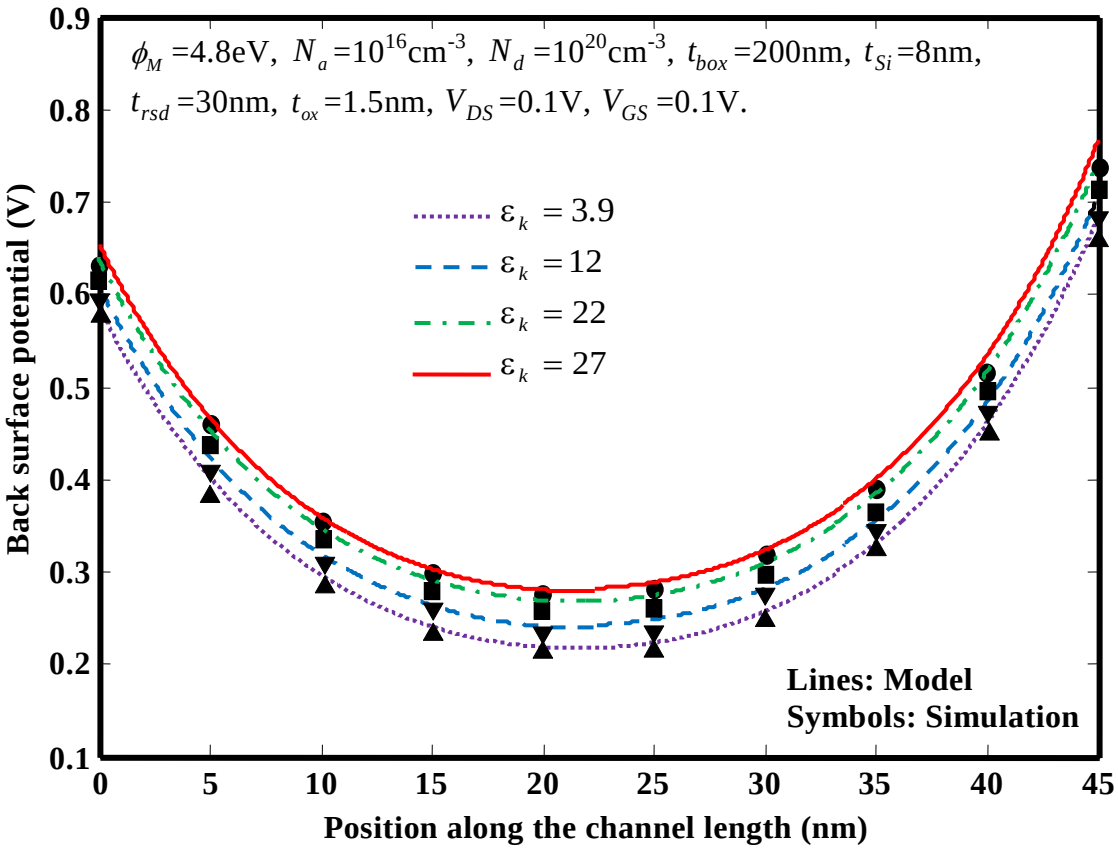


Fig. 4.4: Back surface potential along the channel length for various gate-dielectric constants (ε_k)

4.6.2 Threshold Voltage

Figure 4.5 presents the variation of threshold voltage with respect to channel length for different effective oxide thicknesses, t_{ox} =1.5nm and 3nm. It is observed that for a fixed value of channel thickness, the capacitive coupling between the gate electrode and channel region increases for a reduced gate-dielectric thickness. Thus, the gate electrode has more control over the channel region, resulting in decreased threshold voltage roll-off.

Figure 4.6 exhibits the variation of threshold voltage with respect to channel length while t_{rsd} as a variable parameter with HfO_2 as a gate-dielectric material. The selected

thickness for source and drain penetration in the BOX is t_{rsd} = 0nm, 30nm, and 100nm. It should be noted that for t_{rsd} = 0 the device acts like conventional SOI MOSFET and as a result the threshold voltage remains higher compared to the cases of t_{rsd} =30nm and 100nm. It may be attributed to the fact that at lower channel doping, back surface gets inverted at first if the channel length is too short. And, since the back channel is being partially controlled by source and drain extension, subthreshold characteristics of the device get deteriorated.

Figure 4.7 displays the threshold voltage variation against the gate-dielectric constant, where the device parameters are ϕ_M =4.6eV, N_a =10^{16}cm^{-3}, N_d =10^{20}cm^{-3}, t_{Si}=8nm, t'_{ox} =1.5nm, t_{box} =200nm, t_{rsd} =30nm, V_{DS} =0.1V, L=45nm. The threshold voltage of the device is found to be decreasing with increase in gate-dielectric constant. This observation is in line with Fig. 4.4, where minimum of surface potential was found to be increasing with increase in the gate-dielectric constant, ε_k . It should be noted that the source channel barrier height gets lower with increase in the minimum of the surface potential and as a result charge carrier from the source may be easily injected into the channel region which is an indication of lowering of the threshold voltage.

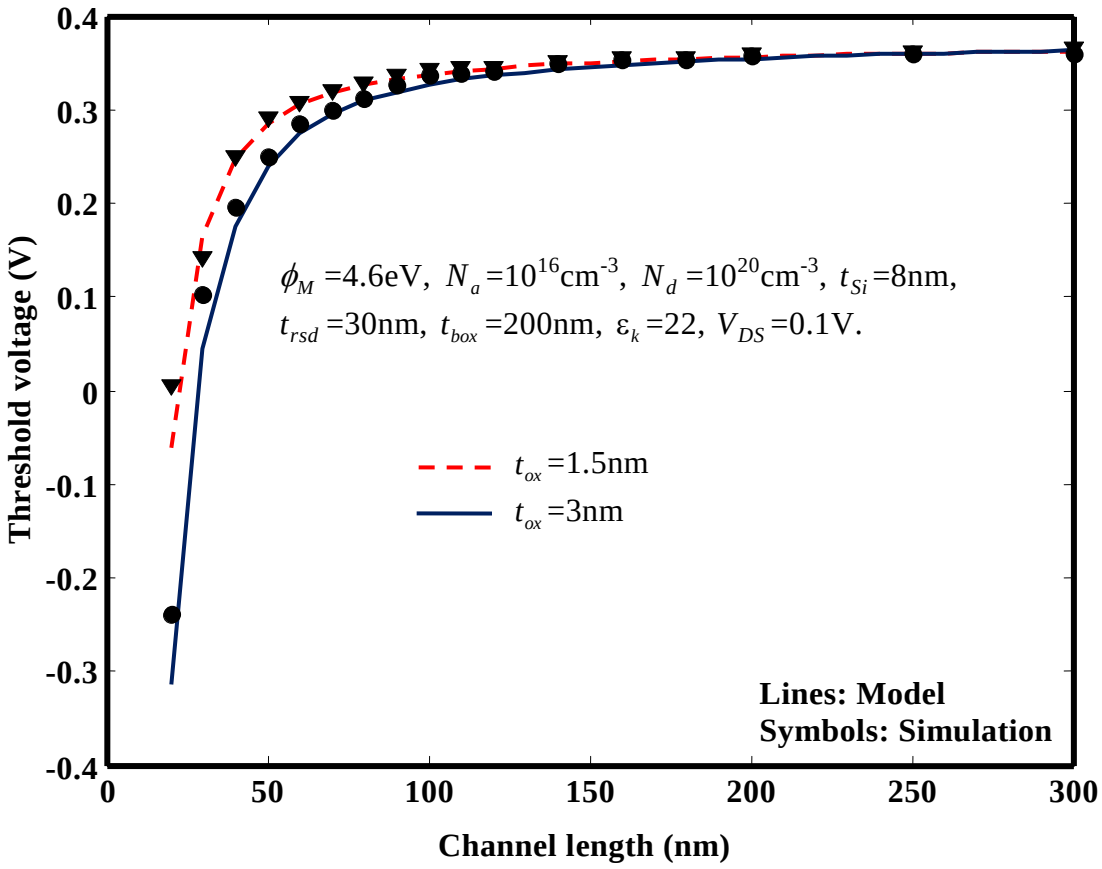


Fig. 4.5: Threshold voltage versus channel length for different gate oxide thicknesses

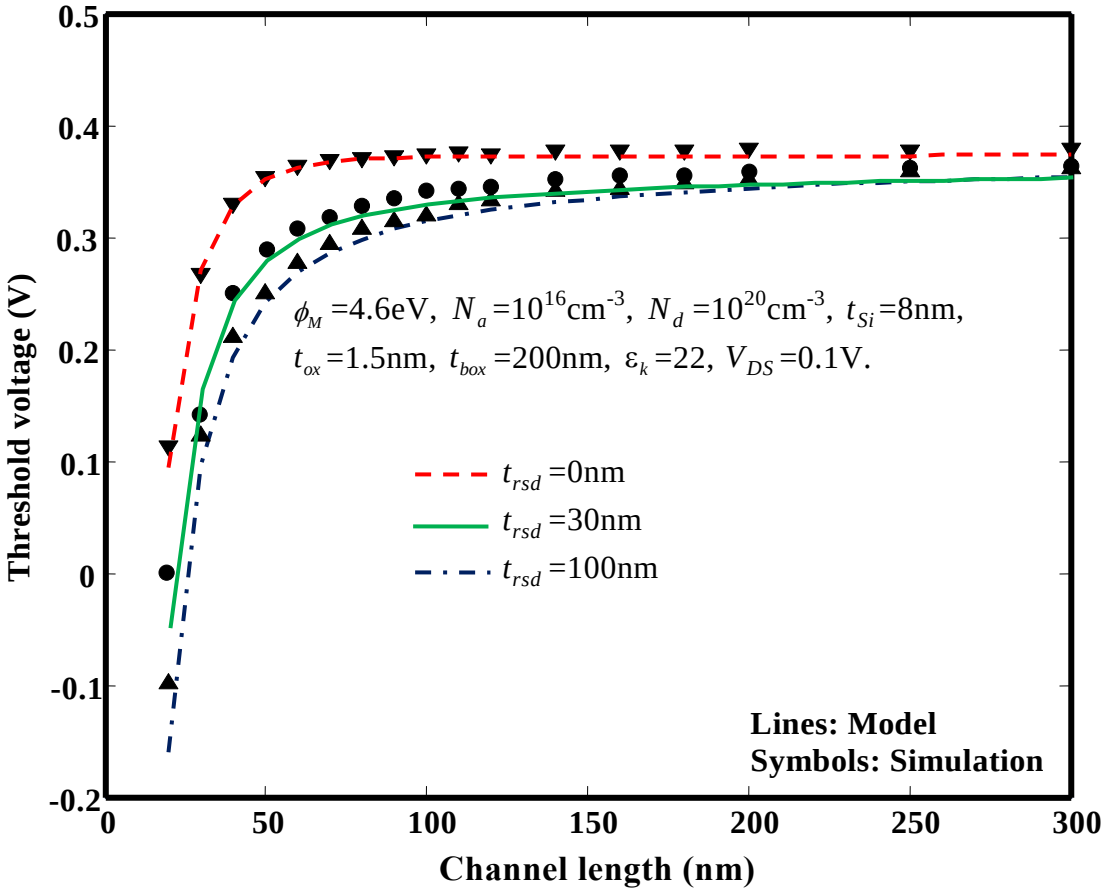


Fig. 4.6: Threshold voltage versus channel length for different recessed oxide thicknesses

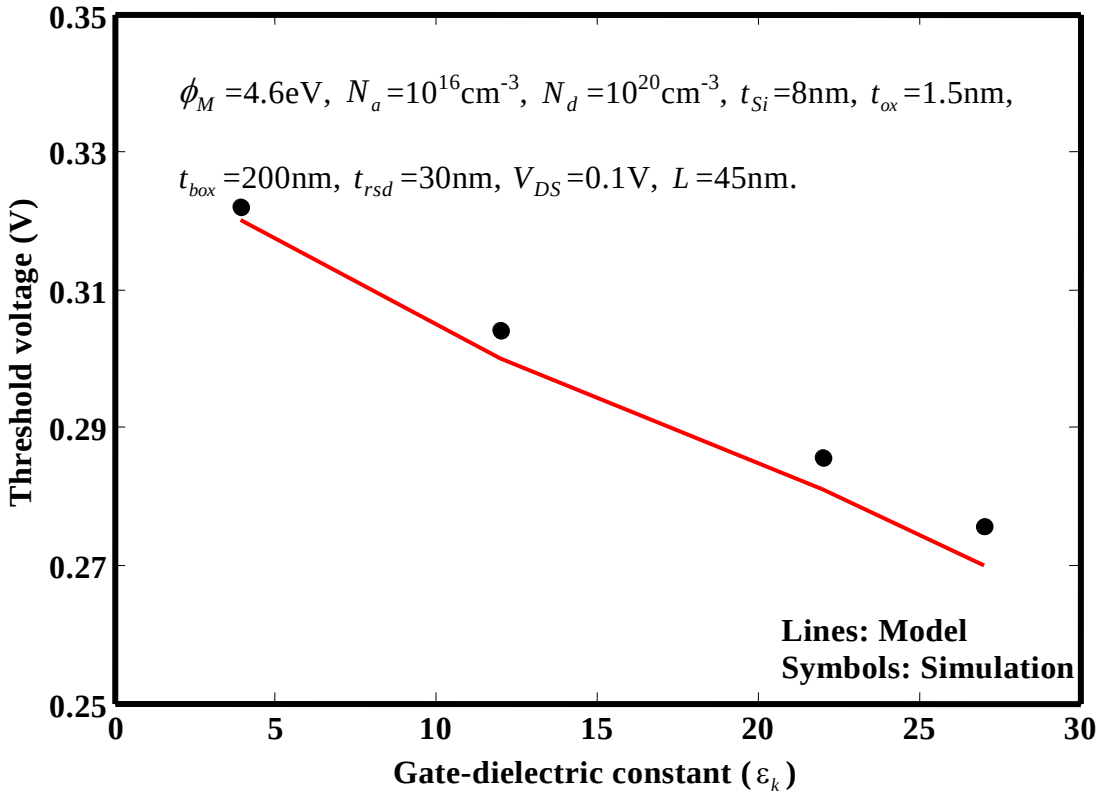


Fig. 4.7: Threshold voltage versus gate-dielectric constant (ε_k)

4.6.3 Subthreshold Current

Figure 4.8 displays the subthreshold current against the gate-to-source voltage for different channel lengths keeping other device parameters constant. It is observed that the subthreshold leakage current is found to be higher at shorter channel length for a fixed gate voltage. This may be attributed to the increased dominance of source/drain over channel electric charges with the decrease in channel length. It should be noted that the model is developed for subthreshold regime of device operation only, and therefore the model results deviate from the numerical simulation results at higher V_{GS} (above threshold).

The effect of gate oxide thicknesses on the subthreshold current is examined in Fig. 4.9. The subthreshold current characteristics are plotted with gate-to-source voltages for two different effective oxide thicknesses (t_{ox} =1 and 1.5nm). It is observed that a thinner gate oxide renders lower subthreshold current with better gate electrostatics in the channel

region. In Fig. 4.10, the variations of subthreshold current against gate to source voltage have been shown for different gate-dielectric constants. It can be observed from the figure that for the same amount of equivalent oxide thickness, the high-*k* gate-dielectric materials cause slightly higher subthreshold leakage current compared to silicon dioxide. The reason of the same may be as follows. For the same effective oxide thickness a high-*k* dielectric material will be thicker by a factor of $\varepsilon_k / \varepsilon_{SiO_2}$ compared to the SiO_2. And, a thicker dielectric layer results in an increase in the fringing electric field lines from the bottom of the gate electrode to the source and drain regions.

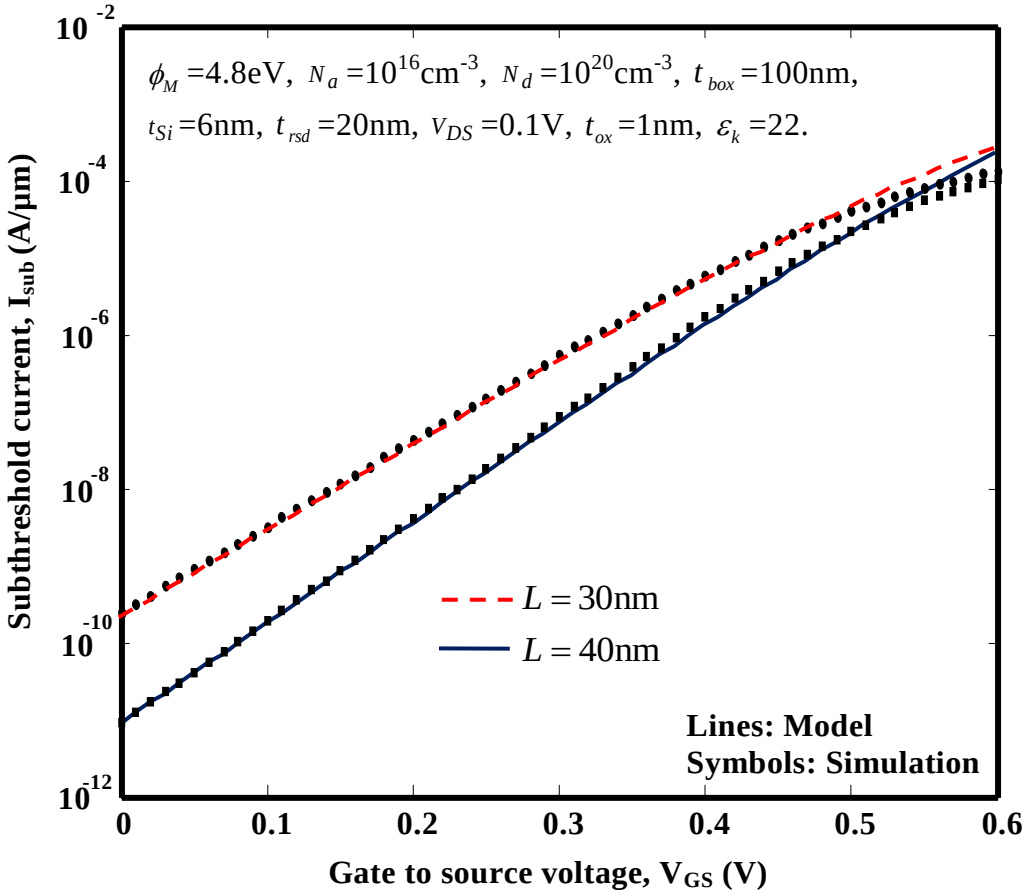


Fig. 4.8: Subthreshold current versus gate to source voltage for different channel lengths.

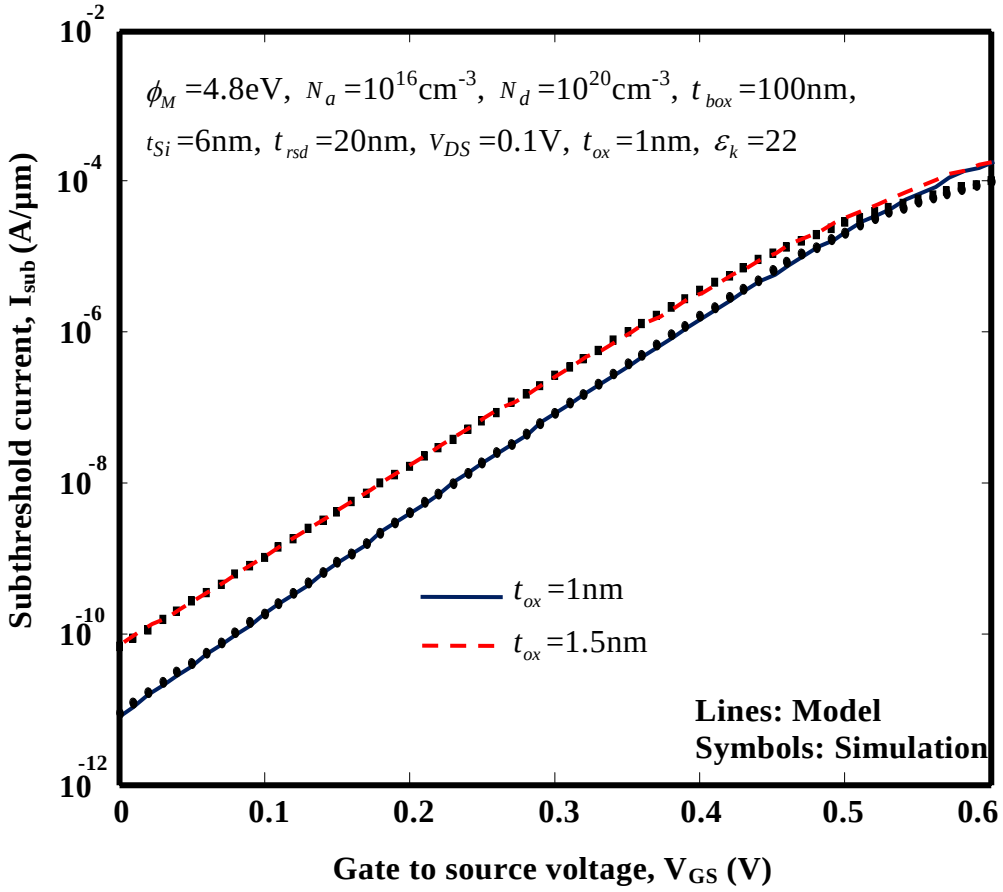


Fig. 4.9: Subthreshold current versus gate to source voltage for different oxide thicknesses.

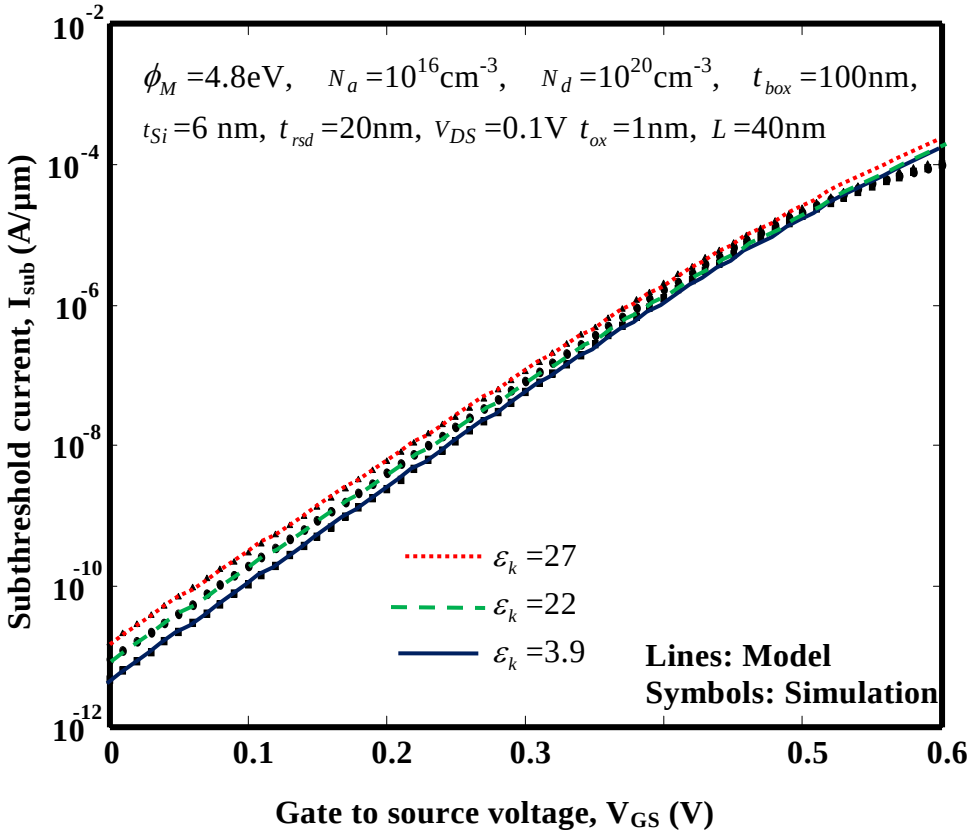


Fig. 4.10: Subthreshold current versus gate to source voltage for varying gate-dielectric constants.

4.6.4 Subthreshold Swing (*S*)

Figures 4.11 and 4.12 show the dependence of the subthreshold swing on the channel length (L) for different channel thicknesses (t_{Si}) and gate oxide thickness (t_{ox}).The switching characteristics of the device are found to be deteriorated with decreasing channel length. The results indicate that for the Re-S/D SOI MOSFET with high-*k* gate-dielectric material for a fixed channel length (L), the subthreshold swing characteristics can be improved by using the thinner channel thickness (t_{Si}) and effective gate oxide thickness (t_{ox}) of the device. This is due to the fact that a thin layer of front-gate oxide and channel thickness improves the gate control over the channel by strengthening the vertical electric field across the channel.

Fig. 4.13 demonstrates the subthreshold swing variation for different recessed source/drain thicknesses keeping all other parameters constant. The subthreshold swing is found to be increased with the increasing recessed-source/drain thicknesses. This increase in the subthreshold swing may be attributed to the coupling of the back-surface of the channel region to the extended source and drain through the buried-oxide.

The influence of gate-dielectric permittivity on subthreshold swing is shown in Fig. 4.14 by keeping all other device parameters constant. A device with high gate-dielectric permittivity is found to possess high subthreshold swing parameter value. However, this slight increase in subthreshold swing may not be a severe problem for the devices with high-*k* gate-dielectric materials which significantly controls the gate-leakage currents.

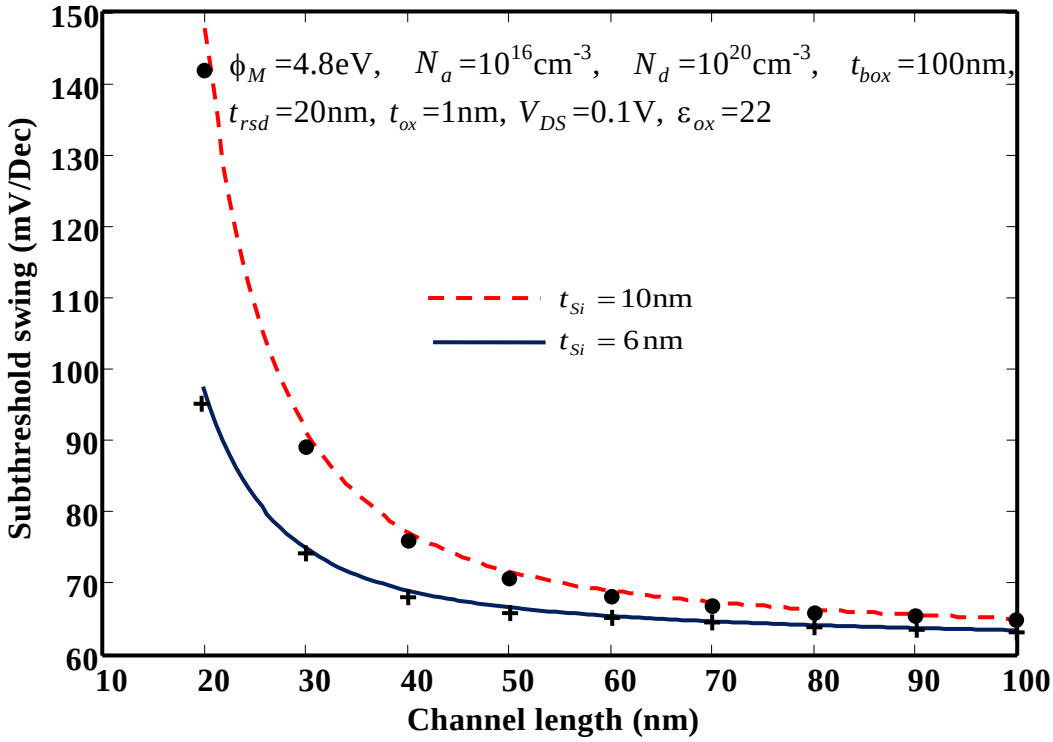


Fig. 4.11: Subthreshold swing variation with device channel length for different Si film thicknesses

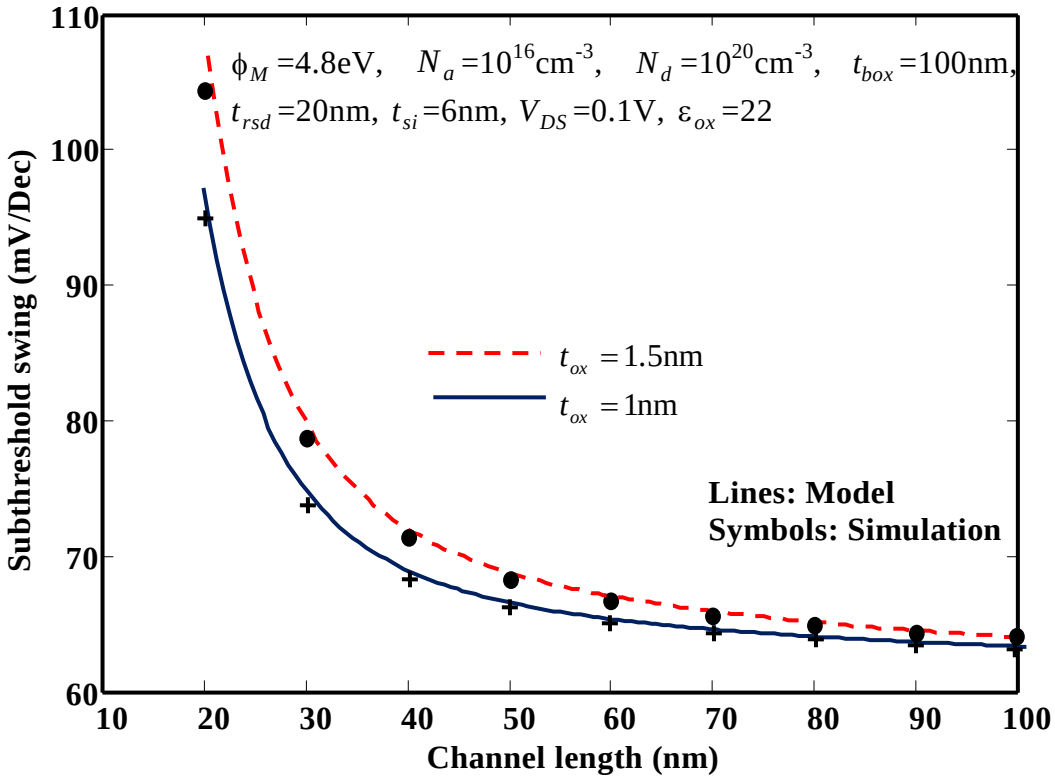


Fig. 4.12: Subthreshold swing variation with device channel length for different oxide thicknesses

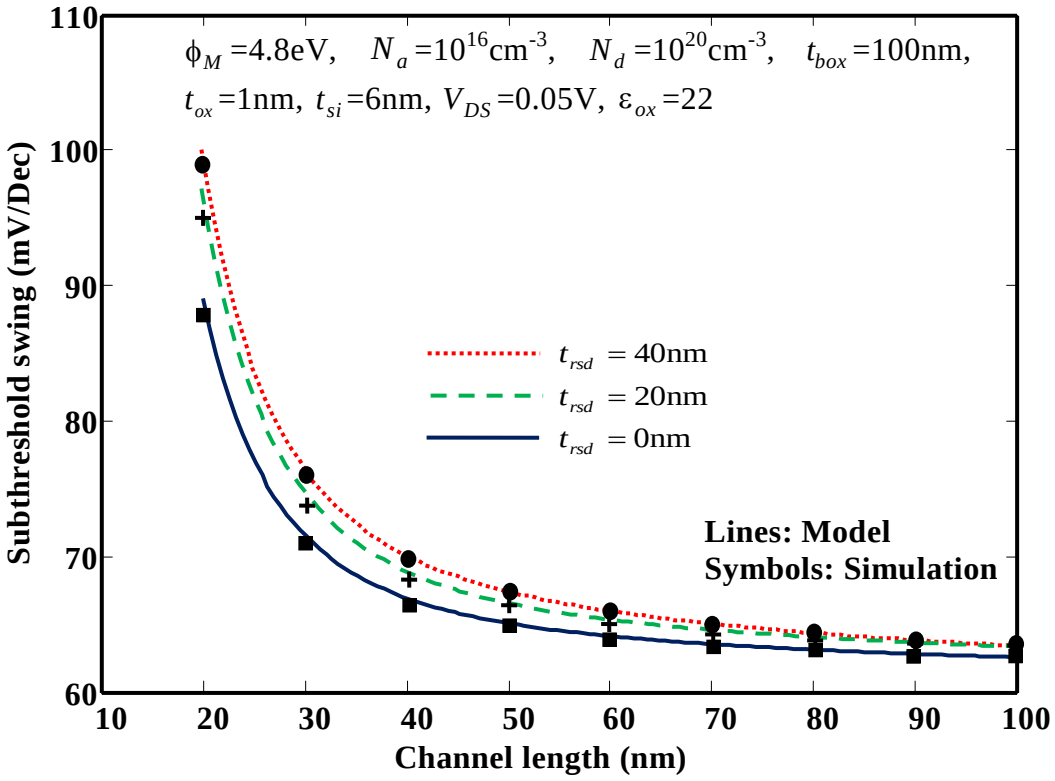


Fig. 4.13: Subthreshold swing variation with device channel length for different recessed source/drain thicknesses

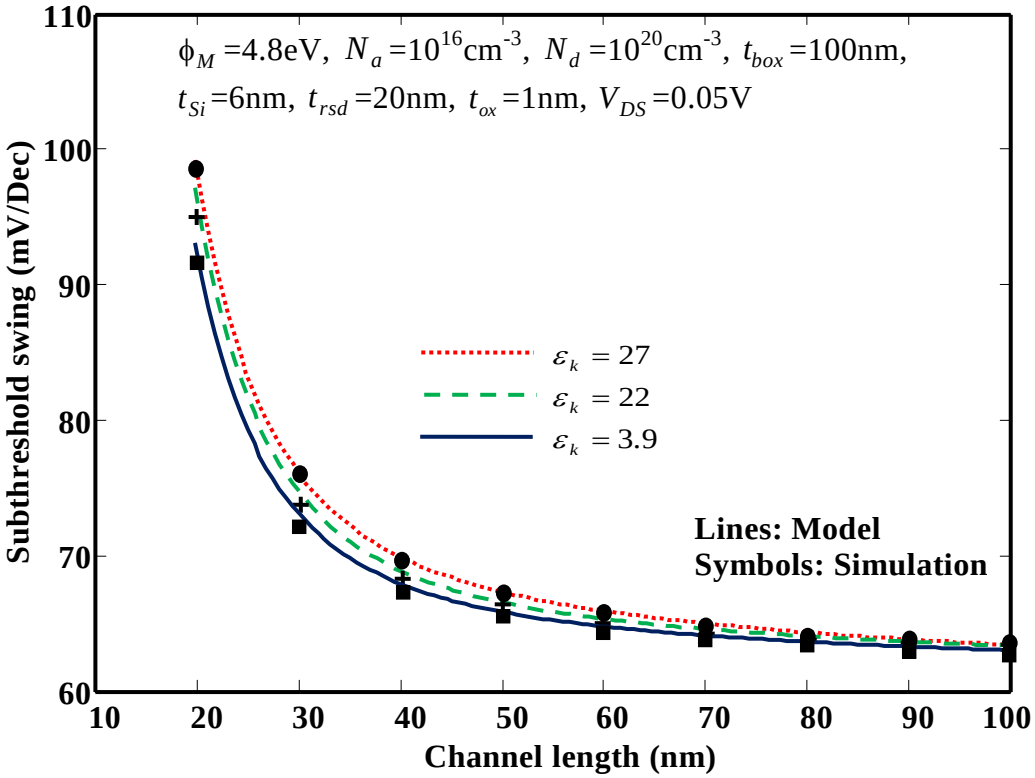


Fig. 4. 14: Subthreshold swing variation with device channel length for different gate-dielectric constants.

4.7 Summary and Conclusion

In this chapter, a detailed study of the subthreshold characteristics is presented for fully-depleted recessed-source/drain (Re-S/D) SOI MOSFETs with high-*k* gate-dielectric material. The 2D surface potential is formulated by solving two-dimensional Poisson's equation in the channel region using appropriate boundary conditions. Subsequently, the modeling of other subthreshold characteristics such as threshold voltage, subthreshold current and subthreshold swings are presented for the device. The present models include the effect of high-*k* gate-dielectric induced fringing field lines in terms of a capacitance C_{bot}, which is originated due to the electrostatic interaction between the bottom of the gate-electrode and source/drain. However, due to the thick spacer between source and drain the other parasitic capacitances C_{pp} and C_{top} have been neglected in the present models. It is observed that decrease in the gate oxide thickness and channel thickness reduces the threshold voltage roll-off, subthreshold current and subthreshold swing with better gate electrostatics in the channel region. A slight degradation of subthreshold characteristics with high-*k* gate-dielectric materials is observed due to the induced fringing field lines from gate electrode to source/drain. It is found that the present models predict the threshold voltage, subthreshold current and subthreshold swing of Re-S/D SOI MOSFETs correctly in a wide range of gate-dielectric materials and other device parameters. Furthermore, the obtained models don't need iterative calculations; hence these models are convenient for fast evaluation of the short-channel device design criteria. Thus, this model provides an efficient tool for the design of high-*k* gate-dielectric Re-S/D SOI MOSFETs including the effects of parasitic internal fringe capacitance. A reasonably good matching between the model results and ATLAS^{TM} simulation data confirms the validity of the proposed subthreshold characteristic model of the Re-S/D SOI MOSFET with high-*k* gate-dielectric material over a wide variation in device parameters.

Chapter 5

Analytical Modeling and Simulation of Subthreshold Characteristics of Short-Channel Fully-Depleted Recessed-Source/Drain SOI MOSFET with Back-Gate Control

5.1 Introduction

In Chapters 3 and 4, the modeling and simulation of subthreshold characteristics of short-channel DMG Re-S/D SOI MOSFET and Re-S/D SOI MOSFET with high-*k* gate-dielectric material were presented respectively. In the present chapter, an attempt has been made to analytically analyze the subthreshold characteristics of short-channel Re-S/D SOI MOSFET with back-gate control by considering the 2D effects in both channel region and buried oxide (BOX) layer. It has been discussed in Chapter 2 that the short-channel effects are well suppressed in a FD SOI MOSFET, when the silicon channel thickness (t_{Si}) is less than or equal to one-fourth of the channel length (L). However, in sub-30nm channel length regime, t_{Si} needs to be scaled below 5nm; therefore, the large parasitic series resistance and threshold voltage sensitivity to t_{Si} variation become serious issues [Noguchi *et al.* (2001), Chan *et al.* (1994)]. The extended source and drain offer low source and drain resistance, respectively, and facilitate better source and drain contacts and consequently decrease the total series resistance [Thean *et al.* (2006)]. On the other hand, it is found from the literature survey that short- channel

devices severely suffer with threshold voltage fluctuation. Hence, to suppress the threshold voltage fluctuation in short-channel length devices, the application of back-gate bias is necessary [Yang *et al.* (1995), Numata *et al.* (2004), Majumdar *et al.* (2009)]. Thus, the presence of a back-gate in FD Re-S/D SOI MOSFETs could be a potential option to improve the device performance in terms of large threshold voltage (V_{th}) controllability, less parasitic series resistance, on-current (I_{on}) improvement, and off-current (I_{off}) suppression as well [Majumdar *et al.* (2009)]. Keeping the above facts in view, an attempt has been made in this chapter to present a theoretical and simulation-based study of the potential distribution, threshold voltage, subthreshold swing and subthreshold current of the FD Re-S/D SOI MOSFETs with back-gate control. The layout of the present chapter is outlined as follows.

In section 5.2, the 2D surface potential function of the short-channel FD Re-S/D SOI MOSFET device with back-gate control is derived by solving the 2D Poisson's equation using parabolic approximation method. Section 5.3 presents the analytical threshold voltage modeling of the device. The analytical subthreshold current and subthreshold swing models are developed in sections 5.4 and 5.5 respectively. Results and discussion are presented in section 5.6. Finally, the summary and conclusion of the present chapter are presented in section 5.7.

5.2 Modeling of Two-Dimensional (2D) Surface Potential

The schematic structure of a Re-S/D UTB SOI MOSFET with back-gate control is shown in Fig. 5.1, where, L is the gate length, t_{Si} is the Si film thickness, t_{ox} is the gate oxide thickness and t_{box} is the buried oxide thickness. N_a, N_d and N_{sub} represent channel, source/drain, and substrate doping concentrations respectively. V_{Gs}, V_{DS} and V_{BG} are the gate to source, drain to source, and back-gate voltages, respectively. The work functions of front-gate and back-gate materials are considered to be ϕ_{FM} and ϕ_{BM} respectively. The x- and y-axes of the 2D structure are considered to be along the channel-gate oxide interface and the source-channel interface respectively, as shown in Fig. 5.1.

It is important to mention that the Re-S/D SOI structures of Chapters 3 and 4 were shown with the p^+ substrate. This was deliberately done to simplify the analytical modeling, although, the Si wafers, which are available in the market, are generally lightly doped. A lightly doped p substrate may not provide an ideal back-gate contact and builds the substrate induced surface potential (SISP) effects [Imam *et al.* (1999), Kumar *et al.* (2014)]. The SISP may alter the threshold characteristics of the device. Therefore, the back-gate control or biasing may be avoided if the device is fabricated on p substrate. However, a highly doped p^+ substrate may cut down the SISP effects significantly. In the present case, since we have considered a separate back-gate on the substrate as done in Numata *et al.* (2004), and Fasarakis *et al.* (2014) the substrate doping really does not matter much and the substrate only provide mechanical support to the structure. Furthermore, it has been discussed in Chapter 2 that 2D effects in the BOX layer could not be neglected for short-channel devices with back-gate control. Thus, in the present chapter, we have considered the 2D effects in both channel region and buried oxide (BOX) layer to model a short-channel Re-S/D UTB SOI MOSFET with back-gate control. The potentials in the channel region and BOX are named as $\phi_1(x,y)$and $\phi_2(x,y)$ respectively. The other parameters used in modeling and simulation are detailed in Table 5.1.

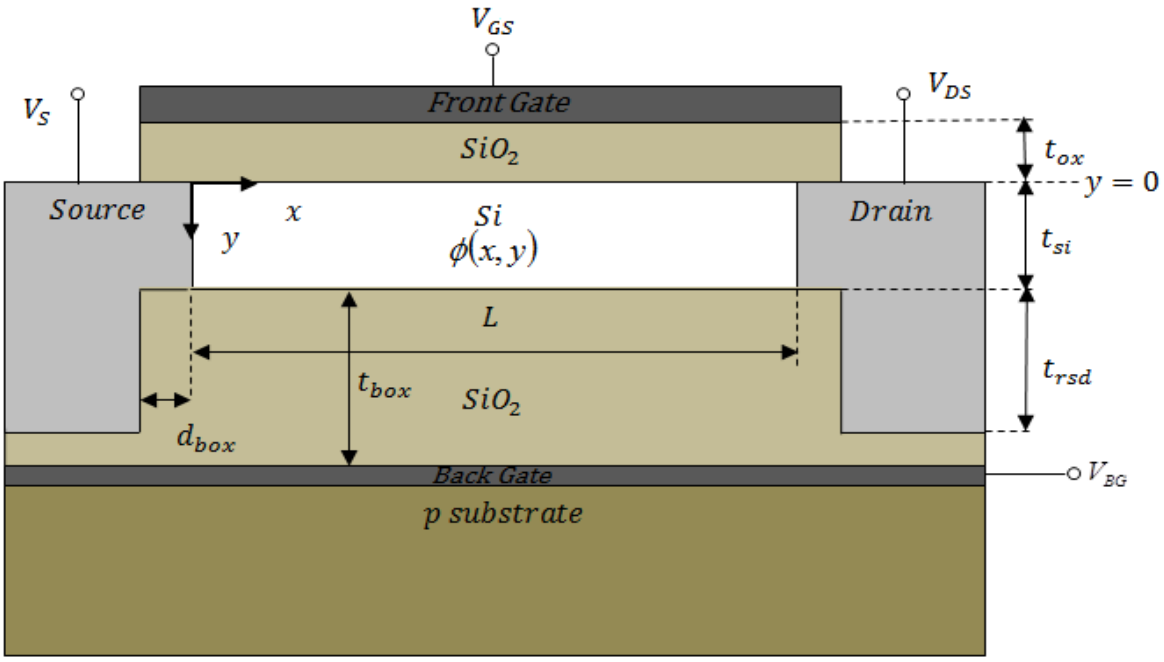


Fig. 5.1: The schematic structure of the Re-S/D FD SOI MOSFET with back-gate control

Parameters	Symbol	values
Front-gate work-function	ϕ_{FM}	4.71eV, 4.8eV
Back-gate work-function	ϕ_{BM}	4.71eV, 4.8eV
Channel Doping	N_a	10^{15}cm^{-3}
Source/Drain Doping	N_d	10^{20}cm^{-3}
Substrate Doping	N_{sub}	10^{15}cm^{-3}
Silicon Thickness	t_{Si}	6-10nm
Gate Oxide Thickness	t_{ox}	1.5-3nm
Buried Oxide Thickness	t_{box}	40-80nm
The depth of S/D in the buried oxide	t_{rsd}	0- 25nm
Recessed Length	d_{box}	3nm
Channel Length	L	20-120nm
Front-gate Voltage	V_{GS}	-0.2-0.6V
Drain Voltage	V_{DS}	0.05V
Back-gate Voltage	V_{BG}	-5 to 2V

Table 5. 1: Device parameter values used for modeling and simulation of a Re-S/D FD SOI MOSFET with back-gate control

The 2D Poisson's equations for potential in the channel region and BOX are

$$\frac{\partial^2\phi_1(x,y)}{\partial x^2}+\frac{\partial^2\phi_1(x,y)}{\partial y^2}=\frac{qN_a}{\varepsilon_{Si}} \qquad \text{for } 0\le y\le t_{Si} \tag{5.1}$$

$$\frac{\partial^2\phi_2(x,y)}{\partial x^2}+\frac{\partial^2\phi_2(x,y)}{\partial y^2}=0 \qquad \text{for } t_{Si}\le y\le t_{Si}+t_{box} \tag{5.2}$$

The potential distribution in the channel region and BOX are approximated by the following polynomials [Young *et al.* (1989)]

$$\phi_1(x,y)=\phi_f(x)+C_{11}(x)y+C_{12}(x)y^2 \qquad \text{for } 0\le y\le t_{Si} \tag{5.3}$$

$$\phi_2(x,y)=C_{20}(x)+C_{21}(x)y+C_{22}(x)y^2 \qquad \text{for } t_{Si}\le y\le t_{Si}+t_{box} \tag{5.4}$$

where, $\phi_f(x)=\phi_1(x,0)$ is the surface potential at SiO_2/Si interface and the arbitrary coefficients $C_{11}(x)$, $C_{12}(x)$, $C_{20}(x)$, $C_{21}(x)$ and $C_{22}(x)$ are the functions of x only. These coefficients are to be determined using the following boundary conditions:

The continuity of electric flux at SiO_2/Si interface is formulated as:

$$\left[\frac{\partial\phi_1(x,y)}{\partial y}\right]_{y=0}=\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{\phi_f(x)-V'_{GS}}{t_{ox}}=\frac{\phi_f(x)-V'_{GS}}{t_{ox}.\gamma} \tag{5.5}$$

The electric flux at Si/BOX interface is also continuous as:

$$\left[\frac{\partial\phi_1(x,y)}{\partial y}\right]_{y=t_{Si}}=-\frac{E_b}{\gamma}+\frac{C_{rsd}}{\varepsilon_{Si}L}\left[V'_{DS}-2\phi_b(x)\right] \tag{5.6}$$

The electric field at the bottom of the channel region is:

$$\left[\frac{\partial\phi_2(x,y)}{\partial y}\right]_{y=t_{Si}}=-E_b+\frac{V'_{DS}-2\phi_b(x)}{t^*_{rsd}} \tag{5.7}$$

The surface potential at the source end is

$$\phi_1(0,y)=V_{bi} \tag{5.8}$$

The surface potential at the drain end is

$$\phi_1(L,y) = V_{bi} + V_{DS} \tag{5.9}$$

The surface potential at the back-gate is

$$\phi_2(x, y = t_{Si} + t_{ox}) = V'_{BG} \tag{5.10}$$

where, $\gamma = \frac{\varepsilon_{Si}}{\varepsilon_{ox}}$, $V'_{GS} = V_{GS} - V_{FB1}$, $V'_{DS} = V_{DS} - 2V_{FB2}$, and $V'_{BG} = V_{BG} - V_{FB3}$; V_{FB1}, V_{FB2} and V_{FB3} represent the flat-band voltages which are given as $V_{FB1} = \phi_{FM} - \phi_{Si}$, $V_{FB2} = V_T\, ln\left(\frac{N_a N_d}{n_i^2}\right)$ and $V_{BM} = \phi_{BM} - \phi_{Si}$; The symbol ϕ_{Si} represents the silicon body work function and given by $\phi_{Si} = \chi_{Si} + \frac{E_g}{2} + V_T \ln\left(\frac{N_a}{n_i}\right)$, χ_{Si} and E_g are the electron affinity and energy band gap of the silicon, respectively. N_d is the doping concentration, n_i is the intrinsic carrier concentration in the silicon, V_{bi} is the built-in voltage at the source/drain and Si interface given by $V_{bi} = V_T\, ln\left(\frac{N_a N_d}{n_i^2}\right)$, V_T is the thermal voltage, V_{DS}, V_{GS} and V_{BG} are the drain to source, gate to source and back-gate bias voltages, respectively. E_b represents the BOX electric field component at Si/BOX interface. The back surface potential at Si/BOX interface is $\phi_b(x) = \phi_1(x, y = t_{Si}) = \phi_2(x, y = t_{Si})$. C_{rsd} is the recessed source/drain buried oxide capacitance per unit length which is given as [Svilicic *et al.* (2009)]

$$C_{rsd} = \begin{cases} \dfrac{\varepsilon_{box}}{\left(\frac{\pi}{2} + \frac{\pi}{2}.sec\,h\frac{t_{rsd}}{d_{box}}\right)} ln\left(1 + \dfrac{L}{2d_{box}}\right) & for \dfrac{L}{2} < t_{rsd} \\ \dfrac{\varepsilon_{box}}{\left(\frac{\pi}{2} + \frac{\pi}{2}.sec\,h\frac{t_{rsd}}{d_{box}}\right)} ln\left(1 + \dfrac{t_{rsd}}{2d_{box}}\right) & for \dfrac{L}{2} > t_{rsd}, t_{rsd} = 0 \end{cases} \tag{5.11}$$

where, d_{box} is the length of source/drain overlap over buried oxide, $t_{rsd}^{*} = \frac{\varepsilon_{box} L}{C_{rsd}}$ is the effective thickness of source/drain extensions in buried oxide.

By using the boundary conditions of Eqns. (5.5) and (5.6) in Eq. (5.3), the coefficients $C_{11}(x)$ and $C_{12}(x)$ can be written as

$$C_{11}(x) = \frac{\phi_f(x) - V'_{GS}}{t_{ox}.\gamma} \tag{5.12}$$

$$C_{12}(x) = \frac{V'_{GS} - \phi_f(x)}{2t_{Si}t_{ox}.\gamma} - \frac{E_b}{2t_{Si}\gamma} + \frac{C_{rsd}}{2t_{Si}\varepsilon_{Si} L}\left[V'_{DS} - \phi_b(x)\right] \tag{5.13}$$

Now, the expression for $\phi_1(x,y)$ is obtained by substituting the values of $C_{11}(x)$ and $C_{12}(x)$ into Eq. (5.3). Thus, the potential $\phi_1(x,y)$ can be written as

$$\phi_1(x,y) = \phi_f(x) + \frac{\phi_f(x) - V'_{GS}}{t_{ox}.\gamma}\, y + \left\{\frac{V'_{GS} - \phi_f(x)}{2t_{Si}t_{ox}.\gamma} - \frac{E_b}{2t_{Si}\gamma} + \frac{C_{rsd}}{2t_{Si}\varepsilon_{Si} L}\left[V'_{DS} - \phi_b(x)\right]\right\} y^2 \tag{5.14}$$

Substituting $y = t_{Si}$ in Eq. (5.14) gives

$$\phi_b(x) = \frac{C_{Si}}{C_{Si} + C_{rsd}}\left\{\phi_f(x)\left[1 + \frac{t_{Si}}{2t_{ox}.\gamma}\right] - \frac{t_{Si}}{2t_{ox}.\gamma}V'_{GS} - \frac{t_{Si}}{2\gamma}E_b + \frac{C_{rsd}}{2C_{Si}}V'_{DS}\right\} \tag{5.15}$$

where, $C_{Si} = \frac{\varepsilon_{Si} L}{t_{Si}}$ is the silicon-body capacitance per channel width [Svilicic *et al.* (2009)]

With the help of Eq. (5.15), Eq (5.14) can be expressed in terms of $\phi_b(x)$ as

$$\begin{aligned}\phi_1(x,y) = V'_{GS} + \frac{2\gamma t_{ox}}{t_{Si}+2\gamma t_{ox}}\left[\phi_b(x)\left(\frac{C_{Si}+C_{rsd}}{C_{Si}}\right) - V'_{GS} + \frac{E_b t_{Si}}{2\gamma} - \frac{C_{rsd}}{2C_{Si}}V'_{DS}\right] \\ + \frac{2}{t_{Si}+2\gamma t_{ox}}\left[\phi_b(x)\left(\frac{C_{Si}+C_{rsd}}{C_{Si}}\right) - V'_{GS} + \frac{E_b t_{Si}}{2\gamma} - \frac{C_{rsd}}{2C_{Si}}V'_{DS}\right] y \\ + \left\{\frac{1}{t_{Si}(t_{Si}+2\gamma t_{ox})}\left[-\phi_b(x)\left(\frac{C_{Si}+C_{rsd}}{C_{Si}}\right) + V'_{GS} - \frac{E_b(t_{Si}+\gamma t_{ox})}{\gamma} + \frac{C_{rsd}}{2C_{Si}}V'_{DS}\right]\right. \\ \left. + \frac{C_{rsd}}{2C_{Si}t_{Si}^2}\left(V'_{DS} - 2\phi_b(x)\right)\right\} y^2\end{aligned} \quad (5.16)$$

Furthermore, the arbitrary constants $C_{20}(x)$, $C_{21}(x)$ and $C_{22}(x)$ of Eq. (5.4) can be obtained by using the boundary conditions Eqns. (5.7) and the surface potentials at $y = t_{Si}$ and $y = t_{Si} + t_{box}$ in Eq. (5.4):

$$C_{20}(x) = \frac{t_{box}^{\ 2} - t_{Si}^{\ 2}}{t_{box}^{\ 2}}\left(-V'_{BG} + \phi_b(x)\right) + V'_{BG} + \frac{t_{Si}(t_{Si}+t_{box})}{t_{box}}E_b - \frac{t_{Si}(t_{Si}+t_{box})}{t^*_{rsd}t_{box}}\left(V'_{DS} - 2\phi_b(x)\right) \quad (5.17)$$

$$C_{21}(x) = \frac{2t_{Si}}{t_{box}^{\ 2}}\left(-V'_{BG} + \phi_b(x)\right) - \frac{(2t_{Si}+t_{box})}{t_{box}}E_b + \frac{(2t_{Si}+t_{box})}{t_{box}t^*_{rsd}}\left(V'_{DS} - 2\phi_b(x)\right) \quad (5.18)$$

$$C_{22}(x) = \frac{-1}{t_{box}^{\ 2}}\left(-V'_{BG} + \phi_b(x)\right) + \frac{1}{t_{box}}E_b - \frac{1}{t^*_{rsd}t_{box}}\left(V'_{DS} - 2\phi_b(x)\right) \quad (5.19)$$

Now, the expression $\phi_2(x,y)$ can be obtained by substituting the values of $C_{20}(x)$, $C_{21}(x)$ and $C_{22}(x)$ into Eq. (5.4).

$$\begin{aligned}\phi_2(x,y) = \frac{t_{box}^{\ 2} - t_{Si}^{\ 2}}{t_{box}^{\ 2}}\left(-V'_{BG} + \phi_b(x)\right) + V'_{BG} + \frac{t_{Si}(t_{Si}+t_{box})}{t_{box}}E_b - \frac{(t_{Si}+t_{box})t_{Si}}{t^*_{rsd}t_{box}}\left(V'_{DS} - 2\phi_b(x)\right) \\ + \left[\frac{2t_{Si}}{t_{box}^{\ 2}}\left(-V'_{BG} + \phi_b(x)\right) - \frac{(2t_{Si}+t_{box})}{t_{box}}E_b + \frac{(2t_{Si}+t_{box})}{t_{box}t^*_{rsd}}\left(V'_{DS} - 2\phi_b(x)\right)\right] y \\ + \left[\frac{-1}{t_{box}^{\ 2}}\left(-V'_{BG} + \phi_b(x)\right) + \frac{1}{t_{box}}E_b - \frac{1}{t^*_{rsd}t_{box}}\left(V'_{DS} - 2\phi_b(x)\right)\right] y^2\end{aligned} \quad (5.20)$$

Using the Eq. (5.20) into Eq. (5.2), the BOX electric field component at Si/BOX interface can be obtained as

$$E_b = \frac{1}{t_{box}}\left(-V'_{BG} + \phi_b(x)\right) + \frac{\left(V'_{DS} - 2\phi_b(x)\right)}{t^*_{rsd}} - \frac{t_{box}}{2}\frac{d^2\phi_b(x)}{dx^2} \tag{5.21}$$

Now, the second-order differential equation of back-surface potential, $\phi_b(x)$ can be obtained by solving the Eq. (5.1) using Eqns. (5.16) and (5.21):

$$\frac{d^2\phi_b(x)}{dx^2} + \alpha_b\phi_b(x) = \beta_b \tag{5.22}$$

where, α_b and β_b are

$$\alpha_b = \frac{\dfrac{-2}{t_{Si}\left(t_{Si}+2\gamma t_{ox}\right)}\left[\dfrac{C_{Si}+C_{rsd}}{C_{Si}} + \dfrac{\left(t_{Si}+\gamma t_{ox}\right)}{t_{box}\gamma} - 2\dfrac{\left(t_{Si}+\gamma t_{ox}\right)}{\gamma t^*_{rsd}} + \dfrac{C_{rsd}}{C_{Si}t_{Si}}\left(t_{Si}+2\gamma t_{ox}\right)\right]}{\left[1+\dfrac{t_{box}\left(t_{Si}+\gamma t_{ox}\right)}{t_{Si}\left(t_{Si}+2\gamma t_{ox}\right)\gamma}\right].} \tag{5.23}$$

$$\beta_b = \frac{\left\{\begin{array}{l}\dfrac{qN_a}{\varepsilon_{Si}} - \left[\dfrac{2}{\left(t_{Si}+2\gamma t_{ox}\right)t_{Si}}\right]V'_{GS} - \dfrac{2}{t_{Si}\gamma}\left(\dfrac{t_{Si}+\gamma t_{ox}}{t_{Si}+2\gamma t_{ox}}\right)\left(\dfrac{V'_{BG}}{t_{box}} - \dfrac{V'_{DS}}{t^*_{rsd}}\right) \\ \qquad + \dfrac{C_{rsd}}{C_{Si}t_{Si}}\left(\dfrac{2}{t_{Si}+2\gamma t_{ox}} + \dfrac{1}{t_{Si}}\right)V'_{DS}\end{array}\right\}}{\left[1+\dfrac{t_{box}\left(t_{Si}+\gamma t_{ox}\right)}{t_{Si}\left(t_{Si}+2\gamma t_{ox}\right)\gamma}\right]} \tag{5.24}$$

By solving the second-order differential equation (5.22), the following expression for back surface potential distribution along the channel can be obtained as

$$\phi_b(x) = A_b.e^{\sqrt{\alpha_b}x} + B_b.e^{-\sqrt{\alpha_b}x} - \frac{\beta_b}{\alpha_b} \tag{5.25}$$

Now, the coefficients A_b and B_b of Eq. (5.22) are determined using the boundary conditions of Eqns. (5.8) and (5.9)

$$A_b = \frac{\beta_b\left(e^{\sqrt{\alpha_b}L} - 1\right) + \alpha_b\left[V_{bi}\left(e^{\sqrt{\alpha_b}L} - 1\right) + V_{DS}e^{\sqrt{\alpha_b}L}\right]}{\alpha_b\left(e^{2\sqrt{\alpha_b}L} - 1\right)} \tag{5.26}$$

$$B_b = \frac{e^{\sqrt{\alpha_b}L}\left\{\beta_b\left(e^{\sqrt{\alpha_b}L}-1\right)-\alpha_b\left[V_{bi}\left(1-e^{\sqrt{\alpha_b}L}\right)+V_{DS}\right]\right\}}{\alpha_b\left(e^{2\sqrt{\alpha_b}L}-1\right)} \tag{5.27}$$

In order to obtain the front-surface potential, $\phi_f(x)$ the Eq. (5.15) has been differentiated twice with respect to x

$$\frac{d^2\phi_f(x)}{dx^2} = \frac{2\gamma t_{ox}}{t_{Si}+2\gamma t_{ox}}\left(\frac{C_{Si}+C_{rsd}}{C_{Si}}\right)\frac{d\phi_b(x)}{dx^2} + \frac{t_{ox}t_{Si}}{\left(t_{Si}+2\gamma t_{ox}\right)}\frac{d^2E_b}{dx^2} \tag{5.28}$$

The Eq. (5.28) is solved using Eq. (5.21), and the obtained expression is written as

$$\frac{d^2\phi_f(x)}{dx^2} = \frac{d^2\phi_b(x)}{dx^2}\frac{2\gamma t_{ox}}{t_{Si}+2\gamma t_{ox}}\left[\left(\frac{C_{Si}+C_{rsd}}{C_{Si}}\right)+\frac{t_{Si}}{2\gamma t_{box}}-\frac{t_{Si}}{2\gamma t^*_{rsd}}\right]-\frac{\gamma t_{box}t_{ox}t_{Si}}{2\gamma\left(t_{Si}+2\gamma t_{ox}\right)}\frac{d^4\phi_b}{dx^4} \tag{5.29}$$

By differentiating the Eq. (5.22) twice with respect to x, we can obtain

$$\frac{d^4\phi_b(x)}{dx^4} = -\alpha_b\frac{d^2\phi_b(x)}{dx^2} \tag{5.30}$$

Using Eqns. (5.29) and (5.30) into Eq. (5.21), E_b can be obtained in terms of front-surface potential, $\phi_f(x)$

$$E_b = \frac{1}{C_1}\left[-\frac{V'_{sub}}{t_{box}}+\frac{V'_{DS}}{t^*_{rsd}}+\left(1+\frac{t_{Si}}{2\gamma t_{box}}\right)\left(\frac{C_{Si}}{C_{Si}+C_{rsd}}\right)\left(\frac{t^*_{rsd}-2t_{box}}{t^*_{rsd}t_{box}}\right)\left(\phi_f(x)-\frac{V'_{GS}t_{Si}}{2\gamma t_{box}}+\frac{C_{rsd}}{2C_{Si}}V'_D\right)\right.$$
$$\left.-\frac{t_{box}}{2}\left(\frac{1}{C_2}\right)\frac{d^2\phi_f(x)}{dx^2}\right] \tag{5.31}$$

$$C_1 = 1+\frac{t_{Si}}{2\gamma t_{box}}\left(\frac{C_{Si}}{C_{Si}+C_{rsd}}\right)\left(\frac{t^*_{rsd}-2t_{box}}{t^*_{rsd}t_{box}}\right)$$

$$C_2 = \frac{2\gamma t_{ox}}{t_{Si}+2\gamma t_{ox}}\left[\left(\frac{C_{Si}+C_{rsd}}{C_{Si}}\right)+\frac{t_{Si}}{2\gamma t_{box}}-\frac{t_{Si}}{2\gamma t^*_{rsd}}-\frac{t_{box}t_{Si}\alpha_b}{4\gamma}\right] \tag{5.32}$$

Using the Eqns. (5.14), (5.15) and (5.31), Eq. (5.1) can be solved to obtain the second-order differential equation of front-surface potential, $\phi_f(x)$ which is given as

$$\frac{d^2\phi_f(x)}{dx^2}+\alpha_f\phi_f(x)=\beta_f \tag{5.33}$$

where, α_f and β_f are

$$\alpha_f=\frac{\dfrac{-1}{t_{Si}\gamma t_{ox}}+\left(1+\dfrac{t_{Si}}{2\gamma t_{ox}}\right)\left(\dfrac{C_{Si}}{C_{Si}+C_{rsd}}\right)\left[\dfrac{C_3}{C\gamma t_{ox}}\left(\dfrac{t_{rsd}^{*}-2t_{box}}{t_{rsd}^{*}t_{box}}\right)-2\right]}{1+\dfrac{t_{box}}{2}\left(\dfrac{C_3}{C_2C_1}\right)} \tag{5.34}$$

$$C_3=1+\frac{C_{rsd}}{\varepsilon_{Si}L}\left(\frac{C_{Si}}{C_{Si}+C_{rsd}}\right)\left(\frac{t_{Si}}{2}\right) \tag{5.35}$$

$$\beta_f=\frac{\begin{array}{r}\dfrac{qN_a}{\varepsilon_{Si}}-\dfrac{C_3}{C_1\gamma}\left(1+\dfrac{t_{Si}}{2\gamma t_{box}}\right)\left(\dfrac{C_{Si}}{C_{Si}+C_{rsd}}\right)\left(\dfrac{t_{rsd}^{*}-2t_{box}}{t_{rsd}^{*}t_{box}}\right)\left[-\dfrac{V'_{GS}t_{Si}}{2\gamma t_{box}}+\dfrac{C_{rsd}}{2C_{Si}}V'_{DS}\right]\\ +\dfrac{C_{rsd}}{\varepsilon_{Si}L}V'_{DS}-2\dfrac{C_{rsd}}{\varepsilon_{Si}L}\left[-\dfrac{V'_{GS}t_{Si}}{2\gamma t_{box}}+\dfrac{C_{rsd}}{2C_{Si}}V'_{DS}\right]-\dfrac{V'_{GS}}{\gamma t_{Si}t_{box}}-\dfrac{C_3}{C_1\gamma}(C_4)\end{array}}{1+\dfrac{t_{box}}{2}\left(\dfrac{C_3}{C_2C_1}\right)} \tag{5.36}$$

$$C_4=\left(\frac{C_{Si}+C_{rsd}}{C_{Si}}\right)\left[-\frac{V'_{sub}}{t_{box}}-\frac{V'_{GS}t_{Si}}{2\gamma t_{ox}}+\frac{C_{rsd}}{2C_{Si}}V'_{DS}\right] \tag{5.37}$$

By solving the second-order differential equation (5.33), the following expression for front-surface potential distribution along the channel can be obtained as

$$\phi_f=A_f.e^{\sqrt{\alpha_f}x}+B_f.e^{-\sqrt{\alpha_f}x}-\frac{\beta_f}{\alpha_f} \tag{5.38}$$

Now, the coefficients A_f and B_f of Eq. (5.38) are determined using the boundary conditions of Eqs. (5.8) and (5.9).

$$A_f = \frac{\beta_f\left(e^{\sqrt{\alpha_f}L}-1\right)+\alpha_f\left[V_{bi}\left(e^{\sqrt{\alpha_f}L}-1\right)+V_{DS}e^{\sqrt{\alpha_f}L}\right]}{\alpha_f\left(e^{2\sqrt{\alpha_f}L}-1\right)} \tag{5.39}$$

$$B_f = \frac{e^{\sqrt{\alpha_f}L}\left\{\beta_f\left(e^{\sqrt{\alpha_f}L}-1\right)-\alpha_f\left[V_{bi}\left(1-e^{\sqrt{\alpha_f}L}\right)+V_{DS}\right]\right\}}{\alpha_f\left(e^{2\sqrt{\alpha_f}L}-1\right)} \tag{5.40}$$

The minimum of the front- and back-surface potential $\phi_{f\min,b\min}$ could be derived by following the same method used in Chapters 3 and 4, and the obtained expression is

$$\phi_{f\min,b\min} = 2\sqrt{A_{f,b}B_{f,b}} - \frac{\beta_{f,b}}{\alpha_{f,b}} \tag{5.41}$$

Now, the virtual cathode potential $\phi_{vc}(y)$ in terms of minimum front- and back- surface potentials similar to Chapters 3 and 4 [Chen *et al.* (2003)]

$$\begin{aligned}\phi_{vc}(y) = \phi_{b\,min}&\left[\frac{C_{Si}+C_{rsd}}{C_{Si}}\frac{1}{t_{Si}+2\gamma t_{ox}}\left(2\gamma t_{ox}+2y-\frac{1}{t_{Si}}y^2\right)\right.\\&\left.+\left(\frac{1}{t_{box}}-\frac{2}{t^*_{rsd}}+\alpha_b\frac{t_{box}}{2}\right)\left(t_{Si}t_{ox}+\frac{t_{Si}}{\gamma}y-\frac{t_{Si}+2\gamma t_{ox}}{t_{Si}}y^2\right)-\frac{C_{rsd}}{C_{Si}t_{Si}^2}y^2\right]\\&+\left(V'_{GS}\right)\left[1-\frac{1}{t_{Si}+2\gamma t_{ox}}\left(-2\gamma t_{ox}-2y+\frac{1}{t_{Si}}y^2\right)\right]\\&+\left(V'_{DS}\right)\left\{\frac{C_{rsd}}{C_{Si}}\left[\frac{-\gamma t_{ox}}{t_{Si}+2\gamma t_{ox}}-\frac{1}{t_{Si}+2\gamma t_{ox}}y+\frac{1}{t_{Si}}\left(\frac{1}{t_{Si}+2\gamma t_{ox}}\right)y^2+\frac{1}{2t_{Si}^2}y^2\right]\right.\\&\qquad\left.+\left(t_{Si}t_{ox}+\frac{t_{Si}}{\gamma}y-\frac{t_{Si}+2\gamma t_{ox}}{t_{Si}}y^2\right)\frac{1}{t^*_{rsd}}\right\}\\&+\left(-\frac{V'_{sub}}{t_{box}}-\beta_b\frac{t_{box}}{2}\right)\left(t_{Si}t_{ox}+\frac{t_{Si}}{\gamma}y-\frac{t_{Si}+2\gamma t_{ox}}{t_{Si}}y^2\right)\end{aligned} \tag{5.42}$$

$$\phi_{vc}(y)=\phi_{f\,min}\left[\left(1+\frac{1}{\gamma t_{ox}}y-\left(\frac{1}{2t_{Si}\gamma t_{ox}}\right)y^2+\frac{C_5}{C_1}\left(1+\frac{t_{box}}{2C_2}\alpha_f\right)\right)+\right.$$
$$-\frac{V'_{GS}}{\gamma t_{ox}}y+\left(\frac{1}{2t_{Si}}\right)\left(\frac{V'_{GS}}{\gamma t_{ox}}+\frac{C_{rsd}}{\varepsilon_{Si}L}V'_{DS}\right)y^2+\frac{1}{C_1}\left[\frac{-V'_{sub}}{t_{box}}+\frac{-V'_{DS}}{t^*_{rsd}}\right] \quad (5.43)$$
$$\left.+\frac{C_5}{C_1}\left(\frac{-V'_{GS}t_{Si}}{2\gamma t_{box}}+\frac{C_{rsd}}{2C_{Si}}V'_{DS}-\frac{t_{box}}{2}\left(\frac{1}{C_2}\right)\beta_f\right)\right.$$

$$C_5=\left(1+\frac{t_{Si}}{2\gamma t_{box}}\right)\left(\frac{C_{Si}}{C_{Si}+C_{rsd}}\right)\left(\frac{t^*_{rsd}-2t_{box}}{t^*_{rsd}t_{box}}\right)$$

5.3 Threshold Voltage Formulation

The threshold voltage associated with front- and back-surfaces of the channel could be obtained using Kumar *et al.* (2014), similar to our consideration in Chapters 3 and 4.

$$\phi_{f\,min,min}\Big|_{V_G=V_{th\,f,b}}=2\phi^*_{f,Si}=\begin{cases}2\phi_{f,Si} & for,N_a>n_T\\ \phi_{f,Si}+\dfrac{kT}{q}ln\left(\dfrac{n_T}{n_i}\right) & for,N_a<n_T\end{cases} \quad (5.44)$$

where, $\phi_{f,Si}$ is the Fermi potential, n_T is a critical concentration of electron in the channel to turn on the device [Chen *et al.* (2003), Svilicic *et al.* (2010) and Kumar *et al.* (2014)].

Now, after using Eq. (5.44) in Eq. (5.41), we get the following equations for back-channel threshold voltages $V_{th\,b}$

$$V_{th\,b}=\frac{-b_b+\sqrt{b_b^{\,2}-4a_bc_b}}{2a_b} \quad (5.45)$$

where,

$$a_b=u_{b1}u_{b2}-\left(\frac{m_b}{2\alpha_b}\right)^2 \quad (5.46)$$

$$c_b = v_{b1}v_{b2} - \phi_{f,Si}{}^2 - \left(\frac{m_b}{2\alpha_b}\right)^2 - \frac{n_b}{\alpha_b}\phi_{f,Si} \tag{5.47}$$

$$b_b = u_{b1}v_{b2} + u_{b2}v_{b1} - \frac{m_b n_{f,b}}{2\alpha_b{}^2} - \frac{m_b}{\alpha_b}\phi_{f,Si} \tag{5.48}$$

$$v_{b1} = \frac{n_b\left(e^{\sqrt{\alpha_b}L} - 1\right) + \alpha_b\left[V_{bi}\left(e^{\sqrt{\alpha_b}L} - 1\right) + V_{DS}e^{\sqrt{\alpha_b}L}\right]}{\alpha_b\left(e^{2\sqrt{\alpha_b}L} - 1\right)} \tag{5.49}$$

$$v_{b2} = \frac{e^{\sqrt{\alpha_b}L}\left\{n_b\left(e^{\sqrt{\alpha_b}L} - 1\right) - \alpha_b\left[V_{bi}\left(1 - e^{\sqrt{\alpha_b}L}\right) + V_{DS}\right]\right\}}{\alpha_b\left(e^{2\sqrt{\alpha_b}L} - 1\right)} \tag{5.50}$$

$$u_{b1} = \frac{m_b\left(e^{\sqrt{\alpha_b}L} - 1\right)}{\alpha_b\left(e^{2\sqrt{\alpha_b}L} - 1\right)} \tag{5.51}$$

$$u_{b2} = \frac{m_b e^{\sqrt{\alpha_b}L}\left(e^{\sqrt{\alpha_b}L} - 1\right)}{\alpha_b\left(e^{2\sqrt{\alpha_{f,b}}L} - 1\right)} \tag{5.52}$$

$$m_b = \frac{\left[\frac{-2}{(t_{Si} + 2\gamma t_{ox})t_{Si}}\right]V'_{GS}}{\left[1 + \frac{t_{box}(t_{Si} + \gamma t_{ox})}{t_{Si}(t_{Si} + 2\gamma t_{ox})\gamma}\right]} \tag{5.53}$$

$$n_b = \frac{\left\{\frac{qN_a}{\varepsilon_{Si}} - \frac{2}{t_{Si}\gamma}\left(\frac{t_{Si} + \gamma t_{ox}}{t_{Si} + 2\gamma t_{ox}}\right)\left(\frac{V'_{BG}}{t_{box}} - \frac{V'_{DS}}{t^*_{rsd}}\right) + \frac{C_{rsd}}{C_{Si}t_{Si}}\left(\frac{2}{t_{Si} + 2\gamma t_{ox}} + \frac{1}{t_{Si}}\right)V'_{DS}\right\}}{\left[1 + \frac{t_{box}(t_{Si} + \gamma t_{ox})}{t_{Si}(t_{Si} + 2\gamma t_{ox})\gamma}\right]} \tag{5.54}$$

Similarly, we get the following equations for front-channel threshold voltages $V_{th\,f}$

$$V_{th\,f} = \frac{-b_f + \sqrt{b_f{}^2 - 4a_f c_f}}{2a_f} \tag{5.55}$$

where,

$$a_f = u_{f1}u_{f2} - \left(\frac{m_f}{2\alpha_f}\right)^2 \tag{5.56}$$

$$c_f = v_{f1}v_{f2} - \phi_{f,Si}{}^2 - \left(\frac{m_f}{2\alpha_f}\right)^2 - \frac{n_f}{\alpha_f}\phi_{f,Si} \tag{5.57}$$

$$b_f = u_{f1}v_{f2} + u_{f2}v_{f1} - \frac{m_f n_f}{2\alpha_f{}^2} - \frac{m_f}{\alpha_f}\phi_{f,Si} \tag{5.58}$$

$$v_{f1} = \frac{n_f\left(e^{\sqrt{\alpha_f}L} - 1\right) + \alpha_f\left[V_{bi}\left(e^{\sqrt{\alpha_f}L} - 1\right) + V_{DS}e^{\sqrt{\alpha_f}L}\right]}{\alpha_f\left(e^{2\sqrt{\alpha_f}L} - 1\right)} \tag{5.59}$$

$$v_{f2,b2} = \frac{e^{\sqrt{\alpha_f}L}\left\{n_f\left(e^{\sqrt{\alpha_f}L} - 1\right) - \alpha_f\left[V_{bi}\left(1 - e^{\sqrt{\alpha_f}L}\right) + V_{DS}\right]\right\}}{\alpha_f\left(e^{2\sqrt{\alpha_f}L} - 1\right)} \tag{5.60}$$

$$u_{f1} = \frac{m_f\left(e^{\sqrt{\alpha_f}L} - 1\right)}{\alpha_f\left(e^{2\sqrt{\alpha_f}L} - 1\right)} \tag{5.61}$$

$$u_{f2} = \frac{m_f e^{\sqrt{\alpha_f}L}\left(e^{\sqrt{\alpha_f}L} - 1\right)}{\alpha_f\left(e^{2\sqrt{\alpha_f}L} - 1\right)} \tag{5.62}$$

$$m_f = \frac{\left\{\frac{C_3}{C_1\gamma}\left(1 + \frac{t_{Si}}{2\gamma t_{box}}\right)\left(\frac{C_{Si}}{C_{Si} + C_{rsd}}\right)\left(\frac{t^*_{rsd} - 2t_{box}}{t^*_{rsd}t_{box}}\right)\left[-\frac{t_{Si}}{2\gamma t_{box}}\right] - 2\frac{C_{rsd}}{\varepsilon_{Si}L}\left[-\frac{t_{Si}}{2\gamma t_{box}}\right] - \frac{1}{\gamma t_{Si}t_{box}}\right\}}{1 + \frac{t_{box}}{2}\left(\frac{C_3}{C_2C_1}\right)}V'_{GS} \tag{5.63}$$

$$n_f = \frac{\begin{aligned}&\frac{qN_a}{\varepsilon_{Si}} - \frac{C_3}{C_1\gamma}\left(1 + \frac{t_{Si}}{2\gamma t_{box}}\right)\left(\frac{C_{Si}}{C_{Si} + C_{rsd}}\right)\left(\frac{t^*_{rsd} - 2t_{box}}{t^*_{rsd}t_{box}}\right)\left[\frac{C_{rsd}}{2C_{Si}}V'_{DS}\right] \\ &+ \frac{C_{rsd}}{\varepsilon_{Si}L}V'_{DS} - 2\frac{C_{rsd}}{\varepsilon_{Si}L}\left[\frac{C_{rsd}}{2C_{Si}}V'_{DS}\right] - \frac{C_3}{C_1\gamma}(C_4)\end{aligned}}{1 + \frac{t_{box}}{2}\left(\frac{C_3}{C_2C_1}\right)} \tag{5.64}$$

The threshold voltage of the device depends on that surface (front or back) of the device which will have the higher value of minimum surface potential (lesser barrier height). The device threshold voltage can be given as

$$V_{th} = \begin{cases} V_{thf}, & for \quad \phi_{f,min} > \phi_{b,min} \\ V_{thb}, & for \quad \phi_{f,min} < \phi_{b,min} \end{cases} . \tag{5.65}$$

Further, the quantum effects induced correction term ΔV_{th} is added in the threshold voltage model of Eq. (5.65) models like our previous consideration in Chapters 3 and 4 [Dort *et al.* (1992)].

5.4 Subthreshold Current Formulation

The subthreshold current is mainly dominated by the diffusion phenomenon and is proportional to the carrier concentration at the minimum surface potential position (virtual cathode) as calculated in section 5.3. Therefore, by employing the 2D surface potential function derived in section 5.2, the expression of subthreshold current can be written as follows:

$$I_{sub} = \frac{qD_n n_i^2}{L_e N_a}\left(1 - exp\left(-\frac{V_{DS}}{V_T}\right)\right)\int_0^{t_{Si}} exp\left(\frac{\phi_{vc}(y)}{V_T}\right)dy \tag{5.66}$$

where, $\phi_{vc}(y)$ is given in (5.42) and (5.43); the other parameters are given in section 3.4 of Chapter 3.

Now, Eq. (5.66) has been solved by following the method which is given in section 3.4 of Chapter 3, and the obtained final subthreshold current expression, I_{sub} is

$$I_{sub} = \frac{qD_n n_i^2}{L_e N_a}\left(1 - exp\left(-\frac{V_{DS}}{V_T}\right)\right)V_T\left[\frac{I_f}{E_f} + \frac{I_b}{E_b}\right] \tag{5.67}$$

where,

$$I_f = exp\left(\frac{\phi_{vc}(y=0)}{V_T}\right) - exp\left(\frac{\phi_{vc}(y=y_m)}{V_T}\right) \tag{5.68}$$

$$I_b = exp\left(\frac{\phi_{vc}(y=y_m)}{V_T}\right) - exp\left(\frac{\phi_{vc}(y=t_{Si})}{V_T}\right) \tag{5.69}$$

$$E_f = (\phi_{vc}(y=0) - \phi_{vc}(y=y_m))/y_m \tag{5.70}$$

$$E_b = (\phi_{vc}(y=y_m) - \phi_{vc}(y=t_{Si}))/(t_{Si} - y_m) \tag{5.71}$$

5.5 Subthreshold Swing Formulation

This section presents the modeling of subthreshold swing of short-channel Re-S/D SOI MOSFETs with back-gate control. Subthreshold swing (S) of Re-S/D SOI MOSFETs with back-gate control can be written as [Dey *et al.* (2008), Svilicic *et al.* (2010)]

$$S = \begin{cases} ln10.V_T.\left(\frac{d\phi_{f\,min}}{dV_{GS}}\right)^{-1} & for\,\phi_{f\,min} > \phi_{b\,min} \\ ln10.V_T.\left(\frac{d\phi_{b\,min}}{dV_{GS}}\right)^{-1} & for\,\phi_{b\,min} > \phi_{f\,min} \end{cases} \tag{5.72}$$

By substituting Eq. 5.41 into Eq. 5.72, the following subthreshold slope expression for Re-S/D SOI MOSFETs with back-gate control is obtained

$$S = \begin{cases} \frac{ln10.V_T}{\alpha_f}\left[\frac{A_f e^{\sqrt{\alpha_f}L} + B_f}{\sqrt{A_f B_f}\left(e^{\sqrt{\alpha_f}L}+1\right)} - 1\right]\left[\frac{K_f}{1+\frac{t_{box}}{2}\left(\frac{C_3}{C_2 C_1}\right)}\right] & for\,\phi_{f\,min} > \phi_{b\,min} \\ \frac{ln10.V_T}{\alpha_b}\left[\frac{A_b e^{\sqrt{\alpha_b}L} + B_b}{\sqrt{A_b B_b}\left(e^{\sqrt{\alpha_b}L}+1\right)} - 1\right]K_b & for\,\phi_{b\,min} > \phi_{f\,min} \end{cases}^{-1} \tag{5.73}$$

where,

$$K_f = -\frac{C_3}{C_1\gamma}\left(\frac{C_{Si}}{C_{Si}+C_{rsd}}\right)\left(-\frac{t_{Si}}{2\gamma t_{box}}\right)\left[1-\left(1+\frac{t_{Si}}{2\gamma t_{box}}\right)\left(\frac{t^*_{rsd}-2t_{box}}{t^*_{rsd}t_{box}}\right)\right] - 2\frac{C_{rsd}}{\varepsilon_{Si}L}\left(-\frac{t_{Si}}{2\gamma t_{box}}\right) - \frac{1}{\gamma t_{Si}t_{box}} \tag{5.74}$$

$$K_b = \frac{-2}{\gamma}\left[\frac{\gamma + 2\gamma t_{box} + t_{Si}}{t_{Si}^2 + (2\gamma + 1)t_{box}t_{Si} + \gamma t_{box}^2}\right] \tag{5.75}$$

5.6 Results and Discussion

In this section, we have compared the analytical results obtained from the proposed models with the numerical simulation data obtained by simulating the device structure under consideration with a commercially available 2D device simulator ATLAS^{TM}.

5.6.1 Surface Potential

Figure 5.2 shows the variation of front-channel and back-channel surface potentials along the channel length direction for two different back-gate bias voltages (V_{BG}=0V, -2V). For V_{BG}=0V, it could be observed that the minimum of back-channel surface potential is higher than that of front-channel minimum surface potential. This is attributed to the strong coupling between extended-source/drain and back-channel which in turn causes an early inversion at the back-channel compared to the front-channel. Since the inversion takes place at Si-BOX interface rather than Si-SiO_2 interface, the front-gate does not control the channel charge effectively. Subsequently, the device becomes prone towards the short-channel effects, which is one of the drawbacks of Re-S/D SOI MOSFETs. The above mentioned behavior of the Re-S/D SOI MOSFET has been reported in Chapters 3 and 4. However, a negative voltage at the back-gate lifts the minimum of front-surface potential higher than that of back-surface potential. And subsequently, the front-surface of the channel gets inverted before the back-surface, like the FD SOI MOSFETs. Thus, the introduction of back-gate in Re-S/D SOI MOSFETs is expected to improve the short-channel effects immunity of the device, which is investigated hereafter in this section.

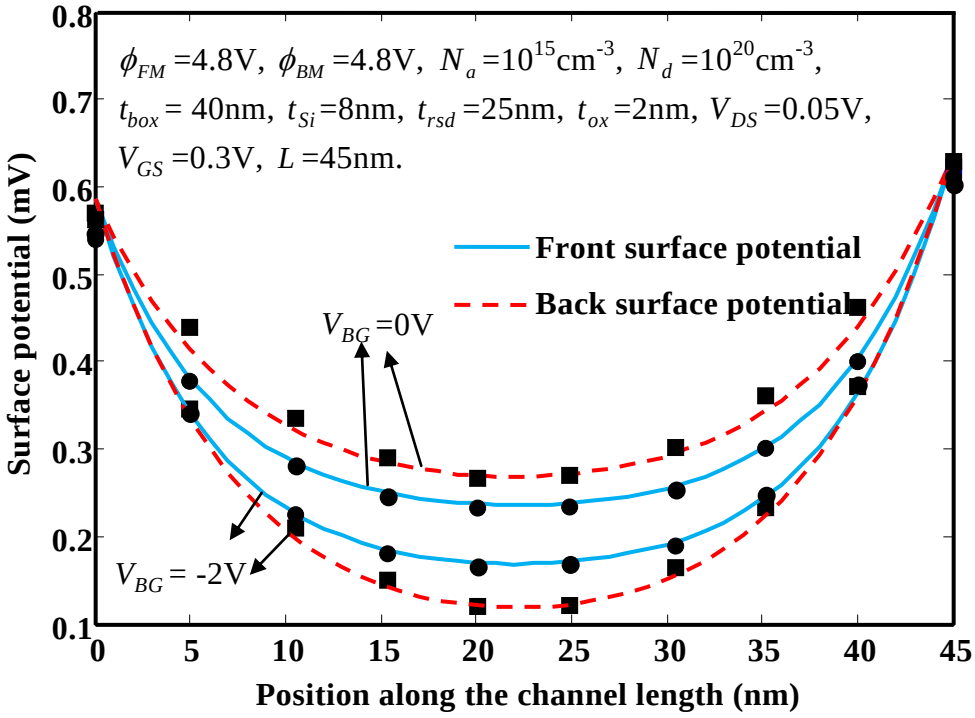


Fig. 5.2: Surface potential along the channel length at front-channel and back-channel

5.6.2 Threshold Voltage

Figure 5.3 displays the front-channel and back-channel threshold voltage along the channel length for different back-gate voltages. It also includes the corresponding numerical simulation data of threshold voltage obtained from ATLAS simulation. It could be observed that the back-channel threshold voltage results obtained from the developed model are in close agreement with the ATLAS simulation results for V_{BG} =0, and 1V. But in case of V_{BG} = -1V, the numerical simulation results match with the model results which are associated with the front-channel. This is in complete agreement with the observations of Fig. 5.2 where, for V_{BG} = -1V, the minimum of front-surface potential is higher than the same of back-surface potential resulting in the threshold voltage being associated with the front-channel. Further, the threshold voltage roll-off at a shorter channel length (L<60nm) is found to be lesser in case of negative back-gate bias voltage.

Figure 5.4 shows the variation in the front-channel threshold voltage due to variation in the Si-body thickness. It is observed that the roll-off increases at higher channel thickness due to the reduction in the controllability of the gate electrodes. Thus, thinner channel provides better control on short-channel effects.

In Fig. 5.5, front-channel threshold voltage is plotted against channel length at t_{rsd} = 0nm, 10nm, and 25nm to show the threshold voltage sensitivity against the source/drain depth in the BOX. The device with t_{rsd} = 0nm is nothing but an asymmetrical DG MOSFET, which shows better SCE immunity than recessed-S/D structure. From the figure, it can be observed that the threshold voltage is found to be decreased with the increase of source/drain penetration in the BOX. The decrease in the threshold voltage is attributed to the loss of the gate control and growing influence of the source and drain.

Figure 5.6 shows the dependence of the front-gate and back-gate threshold voltage on the back-gate bias voltage (V_{BG}). It is observed from the figure that the threshold voltage V_{th} increases almost linearly with decreasing V_{BG}. Figure 5.6 also reflects the results of Fig. 5.3 i.e. the back-gate bias voltage effectively control the threshold voltage. For positive back-gate voltage, back-channel gets inverted before the front-channel. However, a negative back-gate voltage causes peak of inversion charge density to shift back to the Si-SiO_2 interface.

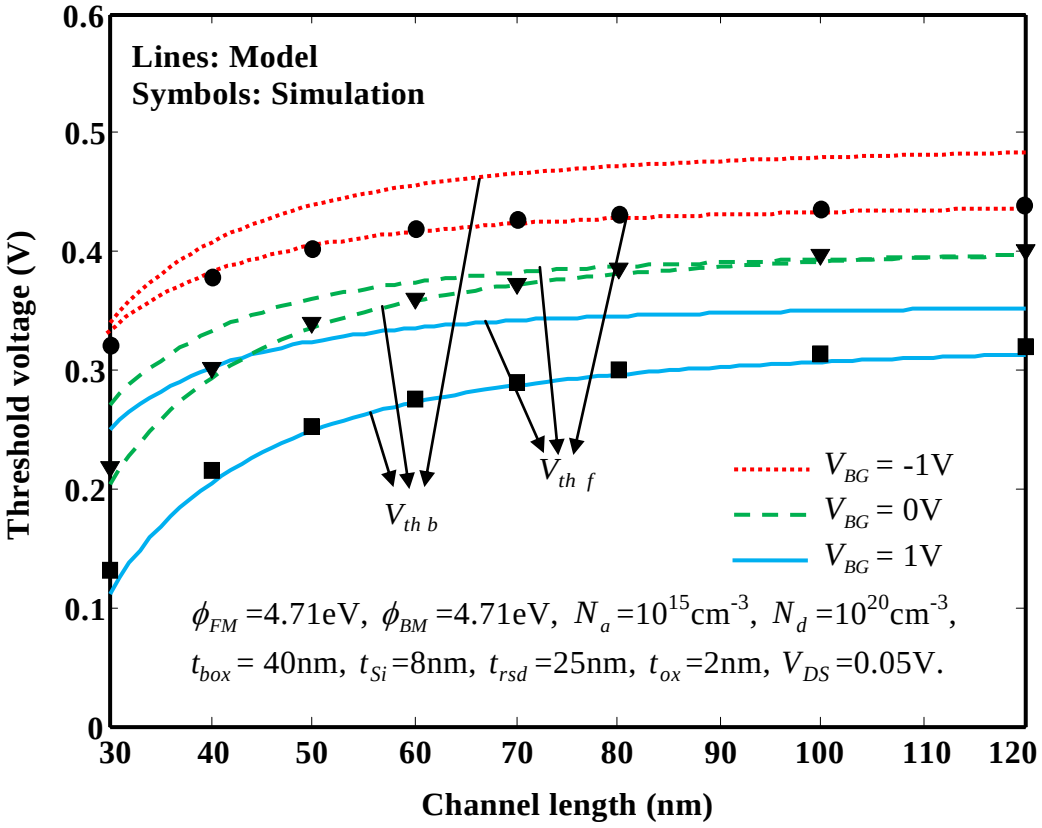


Fig. 5.3: Threshold voltage along the channel length for various back-gate bias voltages

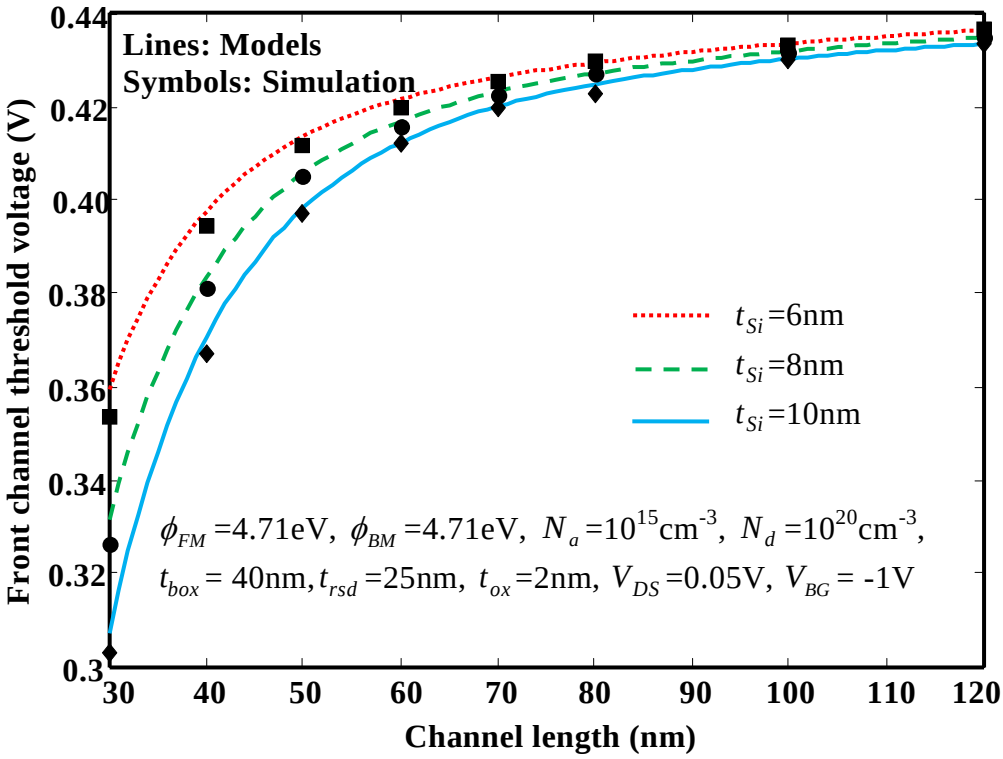


Fig. 5.4: Front-channel threshold voltage along the channel length for various silicon channel thickness

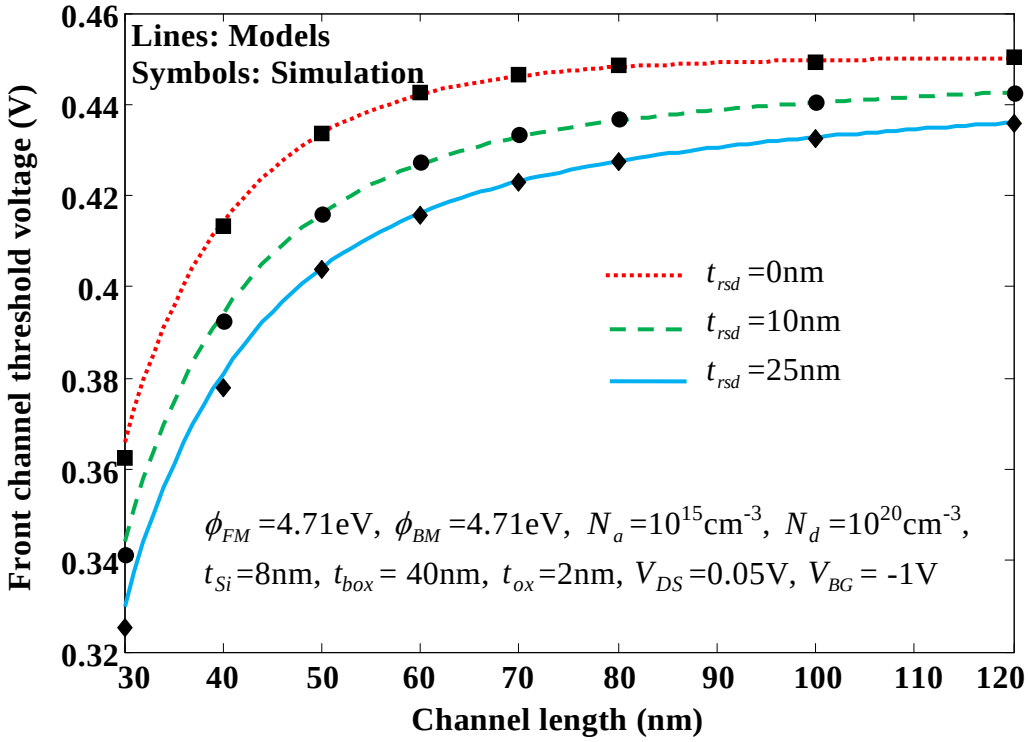


Fig. 5.5: Front-channel threshold voltage versus gate length for varying recessed oxide thickness

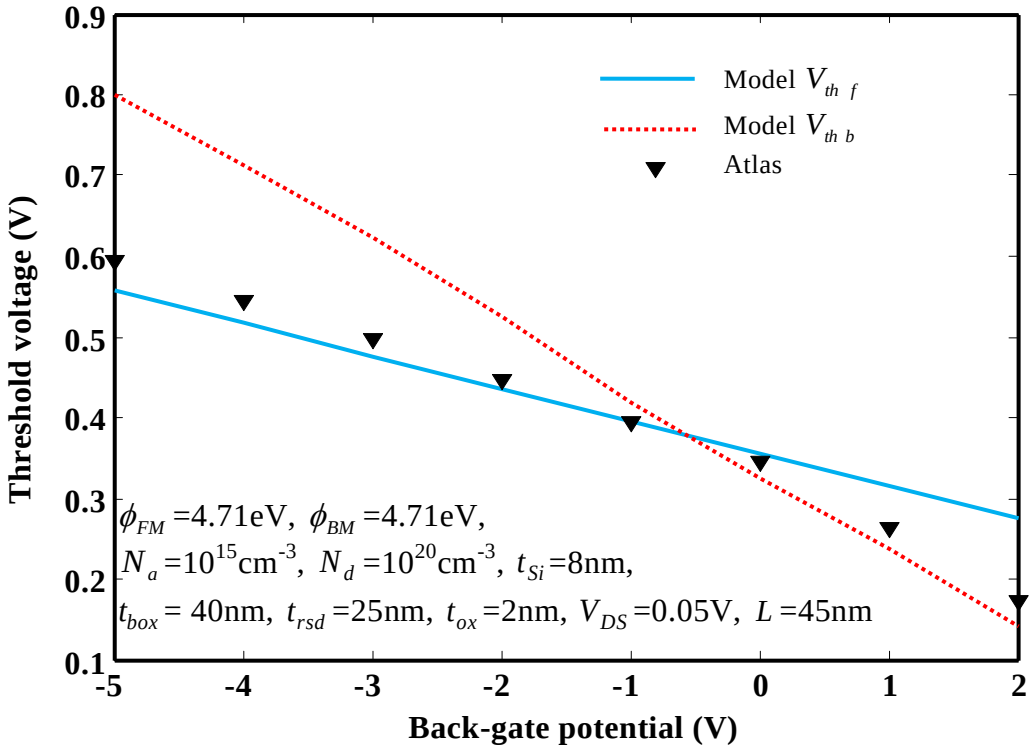


Fig. 5.6: Front- and back-threshold voltage versus back-gate potential

5.6.3 Subthreshold Current

The subthreshold current (I_{Sub}) with the gate voltage for three different buried oxide thicknesses (t_{box}) is plotted in Fig. 5.7. It should be noted that the present subthreshold current model of Eq. (5.79) is based on only the diffusion phenomenon of current transport, and therefore, the subthreshold current can be observed in agreement with the simulation results below the threshold voltage of devices. It is observed from Fig. 5.7 that for the fixed values of V_{GS} the subthreshold current is decreased with the decrease in BOX thickness. This decrease of I_{Sub} using a thinner BOX is due to a higher impact of back-gate reverse bias on it. In Fig. 5.8, subthreshold current has been plotted against the applied gate voltage for different values of the channel lengths. The subthreshold current is observed to be increased with the reduction in the channel length due to the increased short-channel effects. It is also observed that decreasing the channel length of the device from 40nm to 30nm increases the subthreshold leakage current by two orders of magnitude.

The subthreshold current (I_{Sub}) variation with the gate to source voltage V_{GS} for different recessed-source/drain thickness (t_{rsd}) is considered in Fig. 5.9. It is found that at t_{rsd} = 0nm (conventional SOI with back-gate), I_{Sub} is ~ 2*10^{-10} A/μm and as t_{rsd} increases to 25nm, I_{Sub} becomes ~ 5*10^{-10} A/μm. It is due to the fact that a deeper recessed source/drain offers higher short-channel effects due to the stronger coupling between recessed-source/drain and channel region. Figure 5.10 displays the impact of different back-gate voltages over the subthreshold current variation. The subthreshold current is found to be decreased with decreasing back-gate voltage. This is because the reverse back-gate voltage decreases the front-surface barrier height, which causes the inversion layer at the front-surface of the channel like conventional SOI MOSFETs.

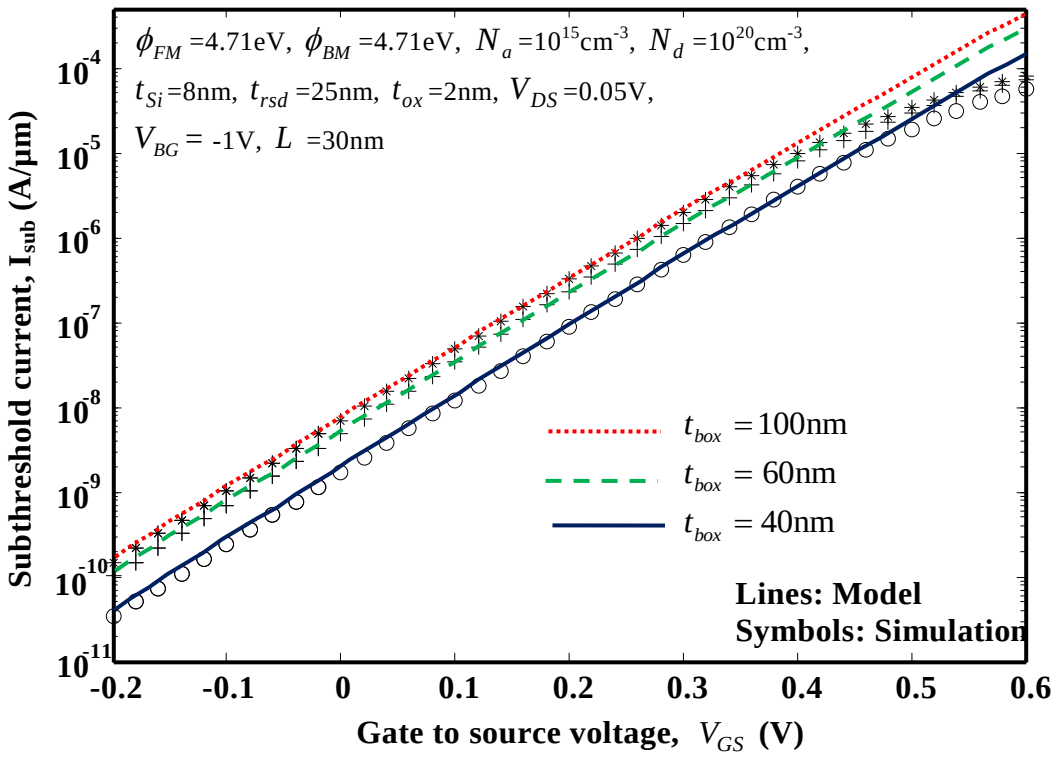


Fig. 5.7: Subthreshold current versus gate to source voltage for different buried oxide thickness.

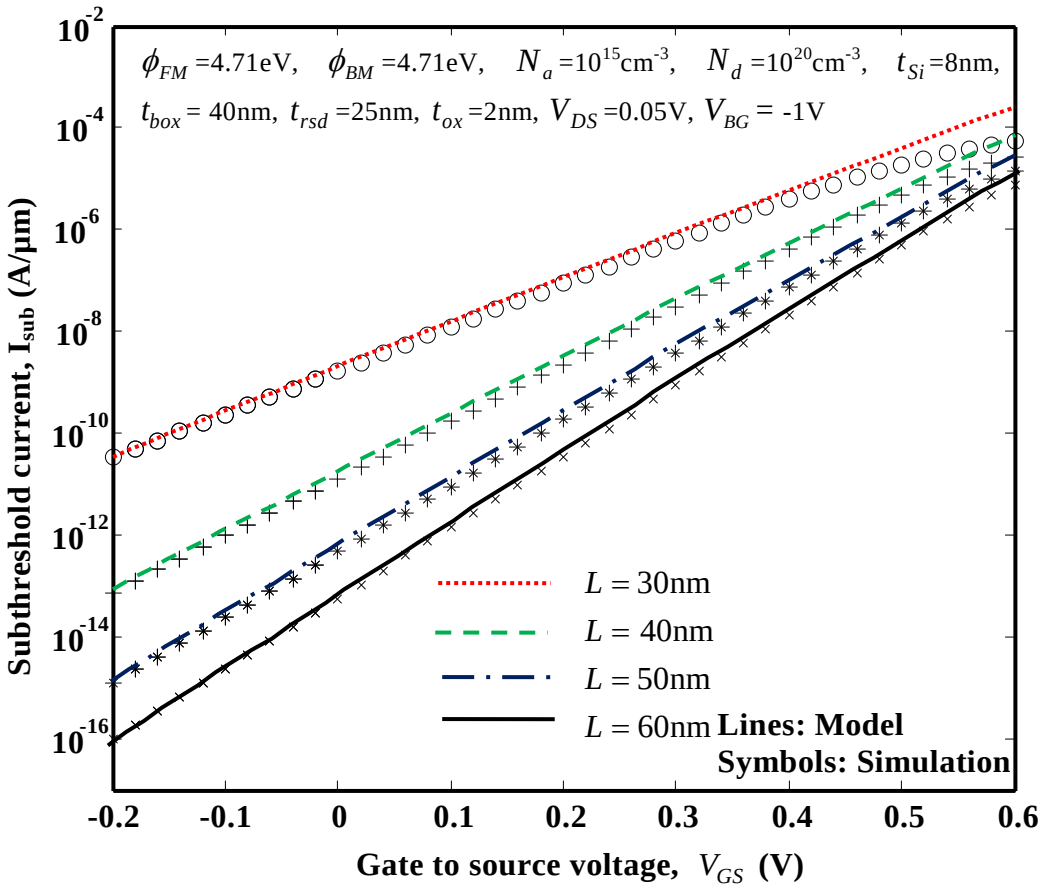


Fig. 5.8: Subthreshold current versus gate to source voltage for different channel Lengths.

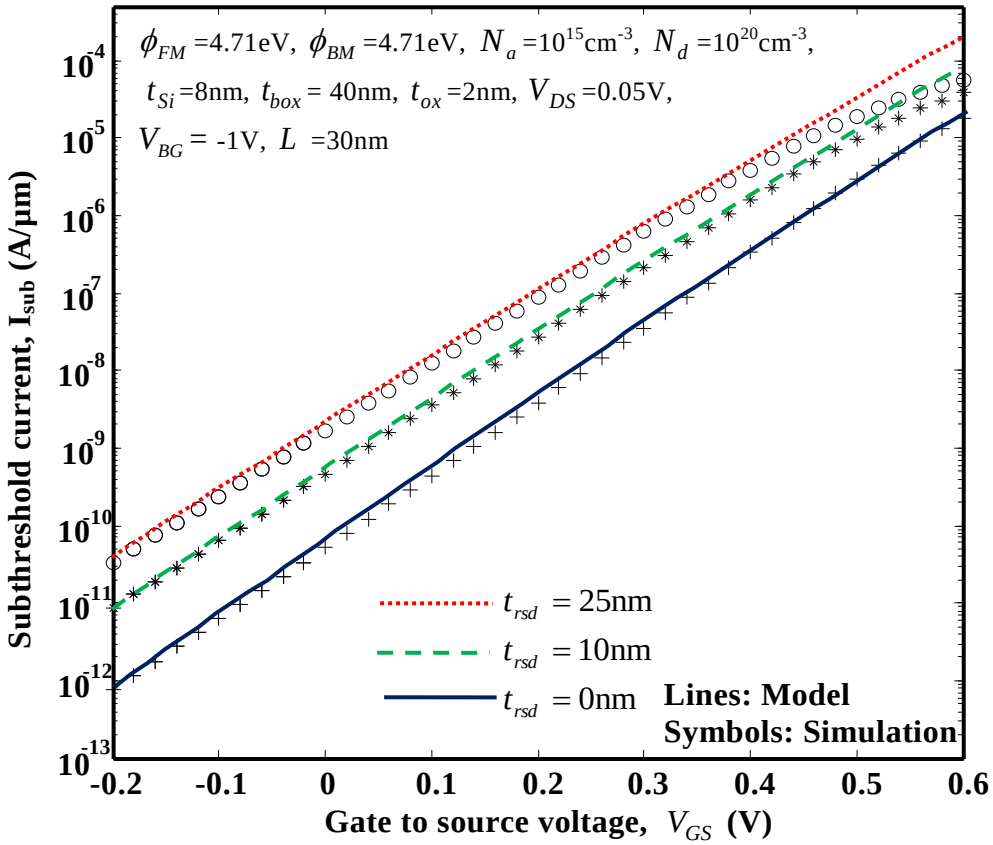


Fig. 5.9: Subthreshold current versus gate to source voltage for different recessed source/drain thicknesses

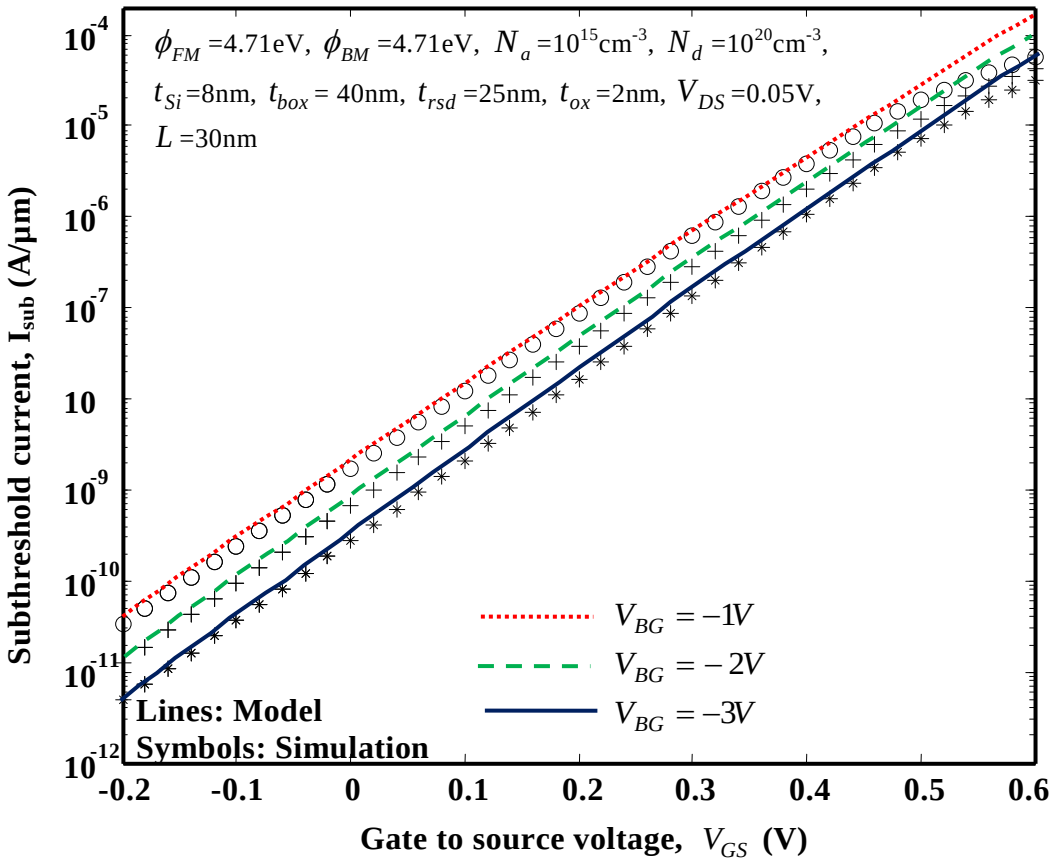


Fig. 5. 10: Subthreshold current versus gate to source voltage for different back-gate voltage

5.6.4 Subthreshold Swing(*S*)

The variation of the subthreshold swing (S) against the channel length is shown in Fig. 5.11 for different channel thicknesses. It is observed that at L =20nm and t_{Si}=8nm the subthreshold swing, S is found to be ~ 162mV/Dec. and as t_{Si} decreases to 6nm, S becomes ~ 128mV/Dev. i.e., the subthreshold swing is increasing rapidly with the increase in the silicon channel thickness.

Figure 5.12 shows the variation of subthreshold swing (S) against the device channel lengths for different BOX thicknesses. The parameter S is found to be increased with the shrinkage of channel length < 70nm resulting in the poor switching characteristics of the device. However, for a fixed gate-length, the switching characteristics are observed to be improved with decreasing values of gate oxide thickness. Since, the gate will be in better position to control the channel for smaller gate oxide thickness, the

above results seem to be well justified. The impact of back-gate voltage on the subthreshold swing (*S*) is presented in Fig. 5.13. It is observed that the reverse back-gate bias voltage can improve switching characteristics immensely. As the reverse back-gate voltage decreases from -1V to -3V the switching characteristics are found to be improved by ~ 30mV/Dec by keeping the other parameters constant.

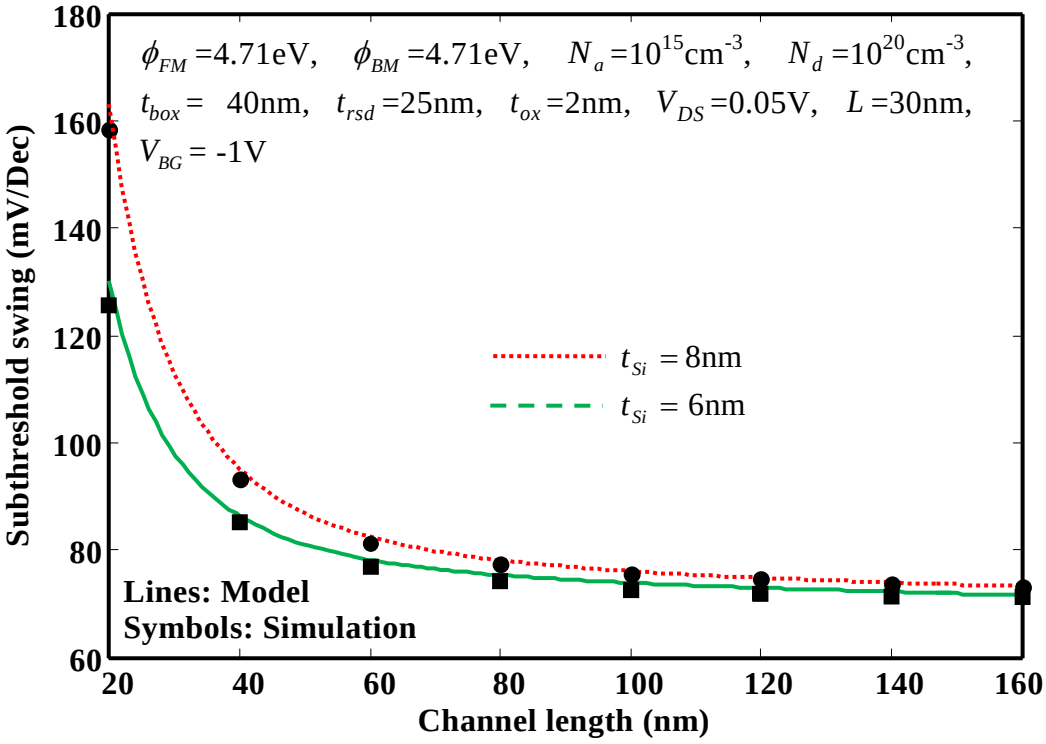


Fig. 5.11: Subthreshold swing variation with channel length for different silicon thicknesses.

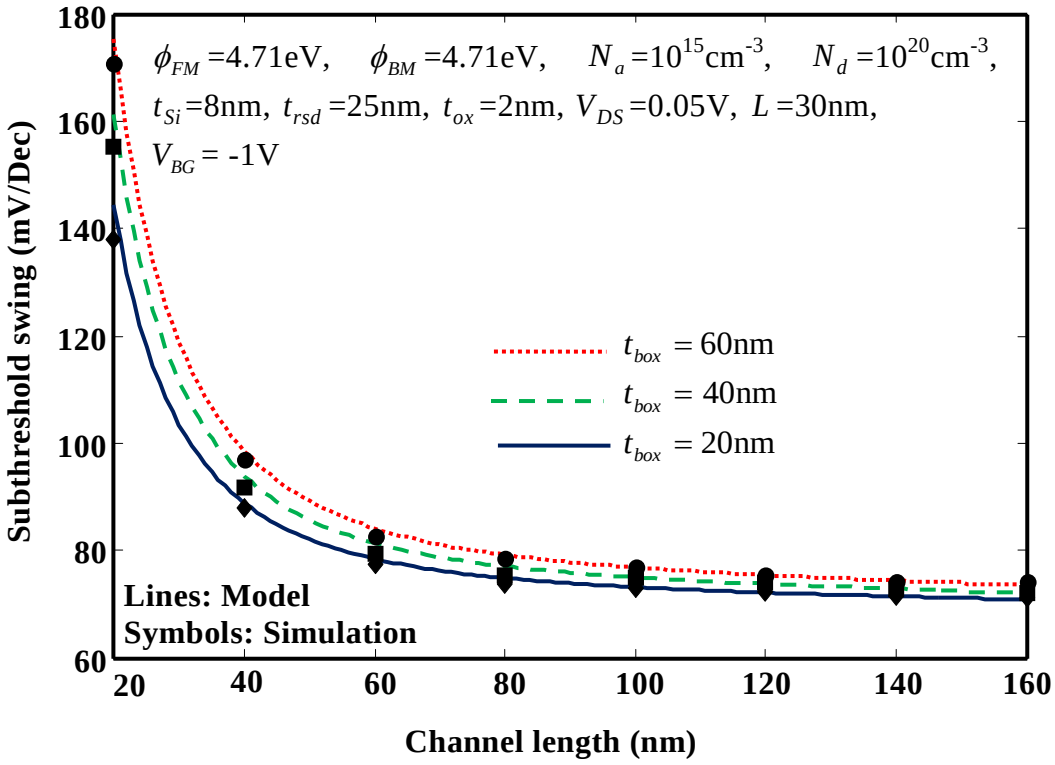


Fig. 5. 12: Subthreshold swing variation with channel length for different buried oxide thickness

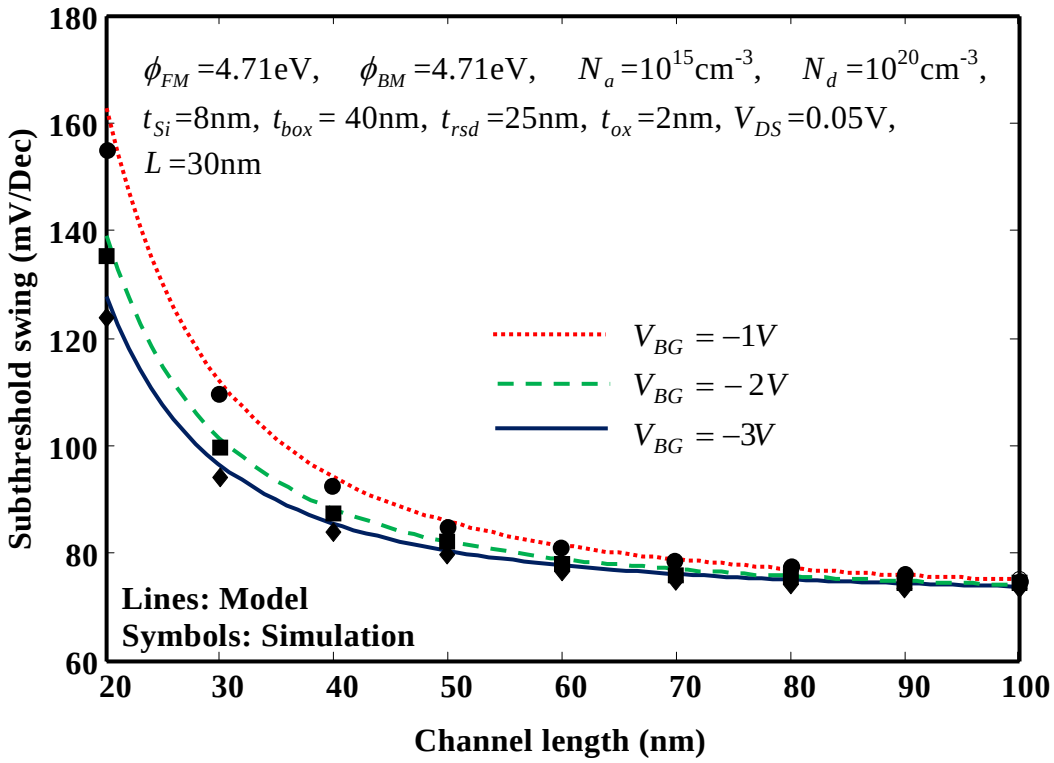


Fig. 5. 13: Subthreshold swing variation with channel length for different back-gate voltage.

5.7 Summary and Conclusion

In this chapter, threshold voltage, subthreshold swing and subthreshold current models are formulated for short-channel back-gated Re-S/D SOI MOSFETs by considering the 2D effects in both channel region and buried oxide (BOX) layer. The variations in the threshold voltage, subthreshold current and subthreshold swing have been analyzed against the back-gate bias voltage, channel thickness, BOX thickness, gate oxide thickness and recessed source/drain thickness. It has been found that a negative back-gate bias voltage shift the peak of inversion charge density from back-channel to the front-channel resulting in an excellent short-channel-effects immunity in the device. The V_{th} roll-off and subthreshold swing roll-up of the Re-S/D SOI MOSFET are found to be significantly decreased with reverse back-gate bias voltage compared to the positive or no potential at the back-gate. Hence, the use of negative bias voltage is a potential solution to reduce the short-channel effects in the Re-S/D SOI MOSFET. The excess short-channel effects owing to the recessed-source/drain thickness may also be

compensated by carefully applying the reverse back-gate bias voltage. Moreover, the model results are found to be in very good agreement with numerical simulation data obtained from ATLAS^{TM}.

Chapter 6

Conclusion and Future Scopes of Work

6.1 Introduction

The present dissertation reports the analytical modeling and simulation of subthreshold characteristics of short-channel fully-depleted (FD) recessed-source/drain (Re-S/D) SOI MOSFETs. In Re-S/D SOI MOSFETs, the source and drain are extended deeper into the buried oxide (BOX) region in order to reduce total series resistance and facilitate better source and drain contacts. Recessing source and drain deeper into the BOX improves the 'on' current of SOI MOSFETs. Further, CMOS performance boosters such as high-*k* gate-dielectric, multi-gate and back-gate etc. help to improve the on-current of the device. However, the subthreshold characteristics of Re-S/D SOI MOSFETs need to be analyzed rigorously as the extended source and drain may control the channel and, hence, diminish the subthreshold performance. Further, it is also interesting to observe how the presence of a performance booster affects the subthtreshold behavior of the device. The present chapter has been devoted to summarize the works carried out in this dissertation and conclude the major observations which are already presented in the previous chapters of this dissertation.

6.2 Chapter-wise Summary and Conclusion

Chapter 1 presents a brief history of semiconductor devices. MOSFET scaling techniques and its effect on the performance of the CMOS devices have also been discussed. Various CMOS technology boosters including channel engineering and gate material engineering have been introduced. The problems associated with the multi-gate

field-effect transistors (MuGFETs) are briefly discussed. The salient features, challenges and remedies of FD ultra-thin SOI MOSFETs are also presented in Chapter 1. Finally, suggestions for further work have been outlined at the end of this chapter.

Chapter 2 presents a brief review of SOI MOSFETs. Some state-of-the-art research works on SOI MOSFETs have been briefly discussed. Some major findings of the literature review are given below:

- The SOI-MOSFET is a highly scalable structure. The device could be used to fabricate a highly dense integrated circuit as the device offers higher drive current, higher scalability etc. as compared to the conventional CMOS devices.
- A number of studies have shown that the SOI MOS structures with more than one material for gate contacts can provide better immunity to short-channel effects (SCEs) and hot-carrier effects (HCEs). Thus, the theoretical modeling of the subthreshold characteristics could be very important to study the switching characteristics of these devices.
- Analytical modeling of the subthreshold characteristics of Re-S/D SOI MOSFET with high-*k* gate-dielectric could be very useful for studying the fringing field effects on the threshold voltage, subthreshold swing and subthreshold current of the device.
- Further, there is an ample scope of developing analytical models for the subthreshold characteristics of Re-S/D SOI MOSFETs with back-gate control.

Chapter 3 presents the analytical modeling and simulation of the subthreshold characteristics such as threshold voltage, subthreshold current and swing for a short-channel dual-metal-gate (DMG) recessed-source/drain (Re-S/D) SOI MOSFET. The proposed models are validated by comparing the theoretical results with the simulation data obtained by using the commercially available ATLAS^{TM} device simulation software from Silvaco International.

The major observations are given as follows:

- It is observed that the back-channel minimum surface potential is greater than the same of front-channel surface potential by ~70 mV for ϕ_{M1}=4.8eV, ϕ_{M2}=4.6eV, L=60nm, $L_1 : L_2 = 1:1$, t_{Si}=10nm, t_{ox}=2nm, t_{rsd}=30nm, t_{box}=100nm, d_{box}=3nm, N_a=10^{16}cm^{-3}, V_{DS}=0.1V, V_{GS}=0.1V. Therefore, the back-surface of the channel gets inverted before the front-surface. This trend is observed for undoped short-channel length devices.

- The reduction in the gate oxide, buried oxide and recessed S/D thicknesses effectively control the SCEs.

- It is found that the increase in the recessed source/drain thickness increases the SCEs due to a stronger coupling between extended source/drain and back-surface of the channel region. However, reducing the gate oxide and channel thicknesses compensate the increased SCEs effectively

- The control to screen gate length ratio ($L_1 : L_2$) may act as an additional controlling parameter which can modulate the subthreshold characteristics of DMG Re-S/D SOI MOSFETs.

- The increased threshold voltage roll-off, subthreshold swing and subthreshold current because of recessing source and drain deeper into the BOX can be suppressed by choosing the device parameters judiciously

- The developed models include the effect of various device parameters such as the thickness of gate oxide, channel, buried oxide and recessed source/drain, control to screen gate length ratio, and channel length.

- The model results are observed to be in good agreement with the simulation data, which confirms the validity of the proposed model.

Chapter 4 presents the modeling and simulation of the subthreshold characteristics of the Re-S/D SOI MOSFET with high-*k* gate-dielectric material. The developed models estimate the effect of fringing fields, due to thicker physical thickness of high-*k*

dielectrics, on the subthreshold characteristics of Re-S/D SOI MOSFETs. The effects of the gate-dielectric permittivity, spacer oxide permittivity, spacer width, gate length, and the width of device are incorporated in the model. The major observations of Chapter 4 are given as follows.

- Different high-*k* dielectrics such as $HfSiO_4$, HfO_2 and La_2O_3 were used as the insulators to examine the subthreshold characteristics of Re-S/D SOI MOSFET with high-*k* gate-dielectric material.

- The surface potential, which was obtained from 2D electrostatic potential, was modified by adding a potential $V(x)$ in order to capture the effects of high-*k* dielectric induced fringing fields.

- A drop of ~30mV is observed in the threshold voltage when HfO_2 replaces SiO_2 as a gate dielectric with ϕ_M =4.8eV, N_a =10^{16}cm^{-3}, N_d =10^{20}cm^{-3}, t_{box} =200nm, t_{Si} =8nm, t_{rsd} =30nm, t_{ox} =1.5nm, V_{DS} =0.1V, V_{GS} =0.1V

- It is also observed that decrease in the gate oxide thickness and channel thickness reduces the threshold voltage roll-off, subthreshold current and subthreshold swing with better gate electrostatics in the channel region.

- A slight degradation in subthreshold characteristics is observed with high-*k* gate-dielectric materials due to the induced fringing field lines from gate electrode to source/drain.

- The present models predict the subthreshold characteristics such as threshold voltage, subthreshold current and subthreshold swing of Re-S/D SOI MOSFETs correctly for a wide range of gate dielectric materials and other device parameters.

- The model results are observed to be in good agreement with the simulation data, which confirms the validity of the proposed models.

Chapter 5 presents the modeling and simulation of the effects of back-gate engineering on the subthreshold characteristics of Re-S/D SOI MOS structures. The 2D effects of

back-gate bias voltage are considered in both channel region and buried oxide (BOX) layer. The developed models are tested for wide variations in parameters like back-gate voltage, the channel length, the silicon thickness, the front-gate oxide thickness, the buried oxide thickness and the recessed source/drain thickness. The main results of this chapter can be written as follows:

- As the BOX layer thickness is reduced, the control of the back-gate bias placed underneath the SOI layer over the channel is increased.
- It has been found that a negative back-gate bias voltage (> -0.5V) shifts the peak of inversion charge density from back-surface of the channel to the front-surface resulting in an excellent short-channel-effects immunity in the device.
- Moreover, the threshold voltage can be changed by changing reverse back-gate bias voltage. This dynamic threshold voltage control can be used to optimize the power verses delay trade-off.
- Our investigations reveal that the threshold voltage roll-off is improved by ~55mV as the channel thickness t_{Si} reduces from 10nm to 6nm for ϕ_{FM} =4.71eV, ϕ_{BM} =4.71eV, N_a =10^{15}cm^{-3}, N_d =10^{20}cm^{-3}, t_{box} = 40nm, t_{rsd} =25nm, t_{ox} =2nm, V_{DS} =0.05V, V_{BG} = -1V due to the improvement in the gate electrostatics on the channel.
- By varying the back-gate bias voltage from -1V to -3V the subthreshold current and subthreshold swing can be reduced by ~one order of magnitude and ~35mV/Dec, respectively by keeping the other parameters constant.
- The degradation of the threshold voltage, subthreshold current and subthreshold swing owing to the increased Re-S/D thickness can be compensated by applying a suitable negative bias voltage at the back-gate.
- The model results are in good agreement with the simulation data obtained by using the commercially available 2D device simulator ATLAS^{TM}.

6.3 Suggestions for Further Work

We know that research is a continuous process and no dissertation is complete in every respect.

The work carried out in this dissertation may be further in the following areas.

- It has been observed in the literature that the mobility of the charge carriers improves by a strain in the channel, hence modeling and simulation of the subthreshold characteristics of the short-channel Re-S/D strained-Si SOI MOSFETs could be done.
- Since the analog and radio frequency (RF) performance evaluation is very important for a device to check its suitability for RF circuit design and system-on- chip applications, the analog and RF analysis of Re-S/D SOI MOSFETs could be done in detail.
- A continuous drain current model valid in all regions of the device operation is required for short-channel Re-S/D SOI MOSFETs.
- The analytical models for various device capacitors could be presented in the subthreshold regime of the device operation
- Unified 2D models can be developed for studying the subthreshold characteristics of the Re-S/D SOI MOSFETs including the effects of double/triple materials for the gate electrode, high-*k* dielectric material, and back-gate biasing
- Experimental results can provide further confirmation of the efficacy of developed models.

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