DEVELOPMENT OF EFFICIENT SOFT SWITCHING SYNCHRONOUS BUCK CONVERTER TOPOLOGIES FOR LOW VOLTAGE HIGH CURRENT APPLICATIONS

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by

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This is to certify that the work presented in this dissertation entitled *"Development of efficient soft switching synchronous buck converter topologies for low voltage high current applications"* by "*S.Shiva Kumar"*, Roll Number: 512EE1014, is a record of original research carried out by him under my supervision and guidance in partial fulfilment of the requirements of the degree of *Doctor of Philosophy* in *Electrical Engineering*. Neither this dissertation nor any part of it has been submitted for any degree or diploma to any institute or university in India or abroad.

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I, S. Shiva Kumar, Roll Number 512EE1014 hereby declare that this dissertation entitled *"Development of efficient soft switching synchronous buck converter topologies for low voltage high current applications"* represents my original work carried out as a doctoral student of NIT Rourkela and, to the best of my knowledge, it contains no material previously published or written by another person, nor any material presented for the award of any other degree or diploma of NIT Rourkela or any other institution. Any contribution made to this research by others, with whom I have worked at NIT Rourkela or elsewhere, is explicitly acknowledged in the dissertation. The works of other authors cited in this dissertation have been duly acknowledged under the section "Bibliography". I have also submitted my original research records to the doctoral scrutiny committee for evaluation of my dissertation.

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Abstract

Switched mode power supplies (SMPS) have emerged as the popular candidate in all the power processing applications. The demand is soaring to design high power density converters. For reducing the size, weight, it is imperative to channelize the power at high switching frequency. High switching frequency converters insist upon soft switching techniques to curtail the switching losses. Several soft switching topologies have been evolved in the recent years.

Nowadays, the soft switching converters are vastly applied modules and the demand is increasing for high power density and high efficiency modules by minimizing the conduction and switching losses. These modules are generally observed in many applications such as laptops, desktop processors for the enhancement of the battery life time. Apart from these applications, solar and spacecraft applications demand is increasing progressively for stressless and more efficient modules for maximizing the storage capacity which inturn enhances the power density that improves the battery life to supply in the uneven times.

Modern trends in the consumer electronic market focus increases in the demand of lower voltage supplies. Conduction losses are significantly reduced by synchronous rectifiers i.e., MOSFET's are essentially used in many of the low voltage power supplies. Active and passive auxiliary circuits are used in tandem with synchronous rectifier to diminish the crucial loss i.e., switching loss and also it minimizes the voltage and current stresses of the semiconductor devices.

The rapid progress in the technology and emerging portable applications poses serious challenges to power supply design engineers for an efficient power converter design at high power density. The primary aim is to design and develop high efficiency, high power density topologies like: buck, synchronous buck and multiphase buck converters with the integration of soft switching techniques to minimize conduction and switching losses sustaining the voltage and current stresses within the tolerable range.

In this work, two ZVT-ZCT PWM synchronous buck converters are introduced, one with active auxiliary circuit and the other one with passive auxiliary circuit. The operating principle and comprehensive steady state analysis of the ZVT-ZCT PWM synchronous buck converters are presented. The converters are designed to have high efficiency and low voltage that is suitable for high power density application. The semiconductor devices used in the topologies in addition to the main switch operate with soft switching conditions. The

topologies proposed render a large overall efficiency in contrast to the contemporary topologies. In addition the circuit's size is less, reliable and have high performance-cost ratio.

The new generation microprocessor demands the features such as low voltage, high current, high power density and high efficiency etc., in the design of power supplies. The supply voltage for the future generation microprocessors must be low, in order to decrease the power consumption. The voltage levels are dripping to a level even less than 0.7V, and the power consumption increases as there is an increase in the current requirement for the processor. In order to meet the demands of the new generation microprocessor power supply, a soft switching multiphase PWM synchronous buck converter is proposed. The losses in the proposed topology due to increasing components are pared down by the proposed soft switching technique.

The proposed converters in this research work are precisely described by the mathematical modelling and their operational modes. The practicality of the proposed converters for different applications is authenticated by their simulation and experimental results.

Keywords*: *Soft switching; Zero Voltage Transition; Zero Current Transition; Pulse-width modulation; Synchronous Buck Converter; Multphase Buck Converter.

Notations

R_{dson}	-On resistance of MOSFET
C_{oss}	-MOSFET Output Capacitance
v_{phase}	-Instantaneous voltage at output
I_L	-Load current
V_D	-Drain to source voltage in MOSFET
P_c	-Conduction loss
P_{BD}	-Body diode power loss
I_{SD}	-Body diode current
t_D	-Body diode on time
T_{Fall}	-Fall time
T_{rise}	-Rise time
f_{SW}	-Switching frequency
Q_{oss}	-Output charge of MOSFET
Q_{rr}	-Reverse recovery charge
P_{MOSFET}	-Total loss in MOSFET
$P_{Switching}$	-Switching loss in MOSFET
$P_{conduction}$	-Conduction loss
L_r	-Resonant Inductor
C_r	-Resonant Capacitor
L_b	-Auxiliary Inductor
C_{s1}	-Auxiliary Capacitor
L_0	-Filter Inductor
C_0	-Filter Capacitor
D_1, D_2, D_3	-Auxiliary circuit diodes
V_{in}	-Input Voltage
V_0	-Output Voltage
I_0	-Output Load current
R_0	-Output load resistance
V_g	-Gate pulse voltage
$V_{g(aux)}$	-Gate pulse voltage for auxiliary switch
I_{Lr}	-Current through resonant inductor

V_{Cs1}	-Voltage across the capacitor C_{s1}
V_{cr}	-Voltage across the resonant capacitor C_r
D_{min}	-Minimum duty cycle
I_{0max}	-Maximum current of inductor L
Δp	-Energy stored in each cycle in the resonant capacitor C_r
L_b	-Auxiliary circuit buffer inductor
C_b	-Auxiliary circuit buffer capacitor
D_1, D_2	-Schottky diodes in the auxiliary circuit
D_{s1}, D_{s2}	-Body diodes of the MOSFET switches S_1, S_2.
t_{01}, t_{12}, etc	-Time interval between modes
$I_{0(avg)}$	-Average output current
τ	-Time period of one switching cycle
I_{Lrmax}	-Maximum inductor current
V_{Crmax}	-Maximum voltage across capacitor C_r
ω	-Resonant frequency
Z	-Characteristic Impedance
t_1, t_2, etc.	-Instants of Time in different modes
L_1, L_2, L_3	-Filter Inductors
$i_{resonant}$	-Resonant current
S_1, S_2, S_3 etc.,	-MOSFET switches
C_{s1}, C_{s3}, C_{s5}	-Auxiliary circuit capacitors
R	-Body diode resistance

Abbreviations

SMPS	-Switch mode power supplies
BJT	-Bipolar junction transistor
IGBT	-Insulated -gate bipolar transistor
MOSFET	-Metal-Oxide-Semiconductor Field-Effect-Transistor
PWM	- Pulse Width Modulation
AMD	- Advanced Micro Devices
VR	- Voltage Regulator
VRM	- Voltage Regulator Module
POL	- Point of load
DC-DC	- Direct Current – Direct Current
RR	- Reverse recovery
SR	- Synchronous Rectifier
ZVT	- Zero Voltage Transition
ZCT	- Zero Current Transition
ZCZV	-Zero current Zero voltage
ZVS	- Zero Voltage Switching
ZCS	- Zero Current Switching
EMI	- Electromagnetic Interference
MRC	-Multi-resonant converter
QRC	- Quasi Resonant Converter
QSC	- Quasi-Square-wave Converters
DSP	- Digital Signal Processors
PSIM	- Power Simulation
SBC	- Synchronous Buck Converter
PCB	- Printed Circuit Board

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Chapter 1

INTRODUCTION

CHAPTER 1: INTRODUCTION

1.1 Introduction

Switched mode power supplies (SMPS) have become standard candidate in most of the power processing applications. The design demand is forever moving towards higher power densities. The designer has to find the right tradeoff among efficiency, size, weight, thermal design, EMI issues and cost. Higher power density requires higher switching frequency. Higher switching frequency leads to high switching loss and associated problems. The concept of soft switching addresses these issues. The analysis and design methodologies of hard switched converters matured in 1970's and 1980's [1]. Good analytical circuit models have come into use out of these efforts [2] - [5]. In contrast to hard switching converters, the soft switching converters offer several advantages. Several families of soft switching converters emerged in the past few decades [6] - [44]. Analysis and modelling methods have been proposed in relation with these topologies [45] - [48]. Different degrees of efficiency improvement and increase in switching frequency have been obtained. As a result, there has been a constant increase in the power density of SMPS in the past few decades.

Resonant switching techniques reduce the switching losses to practically zero; the switching frequency then may be increased to hundreds of kHz to achieve higher power densities. Such converters in general are classified as `Soft switching converters' [6]. In these converters, the switching transitions occur with zero loss. Exploitation of resonant transitions in power conversion is not new. Resonant circuits were used to provide forced commutation in the thyristor era. The use of such techniques diminished with the introduction of fully controlled switches such as BJTs, MOSFETS and IGBTs. With the demand for higher power density and lower switching loss, there is a renewed interest in the resonant switching techniques. The switching techniques in the resonant converter employ zero voltage switching and/or zero current switching. Soft switching is also referred to as Zero current switching (ZCS) or Zero voltage switching (ZVS) in the literature [6]. In zero current switching, the device turns-on with zero current and turns-off after the current drops to zero. In zero voltage switching, the switch turns-off at zero voltage and turns-on after the device voltage drops to zero.

The concept of resonant switch was first proposed in [12]. The basic resonant switches are `Zero current switch' and `Zero voltage switch', shown in fig. 1.1. The `Resonant switch converters' are obtained by replacing the controllable switches in PWM converters with the ‘Resonant Switch'. The resonant switch is the combination of a switch and reactance’s. The switch has a series inductance to achieve ZCS or a shunt capacitance to achieve ZVS. The

family of DC-DC converters with resonant switches are known as `Quasi-resonant converters' (QRC's) [12] - [14].

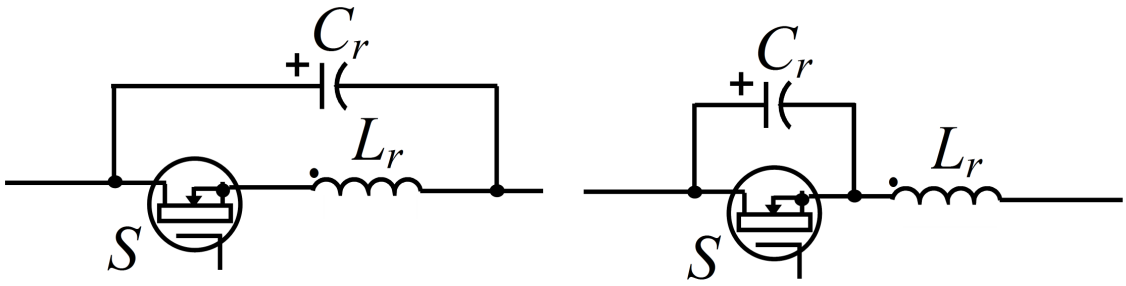


Fig. 1.1: Basic resonant switches (a) Zero current resonant switch (b) Zero voltage resonant switch

Resonant switch converters, employing fig. 1.1 (a) are ZCS QRC's - The current in the switch starts from zero at turn-on. The turn-off of the device is when the current through the device has come down to zero. The devices are designed for high peak current. Conduction loss is high and practically independent of the load current. The loss due to the discharge of the parasitic junction capacitance of the device during turn-on is significant at switching frequencies above 1MHz. Hence, at higher switching frequencies, resonant switch converters employing fig. 1.1 (a) is preferred to ZCS QRC's. Resonant switch converters, employing fig. 1.1 (b) are ZVS QRC's - The turn-on of the device is while the body diode is conducting. During turn-off, the shunt capacitor constraints the device voltage to increase slowly. The active switch in ZVS QRC's is subjected to relatively low current stress. However, the active switch suffers from excessive voltage stress. Quasi-resonant converters are available in a wide variety of topologies [15].

New families of converters called multi-resonant converters (MRC's) were reported in [16]-[17]. The ZVS multi-resonant converter technique uses all parasitics of the power stage. All devices operate with ZVS. This substantially reduces the switching losses. Both active and passive switches suffer from voltage and current stress, higher than in PWM counterparts. This leads to a substantial increase in the conduction loss. A new family of converters called `Quasi-Square-wave Converters' (QSC) were reported in [18]. QSC's had reduced voltage stresses and operated with improved efficiency. However, the switches suffered from higher current stress, twice that in the PWM counterpart. In resonant load and resonant switch converters, switching losses are reduced at the cost of conduction losses of the main switch. The output voltage is controlled by varying the switching frequency. When the switching frequency varies, the EMI filters become heavier; this puts additional size penalty on the converter.

In the above converters, the resonant elements handle many times the load current and the circuit voltage. This may be overcome if the resonant elements are not in the direct path of the power flow. Later developments in ZVS/ZCS converters adopted a different strategy- the

resonant elements were away from the main path of the power flow. The resonant elements shaped the switch voltage/current only during the switch transitions. When the switching transitions are over, the circuit reverts back to the PWM mode. The converter achieves soft switching while preserving the characteristics of the PWM converter. In recent years, various soft transition techniques have been proposed to reduce the switching losses. The converters employing soft transition techniques (Zero voltage transition (ZVT) or Zero current transition (ZCT)) are called `Soft transition converters [19]. These converters achieve soft switching (ZVS or ZCS) through an active auxiliary circuit. This auxiliary circuit becomes active only during the switching transitions. The ZVT technique forces the switch voltage to zero, before the switch is driven on. The ZCT forces the current through the switch to zero, before the switch is driven off.

The main power is not processed in the auxiliary circuit. A good soft transition scheme will have the following features:

- Lower switching losses
- Reduction of switch Current/Voltage
- Soft recovery for the freewheeling diode

These features contribute to higher power density and improvement in the efficiency.

A number of soft transition converters employing ZVT/ZCT have been reported [20] - [34]. All these converters employ an auxiliary network to obtain soft switching for the main switch. These converters achieve ZVS for both the active and the passive switches. The VA ratings of the main switch are same as that of the source voltage and load current. In these converters, the main switch transitions are lossless; auxiliary switch turn-off transition is lossy.

The demands for processing power have been observed in the companies such as Intel and AMD repeatedly self–obsolete themselves with powerful and faster processor chips. These advancements have been made by the increase in the transistor density, which can be fabricated in a particular area of silicon. The processor current requirement increases exponentially over a few decades and in future it may exceed 100A in the different processor applications. The Moore's law which state, "transistor density doubles every twelve months" is successful in the prediction of evolution of microprocessors. Currently, there are millions of transistors and by 2018 there will be billions of transistors on a particular chip. A converter that supplies 120A/0.8V is in need by the year 2018 [185-186].

The power management techniques are introduced in a microprocessor, for modules of transistors in the recent years. The decline of microprocessor supply voltage is one of the solutions. Many company's microprocessors including Intel uses a non-standard power

supply of less than 5V and these voltages is continuously getting decreased. Furthermore, the transistors number increases in the microprocessor that leads to increase in the microprocessor current demand. The low voltage, high current and tight voltage regulation inflict challenges for power supply design of microprocessors. Fig. 1.2 shows the voltage and current variation as per the current demands of the Intel's processors.

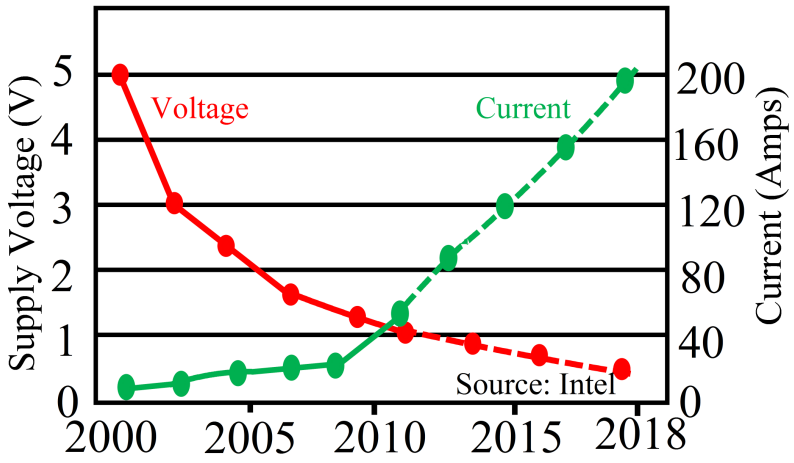


Fig. 1.2: Intel's road map for the processors required current and voltage

1.2 Losses in converters

In general losses are bound to be present in the elements of the converter. The loss of each element depends on its operational characteristics. The loss distribution varies widely, but the switching elements play a significant role. The other component losses also cannot be neglected. MOSFET's are well- known switching elements which are the cause for switching and conduction loss. The power loss of the MOSFET is categorized as conduction and switching losses. The calculations applied are approximate, as the losses are neglected during the operation. Conduction loss is the product of current square times the resistance in the switch during conduction, whereas the switching loss is considered to be the overlap of the current and voltage of the switching element. Switching loss is obtained as the product of half the drain voltage and the inductor current during the switching transition time (fall and rise times) [81-83]. Output capacitance C_{oss}, body diode conduction loss is also other elements which cause the losses in the converter. Output capacitance C_{oss} loss is calculated as the product of half the C_{oss} times the square of the input voltage and multiplied by the switching frequency [84-88]. Calculation of output capacitor C_{oss} loss has been introduced on the basis of a basic energy concept in [87-89]. The output capacitor C_{oss} is located in between the drain-source and drain- gate, its value is obtained from the datasheet of the MOSFET. Calculation of each element loss is required in order to minimize the respective losses to enhance the overall efficiency. The usage of synchronous rectifier results in the reduction of

the conduction loss, but develops supplemental switching losses. This effect is reduced by the addition of the resonant tank in the converter.

The two basic terms, overlap VI loss and C_{oss} loss have a relation between C_{oss} and switching loss obtained as a ratio that can't be segregated. Switching loss is the combination of total switching and C_{oss} losses i.e., $0.5I_L.V_D.(T_{fall} + T_{rise})$ [45]. C_{oss} loss has an indirect effect as it affects the rise and fall time period, which inturn affects the switching loss.

The power loss of the MOSFET is given by:

$$P_{MOSFET} = P_{Switching} + P_{Conduction}$$

Conduction losses are calculated as

$$P_{Conduction} = I_{rms}^2 . R_{dsON}$$

Where I_{rms} is the current through the MOSFET,

R_{dsON} is ON state resistance,

A specific dead time is allowed between two synchronous MOSFET's to avoid current shoot through. This results in the current commutation from MOSFET channel to its body diode, where a negative voltage drop develops between drain-source channels. This time is considered as body diode ON time t_D. The calculation of body diode loss is obtained by the parameters as follows; the forward voltage drop of body diode V_D, source to drain body diode current I_{sD}, the body diode ON time t_D and the switching frequency f_{sw}.

$$P_{BD} = V_D I_{sD} t_D f_{sw}$$

The switching loss at the instant of OFF time is calculated by the output charge Q_{oss} and the reverse recovery charge Q_{rr} that build the losses during the transition of turning OFF the synchronous rectifier MOSFET. It is given by

$$P_s = V_T \left(\frac{1}{2} Q_{oss} + Q_{rr} \right) f_{sw}$$

V_T is the instantaneous voltage of MOSFET.

Therefore, the losses of the synchronous rectifier are expressed as:

$$P_{SR} = P_C + P_s + P_{BD}$$

Application of soft switching enhances the overall efficiency by the reduction of inevitable losses as shown in fig. 1.3. Many converter topologies are proposed for enhancing the efficiency [91-95].

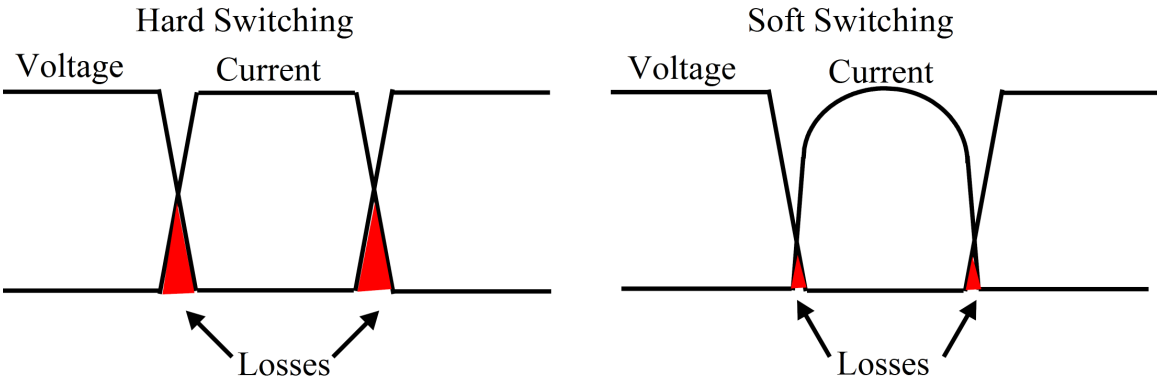


Fig. 1.3: Switching losses in the conventional and resonant converter

1.3 Contrast between different resonant converters

Table1.1 Comparison between the soft switching techniques

Switching technique	Advantage	Drawback	Operating condition
Quasi resonant	decrease the switching stress	Current is discontinuous	Works with variable frequency
Resonant	Operates at zero voltage and zero current to minimize the losses	High voltage and current peaks with greater complexity	Applicable for converters operating under 100 kHz frequency.
Zero voltage Transition (ZVT)	Operates at high frequency and minimizes the parasitic effects	Losses occur due to $C\,dv/dt$ across the gate are not minimized	During the transition times it works as a resonant converter and rest it operates as a conventional PWM converter.
Zero Current Transition (ZCT)	Minimizes the turn-OFF loss	Losses in the junction capacitance	Operates at the instant of switch, turn-OFF time.
Zero voltage Transition (ZVT) - Zero Current Transition (ZVT)	Eliminates both turn-ON and turn-OFF losses		Operates on both the instances of turn-ON and turn-OFF; acts as a traditional PWM converter for the remaining period.

Research is still in demand to introduce novel topologies, in the recent years the converters embedded with quasi-resonant, resonant and ZVT-ZCT technique is in use [96].

Each soft switching technique has its own significance as per the application. In a resonant converter, a regular PWM converter is added by a resonant element switch network. The converter which emerges has both the properties of the resonant switch network and PWM converter.

1.4 Motivation

The huge demand of power converters for portable electronic circuitry under various power ratings constitutes solid tests for power supply designers. Increased current demand, low operating voltages and the state of the microprocessor based or microcontroller based systems develops new opportunities for power distribution and management. High power density, high efficiency and proper voltage regulation are the issues which become critical if conventional converters are used for low operating voltage. Due to advances in power electronics converter design and control methods, the electrical energy conversion from one form to another with enhancing efficiency and low cost is being made possible. But a tradeoff is considered for some issues such as size, cost, weight and power density, etc., in modern day power electronic circuitry. The advantages in cost, size and performance endorses the power electronic applications broadly in many fields like industrial, residential, aerospace and military in the recent years. According to Moore's law, the number of transistors on an IC has doubled every year. To attain high power density with a large rate of increase in the number of transistors appeals rise in the switching frequency that induces the switching losses.

The increase in the acclaim of low power portable equipment asserts for efficient and high power density converter. The power density of a converter is enhanced by reducing the losses of size of components. The switching frequency is a prime factor for the reduction of the size of the components. The switching frequency is a prime factor for the reduction of the size of the components to a certain extend. Quasi-resonant, resonant, ZVT-PWM, ZCT-PWM, ZVT-ZCT-PWM converter topologies have been proposed in the recent years, in order to reduce the losses. The resonant converter experiences the high current peaks and high voltage across the switching devices. ZVT-ZCT PWM converters are in huge demand since they provide lower voltage and current stresses. This inturn affects the ratings of the device to be higher than the conventional converters. The enhanced efficiency can be accomplished by using the proper topology that alleviates the conduction and switching loss. The modern power electronic converter topologies insist on high efficiency, low cost power supply, high power density for portable applications motivate to design and develop ZVT-ZCT PWM

synchronous buck converters with the addition of active and passive auxiliary circuits at different operating conditions. ZVT-ZCT PWM synchronous buck converters attains high efficiency by the reduction of losses. They also attain low cost and low power rating elements in the converter by reducing voltage and current stresses.

Programmable devices such as microprocessors and DSP's are extensively used in many commercial and industrial applications. In order to meet the demands of these programmable devices, there should be declined in the operating voltage without changing the power consumption, while sustaining the higher operating switching frequency. These demands can be achieved by the use of multiphase synchronous buck converter. Increase in the number of components and switches results in the lower efficiency. Reduction of losses in the multiphase buck converter to accomplish the demand of high efficiency is now a challenging task. These demands motivate to employ the soft switching techniques into the synchronous buck converter to attain high power density with an enhanced efficiency.

1.5 Objectives

From the above discussions the thesis objectives are as follows:

- To employ the soft switching techniques in the synchronous buck converter topology using an active auxiliary circuit. The proposed topology should enhance the efficiency for high power density applications. The main aim is to reduce the voltage and current stresses using the auxiliary circuit.
- To implement the soft switching into the synchronous buck converter embedding the passive snubber circuit. A passive auxiliary circuit in the synchronous buck converter should fulfill the demands of high efficiency, high power density maintaining high operating switching frequency. It will also accomplish the objective of reducing high voltage and current stresses.
- To design and develop multiphase synchronous buck converter for modern generation microprocessor power supply unit for point of load (POL) applications at low operating output voltage and high load current by reducing switching losses, voltage and current stresses.

1.6 Organisation of the thesis

Chapter I presents the background of the work. The significance of loss analysis to measure the degree of performance of a topology is discussed. Comparisons between different soft switching techniques are included. Finally, factors for motivation and objectives have been discussed.

Chapter II includes the design and implementation of ZVT-ZCT soft switching technique in the synchronous buck converter to accomplish high efficiency for higher power density applications. An active auxiliary circuit is incorporated in the conventional PWM synchronous buck converter which makes the main switch to operate with ZVS at turn-ON and ZCS at turn OFF. The principle of operation and steady state analysis of the proposed converter has been discussed. The simulation and experimental results that validate the performance of the proposed converter have been presented. To mitigate the disadvantages of active auxiliary circuit such as surplus switching loss and its complex circuitry the active auxiliary circuit is substituted with a simple passive auxiliary circuit.

In **chapter III**, a passive auxiliary circuit introduced into the conventional synchronous buck converter is discussed. The detailed steady state analysis and operating principle are presented. The design details of the auxiliary circuit components are included and a prototype has been built in the laboratory. The performance of the proposed converter is verified by the simulation and experimental results.

Chapter IV introduces the implementation of the soft switching technique into the multiphase synchronous buck converter incorporated with an auxiliary circuit for reduction of switching losses. The steady state analysis of the proposed converter has been explained comprehensively. The design and fabrication of the proposed converter have been executed in the simulation and experimental results.

Chapter V deals with summary and future work of the buck converters.

Chapter 2

PERFORMANCE ENHANCEMENT OF SYNCHRONOUS BUCK CONVERTER WITH INTEGRATION OF ACTIVE AUXILIARY CIRCUIT

CHAPTER 2: PERFORMANCE ENHANCEMENT OF SYNCHRONOUS BUCK CONVERTER WITH INTEGRATION OF ACTIVE AUXILIARY CIRCUIT

2.1 Introduction

In the recent times, the Zero Voltage Transition-Zero Current Transition (ZVT-ZCT) technique applied to the synchronous buck converter emanates as a prior converter that maintains voltage and current stresses within tolerable limits. These modules are found immensely in the high- power applications. In addition to that, the solar and spacecraft applications demanding efficient DC-DC modules for improving the storage capacity which is to be used in intermittent times.

The Zero Voltage Transition (ZVT) – Zero Current Transition (ZCT) technique applied to synchronous buck converter (SBC) reduces the conduction and switching losses which inturn enhances the efficiency. The voltage and current mode soft switching method that has drawn attention in the recent times is Zero Voltage Transition (ZVT) – Zero Current Transition (ZCT) [67, 100-108]. The demand boosts as its operation is close to the PWM converters and in addition to that, provides low conduction and switching losses. The auxiliary circuit of the Zero Voltage Transition (ZVT) – Zero Current Transition (ZCT) converters is activated just before the main switch is made active and culminates after it is accomplished. The ratings of auxiliary circuit components are lower than those in main power circuit as the auxiliary circuit is activated for a small fraction of the switching cycle; this makes a provision for the converter's to shrink its size and cost.

The converters proposed in [102, 105, 109-110]; suffer from hard switching turn OFF that leads to increase in switching losses. The auxiliary switch is turned-off while it is conducting that causes switching losses and electromagnetic inference (EMI) to appear that offsets the advantage of using the auxiliary circuit. The converters proposed in [108-111, 105] have very high current stresses on the main switch. The main converter switch operates with a higher peak current stress and with the more circulating current which results in the need for a higher current rated switch that increases conduction losses. Reduction of switching losses for low power circuits such as synchronous buck is not presented in the [112-127].

Switching losses are reduced by inculcating soft switching function into the standard PWM-converters utilizing the Zero Voltage Transition (ZVT) – Zero Current Transition (ZCT) technique. The auxiliary circuit proposed transfers energy from input voltage source to

output, suitable for high power applications. It also shares the output current stress between the main switch and auxiliary switch. There is no additional voltage and current stress on the main switch and the semiconductor devices used are soft switched.

The various other proposed ZVT-ZCT PWM converters have one of the following flaws:

1. During current conduction through the auxiliary switch, it is turned OFF. This leads to switching losses and EMI to occur that cancel out the advantages using the auxiliary switch. The converters proposed in [102, 110, 187, 188] experience hard-switching turn OFF.
2. The auxiliary circuit affects the main switch of the converter to operate at high peak current stress and more circulating current. This causes to use higher current rating switching device for the main switch that also increases the conduction losses. The converters that are proposed in [25, 32, 44, 49, 98, and 105] suffer with high current stress on the main switch.
3. The components used for auxiliary circuit in the proposed converters [102, 26, 29, 32] contain high voltage and current stresses. The converters proposed in [108, 111] have low current stress on the main switch, but the circuit is complex.

This chapter is organised as follows: section 2.2 describes about the proposed topology. Section 2.3 explains the principle of operation and its operating modes. Section 2.4 provides the design procedure of magnetic elements used. Section 2.5 includes the simulation and experimental results that exposes the features of the proposed converter. In section 2.6, efficiency curve is shown that explains the operation of the converter over wide range of load, also the efficiency curve is compared with conventional and contemporary topologies. Section 2.7 summarises the important features.

2.2 Topology description

The circuit scheme of the proposed ZVT-ZCT synchronous buck converter with active auxiliary circuit is shown in Fig. 1. The converter comprises of main switch S_1, synchronous switch S_2, filter capacitor C_o, and filter inductor L_o. The proposed auxiliary circuit includes an auxiliary switch S_3, auxiliary inductors L_b and L_r, diodes D_1, D_2, D_3 and a capacitor C_r.

To simplify the analysis the following conditions are assumed in a switching cycle.

1. The auxiliary capacitor is charged to $2V_{in}$ and the synchronous switch is conducting before mode 1.
2. Inductor current I_{L0} is constant and equal to I_o
3. L_b is much larger than L_r.

4. All circuit elements are ideal.

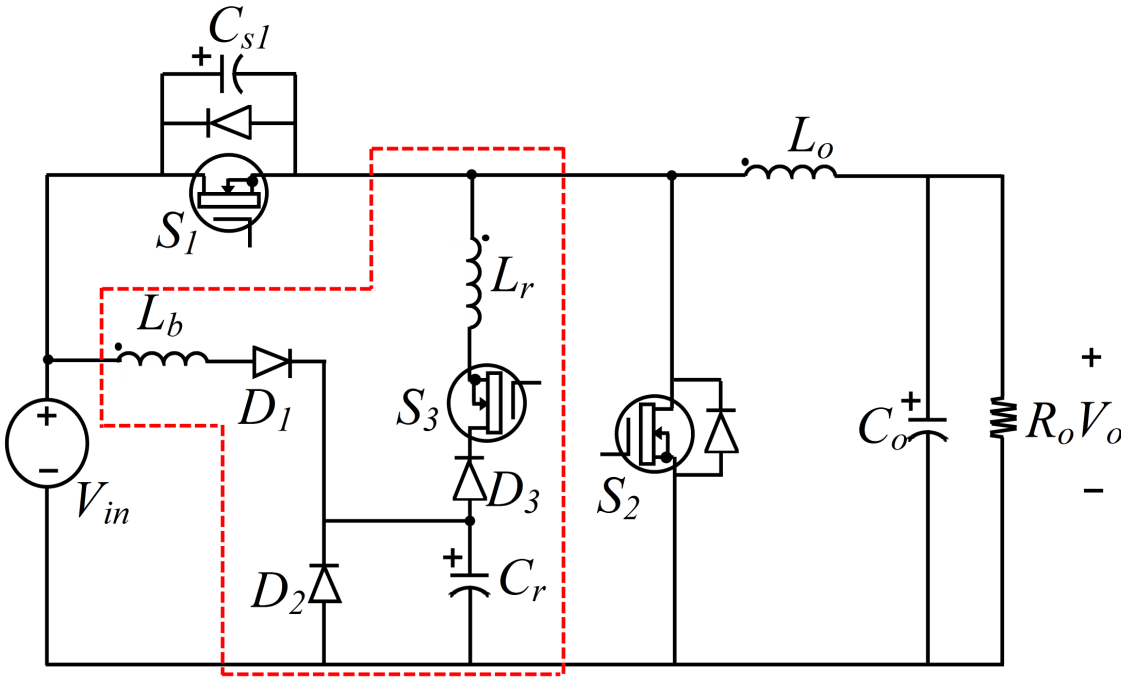


Fig. 2.1: Proposed ZVT-ZCT PWM Synchronous buck converter with active auxiliary circuit

2.3 Operational modes

In this section, the operating modes of the proposed converter are comprised of 14 states, considering the different current paths of the elements and switch voltages. The waveforms are presented in fig. 2.2, and the operating mode analysis is explained by the current paths shown in fig. 2.3.

Mode 1 (t_0 — t_1): In mode 1 auxiliary switch is turned ON, that causes resonance between the auxiliary capacitor C_r and the auxiliary inductor L_r. The current of L_r increases during the resonant period. When L_r current becomes equal to the output current, the synchronous switch body diode turns OFF under ZCZV condition. Snubber capacitor voltage is constant that is charged to V_{in}, which causes ZV condition. The L_r current and C_r voltage expressions for this mode are:

$$I_{Lr} = \frac{2V_{in}}{z_1} sin(\omega_1(t - t_0)) \tag{2.1}$$

$$V_{Cr} = 2V_{in} cos\left(\omega_1 (t - t_0)\right) \tag{2.2}$$

Where

$$\omega_1 = \frac{1}{\sqrt{L_r C_r}} \tag{2.3}$$

$$Z_1 = \sqrt{\frac{L_r}{C_r}} \tag{2.4}$$

This mode ends when L_r is equal to the output current. The duration of this mode and capacitor voltage C_r are given by

$$t_1 - t_0 = \frac{sin^{-1}\left(I_o Z_1 \big/ 2V_{in}\right)}{\omega_1} = \Delta t_1 \tag{2.5}$$

$$V_{Cr} = 2V_{in}\, cos(\omega_1 \Delta t_1) \tag{2.6}$$

Mode 2 (t_1 — t_2): In this mode, resonance occurs between L_r, C_r and C_{s1}. The snubber capacitor discharges during the resonance. In this mode, some part of the energy is transferred to the output. At the end of the mode voltage across Cr becomes equal to zero.

$$I_{L_r} = \left(I_0 - \frac{I_0}{I_{L_0} C_{s1} \omega_2^2}\right) cos\left(\omega_2 (t - t_1)\right) + \frac{V_{Cr}}{L_r \omega_2} sin\left(\omega_2 (t - t_1)\right) + \frac{I_0}{I_{L_0} C_{s1} \omega_2^2} \tag{2.7}$$

$$V_{C_{S1}} = V_{in} - \frac{1}{C_{s1}} \int_{t_1}^{t_2} (I_{Lr} - I_0) dt \tag{2.8}$$

$$V_{Cr} = V_{Cr} - \frac{1}{C_{s1}} \int_{t_1}^{t_2} (I_{Lr}) dt \tag{2.9}$$

$$\omega_2 = \frac{1}{\sqrt{\frac{L_r C_{s1} C_r}{C_r + C_{s1}}}} \tag{2.10}$$

Calculation the time interval of this mode is complex from (7) and (8). In order to simplify the analysis, the auxiliary capacitor C_r and snubber capacitor C_{s1} are assumed to be equal. Therefore

$$C_r = C_{s1} = C \tag{2.11}$$

$$\omega = \frac{1}{\sqrt{L_r C_r}} = \omega_1 = \frac{\omega_2}{\sqrt{2}} \tag{2.12}$$

$$Z = \sqrt{\frac{L_r}{C}} = Z_1 \tag{2.13}$$

$$L_r C \omega_2^2 = 2 \tag{2.14}$$

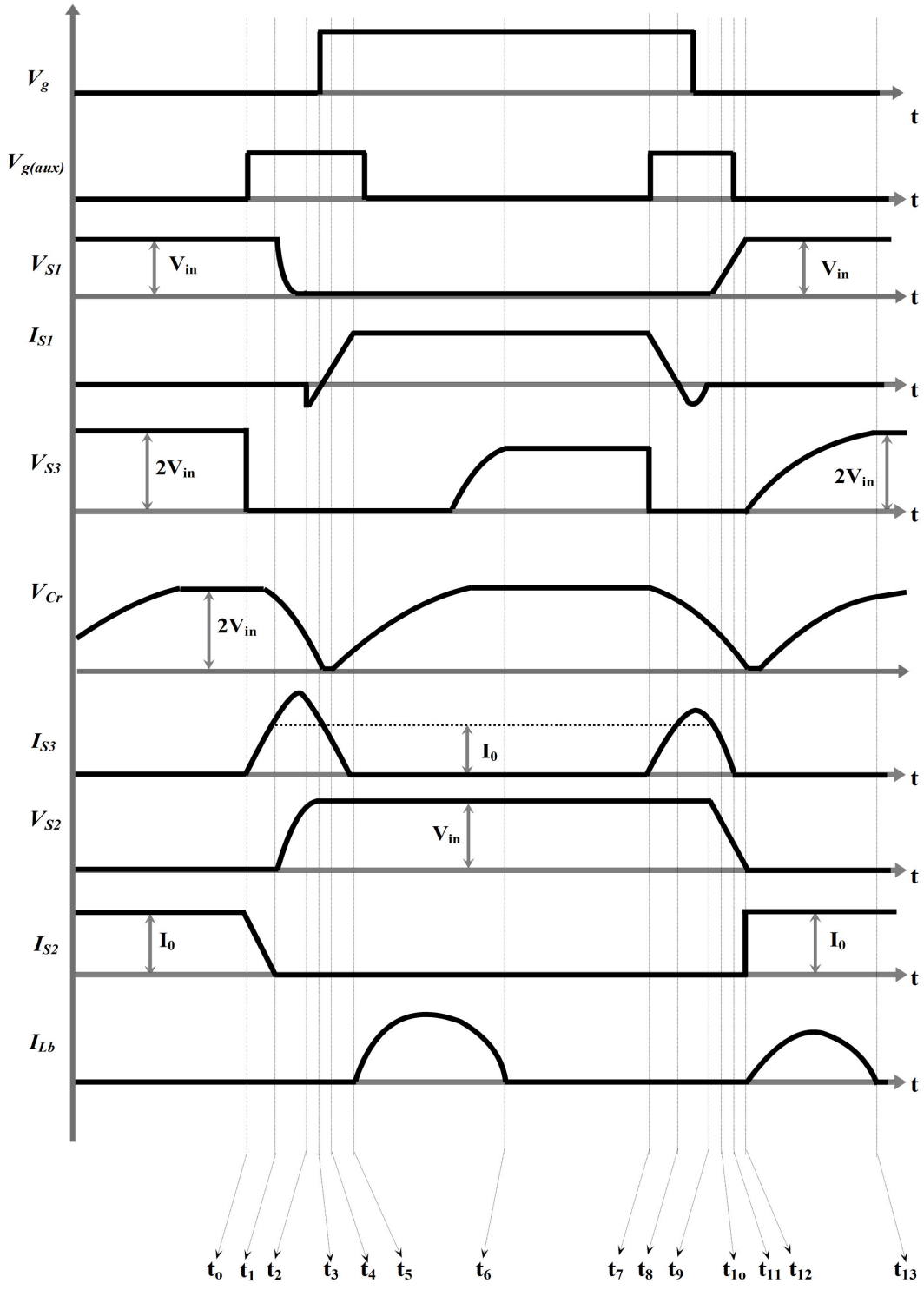


Fig. 2.2: Essential theoretical waveforms of proposed converter

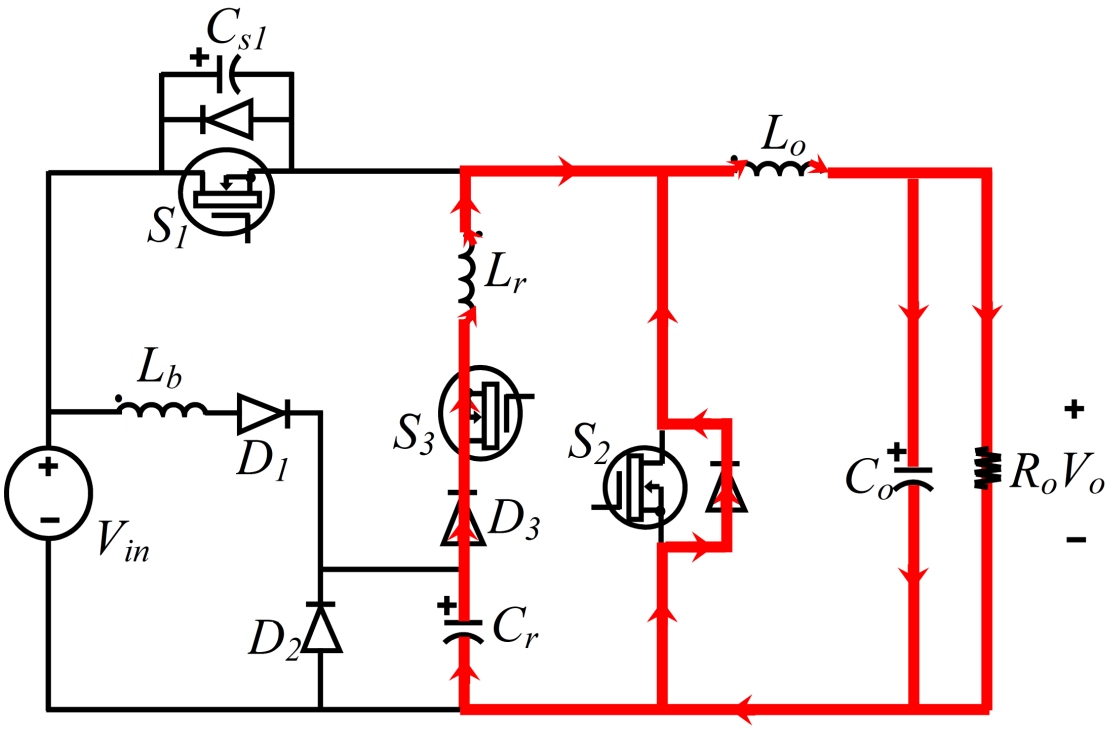


Fig. 2.3 (a): Modes of operation: Mode 1 (t_0 — t_1)

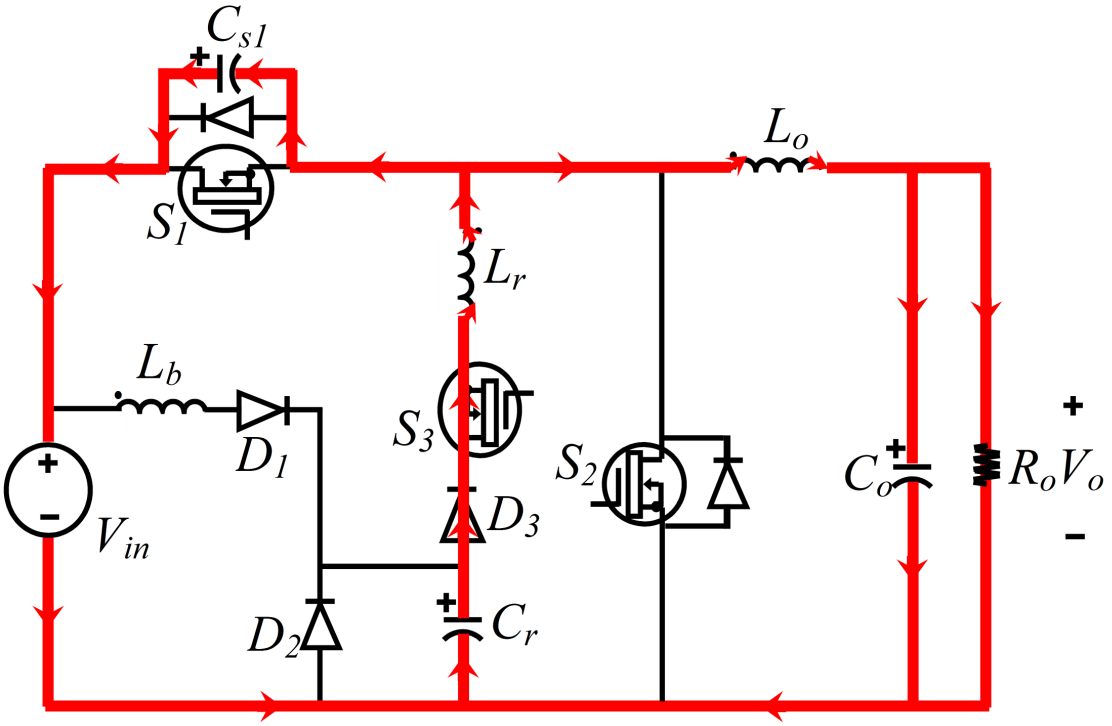


Fig. 2.3 (b): Modes of operation: Mode 2 (t_1 — t_2)

$$\frac{Z}{L_r \omega_2} = \frac{1}{\sqrt{2}} \tag{2.15}$$

$$\frac{I_0}{C\omega} = I_0 Z = \frac{V_{in}}{1.2} \tag{2.16}$$

The equations (6) and (7) are simplified as follows:

$$V_{Cr} = 1.82 V_{in} \tag{2.17}$$

$$I_{L_r} = \left(I_0 - \frac{I_0}{2} \right) cos\left(\omega_2 \left(t - t_1\right)\right) + \frac{1.82 * 1.2 Z_1 I_0}{L_r w_2} sin\left(\omega_2 \left(t - t_1\right)\right) + \frac{I_0}{2} \tag{2.18}$$

$$= \left[\frac{1}{2} cos\left(\omega_2 \left(t - t_1\right)\right) + \frac{1.82 * 1.2}{\sqrt{2}} sin\left(\omega_2 \left(t - t_1\right)\right) + \frac{1}{2} \right] \left(I_0\right)$$

The duration of this interval is obtained as $0.55\pi/\omega_2$ and also from (8) and (18), the inductor current L_r and the snubber capacitor C_r voltage $1.96I_o$ and $0.18V_{in}$ respectively. Another resonance between L_b and C_r occurs when the voltage of capacitor C_r falls below V_{in}. L_b is assumed to be larger than L_r, L_b and C_r are under resonance which is very slow and hence its effect can be negligible until the sixth mode.

Mode 3 (t_2 — t_3): In this mode, D_1 gets forward bias and the resonance between C_r and L_r will continue. This mode ends when C_r is discharged and due to this the main switch body diode conducts. The inductor L_r current and capacitor C_r voltage is given by:

$$I_{L_r} = \left(1.96 - 1\right) cos\left(\omega_2 \left(t - t_2\right)\right) + (0.18 - 1)\, sin\left(\omega_2 \left(t - t_2\right) + 1\right).I_0 \tag{2.19}$$

$$V_{Cs1} = 0.18 V_{in} - \frac{1}{C_{s1}} \int_{t2}^{t3} (\, I_{Lr} - I_0 \,) dt \tag{2.20}$$

The resonant inductor L_r current at the end of this mode is $1.65I_0$ and duration of this mode is given by $0.99\pi/\omega$.

Mode 4 (t_3 — t_4): When the snubber capacitor is discharged, the body diode of the main switch starts conducting and L_r current decreases linearly. The main switch turns ON at the ZCZV condition before the inductor L_r current becomes lesser than the output current. The duration of the mode is given by:

$$t_4 - t_3 = \frac{0.65 L_r I_0}{V_{in}} = \Delta t_4 \tag{2.21}$$

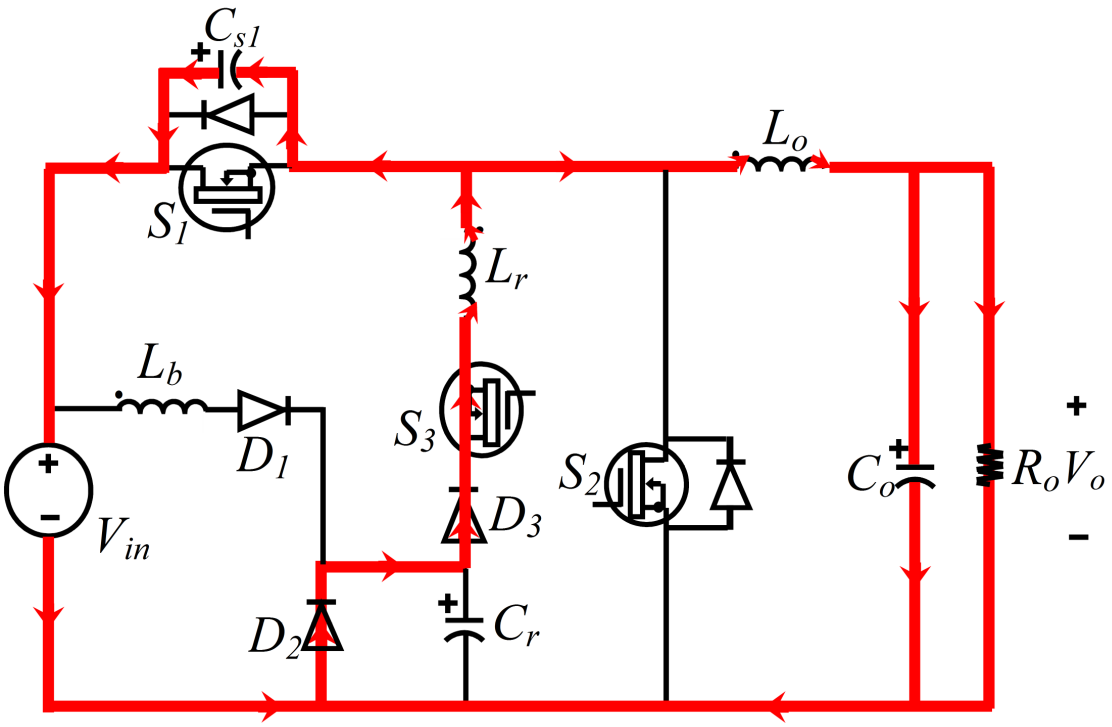
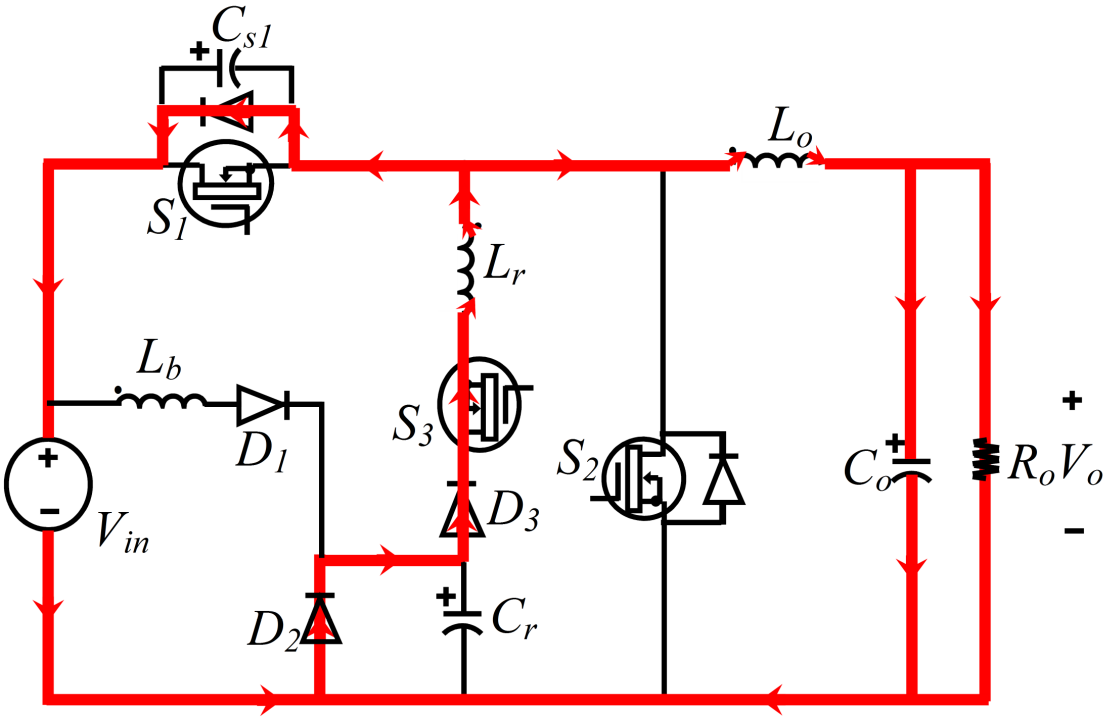


Fig. 2.3 (c): Modes of operation: Mode 3 (t_2 — t_3)



Mode 4 (t_3—t_4)

Fig. 2.3 (d): Modes of operation: Mode 4 (t_3 — t_4)

Mode 5 (t_4 — t_5): In this mode main switch is turned ON and the voltage across L_r is V_{in} and its current decreases linearly to zero. The main switch current increase linearly from

zero to output current I_0. At the end of this mode due to ZC condition the auxiliary switch is turned OFF as its current is reduces to zero. The duration of this mode is given by:

$$t_5 - t_4 = \frac{L_r I_0}{V_{in}} = \Delta t_5 \tag{2.22}$$

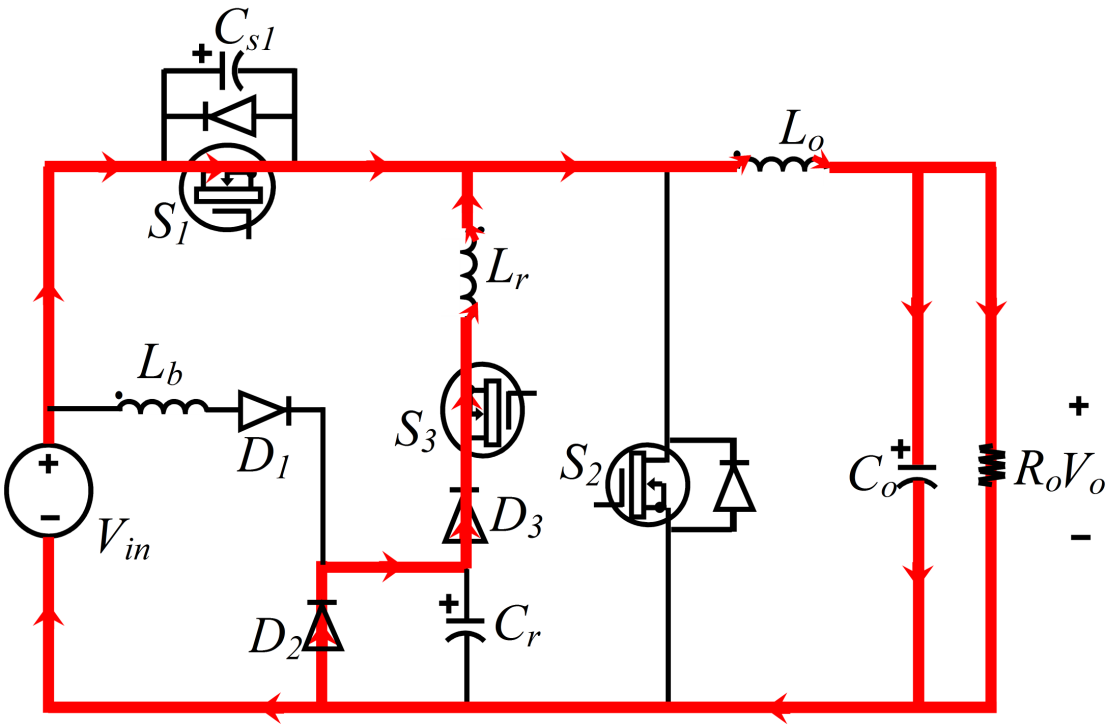


Fig. 2.3 (e): Modes of operation: Mode 5 (t_4 — t_5)

Mode 6 (t_5 — t_6): In this mode due to the slow resonance of the inductor L_b and capacitor C_r the auxiliary capacitor is charged to $2V_{in}$. The inductor current I_{Lb} and capacitor voltage V_{Cr} are given by:

$$I_{L_b} = \frac{V_{in}}{Z_3} sin\left(\omega_3 \left(t - t_4\right)\right) \tag{2.23}$$

$$V_{C_r} = V_{in}\left(1 - cos\left(\omega_3 \left(t - t_4\right)\right)\right) \tag{2.24}$$

Where,

$$\omega_3 = \frac{1}{\sqrt{L_b C_r}} \tag{2.25}$$

$$Z_3 = \sqrt{\frac{L_b}{C_r}} \tag{2.26}$$

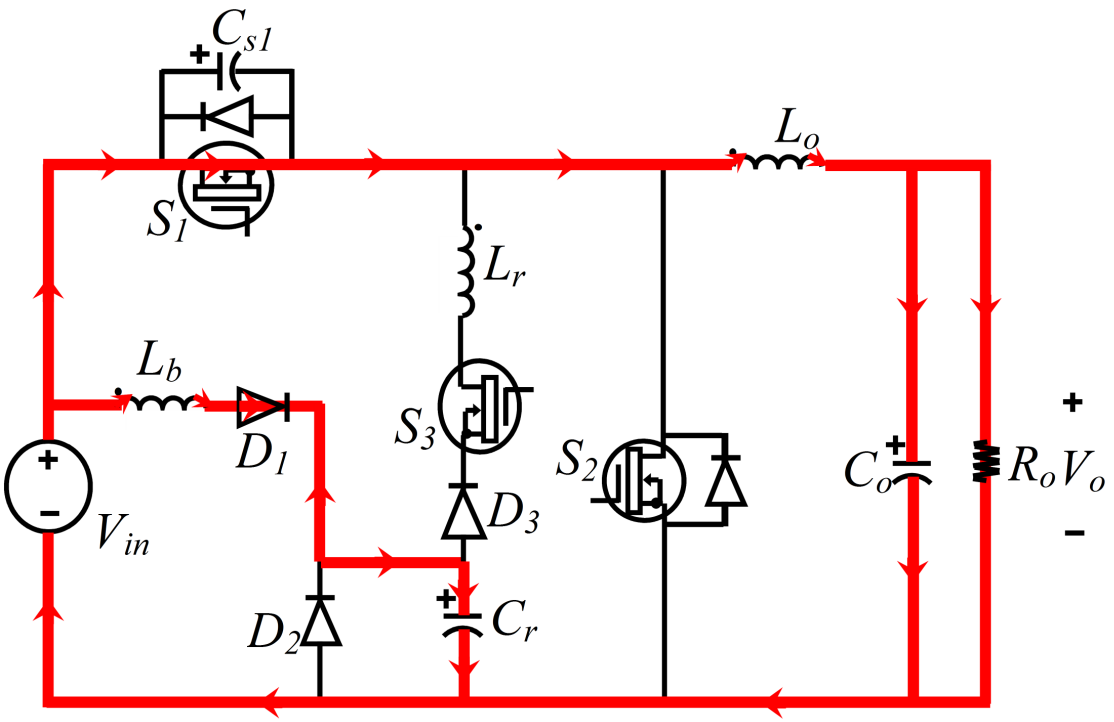


Fig. 2.3 (f): Modes of operation: Mode 6 (t_5 — t_6)

Now C_r is charged to $2V_{in}$ so that the duty cycle of the converter is reduced to:

$$\frac{D_{\min}}{f} = \pi\sqrt{L_b C_r} \tag{2.27}$$

Mode 7 (t_6 — t_7): In this mode the converter operates as a regular PWM synchronous buck converter as the resonance between L_b and C_r comes to an end.

Mode 8 (t_7 — t_8): In this mode the auxiliary switch is turned ON and the resonance occurs between L_r and C_r. As L_r is in series with the switch S_3 it is turned ON under ZC condition. The inductor current L_r increases and the main switch current decreases in this duration of resonance. The equations in this mode are:

$$I_s = I_0 - I_{L_r} = I_0 - \frac{V_{in}}{Z} sin\left(\omega\left(t - t_6\right)\right) \tag{2.28}$$

$$V_{C_r} = V_{in}\left(1 + cos\left(\omega\left(t - t_6\right)\right)\right) \tag{2.29}$$

It can be seen that from (2.28) the ZCZV condition for the main switch turn OFF is achieved if:

$$\frac{V_{in}}{Z} \geq I_0 \tag{2.30}$$

By taking into account the 20% over design

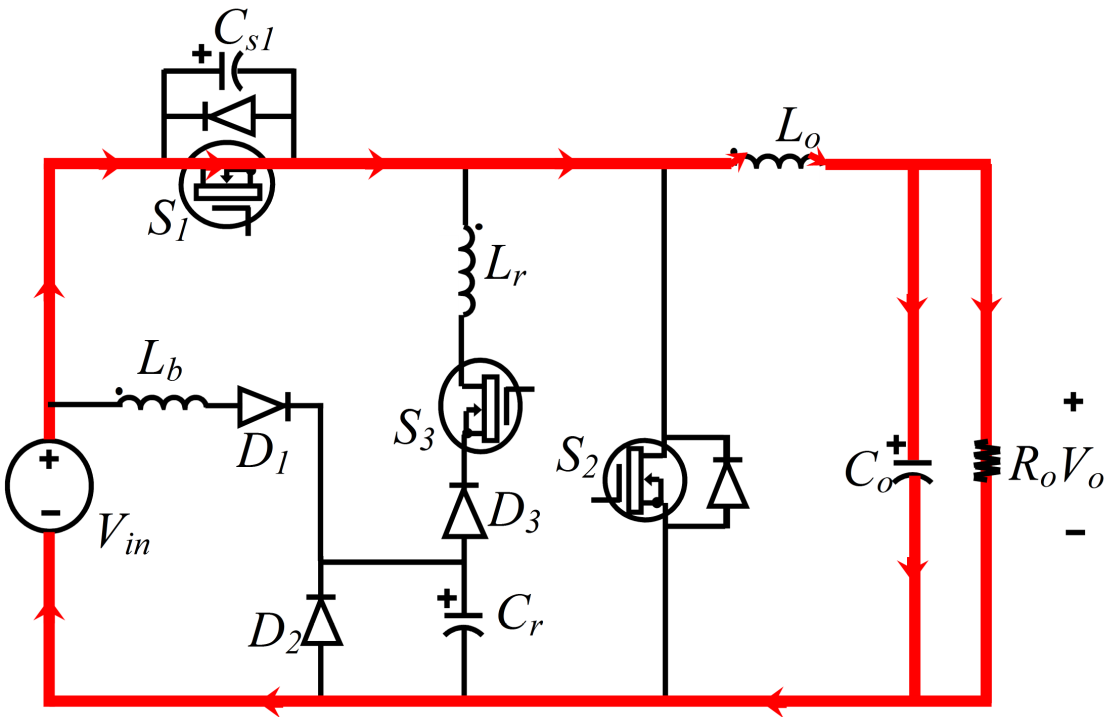


Fig. 2.3 (g): Modes of operation: Mode 7 (t_6 — t_7)

$$\frac{V_{in}}{Z} = 1.2 I_{0_{max}} \qquad (2.31)$$

Where I_{0max} is maximum current of the inductor L_0 at the switch turn OFF. The inductor current I_{L0} is assumed constant, so I_0 is substituted in place of I_{0max}.

At the end of this mode the inductor current L_r reaches I_0 and the duration of this mode is given by $0.31\pi/\omega$.

Mode 9 (t_8 — t_9): In this mode the main switch is turned OFF under ZCZV condition as the body diode of the main switch conducts. The inductor L_r current declines from its peak value to I_0. From (2.28), (2.29), and (2.31) the period of this mode is computed as $0.37\pi/\omega$ and voltage across capacitor C_r becomes equal to $0.45V_{in}$.

Mode 10 (t_9 — t_{10}): In this mode, the resonance occurs between C_r, L_r and C_{s1}. The equations of this mode are given by;

$$I_{Lr} = \left(I_0 - \frac{I_0}{I_{Lr} C_{s1} \omega_2^2} \right) cos\left(\omega_2 (t - t_9)\right) + \frac{(1-0.45) V_{in}}{L_r \omega_2} sin\left(\omega_2 (t - t_9)\right) + \frac{I_0}{L_r C_{s1} \omega_2^2} \qquad (2.32)$$

$$V_{Cr} = 0.45 V_{in} - \frac{1}{C_r} \int_{t_9}^{t_{10}} (I_{Lr})\, dt \qquad (2.33)$$

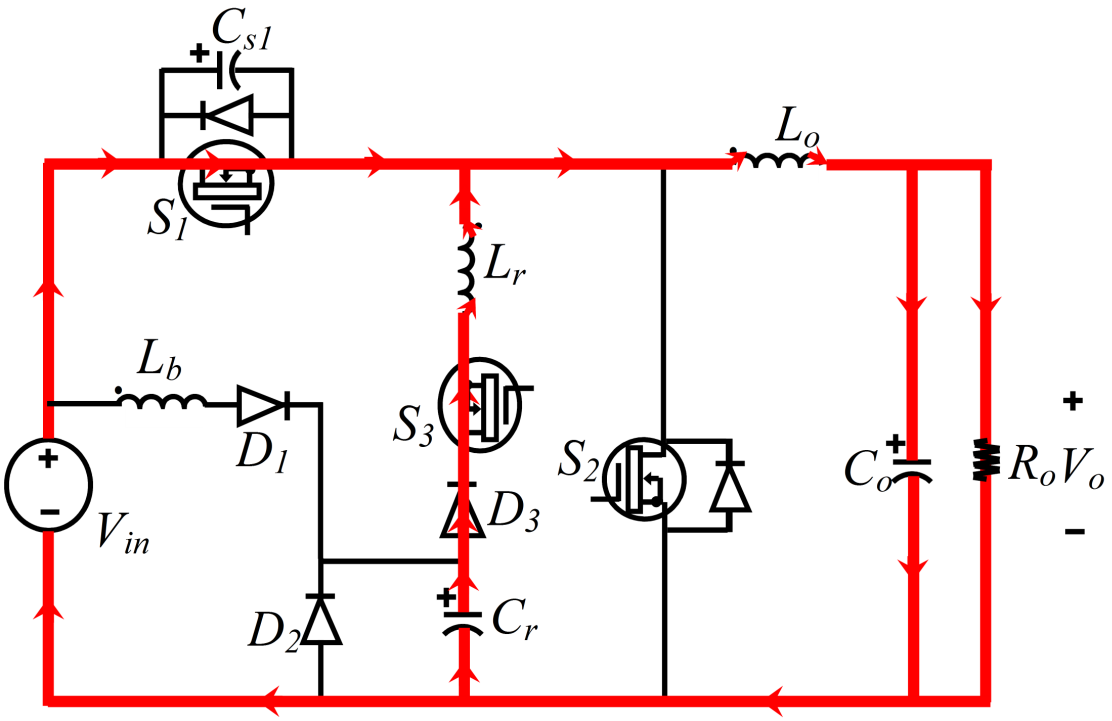


Fig. 2.3 (h): Modes of operation: Mode 8 (t_7 — t_8)

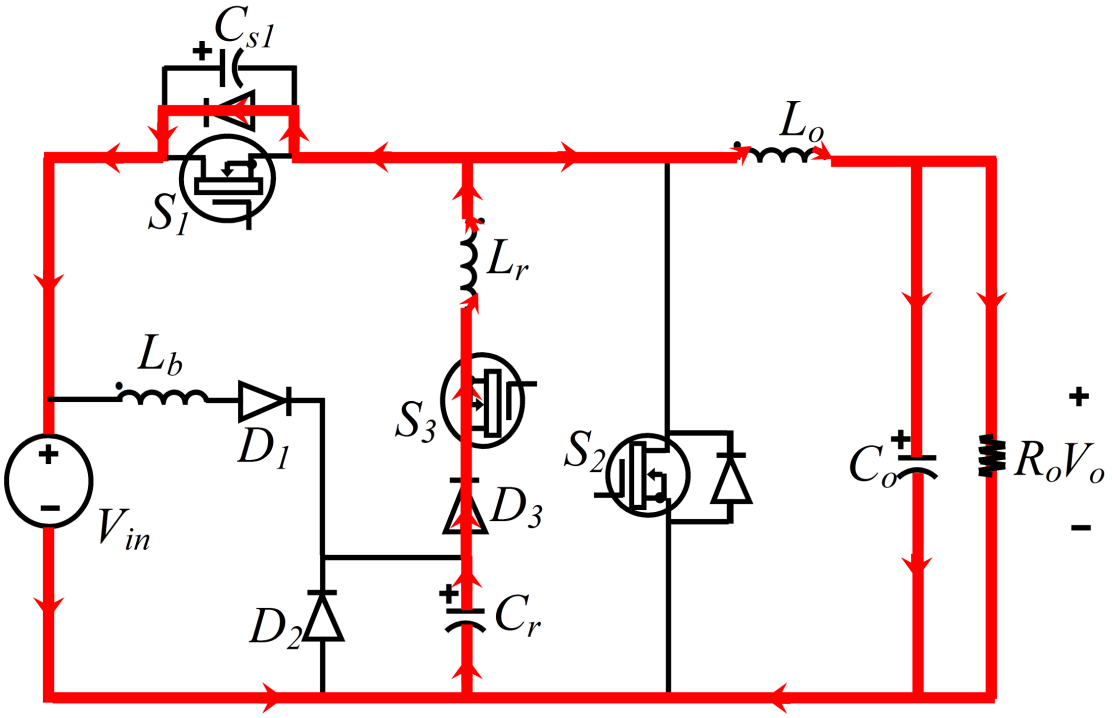


Fig. 2.3 (i): Modes of operation: Mode 9 (t_8 — t_9)

$$V_{Cs1} = \frac{1}{C_{s1}} \int_{t_9}^{t_{10}} (I_{Lr} - I_0)\, dt \tag{2.34}$$

At the end of this mode the capacitor C_r is completely discharged and D_2 is forward biased. The period of this mode is given by $0.39\pi/\omega_2$. The inductor L_r current is $0.23I_0$ and the voltage across capacitor C_{s1} is obtained as $0.25V_{in}$.

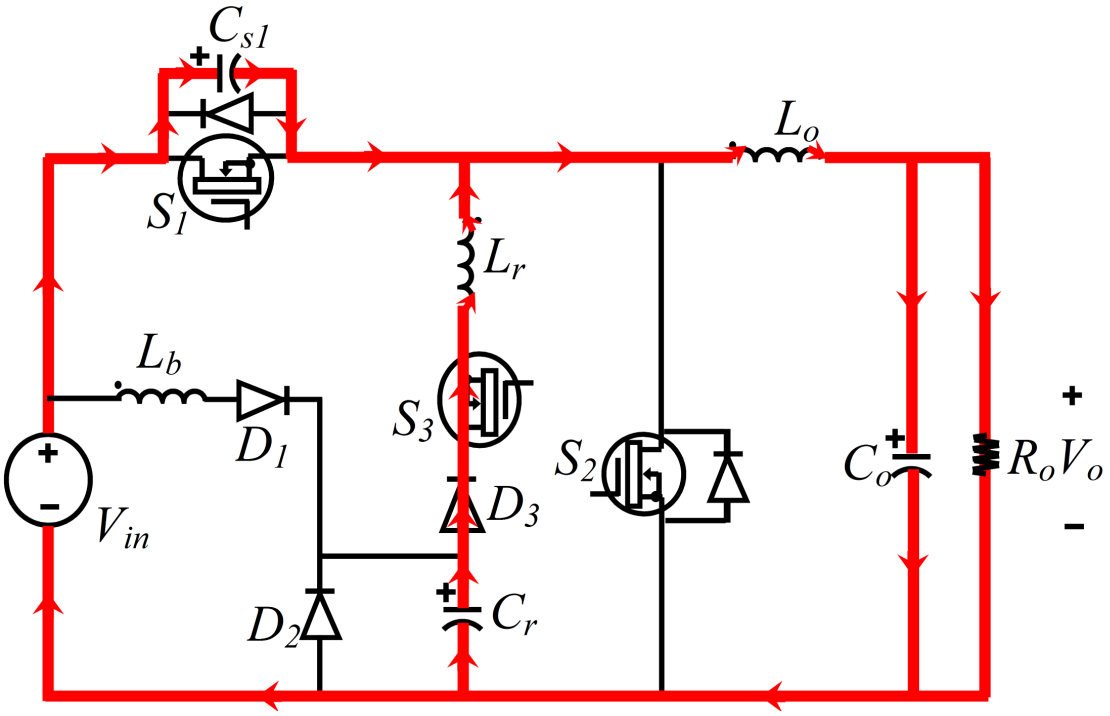


Fig. 2.3 (j): Modes of operation: Mode 10 (t_9 — t_{10})

Mode 11 (t_{10} — t_{11}): In this mode diode D_2 is conducting; the resonance takes place between L_r and C_{s1}. At the end of this mode inductor L_r current becomes zero, the auxiliary switch is turned OFF under ZC condition.

$$I_{Lr} = (1-0.23)\cos\left(\omega(t-t_{10})\right) + \left((1-0.25)(1.2)\sin\left(\omega(t-t_{10})\right)+1\right).I_0 \tag{2.35}$$

$$V_{Cs1} = 0.25V_{in} - \frac{1}{C_{s1}} \int_{t_{10}}^{t_{11}} (I_{Lr} - I_0)\, dt \tag{2.36}$$

At the end of this mode the period of this mode is $0.1\pi/\omega$ and the voltage across C_{s1} is given as $0.6V_{in}$.

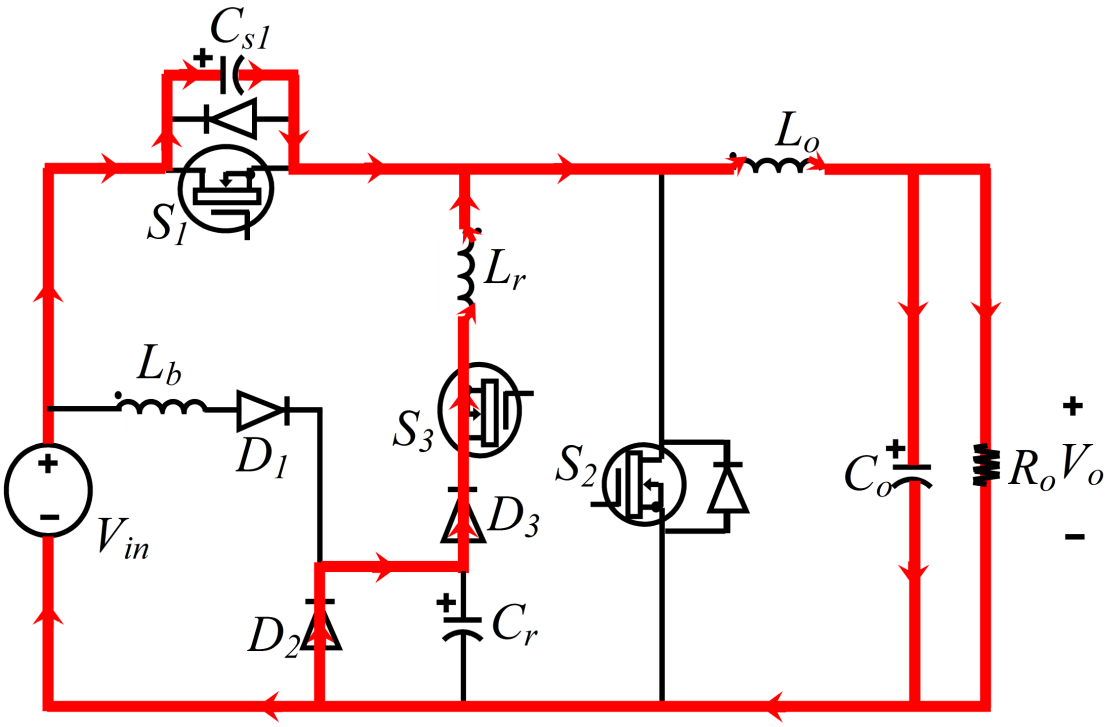


Fig. 2.3 (k): Modes of operation: Mode 11 (t_{10} — t_{11})

Mode 12 (t_{11} — t_{12}): Inductor L_r charges C_{s1} with a constant current to V_{in}, due to this the body diode of switch S_2 conducts. The period of this mode is given by

$$t_{12} - t_{11} = \frac{(1-0.6)V_{in}C_{s1}}{I_0} \tag{2.37}$$

Mode 13 (t_{12} — t_{13}): The synchronous switch is turned ON under ZV condition and due to the resonance between C_r and L_r, C_r is charged to $2V_{in}$. The equations in this period are similar to the mode 5. Prior to turn ON the main switch the C_r should be charged to $2V_{in}$, the minimum switch OFF time is given by:

$$t_{off} = \pi\sqrt{L_b C_r} \tag{2.38}$$

Mode 14 (t_{13} — t_{14}): In this mode, the synchronous switch continues to conduct and the converter operates similar to conventional PWM synchronous buck converter.

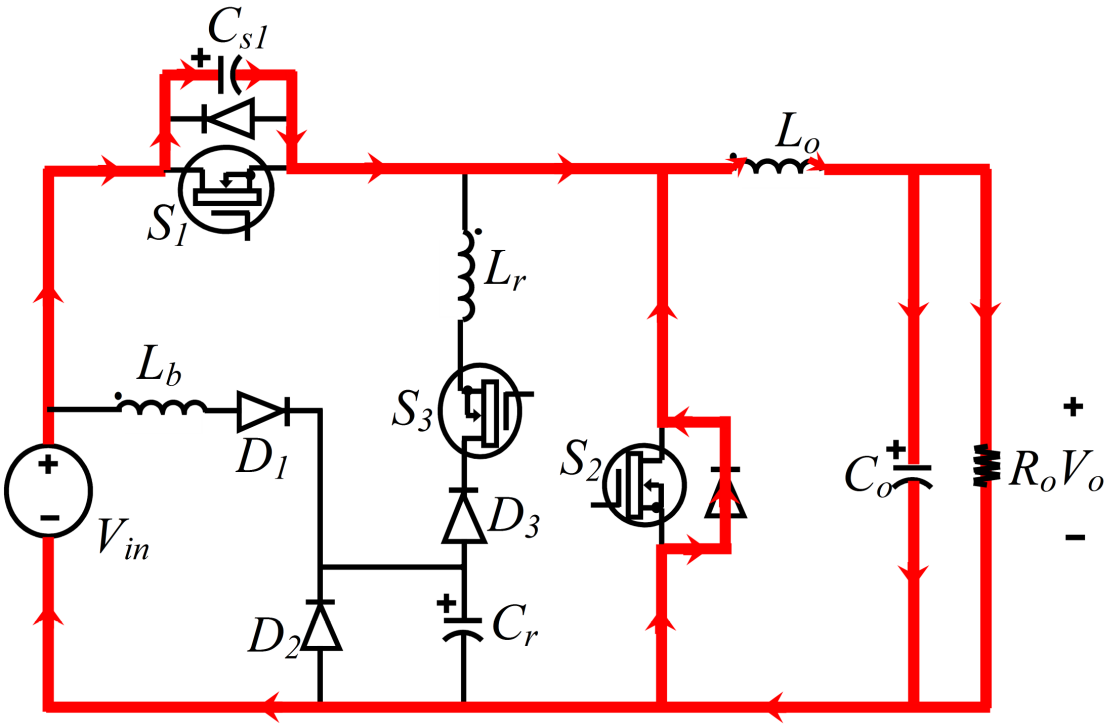


Fig. 2.3 (l): Modes of operation: Mode 12 (t_{11} — t_{12})

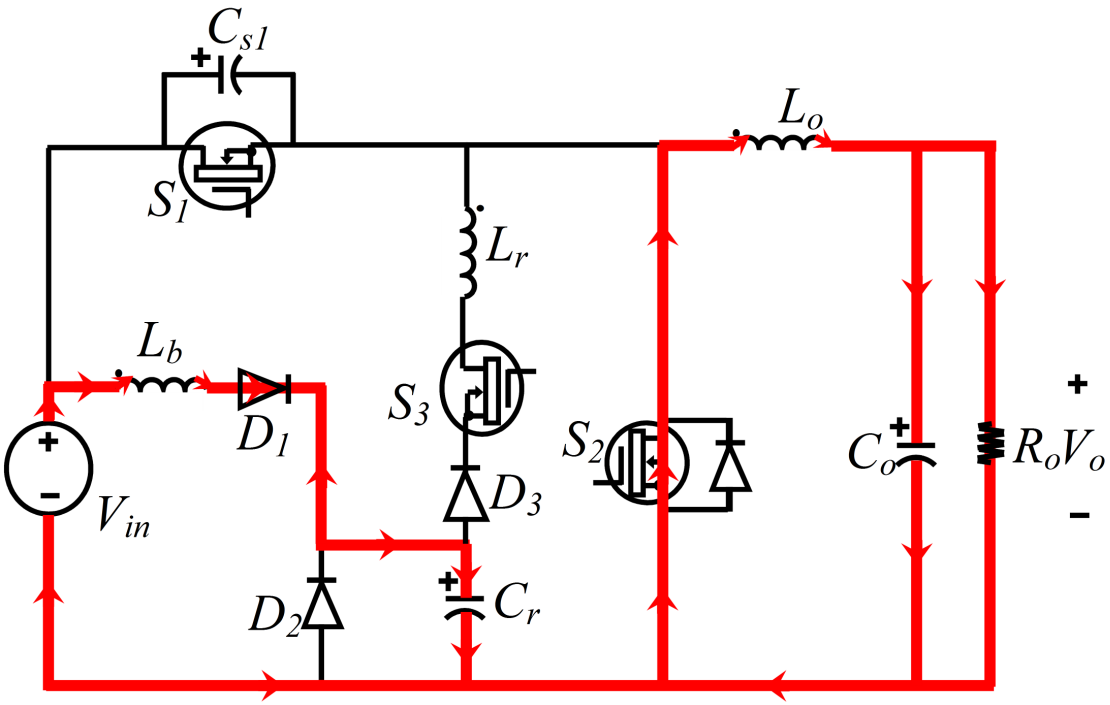


Fig. 2.3 (m): Modes of operation: Mode 13 (t_{12} — t_{13})

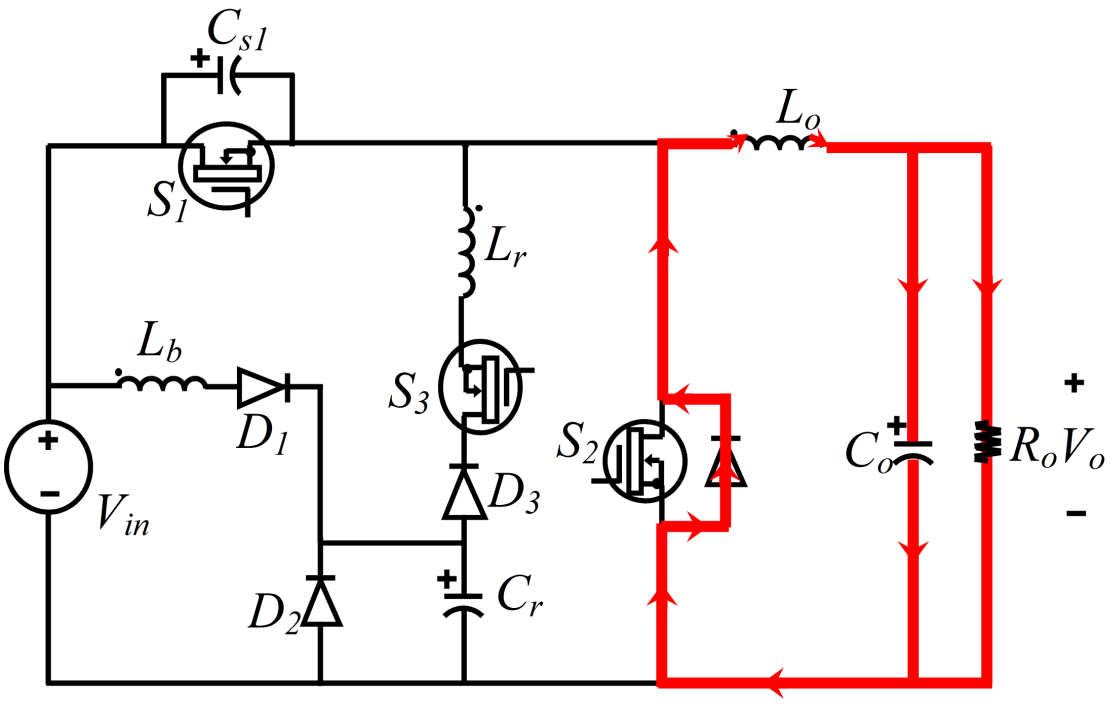


Fig. 2.3 (n): Modes of operation: Mode 14 (t_{13} — t_{14})

2.4 Design Procedure

The conventional PWM converter's design is well-known and extensively presented in the literatures. Now, it is time to focus on eloquent aspects of designing the auxiliary circuits. The snubber capacitor C_{s1}, the resonant capacitor C_r, the inductors L_r and L_b are the essential components while designing the auxiliary circuit.

2.4.1 Snubber Capacitor C_{s1}, Resonant Capacitor C_r and Inductor L_r

Snubber capacitor C_{s1} is chosen to be equal to C_r and L_r is chosen to satisfy (2.31). C_{s1} is not completely discharged when C_{s1} is selected as greater than C_r and the soft switching to turn ON the main switch is not achieved. The auxiliary switch, turn OFF condition in the mode11 is not satisfied if C_{s1} is chosen lesser than C_r. The effective duty cycle of the auxiliary switch increases as in each cycle some of the energy stored in C_r is transferred to the output in contrast with the traditional synchronous buck converter. The energy stored in each cycle in C_r is transferred to the output, exempting some of the parts which are recuperated to the input voltage source while discharging C_{s1}. This part is computed as

$$\Delta p = \left(\frac{1}{2} C_{s1} . V_{in}^2 + \frac{1}{2} L_r (1.65 - 1) I_0^2 + \frac{1}{2} C_r (1.55 - 0.45) V_{in}^2 \right) f \qquad (2.39)$$

where the first term is the energy recuperated to the input voltage source in the mode 2 and mode 3, the second exists due to the fourth mode and the third term because of the ninth mode. The remaining energy in the output is given by

$$\Delta p_0 = 2.\frac{1}{2} C_r .(2V_{in})^2 .f - \Delta p \tag{2.40}$$

The C_{s1} is designed by using the equation (2.31) i.e.,

$$\frac{V_{in}}{Z} = 1.2 I_{0max} \text{ where } I_{0max} = 15\text{A (approx.)}, V_{in} = 12\text{V}$$

$$Z = \sqrt{\frac{L_r}{C}} \text{ where } C = C_r = C_{s1}.$$

By the above equation either L_r or C has to be chosen value. Based on the simulation, experimental study and analysis of the converter L_r is chosen as 4µH. Substituting L_r= 4µH we get C_{s1}= C_r= 18nF which is adjusted to 22nF for getting satisfactory operating analysis and efficiency enhancement.

2.4.2 Inductor L_b

L_b should be greater than L_r is assumed in the theoretical analysis. The simulation results of the converter to operate according to the theoretical analysis as predicted, L_b is chosen as follows:

$$L_b \geq 5L_r \tag{2.41}$$

2.5 Simulation and Experimental Results

The proposed active auxiliary circuit is incorporated with synchronous buck converter with an input voltage V_{in} = 12V, output current I_o = 15A, output voltage V_o = 5V, switching frequency at 100 kHz has been implemented and validated with experimental results. The operating characteristics of the proposed converter are shown by simulation using PSIM co-simulated with MATLAB/SIMULINK environment. Table 2.1 shows the major parameters and components used in the power circuit of proposed converter. Fig. 2.4 (a)-(e) shows the simulation results of the proposed converter and Fig. 2.5 (a)-(e) presents the experimental results that validate the operation of proposed converter. The Fig. 2.7 shows the experimental setup of the proposed ZVT-ZCT PWM SBC.

TABLE 2.1

COMPONENTS USED FOR PROPOSED CONVERTER

Component	Value/Model
Main switch S_1	IRF640
Synchronous Switch S_2	IRF640
Auxiliary Switch S_3	IRF640
Schottky diode, D_1	BYV28-200
Schottky diode, D_2	BYV28-200
Schottky diode, D_3	BYV28-200
Inductor, L_r	4µH
Inductor, L_b	50µH
Capacitor, C_r	22nF
Output Inductor, L_o	100µH
Output Capacitor, C_o	100µF

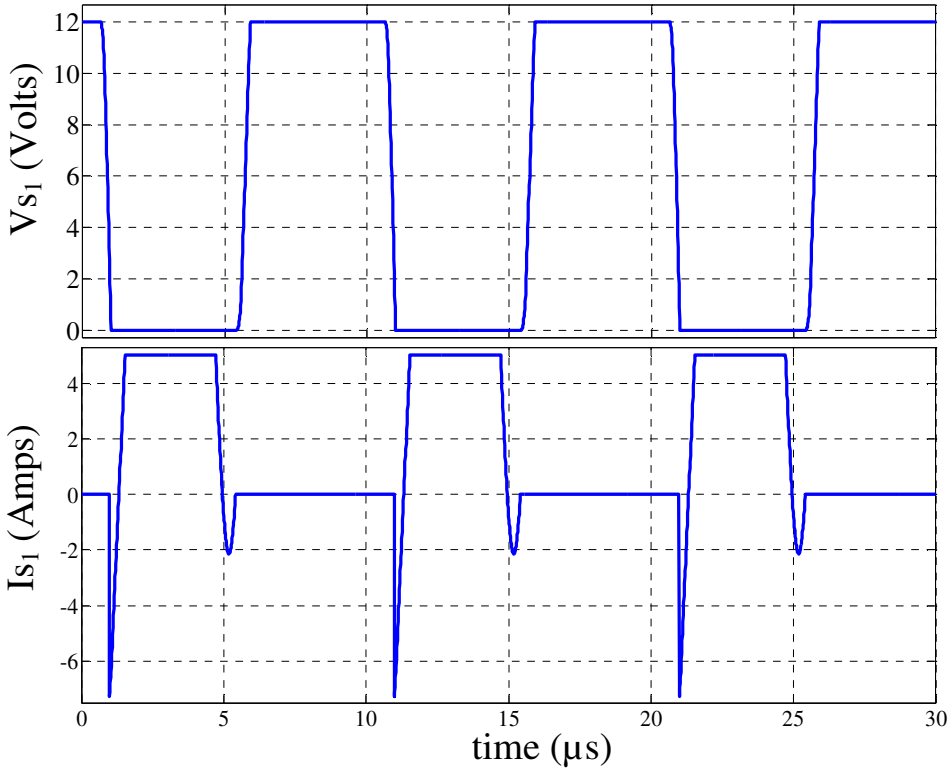


Fig. 2.4 (a): Simulated voltage and current waveforms of main switch S_1: V_{s1} in Volts and I_{s1} in Amps.

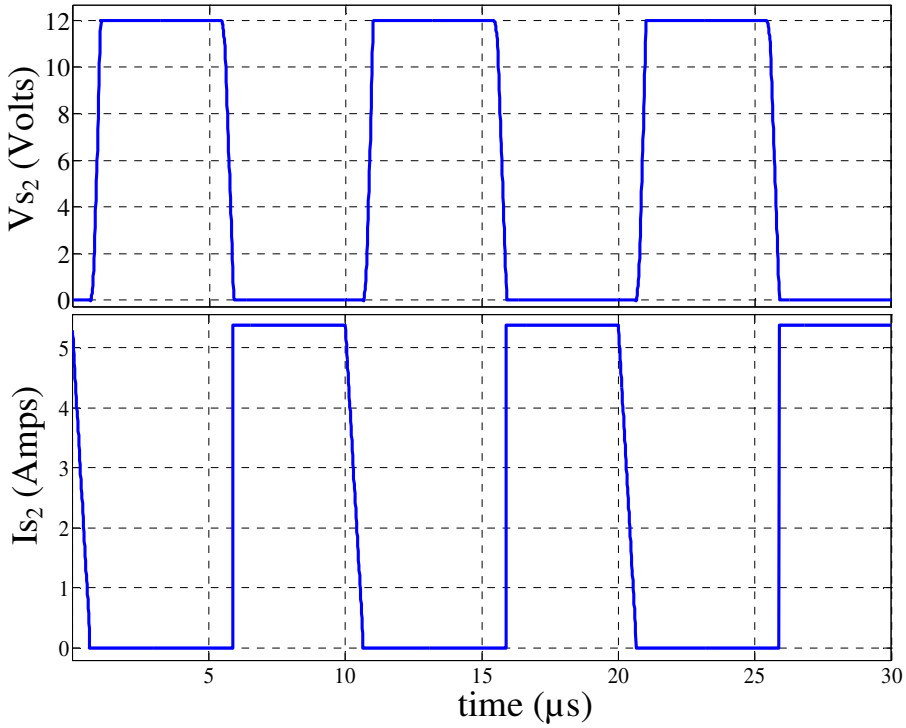


Fig. 2.4 (b): Simulated voltage and current waveforms of synchronous switch S_2: V_{s2} in Volts and I_{s2} in Amps.

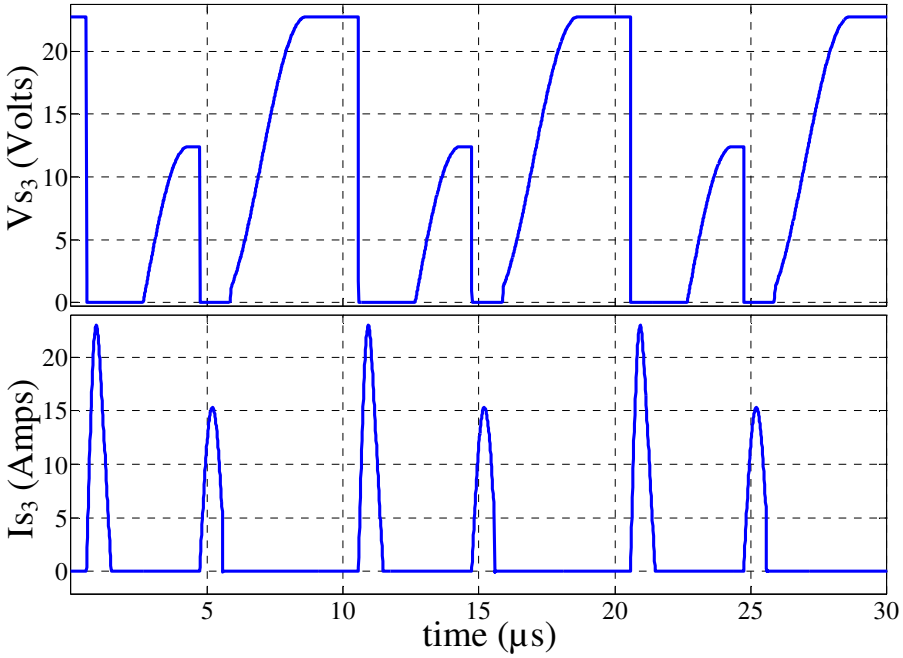


Fig. 2.4 (c): Simulated voltage and current waveforms of auxiliary switch S_3: V_{s3} in Volts and I_{s3} in Amps.

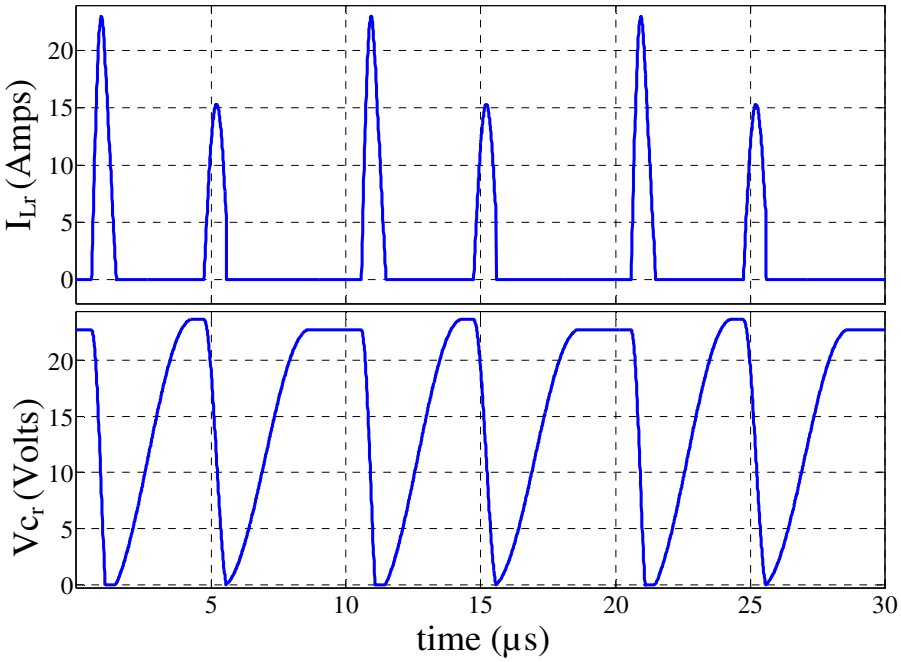


Fig. 2.4 (d): Simulated current and voltage waveforms of inductor L_r and resonant capacitor C_r: I_{Lr} in Amps and V_{Cr} in Volts.

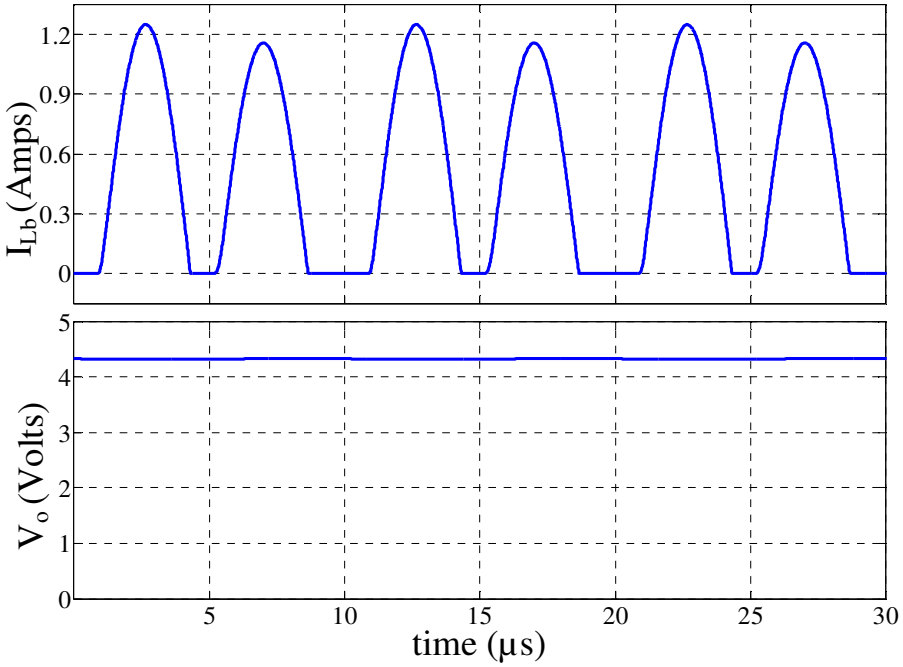


Fig. 2.4 (e): Simulated current and voltage waveforms of inductor L_b and output capacitor C_o: I_{Lb} in Amps and V_o in Volts.

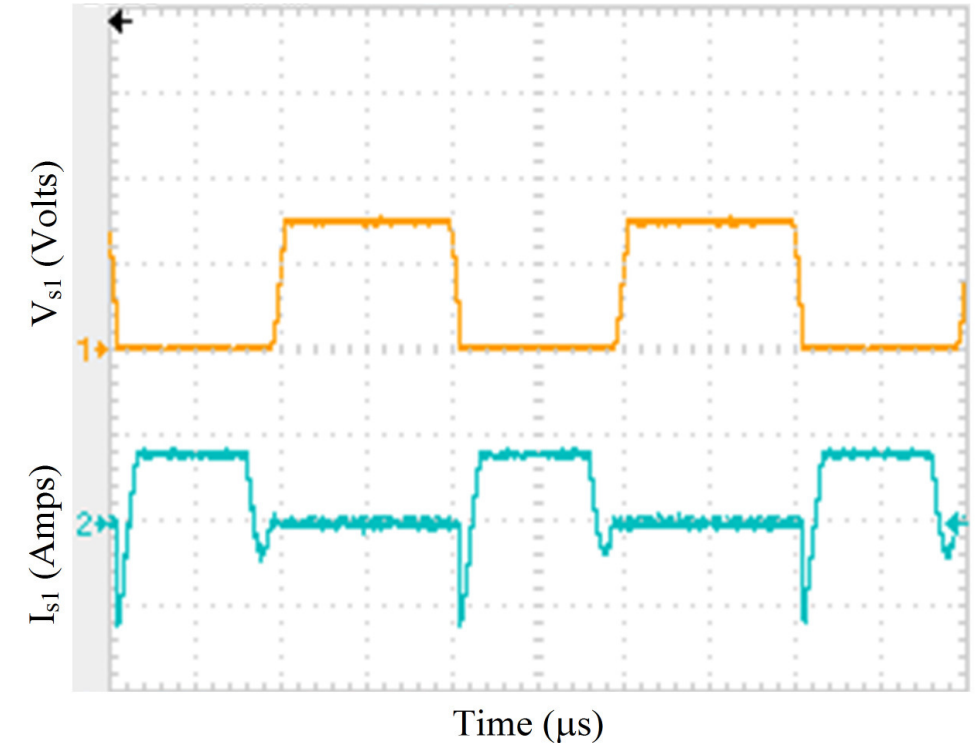


Fig. 2.5 (a): Experimental voltage and current waveform of Main switch S_1: [Vs_1: 8V/Div; Is_1: 5A/Div; time: 2.5µs/Div]

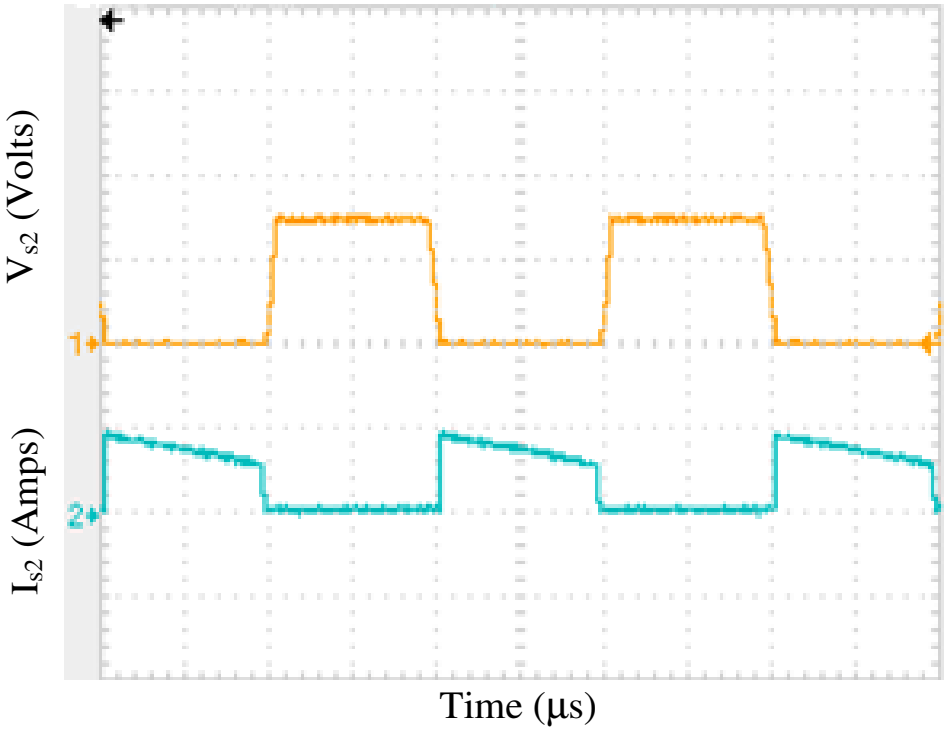


Fig. 2.5 (b): Experimental voltage and current waveform of synchronous switch S_2: [Vs_2: 8V/Div; Is_2: 5A/Div; time: 2.5µs/Div]

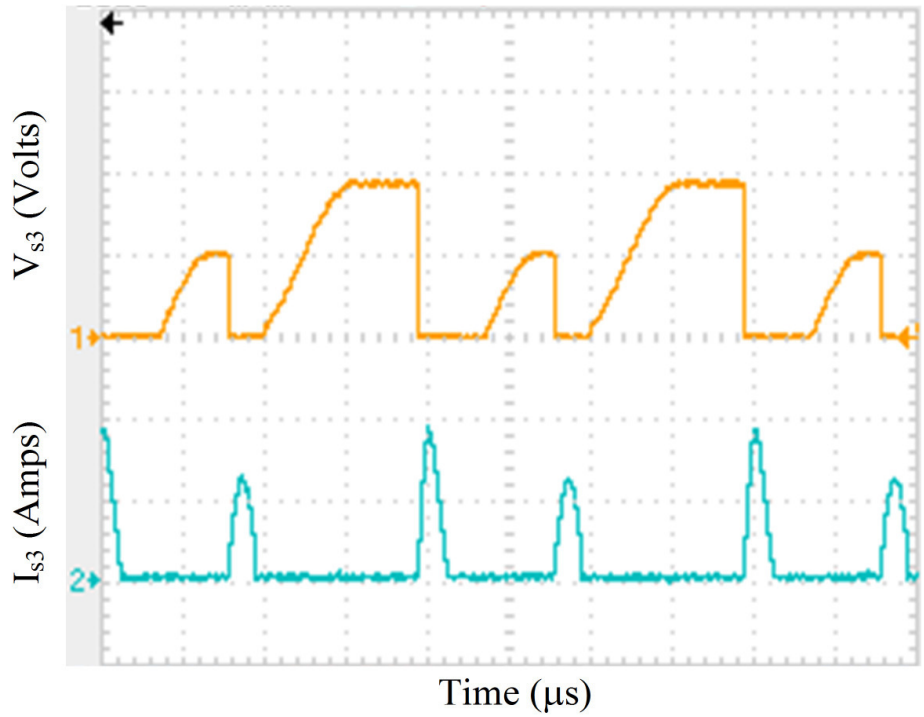


Fig. 2.5 (c): Experimental voltage and current waveform of auxiliary switch S_3: [Vs_3: 12V/Div; Is_3: 12A/Div; time: 2.5µs/Div]

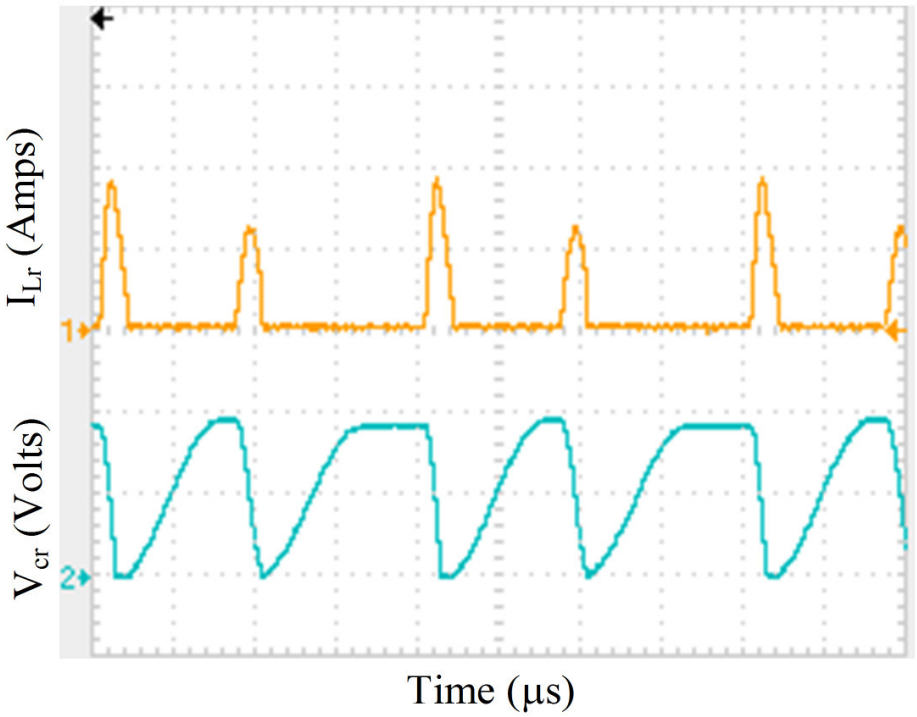


Fig. 2.5 (d): Experimental current and voltage waveform of inductor L_r and resonant capacitor C_r: [I_{Lr}: 12A/Div; V_{cr}: 15V/Div; time: 2.5µs/Div]

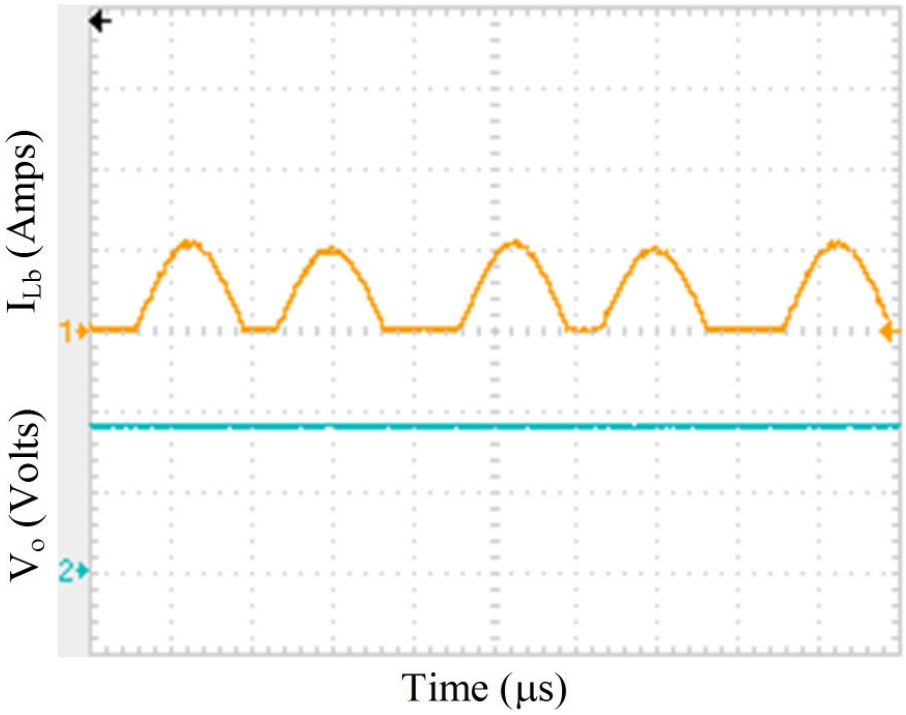


Fig. 2.5 (e): Experimental current and voltage waveform of inductor L_b and output capacitor C_o: [I_{Lb}: 1.5A/Div; V_o: 4V/Div; time: 2.5us/Div]

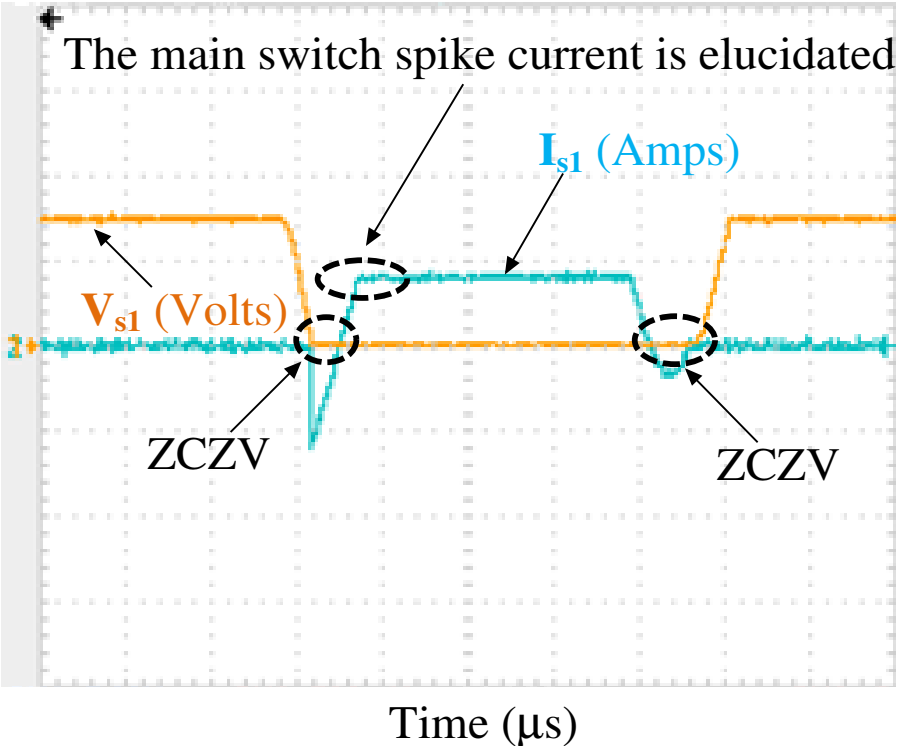


Fig. 2.6 (a): Experimental voltage and current waveforms of main switch S_1 exhibits soft switching conditions [Vs_1:8 V/Div; Is_1: 5A/Div; time: 0.1µs/Div].

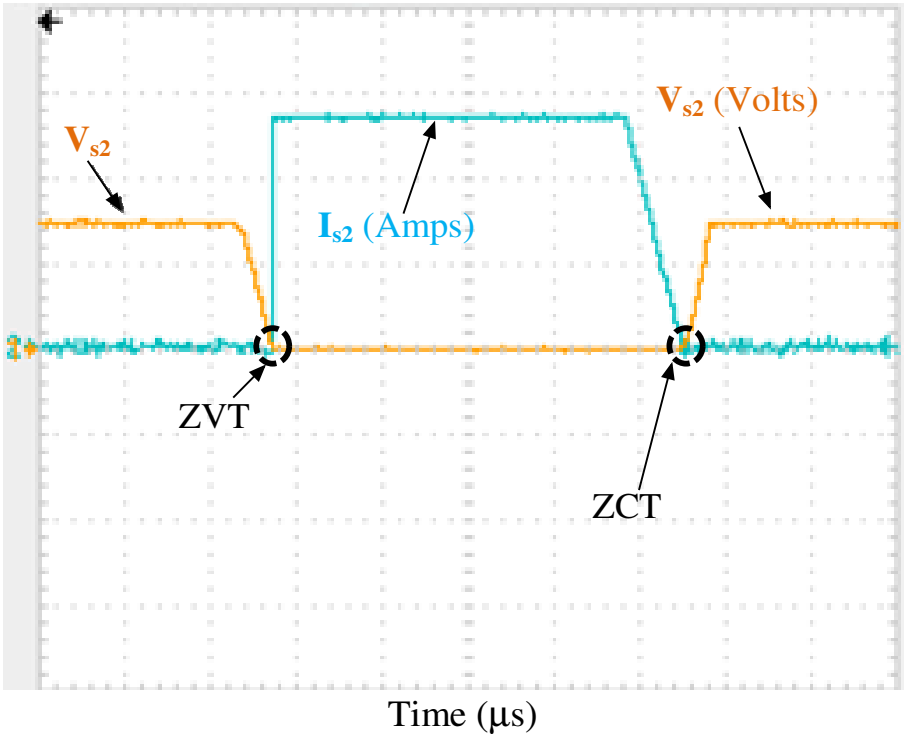


Fig. 2.6 (b): Experimental voltage and current waveforms of synchronous switch S_2 exhibits soft switching conditions [Vs_2:8V/Div; Is_2:5A/Div; time: 0.1µs/Div].

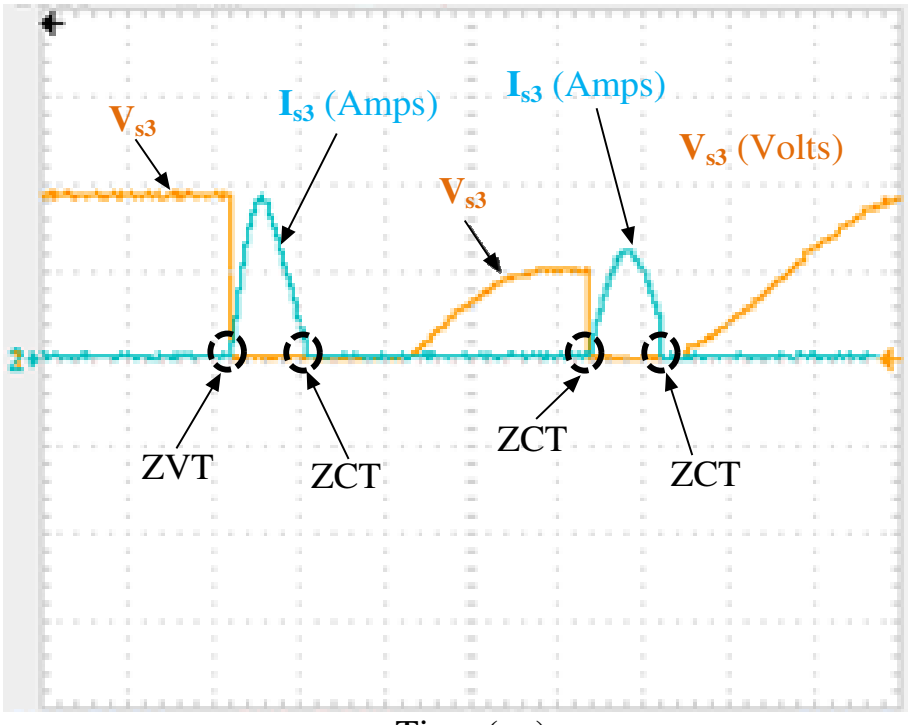


Fig.2.6 (c): Experimental voltage and current waveforms of auxiliary switch S_3 exemplifying soft switching conditions [Vs_3:12V/Div; Is_3:12A/Div; time: 0.1µs/Div].

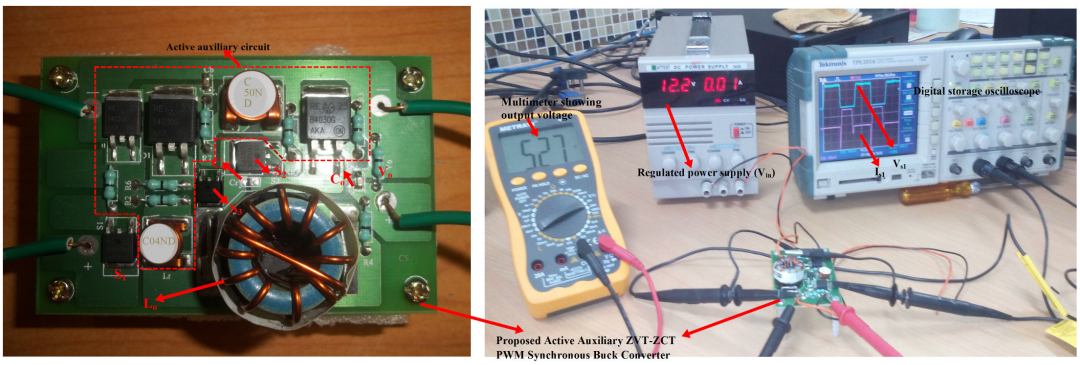


Fig. 2.7: Experimental setup of Proposed ZVT-ZCT PWM synchronous Buck Converter

2.5.1 Main switch S_1

From Fig's. 2.4 (a), 2.5 (a) and 2.6 (a) that the main switch S_1 is turned ON under ZCZV condition when the inductor current I_{Lr} reaches above the output current and turned OFF under ZCZV condition when I_{Lr} falls below the output current. Fig. 2.6 (a) signifies that the main switch S_1 spike current fall significantly; the waveform replicates the traditional buck converter. Therefore, the rating of the main switch required for the buck converter is economized by the introduction of ZVT-ZCT operation.

2.5.2 Synchronous switch S_2

From Figs. 2.4 (b), 2.5 (b) and 2.6 (b) the synchronous switch S_2 is turned ON under ZV condition when resonant capacitor is charged to $2V_{in}$ during the resonance with L_b and turned OFF under ZCZV condition when L_r current become equal to the output current. The synchronous switch has low stress and operates within the tolerable limits.

2.5.3 Auxiliary switch S_3

It is noted from Figs. (2.4 (c), 2.5 (c) and 2.6 (c) the auxiliary switch S_3 operates under soft switching conditions. In the proposed auxiliary circuit the switch conducts twice in one switching cycle. Initially the switch conducts under ZV condition and turns OFF under ZC condition. Later, as the inductor L_r is in series with switch S_3 it operates under ZC condition when it is turned ON and it is turned OFF under ZC condition when the inductor L_r current falls to zero. The voltages of main switch S_1 and synchronous switch S_2 are stressless while auxiliary switch S_3 has small overshoot compared to the traditional buck converter.

2.6 Efficiency curve

Fig. 2.8 shows the efficiency comparison of the proposed converter with the traditional buck converter at the same circuit conditions. The proposed converter has the efficiency of

96% at maximum load in contrast to the conventional buck converter. At light loads, the efficiency is increased to 90% compared to the traditional buck converter. From fig. 7 it can be seen that efficiency values of the proposed converter are comparatively higher than the traditional buck converter at different loads.

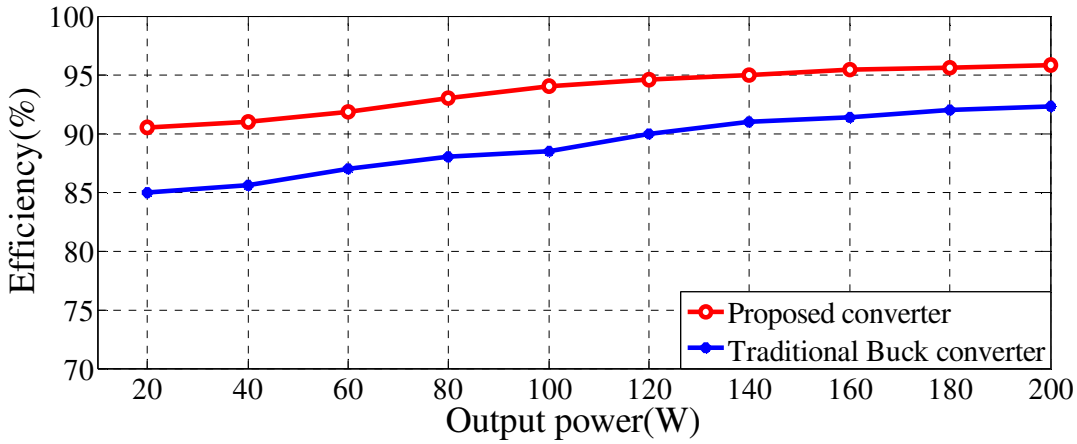


Fig. 2.8: Efficiency curve of the proposed converter in comparison with traditional buck converter

2.6.1 Contrast with contemporary topologies

Table 2.2 shows the comparison of recent topological circuits with relatively same operating conditions in comparison to the proposed circuit. As shown in the Table 2.2, the circuits are contemporary ZVT-ZCT PWM topologies [116, 117] are prominent in curtailing the spike of the main switch and diminishing the reverse recovery (RR) problem of the synchronous switch body diode. The RR problem of main diode is eliminated. In [116] the coupled inductor is used in the auxiliary circuits which inturn expands the volume of the total circuit. Compared to [116, 117] the stresses on the main and synchronous switches are negligible. The proposed auxiliary circuit not only exceeds the advantages of the contemporary circuits, but also obliges the switches to operate under soft switching conditions. The RR problem compared to conventional circuits is largely enhanced, besides the efficiency is improved at maximum. Efficiency enhancement relative to the hard-switching converter is shown in fig. 2.8. Fig. 2.11 presents that the efficiency of the proposed ZVT–ZCT SBC is comparatively high with reference to the contemporary topologies. At low loads, the proposed converter and the converters of [116], [117] attaining equivalent performance, but as load increases the performance of proposed ZVT-ZCT SBC is superior to the contemporary topologies. The Table 2.2 and the results proclaim that the proposed auxiliary circuit has accomplished comparable efficiency enhancement over the hard switching circuit to a decent value. The voltage stresses from the results, it is evident that

they are almost equal to the input voltage (V_{in}) except the auxiliary switch which is twice the input voltage ($2V_{in}$) though it is outweighed by the performance enhancement of the converter. The proposed converter doesn't use the coupled inductor as [116] and also it has a simple design and is easy to control.

2.6.2 Overview of the contemporary topologies [116] and [117]

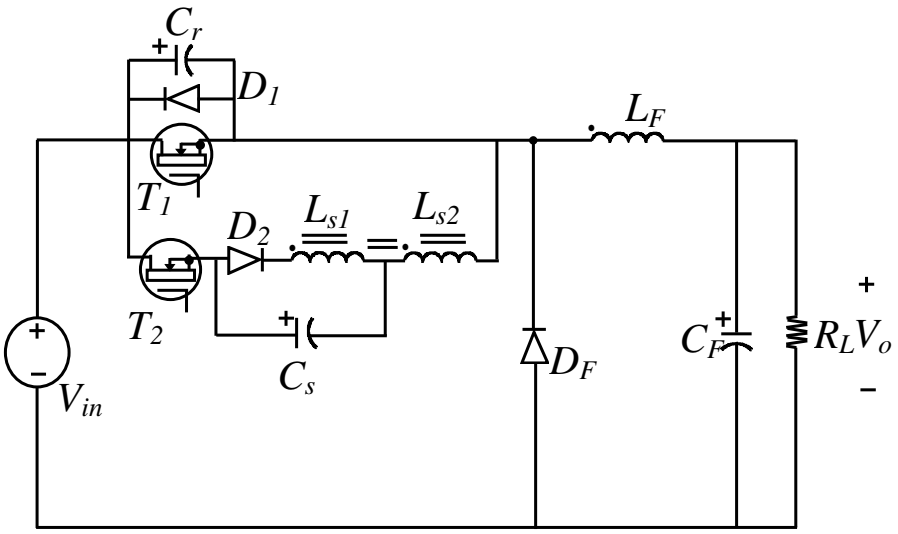


Fig. 2.9: Circuit diagram of the topology proposed by S. Urgun [116]

S. Urgun [116] has proposed a new ZVT-ZCT quasi-resonant buck converter, which ensures soft switching at the zero crossings that provides ZVT turn-ON and ZCT turn-OFF together for the main switch of active snubber cell presented in [116]. The circuit combines most of the advantages similar to the previous published works such as the semiconductor devices used operate under soft switching conditions. The soft switching operation of the new converter is maintained for the whole line and load ranges. The circuit scheme of [116] is shown in the fig 2.9. The active snubber cell consists of a centre tapped and a magnetically coupled snubber inductor (L_{s1} and L_{s2}), snubber capacitor (C_s), a main switch (T_1), an auxiliary switch (T_2), the output filter capacitor (C_F), main inductor (L_F) and two auxiliary diodes D_1 and D_2. C_r is considered to be a parasitic capacitor. The circuit is designed for 200W and 100 kHz frequency. From fig 2.11 it can be seen that at full load the overall efficiency is 96%.

Hong Tzer Yang [117] has proposed a new dual resonant tank circuit for high frequency ZVT PWM DC-DC converters with synchronous rectification. The significance of the circuit is that not only the switching loss of the main switch is reduced but also the switching losses incurred by the synchronous rectifier (SR) are minimized. Further, the SR can be turned-on

with ZVS condition by the proposed resonant tank. The advantages of using SR are thus retained to reduce the conduction loss in place of the diode in the original circuit. The diodes and auxiliary switch in the proposed resonant tank circuit operates with soft switching condition. The circuit of the [117] is shown in the fig. 2.10. The circuit consists of a filter inductor Lm, main switch S_1 and SR switch S_{SR}, the dual resonant tank is formed by resonant inductors L_{r1}, L_{r2}, resonant capacitor C_r, auxiliary switch S_a and auxiliary diodes D_1, D_2 and D_3. The circuit is designed for 200W, 100 kHz frequency and the efficiency at full load is achieved as 95%.

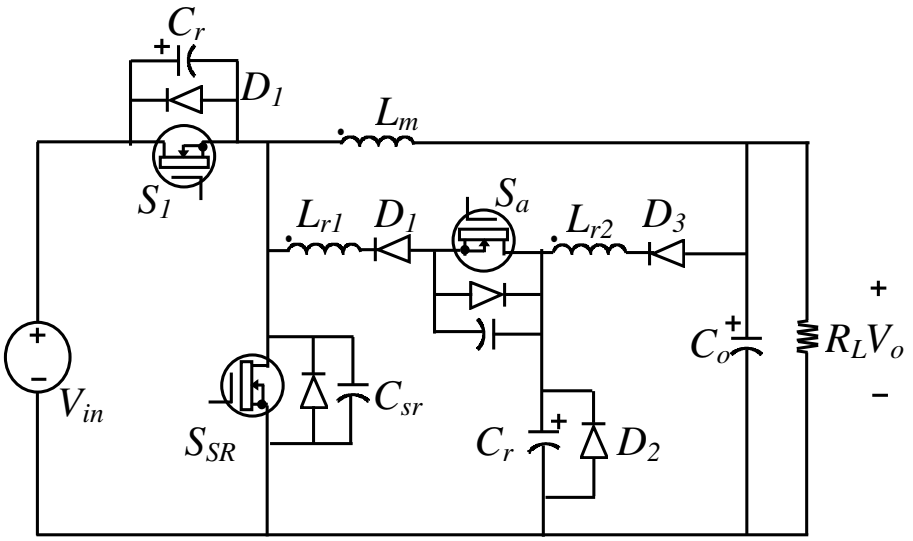


Fig. 2.10: Circuit diagram of the topology proposed by Hong Tzer Yang [117]

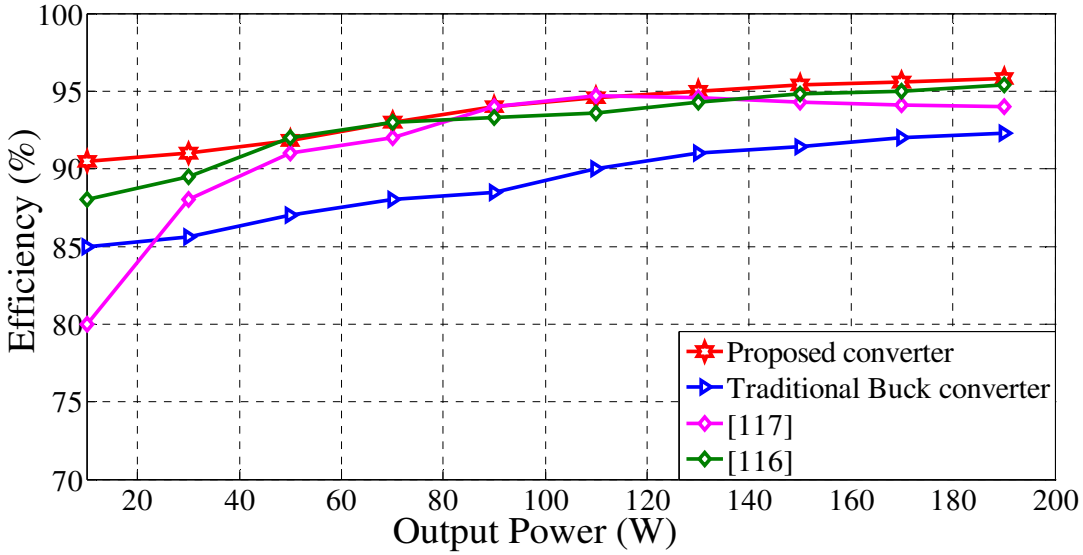


Fig. 2.11: Efficiency curve of the proposed converter in contrast with contemporary topologies

TABLE 2.2

Contrast with contemporary topologies

	Converter proposed by S. Urgun [116]	Converter proposed by Hong-Tzer yang [117]	Proposed ZVT-ZCT PWM SBC converter
Stresses on main switch (spike current, spike voltage)	Low	Low	Very low
Stresses on synchronous switch (spike current, spike voltage)	Low	Low	Eliminated
Reverse recovery of main diode	Eliminated	Replaced by SR	Replaced by SR
Reverse recovery of SR diode	Eliminated	Eliminated	Eliminated
Overhead of auxiliary circuit 1. Switch 2. Diode 3. Inductor 4. Capacitor 5. Coupled inductor	 1 2 0 1 1	 1 3 2 1 0	 1 3 2 1 0
Maximum Efficiency improvement over hard switching circuit	4.5	5	7

2.7 Summary

A new active auxiliary circuit is incorporated with the synchronous buck converter. The auxiliary circuit provides zero current and zero voltage condition for the main switch while zero current switching condition for auxiliary switch. Due to the embodiment of the auxiliary circuit the voltage and current stresses on the main and the synchronous switch of the converter get pacified as it is evident from the fig. 2.4 (a) and 2.5 (a). The main feature of ZVT-ZCT (Zero-Voltage-Transition- Zero Current Transition) in the proposed converter is attained by the inclusion of auxiliary circuit which is responsible for the reduction of switching losses that inturn enhances the performance of the converter. In addition to that, the voltage and current stresses of the switches are at tolerable limits. The efficiency of the converter is enhanced in contrast with the conventional PWM synchronous buck converter. The performance of the proposed converter is superior to the contemporary topologies as the load increases which depicts from fig. 2.11. The theoretical analysis of the proposed converter is validated by simulation and experimental results.

Chapter 3

A PASSIVE AUXILIARY CIRCUIT INTEGRATED WITH SYNCHRONOUS BUCK CONVERTER FOR PERFORMANCE ENHANCEMENT

CHAPTER 3: A PASSIVE AUXILIARY CIRCUIT INTEGRATED WITH SYNCHRONOUS BUCK CONVERTER FOR HIGH CURRENT APPLICATION

3.1 Introduction

The previous chapter presents the active auxiliary circuit in a synchronous buck converter that provides soft switching for reducing the switching losses. The soft switching with active auxiliary circuit enhances the performance of the converter, but an additional switch is used in active auxiliary circuit which leads to a complex control and increase in the cost. To overcome such limitations a simple auxiliary circuit consisting of a combination of a diode, a capacitor and an inductor is built.

In the recent years, the synchronous rectifiers are playing a prominent role in reducing the losses in conduction, as MOSFETs are employed for low-voltage applications [99-100, 128-131]. In earlier days, it was difficult to operate the converter above 1MHz, but by the advent of resonant switching, the dominant switching frequency loss is reduced. The inclusion of passive auxiliary circuits in synchronous rectifiers for reduction of switching losses which imposes a tolerable voltage and current stresses on the power switches including alleviating the problem of EMI in the converter.

A great deal of research has been done using passive snubber circuitry in many DC-DC topologies for improving the efficiency, reducing of the losses in switching and conduction to recuperate the energy [132-136]. By the inclusion of passive circuits, the converters tend to shrink in terms of cost, size, and also they are proving to be consistent modules having an eminent performance ratio than the active circuits [137-144].

The proposed circuit in this chapter greatly pacifies the reverse recovery peak current through the diode, turn ON and turn OFF loss of the switch. The demand of higher input voltage, lower output voltages, and inturn higher output currents lead to very low duty cycles and mounting the switching losses, thereby resulting in falling off the conversion efficiency. Thus, the efficiency of SBC is optimized by annihilating the switching losses using a soft switching technique with the assistance of a passive snubber. The operation of ZVT-ZCT converters almost replicate with the PWM converters having low switching and conduction losses have allured the attention in the recent times [90, 113, 116-117, 145-148].

The proposed auxiliary circuit has reduced ratings than the main power circuitry as it is activated for a small segment of time during the switching cycle, which leads to a minimized

switching loss in the auxiliary circuit and thereby improving the converter efficiency as switching losses gets diminished. Many other topologies are presented in the literature. Among them, the high-frequency transformers included in DC-DC converters have also proven to be well known topologies. However, in these converters by the inclusion of high-frequency isolation transformer, the usage of number of power switches increases, usually from four to nine, results in high switching and also conduction losses.

Lowering the switching losses for a low-voltage high-current application with the assistance of a simple passive auxiliary circuit as a snubber with low values of components was not present in the [96-100, 113-117, and 128-151]. Thus, this chapter presents a novel ZVT-ZCT PWM SBC by the addition of resonant auxiliary circuit in the proposed converter that exhibits ZVT, ZCT which curtails voltage and current stresses on the main switch and the synchronous switch.

This chapter is organised as follows: section 3.2 describes about the proposed topology. Section 3.3 explains the principle of operation and its operating modes. Section 3.4 shows the derivation of the output voltage. Section 3.5 provides the design procedure of auxiliary circuit elements used. Section 3.6 includes the simulation and experimental results that exposes the features of the proposed converter. In section 3.7, efficiency curve is shown that explains the operation of the converter over a wide range of load; also the efficiency curve is compared with conventional and contemporary topologies. Section 3.8 summarises the important features.

3.2 Topology description

The Fig.1 shows the proposed schematic circuit. The proposed converter is the embodiment of the traditional PWM synchronous buck converter and auxiliary snubber circuit proposed. The Proposed auxiliary circuit is comprised of a resonant inductor L_r, a resonant capacitor C_r, a buffer capacitor C_b, a buffer inductor L_b and auxiliary schottky diodes D_1, D_2. The utilization of body diodes of S_1 , S_2 is also done in the proposed converter.

To simplify the analysis of steady-state operations of the proposed converter, the following conditions are assumed in a switching cycle.

1. Output capacitor C_o and output inductor L_o are large.
2. Diode's reverse recovery time is negligible.
3. Energy storage components or elements are lossless.

4. L_o is very large than resonant inductor L_r.

5. The resonant components or circuits are ideal.

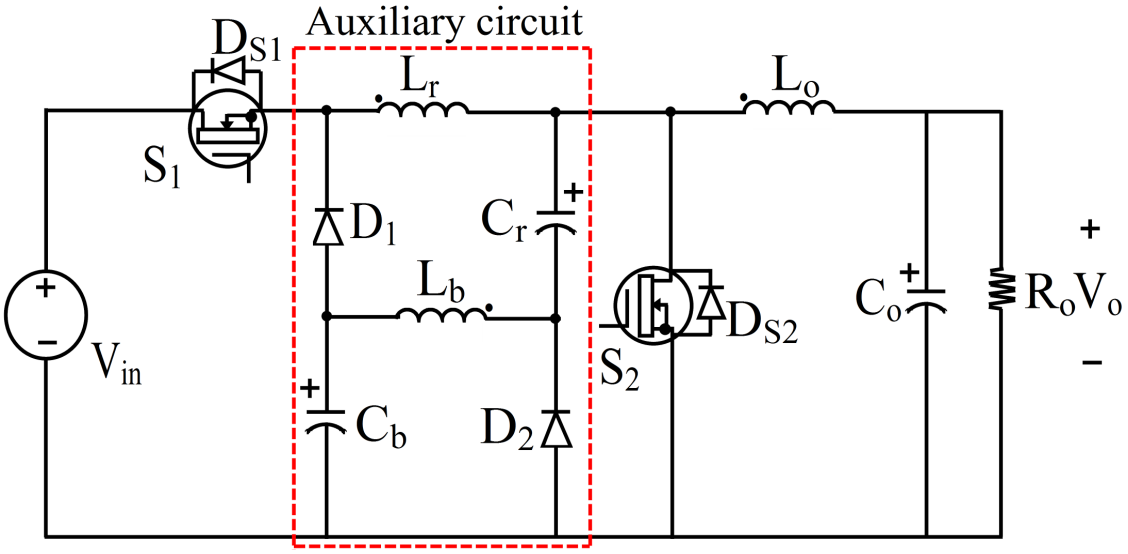


Fig.3.1: Proposed ZVT-ZCT PWM Synchronous buck converter with passive auxiliary circuit

3.3 Operational modes

In this section, the operating modes of the proposed converter are distinguished into six, considering the different current paths of the elements and switch voltages. The waveforms are presented in fig. 3.2, and the operating mode analysis is explained by the current paths shown in fig. 3.3.

Mode 1 (t_0 — t_1): In this mode 1, main switch, S_1 is switched ON. The current path is as shown in figure. At this stage, as the main switch is ON, it experiences zero current turn ON as it is in the series with resonant inductor L_r, the i_{Lr} current rises and i_{Ds2} current through the body diode of the switch S_2 falls concurrently at the same instant of time. This mode ends at $t = t_1$, i_{Ds2} becomes zero and i_{Lr} reaches $I_{o(avg)}$.

$$i_s = i_{Lr} = \frac{V_{in}}{L_r}(t - t_o) \tag{3.1}$$

$$i_{Ds2} = I_{o(avg)} - i_{Lr} = I_{o(avg)} - \frac{V_{in}}{L_r}(t - t_o) \tag{3.2}$$

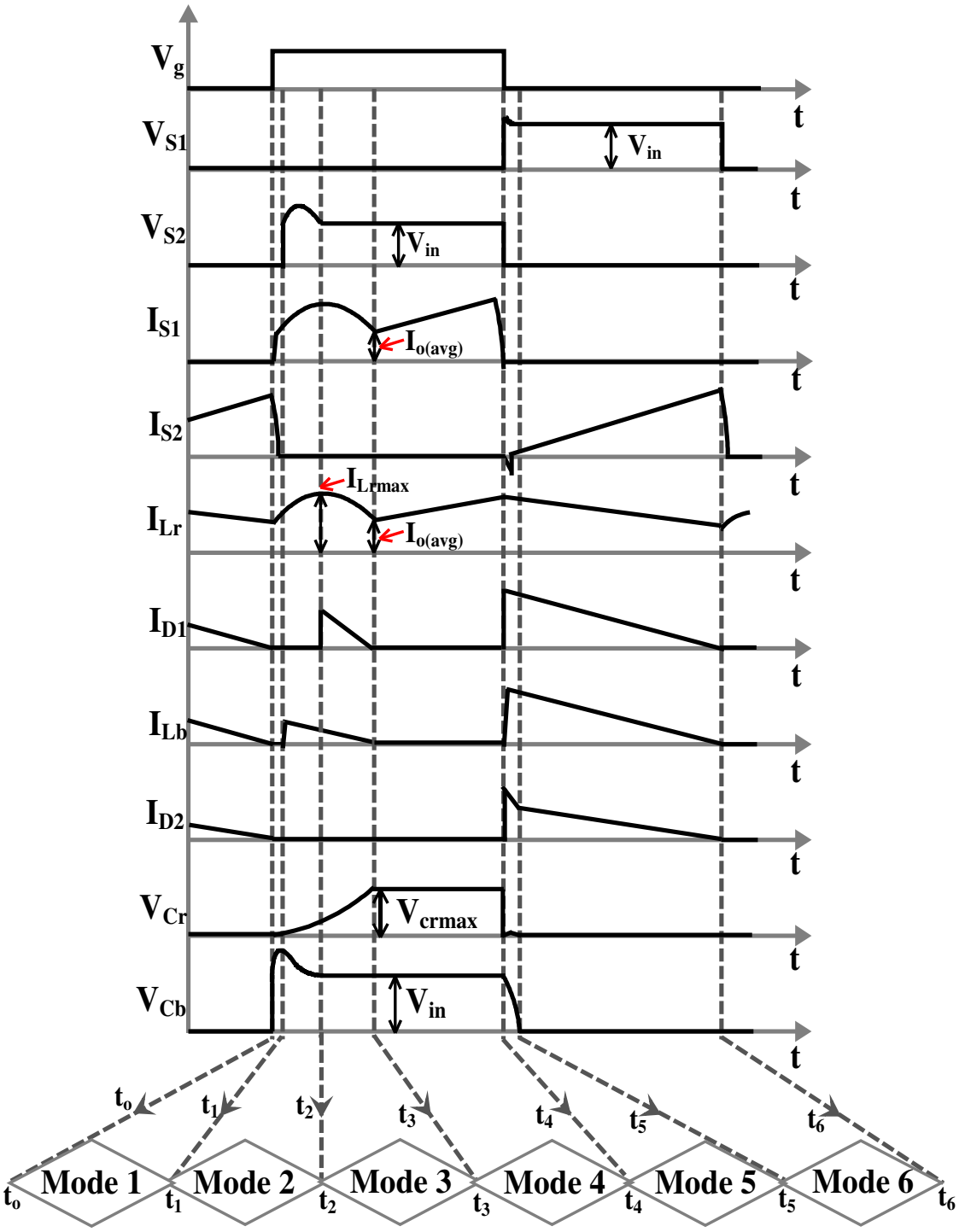


Fig. 3.2: Essential theoretical waveforms of proposed converter

$$t_{01} = \frac{L_r}{V_{in}} * I_{o(avg)} \tag{3.3}$$

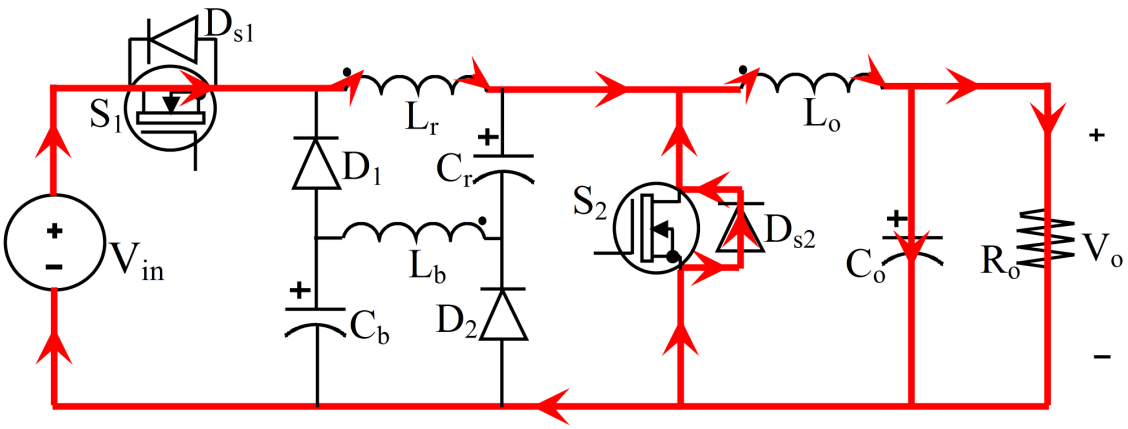


Fig. 3.3 (a): Modes of operation: Mode 1 (t_0 — t_1)

Mode 2 (t_1 — t_2): At the instant when the body diode is OFF, the current passes through the resonant circuit forming L_r, C_r and buffer capacitor C_b. At $t=t_1, i_s=i_{Lr}=I_o, i_{D2}=0$, $V_{cr}=0$ and $V_{cb}=0$. In this interval of time, resonance takes place with the inductors L_r, L_b and C_r, C_b. This mode ends with the C_b charged up to the input voltage.

$$i_{Lr}(t-t_1) = I_{o(avg)} + \frac{V_{in}}{Z_x}\sin\omega_x(t-t_1) \tag{3.4}$$

$$i_{Lb}(t-t_1) = i_{Lr} - I_{o(avg)} = \frac{V_{in}}{Z_x}\sin\omega_x(t-t_1) \tag{3.5}$$

$$V_{cr}(t-t_1) = \frac{C_e}{C_r}[-V_{in}\cos\omega_x(t-t_1)+V_{in}] \tag{3.6}$$

$$V_{cb}(t-t_1) = \frac{C_e}{C_b}[-V_{in}\cos\omega_x(t-t_1)+V_{in}] \tag{3.7}$$

Where,

$$C_e = \frac{C_r C_b}{C_r + C_b}, L_e = L_r + L_b, \omega_x = \frac{1}{\sqrt{L_e C_e}}, Z_x = \sqrt{\frac{L_e}{C_e}}$$

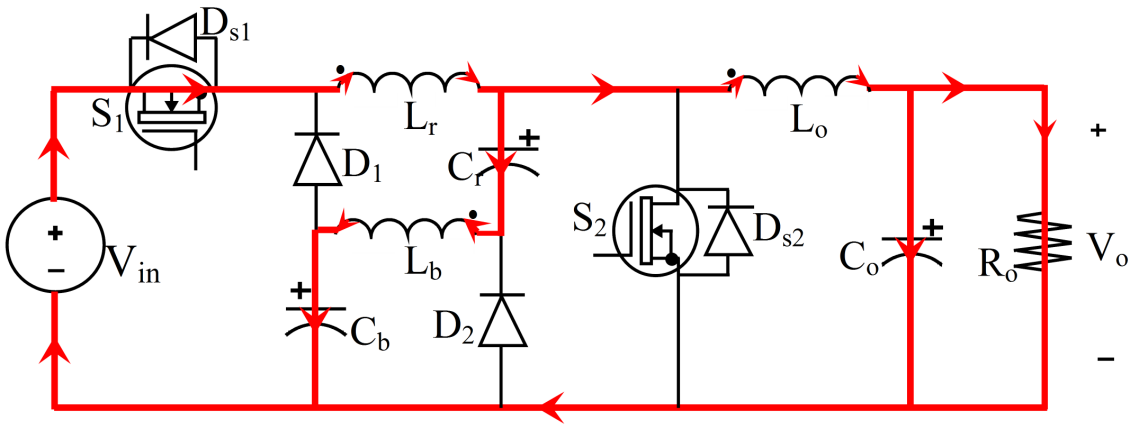


Fig. 3.3 (b): Modes of operation: Mode 2 (t_1 — t_2)

Mode 3 (t_2 — t_3): In this mode diode, D_1 gets conducted with ZVT at the instant, when V_{cb} equals to V_{in}. At $t = t_2$, $i_{S1} = i_{o(avg)}$, $i_{Lr} = i_{Lr\max}$, $V_{cb} = V_{cb\max} = V_{in}$, and $V_{cr} = V_{crx}$ when D_1 gets forward biased a new resonance takes place between L_r, L_b and C_r. This stage ends when i_{Lr} reaches to load current $I_{o(avg)}$ and C_r is charged to its maximum voltage V_{crm}.

$$i_{Lr}(t-t_2) = (i_{Lr(max)} - I_{o(avg)})\cos\omega_y(t-t_2) - \frac{V_{crm}}{Z_y}\sin\omega_y(t-t_2) + I_{o(avg)} \tag{3.8}$$

$$i_{Lb}(t-t_2) = i_{Lr}(t-t_2) - I_{o(avg)} = (I_{Lrmax} - I_{o(avg)})\cos\omega_y(t-t_2) \frac{V_{crm}}{Z_y}\sin\omega_y(t-t_2) \tag{3.9}$$

$$V_{cr}(t-t_2) = (I_{Lr(max)} - I_{o(avg)})Z_y \sin\omega_y(t-t_2) + V_{crm}\cos\omega_y(t-t_2) \tag{3.10}$$

$$t_{23} = \frac{1}{\omega_y}\tan^{-1}\left(\frac{I_{Lr(max)} - I_{o(avg)}}{V_{crm}}\right) \tag{3.11}$$

Where, $\omega_y = \dfrac{1}{\sqrt{(L_r + L_b)C_r}}$, $Z_y = \sqrt{\dfrac{L_r + L_b}{C_r}}$

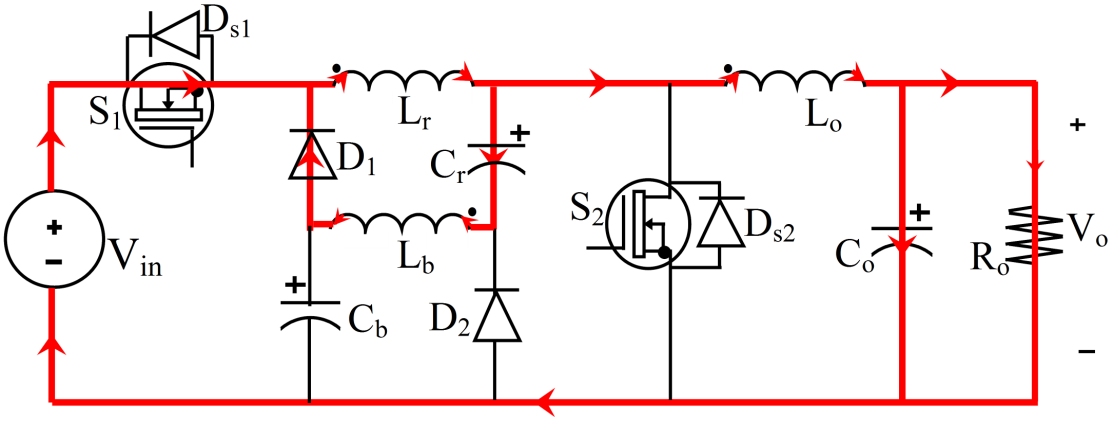


Fig. 3.3 (c): Modes of operation: Mode 3 (t_2 — t_3)

Mode 4 (t_3 — t_4): The diodes D_1 and D_2 are not in conduction mode only the main switch S_1 and resonant inductor L_r are in conduction. This depicts no resonance at this stage, and now the operational circuit is equivalent to the traditional PWM buck topology.

$$i_s = i_{Lr} = \frac{V_{in}}{L_r}(t - t_3) \tag{3.12}$$

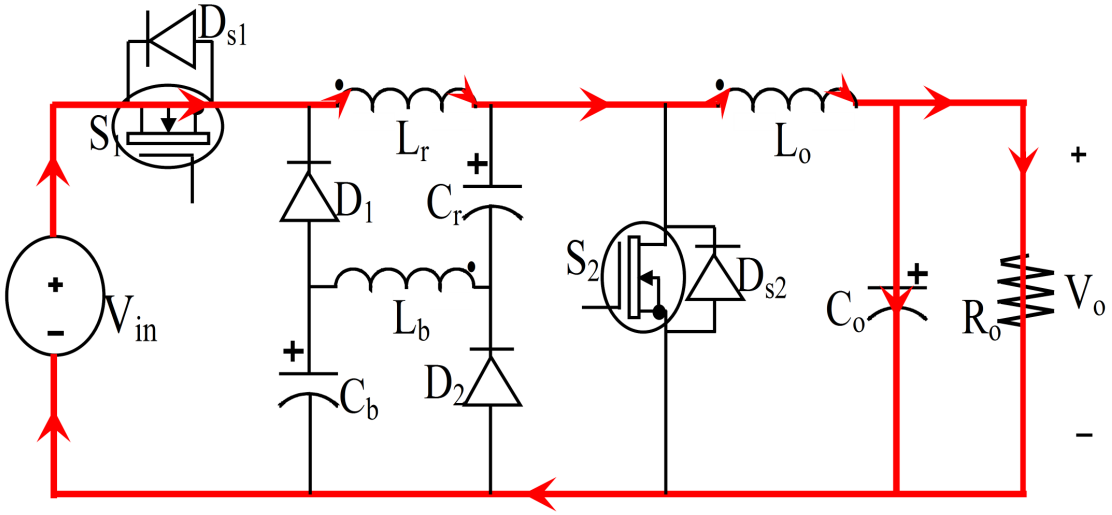


Fig. 3.3 (d): Modes of operation: Mode 4 (t_3 — t_4)

Mode 5 (t_4 — t_5): In this mode, the main switch S_1 is OFF under ZVT and at the same time synchronous switch S_2 is ON under ZCT. As S_2 is conducting, the voltage across the capacitor C_r is clenched to zero, now the resonance takes place with the parallel combination of L_r, L_b and C_b.

$$V_{cr}(t - t_4) = 0$$

$$i_{Lr}(t - t_4) = I_{o(avg)} \cos \omega_z (t - t_4) - \frac{V_{in}}{Z_z} \sin \omega_z (t - t_4) \tag{3.13}$$

$$V_{cb}(t - t_4) = \frac{V_{in}}{Z_z} \cos \omega_z (t - t_4) - I_{o(avg)} Z_z \sin \omega_z (t - t_4) \tag{3.14}$$

$$i_{Lb}(t - t_4) = I_{o(avg)} + I_{Lr} \tag{3.15}$$

Where, $\omega_z = \frac{1}{\sqrt{(L_r + L_b)C_b}}$, $Z_z = \sqrt{\frac{(L_r + L_b)}{C_b}}$

$$t_{45} = \frac{1}{\omega_z} \tan^{-1} \frac{V_{in}}{I_{o(avg)} Z_z} \tag{3.16}$$

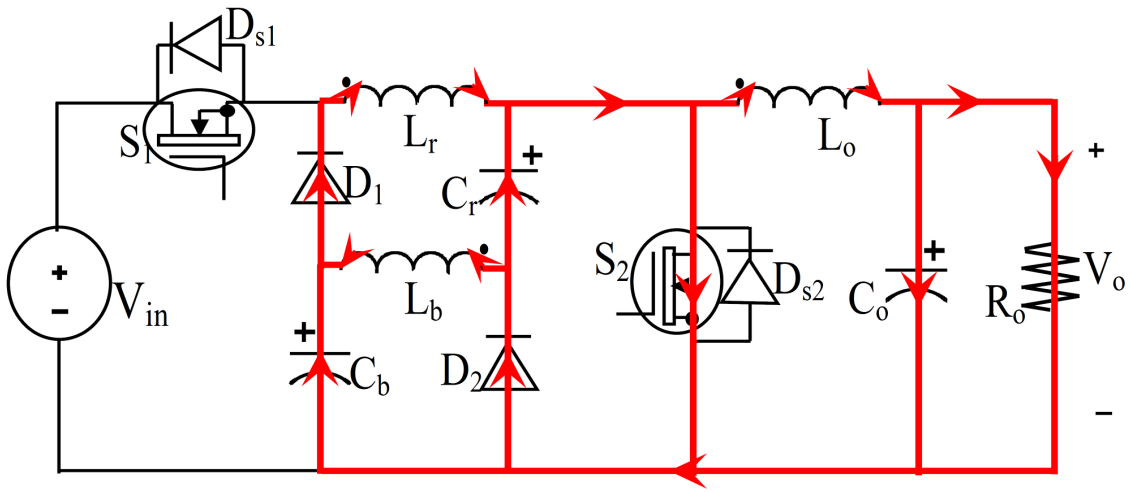


Fig. 3.3 (e): Modes of operation: Mode 5 (t_4 — t_5)

Mode 6 (t_5 — t_6): In this stage, at $t = t_5, i_{S1} = 0, i_{Lr} = I_{o(avg)}$, $V_{cr} = 0$ *and* $V_{cb} = 0$ are the initial conditions for this mode. As i_{Lr} reaches $I_{o(avg)}$, the switch gets turned OFF under ZCT. The preserved energy of L_r and C_r is transferred to the load.

$$V_{cr}(t - t_5) = -\frac{I_o}{C_r}(t - t_5) \tag{3.17}$$

$$i_{Lr}(t - t_5) = -\frac{V_o}{L_r}(t - t_5) + I_{o(avg)} \tag{3.18}$$

In this mode, $i_{Lr} = i_{Lb}$

This mode ends when the body diode of S_2 gets reverse biased and ceases the current through it. The current i_{Lr} reaches minimum value and thereby S_1 gets ON, and repetition of operation continues.

$$t_{56} = \frac{I_{o(avg)} L_r}{V_o} \tag{3.19}$$

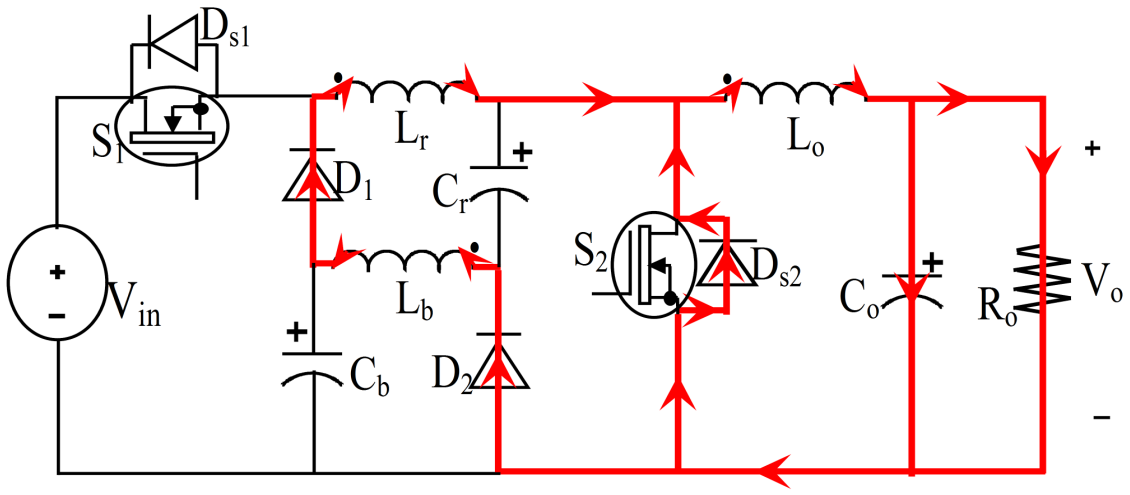


Fig. 3.3 (f): Modes of operation: Mode 6 (t_5 — t_6)

3.4 Output voltage

The output voltage can be evaluated by balancing the volt-Second relationship or by equating the energy relation i.e.,

$$V_o\tau = V_{in}[\frac{1}{2}t_{01} + t_{12} + t_{23} + t_{34} + t_{45} + t_{56}]$$

$$V_o\tau = V_{in}\left(\frac{1}{2}\frac{I_{o(avg)}L_r}{V_{in}} + \frac{1}{\omega_x}sin^{-1}\left(\frac{C_r}{C_e} - 1\right) + \frac{1}{\omega_y}tan^{-1}\left(\frac{I_{Lr(max)} - I_{o(avg)}}{V_{cr\,max}}\right)\right.$$
$$\left. + \frac{1}{\omega_z}tan^{-1}\left(\frac{V_{cr\,max}}{I_{o(avg)}Z_z}\right) + \frac{1}{2}\frac{I_{o(avg)}L_r}{V_o}\right) \quad (3.20)$$

The t_{01} and t_{56} of modes 1 and 6 contains least values compared to other terms in the preceding expression, so they are neglected for making analysis simple.

The voltage conversion ratio will be.

$$\frac{V_o}{V_{in}} = \frac{1}{\tau}\left(\frac{1}{\omega_x}sin^{-1}\left(\frac{C_r}{C_e} - 1\right) + \frac{1}{\omega_y}tan^{-1}\left(\frac{I_{Lr(max)} - I_{o(avg)}}{V_{cr\,max}}\right) + \frac{1}{\omega_z}tan^{-1}\left(\frac{V_{cr\,max}}{I_{o(avg)}Z_z}\right)\right) \quad (3.21)$$

Where $\tau = \frac{1}{f_s}$ and f_s=Switching frequency

From the aforementioned expression, it is evident that voltage conversion ratio relies upon switching frequency irrespective of the duty ratio.

3.5 Design Procedure

The traditional PWM converter's design is well-known and extensively presented in the literatures. Now, it is time to focus on eloquent aspects of designing the auxiliary circuits. The resonant inductor and capacitor design is the most significant part of designing the auxiliary circuit. The auxiliary resonant circuit which is proposed entrusts soft switching condition of the main switch. The design method is developed, by referring previous literatures [18].

3.5.1 Resonant Inductor L_r

Resonant inductor L_r is chosen to allow maximum output current within t_{rise} during the ON time of the main switch.

In this case from equation (3.1)

$$\frac{V_{in}}{L_r} t_{rise} \le I_{o\,max} \tag{3.22}$$

$t_{rise} \rightarrow$ Rise time of the main switch

The aforementioned equations assist the main switch with ZCS turn-ON, and ZVS turn-OFF of the synchronous switch body diode.

3.5.2 Buffer Inductor L_b

Inductor L_b is selected to allow maximum inductor current i_{Lb} within t_{rise} during the ON time of the synchronous switch i.e., $\frac{V_{cb}}{L_b} t_{rise} \le I_{Lb\,max}$; $V_{cb} \cong V_{in}$; $\frac{V_{in}}{L_b} t_{rise} \le I_{Lb\,max}$ (3.23)

$t_{rise} \rightarrow$ Rise time of the inductor L_b current.

3.5.3 Snubber Capacitor C_b

Snubber capacitor C_b is procured such that it discharges from V_{in} to zero with maximum current through it in the time period at the turn-OFF time of the main switch.

In this case, according to (3.14) and (3.16)

$$\frac{1}{I_{o\,max} Z_z} V_{in} \geq t_{fall} \tag{3.24}$$

Where $Z_z = \sqrt{\frac{L_r + L_b}{C_b}}$

3.5.4 Resonant Capacitor C_r

Buffer capacitor C_r is selected such that it charges from zero to the value assumed as half of the input voltage. During the turn-OFF time, the buffer capacitor is feeded by the energies that are preserved in the snubber inductor and the accumulated charge on snubber capacitor. The energy balance can be given as:

$$\frac{1}{2} C_b V_{in}^2 + \frac{1}{2} C_r V_{crm}^2 = \frac{1}{2} L_r I_{o\,max}^2 \tag{3.25}$$

The rate of charging of the capacitor C_b is greater than the fall time of the main switch S_1, which is equal to the increase in the rate of change of current through the inductor L_r.

$$\frac{C_r V_{in}}{I_{Lr\,max} - I_{o(avg)}} \geq t_{12} \tag{3.26}$$

From equation (3.7), t_{12} can be derived as,

$$t_{12} = \frac{1}{\omega_x} sin^{-1}\left(\frac{C_b}{C_e} - 1\right) \tag{3.27}$$

Solving the above two equations, C_r is derived as.

$$sin\left(\frac{\omega_x C_r V_{in}}{I_{Lr\,max} - I_{o(avg)}}\right) \geq \frac{C_b}{C_r} \tag{3.28}$$

From the aforementioned equations, it is clear that C_r is greater than C_b.

3.6 Simulation and Experimental Results

The Proposed converter functions with an input voltage V_{in}=12V, an output voltage V_o=4V, a load current of 15A and a switching frequency of 100 kHz. The functional characteristics of the proposed ZVT-ZCT SBC are executed by the simulation using PSIM 7.1 software co-simulated with MATLAB/SIMULINK. Fig. 3.4(a)—(e) shows the simulation results of the proposed converter. In Fig. 3.4 (a) the voltages of main switch S_1 and synchronous switch S_2 has an overshoot value of 0.5V compared to the traditional buck

converter which is a minor increase in terms of performance point of view. The waveforms which are shown depicts a time period of four switching cycles, which is 40µs in this particular case.

The synchronous buck converter integrated with the proposed passive auxiliary circuit has been built and substantiated with experimental results. However, there is a slight increase of voltage about 0.5V of main switch S_1 and synchronous switch S_2 as compared to the traditional buck converter. The experimental components employed in the proposed ZVT-ZCT SBC converter are tabulated in Table 1. The fig. 3.5 shows the hardware setup of the proposed ZVT-ZCT PWM SBC.

The fig. 3.6 (a) and fig. 3.6 (b) shows the voltage and current waveforms of main switch S_1 and synchronous switch S_2 depicting low stresses. The fig. 3.6 (c) shows the experimental voltage waveforms of capacitors C_r, C_b. The fig. 3.6 (d) shows the experimental current waveforms of L_b and diode D_2. Fig. 3.6 (e) presents the experimental current waveforms of inductor L_r.

TABLE 3.1

COMPONENTS USED FOR PROPOSED CONVERTER

Component	Value/Model
Main switch S_1	IRLR8721PbF
Synchronous Switch S_2	IRLR8721PbF
Schottky diode, D_1	MBRB4030
Schottky diode, D_2	MBRB4030
Resonant Inductor, L_r	100nH
Buffer Inductor, L_b	22nH
Resonant Capacitor, C_r	10nF
Buffer Capacitor, C_b	4.7nF
Output Inductor, L_o	15µH
Output Capacitor, C_o	15µF

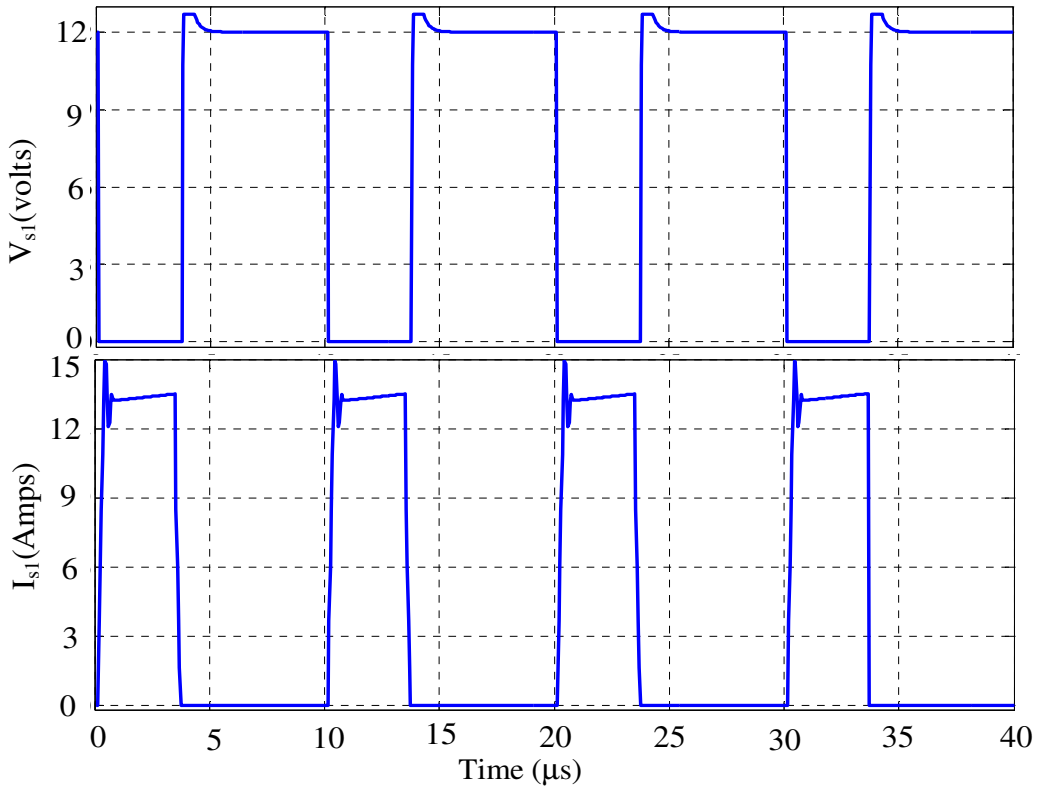


Fig. 3.4 (a): Simulated voltage and current waveforms of main switch S_1: V_{s1} in Volts and I_{s1} in Amps.

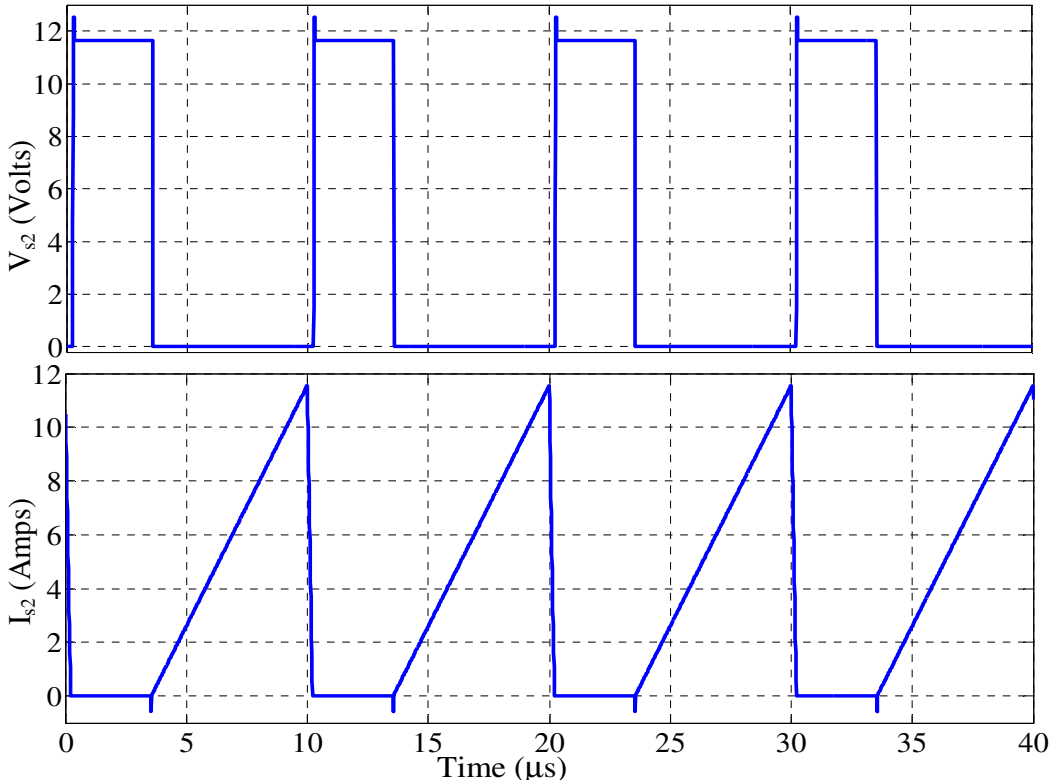


Fig. 3.4 (b): Simulated voltage and current waveforms of synchronous switch S_2: V_{s2} in Volts and I_{s2} in Amps.

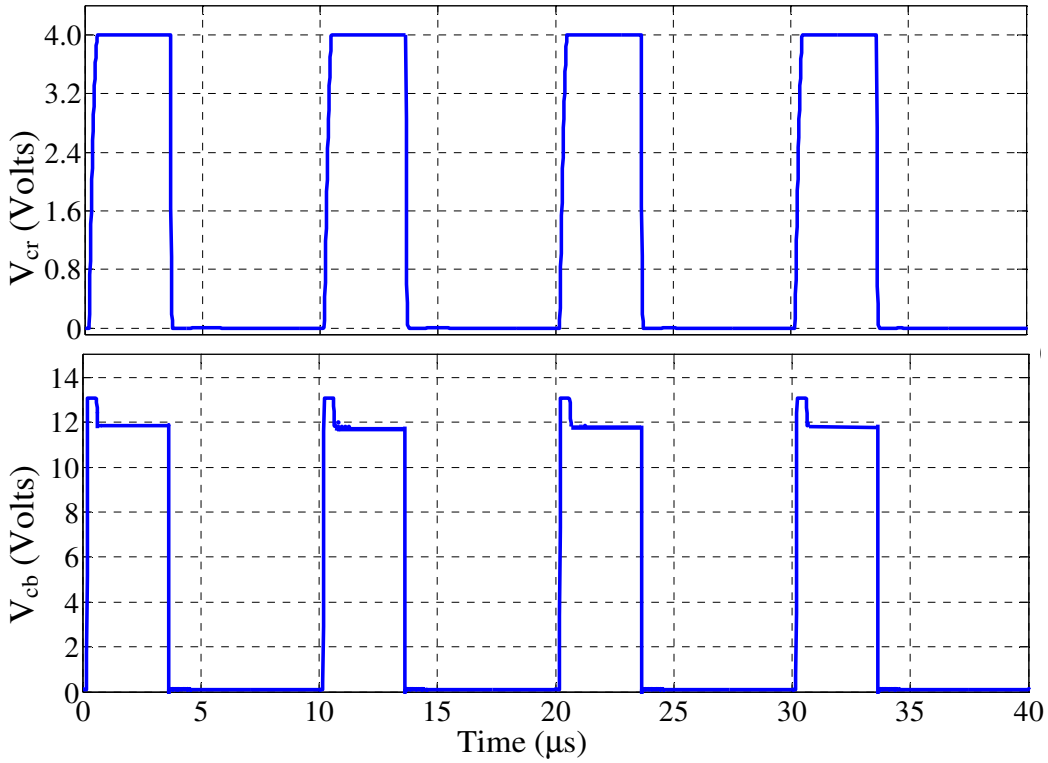


Fig. 3.4 (c): Simulated voltage waveforms of resonant capacitor and snubber capacitor C_r and C_b: V_{cr} and V_{cb} in Volts.

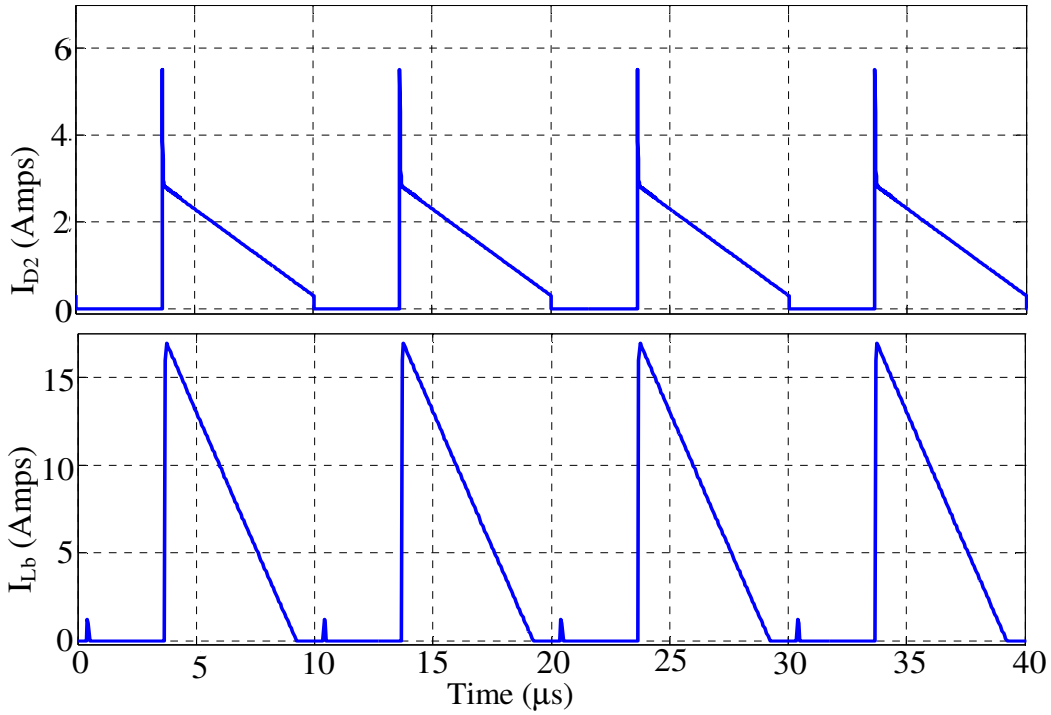


Fig. 3.4 (d): Simulated current waveforms of Diode D_2 and inductor L_b: I_{D2} and I_{Lb} in Amps.

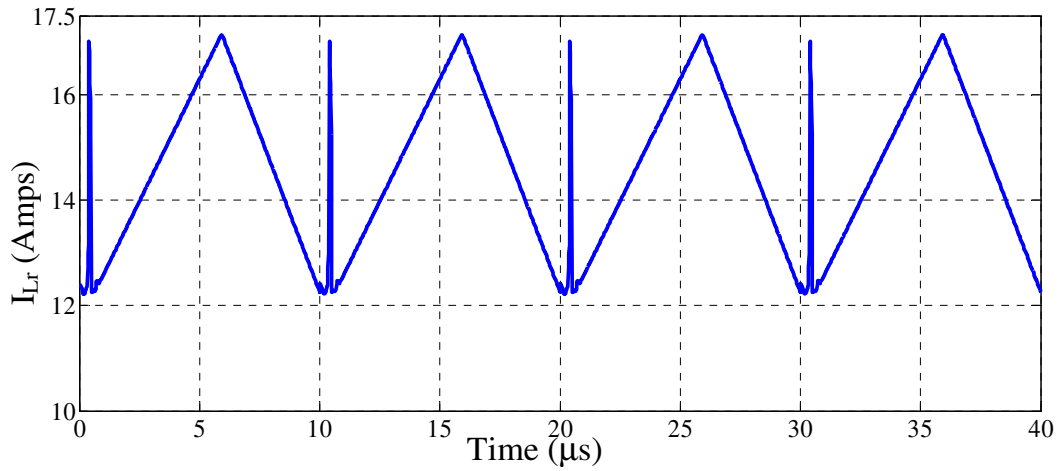


Fig. 3.4 (e): Simulated current waveform of resonant inductor L_r: I_{Lr} in Amps.

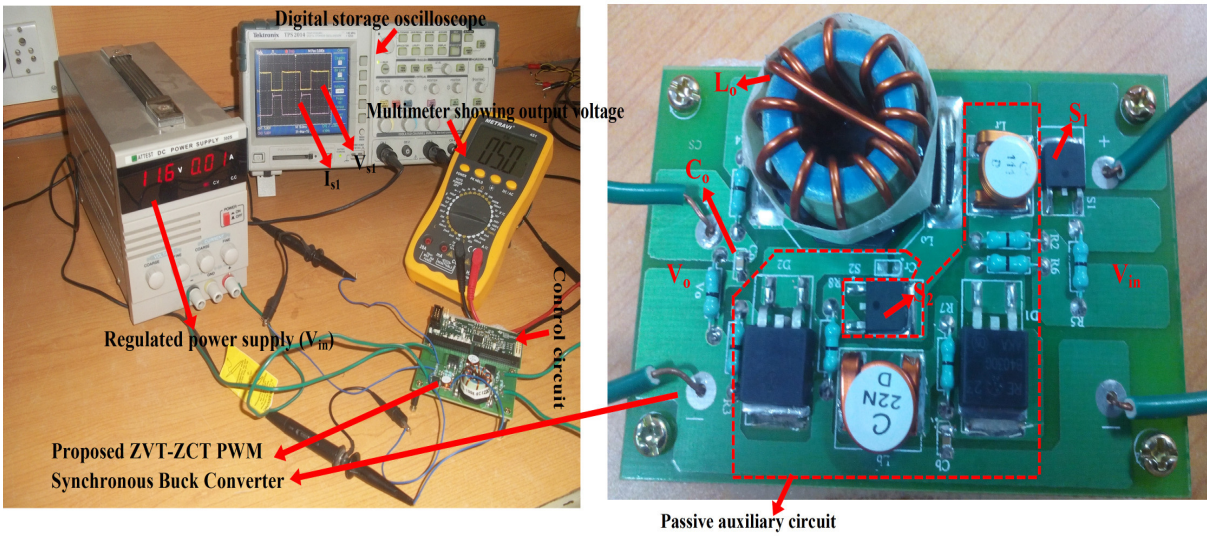


Fig. 3.5: Experimental setup of Proposed ZVT-ZCT PWM synchronous Buck Converter

The fig. 3.7 (a) signifies that the main switch S_1 spike current is plummeted; the waveform is almost equivalent to the traditional buck converter. Consequently, the rating of the main switch required for the buck converter is economized by the introduction of ZVT-ZCT operation. The main switch is turned ON under ZCT and turned OFF with ZVT, due to which the mainstream switching losses got diminished. Fig. 3.7 (b) the synchronous switch S_2 is turned OFF under ZVT and turned ON with ZCT operation. The reverse recovery (RR) effect due to the body diode of S_2 is almost attenuated.

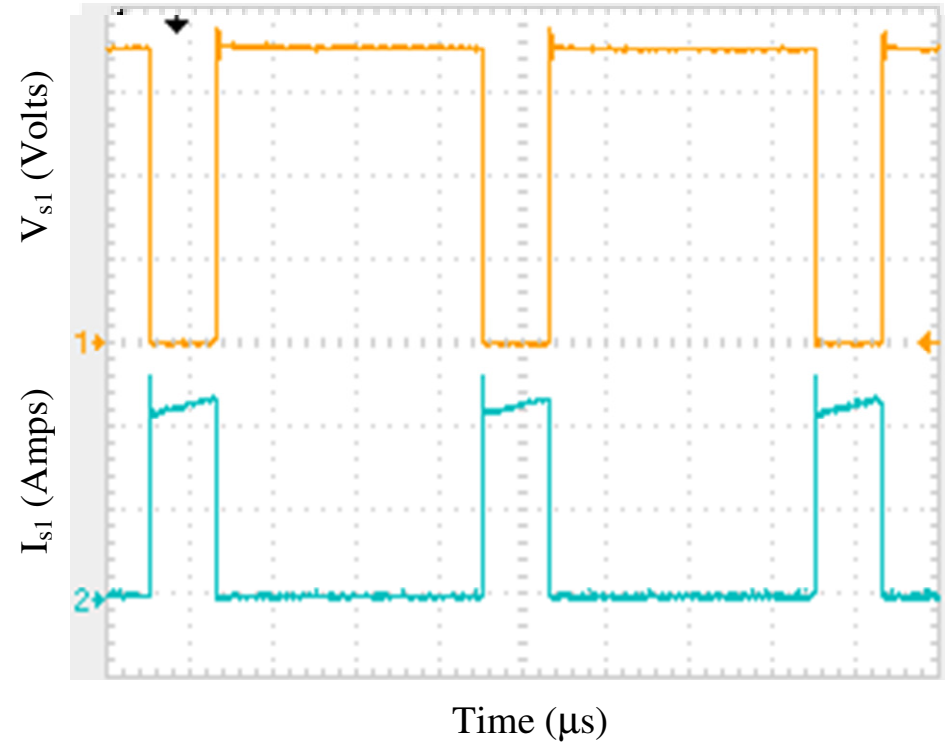


Fig. 3.6 (a): Experimental voltage and current waveform of Main switch S_1: [Vs_1: 3.42V/Div; Is_1: 6A/Div; time: 2.5µs/Div]

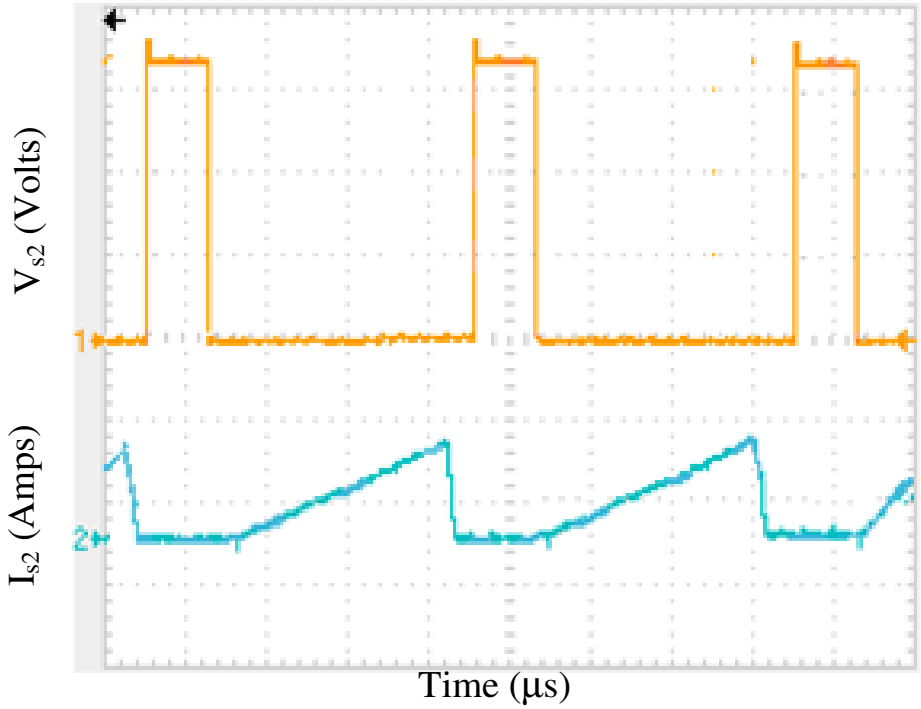


Fig. 3.6 (b): Experimental voltage and current waveform of synchronous switch S_2: [Vs_2: 3.42V/Div; Is_2: 8A/Div; time: 2.5µs/Div]

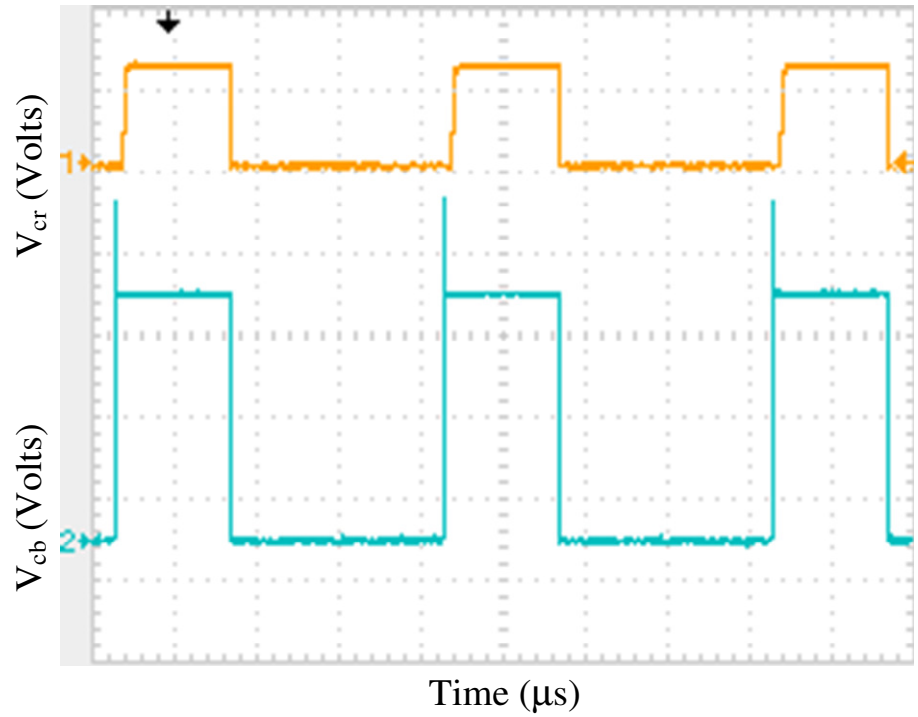


Fig. 3.6 (c): Experimental voltage waveforms of resonant capacitor C_r and buffer capacitor C_b S_3: [V_{cr}: 3V/Div; V_{cb}: 4V/Div; time: 2.5µs/Div]

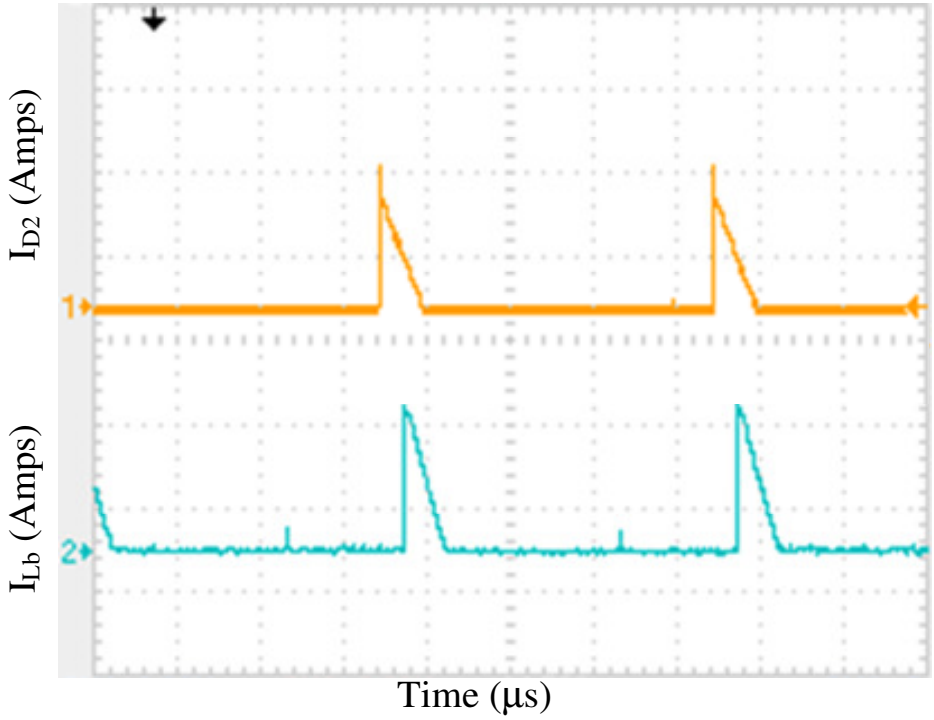


Fig. 3.6 (d): Experimental current waveforms of diode D_2 and inductor L_b: [I_{Lb}: 10A/Div; I_{D2}: 3.5A/Div; time: 2.5us/Div]

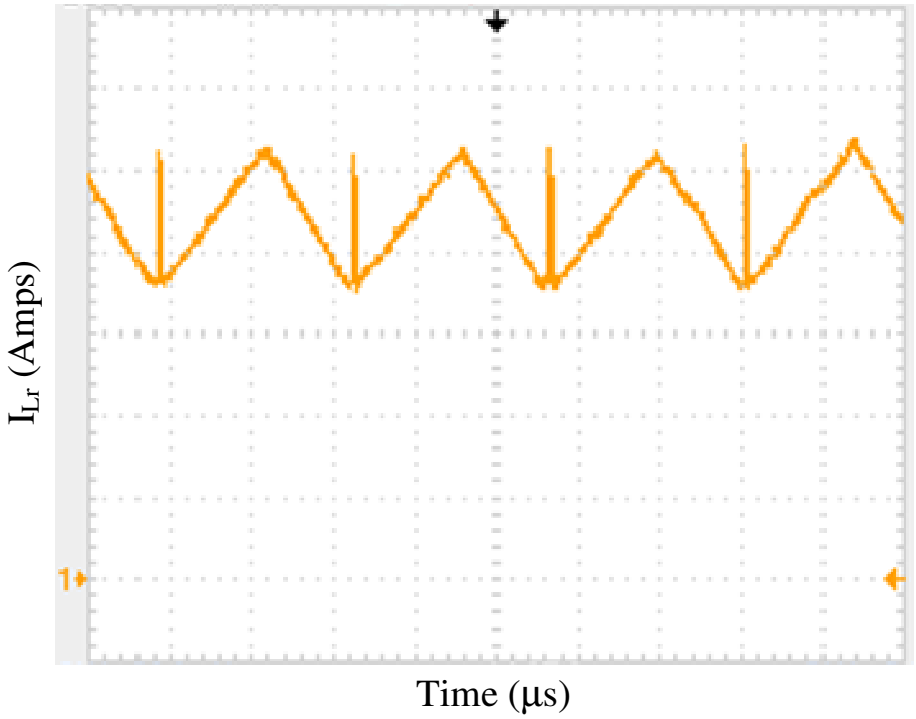


Fig. 3.6 (e): Experimental current waveform of resonant inductor L_r: [I_{Lr}: 3.5A/Div; time: 2.5us/Div]

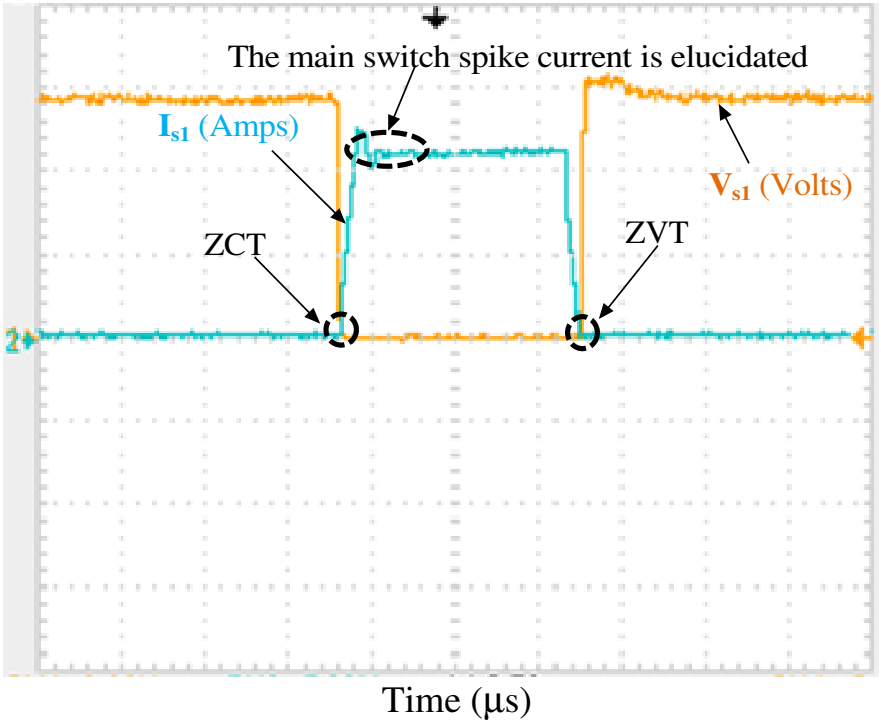


Fig. 3.7 (a): Experimental voltage and current waveforms of main switch S_1 exhibits soft switching conditions [Vs_1:3.42V/Div; Is_1: 6A/Div; time: 0. 1µs/Div].

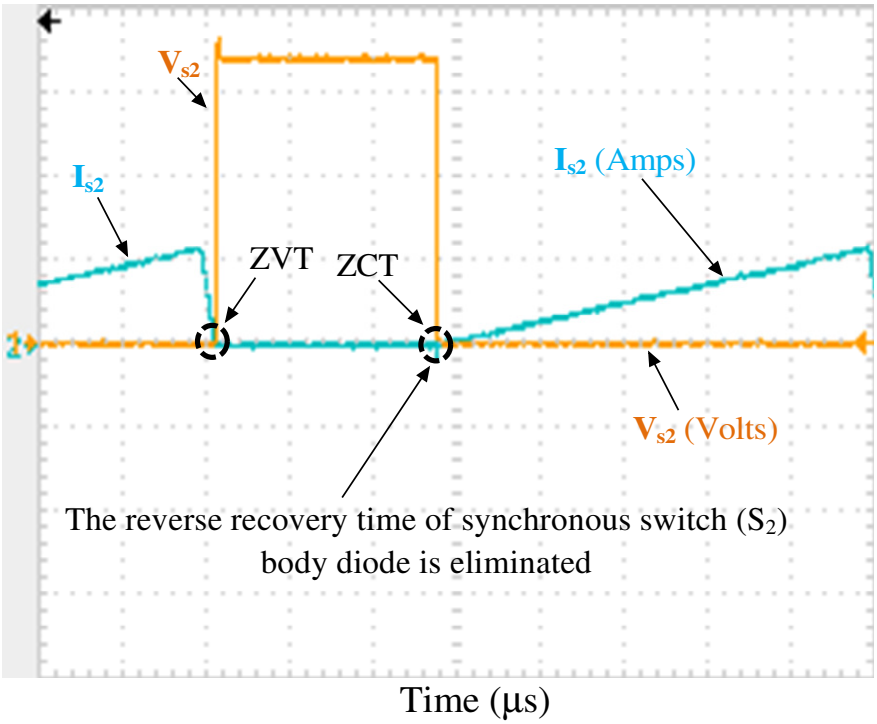


Fig. 3.7 (b): Experimental voltage and current waveforms of synchronous switch S_2 exhibits soft switching conditions [Vs_2: 3.42V/Div; Is_2: 10A/Div; time: 0.1µs/Div].

3.7 Efficiency curve

From fig. 3.8, it can be seen that efficiency values of the proposed converter are comparatively higher than the traditional converter with SR. At nearly 60% of output power, the efficiency of the proposed converter rises to about 98% when compared to the counterpart traditional converter whose efficiency is about 87%. The high efficiency of the proposed converter proves the definiteness of the design values.

3.7.1 Contrast with contemporary topologies

Table 3.2 shows the comparison of recent topological circuits having close operating conditions with the proposed circuit. As shown in the Table 3.2, the circuits are soft switching PWM topologies [116, 189] that are prominent in curtailing the spike of the main switch and diminishing the reverse recovery (RR) problem of the synchronous switch body diode. The RR problem of main diode is eliminated. In [116] the coupled inductor is used in the auxiliary circuit to achieve soft switching of the switches and solve the RR problem. The coupled inductor used in [116] auxiliary circuit, suffers from the limitations of requiring larger volume, complication in design and manufacture, an increment in the ripple of the

output current. In [189], the active auxiliary circuit is used which results in complex control and more expensive than the passive auxiliary circuit.

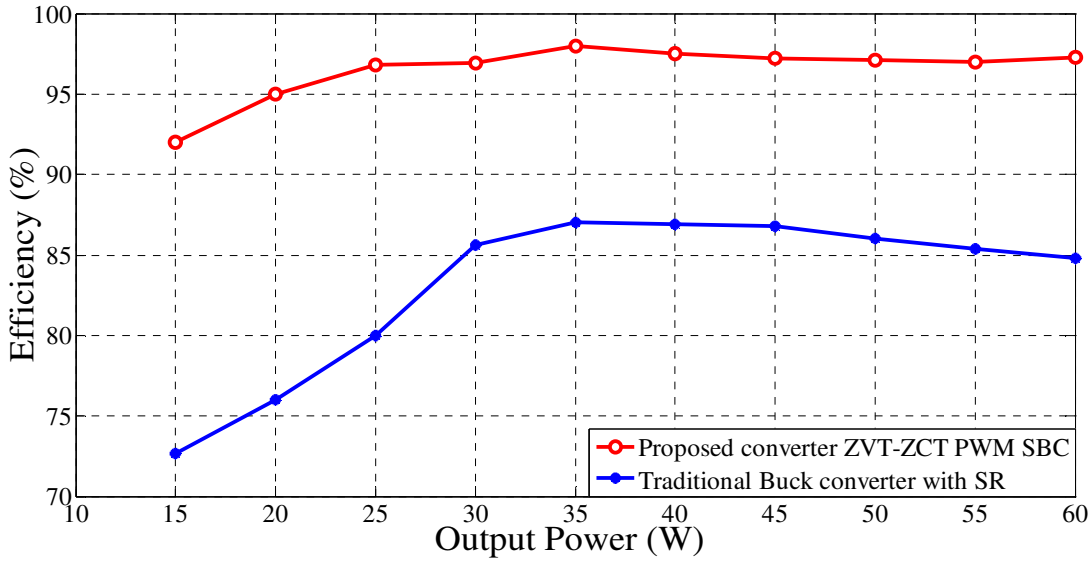


Fig. 3.8: Efficiency curve of proposed converter in comparison with traditional buck converter

The proposed auxiliary circuit not only exceeds the advantages of the contemporary circuits, but also obliges both switches to operate under soft switching conditions. The RR problem compared to conventional circuits is largely enhanced, besides the efficiency is improved at maximum. Efficiency enhancement relative to the contemporary topologies is shown in fig. 3.11. The Table 3.2 and the results claim that the proposed auxiliary circuit has achieved a comparable efficiency enhancement over the hard switching circuit to a decent value with a simple design and is easy to control.

3.7.2 Overview of the contemporary topologies [116] and [189]

S. Urgun [116] has proposed a new ZVT-ZCT quasi-resonant buck converter, which ensures soft switching at the zero crossings that provides ZVT turn-ON and ZCT turn-OFF together for the main switch of active snubber cell presented in [116]. The circuit combines most of the advantages similar to the previous published works such as the semiconductor devices used operate under soft switching conditions. The soft switching operation of the new converter is maintained for the whole line and load ranges. The circuit scheme of [116] is shown in the fig 2.9. The active snubber cell consists of a centre tapped and a magnetically coupled snubber inductor (L_{s1} and L_{s2}), snubber capacitor (C_s), a main switch (T_1), an auxiliary switch (T_2), the output filter capacitor (C_F), main inductor (L_F) and two auxiliary diodes D_1 and D_2. C_r is considered to be a parasitic capacitor. The circuit is designed for

200W and 100 kHz frequency. From fig 2.11 it can be seen that at full load the overall efficiency is 96%.

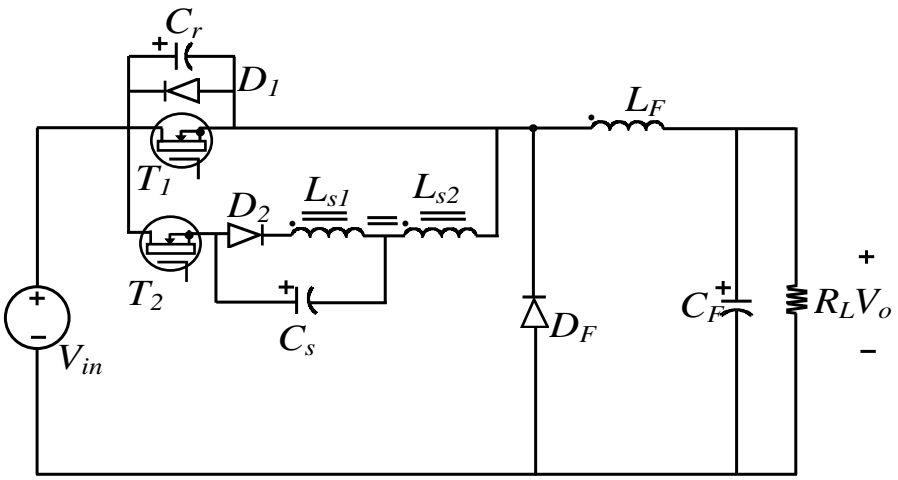


Fig. 3.9: Circuit diagram of the topology proposed by S. Urgun [116]

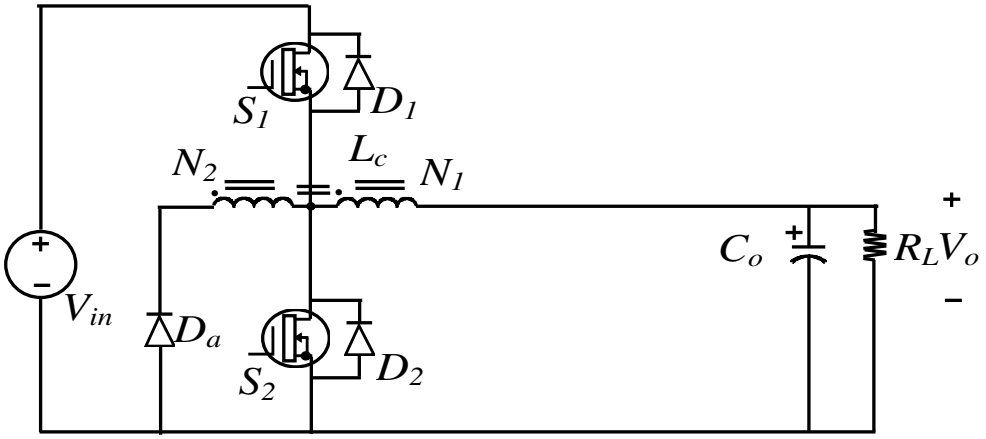


Fig. 3.10: Circuit diagram of the topology proposed by Hyun Lark Do [189]

Hyun Lark Do [189] proposed a zero voltage switching synchronous buck converter with a coupled inductor. An auxiliary circuit incorporated in the conventional synchronous buck converter allows power switches to operate with ZVS. Moreover, the reverse recovery problem associated with the body diode of the synchronous switch is solved. Fig 3.10 shows the circuit diagram of the topology proposed by Hyun Lark Do [189]. The circuit consists of a coupled inductor $L_{c,}$ switches S_1 and S_2, filter capacitor C_o and a diode D_a, the main and auxiliary switches consists of body diodes D_1 and D_2. The circuit is designed for 115W and 100 kHz frequency. The ZVS synchronous buck converter exhibits 93% at full load condition.

TABLE 3.2

CONTRAST WITH CONTEMPORARY TOPOLOGIES

	Converter proposed by Hyun Lark -Do [189]		Converter proposed by Hong Tzer Yang [117]		Proposed ZVT-ZCT PWM SBC converter	
Clamping method	Passive		Active		Passive	
Switching method	Turn ON	Turn OFF	Turn ON	Turn OFF	Turn ON	Turn OFF
	ZVS	Hard-Switching	ZVS	Hard-Switching	ZCS	ZVS
Stresses on main switch (spike current, spike voltage)	Low		Low		Very low	
Stresses on synchronous switch (spike current, spike voltage)	Low		Low		Eliminated	
Reverse recovery of main diode	Not negligible		Replaced by SR		Replaced by SR	
Reverse recovery of SR diode	Not negligible		Eliminated		Eliminated	
Overhead of auxiliary circuit						
1. Capacitor	2		1		2	
2. Inductor	2		2		2	
3. Diode	1		3		2	
4. Coupled Inductor	1		0		0	
5. Switch	0		1		0	
Maximum Efficiency Values at 70% of output power	92.5		94		98	
Maximum Efficiency improvement over hard switching circuit	4.5		6		10	

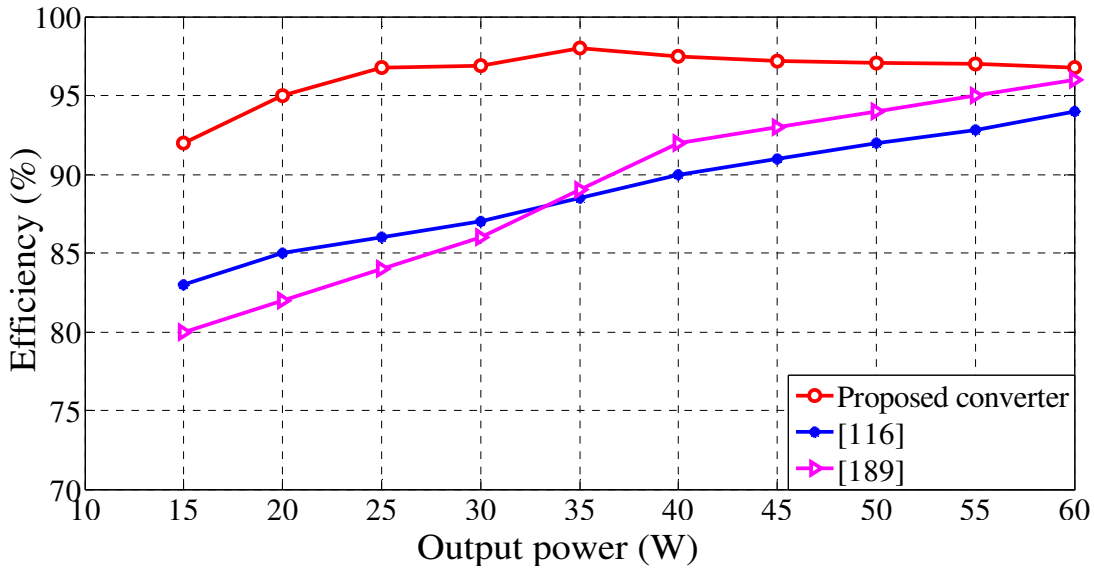


Fig. 3.11: Efficiency curve of proposed converter in contrast with contemporary topologies.

3.8 Summary

The switching and conduction losses in the SBC were minimized by incorporating the concept of ZVT-ZCT. Apart from the main switch which is turned OFF under ZVT and ON under ZCT, the same replicated on the synchronous switch which is also turned ON under ZCT and OFF under ZVT. The energy stored in the snubber is utilized to the load without using the path of the main switch which reduces the conduction loss. The SBC with active auxiliary circuit suffers with this additional conduction loss. The proposed auxiliary circuit integrated with SBC can also be applied to other contemporary circuits; it is proved that the proposed auxiliary circuit achieves ZVT-turn OFF and ZCT-turn ON to both the switches. Particularly, the RR effect of synchronous switch is diminished through the proposed auxiliary circuit, which in turn minimizes the switching losses as correlated with contemporary topologies. Therefore, the switching and conduction losses are diminished; the newly proposed ZVT-ZCT SBC is the most suitable converter for medium and high current applications than the traditional converter, as it has been observed from the efficiency curve and also contrasted with the contemporary topologies. In addition to this, current and voltage stresses on the main power circuit are reduced immensely, and the auxiliary elements designed such that they deal with permissible voltage and current values. Furthermore, the proposed converter structure is simple, low-cost and easily controllable.

Chapter 4

A NEW MULTIPHASE SYNCHRONOUS BUCK CONVERTER INTEGRATED WITH ACTIVE AUXILIARY CIRCUIT FOR PORTABLE APPLICATIONS

CHAPTER 4: A NEW MULTIPHASE SYNCHRONOUS BUCK CONVERTER INTEGRATED WITH ACTIVE AUXILIARY CIRCUIT FOR PORTABLE APPLICATIONS

4.1 Introduction

Chapters 2 and 3 explain the incorporation of the ZVZCT concept to the SBC, which facilitates the reduction of switching losses and also maintains the switching stresses under a tolerable limit. The ZVT-ZCT concept extending to multiphase SBC has emerged as a leading candidate for meeting the power requirement of the portable electronic systems. High current multiphase buck converters (MBC) are used in computing, graphics, and telecom applications. To achieve high power-density converters and high-performance, the switching frequency of the converters need to be increased. The traditional hard-switching pulse-width-modulation (PWM) converters operating at high frequency is limited because of substantial switching loss. A number of soft switching technologies have been proposed to reduce switching losses and most of the new soft switching converters reduce switching losses only at the expense of much-increased voltage/current stresses of the switches, which increases the conduction losses. Another way to achieve high-performance and high power density converters is adopting the multiphase conversion technique [51-61, 158–159]. With the interleaved operation, small size inductors can be used to keep low current ripple at the input and output capacitor filters, and high dynamic performance can be achieved since the operating frequency of input and output filter capacitors are increased by n times for n-phase converters. Higher dynamic performance and higher power-density power conversion can be achieved if both ZVT-ZCT and multiphase conversion techniques are combined.

With a duty cycle of less than 10 %, raising the switching frequency to multi-MHz level will reduce the efficiency to less than 80 % [66-80]. Because the switching frequency is equal to the inductor current ripple frequency, the switching frequency is limited between 300 kHz to 500 kHz [160-165]. When the inductor current slew rate increases by a smaller inductance value to improve the transient response, then the inductor current ripple also increases. It is not only a harmful action of the high-side switch due to larger turn-off loss, but also for the low-side switch due to a larger conduction loss. It also increases the inductor winding losses. This conflict limits the average inductor current in each channel [166-171]. Moreover, there is a tradeoff between efficiency and transient response. As a result, these technical conflicts not only increase the cost and sacrifice the power density, but also it is difficult to meet the

power requirements of future microprocessors before the technical conflicts are resolved [113, 146-147, 171-173]. Therefore, there is a need to increase the efficiency of the multiphase buck converter at a high operating frequency by reducing switching losses. In ZVT converters [116-117, 148,174] generally the auxiliary switch actuates just before the main switch is made active and culminates after it is executed. The converters proposed [175-184] either provide ZVT or ZCT soft switching condition, making some switches in the converter to operate with hard-switching that increases switching loss which affects the overall performance of the converter. Reducing the switching losses for a low voltage, high current application with the assistance of a simple active auxiliary circuit is not present in the literature [49-50, 113, 116-117, 146-147, and 152-184]. The industry standard voltage regulator (VR) topology used to deliver high current and low voltage is the multiphase synchronous buck converter [62-65].

In this chapter, the ZVT-ZCT multiphase synchronous buck converter is presented with the directive to improve its performance and alleviate the issues of the conventional multiphase synchronous buck converter. In contrast to the contemporary topologies the proposed novel topology resolves the issues of unbalance distribution of current, the high amount of losses in the converter, reduces the problem of EMI of the converter and operates with both soft switching conditions that enhances the performance of the converter. The proposed converter achieves ZVS and ZCS with the reduction in voltage and current stresses of the switches to improve the efficiency by minimizing the switching and conduction losses with a simple active auxiliary circuit. Here the proposed multiphase ZVT-ZCT PWM SBC is associated with active auxiliary circuit rather than passive auxiliary circuit because at the high load current passive auxiliary circuit will give high conduction losses.

This chapter is organised as follows: section 4.2 presents a description about the proposed topology. The principle of operation and its operating modes are explained in the section 4.3. Section 4.4 shows the derivation of the output voltage. Section 4.5 provides the design procedure of auxiliary circuit elements used. Section 4.6 explains the simulation and experimental results that exposes the features of the proposed converter. In section 4.7, efficiency curve is shown that explains the operation of the converter over wide range of load. Section 4.8 summarises the important features.

4.2 Topology description

The proposed multiphase converter is shown by Fig. 4.1. It is a combination of the proposed converter along with an active auxiliary circuit that facilitates reduction of

switching losses. The auxiliary circuit consists of inductor L_r, diode D_1, and MOSFET switches S_7, S_8, and S_9. The number of auxiliary MOSFET switches depends on the number of phases. Body diodes of main switches S_1, S_2, and S_3 are utilized to provide zero voltage switching.

In order to analyze the steady-state operations of the proposed circuit, the following assumptions are made during one switching cycle.

1. The input voltage V_{in} is constant.
2. The output voltage V_o is constant or the output capacitor C_o is large enough.
3. The filter Inductors L_1, L_2, L_3 are much larger than the resonant circuit inductor L_r.
4. The resonant circuits are ideal.
5. The reverse recovery time of the diode is ignored.

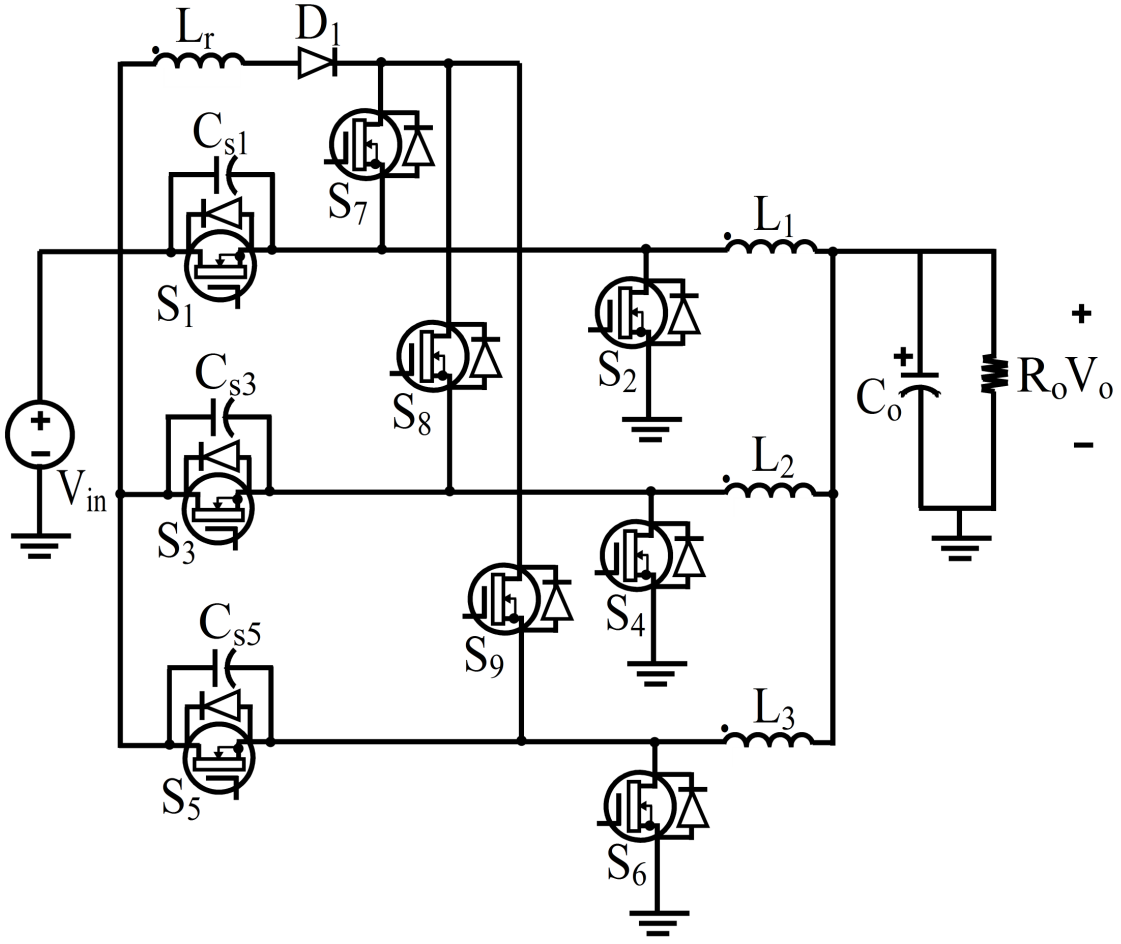


Fig.4.1: Proposed multiphase ZVT-ZCT PWM Synchronous buck converter with active auxiliary circuit

4.3 Operational modes

Based on these assumptions, circuit operations in one switching cycle can be divided into fifteen stages. The key waveforms of these stages are illustrated in Fig. 4.2 and the equivalent circuit schemes of the operation stages are given in Fig. 4.3. The detailed analysis of every stage is presented below:

Mode 1 (t_0 — t_1): Prior to t = t_0, the body diode of switch S_2 was conducting, while the main switch S_1 is off. The equations are $i_{S1} = 0$, $i_{D4} = I_0/3$, $i_{Lr} = 0$, are valid at the beginning of this stage.

At t = t_0, the auxiliary switch S_7 is turned on, which realizes zero-current turn-on as it is in series with the resonant inductor L_r. During this stage, i_{Lr} rises and current i_{Ds2} through the body diode of switch S_1 falls simultaneously at the same rate. The resonance occurs between L_r and C_{s1}.

This mode ends at t = t_1, when i_{Lr} reaches $I_0/3$, and i_{Ds2} becomes zero. The body diode of switch S_2 is turned off with ZCS.

The resonant current through inductor L_r is given by:

$$\frac{di^2_{resonant}(t)}{dt^2} + \frac{i_{resonant}(t)}{L_r C_{s1}} = 0$$

Solving the above instantaneous voltage equation the solution yields:

$$i_{resonant}(t) = \frac{C_{S1} V_{CS1} \omega Sin\omega t}{Z_1} \tag{4.1}$$

$$i_{Lr}(t) = \frac{V_i}{L_r} \times t \tag{4.2}$$

Where $\omega = 1/\sqrt{L_r C_{S1}}$, $Z_1 = \sqrt{L_r / C_{S1}}$

At $t = t_1$, $i_{Lr}(t) = I_o/3$,

Therefore, $t_{01} = t_1 - t_0 = \frac{I_o L_r}{3V_{in}}$.

Mode 2 (t_1 — t_2): Since the inductor current i_{Lr} is increasing continuously beyond one third of load current, the exceeding current makes the diode D_{S1} to conduct. At t = t_1, $i_{S7} = i_{Lr} = I_0/3$. After reaching the peak current I_{Lrmax}, the inductor current starts decreasing. This mode comes to an end when i_{Lr} becomes again equal to $I_o/3$. At this moment, the main switch is triggered to turn ON under zero voltage switching (ZVS).

The discharge current of capacitor C_{S1} through the body diode having a resistance R is given as:

$$RC_{s1}\frac{dv_{C_{s1}}}{dt}+v_{Cs1}=0$$

Solving the above instantaneous voltage equation of capacitor C_{s1} the solution yields:

$$i_{C_{s1}}=\frac{V_{Cs1}}{R}e^{-t/RC_{S1}} \tag{4.3}$$

The inductor current i_{Lr} during this mode is given by:

$$L\frac{di_{Lr}(t)}{dt}+Ri_{Lr}(t)=0 \quad \begin{bmatrix} i_{Lr}(t=t_1)=\frac{I_o}{3} \\ i_{Lr}(t=t_2)=i_{Lr\,max} \end{bmatrix}$$

Solving the above equation for i_{Lr} the solution yields:

$$i_{Lr}(t)=\left(i_{Lr\,max}-\frac{I_o}{3}\right)e^{\frac{-tR}{L_r}} \tag{4.4}$$

At $t=t_1,\ i_{Lr}(t)=I_o/3$,

Therefore, $t_{12}=t_2-t_1=\frac{2L_r}{R}ln\frac{3I_{Lr\,max}}{I_0}$.

Mode 3 (t_2 — t_3): At t = t_2, the main switch is turned on while the auxiliary switch is still in the ON state. Now the stored energy in inductor L_r will be transferred to the load at the same rate as the current increase through the main switch S_1. At t = t_2, $i_{Lr} = I_0/3$.

This mode comes to end when the total energy of the resonant inductor will be transferred to the load. The auxiliary switch S_7 will turn off under ZCS.

The inductor current i_{Lr} during this mode can be expressed as:

$$L\frac{di_{Lr}(t)}{dt}+Ri_{Lr}(t)=0 \quad \begin{bmatrix} i_{Lr}(t=t_2)=i_{Lr\,max} \\ i_{Lr}(t=t_3)=0 \end{bmatrix}$$

Solving the above equation for i_{Lr} the solution yields:

$$i_{Lr}(t)=I_{Lr\max}e^{-tR_{dson}/L_r} \tag{4.5}$$

$$i_{S1}+i_{Lr}=I_0/3 \tag{4.6}$$

At the end of this mode, at t = t_3.

$$i_{S1}=I_o/3 \tag{4.7}$$

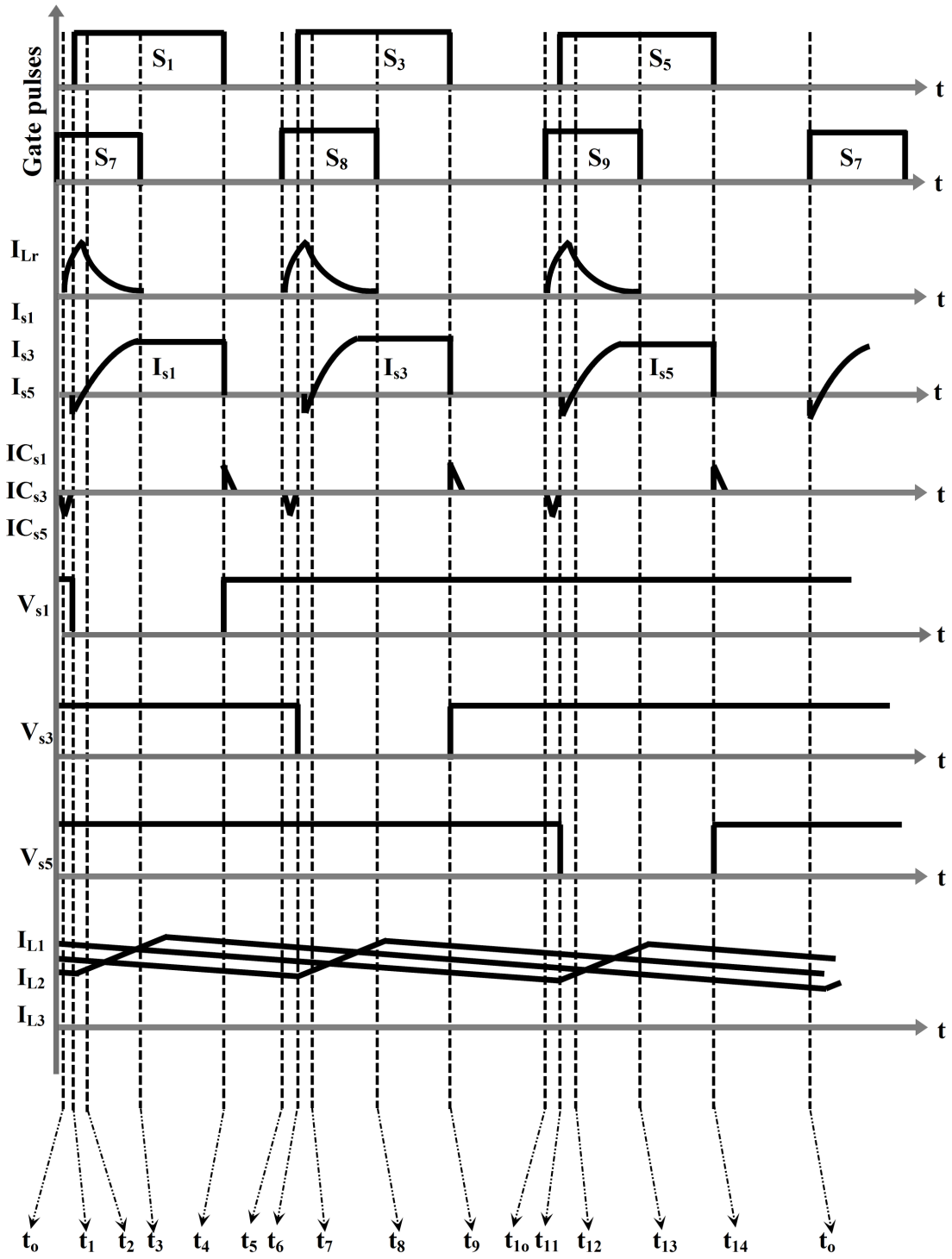


Fig. 4.2: Essential theoretical waveforms of proposed converter

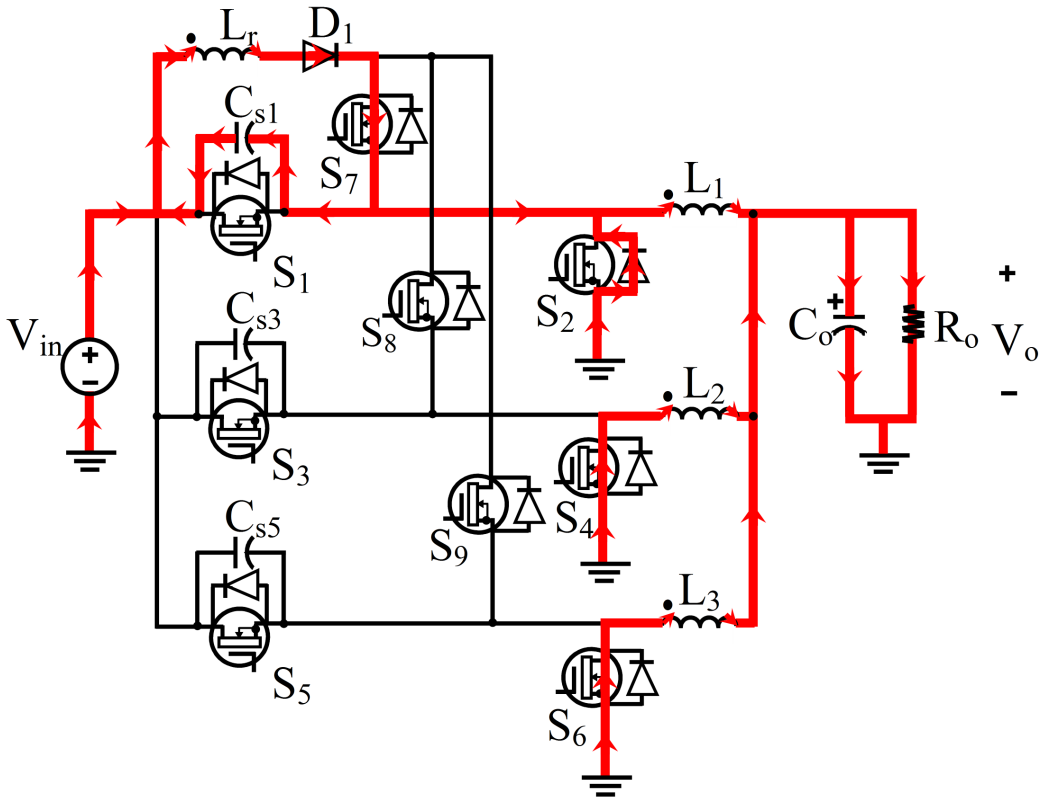


Fig. 4.3 (a): Modes of operation: Mode 1 (t_0 — t_1)

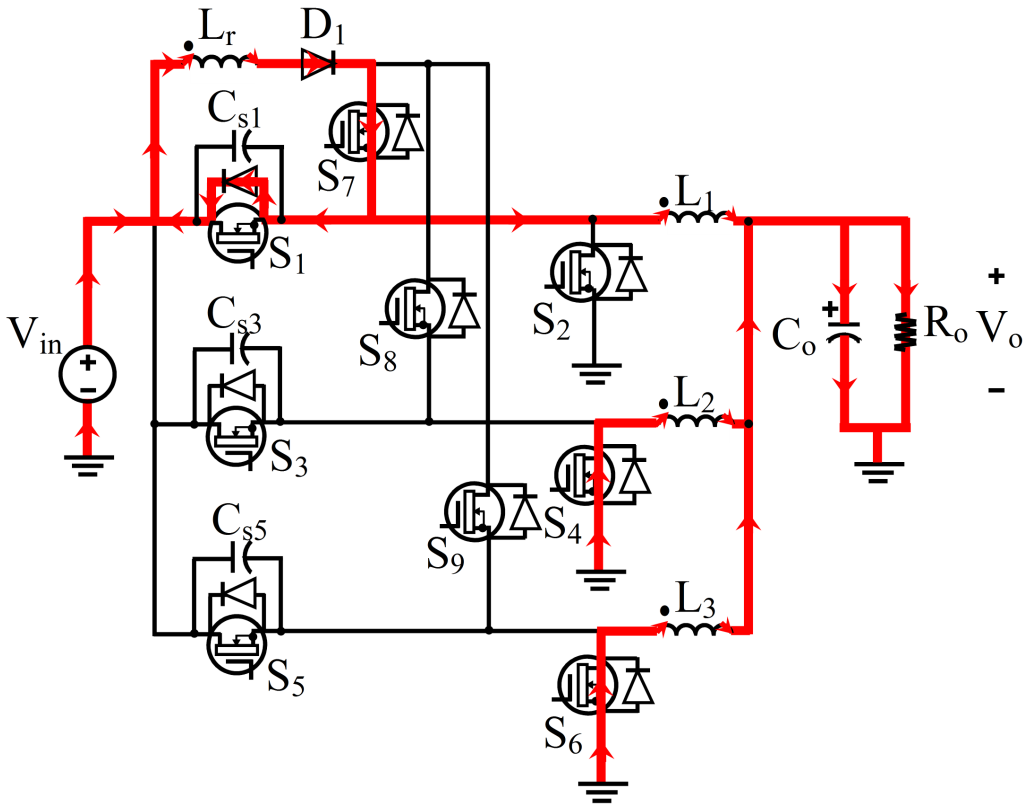


Fig. 4.3 (b): Modes of operation: Mode 2 (t_1 — t_2)

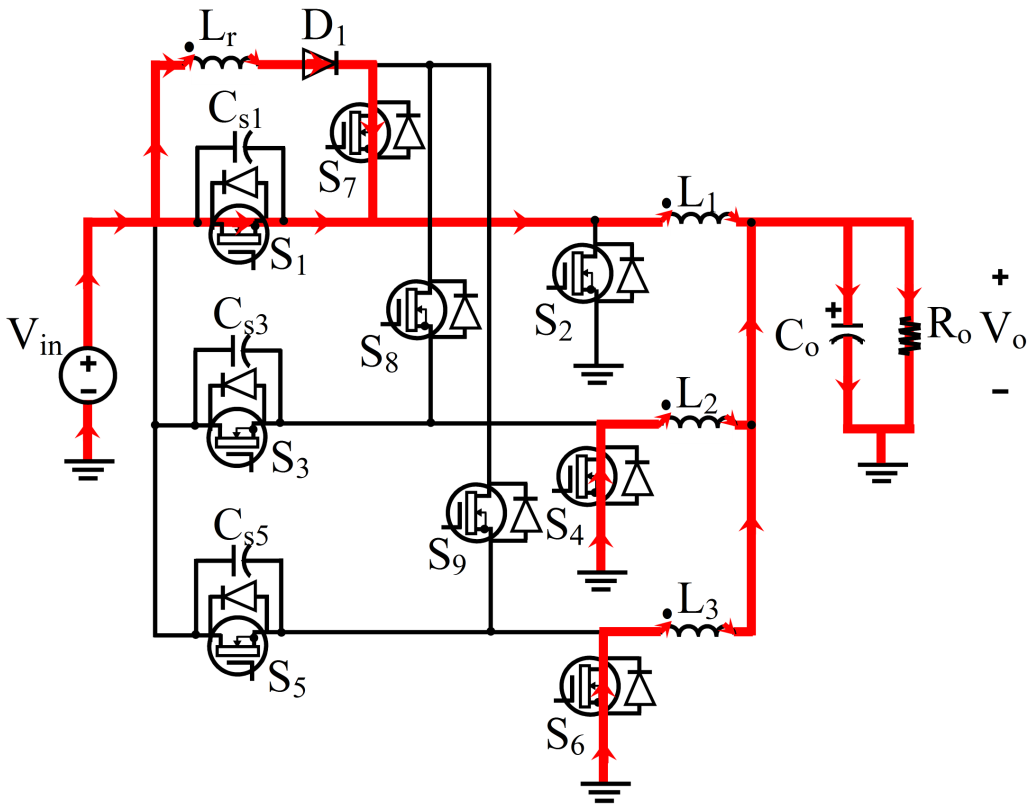


Fig. 4.3 (c): Modes of operation: Mode 3 (t_2 — t_3)

$$i_{Lr} = 0 \tag{4.8}$$

Therefore, $t_{23} = t_3 - t_2 = \frac{2L_r}{R_{dson}} ln \frac{3I_{Lrmax}}{I_0}$.

Mode 4 (t_3 — t_4): In this mode, the converter behaves as a conventional PWM converter. For the required output voltage, the turn on period of the main switch is decided. At the end of this mode, the main switch S_1 is turned off under ZCS due to the existence of capacitor C_{S1} across it. The current expression for this mode can be expressed as:

$$i_{S1} = I_0 / 3 \tag{4.9}$$

Mode 5 (t_4 — t_5): At t = t_4, the synchronous switch is turned on to provide a constant load current. At the end of this mode, the complete operation for one phase converter is completed and the second auxiliary switch S_8 is turned on with a phase difference of 360/n, where n is the number of phases, here n =3. The same five modes will be repeated for each phase. So there are fifteen modes for this proposed multiphase converter. The current expression for this mode can be expressed as:

$$i_{S2} = I_o / 3 \tag{4.10}$$

The current through capacitor v_{Cs1} is given by:

$$RC_{s1}\frac{dv_{C_{s1}}}{dt}+v_{Cs1}=0$$

Solving the above equation for v_{Cs1} the solution yields:

$$i_{C_{s1}}=\frac{V_{Cs1}}{R}e^{-t/RC_{S1}}$$

At the end of this mode, at t = t_5, $i_{Cs1}=0$

Therefore, $t_{45}=t_5-t_4=RC_{s1}\,ln\frac{V_{Cs1}}{RC_{s1}}$.

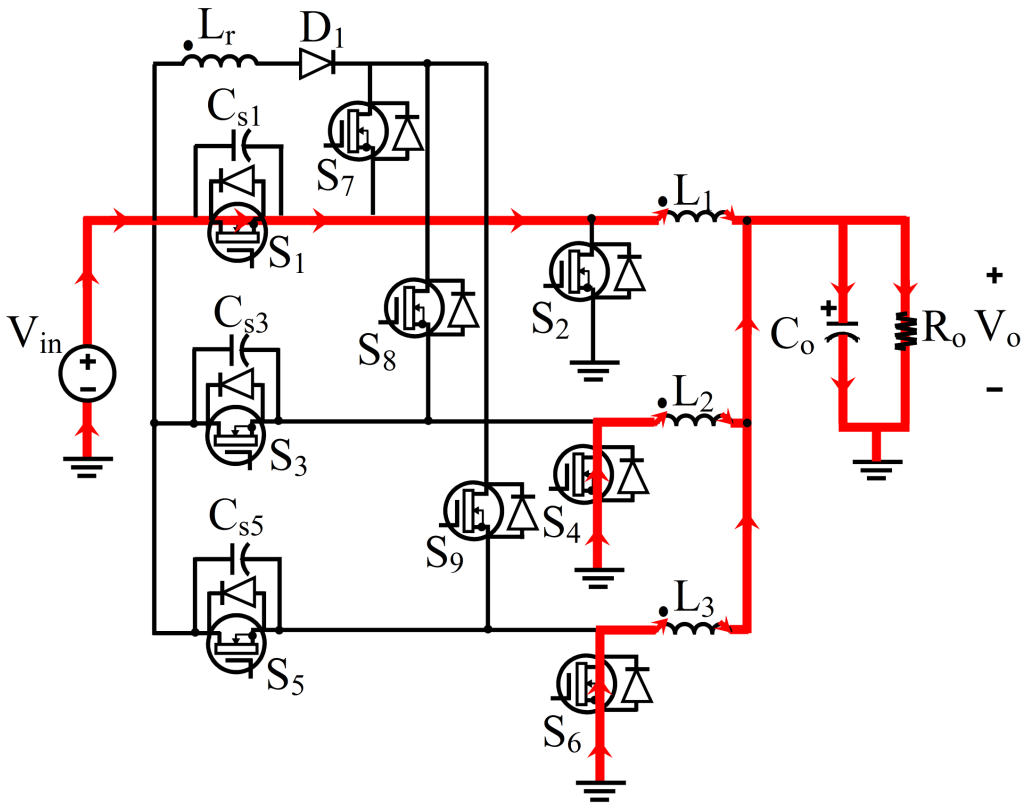


Fig. 4.3 (d): Modes of operation: Mode 4 (t_3 — t_4)

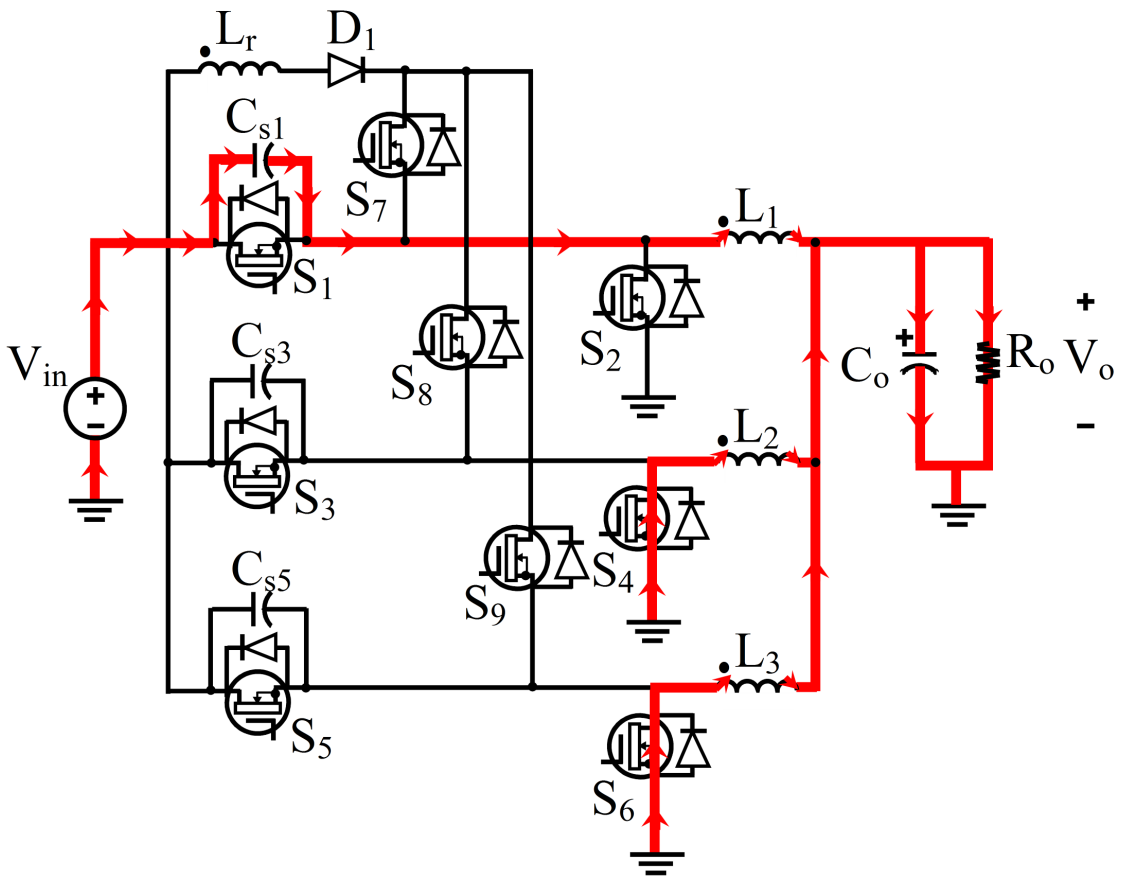


Fig. 4.3 (e): Modes of operation: Mode 5 (t_4 — t_5)

4.4 Output voltage

The output voltage can be evaluated by balancing the volt-second relationship or by equating the energy relation i.e.,

$$V_o\tau = 3V_{in}[\,t_{01} + t_{12} + t_{23} + t_{34} + t_{45}\,]$$

$$V_o\tau = 3V_{in}\left[\frac{I_0 L_r}{3V_{in}} + \frac{2L_r}{R}\ln\frac{3I_{Lrmax}}{I_0} + \frac{2L_r}{R_{on}}\ln\frac{3I_{Lrmax}}{I_0} + RC_{S1}\ln\frac{V_{CS1}}{RC_{S1}}\right] \quad (4.11)$$

Where $\tau = \frac{1}{f_s}$ and f_s =Switching frequency.

From the above expression, it is noticeable that voltage conversion ratio depends upon switching frequency irrespective of the duty ratio.

4.5 Design Procedure

In order to use the proposed converter as an application of VRM, the auxiliary circuit parameters are chosen in an eloquent way. The design procedure of the auxiliary circuit components is as follows:

4.5.1 Resonant Capacitor C_{s1}

Resonant capacitor C_{S1} is selected to discharge from V_{in} to zero with the maximum output current over at least the time period t_{on} during the turn on of body diode. In this state, according to equations (4.3)

$$RC_{S1}\, ln\frac{RI_0}{V_{CS1}} \geq t_{on} \tag{4.12}$$

4.5.2 Resonant Inductor L_r

Resonant inductor L_r is selected such that current through inductor can be reduced to zero from $I_o/3$ in the same duration of rise in current from zero to $I_o/3$ in main switch. In this case, from equation (4.5),

$$t_{23} = \frac{L_r}{R_{dson}} \tag{4.13}$$

4.6 Simulation and Experimental Results

The proposed converter is simulated using simulation software PSIM version 7.1 co-simulated with MATLAB/Simulink. The proposed converter works with an input voltage of V_{in}= 12V and an output voltage of V_o=1V, a load current of 100A and a switching frequency of f_s=500 kHz. Fig. 4.4 (a)—(k) shows the simulation results of the proposed converter.

Fig. 4.4 (a) – 4.4 (i) shows the voltage and current waveforms of the main, synchronous and auxiliary switches in the proposed ZVT-ZCT PWM SBC. Fig. 4.4 (j) and fig. 4.4 (k) presents the current waveform of resonant inductor L_r and shows the currents through filter inductors L_1, L_2, L_3. From the simulation results of the proposed converter which are shown in the fig. 4.4 (a)-4.4 (i), the voltage and current stresses are low as there are no rising and falling peaks during the turn ON and turn OFF of the switches because of the active auxiliary circuit incorporated with conventional multiphase synchronous buck converter which provides soft switching conditions for the switches. From the results, it is clear that the voltages of the switches are not greater than the input voltage and the currents through them

are not more than the average output current that eliminates the complication in switch selection. The simulation results of main, synchronous and auxiliary switches substantiate that the voltage and current stresses are extremely low. The uniform current distribution in each phase, which is a major problem in a multiphase synchronous buck converter, is elucidated in the proposed converter.

TABLE 4.1

COMPONENTS USED FOR PROPOSED CONVERTER

Component	Experimental value/Model
Main Switches, S_1, S_2, S_3	IRLR8721PbF
Synchronous Switches, S_4, S_5, S_6	IRLR8721PbF
Auxiliary Switches, S_7, S_8, S_9	IRLR8721PbF
Diode D_1	MBRB4030
Resonant Inductor, L_r	22 nH
Capacitors C_{s1}, C_{s2}, C_{s3}	4.7 nF
Output Capacitor, C_o	20 µF
Output Inductor, L_1, L_2, L_3	2 µH

The multiphase ZVT-ZCT PWM synchronous buck converter integrated with active auxiliary circuit has been built and substantiated with experimental results. The experimental prototype built in the laboratory of the proposed converter is shown in fig. 4.5. Experimental results shown in fig. 4.6 depicts analogous to the simulation results. Fig. 4.6 (a), fig. 4.6 (c), fig. 4.6 (e) shows the voltage and current waveforms of main switches S_1, S_3, S_5 wherein the voltage and current stresses of the main switches are imperceptible. Fig. 4.6 (b), fig. 4.6 (d), fig. 4.6 (f) presents the voltage and current waveforms of synchronous switches S_2, S_4, S_6, which shows minimal voltage and current stresses. Similarly fig. 4.6 (g)-4.6 (i) corroborates that the voltage and current stresses of auxiliary switches S_7, S_8, S_9 are eliminated. Fig. 4.6 (j) presents the current waveform of resonant inductor L_r. Fig. 4.6 (k) depicts that the current through the filter inductors L_1, L_2, L_3, in each phase uniformly distributed that solves the issue of phase shedding. The experimental components employed in the proposed ZVT-ZCT multiphase SBC converter are tabulated in Table 4.1. Fig. 4.7 (a) signifies that the main switch S_1 spike current is decimated; the waveform is almost equivalent to the traditional buck converter. Thus, the rating of the main switch required for the buck converter is retrenched by the introduction of ZVT-ZCT operation. The main switch is turned ON under

ZVT and turned OFF with ZCT, due to which the mainstream switching losses got diminished. It can be observed from Fig. 4.7 (b) that the synchronous switch S_2 is turned OFF under ZCT and turned ON with ZVT operation. The reverse recovery (RR) effect due to the body diode of S_2 is almost attenuated. The auxiliary switch in fig. 4.7 (c) is turned ON under ZVT and turned OFF with ZCT thereby reducing the voltage and current stresses on the switch. The simulation and experimental results affirms that the component's voltage and current ratings, and also the energy volumes of passive elements used are considerably reduced that enhances the performance of the proposed converter.

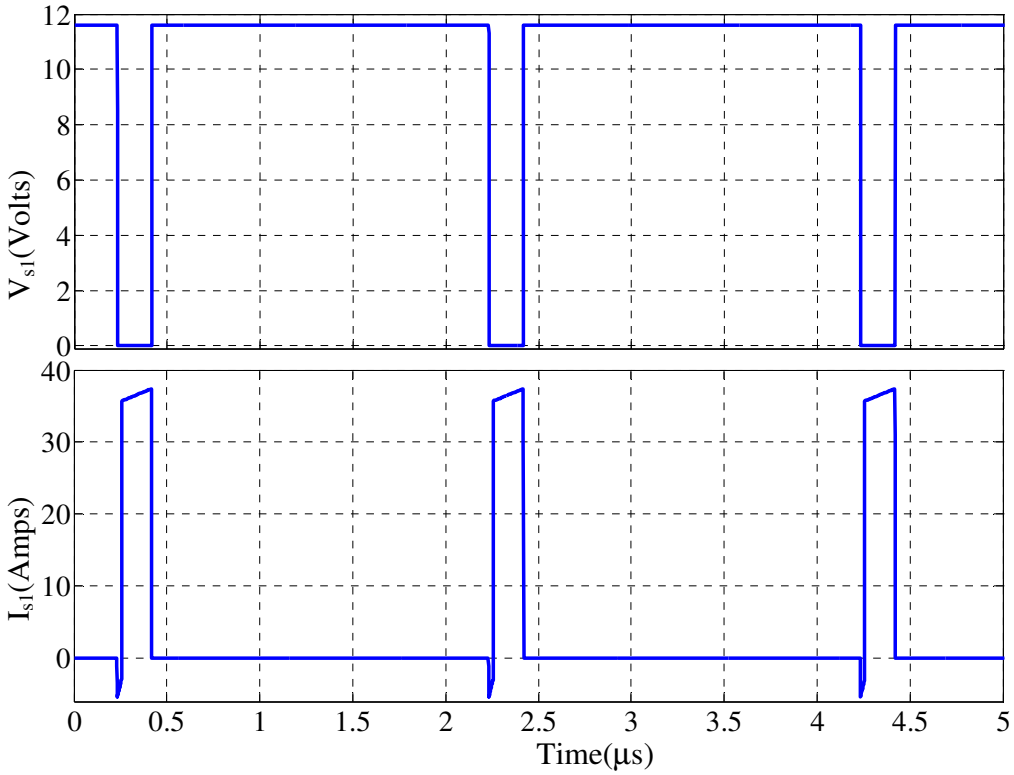


Fig. 4.4 (a): Simulated voltage and current waveforms of main switch S_1: V_{s1} in Volts and I_{s1} in Amps.

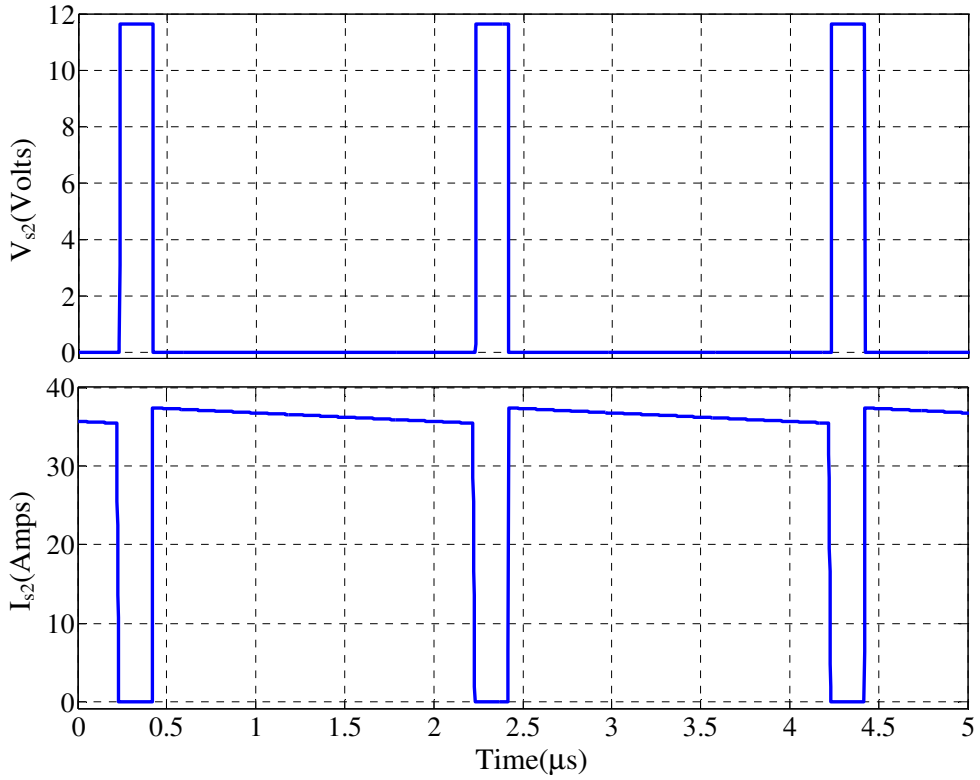


Fig. 4.4 (b): Simulated voltage and current waveforms of synchronous switch S_2: V_{s2} in Volts and I_{s2} in Amps.

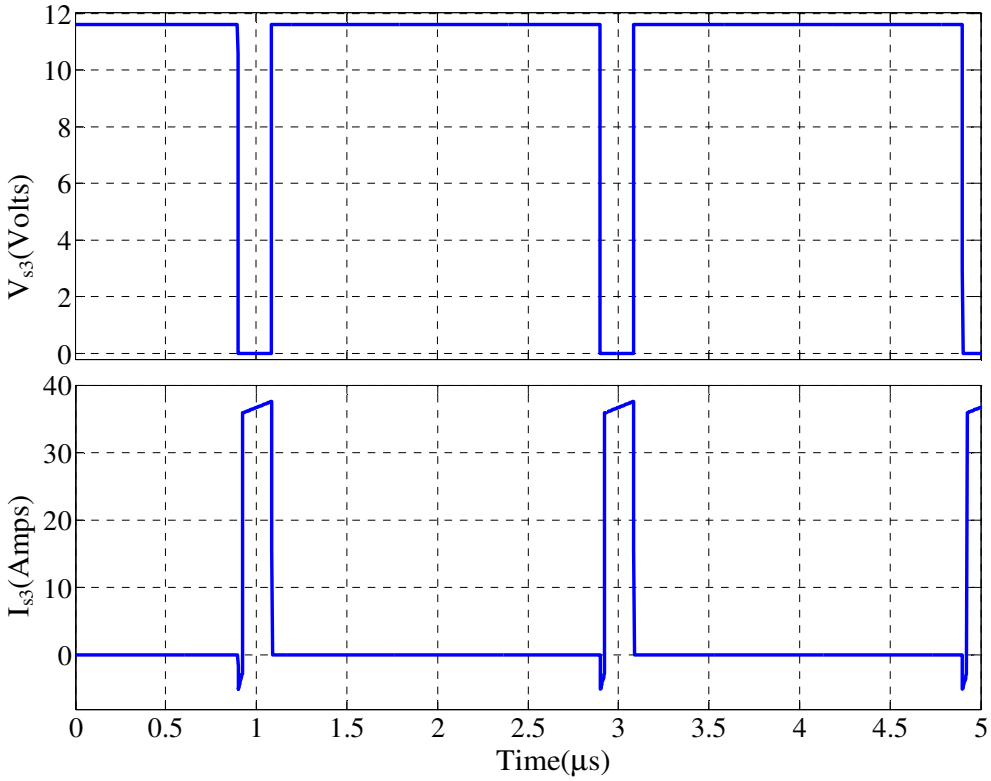


Fig. 4.4 (c): Simulated voltage and current waveforms of synchronous switch S_3: V_{s3} in Volts and I_{s3} in Amps.

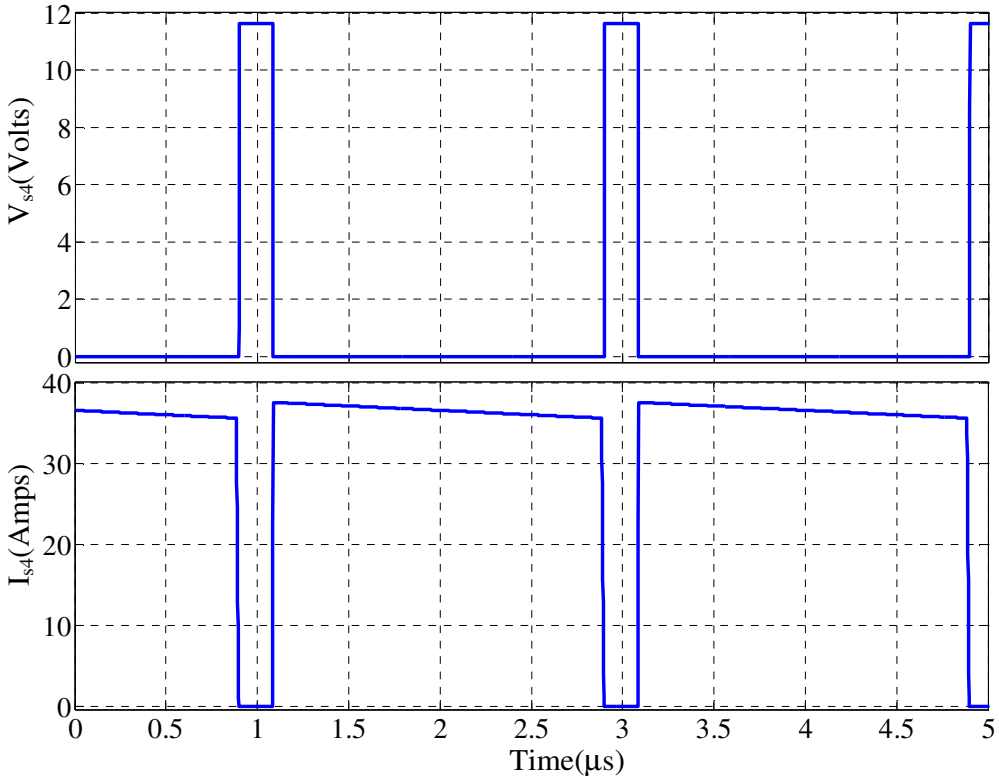


Fig. 4.4 (d): Simulated voltage and current waveforms of synchronous switch S_4: V_{s4} in Volts and I_{s4} in Amps.

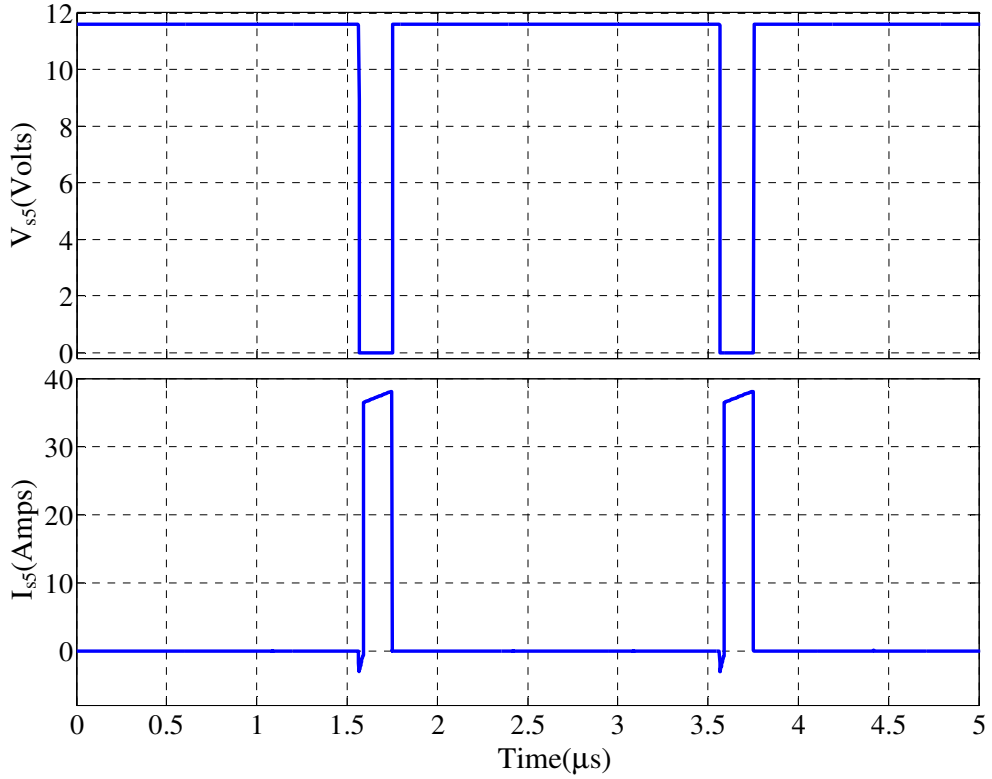


Fig. 4.4 (e): Simulated voltage and current waveforms of synchronous switch S_5: V_{s5} in Volts and I_{s5} in Amps.

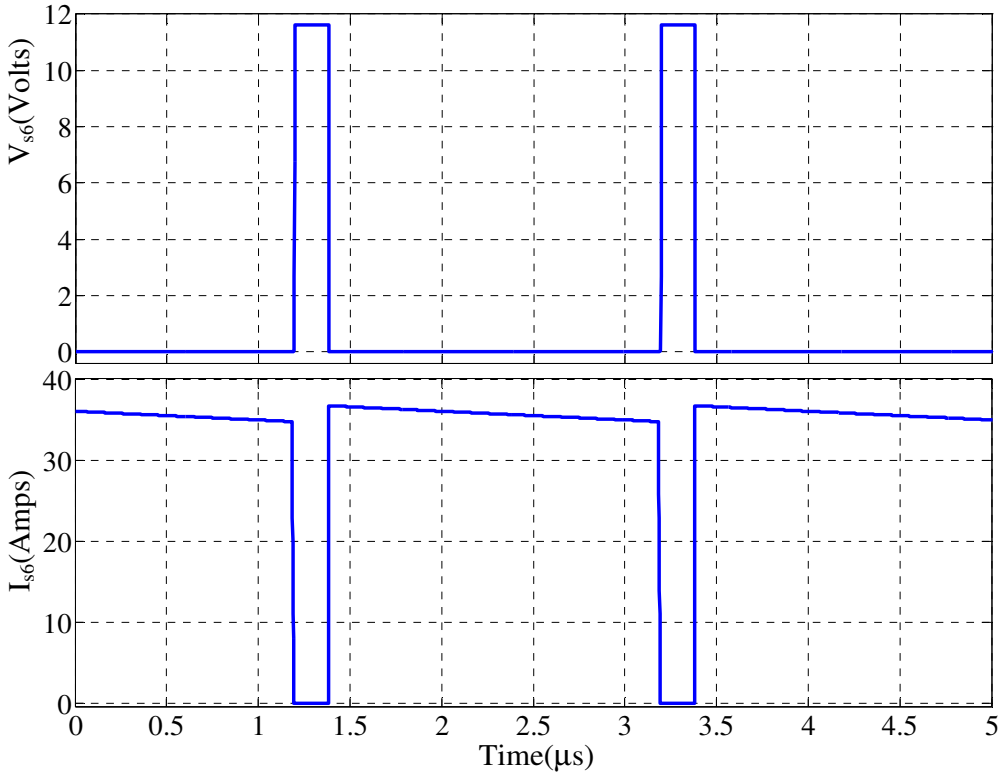


Fig. 4.4 (f): Simulated voltage and current waveforms of synchronous switch S_6: V_{s6} in Volts and I_{s6} in Amps.

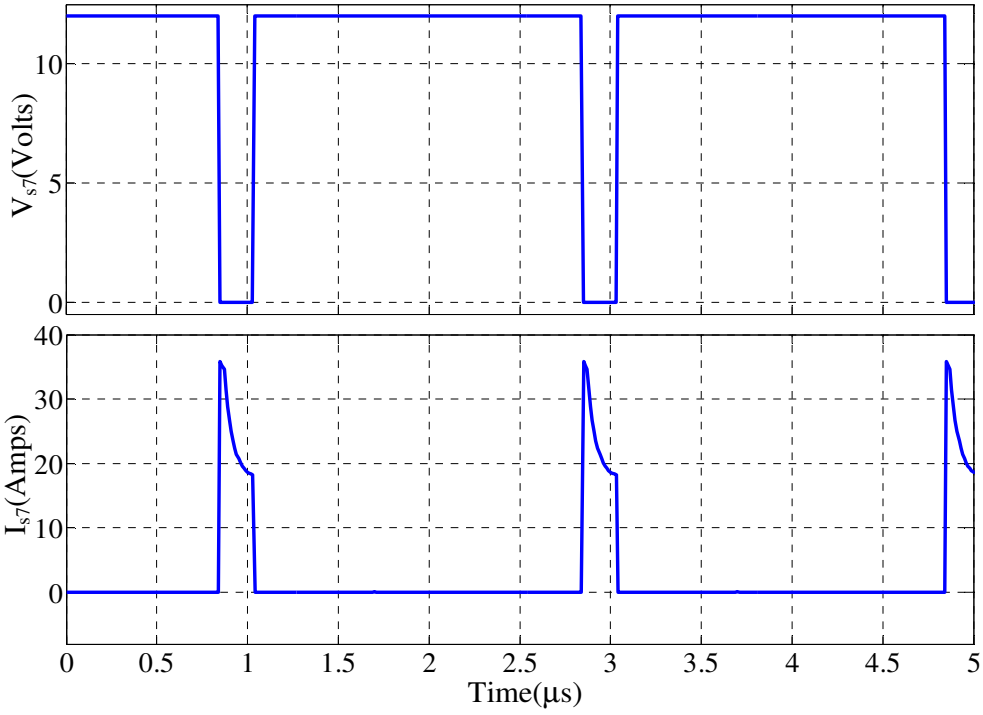


Fig. 4.4 (g): Simulated voltage and current waveforms of synchronous switch S_7: V_{s7} in Volts and I_{s7} in Amps.

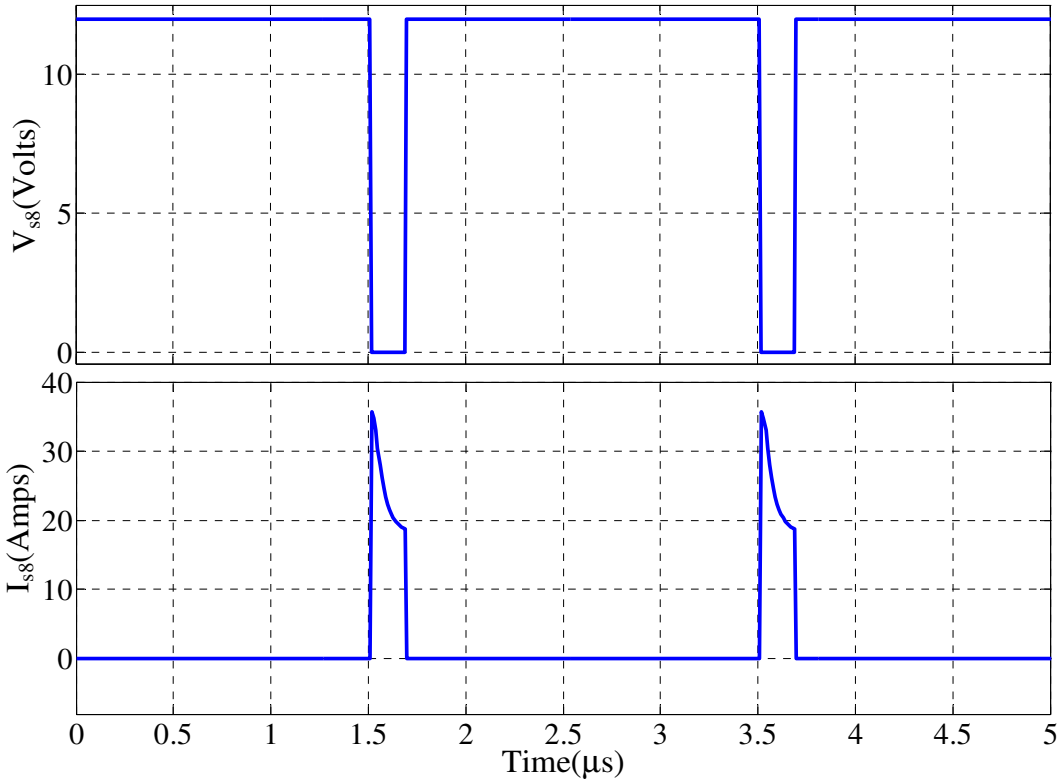


Fig. 4.4 (h): Simulated voltage and current waveforms of synchronous switch S_8: V_{s8} in Volts and I_{s8} in Amps.

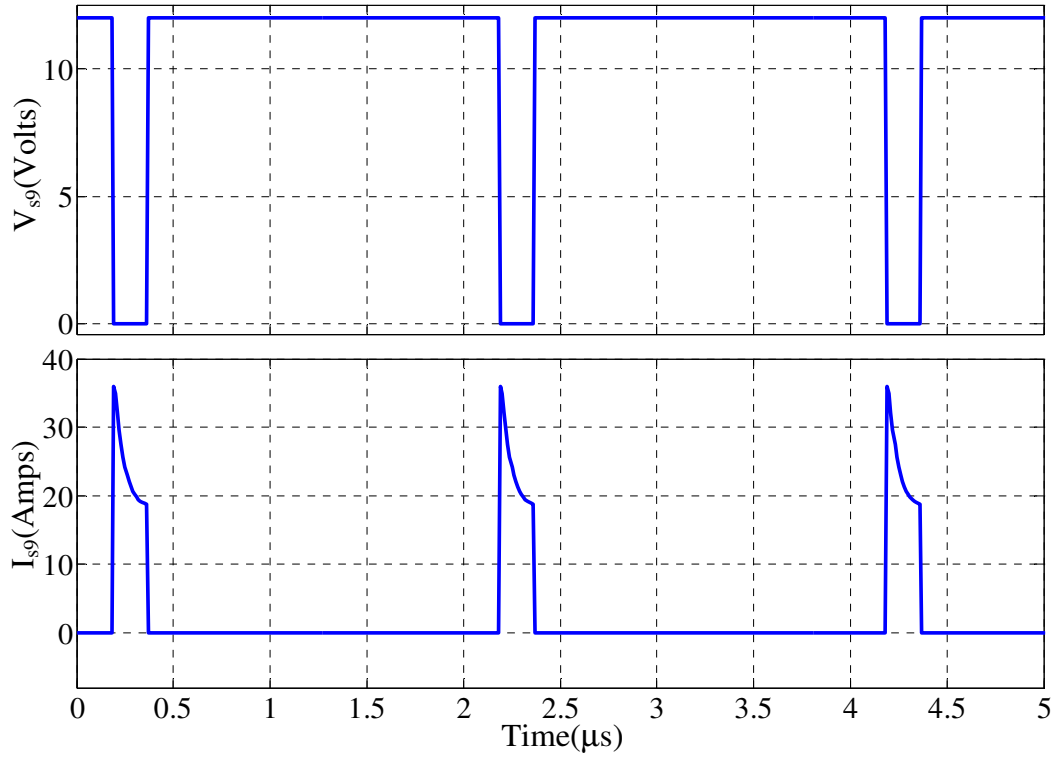


Fig. 4.4 (i): Simulated voltage and current waveforms of synchronous switch S_9: V_{s9} in Volts and I_{s9} in Amps.

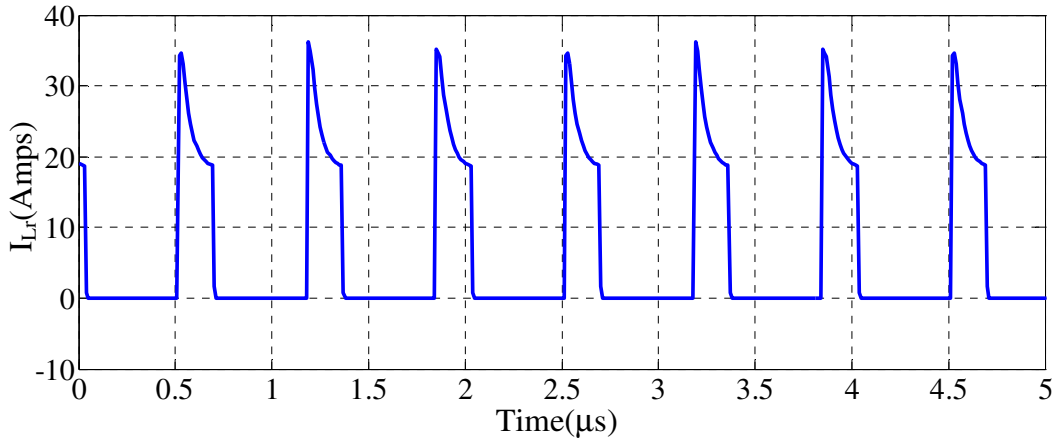


Fig. 4.4 (j): Simulated current waveform of resonant inductor: I_{Lr} in Amps.

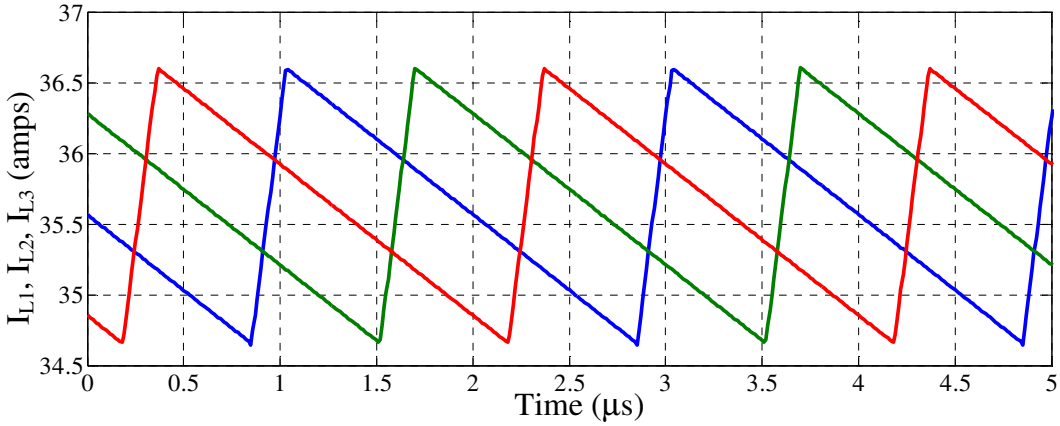


Fig. 4.4 (k): Simulated current waveforms of filter inductors: I_{L1}, I_{L2}, I_{L3} in Amps.

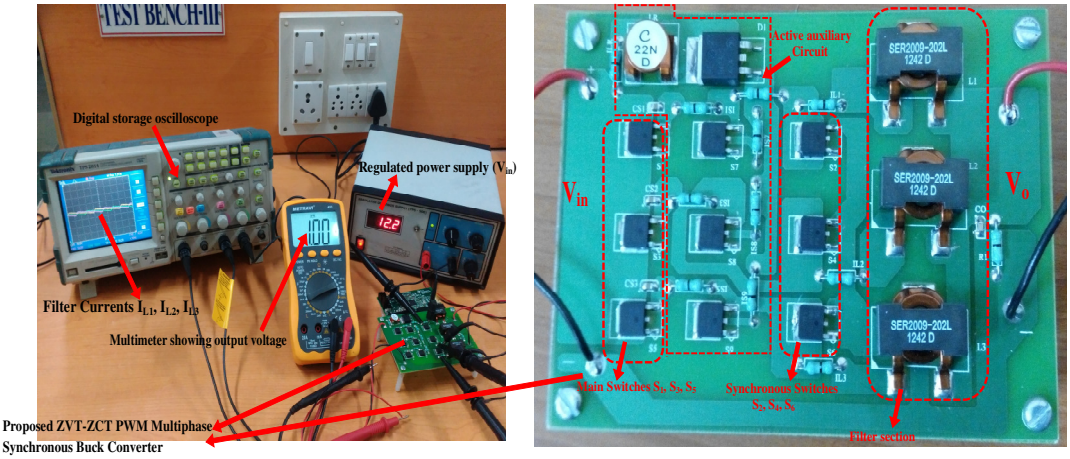


Fig. 4.5: Experimental setup of proposed multiphase ZVT-ZCT PWM synchronous Buck Converter

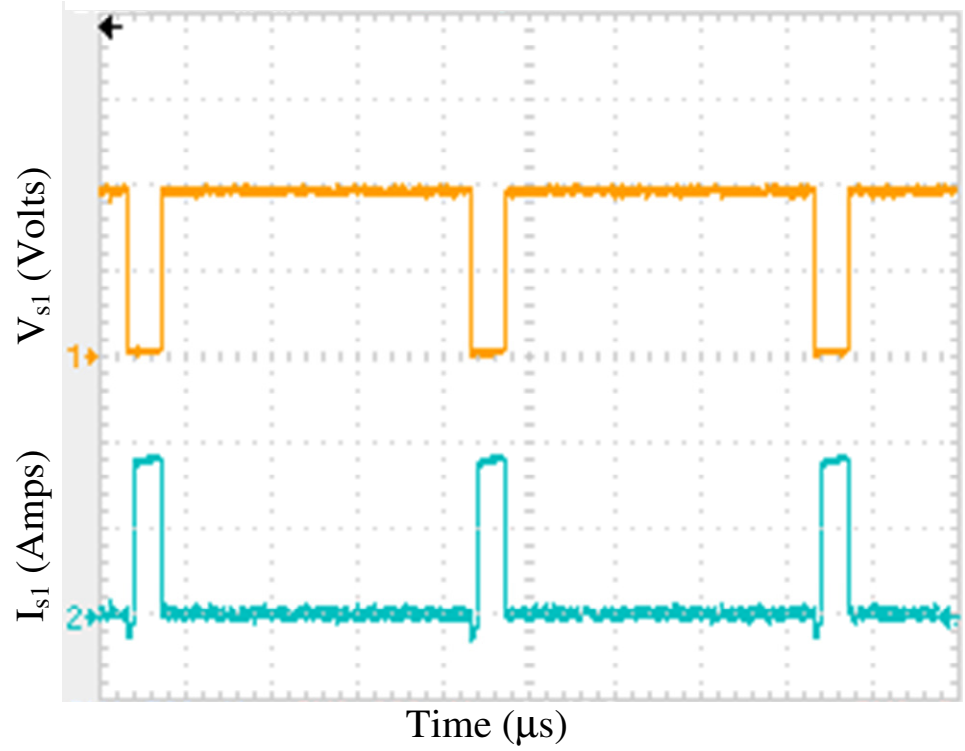


Fig. 4.6 (a): Experimental voltage and current waveform of Main switch S_1: [Vs_1: 6V/Div; Is_1: 17.5A/Div; time: 0.5µs/Div]

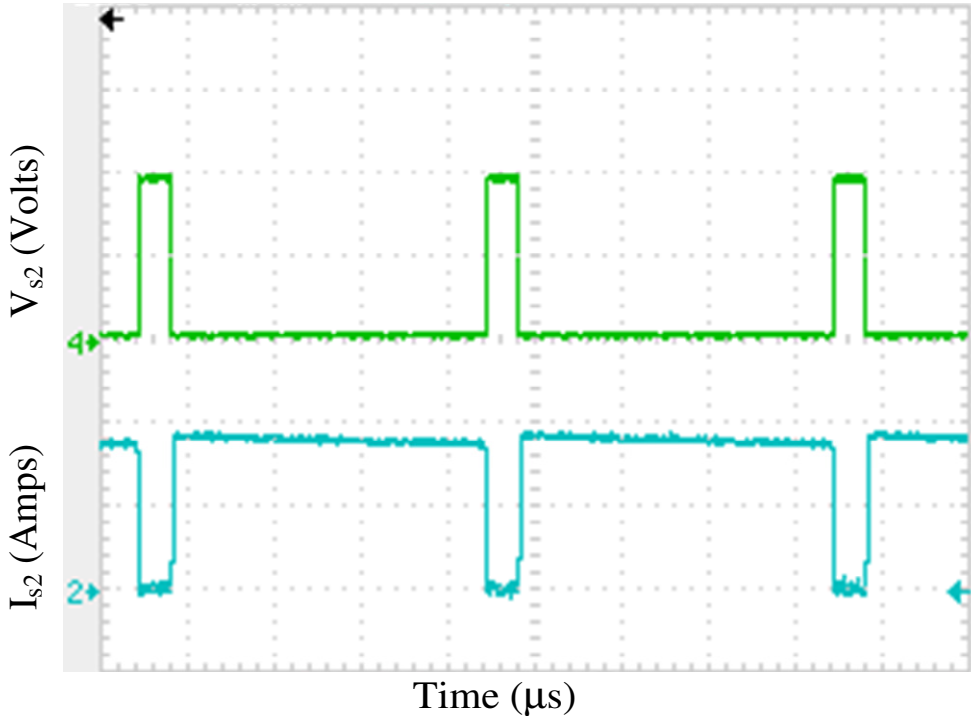


Fig. 4.6 (b): Experimental voltage and current waveform of synchronous switch S_2: [Vs_2: 6V/Div; Is_2: 17.5A/Div; time: 0.5µs/Div]

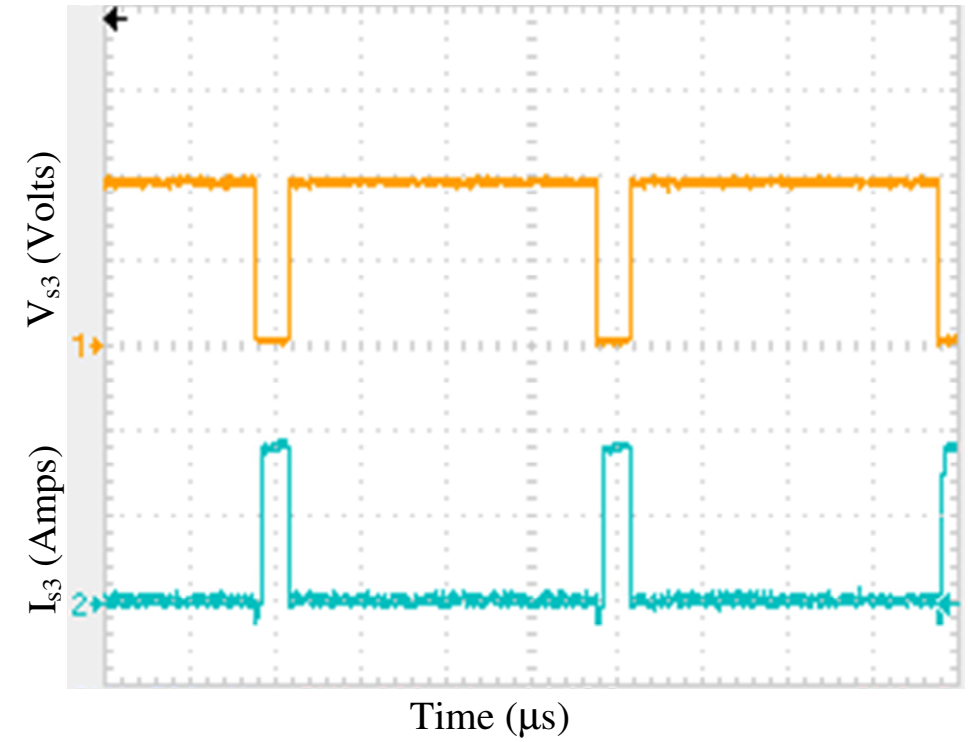


Fig. 4.6 (c): Experimental voltage and current waveform of synchronous switch S_3: [Vs_3: 6V/Div; Is_3: 17.5A/Div; time: 0.5µs/Div]

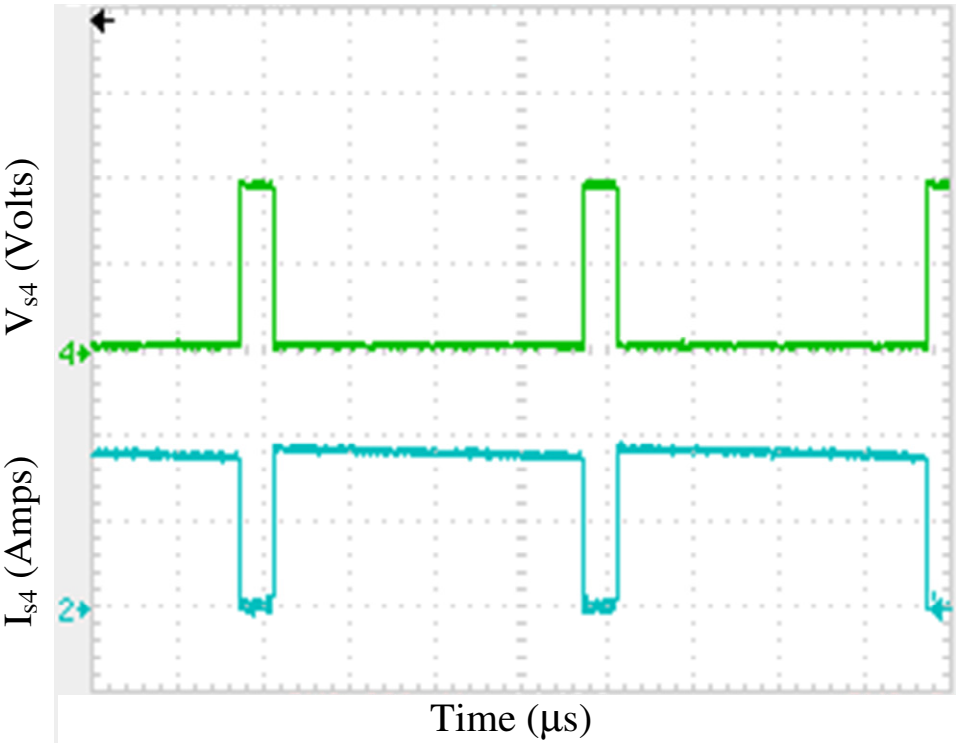


Fig. 4.6 (d): Experimental voltage and current waveform of synchronous switch S_4: [Vs_4: 6V/Div; Is_4: 17.5A/Div; time: 0.5µs/Div]

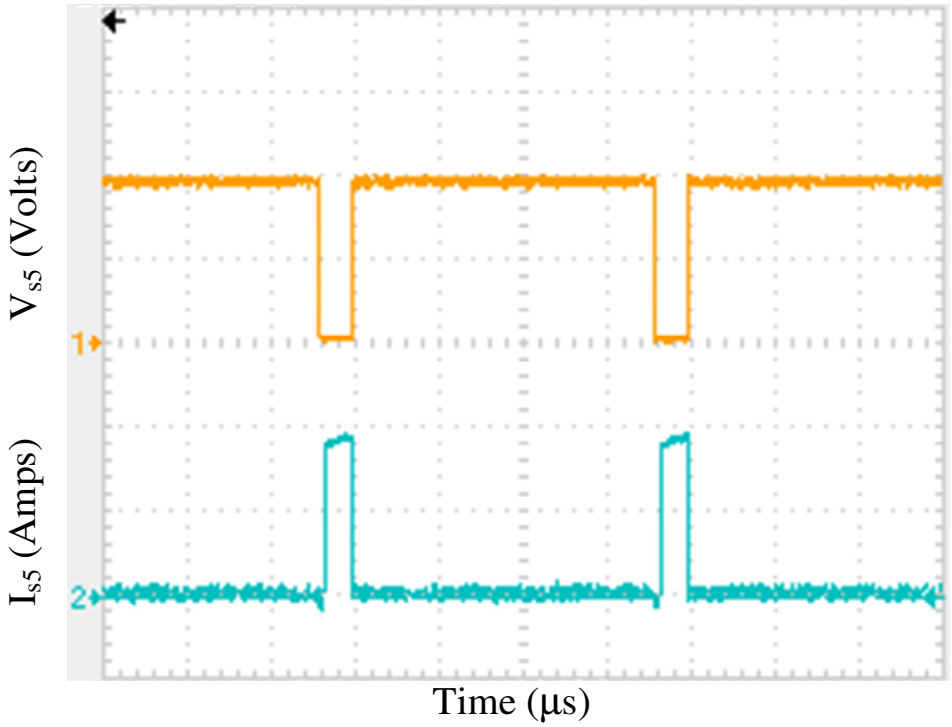


Fig. 4.6 (e): Experimental voltage and current waveform of synchronous switch S_5: [Vs_5: 6V/Div; Is_5: 17.5A/Div; time: 0.5µs/Div]

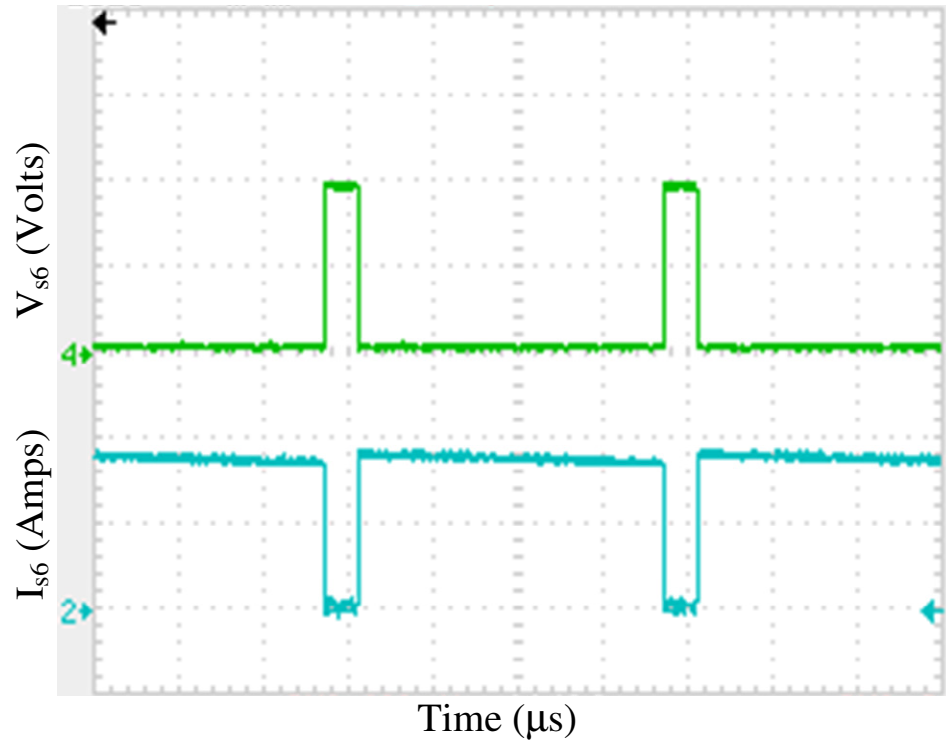


Fig. 4.6 (f): Experimental voltage and current waveform of synchronous switch S_6: [Vs_6: 6V/Div; Is_6: 17.5A/Div; time: 0.5µs/Div]

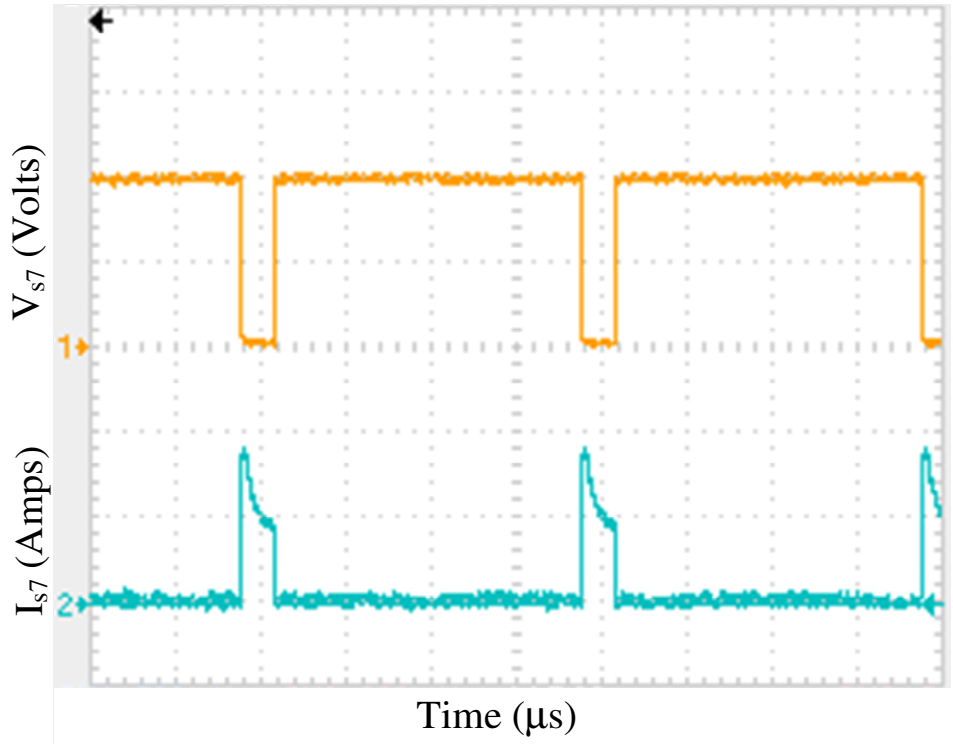


Fig. 4.6 (g): Experimental voltage and current waveform of synchronous switch S_7: [Vs_7: 6V/Div; Is_7: 17.5A/Div; time: 0.5µs/Div]

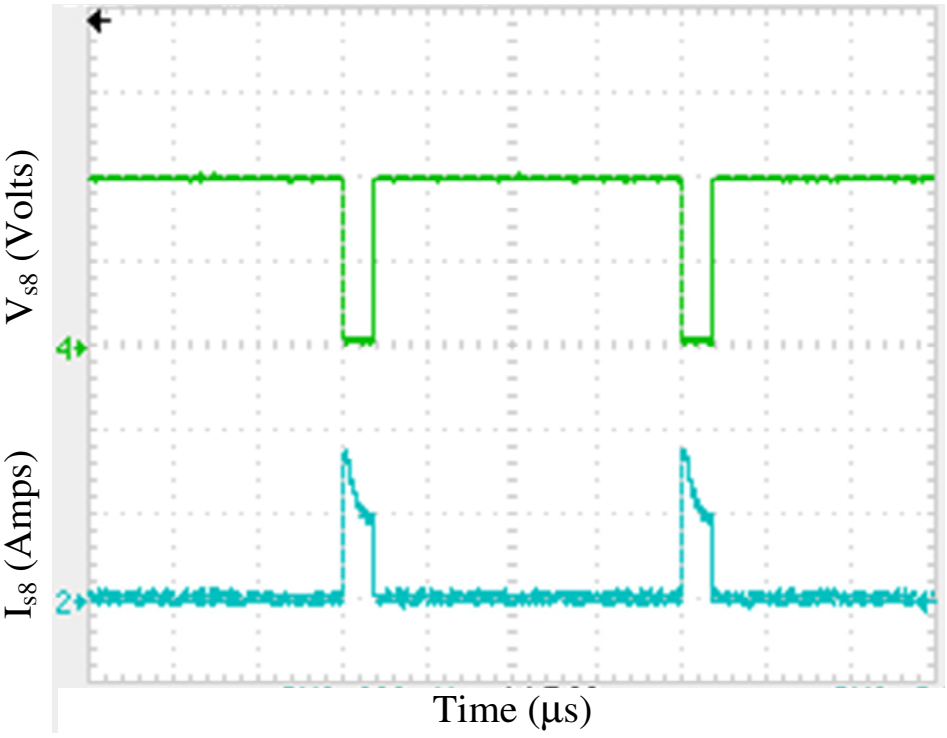


Fig. 4.6 (h): Experimental voltage and current waveform of synchronous switch S_8: [Vs_8: 6V/Div; Is_8: 17.5A/Div; time: 0.5µs/Div]

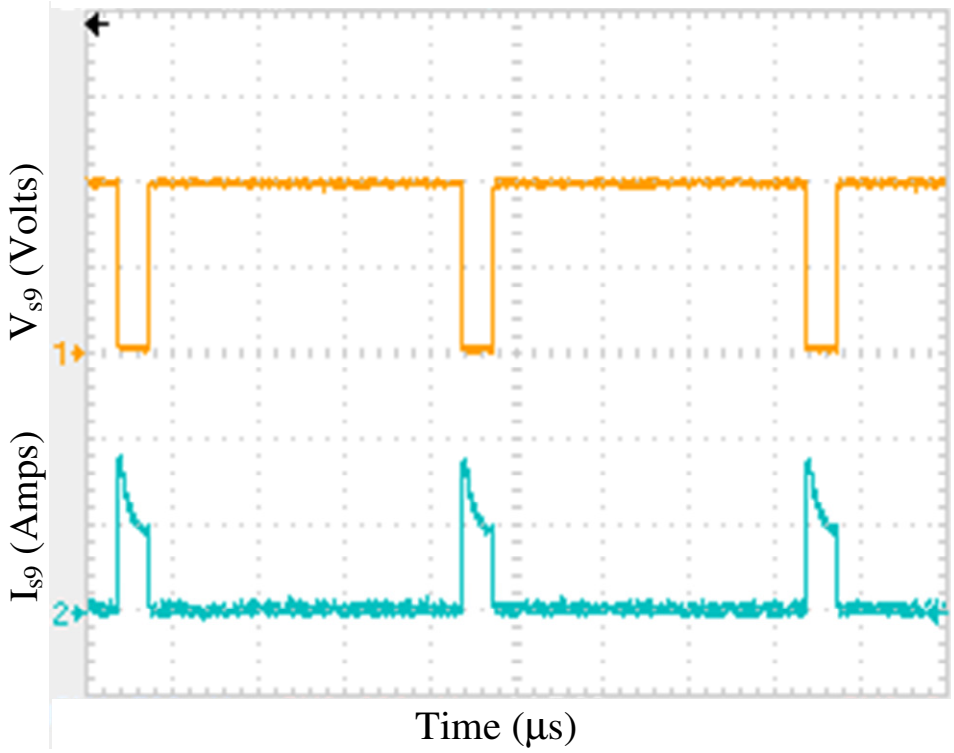


Fig. 4.6 (i): Experimental voltage and current waveform of synchronous switch S_9: [V_{S9}: 6V/Div; I_{S9}: 17.5A/Div; time: 0.5µs/Div]

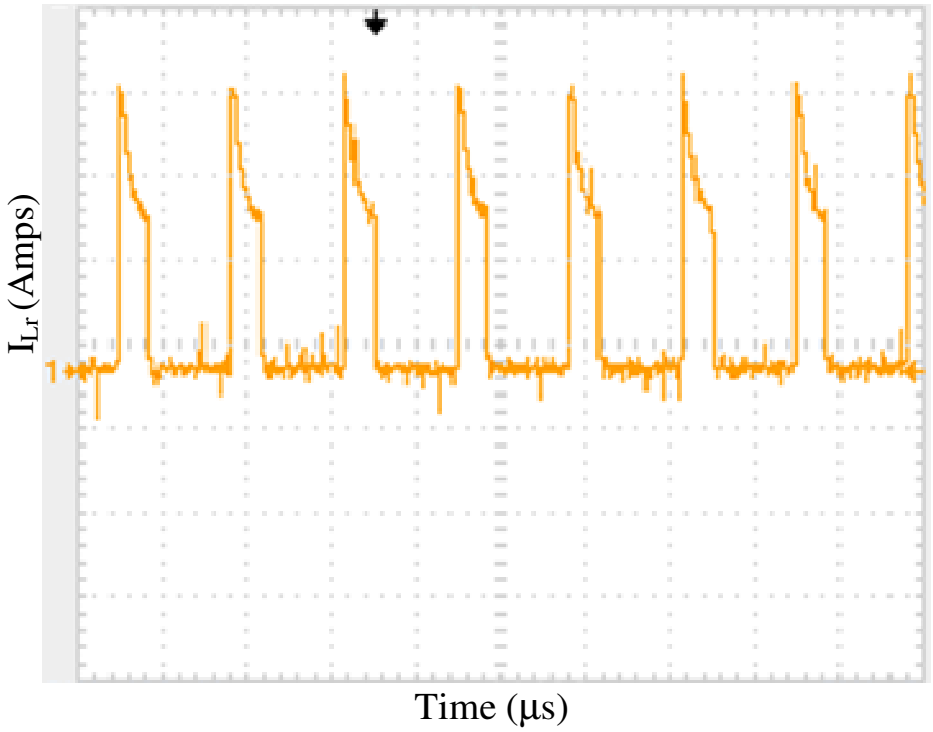


Fig. 4.6 (j): Experimental current waveform of resonant inductor L_r: [I_{Lr}: 10A/Div; time: 0.5µs/Div]

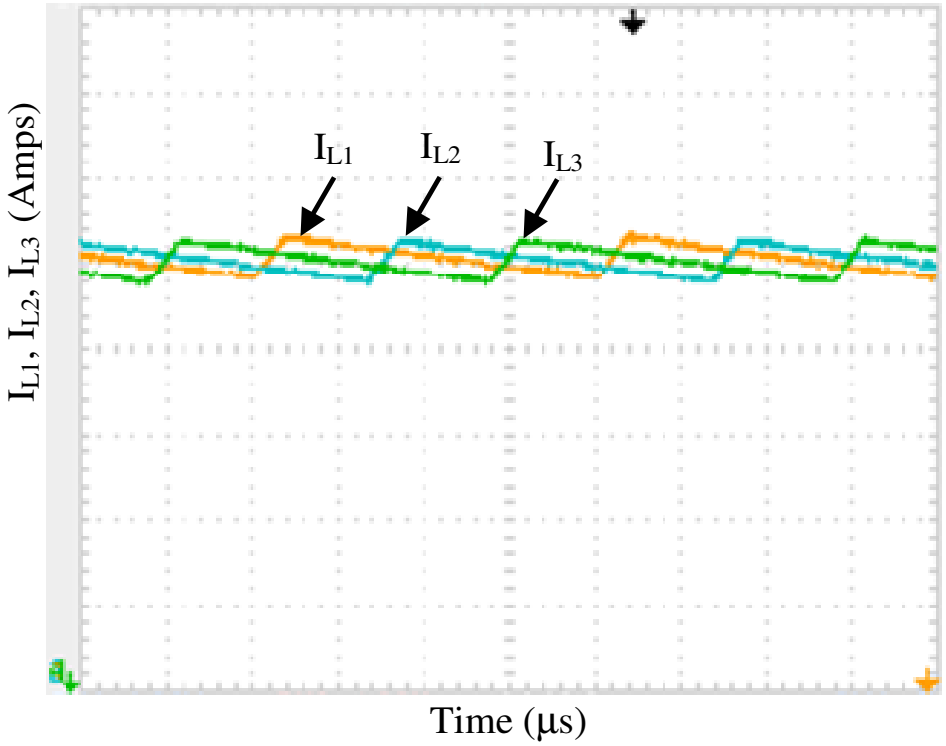


Fig. 4.6 (k): Experimental current waveform of filter inductors L_1, L_2, L_3: [I_{L1}, I_{L2}, I_{L3}: 7A/Div; time: 0.5µs/Div]

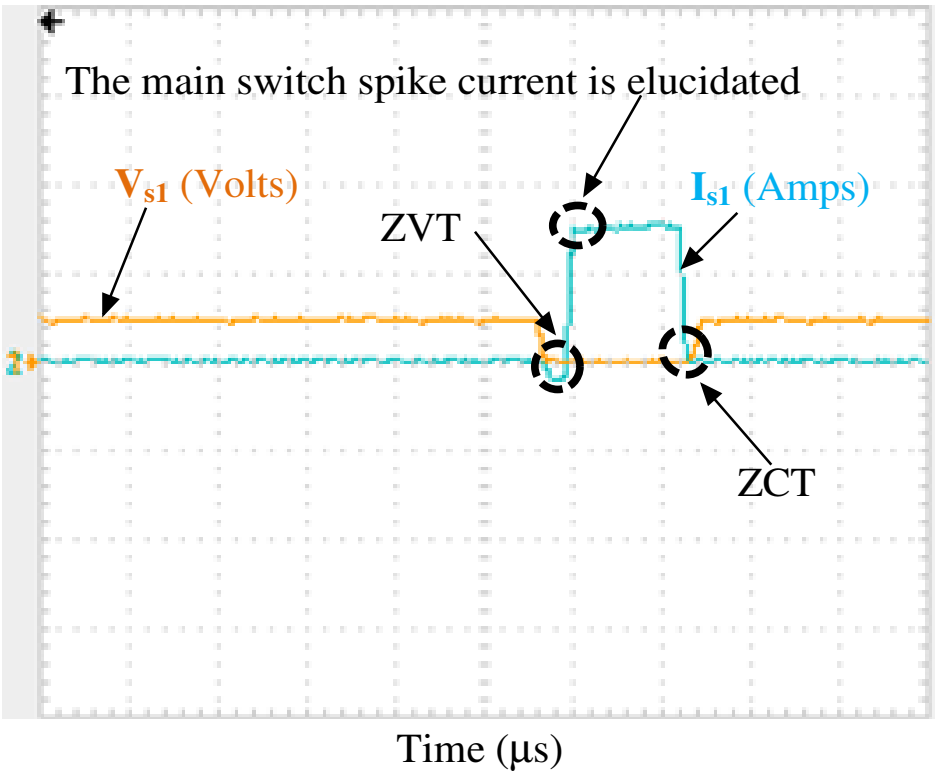


Fig. 4.7 (a): Experimental voltage and current waveforms of main switch S_1 exhibits soft switching conditions [Vs_1:24V/Div; Is_1: 20A/Div; time: 0. 2µs/Div].

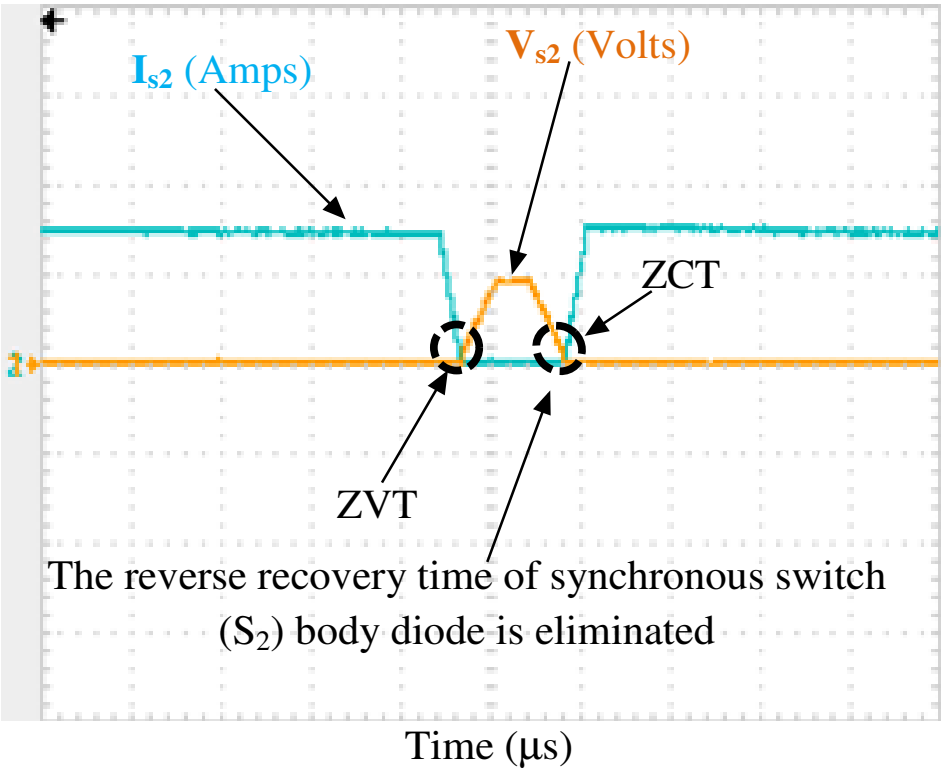


Fig. 4.7 (b): Experimental voltage and current waveforms of synchronous switch S_2 exhibits soft switching conditions [Vs_2: 24V/Div; Is_2: 20A/Div; time: 0.2µs/Div].

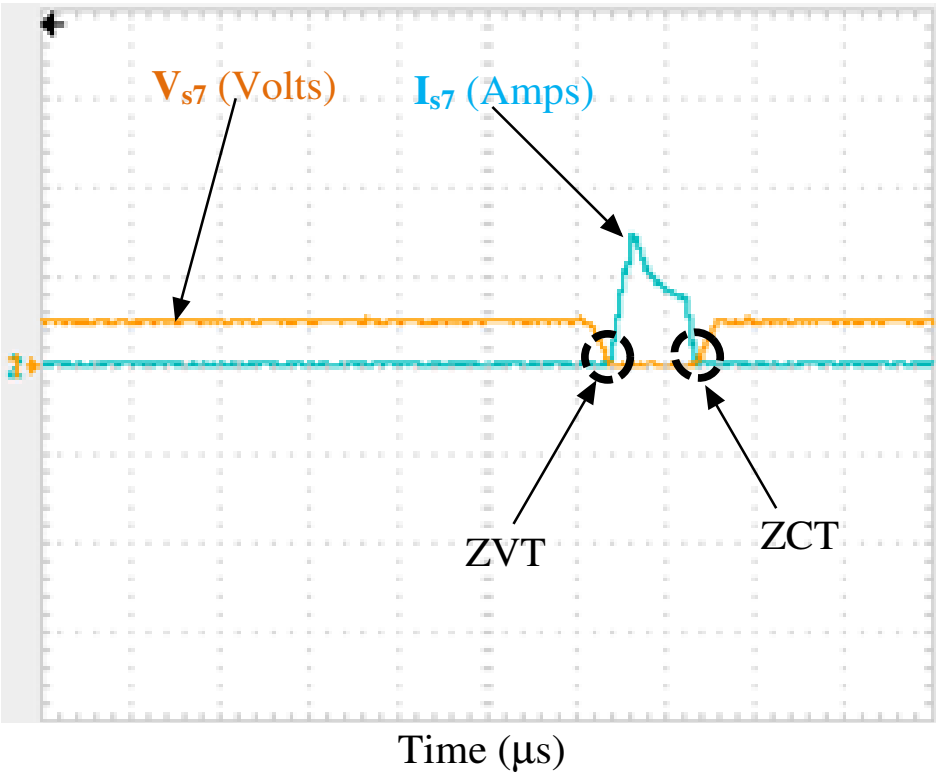


Fig. 4.7 (c): Experimental voltage and current waveforms of auxiliary switch S_7 exhibits soft switching conditions [Vs_7: 24V/Div; Is_7: 20A/Div; time: 0.2µs/Div].

4.7 Efficiency curve

From fig. 4.8, it can be seen that efficiency values of the proposed converter are comparatively higher than the traditional converter. The converter is designed for the maximum output current, and it is accustomed that towards minimum output power efficiency decreases. At nearly 70A of output current, the efficiency of the proposed converter rises to about 96% when compared to the counterpart traditional converter, whose efficiency is about 92%. The high efficiency of the proposed converter proves the definiteness of the design values.

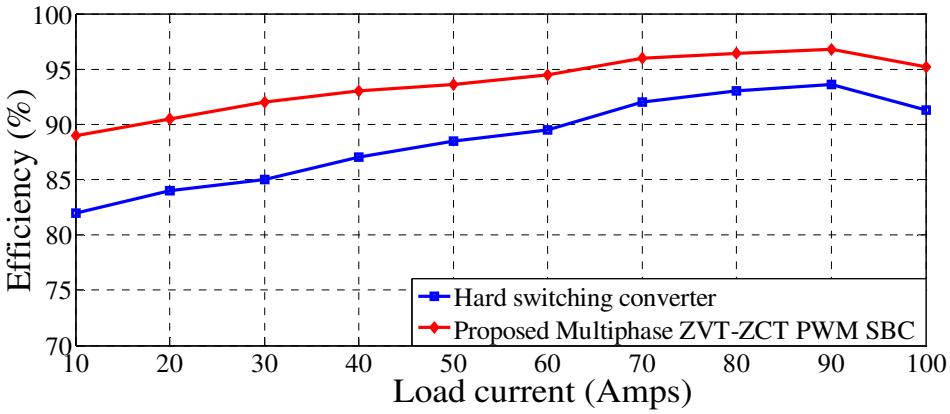
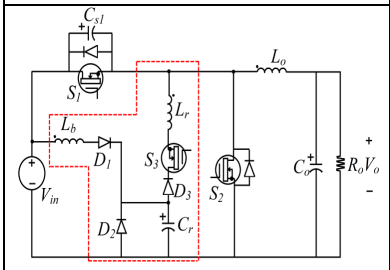
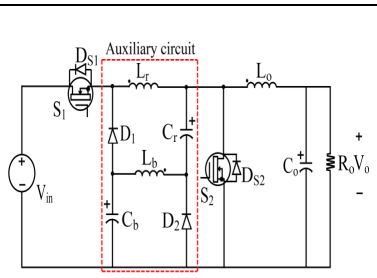
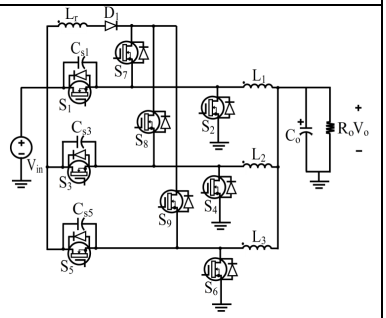


Fig. 4.8: Efficiency curve of proposed converter in comparison with traditional buck converter.

4.7.1 Contrast between the proposed converters

TABLE 4.2
COMPARISON AMONG THE PROPOSED CONVERTERS

Synchronous buck converter with active auxiliary circuit	Passive auxiliary circuit integrated with synchronous buck converter	Multiphase synchronous buck converter with active auxiliary circuit
		
All semiconductor devices operate under soft switching condition. Main switch	All semiconductor devices operate under soft switching condition. Both the switches	The switches in the circuit operate under soft switching condition i.e., ZVS turn ON and

operates with ZCZVS and auxiliary switch turns ON with ZVT and turns OFF with ZCT	operate with ZVT-turn OFF and ZCT-turn ON.	ZCS turn OFF.
The auxiliary circuit consists of an extra switch, diodes D_1, D_2, D_3, resonant inductors L_r, L_b and resonant capacitor C_r. The extra switch increases the complexity of the control circuit; structure is complex and a little high cost.	The auxiliary circuit consists of a resonant inductors L_r, L_b, resonant capacitors C_r, C_b and diodes D_1, D_2. The circuit is easily controllable, simple and low cost.	The auxiliary circuit consists of a switch S_7, a diode D_1, resonant inductor L_r and a resonant capacitor C_{s1} for each phase. The switch in each phase adds control complexity and increases the cost but outweighs the other two converters in terms of application point of view.
The efficiency at maximum load is about 96%	Efficiency at maximum load is 97%	The efficiency at maximum load is 95%.
It is used for high density power applications.	Circuit is used for low power applications at high switching frequency.	Used for low voltage high current applications such as laptop and desktop processors.

Moreover, switching losses of the proposed converters and stresses of the switches are minimised by utilising their corresponding auxiliary circuits.

4.8 Summary

The concept of ZVT-ZCT is implemented in multiphase synchronous buck converter and it is shown that the switching losses in synchronous buck converter are eliminated. Significant efficiency improvement with soft switching as compared to hard-switching converter is achieved and it is evident from the efficiency curve. Both main switch and synchronous switches are turned-on and turned-off under ZVS and ZCS respectively. The auxiliary switches are turned-on and turned-off under ZVS and ZCS with tolerable voltage stresses across the switch. Hence, switching losses are reduced and the proposed multiphase synchronous buck converter is highly efficient than the conventional converter. In contrast to the conventional topology the proposed topology resolves the issues of unbalance distribution of current, the high amount of losses in the converter and operates with both soft switching conditions that enhance the performance of the converter. This proposed converter with a high switching frequency is designed for application in new generation microprocessor.

Chapter 5

CONCLUSIONS AND FUTURE SCOPE

CHAPTER 5: CONCLUSIONS AND FUTURE SCOPE

5.1 Conclusions

The modern power electronic equipment demands high power density, high efficiency, low cost and reliability that creates different challenges to the power supply designer. A switchmode rectifier with enhanced performance should possess these demands. Design of a DC- DC buck converter with high efficiency should be made in viewpoint of contemporary topologies. Applications such as automotive power systems, industrial controls, distributed systems, desktop processors requires DC-DC converter with high step down voltage conversion, that results in high operating switching frequency. The converter operating at high frequency reduces the size of the converter and cost, but raises the frequency related losses i.e., switching loss.

The thesis focuses on finding the solution for high step down converters and low power converter with a high switching frequency. The traditional buck topology is unable to deal with low voltage conversion ratio, as it results in degradation of converter efficiency, lags in utilizing the components and hinders the transient response. The dissertation includes the topologies to overcome these drawbacks by applying the soft switching techniques into the synchronous buck converter.

To accomplish high power density, there is a need to increase switching frequency. The increase in switching frequency leads to rise in the switching loss. Hence, minimizing the loss issue is a prime factor which is achieved by soft switching techniques.

The present research unveils distinct topologies with enhanced performance DC-DC converter for various applications. The work presented in this thesis specifically contributed chapters from 2,3,4 can be summarised as follows:

1. For high density power applications a ZVT-ZCT PWM synchronous buck converter is proposed. The topology is incorporated with active auxiliary circuit and validated in the laboratory. The components used in the auxiliary circuit have lower ratings than the main power circuit; that reduces the loss as it is used for short duration in a switching cycle. The concept of ZVT-ZCT is applied in a synchronous buck converter in the high power conditions result in the decrease of switching loss. Simulation and experimental results show that the main switch turns ON and turns OFF with ZCZV condition, the synchronous switch turns ON with ZVT and turns OFF with ZCT whereas the auxiliary switch turns ON with ZVT and turns OFF with ZCT, so these results lead to the reduction in the switching loss of the proposed converter. The efficiency of the proposed converter is more in contrast to the conventional

synchronous buck converter and it is verified in the efficiency graph. The voltage and current stresses on the switches are low and maintained to be under tolerable values. The converter is structurally simple, cost effective and highly efficient.

2. A passive auxiliary circuit is employed into the synchronous buck converter to accomplish the soft switching, for low power applications at high switching frequency. The reverse recovery peak current of the diode and switching loss of the switches are reduced by a large amount, using a simple passive auxiliary circuit which recovers the energy during turn ON. Furthermore, it also offers ZVS and ZCS switching conditions to turn ON and turn OFF. The energy in the snubber is recovered to the load exempting the use of main switch path, thereby conduction loss is curtailed. But this extra conduction loss is available in synchronous buck converter with active auxiliary switch, as the stored energy is transferred to the load through the main switch path. Consequently, the synchronous buck converter that incorporates passive auxiliary circuit is more efficient. The circuit layout is simple as it uses a lower number of circuit components. Experimental results are analogous to the simulation results and the converter is developed in the laboratory. The voltage and current stresses on the main components are within admissible values.
3. The modern trend new generation microprocessor demands low voltage, high current application converter. In order to meet such demands, the multiphase buck converter is a suitable candidate. The ZVT-ZCT soft swithing technique incorporated into the multiphase synchronous buck converter for high current application. The low duty cycle in the proposed converter facilitates to operate with a high switching frequency. High switching frequency leads to increase in switching loss. Therefore, concept of ZVT-ZCT employed into conventional multiphase synchronous buck converter to enhance the efficiency. An experimental setup is built in the laboratory and authenticated by the efficiency graph with conventional multiphase synchronous buck converter. The switches in the proposed converter turn ON under ZCS and turn OFF under ZVS which is shown by experimental and simulation results. The stresses on the devices are maintained under the tolerable range.

Switching loss in the converters and low duty cycle in low voltage, high current portable equipments are found to be a major concern. These problems in the converters are solved and solutions are established by the proposed soft switching topologies in the thesis.

5.2 Scope for Future Work

The dissertation has made an attempt to cross some technological barricades for the purpose of future power management. Research has been carried out to the maximum extent

and some solutions are found, but for the future research work some suggestions to enhance the quality of research in this area are as follows:

5.2.1 Control issues:

The proposed topologies operate with open loop conditions. Many control strategies such as voltage mode control, hysteresis control, current mode control etc., can be used for the performance enhancement like transient response, line regulation etc.

5.2.2 Parasitic effects in the components:

The parasitic capacitance is an inevitable and undesirable aspect that usually located between parts of the circuit and different electronic components which are in use as they are closely placed in the layout. The internal capacitance exists in different circuit elements such as inductors, transistors and diodes which cause to change their behaviour from ideal circuit element. Parasitic capacitance also exists in the wires and printed circuit board traces which are adjacently spaced conductors.

The inductor because of its orientation of close space winding, it often behaves as it consists of parallel capacitor. The potential difference present across coils is affected by the wires lying adjacent to them at different potentials produce electric field. This makes to act as plates of a capacitor that stores the charge. If the voltage across the coil is varied, it requires more current to charge and discharge the capacitors. In the low frequency circuits, of the voltage doesn't vary quickly, the excess current is negligible, but when the voltage varies abruptly the excess current is high and makes a significant impact on the operation of the circuit.

Thus, the low frequency circuital parasitic capacitance effect is neglected, whereas in the high frequency circuit it causes a major problem. The gate-source parasitic capacitance in the MOSFET creates an inevitable conduction in the switch even when the gate pulse is not applied. Hence, proper design of the converter of high frequency minimizes the effect of parasitic capacitance.

5.2.3 Designing the converter at high switching frequency:

In this dissertation, topologies are proposed and designed upto 500 kHz. The demand of high output power density with high frequency converter has been increased in the recent years. The output power density of the converter experiences untoward effects because of switching frequency. Therefore, there is a need to enhance the PCB layout design and analysis of the circuits that could constitute to improve the operating frequency. Despite, the issues arise from the high frequency converter design, PCB layout circuit design and power device

selection are the key factors to expand the ability of frequency-output product in high frequency converter application.

As frequency increases, the switches need to drive at high speed which is impractical.

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