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Built-In Reliability Design of a High-Frequency SiC MOSFET Power Module

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***Abstract*— A high frequency SiC MOSFET-based three-phase, 2-level power module has been designed, simulated, assembled and tested. The design followed a built-in reliability approach, involving extensive finite-element simulation based analysis of the electro-thermo-mechanical strain and stress affecting the switch during both manufacturing and operation: structural simulations were carried out to identify the materials, geometry and sizes of constituent parts which would maximize reliability. Following hardware development, functional tests were carried out, showing that the module is suitable for high switching frequency operation without impairing efficiency, thus enabling a considerable reduction of system-level size and weight.**

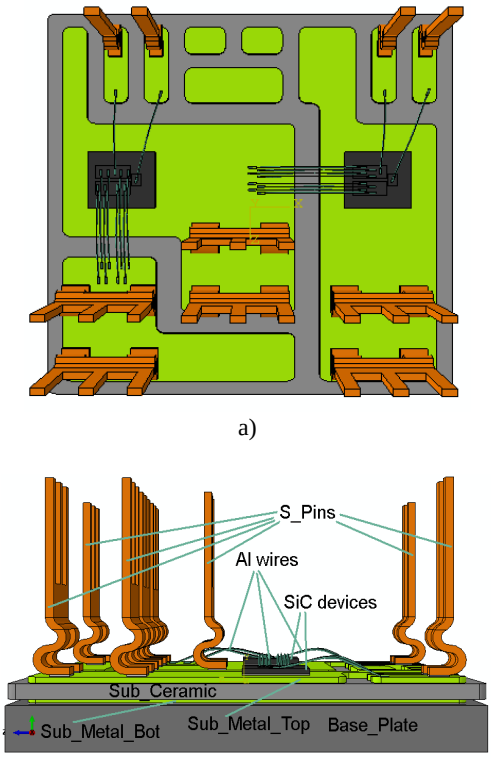
Keywords*— *SiC MOSFET, multi-chip power modules, reliability.

I. Power Module Design

A 1.2 kV SiC-MOSFET based three-phase half-bridge power module was designed, specifically for avionic applications, where improved gravimetric and volumetric power density and efficiency are highly appreciated.

The structure of one phase switch is shown in Fig. 1, with indication of assembly layers and location of interconnection pins. Each switch allocates two SiC MOSFETs, which are soldered on the substrate top metallization (Sub_Metal_Top in Fig. 1 b)) together with the power and drive terminals (S-Pins); the substrate bottom metallization is soldered onto the module base-plate. All the solder joints are made of eutectic tin-silver (Sn-3.5Ag) solder of constant 100 µm thickness. Because this module does not target specifically high-temperature applications, aluminum (Al) bond-wire were used for interconnections to the device top-side, with diameter of 125 µm.

Two types of substrates commonly used in the construction of power modules have been considered, namely Aluminum-Nitride (AlN) and Silicon-Nitride (Si_3N_4). Table I summarizes the main characteristics of interest for the two materials: Si_3N_4 has higher flexural strength than AlN and is thus typically processed in thinner layers than AlN for use in building power modules; this also implies that, although Si_3N_4 has a lower thermal conductivity than AlN, the equivalent thermal resistance of the substrates is comparable if the difference in thickness is taken into account. Here, both experiment and simulations are used to inform the choice on most reliable solution.



a)

b)

Fig. 1. One-phase SiC switch: a) top view, b) side view.

TABLE I
Thermo-Mechanical Characteristics of Substrate Ceramics

	Thermal Conductivity (W/m·k)	Flexural Strength (MPa)	Fracture Toughness (MPam1/2)	CTE (ppm/degree-C)
AlN	170	400	2.7	4.5
Si_3N_4	60	850	5.0	2.7

Preliminary experimental testing was carried out on batches of the two types of assemblies, with different thicknesses of copper tracks deposited onto them. The tiles were subjected to passive thermal cycling and Cu tracks detachment/peel-off was used as an indication of failure. The results are summarized in Table II and give a clear indication that Si_3N_4 tiles can withstand a much higher number of cycles before degradation and failure intervenes. Also, it is interesting to note that the thicker the Cu tracks, the shorter the number of cycles to failure.

TABLE II
SIMULATION CASES WITH CONSIDERATION OF SUBSTRATES AND BUMP SHAPES

		Cu Plate Thickness			
		0.2t	0.3t	0.4t	0.5t
Ceramic Substrate Material	AlN 0.635t	300	200	Failure	Failure
	Si_3N_4 0.32t	>3000	>3000	>3000	>3000

Condition: -40deg.C (30 min.) to 125deg.C (30 min.)
Failure: Cu plate detached after brazing

Finite element (FE) modeling and simulation are employed to investigate the effects of the type and the thickness of substrate and base plate used on the entity of the maximum thermo-mechanical stress and its distribution. Simulations target the analysis of the thermal and thermo-mechanical performance of the assembled power module. The considered simulation cases are listed in Table III.

TABLE III
SIMULATION CASES WITH CONSIDERATION OF SUBSTRATES AND BUMP SHAPES

No	Sub Ceramic Thickness	Sub Metal Bot Thickness	Sub Metal Top Thickness	Base Plate Thickness
A1	1 mm AlN	0.3 mm Cu	0.4 mm Cu	3 mm AlSiC-9
A2	1 mm AlN	0.3 mm Cu	0.4 mm Cu	3 mm AlSiC-12
A3	1 mm AlN	0.3 mm Cu	0.4 mm Cu	2 mm AlSiC-9
A4	0.635 mm AlN	0.3 mm Cu	0.4 mm Cu	2 mm AlSiC-9
A5	0.635 mm AlN	0.2 mm Cu	0.3 mm Cu	2 mm AlSiC-9
A6	0.635 mm AlN	0.3 mm Cu	0.3 mm Cu	2 mm AlSiC-9
B1	0.3 mm Si_3N_4	0.3 mm Cu	0.4 mm Cu	3 mm AlSiC-9
B2	0.3 mm Si_3N_4	0.3 mm Cu	0.4 mm Cu	3 mm AlSiC-12
B3	0.3 mm Si_3N_4	0.3 mm Cu	0.4 mm Cu	2 mm AlSiC-9
B4	0.3 mm Si_3N_4	0.2 mm Cu	0.3 mm Cu	3 mm AlSiC-9
B5	0.635 mm Si_3N_4	0.3 mm Cu	0.4 mm Cu	2 mm AlSiC-9
B6	0.635 mm Si_3N_4	0.2 mm Cu	0.3 mm Cu	2 mm AlSiC-9
B7	0.635 mm Si_3N_4	0.3 mm Cu	0.3 mm Cu	2 mm AlSiC-9

The first one is 0.4mm and 0.3mm thick active brazed Cu on both sides of 1 mm or 0.635mm thick AlN tile. The second one is 0.4 mm and 0.3mm thick or 0.3mm and 0.2mm active brazed Cu on both sides of 0.3mm or 0.635mm thick Si_3N_4 tile, respectively. Also, two types of base plate materials have been considered: AlSiC-9 and AlSiC-12 composites. For each of the two composites, two thicknesses of 3 mm and 2 mm for the Base_Plate were selected and compared in order to reduce the stress/strain accumulation within the solder joints.

The characteristics of the material used for the solder layer, Lead (Pb)-Tin (Sn)-Silver (Ag) solder of the composition 62Pb36Sn2Ag, are summarized in Table IV.

TABLE IV
SOLDER PROPERTIES

Liquidus Temperature (°C)	179
Density (gm/cm3)	8.41
Electrical Conductivity (1.72μΩ-cm (% of IACS))	11.9
Thermal Conductivity @85°C (W/cm-°C)	0.5
Thermal Coefficient of Expansion @20°C (PPM/°C)	27
Tensile Strength (PSI)	7000
Shear Strength (PSI)	7540
Specific Heat Capacity (J/g-°C)	0.167

Modeling and simulation were carried out using well-established commercially available tools (e.g., Abaqus, Ansys). Fig. 2 a) shows the numerical structural model (meshed) of the switch: the largest brick element is 0.5×0.5×1.5mm, and the smallest is 0.5×0.25×0.025mm. Here, the largest brick element is 0.5×0.5×1.5mm, and the smallest is 0.5×0.25×0.025mm. S4R shell elements of 0.5×0.5mm or 0.5×0.25mm in size were also used to discretize the nickel-phosphorous (NiP) finishing on the surfaces of the substrates, and in both the Al and Ni metallization on two sides of the MOSFETs respectively.

The assembly was first subjected to a predefined temperature profile of 221°C down to 25°C for 3 min to simulate the stress and strain developed during the reflow process. In this stage, all the Al wire bonds were deactivated and therefore no strain/stress was developed on them. Power losses of one MOSFET are shown in Fig. 2 b). These losses were considered as heating sources to simulate the thermal performance of the assembly during a realistic mission profile. They were also taken in account in the heat exchange boundary condition. For this boundary condition, a heat exchange coefficient of 5000W m^{-2} K^{-1} was applied to the bottom surface of the base plate, corresponding to typical heat-sink cooling conditions in our lab experiments. The temperature field obtained from the thermal simulation was used as input to simulate the development of stress/strain in the assembly during two cycles of the mission profile. Thermal and mechanical properties of all the materials used in the thermo-mechanical simulation were taken from either references [1-3] or the datasheets of the materials commercially available. Chaboche's plastic model was

used to describe the mechanical properties of both the Cu and Al. The properties of Al were applied to both the Al wire bonds and the Al metallization on the front side of the MOSFETs. Anand's creep model was used to describe the mechanical properties of the Sn-3.5Ag solder alloy.

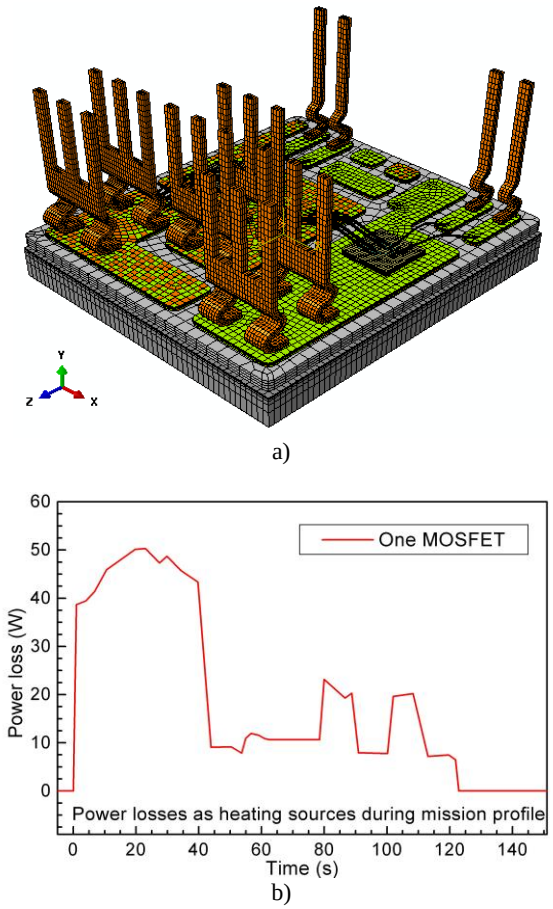


Fig.2. a) Representative meshing system to discretize the designed switch module. b) Power loss of one MOSFET during a realistic mission profile.

II. THERMO-MECHANICAL SIMULATION

For all simulation cases during the mission profile, the highest junction temperature was observed on one MOSFET at 23.01s. The simulation shown is mainly concerned with the stress and strain developed in all solder joints. Simulation results reveal that the maximum von Mises stress in the solder joint between the substrate and the base plate are larger than those in the two solder joints used for attaching the two SiC MOSFETs on the substrate. The maximum creep strain accumulation in the former solder joint is significantly larger than that in the latter two solder joints after the first cycle of the mission profile. However, and depending on the simulation cases, the maximum creep strain accumulation in the former solder joint may be higher or lower than that in the latter two solder joints after the second cycle of the mission profile.

Fig. 3 shows the von Mises stresses and creep strains obtained from simulations in all the solder joints for case A1 after two cycles of the mission profiles. Table V compares the simulation cases for the highest junction temperatures of the MOSFETs and the maximum von Mises stress and creep strain developed in the solder joint between the substrate and the base plate. In Table V, $T_{J,max}$ is for the highest junction temperature of the MOSFETs during the mission profile; S_{max0}, S_{max1} and S_{max2} represent the maximum von Mises stress and ε_{max0}, ε_{max1} and ε_{max2} represent the maximum creep strain in the solder joint of the as-reflowed assembly and the same one after one and two cycles of the mission profile; and $\Delta\varepsilon_{max1}=\varepsilon_{max1}-\varepsilon_{max0}$, $\Delta\varepsilon_{max2}=\varepsilon_{max2}-\varepsilon_{max1}$.

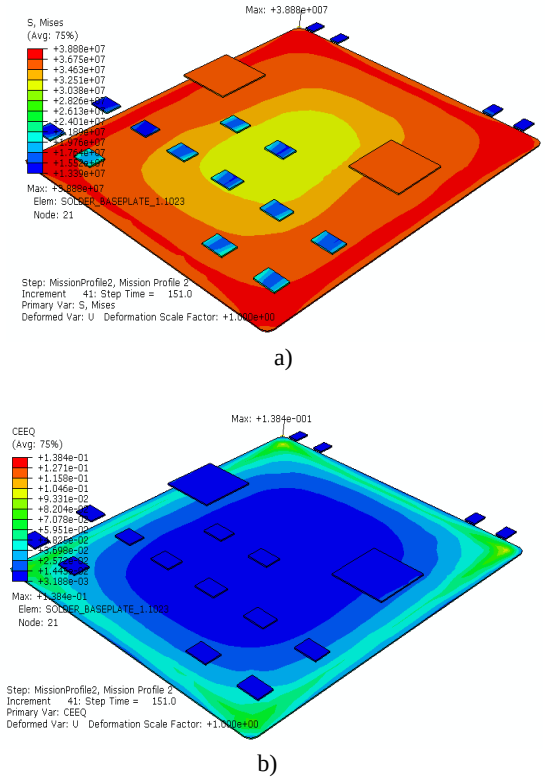


Fig. 3. Simulation results of (a) von Mises stresses and (b) creep strains within all solder joints for simulation case A1 after two cycles of the mission profile.

According to these results, the best design is achieved when the base-plate is 2mm thick AlSiC-9 and the substrate is AlN-based with 0.635mm thick AlN tile (case A4). In this case, the highest junction temperature of the MOSFET is only 0.6°C higher than that in simulation case A1; however, the maximum creep strains and creep strain accumulations dominating the reliability of the critical solder joint in the module would be significantly lower than those in the other simulation cases.

In view of both experimental and simulation results, however, and more particularly due to the relatively small difference in the stress and strain values for the

TABLE V
COMPARISON OF THE HIGHEST JUNCTION TEMPERATURES OF THE MOSFETS AND THE MAXIMUM VON MISES STRESS, CREEP STRAIN AND CREEP STRAIN ACCUMULATION IN THE SOLDER JOINT BETWEEN THE SUBSTRATE AND BASE PLATE FOR THE 13 SIMULATION CASES

Case	$T_{J,MAX}$ (K)	S_{max0} (MPa)	S_{max1} (MPA)	S_{MAX2} (MPa)	ε_{MAX0} (%)	ε_{MAX1} (%)	ε_{MAX2} (%)	$\Delta\varepsilon_{MAX1}$ (%)	$\Delta\varepsilon_{MAX2}$ (%)
A1	363.2	42.6	39.5	38.9	12.65	13.40	13.84	0.75	0.44
A2	363.9	44.2	41.6	40.7	18.84	19.67	20.17	0.83	0.50
A3	363.8	41.0	38.2	37.6	6.87	7.25	7.52	0.37	0.27
A4	363.8	41.3	37.9	37.4	6.83	7.10	7.23	0.27	0.13
A5	365.6	41.3	38.6	38.1	7.65	8.13	8.41	0.48	0.28
A6	364.8	40.8	37.9	37.4	7.07	7.35	7.49	0.28	0.14
B1	366.4	42.6	39.1	38.4	10.96	11.80	12.26	0.84	0.46
B2	367.4	44.2	40.5	39.9	16.79	17.66	18.12	0.87	0.46
B3	367.6	41.3	38.1	37.6	7.32	7.70	8.01	0.38	0.31
B4	368.7	43.0	39.6	41.2	12.10	12.88	13.32	0.78	0.44
B5	370.6	42.5	39.0	38.4	8.98	9.61	9.98	0.63	0.37
B6	373.4	42.4	39.5	39.0	10.25	10.88	11.27	0.63	0.39
B7	372.6	42.5	39.0	38.4	9.17	9.81	10.19	0.64	0.38

simulation results using AlN and Si_3N_4 (e.g., case A1 in comparison with case B3), Si3N4 substrates were retained as the best solution for built-in reliability module development.

III. HARDWARE DEVELOPMENT AND TEST

A. Development

Fig. 4 a) shows details of the assembled switches and module. The module of Fig. 4 b) was later filled with a silicone-based dielectric material to provide the required isolation and insulation. Finally it was fully encapsulated by using a plastic lid leading to the final product of Fig. 4 c). The final module as assembled for both functional and reliability testing weighs 126.5g ±0.5g. In view of the specified goal of lightweight development, this is a very satisfactory results, competitive with presently upcoming commercial solutions. A noteworthy feature of the module is the complete separation of the power and driving terminals and current loops. All power terminals were finally implemented with single connectors, doubled to reduce parasitic inductance and enable high switching frequency.

The module has been subjected to both functional testing in inverter operation and to temperature cycles for technology validation. Here, the results of functional testing are reported to demonstrate the high frequency capability and good thermal performance. Reliability tests are still ongoing at the time of submission.

B. Test

A flexible test setup was designed to test a number of modules that have been manufactured. The setup comprises of four electrolytic capacitors (350V, 3.3mF each) with discharge and balancing resistors (47kΩ each), and the SiC module power pins are mounted directly onto the power plane. The schematic is shown in Fig. 5. Fig. 6 shows a picture of the test setup.

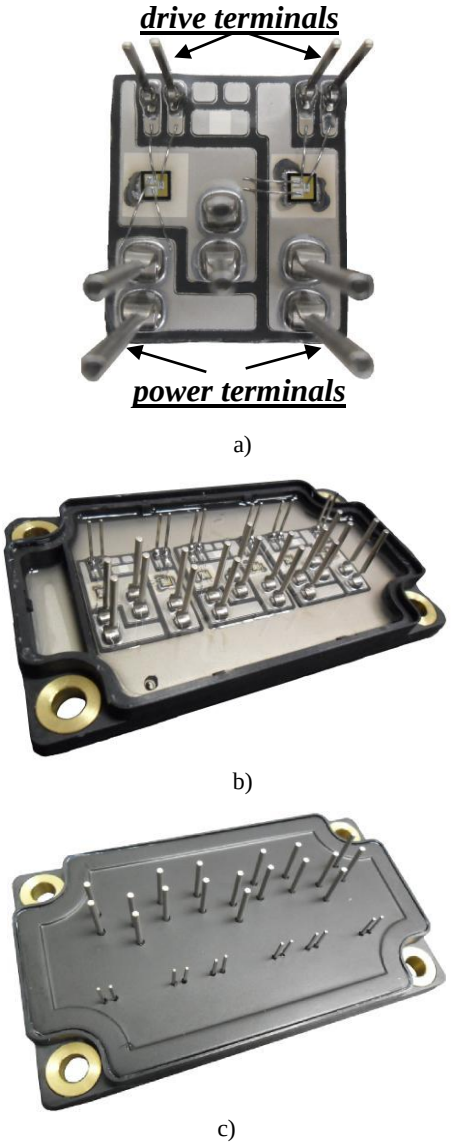


Fig. 4. Assembled switches a), full power module b) and encapsulated device c).

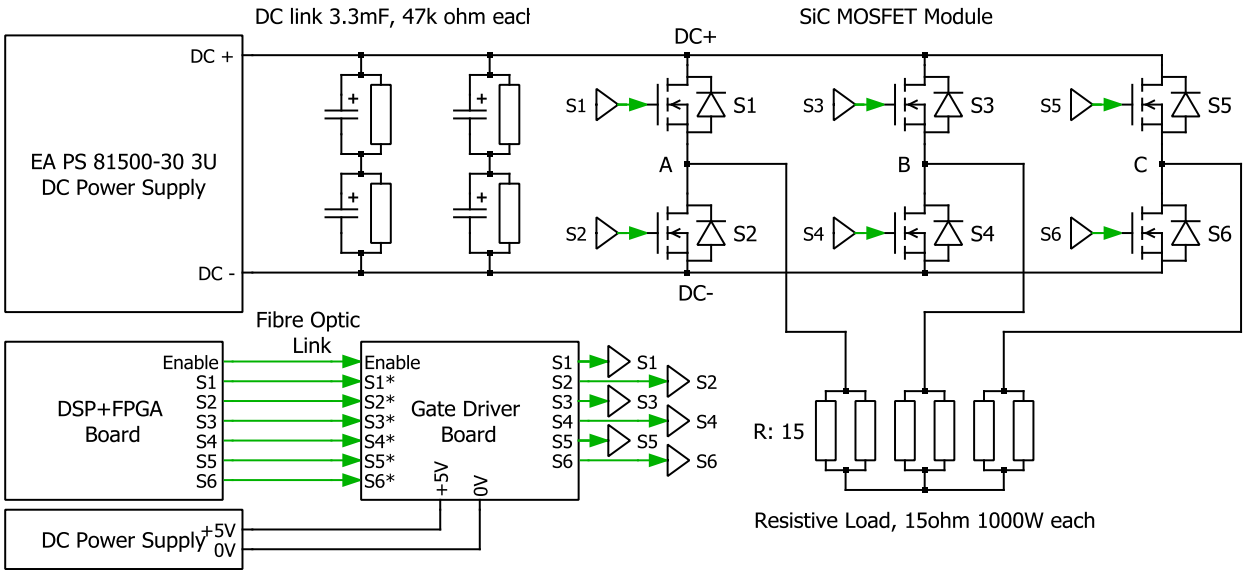


Fig. 5. Schematic of the test circuit.

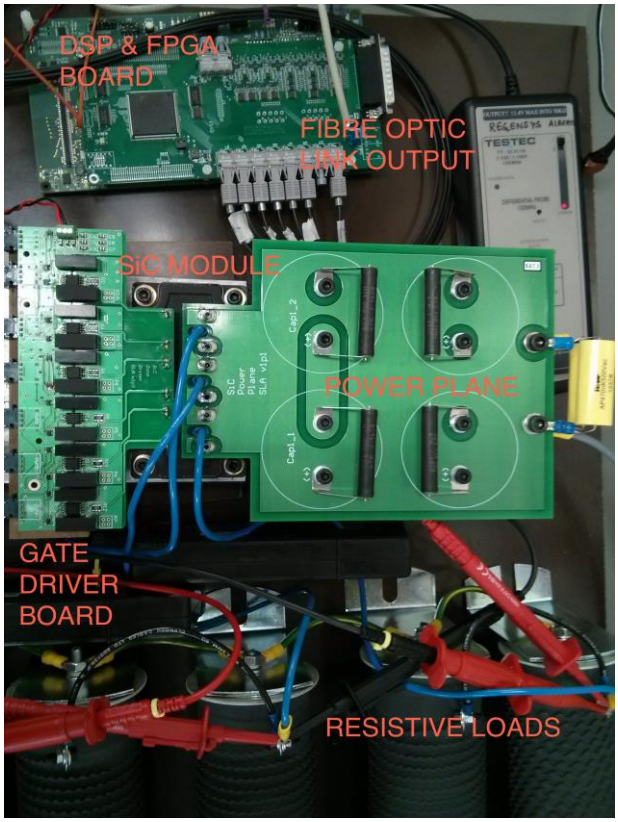


Fig. 6. Photograph of the test set-up.

The inverter was tested in open loop; the necessary PWM drive signals are generated by a DSP and FPGA control platform with programmable dead-time values. The PWM signals are transmitted to a gate driver board, which is mounted directly onto the SiC module gate pins, through fiber optic cables in order to minimize the noise interference at high switching frequencies. An isolated gate drive IC supplies +22V to turn-on and -3.1V to turn-off each individual SiC MOSFET. The input DC link voltage is 540V to represent the DC bus in an avionic systems. The inverter was tested at full load (6kW) and half load (3kW) conditions. The output inductive filter was 3 mH. Output phase-to-neutral RMS voltage is set to 115V with 50Hz fundamental frequency. Tests were run at increasing switching frequencies: 5, 10, 20, 40, 60, 80 and 100 kHz. Fig. 7 shows the three phase current components for a switching frequency of 5 kHz.

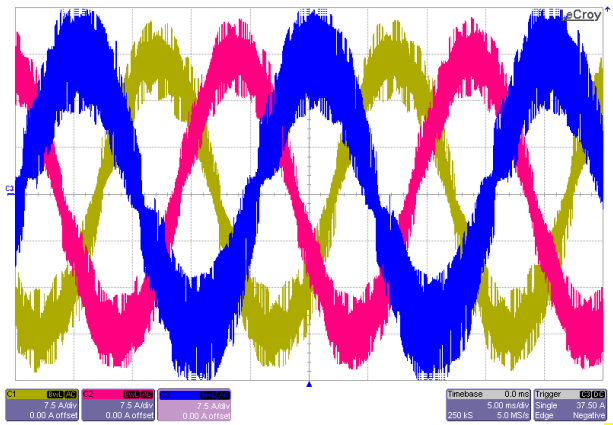
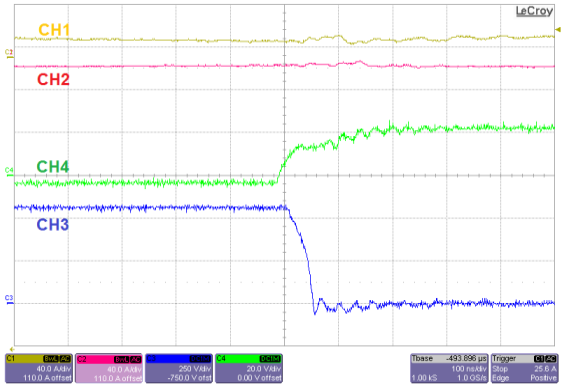
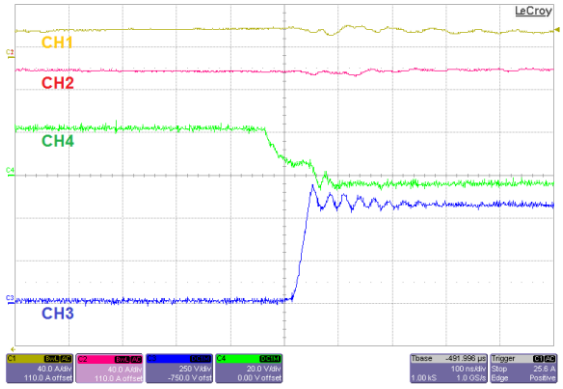


Fig. 7. Phase current waveforms at a switching frequency of 5 kHz.

The output phase voltage and current, and the drain-source (V_{ds}) and gate-source voltage (V_{gs}) waveforms of each SiC MOSFET were also captured. The turn-on and turn-off waveforms of the SiC MOSFET at full load and 100 kHz switching frequency are shown in Fig. 8 a) and b), respectively. These waveforms show that the turn-on and turn-off times of the power switches are less than 60ns at full load.



a)



b)

Fig. 8. Turn-on, a), and turn-off waveforms, b), at f_{sw}=100 kHz, full-load (CH1 and CH2: Current in phase A and B, 40A/div, CH3:V_{ds}=250V/div, CH4:V_{gs}=20V/div, timebase=100ns/div).

In a final test, we removed altogether the inductive filter from the load. Fig. 9 shows the output current waveforms of all three phases at full load and 100 kHz switching frequency in this condition. Although the load at the output of the converter is purely resistive, due to leakage inductance at the output cables and resistors, and high switching frequency, the output phase currents become continuous. Clearly, the ripple is not contained, but these measurements give a very clear indication of the dramatic reduction in inverter volume and size which can be enabled by the high-frequency SiC power module.

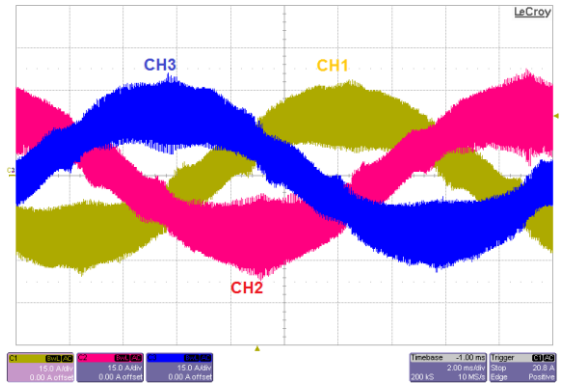


Fig. 9. Output current waveforms at f_s=100 kHz, full-load (CH1= Phase A current 15 A/div, CH2= Phase B current 15 A/div, CH3= Phase C current 15A/div, timebase= 2ms/div).

Finally, Fig. 10 reports the measured efficiency at full load as a function of the switching frequency. A decrease of only 2.5% (i.e., 15 W) is measured for a twentyfold increase in the switching frequency (from 5 to 100 kHz), which is directly attributed to the SiC device characteristics [4].

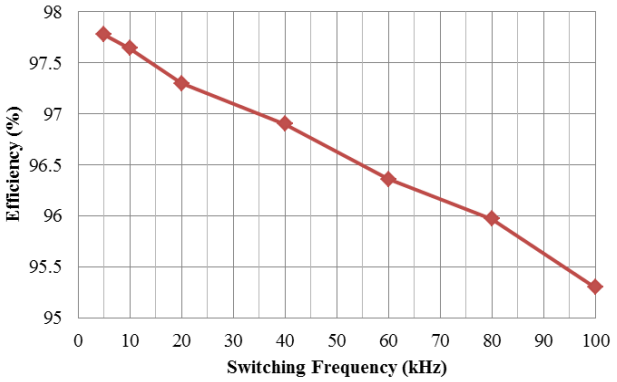


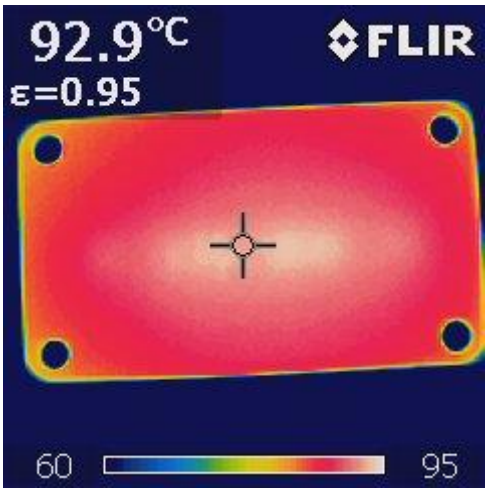
Fig. 10. Efficiency curve of power module at 6 kW output power.

To complete experimental characterization, the SiC power module was dismounted from the heat-sink and the temperature at the baseplate was measured under different operational conditions. To avoid failure, the maximum allowed baseplate temperature was around 90 ºC. This corresponded to the following test conditions: P_{OUT}=2.5 kW at f_s=5kHz and P_{OUT}=1.5kW at f_s=40 and 80 kHz. The baseplate temperature distribution corresponding to these test conditions is given in Fig. 11 a), b) and c). All results highlight a very even temperature distribution, with maximum at the center in line with the expectations, and the capability of the module to work properly and efficiently with noticeable base-plate temperatures, that is, minimum cooling requirements, at high switching frequencies and power levels.

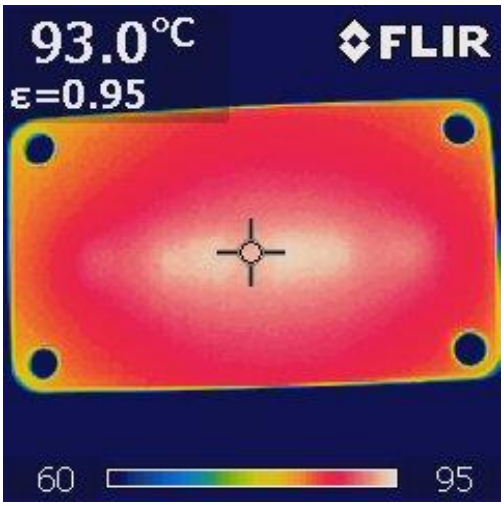
IV. CONCLUSION

In this paper, the design, the thermo-mechanical modeling using finite element analysis and, simulation and experimental results of a lightweight SiC MOSFET module are presented. Simulation results using finite element suggests that the best design is obtained when the Base_Plate is based on AlSiC-9 with a thickness of 2mm and the substrate is AlN-based with 0.635mm thick AlN tile. The module has been tested successfully at full and half load operating conditions using a switching frequency of up to 100 kHz. Experimental results show that the designed power module successfully operates in a wide switching frequency range with high-efficiency at full-load and half-load operating conditions, making it ideal for all applications which prize reduction of system size and weight (e.g., avionic, automotive). In view of the dramatic reduction in output filter size that Such frequency increase enable, the developed SiC power

module must be regarded as a solution enabling optimum trade-off choices in inverter development.



a)



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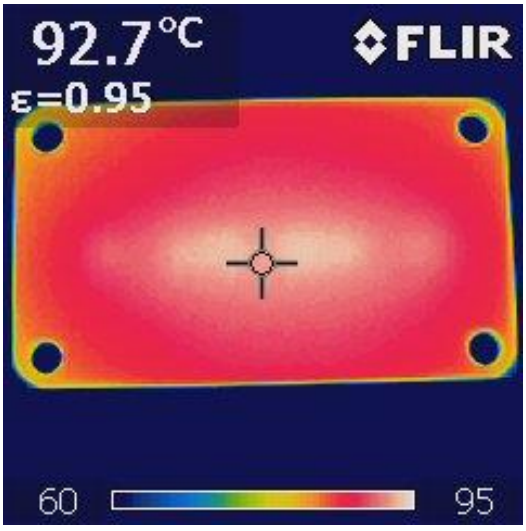

c)

Fig. 11. Infrared thermal mapping of the module baseplate under different operational conditions: P_{OUT}=2.5 kW and f_s=5kHz, a); P_{OUT}=1.5kW at f_s=40 kHz, b); P_{OUT}=1.5kW at f_s=80 kHz, c).

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