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RESEARCH ARTICLE

Minimising bulk lifetime degradation during the processing of interdigitated back contact silicon solar cells

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Abstract

In this work, we develop a fabrication process for an interdigitated back contact solar cell using BBr_3 diffusion to form the p^+ region and $POCl_3$ diffusion to form the n^+ regions. We use the industry standard technology computer-aided design modelling package, Synopsys Sentaurus, to optimize the geometry of the device using doping profiles derived from electrochemical capacitance voltage measurements. Cells are fabricated using *n*-type float-zone silicon substrates with an emitter fraction of 60%, with localized back surface field and contact holes. Key factors affecting cell performance are identified including the impact of e-beam evaporation, dry etch damage, and bulk defects in the float zone silicon substrate. It is shown that a preoxidation treatment of the wafer can lead to a 2 ms improvement in bulk minority carrier lifetime at the cell level, resulting in a 4% absolute efficiency boost.

KEYWORDS

defects, float-zone, IBC, RIE, silicon

1 | INTRODUCTION

The highest single-junction silicon wafer solar-cell power conversion efficiencies reported to date were achieved with the interdigitated back contact (IBC) architecture. Recently, Kaneka Corporation used an IBC heterojunction design to set a new single-junction silicon world record efficiency[1] of 26.7%. Back contact architectures eliminate front surface grid shading, thus potentially leading to higher short-circuit currents. As front surface doping is no longer necessary, a wider range of front surface texturing and light-trapping schemes are possible (e.g. nanoscale texturing).[2,3] Furthermore, a back-contact architecture is well-suited for mechanically stacked tandem cells with emerging materials such as perovskites. The fabrication of an archetypal IBC cell consists of local diffusion of boron into the back surface, followed by local diffusion of phosphorus, leading to alternating (interdigitated) *p*- and *n*-type regions[4]; see Figure 1. The selective collection of the electrons and holes is optimized based on the diffusion length of the carriers as well as the passivation quality of *p*- and *n*-type regions.

A high collection efficiency of electrons and holes is vital for achieving high efficiencies, and therefore, the bulk minority carrier lifetime (or diffusion length) must be sufficiently long to ensure that a very high proportion of carriers reach their respective contacts. For IBC architectures where there are, in general, many high-temperature processes, the material must maintain high bulk lifetimes throughout cell fabrication. In this regard, float-zone (FZ) silicon is an attractive material for back junction solar cells, particularly in the laboratory, where exceptionally high lifetimes can be achieved owing to the high purity of the material.[5] However, recent work by Grant *et al* has demonstrated that FZ silicon contains defects, which are incorporated during crystal growth.[6,7] In as-grown samples, the defects are essentially latent, but they become activated as recombination centres upon heat-treating FZ silicon at temperatures between 450°C and 750°C. Thus, although the as-received lifetime is very high, the lifetime can

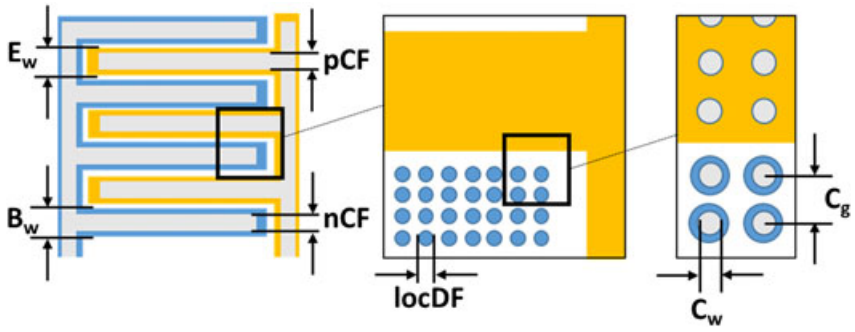

FIGURE 1 Schematic (top view) of the interdigitation in an interdigitated back contact cell, with boron-doped emitter fingers (in yellow), localised phosphorus-doped back surface field (BSF; in blue), and localised contact holes (in grey). The dimensions optimized using the TCAD model are labelled and include width of the p^+ emitter (E_w) and n^+ BSF (B_w) regions; the contact finger widths for n^+ region (nCF) and p^+ region (pCF); the diameter of the local diffusion hole size for the BSF (locDF) and contact hole (C_w), as well as pitch (C_g) for both. [Colour figure can be viewed at wileyonlinelibrary.com]

be degraded during thermal processing by several orders of magnitude. The defect characteristics have been attributed to the growth conditions of the silicon crystal, where the crystals are grown under vacancy rich mode (fast growth rate) usually with the addition of nitrogen doping (10^{14}–10^{15} cm^{-3}) to suppress void formation. It is therefore conceivable that vacancies form part of the recombination active defects. While such defects are present in all commercially available FZ silicon, Grant *et al* have developed a means to annihilate these grown-in defects, thereby making FZ silicon more thermally stable and consequently more suitable for high-efficiency solar cell architectures. This treatment (referred to as "bulk FZ treatment") consists of a dry oxidation for at least 30 minutes at 1050°C, which has the effect of out-diffusing vacancies and/or annihilating the vacancies by injection of interstitials during the dry oxidation.[8,9] In contrast, lower cost Czochralski (Cz) silicon wafers typically contain much higher oxygen concentrations and thus oxygen related defects, which can degrade the lifetime upon thermal processing and during cell operation, thereby making Cz silicon a more challenging material to use for IBC architectures.[10-12]

In this work, we fabricate IBC cells using FZ wafers to investigate the influence of the bulk FZ treatment from the work of Grant *et al* on the cell efficiency. The cells were designed to have a planar front surface to facilitate their use in future planned studies on novel antireflection and light-trapping treatments and on silicon-based tandem cell development. We also present findings on cell fabrication process improvements developed during the study, including overcoming problems caused by reactive ion etching (RIE) and by electron-beam evaporation of metal contacts. We first use Sentaurus technology computer-aided design (TCAD)[13] to design the geometry of the device prior to fabrication. This determines the optimum emitter finger width and fraction as well as the diameter of localized back surface field (BSF) and contact holes. Devices are then fabricated based on this design using a 4-stage lithography process, with various thermal, deposition, and etch steps. Photoluminescence (PL) imaging, transient or quasi-steady-state photoconductance (PC) lifetime measurements, and current-voltage (*I-V*) characteristics are used to identify key degradation effects in the fabrication process. Additional *I-V* measurements are used to quantify performance improvements when defects are treated. Finally, the TCAD model with input from our experimental results is used to identify how the devices can be further improved and to predict efficiencies achievable with this approach.

2 | CELL DESIGN USING TCAD

TCAD modelling was used to optimize the cell geometry. The design was simulated using Sentaurus device, which calculates the current-voltage characteristics using the Poisson equation coupled to the drift-diffusion transport equations.[13] Bulk and surface recombination mechanisms were both taken into account. For the surfaces, both chemical and field-effect passivation were considered. The 1-sun carrier generation profile used is calculated using OPAL2.[14] The doping profile for the emitter and BSF is defined by a Gaussian decay with a set peak dopant concentration and junction depth. The width of the half unit cell is 500 μm. The number of localized diffusions is based on the remaining area after the width of the emitter, and radius of the localized diffusion is taken into account. The parameters for the cell are shown in Table 1.

A 3-dimensional schematic of the unit cell of the IBC model defined in TCAD is presented in Figure 2A. We first optimized the width of the emitter (E_w) and BSF (B_w) regions, and therefore the emitter fraction. Figure 2B plots the efficiency as the widths of the doped regions are varied between 50 and 250 μm (overlaid, numbered diagonal lines indicate the emitter fraction). In the case of the BSF, the width refers to the area in which localised diffusions were used (see Figure 1).

TABLE 1 Input parameters for Sentaurus TCAD model sweep

Cell parameter	Value
Cell thickness	280 μm
Emitter width	50-250 μm
BSF diameter / pitch	10-120 μm / 20-125 μm
Contact diameter / pitch	10 μm / 20-125 μm
Bulk doping	1.5×10^{15} cm^{-3}
Emitter doping peak/junction depth	1×10^{19} cm^{-3} / 1 μm
BSF doping peak/junction depth	1×10^{20} cm^{-3} / 2 μm
Bulk lifetime	5 ms
Auger model	Altermatt *et al*[17]
Mobility model	Klaassen[18]
Front $S_{n,p}$	10 cm/s
Rear $S_{n,p}$	10 cm/s
Front fixed charge	4×10^{11} cm^{-3}
Rear fixed charge	4×10^{11} cm^{-3}

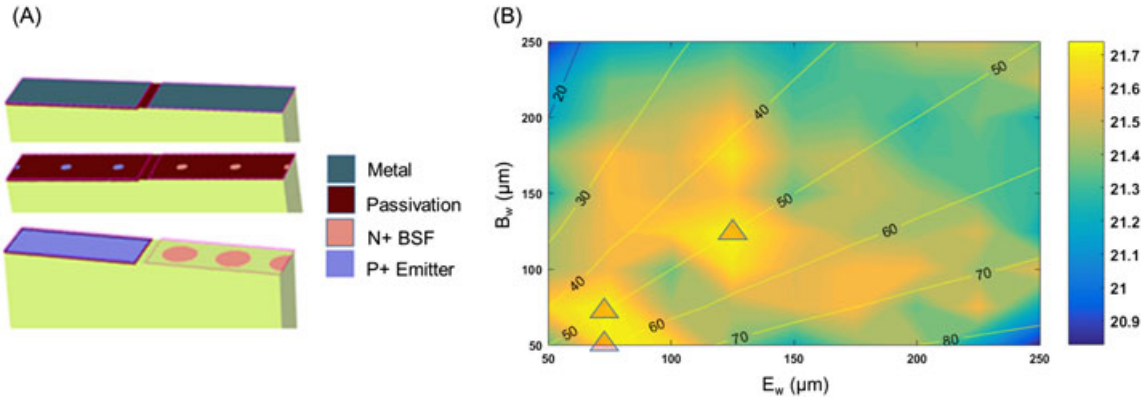

FIGURE 2 A) Schematic of a unit cell used to simulate the interdigitated back contact cell in the 3D technology computer aided design model; B) solar cell efficiency (%) for varying widths of emitter and back surface field regions. The triangles indicate the efficiency optima. [Colour figure can be viewed at wileyonlinelibrary.com]

The contact finger widths (nCF and pCF) were kept the same as the doped region widths, with contact lumped series resistance (R_s) calculated using *Grid*[15] for the varying contact fraction. These results reveal 3 local efficiency optima at emitter/BSF ratios of 75:75, 75:50, and 125:125, as indicated by the overlaid triangles in Figure 2B. These values for the emitter and BSF were then used to find an optimum local diffusion hole size of the BSF (locDF) and an optimum contact pitch (C_g). The results of this are illustrated in Figure 3, where efficiency contours are plotted and different ratios of hole size to pitch are overlaid as diagonal lines. Data for ratios above 50% were omitted as the BSFs overlap and are no longer locally diffused. Increasing the pitch whilst reducing the contact hole size is seen to increase efficiency, predominantly due to improvement in V_{oc}. The optimum cell performance is found for the 125:125 emitter:BSF width ratio, with a pitch size of 100 μm and hole size of 30 μm.

As a validation of the model and comparison to state-of-the-art for diffused junction cells from literature, the optimized geometrical parameters (Geo-A) established in this work were compared against that of the IBC work reported in Franklin *et al*[4] (Geo-B), using both Sentaurus TCAD and Quokka. For consistency, the remaining parameters were taken from the IBC cell reported in Fell *et al*.[16] The results are shown in Table 2. The high efficiency potential of the optimized geometry is observed, with a modest gain in V_{oc} compared to the work in Franklin *et al*.[4] Thus, the fabrication process in this work is based on the TCAD-optimized interdigitation design (GeoA) with E_w = 125 μm, B_w = 125 μm, locDF = 30 μm, C_g = 100 μm, nCF = 125 μm, and pCF = 125 μm.

TABLE 2 Performance of cell under Geo-A and Geo-B modelled in TCAD and Quokka

	J_{sc} (mA/cm^{-2})	V_{oc} (mV)	FF (%)	η (%)
Geo-A (TCAD)	42.0	709	83.6	24.9
Geo-B (TCAD)	42.0	705	83.3	24.7
Geo-A (Quokka)	41.6	703	83.9	24.5
Geo-B (Quokka)	41.6	700	83.8	24.4

3 | EXPERIMENTAL METHODS

3.1 | Device fabrication

The device fabrication process is illustrated in Figure 4 and was based on a recipe taken from Franklin *et al*,[4] with the modified interdigitation design from the TCAD study above. Starting substrates were *n*-type FZ wafers (4″, <100>, 1-5 Ω-cm, 280 μm, double-side polished). In all cases, these were initially cleaned using RCA1, RCA2, and a dilute Hydrofluoric (HF) acid solution. Wafers undergoing the bulk FZ treatment were subjected to a double-sided dry oxidation for 30 minutes at 1050°C (1), which was subsequently stripped in HF (2). Processing for treated and control wafers was therein identical. A 230 nm

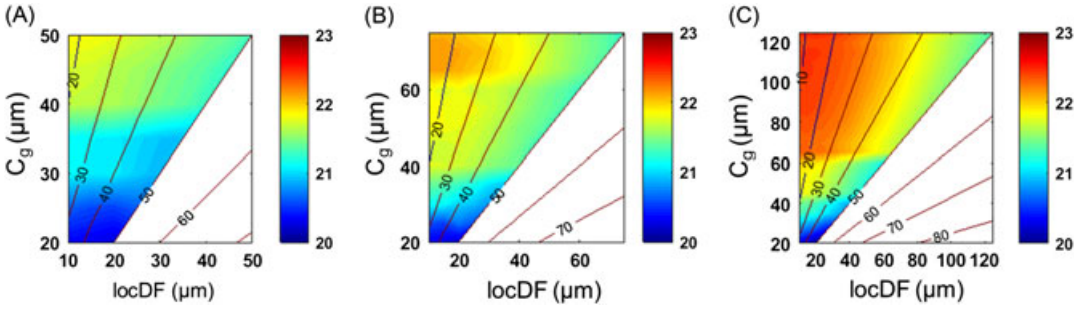

FIGURE 3 Plots of cell efficiency (%) as a function of diameter of localised diffusion (locDF) and pitch (C_g) for the optimum emitter:BSF ratios of A) 75:75; B) 75:50; and C) 125:125, identified by the overlaid triangles in Figure 2B. [Colour figure can be viewed at wileyonlinelibrary.com]

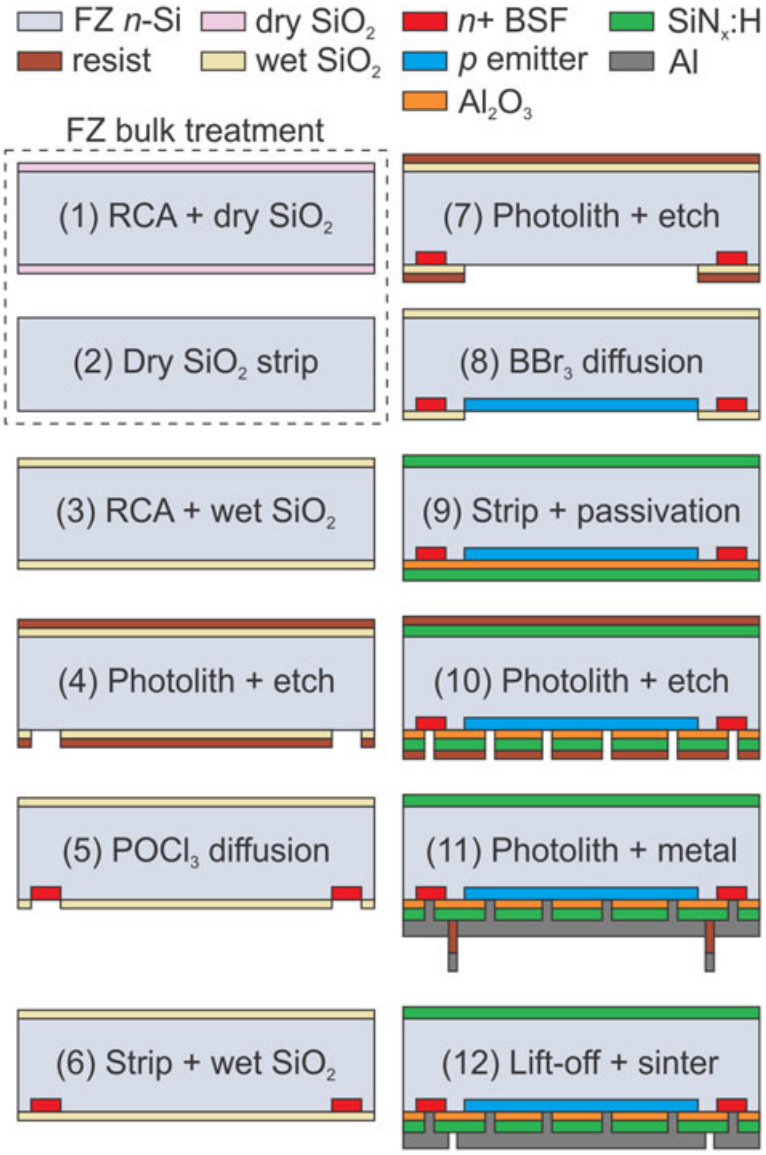

FIGURE 4 Process flow of fabricating the interdigitated back contact cell, with numbers corresponding to the description in Section 3. [Colour figure can be viewed at wileyonlinelibrary.com]

double-sided wet thermal oxide was grown at 1000°C for 45 minutes in a Tempress (TS8603) tube furnace to act as the n^+ (local BSF) diffusion mask (3). Holes for the local BSF were opened in the oxide layer via photolithography and etching, either with a dry, reactive ion etch or a wet etch (4). The positive lithography process for the BSF mask used AZ6632 resist that was spun at 4000 rpm, soft baked for 1 minute at 110°C on a hotplate, exposed with a broadband UV source at a total fluence of 130 mJ/cm^2, developed in AZ826 for 30 s, and finally hard baked at 145°C for 10 minutes on a hotplate. For the dry-etched cells, the subsequent etch step used a plasma process with a CF_4/O_2 ambient (OPT Plasmalab System 100, 35/3 sccm, 165 W, 380 V DC bias, 6 minutes). For the wet-etched cells, a buffered HF (7:1) etch was instead used to transfer the pattern from the resist to the oxide, with an etch time of 270 s at 25°C. As will be shown below, the dry-etch process was abandoned in favour of wet etching due to severe degradation of the bulk lifetime following diffusion. The resist was then removed using acetone and DI water.

Phosphorous doping for the local BSF was undertaken via $POCl_3$ diffusion in a tube furnace (5). This consisted of a pre-diffusion deposition step at 795°C for 25 minutes with a 1:1 $POCl_3$:O_2 gas ratio, followed by a 1-hour drive-in at 920°C. The phosphosilicate glass and n^+ diffusion mask were removed with dilute HF. The creation of the p^+ emitter regions involved growth of a double-sided wet thermal oxide diffusion mask (6), and photolithographic patterning and etching to define the mask openings (7). Parameters for these steps were identical to those described above for the BSF regions. Boron doping was undertaken via tube diffusion using a liquid BBr_3 source (8). This consisted of a deposition step at 850°C with a 1:1 O_2:BBr_3 gas ratio, followed by a drive-in at 920°C and an in situ oxidation to dissolve any potential potential boron-rich layer (BRL) of SiB_6 formed during the process. The borosilicate glass and p^+ diffusion mask were then removed using dilute HF.

With the p^+ and n^+ regions defined on the rear surface, both the front and rear surfaces were passivated (9). First, the rear surface was passivated with a 10-nm layer of Al_2O_3 deposited by atomic layer deposition (ALD; 110 cycles at 200°C, Cambridge Savannah) and capped with a 60-nm layer of PECVD SiN_x:H (Roth and Rau, AK400). The wafer was then dipped in dilute HF to remove the unavoidable Al_2O_3 deposition around the edges of the front surface, before passivating the front surface with a single 80-nm layer of PECVD SiN_x:H. To

activate the Al_2O_3 passivation, the wafer was subsequently annealed in an RTA at 400°C for 10 minutes in a N_2 ambient. The final step of metallization was achieved using 2 lithography steps. In the first step, 10-μm diameter contact holes were opened in the rear passivation stack using the same positive process as for the n^+ diffusion mask, but with the wet etch time increased to 10 minutes to fully clear the Al_2O_3/SiN_x stack (10). A second lithography step, based on a negative resist lift-off process, was then used to define the contact fingers (11). This consisted of a dehydration bake (180°C, 5 minutes), resist spinning (AZ nLOF2035, 3000 rpm for 30 s), hotplate soft bake (1 minute, 110°C), exposure (i-line, 72 mJ/cm^2), development (AZ826, 60 s), and finally a hotplate hard bake (150°C, 5 minutes). With the contact finger mask in place, the wafer was given a brief dip in 7:1 buffered HF for 3 s to remove any native oxide immediately before deposition of a 1 μm thick aluminium layer via e-beam evaporation or thermal evaporation. Metal lift-off was achieved by soaking in acetone and ultrasonic agitation (12). The final step was a 1-minute sinter at 350°C in an N_2 ambient to help lower the contact resistance and form an ohmic contact.

3.2 | Characterization

The devices were characterized using several techniques. Doping profiles of the p^+ and n^+ regions were measured using an electrochemical capacitance voltage tool (WEP, CVP21). The passivation quality and effective minority carrier lifetime were measured quantitatively using transient or quasi-steady-state PC on a Sinton WCT-120 lifetime tester with an inductive coil modified to measure small (2 × 2 cm) samples and qualitatively using PL imaging (BTi LIS-R1) at various stages during fabrication, on the cells themselves and on test wafers. The accuracy of all PL images was improved by applying point spread function deconvolution.[19] Al_2O_3 deposited by ALD was used as a passivation layer to investigate RIE damage. Photoconductance measurements were also performed on some finished cells that were stripped back (HF and alkaline etch) to the bare wafer and re-passivated to investigate bulk lifetimes. All stated carrier lifetimes were extracted from PC measurements at an excess carrier density of 10^{15} cm^{-3}. *I-V* characteristics of cells were measured without temperature control using a triple A class solar simulator (ABET Technologies Sun 3000) with a source measurement unit.

4 | RESULTS

4.1 | Damage from electron beam evaporation of metal contacts

Lifetime degradation was clearly observed in our wafers via PL images taken before and immediately after electron beam evaporation of the metal contacts, including in non-metallized regions. The left half of Figure 5A shows the PL image of a wafer after e-beam evaporation, while the right half shows the same wafer after sintering (350°C, 1 minute, N_2). The imaging conditions (1 s exposure, 1 sun illumination) and colour scales are identical for both. The lack of PL signal in the left-hand image indicates the heavy presence of defects that promote nonradiative recombination, despite a passivation anneal at 420°C prior to metallization. We suggest that this is likely due to X-rays

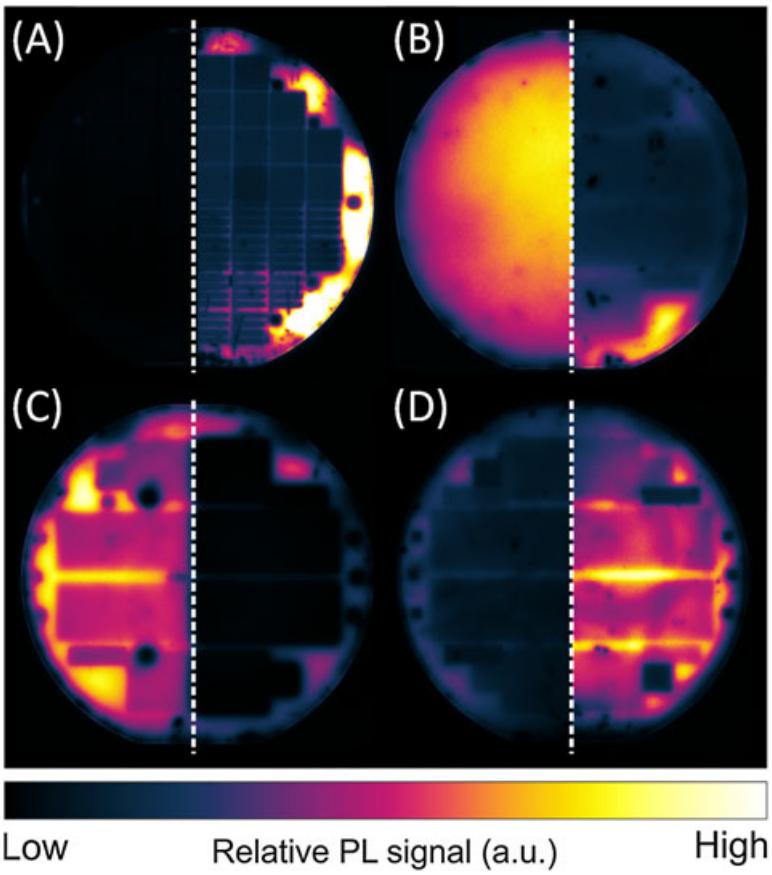

FIGURE 5 A) Photoluminescence (PL) image of wafer pre-sintering (left) and post-sintering (right); B) PL image of wafer pre-RIE (left) and post-RIE (right) etch; C) PL image of wafer using buffered HF etch (left) and RIE etch (right) with proceeding boron diffusion; D) PL image of wafer without (left, cell A) and with (right, cell B) bulk float-zone treatment. All wafers are 4″ in diameter. All images are at 1 sun, with exposure times of 1 s for (A) and 0.1 second for (B), (C), and (D). The relative PL signal is only directly comparable between the 2 samples (left and right) in each frame (A-D). [Colour figure can be viewed at wileyonlinelibrary.com]

emitted during electron-beam evaporation of the aluminium, which are known to cause material degradation in the form of increased oxide traps, charges, and surface states.[20-22] A dramatic increase in the PL counts (relative increase in lifetime and V_{oc}) is seen following the sintering step (right-hand image), particularly for the undiffused and non-metallized region around the perimeter. The sintering treatment appears to reverse some of the damage during electron beam evaporation. Further improvements are expected by replacing electron-beam evaporation with a thermal evaporation process, which would avoid the generation of damaging X-rays during metallization.

4.2 | RIE damage

When dry etching was used for pattern transfer prior to diffusion (steps 4 and 7 in Figure 4), low PL counts were observed in patterned regions of the wafer (Figure 5B, right side), whereas lifetime monitor wafers maintained high PL counts (Figure 5B, left side). These monitors underwent identical diffusion and passivation steps, but did not undergo any patterning. RIE-induced damage of the patterned area was therefore suspected. Shallow implantation of reactive ions as well as lattice damage has been shown to produce surface degradation in silicon.[23-27] The right-hand image in Figure 5C shows a PL image of a test wafer patterned using RIE, then doped using BBr_3 diffusion and finally passivated with ALD Al_2O_3. The patterned areas appear black, indicating that the RIE-induced degradation is dramatically enhanced after subsequent dopant diffusion due to drive-in of the implanted ions deeper into the bulk and the formation of recombination active defects. The process was repeated but with a buffered HF etch used instead of RIE. The PL image of the resulting sample (Figure 5C, left side) illustrates that significant improvements in lifetime are achieved with wet etching compared to the dry etching process. This is supported by PC measurements (Figure 6), which reveal an increase in effective minority carrier lifetime in cells, after passivation anneal and before contact opening (ie, after step 9 in Figure 4), from <100 to 460 μs when RIE was replaced by wet etching for the pre-diffusion pattern transfer steps. The measurements in Figure 6 are aggregated transient measurements, as multiple cells are measured over the sensor region, including the higher lifetime regions in between the cells. Therefore, the lifetime measurements in Figure 6 could be overestimated, and thus the actual bulk lifetime of the cells is likely to be slightly lower than measured.

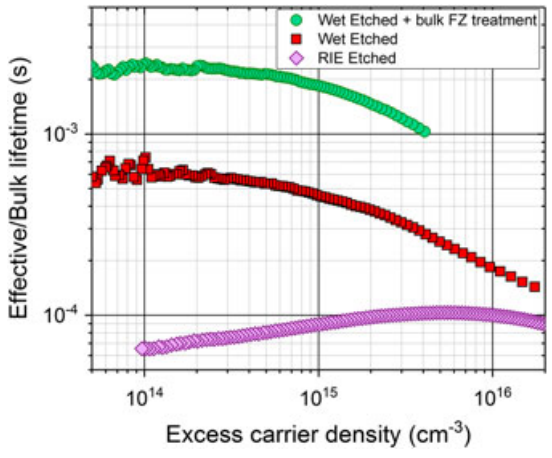

FIGURE 6 Measured effective minority carrier lifetime of cells on float-zone (FZ) 3.2 Ω-cm *n*-type silicon wafer (prior to metallisation) for RIE-etched cells, wet-etched cells (cell A) and wet-etched cells with bulk FZ treatment (cell B). [Colour figure can be viewed at wileyonlinelibrary.com]

4.3 | Bulk defects

Recent literature has shown the presence of grown-in defects limiting the lifetime of commercially manufactured FZ silicon.[6,7,28] Although initially often latent, such defects can become recombination-active and hence reduce bulk lifetime after heat treatments at moderate temperatures (450-750°C). Fortunately, this effect can be removed by annihilating the defects with a high-temperature oxidation (>1000°C) and subsequent oxide strip, thereby stabilizing the bulk lifetime against future thermal treatments. To explore the influence of this bulk FZ treatment on the IBC cell performance, 2 wafers were put through the cell fabrication process in Figure 4; one as-grown (cell A) and a second with the bulk FZ treatment (cell B) of a dry oxidation (1050°C/30 mins) and wet chemical strip. All other processing was identical. Figure 5D shows a PL image of wafers (processed up to step 9 in Figure 4), without (left, cell A) and with (right, cell B) the bulk FZ treatment. The significantly higher PL counts for the treated wafer clearly illustrate the benefit of the bulk FZ treatment on the carrier lifetime. This is supported by PC lifetime measurements that indicate an increase in minority carrier lifetime from 460 μs to 1.8 ms when using wafers subjected to the bulk FZ treatment (Figure 6). This translates to improvement at the final cell level, as shown by the *I-V* characteristics of cells with and without the bulk FZ treatment presented in Figure 7. From this, we can see a 28% relative increase in efficiency (from 14.3% to 18.3% absolute) due to the boost in lifetime conferred by the bulk FZ treatment.

Further investigation of the improvements to bulk lifetime was undertaken. Effective lifetime (τ_{eff}) measurements of the base material (3.2 Ω-cm *n*-type) from 2 IBC cells (without (cell A) and with (cell B) the bulk FZ treatment) were analysed, following dielectric removal and a diffusion etch using HF and 25% TMAH, respectively. The 2 × 2 cm cell

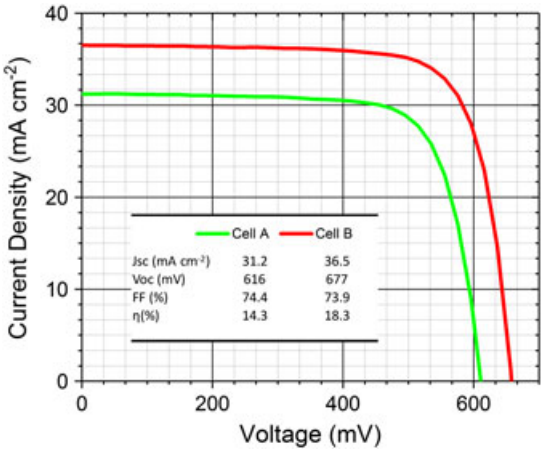

FIGURE 7 One-sun *I-V* measurement for solar cells with (cell B) and without (cell A) bulk float-zone treatment. [Colour figure can be viewed at wileyonlinelibrary.com]

samples were passivated by dipping them in a superacid (SA) solution of trifluoromethanesulfonimide dissolved in dichloroethane (2 mg/mL) as outlined in Bullock *et al*[29] and Grant *et al*.[30] In this case, the passivation is assumed to be conformal (i.e. it also passivates the edges). The SA passivation process occurs at room temperature, so artefacts that occur because of annealing during passivation by conventional dielectrics are avoided.

To investigate/remove edge recombination effects on the 2 × 2 cm IBC cell samples, 2 additional control 270 μm thick FZ 2.6 Ω-cm *n*-type samples were passivated with SA, (1) a 4-inch quarter sample and (2) a 2 × 2 cm sample from the same wafer. From the resulting lifetime results presented in Figure 8, it is evident that SA passivation provides excellent surface passivation, yielding a τ_{eff} of approximately 5 ms on the larger quarter wafer sample (blue circles). In contrast, the smaller 2 × 2 cm control sample yields a τ_{eff} of approximately 4 ms (orange squares), which we attribute to edge recombination effects that do not impact the larger sample. In both cases, however, the surface recombination velocity of SA-passivated silicon is predicted to be 0.65 ± 0.05 cm/s using the *S* parameterisation developed in Grant *et al*.[30] Therefore, to correct for a surface recombination velocity, S, of 0.65 ± 0.05 cm/s (front/back) on both control samples, we have used the following equation[31] (where *W* corresponds to the sample thickness):

$$1/\tau_{eff} = 1/\tau_{bulk} + 2S/W, \quad (1)$$

whereby the dashed blue line in Figure 8 represents the calculated bulk minority carrier lifetime (τ_{bulk}) and the dashed brown line represents the edge affected τ_{eff} of the smaller 2 × 2 cm control sample. Therefore, the difference between the true bulk lifetime (blue dashed line) and edge affected lifetime of the smaller 2 × 2 cm sample (brown dashed line) yields a total "effective" edge recombination velocity (S_{edge}) of approximately 0.7 cm/s.

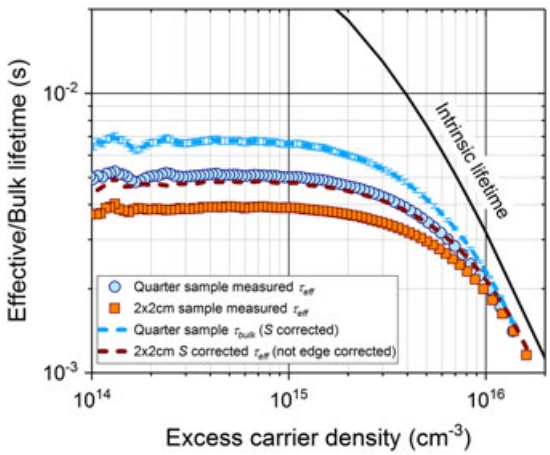

FIGURE 8 Effective/bulk lifetime of FZ 2.6 Ω-cm *n*-type silicon superacid-passivated control samples. Blue circles, τ_{eff} measurement on a quarter sample; blue dashed line, bulk lifetime after correcting for *S* = 0.65 ± 0.05 cm/s; orange squares, τ_{eff} measurement of a 2 × 2 cm sample from the same wafer; brown dashed line, 2 × 2 cm *S* corrected lifetime, but without edge recombination correction. The black line corresponds to the intrinsic limit.[32] [Colour figure can be viewed at wileyonlinelibrary.com]

Turning back to the 2 IBC cell samples, Figure 9A plots the measured effective lifetime of cell A (no bulk FZ treatment) and cell B (with bulk FZ treatment) after removal of the dielectric layer and diffused region and subsequent passivation with SA. Before correcting for both surface and edge recombination, it is evident that cell A has a lower bulk lifetime compared to cell B. However, to ascertain the true bulk lifetime of each cell material, both surface (*S* = 0.55 ± 0.05 cm/s) and edge recombination (S_{edge} = 0.7 cm/s) effects were removed from the measured τ_{eff}. In this case, a lower *S* value is used because the doping of the cell material is lower compared to the control samples of Figure 8, thereby resulting in a slightly lower *S* as outlined in Grant *et al*.[30] The true bulk lifetime of each cell is therefore given by the dashed lines in Figure 9A. As seen in Figure 9A, the actual difference in bulk lifetime is approximately 2 ms once external recombination mechanisms are accounted for (surface and edge).

Finally, to quantify the bulk lifetime reduction during IBC cell fabrication, Figure 9B plots the effective (solid symbols) and bulk lifetimes (dashed lines) of 2 silicon wafers (neither of which were subjected to the bulk FZ treatment), (1) in the as-received condition and (2) after the boron diffusion, which was subsequently etched away prior to SA passivation. From Figure 9B, it is evident that the "as-received" silicon wafer yields a very high τ_{bulk} of >20 ms (τ_{eff} > 10 ms), thereby indicating the material of choice is suitable for IBC cells. However, when a sister silicon wafer underwent a boron diffusion, as outlined in section 3.1, a significant reduction in the bulk lifetime was observed, where τ_{bulk} values of <2 ms were measured. Although the boron-diffused wafer shows a lower τ_{bulk} than the cell wafers shown in Figure 9A, we postulate that the τ_{bulk} of the cell wafers has been preserved by the heavy phosphorus diffusion, in which case some gettering has occurred as previously demonstrated in Zheng *et al*.[33] Although we do not understand the cause for the large reduction in τ_{bulk} following the boron diffusion, we can postulate that some level of contamination has occurred during this process, which could be reduced by removing the BRL by a wet chemical process to prevent any impurities in the BRL being diffused into the bulk material during the traditional in situ oxidation to dissolve the BRL.[18] On the contrary, it is also known that boron diffusions can form dislocations that diffuse into the bulk material, which have shown dependence on the BRL thickness.[34] Therefore, to minimise bulk degradation during cell fabrication, an optimised boron diffusion process, which limits bulk contamination or defect formation, is required and/or a phosphorus diffusion barrier is necessary to minimise any contamination or defect penetration resulting from the boron diffusion (ie, front side n^+ protection layer). In the latter case, the protective n^+ layer can be removed during front-side texturing or immediately before surface passivation.

4.4 | Further analysis with TCAD modelling

To observe the influence of varying lifetime on the IBC cell, we used the TCAD model but replaced the doping profile for the emitter and BSF with ECV measured experimental data, as well as typical fixed charge, interface defect density, and capture cross-sectional data for the dielectric/doped (n, n^+, and p^+) interfaces used for the solar cells. The bulk lifetime was then varied to gauge its influence on efficiency. The same sweep was undertaken when the lumped resistance (calculated

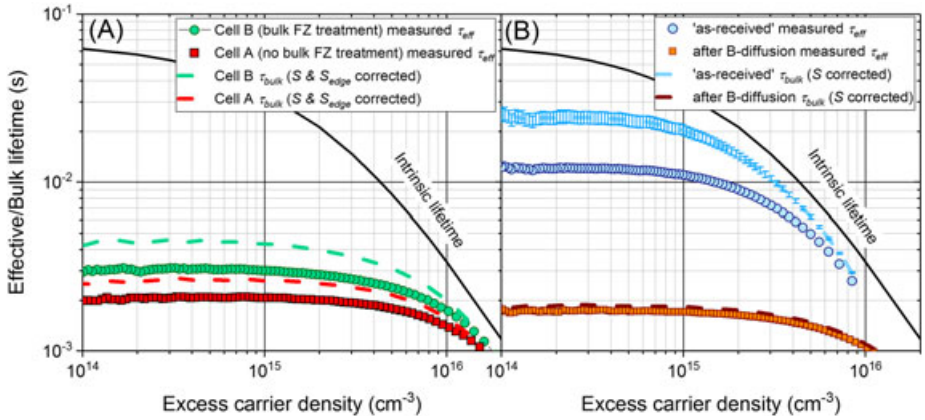

FIGURE 9 Superacid (SA)-passivated effective/bulk lifetime of FZ 3.2 Ω-cm *n*-type silicon. A) τ_{eff} measurement of 2 × 2 cm cell A (no bulk float-zone [FZ] treatment, red squares) and cell B (bulk FZ treatment, green circles). The figure also plots τ_{bulk} for cell A (red dashed line) and cell B (green dashed line) after correcting for both *S* and S_{edge}. B) τ_{eff} (solid symbols) and τ_{bulk} (dashed lines) of two silicon wafers, (i) in the as-received condition and (ii) after a boron diffusion, which was subsequently etched away prior to SA passivation. The black lines represent the intrinsic limit.[32] [Colour figure can be viewed at wileyonlinelibrary.com]

using *Grid*[15]) from the cell was reduced by increasing the thickness of the metal contacts to 4 μm (a key limiting factor in the latest cell fabrication batch is that metal contacts were only 1 μm in thickness). Furthermore, to observe the influence of lifetime under improved passivation, the sweep was undertaken with *S* values reduced to 10 cm/s on undiffused and 100 cm/s for diffused interfaces. Finally, the solar cell efficiency as a function of the bulk minority carrier lifetime is shown when light trapping with ARC is used to increase the carrier generation rate, G_{opt}.

The results are illustrated in Figure 10. This shows that the efficiency significantly increases for lifetime values up to 2 ms and remains roughly constant for higher lifetime values. The same is the case for increased lumped R_s. However, with improved *S* (and enhanced carrier generation), the plateau is shifted to lifetime values exceeding 10 ms. The modelled results show that for cell B, a difference in τ_{bulk} of 2 to 5 ms does not result in any significant change of efficiency performance, unlike our experimental data, which showed a 28% increase.

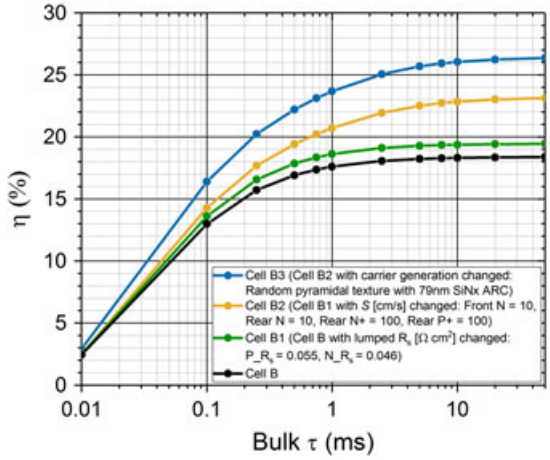

FIGURE 10 Modelled 1-sun solar cell efficiency as a function of the bulk minority carrier lifetime. The solar cell was simulated in Sentaurus TCAD using the current cell design (black), a lower lumped series resistance (green), lower *S* values at all surfaces (yellow), and improved light trapping (blue). [Colour figure can be viewed at wileyonlinelibrary.com]

The lifetime measurements of the cell wafers shown in Figure 6 (cells A and B), however, are significantly lower. We therefore postulate that the significant difference in lifetime between cell A with Al_2O_3/SiN_x passivation (Figure 6) and cell A with SA passivation (Figure 9A) is not limited by surface recombination but rather bulk, which can only occur if the defect present in cell A (passivated with Al_2O_3/SiN_x) is partly removed during the TMAH etch (approximately 5 μm per side) to remove the diffused regions prior to SA passivation. This indicates that some portion of the grown-in defect diffuses towards the surface during the various thermal processes, suggesting that this approach is still not as effective as performing a single high-temperature thermal oxidation prior to IBC fabrication, where the grown-in defect can out-diffuse more efficiently. Our results indicate that vacancies could be the diffusing species, as suggested by Voronkov and Falster[8]; however, the exact nature of the defect and how it diffuses/changes with thermal treatments is still unclear. Nevertheless, our measurements indicate that the bulk lifetime measurements for cell A were overestimates following SA passivation due to the etch-back required to remove the diffused regions of the cell, and thus any bulk defects within approximately 5 μm of the surfaces. It should be noted that the lower lifetimes shown in Figure 6 are also overestimates due to being aggregated transient measurements on whole wafers (not only cell areas; see Section 4). The efficiency improvement observed in the TCAD simulations also highlights the potential for this IBC cell when very high bulk lifetime values can be maintained (approximately 10 ms), with η > 19% for improved R_s, η > 22% for improved *S* and η > 26% with improved light trapping. It should be noted that the model does not take into account edge recombination.

5 | CONCLUSION

Interdigitated back contact cells were fabricated with and without a bulk FZ treatment, with the former showing a 28% relative increase in efficiency (from 14.3% to 18.3% absolute). Minority carrier lifetime analysis of the wafers showed a significant increase in the maximum effective lifetime from 460 μs to 1.8 ms due to the bulk FZ treatment.

Furthermore, once the cells were stripped of their diffused areas and re-passivated using SA, bulk lifetime values of 2 ms (cell A) and 5 ms (cell B) were found for wafers without and with the bulk FZ treatment, respectively, suggesting a near surface defect was present in the cell wafers that affected the untreated wafer more severely compared to the treated wafer. TCAD simulations predict that this difference in bulk lifetime would not result in a significant efficiency improvement. However, upon careful examination of the bulk lifetime of cell A before and after etching the diffused regions, it is suggested that bulk defects were present in the near surface region, thus limiting the bulk lifetime to <460 μs on the cell level. This lifetime was boosted to approximately 2 ms once approximately 5 μm of silicon was removed from the surface prior to SA passivation. In this case, the lifetime increase from <460 μs (cell A) to 5 ms (cell B) is consistent with the enhancement in efficiency as simulated by TCAD and our experimental data. TCAD simulations showed that this bulk lifetime boost can result in significant enhancement of performance in the cells when maintaining low-surface recombination velocities. Furthermore, the simulations also highlighted the potential for high performance of these cells through improved series resistance, passivated regions, and light trapping, with $\eta > 26\%$ for $\tau > 10$ ms. Other degradation mechanisms in the fabrication process, which limited performance, were observed in this work, including e-beam evaporation and RIE damage. Photoluminescence studies showed improvements when metallization was followed by a sinter and when dry etching during the pre-diffusion pattern transfer was replaced with wet etching.

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REFERENCES

1. Yoshikawa K, Kawasaki H, Yoshida W, *et al*. Silicon heterojunction solar cell with interdigitated back contacts for a photoconversion efficiency over 26%. *Nat Energy*. 2017;2:17032.
2. Rahman T, Bonilla RS, Nawabjan A, Wilshaw PR, Boden SA. Passivation of all-angle black surfaces for silicon solar cells. *Sol Energy Mater Sol Cells*. 2017;160:444-453.
3. Savin H, Repo P, von Gastrow G, *et al*. Black silicon solar cells with interdigitated back-contacts achieve 22.1% efficiency. *Nat Nanotechnol*. 2015;10(7):624-628.
4. Franklin E, Fong K, McIntosh K, *et al*. Design, fabrication and characterisation of a 24.4% efficient interdigitated back contact solar cell. *Prog Photovolt*. 2016;24(4):411-427.
5. Trupke T, Bardos RA, Hudert F, Würfel P, Zhao J, Wang A, Green MA. Effective excess carrier lifetimes exceeding 100 milliseconds in float zone silicon determined from photoluminescence. In Proceedings of the 19th European Photovoltaic Solar Energy Conference, Paris, France. 2004:758-761.
6. Grant NE, Markevich VP, Mullins J, *et al*. Permanent annihilation of thermally activated defects which limit the lifetime of float-zone silicon. *Phys Status Solidi A*. 2016;213(11):2844-2849.
7. Grant NE, Markevich VP, Mullins J, Peaker AR, Rougieux F, Macdonald D. Thermal activation and deactivation of grown-in defects limiting the lifetime of float-zone silicon. *Phys Status Solidi RRL*. 2016;10(6):443-447.
8. Voronkov V, Falster R. Vacancy out-diffusion in nitrogen-doped silicon. *Phys Status Solidi C*. 2012;9(10–11):1987-1991.
9. Abe T, Takahashi T. Intrinsic point defect behavior in silicon crystals during growth from the melt: a model derived from experimental results. *J Cryst Growth*. 2011;334(1):16-36.
10. Murphy JD, Al-Amin M, Bothe K, Olmo M, Voronkov V, Falster R. The effect of oxide precipitates on minority carrier lifetime in n-type silicon. *J Appl Phys*. 2015;118(21):215706
11. Søndenå R, Hu Y, Juel M, Wiig MS, Angelskår H. Characterization of the OSF-band structure in n-type Cz-Si using photoluminescence-imaging and visual inspection. *J Cryst Growth*. 2013;367:68-72.
12. Haunschild J, Reis IE, Geilker J, Rein S. Detecting efficiency-limiting defects in Czochralski-grown silicon wafers in solar cell production using photoluminescence imaging. *Phys Status Solidi RRL*. 2011;5(5–6):199-201.
13. Synopsys. *Sentaurus TCAD Version K-2015.06*. Mountain View, CA: Synopsys Inc.; 2015.
14. https://www2.pvlighthouse.com.au/calculators/opal%202/opal%202.aspx.
15. https://www2.pvlighthouse.com.au/calculators/Grid%20calculator/Grid%20calculator.aspx.
16. Fell A, McIntosh KR, Altermatt PP, *et al*. Input parameters for the simulation of silicon solar cells in 2014. *IEEE J Photovolt*. 2015;5(4):1250-1263.
17. Altermatt PP, Schmidt J, Heiser G, Aberle AG. Assessment and parameterisation of Coulomb-enhanced Auger recombination coefficients in lowly injected crystalline silicon. *J Appl Phys*. 1997;82(10):4938-4944.
18. Klaassen D. A unified mobility model for device simulation—I. Model equations and concentration dependence. *Solid-State Electron*. 1992;35(7):953-959.
19. Payne DNR, Vargas C, Hameiri Z, Wenham SR, Bagnall DM. An advanced software suite for the processing and analysis of silicon luminescence images. *Comput Phys Commun*. 2017;215:223-234.
20. Ning TH. Electron trapping in SiO2 due to electron-beam deposition of aluminum. *J Appl Phys*. 1978;49(7):4077-4082.
21. Collins D, Sah C. Effects of X-ray irradiation on the characteristics of metal-oxide-silicon structures. *Appl Phys Lett*. 1966;8(5):124-126.
22. Hamasaki M. Radiation effects on thin-oxide MOS capacitors caused by electron beam evaporation of aluminum. *Solid-State Electron*. 1983;26(4):299-303.
23. Jansen H, Gardeniers H, de Boer M, Elwenspoek M, Fluitman J. A survey on the reactive ion etching of silicon in microtechnology. *J Micromech Microeng*. 1996;6(1):14.
24. Oehrlein GS, Tromp R, Tsang J, Lee Y, Petrillo E. Near-surface damage and contamination after CF 4/H 2 reactive ion etching of Si. *J Electrochem Soc*. 1985;132(6):1441-1447.
25. Connick IWH, Bhattacharyya A, Ritz KN, Smith WL. Study of reactive-ion-etch-induced lattice damage in silicon by Ar, CF_4, NF_3, and CHF_3 plasmas. *J Appl Phys*. 1988;64(4):2059-2063.
26. Pang S, Rathman D, Silversmith D, Mountain R, DeGraff P. Damage induced in Si by ion milling or reactive ion etching. *J Appl Phys*. 1983;54(6):3272-3277.

27. Ikawa E, Endo N, Tajima M, Kurogi Y. Annealing and oxidation effects after CF_4/H_2 dry etching for damage recovery. *Surf Sci*. 1986;172(3):763-772.

28. Rougieux FE, Grant NE, Barugkin C, Macdonald D, Murphy JD. Influence of annealing and bulk hydrogenation on lifetime-limiting defects in nitrogen-doped floating zone silicon. *IEEE J Photovolt*. 2015;5(2):495-498.

29. Bullock J, Kiriya D, Grant N, *et al*. Superacid passivation of crystalline silicon surfaces. *ACS Appl Mater Interfaces*. 2016;8(36):24205-24211.

30. Grant NE, Niewelt T, Wilson NR, *et al*. Superacid-Treated Silicon Surfaces: Extending the Limit of Carrier Lifetime for Photovoltaic Applications. *IEEE J Photovolt. Under Review* 2017.

31. Sproul A. Dimensionless solution of the equation describing the effect of surface recombination on carrier decay in semiconductors. *J Appl Phys*. 1994;76(5):2851-2854.

32. Richter A, Glunz SW, Werner F, Schmidt J, Cuevas A. Improved quantitative description of Auger recombination in crystalline silicon. *Phys Rev B*. 2012;86(16):165202.

33. Zheng P, Rougieux F, Samundsett C, *et al*. Upgraded metallurgical-grade silicon solar cells with efficiency above 20%. *Appl Phys Lett*. 2016;108(12):122103.

34. Kessler MA, Ohrdes T, Wolpensinger B, Harder N-P. Charge carrier lifetime degradation in Cz silicon through the formation of a boron-rich layer during BBr_3 diffusion processes. *Semicond Sci Technol*. 2010;25(5):055001.

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