An Inductorless Bias-Flip Rectifier for Piezoelectric Energy Harvesting

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Abstract

Piezoelectric vibration energy harvesters have drawn much interest for powering self-sustained electronic devices. Furthermore, the continuous push towards miniaturization and higher levels of integration continue to form key drivers for autonomous sensor systems being developed as parts of the emerging Internet of Things paradigm. The synchronized switch harvesting on inductor (SSHI) and synchronous electrical charge extraction (SECE) are two of the most efficient interface circuits for piezoelectric energy harvesters; however, inductors are indispensable components in these interfaces. The required inductor values can be up to $10\,\mathrm{mH}$ to achieve high efficiencies, which significantly increase overall system volume, counter to the requirement for miniaturized self-power systems for IoT. An inductorless bias-flip rectifier is proposed in this paper to perform residual charge inversion using capacitors instead of inductors. The voltage flip efficiency goes up to 80% while 8 switched capacitors are employed. The proposed SSHC (Synchronized Switch Harvesting on Capacitors) circuit is designed and fabricated in a $0.35\,\mu\mathrm{m}$ CMOS process. The performance is experimentally measured and it shows a 9.7× performance improvement compared to a full-bridge rectifier for the case of a $2.5\,\mathrm{V}$ open-circuit zero-peak voltage amplitude generated by the piezoelectric harvester. This performance improvement is higher than most of reported state-of-the-art inductor-based interface circuits while the proposed circuit has a significantly smaller overall volume enabling system miniaturization.

Index Terms

Energy harvesting, piezoelectric transducer, bias-flip, synchronized switch harvesting on inductor (SSHI), synchronized switch harvesting on capacitors (SSHC), rectifier.

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I. Introduction

Piezoelectric vibration energy harvesting (PVEH) has drawn much interest in recent years as a means of harvesting ambient kinetic energy to power wireless sensors and portable and implantable electronics [1], [2]. Among the various candidate vibration energy harvesting techniques considered, piezoelectric materials are widely used due to their relatively high power density [3], scalability and compatibility with conventional integrated circuit technologies [4]. As the energy generated by a piezoelectric transducer (PT) cannot be directly used to power load electronics, an interface circuit is needed to rectify the output power and provide a stable supply. A typical piezoelectric VEH can provide an power density of around 10 - 500 $\mu\mathrm{W/cm^3g^2}$, which sets a significant constraint on designing the associated power conditioning interface circuit [5], [6]. Full-bridge rectifiers (FBR) are widely used due to their simplicity and stability; however, their power efficiencies are relatively low as they set high voltage thresholds for the input voltage to overcome prior to any energy extraction [7], [8].

Recently, various interface circuits have been reported based on inductors employed to improve the power efficiency with RLC loops [9]–[14]. The SSHI (Synchronized Switch Harvesting on Inductor) rectifier (or inductor-based bias-flip) is one of the most energy-efficient circuits with ideally no-charge wastage developed for this purpose [15], [16], which synchronously flips the voltage across the PT to minimize energy wastage due to charging the internal capacitor [17]. However, most of these reported circuits require large inductors, up to 10 mH, to achieve acceptable efficiencies and these large inductors significantly increase the system volume, counter to the requirement for miniaturized self-powered systems.

In this paper, an alternative SSHC (Synchronized Switch Harvesting on Capacitors) approach is proposed to synchronously flip the voltage across the PT using one or multiple switched capacitors instead of an inductor. This design does not require any inductor, thus significantly reduces the required system volume. This feature is particularly necessary when considering the design of miniaturized energy harvesting systems integrating MEMS (microelectromechanical systems) harvesters for applications to implantable devices and miniaturized wireless sensor nodes. Compared to reported state-of-the-art interface circuits, the proposed circuit also achieves higher voltage flip efficiency, hence higher energy extraction efficiency. The background and conventional SSHI interfaces are presented in Section II. The proposed interface circuit and circuit implementations are shown in Section III and Section IV, respectively. Section V provides measured results and comparisons with state-of-the-art interface circuits and a summary and conclusion is provided in Section VI.

II. Inductor-based SSHI interface

Fig. 1a shows the circuit schematic of a parallel-SSHI rectifier, which consists of a full-bridge rectifier (FBR) with a switch-controlled inductor to synchronously flip the voltage across the PT. A weakly coupled piezoelectric transducer (PT) is employed in this work; hence, the synchronized switch damping (SSD) effect [18] is neglected and the PT can be modeled as a current source I_P in parallel with a capacitor C_P [9]. The associated waveforms of the SSHI circuit are shown in Fig. 1b. Before zero-crossing instants of the current source I_P, the voltage across the PT, V_{PT}, equals to $V_S + 2V_D$ or $-(V_S + 2V_D)$. In order to overcome the threshold set by the FBR and transfer energy into the storage capacitor C_S in the next half-cycle, V_{PT} needs to be flipped from $V_S + 2V_D$ to $-(V_S + 2V_D)$ (or vice-versa). In an SSHI interface, analog switches driven by a synchronized pulse signal ϕ_{SSHI} are employed to control the RLC oscillation loop to flip the voltage. The resulting flipped voltage V_F is always lower than $V_S + 2V_D$ due to the resistive damping in the RLC loop, which can written as $V_F = (V_S + 2V_D)e^{-\frac{\pi}{\sqrt{\frac{4L}{R^2C}-1}}}$. After the voltage flip, $|V_{PT}|$ needs to be charged from V_F to $V_S + 2V_D$ and this amount of energy is wasted. Therefore, the power efficiency of an SSHI interface usually depends on the voltage flip efficiency, which is expressed as:

$$\eta_{SSHI} = \frac{V_F}{V_S + 2V_D} = e^{-\frac{\pi}{\sqrt{\frac{4L}{R^2C_P}-1}}} \tag{1}$$

where C_P, L and R represent the internal capacitor of the PT, the inductor and total resistance in the RLC loop, respectively. As C_P is inherently constant for a given PT, η_{SSHI} can only be increased by increasing L or decreasing R. In order to miniaturize the system, L is typically chosen in the range of a few mH; however, an inductor of this value still occupies significant system volume. While decreasing R, the contributory factors of R should be mentioned. Usually, R is the total resistance in the RLC circuit, which includes DC resistance of the inductor R_{IND}, ON resistance of CMOS switches R_{SW} and other parasitic resistance R_{PAR}, such as CMOS wiring, vias and contacts. In terms of R_{IND}, it is usually proportional to the inductance L for a given inductor family. Hence, R_{IND} should also be considered while choosing the inductor for SSHI circuits. In order to reduce R_{SW}, the transistor sizes of the two analog switches shown in Fig. 1a need to be designed to be larger; as a result, the gate capacitance of the transistors is increased. These large switches are usually power-hungry when driven. The following sections of this paper propose a novel interface circuit with the ability of performing highly efficient voltage flipping without employing inductors, hence the energy efficiency is increased with smaller required volume.

III. Proposed SSHC interface circuit

In this section, an inductor-less interface circuit is introduced, which employs one or multiple synchronized switched capacitors to increase voltage flip efficiency and hence power extraction efficiency. The performance is then compared with an SSHI interface.

A. SSHC with one capacitor

Fig. 2a shows the circuit diagram of the proposed SSHC (Synchronized Switch Harvesting on Capacitors) interface circuit with one switched capacitor C_1, or it can be called a charge-swap capacitor. In order to perform the charge inversion, five analogue switches driven by three pulse signals (ϕ_p, ϕ_0 and ϕ_n) are used. The three non-overlapping switching signals are synchronously generated to turn ON the five switches sequentially in a specific order. The order of the three pulses depends on the polarization of the voltage V_{PT}.

Fig. 2b shows the waveforms of the voltage V_{PT}, the voltage across the capacitor C_1 and the three pulse signals driving the five switches. At each zero-crossing moment of I_P, the three pulse signals (ϕ_p, ϕ_0 and ϕ_n) are sequentially generated to flip the voltage V_{PT}. Assuming $V_{PT} = V_S + 2V_D$ before the flipping instant (the left zoom-in figure), V_{PT} needs to be flipped towards negative. In this case, the pulse ϕ_p is first generated to damp a part of charge from C_P into the charge-swap capacitor C_1. Then, the pulse ϕ_0 clears the residual charge in C_P and the pulse ϕ_n charges C_P from

C_1 in the opposite sense. This allows the voltage V_{PT} to be partially flipped. While V_{PT} is supposed to be flipped from $-(V_S+2V_D)$ towards positive polarity, the three pulses are now generated in an inversed order: $\phi_n \rightarrow \phi_0 \rightarrow \phi_p$ (the right zoom-in figure). As shown in the figure, the voltage flip efficiency is around 1/3. This is the optimal flip efficiency while using one charge-swap capacitor and the theoretical discussion will follow in Section III-C.

B. SSHC with multiple capacitors

In order to flip additional charge across the capacitor C_P, more synchronized switched capacitors can be added to transfer more charge from C_P into a series of capacitors and conversely charge C_P to a higher voltage level. Fig. 3a shows the proposed SSHC interface circuit with k switched capacitors. In this design, there are $4k+1$ analog switches and $2k+1$ switching signal phases: ϕ_0, ϕ_{1p}, ϕ_{1n}, ϕ_{2p}, ϕ_{2n}, ϕ_{3p}, ϕ_{3n}, etc.

Assuming the number of switched capacitors is $k = 8$, the instant when V_{PT} is being flipped from $-(V_S + 2V_D)$ towards positive and from $V_S + 2V_D$ towards negative are shown in Fig. 3b. The voltage V_{PT} and the 17 (as $2k + 1$ while $k = 8$) phases of the switching signals are shown in the figure. From the figure, it can be seen that, in order to flip V_{PT} from $-(V_S + 2V_D)$ towards positive, the phase order of the 17 pulses is: ϕ_{1n}, ..., ϕ_{8n}, ϕ_0, ϕ_{8p}, ..., ϕ_{1p}. The first 8 phases aim to sequentially transfer charge from C_P to the 8 switched capacitors, C_1 to C_8. The phase ϕ_0 clears the residual charge in C_P and the following 8 phases sequentially connect the 8 switched capacitors in an opposite sense to flip the voltage V_{PT}. While V_{PT} needs to be flipped from V_S+2V_D towards negative, the phase order of the 17 pulses is completely reversed, as shown in the figure. The theoretical discussion on optimal voltage flip efficiencies using multiple capacitors and the constraints on the capacitance values will follow in the next section.

C. Performance analysis

In this section, the voltage flip efficiency of the proposed SSHC interface circuit is calculated and its performance is compared with the SSHI interface. Assuming one charge-swap capacitor is present in the SSHC interface circuit, as previously shown in Fig. 2a, and the voltage V_{PT} needs to be flipped from positive to negative at the first I_P zero-crossing moment, this voltage equals to $V_S + 2V_D$. Before the first flipping is performed, the voltage across the switched capacitor is zero, noted as $V_1 = 0\,\mathrm{V}$. At the first zero-crossing moment of I_P, the first pulse ϕ_p is present. C_P and C_1 are connected and the charge flows into C_1 until the voltages across the two capacitors are equal. As the total charge keeps unchanged, the voltage across C_P and C_1 at the end of first phase ϕ_p is:

$$V_{PT} = V_1 = \frac{C_P}{C_P + C_1}(V_S + 2V_D) \tag{2}$$

where V_1 is voltage across the switched capacitor C_1. At the second phase, a pulse ϕ_0 is generated to clear the residual charge in C_P. The charge in C_1 remains unchanged during this phase. Hence the voltage across C_P and C_1 at the end of the second phase is:

$$\begin{aligned} V_{PT} &= 0 \\ V_1 &= \frac{C_P}{C_P + C_1}(V_S + 2V_D) \end{aligned} \tag{3}$$

At the third phase ϕ_n, C_1 is connected with C_P in an opposite sense to charge C_P to a negative voltage. Due to the conservation of charge in these two capacitors, the remaining charge in C_1 after the second phase is shared between C_P and C_1. Hence the voltages V_{PT} and V_1 at the end of the third phase are:

$$V_{PT} = V_1 = -\frac{C_P C_1}{(C_P + C_1)^2}(V_S + 2V_D) = -(V_S + 2V_D)\frac{x}{(1+x)^2} \tag{4}$$

where x is the ratio between C_1 and C_P. It can be seen that V_{PT} is a negative value after three phases of voltage flipping. From (4), it can be found that V_{PT} attains the minimum while $x = 1$, or $C_1 = C_P$. Therefore, the minimum value of V_{PT} at the end of the first voltage flipping is:

$$V_{PT} = V_1 = -\frac{1}{4}(V_S + 2V_D) \tag{5}$$

The result obtained in the (5) is under the assumption that the initial voltage across the switched capacitor C_1 is $0\,\mathrm{V}$. However, before the second zero-crossing moment where V_{PT} needs to be flipped from negative to positive, V_1 equals to $-\frac{1}{4}(V_S + 2V_D)$. Assuming $C_1 = C_P$ is chosen for future calculations, V_{PT} and V_1 values after each phase of ϕ_n, ϕ_0 and ϕ_p during the second voltage flipping stage are:

$$\begin{aligned}
before\ \phi_n: &\ \ V_{PT} = -(V_S + 2V_D), \quad V_1 = \frac{1}{4}(V_S + 2V_D) \\
\Rightarrow after\ \phi_n: &\ \ V_{PT} = -V_1 = -(\frac{1}{4} + 1)\frac{1}{2}(V_S + 2V_D) \\
\Rightarrow after\ \phi_0: &\ \ V_{PT} = 0\,\mathrm{V}, \quad V_1 = (\frac{1}{4} + 1)\frac{1}{2}(V_S + 2V_D) \\
\Rightarrow after\ \phi_p: &\ \ V_{PT} = V_1 = ((\frac{1}{4})^2 + \frac{1}{4})(V_S + 2V_D) = \frac{5}{16}(V_S + 2V_D)
\end{aligned} \tag{6}$$

It can be seen from (6) above, more charge is inverted in the second zero-crossing moment compared to the first one. Due to the accumulation of remaining charge in C_1, the resulting $|V_{PT}|$ at the end of the n^{th} voltage flipping stage is:

$$\begin{aligned}
|V_{PT}| &= ((\frac{1}{4})^n + \cdots + (\frac{1}{4})^2 + \frac{1}{4})(V_S + 2V_D) = \sum_{1 \le i \le n} (\frac{1}{4})^i (V_S + 2V_D) \\
\Rightarrow \lim_{n \to \infty} |V_{PT}| &= \frac{1}{3}(V_S + 2V_D)
\end{aligned} \tag{7}$$

While n tends to infinity, $|V_{PT}|_{n \to \infty} = \frac{1}{3}(V_S + 2V_D)$, which means that the optimal voltage flip efficiency for the SSHC interface circuit with one switched capacitor is $\eta_{SSHC-1} = \frac{1}{3}$ while $C_1 = C_P$.

The condition $C_1 = C_P$ has been shown for the single capacitor SSHC implementation. When the number of capacitors increases to k, as shown in Fig. 3a, the above derivations for k capacitors can still be applied but result in a lengthy calculation. Alternatively, to provide a concise derivation for the optimal values of the capacitors, the following alternative method provides a generalized approach to determine the condition for optimal flip efficiency as $C_P = C_1 = C_2 = C_3 = ... = C_k$. Assuming there are two capacitors, C_P and C_k, the voltage across one of them is V_C and across the other one is $0\,\mathrm{V}$. It can be assumed that C_P is associated with voltage V_C and the voltage across C_k is $0\,\mathrm{V}$. After these two capacitors are shorted, the resulting voltages across them are equal:

$$V_{Cp} = V_{Ck} = \frac{C_P V_C}{C_P + C_k} \tag{8}$$

It can be seen that a certain amount of energy is transferred from C_P to C_k. As some energy will be transferred back to C_P later to flip the voltage, so the desirable case is that the energy transferred between these two capacitors is the maximum possible. Hence, after the first shorting, the energy transferred from C_P into C_k is:

$$E_{Ck} = \frac{1}{2} C_k V_{Ck}^2 = \frac{1}{2} \frac{C_k C_P^2}{(C_P + C_k)^2} V_C^2 \tag{9}$$

By setting the derivative of E_{C1} to 0, the equation becomes:

$$\begin{aligned}\frac{\partial E_{Ck}}{\partial C_k} = \frac{1}{2}V_C^2\frac{C_P^2(C_P+C_k)^2 - 2C_kC_P^2(C_P+C_k)}{(C_P+C_k)^4} = 0 \\ \Rightarrow C_k = C_P\end{aligned} \tag{10}$$

Therefore, $C_k = C_P$ is the condition that the transferred energy from C_P to C_k is maximum. If there is only one capacitor, the next steps are to clear the remaining charge in C_P and then short the two capacitors in the opposite polarization. In this step, the energy is now transferred from C_k to C_P and the same derivation previously performed can be reused to find that the transfered energy attains its maximum while $C_k = C_P$. If there are k capacitors, the same derivations above can be performed for each individual capacitor from C_1 to C_k. After some calculations, the energy transfered into each individual capacitor reaches the maximum while $C_1 = C_P$, $C_2 = C_P$, $\ldots$, $C_k = C_P$, which can be rewritten as $C_P = C_1 = C_2 = C_3 = ... = C_k$.

Considering an SSHC interface with up to 8 switched capacitors, the circuit is simulated and the voltage flip efficiency is obtained in Table I. The first column is the number of switched capacitors employed for a SSHC interface and the second column shows the simulated voltage flip efficiencies. The flip efficiencies shown in the table are the values under assumptions that all the switched capacitors have the same capacitance of the PT internal capacitor C_P, such that $C_1 = C_2 = ... = C_8 = C_P$. The third column shows the calculated inductor value required for a SSHI interface circuit to achieve the same voltage flip efficiencies. The equation for calculating the SSHI flip efficiencies is given in (1). In the calculations, the capacitance is set as $45\,\mathrm{nF}$, which matches the C_P for the measurements in this paper. The total resistance in the RLC loop consists of the DC resistance of the inductor, ON resistance of all CMOS switches, and parasitic resistance including CMOS metal wires, vias between metal layers and contacts. This value varies among different implementations and it is usually between $30\,\Omega$ and $70\,\Omega$ for most implementations. In order to provide fair comparisons, $50\,\Omega$ is chosen for the calculations. The quality factor of an RLC circuit is expressed as $Q = \frac{1}{R}\sqrt{\frac{L}{C_P}}$. As C_P is the internal capacitance and cannot be modified for a given PT, the resistance R and the inductor L dominate the voltage flip efficiency in SSHI circuits.

From the table, it can be found that the SSHI interface circuit requires large inductors to achieve equal voltage flip efficiencies as the SSHC interface circuit. An inductor in the mH scale typically occupies a volume of $\sim$ 100's mm^3; however, a surface-mount (SMD) ceramic capacitor (imperial 0402/0201 package) can take up a volume of less than $0.5\,\mathrm{mm}^3$. Hence, the proposed SSHC interface circuit significantly reduces the system volume by employing capacitors instead of inductors. This advantage is particularly suitable for miniaturized MEMS energy harvesting systems. In the next section, the circuit implementations of the proposed SSHC interface circuit will be presented.

IV. Circuit implementation of the proposed SSHC interface

A. System architecture

The system architecture of the proposed SSHC interface circuit is shown in Fig. 4. The five blocks implemented on-chip are "zero-crossing detection", "pulse generation", "pulse sequencing", "switch control" and "voltage regulator" blocks. At each zero-crossing moment of I_P, a rising edge is generated in signal SYN and the signal PN indicates the direction that V_{PT} will be flipped, where $V_{PT} = V_P - V_N$. The signal PN is needed because the pulse phase orders for different voltage flip directions are different, as shown in Fig. 3b. Assuming there are k switched capacitors employed in the SSHC circuit, after the "pulse generated" block reads a rising edge in SYN, $2k+1$ sequential pulses are generated. In the following "pulse sequencing" block, these $2k+1$ signals are sequenced according to the level of the signal PN. Then, these sequenced $2k+1$ signals are used to drive analog switches in the "switch control" block to perform voltage flipping with the k off-chip capacitors. In order to achieve the optimal voltage flip efficiency, the values of the k off-chip capacitors are chosen as $C_1 = C_2 = ... = C_k = C_P$. A voltage regulator with over-voltage protection is employed to make the system being self-powered. The internal transistor-level circuit diagrams and operations for each block are presented and explained in the following sections.

B. Zero-crossing detection

Fig. 5a shows the circuit diagram of the zero-crossing detection block. In order to find the zero-crossing moment of the current source I_P, two continuous-time comparators are employed to compare V_P and V_N with a reference voltage V_{ref}. While I_P is close to zero, the diodes of the full-bridge rectifier (FBR) are just about to turn OFF. At this moment, one of V_P and V_N is close to

$-V_D$ and the other one is close to $V_S + V_D$. Hence, the reference voltage V_{ref} is set slightly higher than the negative value of the voltage drop of a diode ($-V_D$) so that either V_P or V_N going from $-V_D$ towards positive can trigger the comparator and generate a synchronous signal. The outputs of these two comparators are ANDed so that a rising edge in the SYN signal is generated to flip the voltage V_{PT} for each zero-crossing moment of I_P. Fig. 5b shows the associated waveform of this block. A signal named PN is also generated in this block, which indicates the polarization of V_{PT} before it is flipped at each zero-crossing moment. This signal is then used in the "pulse sequencing" block to help sequence the switch-driving pulses.

C. *Pulse generation*

Fig. 6 shows the circuit diagram of the pulse generation block for up to 8 switched capacitors in the SSHC interface circuit. 17 pulse cells are employed in this block to generate up to 17 sequential pulses, of which the pulse width can be tuned externally. The input signal SYN is the synchronous clock signal generated from the zero-crossing detection block. A rising edge in SYN drives the 17 pulse cells sequentially to generate one individual pulse in each cell. The 8 off-chip switched capacitors can be selectively enabled by input signals $EN_1 - EN_8$ and signal EN_0 enables the ϕ_0 switch, which aims to clear the residual charge in C_P. These 9 digital input signals can be set externally according to the number of switched capacitors employed. If all of these 9 signals are low, the interface circuit simply works as a full-bridge rectifier. The input EN_0 is forced to high if any of $EN_1 - EN_8$ are high because the residual charge in C_P needs to be cleared in the middle phase of the voltage flipping process. The diagram for the pulse cell is also illustrated in the figure. The pulse signal is generated by ANDing the delayed and inverted versions of the input signal. For the very first pulse cell, the input signal is SYN and the input signals for the following cells are delayed versions of SYN. The delay in one pulse cell is performed by using two weak inverters charging a capacitor. The pulse width of the generated pulse for each cell can be tuned by adjusting the on-chip variable capacitor, which can be set externally. The three switches in one pulse cell are CMOS analog switches, which aims to enable and bypass the selected pulse cells. If any of $EN_1 - EN_8$ signals are low, the corresponding pulse cells for the disabled capacitors are bypassed so that the SYN signal has nearly no delay while bypassing these cells.

D. Pulse sequencing

After the up to 17 sequential pulses are generated, they need to be sequenced before driving the switches to flip V_{PT}. Fig. 7 shows the pulse sequencing block, which consists of 8 multiplexers. While the input signal PN is high, V_{PT} needs to be flipped from positive to negative. In this case, the output sequence of the 17 pulses after the sequencing block should be $\phi_{1p} \rightarrow \phi_{2p} \rightarrow \phi_{3p} \rightarrow \phi_{4p} \rightarrow \phi_{5p} \rightarrow \phi_{6p} \rightarrow \phi_{7p} \rightarrow \phi_{8p} \rightarrow \phi_0 \rightarrow \phi_{8n} \rightarrow \phi_{7n} \rightarrow \phi_{6n} \rightarrow \phi_{5n} \rightarrow \phi_{4n} \rightarrow \phi_{3n} \rightarrow \phi_{2n} \rightarrow \phi_{1n}$. While PN is low, the pulse sequence is completely inversed. The pulse ϕ_0 is always in the middle of the sequence so it does not need sequencing. However, two redundant gates (AND and OR gates) are added for ϕ_0, which aims to ensure that all pulses have the same delay to avoid overlapping. Fig. 8 shows the associated waveforms of this block for different PN levels.

E. Switch control and voltage regulation blocks

Fig. 9 shows the circuit diagram of the switch control block, which consists of 17 two-stage level shifters and 33 analog CMOS switches. The schematic of a CMOS switch is shown in the figure, which consists of an inverter, an isolated NMOS and a PMOS and their body diodes are also shown in the figure. The 8 capacitors $C_1 - C_8$ are implemented off-chip as their capacitances are $45\,\mathrm{nF}$, which are equal to the internal capacitance of the piezoelectric transducer C_P. The sequenced pulses obtained from the pulse sequencing block cannot be directly used for driving the 33 switches because different voltage levels are needed. For each switch, the voltage on either side varies over a wide range between $-V_D$ and $V_S + V_D$; however, the voltage levels of the pulses signals from the pulse sequencing block are $0\,\mathrm{V}$ and $1.5\,\mathrm{V}$ ($V_{DD} = 1.5\,\mathrm{V}$ is used in this implementation). Therefore, the high and low levels of the switch driving signals should be shifted to a large voltage range in order to fully turn ON and OFF the 33 switches with level shifters [19]. The translated voltage levels, V_{DDA} and V_{SUB} are gate over-driving voltages to fully turn ON and OFF the switches. These two voltage levels are also used to bias the body diodes of the CMOS switches. In the schematic showing the body diodes, node B_P is biased at V_{SUB}, T and B_N are biased at V_{DDA} and the SUB is the common substrate of the entire chip, which is grounded at $0\,\mathrm{V}$. These two voltages are the highest and lowest voltage levels, respectively, in the system and a simplified implementation is shown in Fig. 10. Detailed similar circuit implementations are presented in [10]. Another implementation employing switched-capacitor DC-DC converters to generate gate over-driving voltage levels can be found in [9].

Fig. 11 shows the implementation of an over-voltage protection (OVP) and a voltage regulator. The OVP aims to limit the voltage stored in the capacitor C_S and the voltage regulator is employed to provide a stable $1.5\,\mathrm{V}$ supply to the interface circuit with the harvested energy. The resistors are off-chip implemented with values $R_1 = 100\,\mathrm{M\Omega}$, $R_2 = 10\,\mathrm{M\Omega}$, $R_3 = 50\,\mathrm{M\Omega}$, $R_1 = 100\,\mathrm{M\Omega}$. The circuit diagram of the low-power comparator is shown in Fig. 12. The power consumption of this comparator is around $62\,\mathrm{nW}$ and the delay time is around $65\,\mathrm{\mu s}$. As the power capacitor C_S is large and V_S varies slowly, some performance criteria such as the speed of the comparators and the voltage reference is sacrificed for low power consumption reasons.

V. Measurement results

The proposed SSHC interface circuit was designed and fabricated in a $0.35\,\mathrm{\mu m}$ HV CMOS process. The system was experimentally evaluated using a commercially available piezoelectric transducer (PT) of dimension $58\,\mathrm{mm} \times 16\,\mathrm{mm}$ (Mide Technology Corporation V21BL). This PT has an measured internal capacitance of $C_P = 45\,\mathrm{nF}$ and the 8 off-chip switched capacitors are chosen with the equal capacitances of $45\,\mathrm{nF}$ to achieve the optimal voltage flip efficiency. During the measurement, a shaker (LDS V406 M4-CE) was excited at the natural frequency of the PT at $92\,\mathrm{Hz}$ and driven by a sine wave from a function generator (Agilent Technologies 33250A 80 MHz waveform generator) amplified by a power amplifier (LDS PA100E Power Amplifier). A super capacitor is employed as the energy storage capacitor (AVX BestCap BZ05CA103ZSB) with a measured capacitance $C_S \approx 5.2\,\mathrm{mF}$. As the circuit is self-sustained with an on-chip voltage regulator, the voltage supply from the voltage regulator is only available when voltage across the storage capacitor satisfies $V_S \geq 1.5\,\mathrm{V}$. While $V_S < 1.5\,\mathrm{V}$, the interface circuit simply works as a full-bridge rectifier (FBR) as all the 33 switches are OFF until V_S is charged to $1.5\,\mathrm{V}$. Hence, an external power supply at $1.5\,\mathrm{V}$ was used while measuring the harvested power for $V_S < 1.5\,\mathrm{V}$. Fig. 13 shows the die photograph of the test chip.

Table II lists the power consumption due to different blocks of the proposed SSHC interface circuit. The first 6 lines shown in the table are obtained from simulations with assumptions that 8 switched capacitors are employed (with 80% voltage flip efficiency) and the PT resonant frequency is $92\,\mathrm{Hz}$. The last two lines are the measured static and dynamic power consumption of the chip. The static power loss is measured while the PT is not vibrating and the dynamic power loss is measured while the PT is excited at $92\,\mathrm{Hz}$. Hence, the difference between these two measured power consumption values is due to the operation of the "pulse generation" and "pulse sequencing" blocks because while the PT is static, the voltage across it is not being flipped. While employing fewer switched capacitors, the power loss due to the "pulse generation" and "switch control" blocks can be much lower. This is because fewer pulse signals will be generated and fewer switches in the switch control block will be driven in this case. The PT resonant frequency also affects the power consumption of these two blocks because a series of pulse signals are generated for every half period of the excitation frequency. Hence, higher frequency proportionally results in more pulse signals and more power consumed in generating pulses and driving switches.

Fig. 14 shows the measured waveforms and the four sub figures show the cases while the numbers of enabled switched capacitors are set to 1, 2, 4 and 8, respectively. From Fig. 14a, it can be seen that the voltage across the piezoelectric transducer V_{PT} is flipped from $\pm 2.8\,\mathrm{V}$ to $\mp 0.94\,\mathrm{V}$. The voltage flip efficiency is around 1/3, which matches the calculated efficiency shown in table I. The zoom-in voltage flipping instants for V_{PT} flipped from positive to negative and from negative to positive are also shown in the figure with the three switch signals ϕ_{1p}, ϕ_0 and ϕ_{1n}. There are only 3 switch signals needed for 1 switched capacitor because the switch signal number required for k switched capacitors is $2k+1$, as mentioned previously. In order to flip V_{PT} in two different directions, the sequence of the switched signals are inversed, as previously explained. While 2, 4 and 8 switched capacitors are enabled (Fig. 14b, Fig. 14c and Fig. 14d), V_{PT} is flipped with efficiencies of 1/2, 2/3 and 4/5, respectively. These results closely match the calculations. As more switch signals are needed to drive more capacitors, these signals are ORed for display due to the limited number of oscilloscope channels. Although the sequence of the switched signals cannot be seen from the ORed version, their sequences for different voltage flip direction are completely inversed. As explained in section III-B, the middle signal ϕ_0 aims to clear the residual charge in C_P

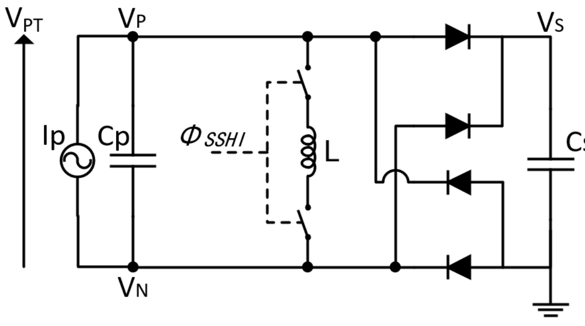
after most of charge has been transferred into the switched capacitors. From the zoom-in voltage flip instants of the figures, it can be seen that V_{PT} goes to $0\,\mathrm{V}$ at the very middle pulse and it is flipped to an opposite polarization during the following pulses.

Fig. 15 shows the measured electrical output power of the PT with a conventional full-bridge rectifier (FBR) and with the proposed SSHC rectifier with up to 8 switched capacitors. The electrical output power is measured and calculated from a small voltage increase of V_S in a short period of time, where V_S is the voltage across the storage capacitor C_S connected to the output of a FBR (refer to Fig. 3a). The power at a specific V_S is calculated as $P = \frac{1}{2T}C_S((V_S + \Delta V_S)^2 - V_S^2)$, where ΔV_S is a small voltage increase in V_S and T is the time elapsed. In Fig. 15a, the voltage across the capacitor C_S is varied to measure the peak power points for each configurations of the interface circuits. During these measurement, the PT is excited at an acceleration level of $1.2\,\mathrm{g}$, which produces an open-circuit voltage amplitude of $V_{OC} = 2.5\,\mathrm{V}$ across the PT. From the figure, it can be seen that the output power of an FBR is around $16.7\,\mu\mathrm{W}$ while the proposed SSHC with only 1 switched capacitor can output $45.1\,\mu\mathrm{W}$ power with 2.7× relative performance improvement with respect to the FBR. While two switched capacitors are employed, the output power increases to $65.5\,\mu\mathrm{W}$ with 3.9× overall improvement. In this implementation, the maximum supportable number of the switched capacitors is 8, which increases the output power to $161.8\,\mu\mathrm{W}$. Hence, the output power with 8 switched capacitors improves the performance by 9.7× compared to an FBR. The trend of the power curve in the figure also implies that the output power for 8 switched capacitors can go higher for higher V_S values; however, the peak power point cannot be achieved in this implementation as the CMOS circuit is not designed to work at such high voltages. Fig. 15b shows the output power with a fixed voltage $V_S = 5\,\mathrm{V}$ and the excitation level is varied from $0\,\mathrm{g}$ to $7.5\,\mathrm{g}$ (equivalent to V_{OC} varying from $0\,\mathrm{V}$ to $15\,\mathrm{V}$). The proposed SSHC interface with 8 switched capacitors can provide output power up to $1.2\,\mathrm{mW}$.

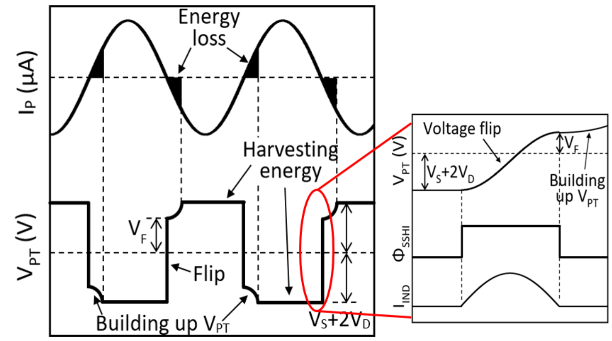
Table III shows the performance comparisons among state-of-the-art interface circuits for piezoelectric energy harvesters and the proposed SSHC interface with up to 8 switched capacitors. The second column from the left shows the employed techniques. The three following columns are the specifications of the piezoelectric transducers, including models of the PTs, internal capacitances and resonant frequencies. The column starting with "V_{OC}" shows the open-circuit voltage amplitudes of the PTs used for measurements. The column "Inductor" shows the inductor values required for different interface circuits. The "normalized volume" is an estimated value for each start-of-the-art interface circuit, which includes the integrated circuit (IC) and all off-chip components except the PT. The IC chips for all the interface circuits are assumed to occupy $10\,\mathrm{mm}^3$ with sufficient clearance to surrounding components. As a surface-mount device can be as small as $1\,\mathrm{mm}^3$, each off-chip capacitor or resistor is assumed to occupy $2\,\mathrm{mm}^3$ with $1\,\mathrm{mm}^3$ of clearance. The unit volume for a highly compact inductor (including estimated clearance) is assumed to be $100\,\mathrm{mm}^3/\mathrm{mH}$. If multi-layer circuit boards are used, the clearance between components can be further decreased and wires can be placed in the inner layers of the board. Therefore, the total estimated volume for each interface circuit is the mathematical sum of the chip, off-chip capacitors, resistors and inductors with considerations of clearance. It can be seen that the proposed SSHC interface circuit occupies less volume than state-of-the-art circuits due to its inductor-less design. The normalized volume values for this work varies between 1 and 1.6 for different numbers of switched capacitors that are employed. The column $\frac{P_{IC}}{P_{FBR}}$ shows the output power performance improvement of the interface circuits compared to an FBR, where the term P_{IC} represents the output power using the proposed rectification IC (integrated circuit) and the term P_{FBR} represents the output power using the full-bridge rectifier (FBR). As a higher V_{OC} can significantly improve the output power of a FBR and decrease $\frac{P_{IC}}{P_{FBR}}$, V_{OC} is chosen at $2.5\,\mathrm{V}$ in this implementation. This is because most of cited references in this table use V_{OC} around this value and this provides a relatively fair performance comparison with state-of-the-art circuits. The figure of merit (FOM) represents the performance improvement per unit volume, which is given by $FOM = \frac{P_{IC}}{P_{FBR}}\frac{1}{V_{NOR}}$, where V_{NOR} is the normalized volume. The FOM shows that although the SSHC interface with 8 switched capacitors takes more room with additional off-chip capacitors, the extra capacitors still have positive contributions to the FOM as a surface-mount capacitor is extremely small compared to other components in the system, such as inductors. However, with the inductor-sharing technique, a SSHI energy harvesting system can employ only one inductor to be shared between the SSHI rectifier and following DC-DC conversion blocks to increase the inductor utilization [9]. Due to the inductor-less architecture of the proposed rectifier, inductors should be avoided in other parts of the IoT/sensor system to achieve a fully inductorless system. Therefore, if this SSHC rectifier is employed in a IoT/sensor system in the future, some circuits that may need inductors, such as bulk/boost DC-DC converters, should be replaced by high-efficiency switched-capacitor (SC) DC-DC converters [20], in order to address an inductorless implementation for miniaturization reasons.

VI. Conclusion

This paper introduced an inductor-less interface circuit for piezoelectric vibration-based energy harvesters employing switched capacitors to synchronously flip the residual charge across the piezoelectric transducer (PT) to significantly improve key circuit metrics. Compared to reported state-of-the-art interface circuits, such as SSHI (synchronized switch harvesting on inductor), SECE (synchronous electrical charge extraction) and other approaches, the proposed interface circuit completely removes the requirement for an inductor to flip the voltage across the PT. With theoretical calculations, the voltage flip efficiency is 1/3 when only one switched capacitor is employed and this efficiency approaches 80% with 8 switched capacitors. In order to achieve these optimal theoretical voltage flip efficiencies, the capacitances of the switched capacitors should equal to the internal capacitance of the PT. For an SSHI interface circuit to achieve equal voltage flip efficiency, a large inductor is required, which is very impractical in miniaturized systems for real-world implementations. The measured results show that the proposed SSHC interface circuit improves the performance by 9.7$\times$ compared to a full-bridge rectifier. The performance boost is higher than reported inductor-based interface circuits with smaller system volume requirements due to the proposed capacitor-based design and hence a much higher energy efficiency per unit volume is obtained. Future work is currently addressing full on-chip integration of the circuit and switched capacitors for piezoelectric MEMS energy harvesters that could enable a new-class of fully integrated self-powered CMOS-MEMS sensor nodes. The aim of this paper is introduce a new inductorless bias-flip circuit architecture; however, additional features missing in this work can be integrated in future implementations to improve overall performance, such as maximum power point tracking (MPPT), cold-startup, associated switched-capacitor DC-DC converters, integration with electronic loads, etc.

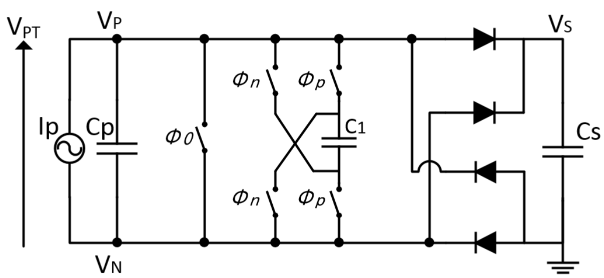


(a) Circuit diagram of an SSHI interface.

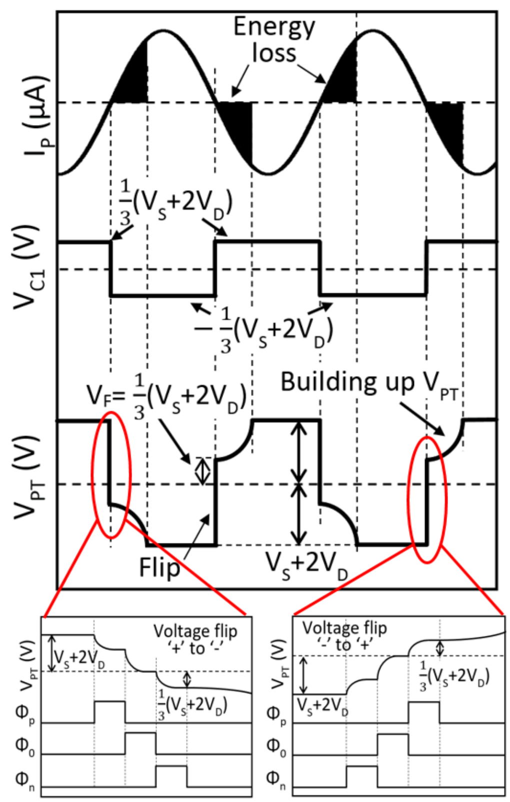


(b) Waveforms.

Fig. 1: SSHI interface circuit and the associated waveforms.

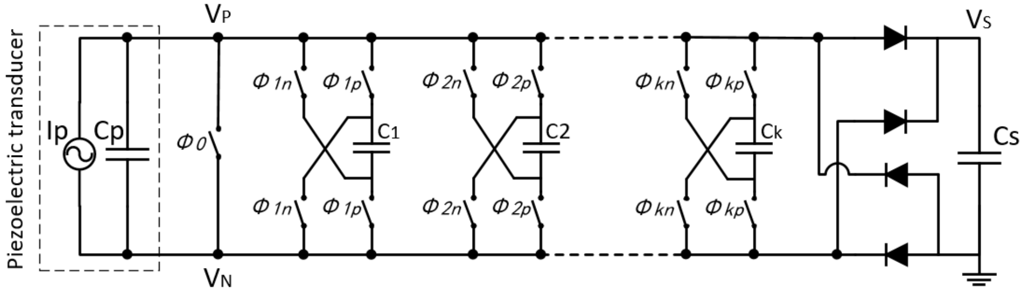


(a) SSHC interface with one charge-swap capacitor.

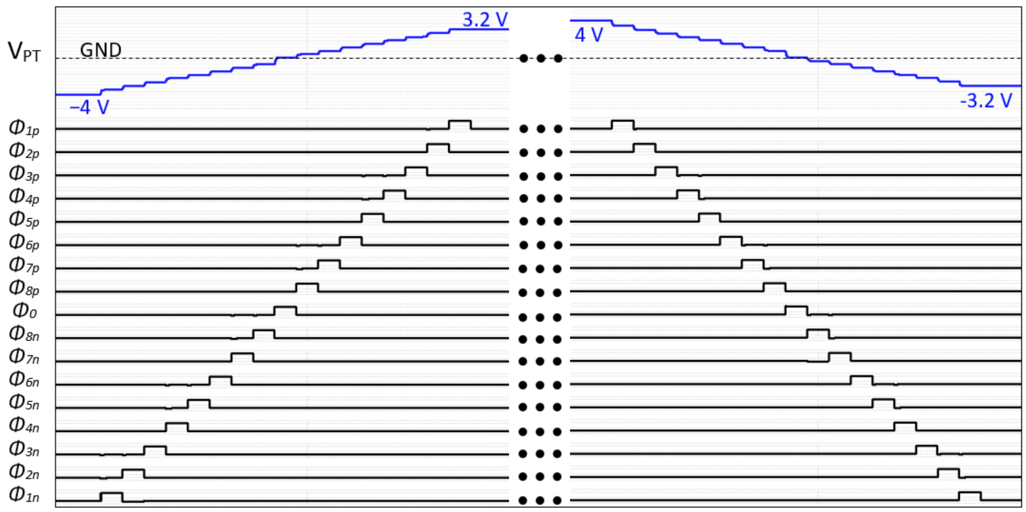


(b) Waveforms.

Fig. 2: Proposed SSHC interface circuit and the associated waveforms.



(a) SSHC interface with k synchronized switched capacitors.



(b) Simulated waveforms of V_{PT} flip instants for the SSHC interface with 8 synchronized switched capacitors.

Fig. 3: Proposed SSHC interface circuit with k synchronized switched capacitors.

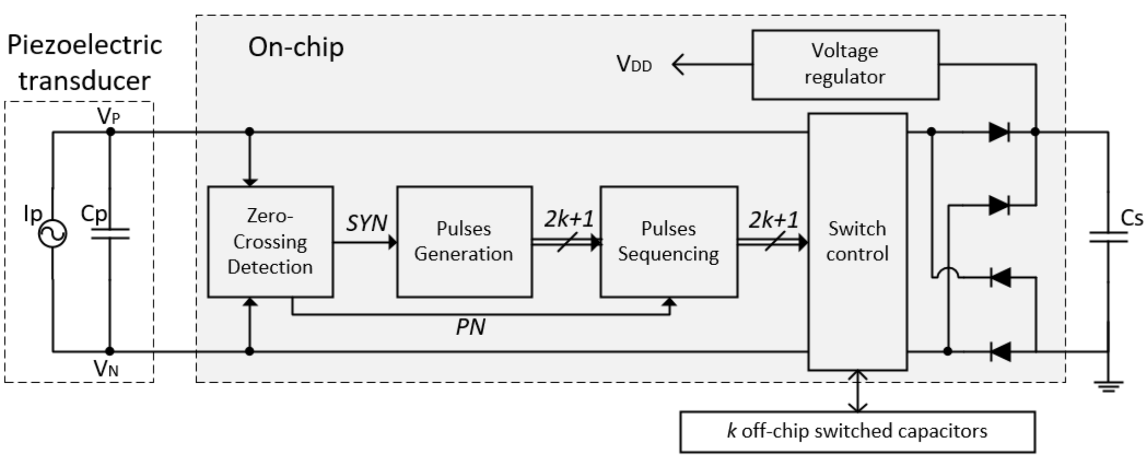
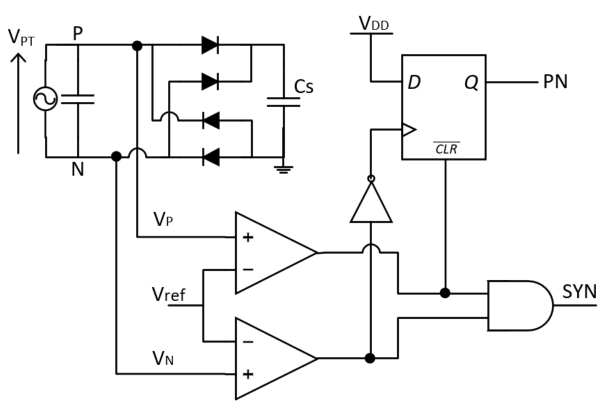


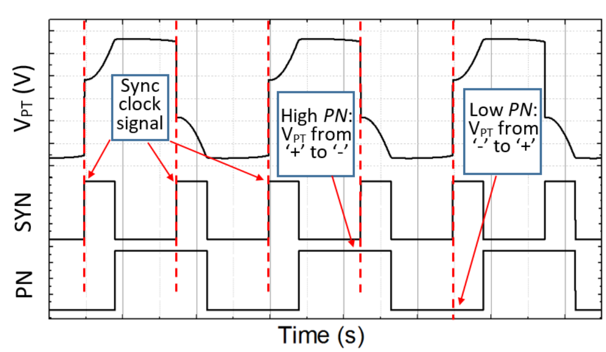
Fig. 4: System architecture of the proposed SSHC interface circuit.

TABLE I: Performance comparison between SSHI and SSHC (equation to calculate L in SSHI is shown in (1) and the assumptions are: η_{SSHI} is shown in the second column, $C_P = 45\,\text{nF}$ and $R = 50\,\Omega$)

SSHC capacitor number	Voltage flip efficiency	Required L for SSHI (mH)
1	1/3	0.26
2	1/2	0.61
3	3/5	1.09
4	2/3	1.71
5	5/7	2.48
6	3/4	3.38
7	7/9	4.42
8	4/5	5.60



(a) Circuit diagram of zero-crossing detection block.



(b) Associated waveforms.

Fig. 5: Zero-crossing detection block.

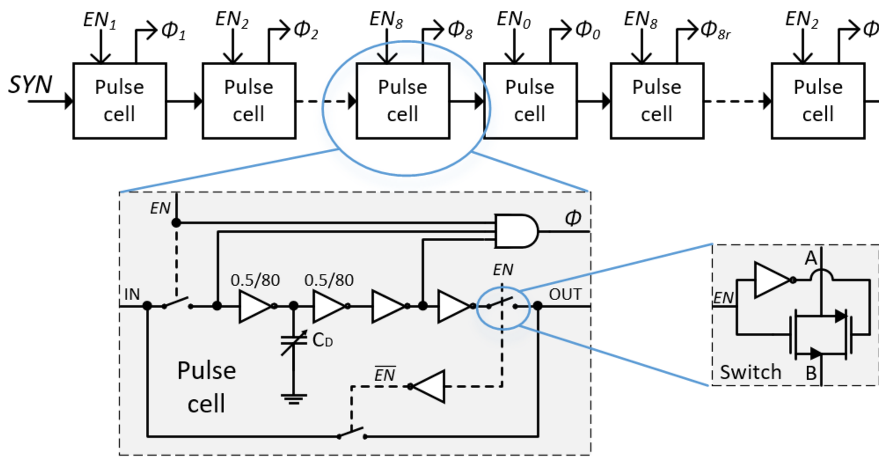


Fig. 6: Circuit diagram of the pulse generation block.

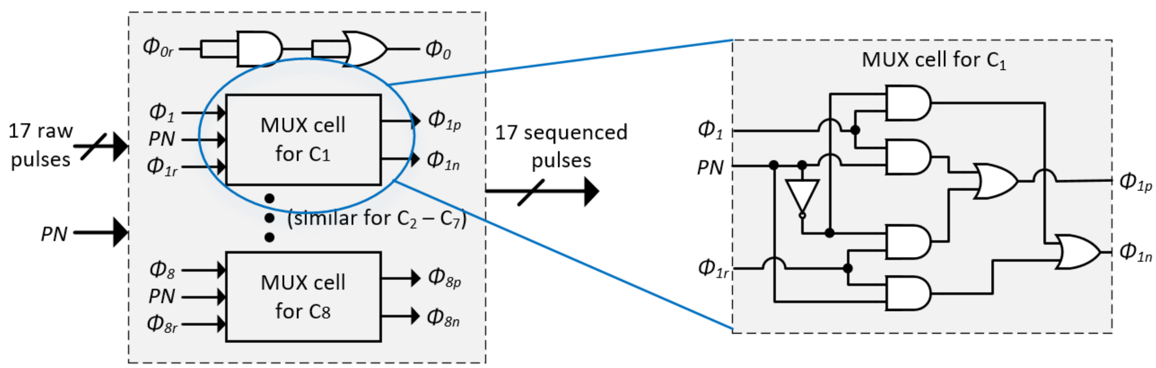


Fig. 7: Circuit diagram of the pulse sequencing block.

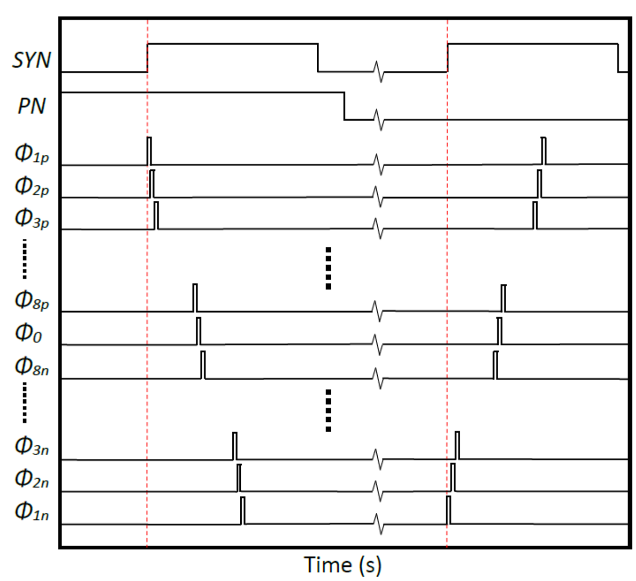


Fig. 8: Associated waveforms of the pulse sequencing block.

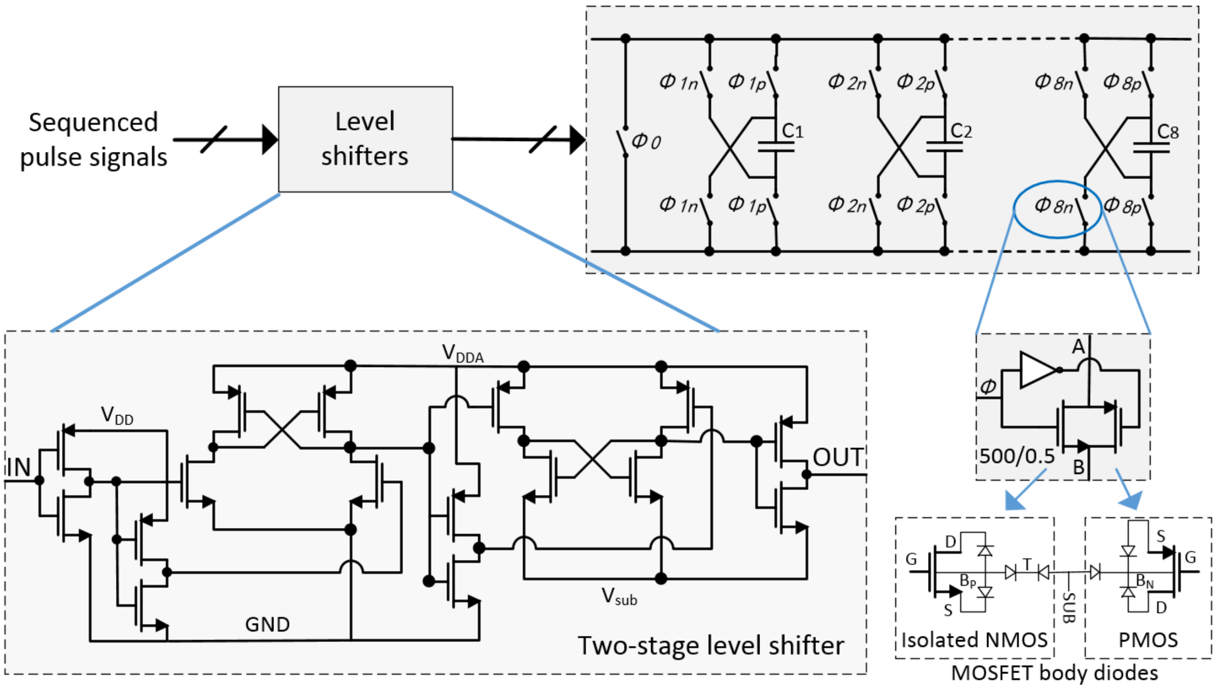


Fig. 9: Circuit diagram of the switch control block.

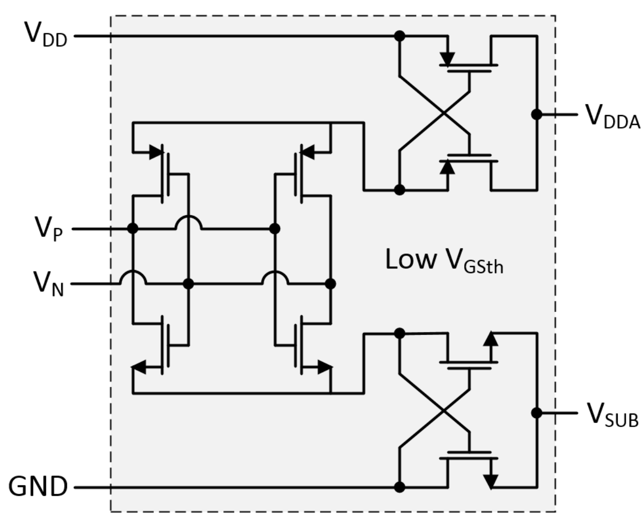


Fig. 10: V_{DDA} and V_{SUB} generation circuit.

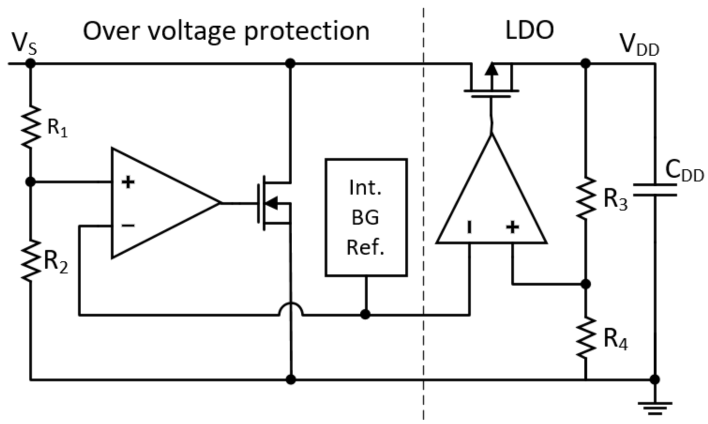


Fig. 11: Circuit diagram of the voltage regulator and over-voltage protection.

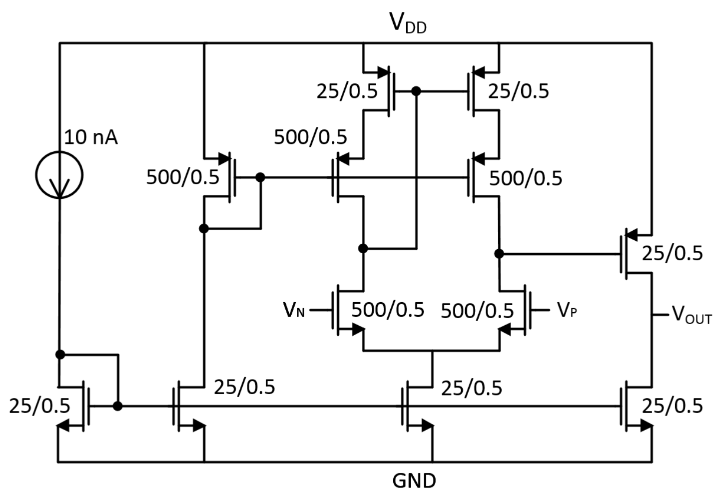


Fig. 12: Circuit diagram of the comparator.

TABLE II: Breakdown of the chip power consumption.

Loss mechanism	Power loss	Percentage
Zero-crossing detection	189 nW	13.2%
Pulse generation	93 nW	6.5%
Pulse sequencing	0.3 nW	0.02%
Switch control	690 nW	48.3%
Voltage regulator	458 nW	32%
Simulated total	1.43 µW	100%
Measured total	$\sim$ 0.9 µW	(static)
Measured total	$\sim$ 1.7 µW	(dynamic)

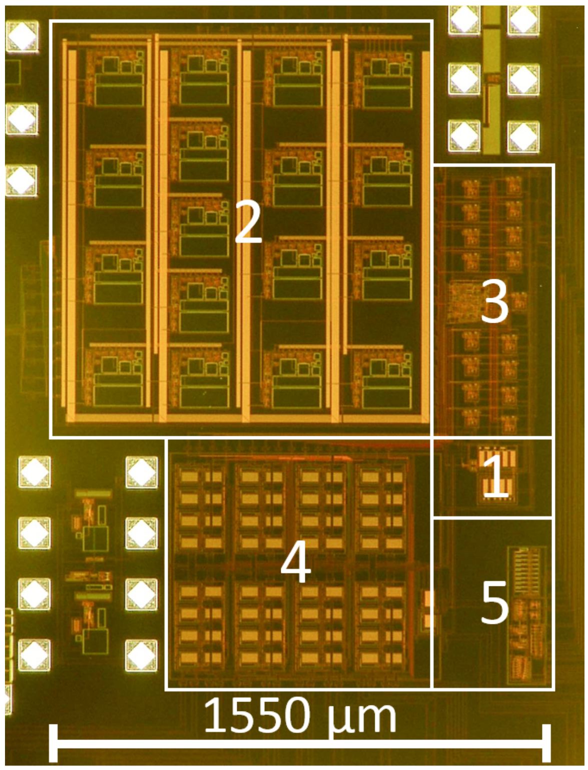
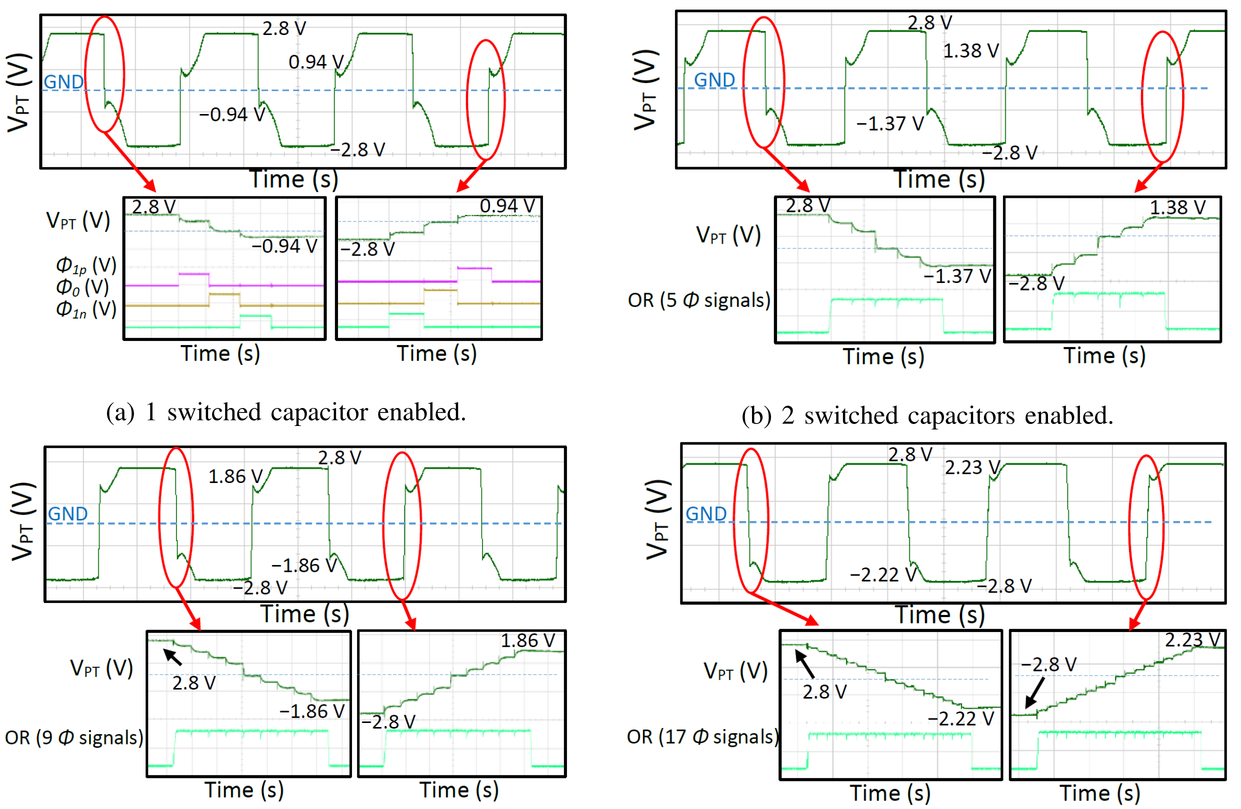


Fig. 13: Micrograph of the test chip fabricated in a $0.35\,\mu\mathrm{m}$ CMOS foundry process. The active area for the proposed circuit is $2.9\,\mathrm{mm}^2$. (1. zero-crossing, 2. pulse generation, 3. pulse sequencing and level shifters, 4. switch control, 5. OVP and voltage regulator).



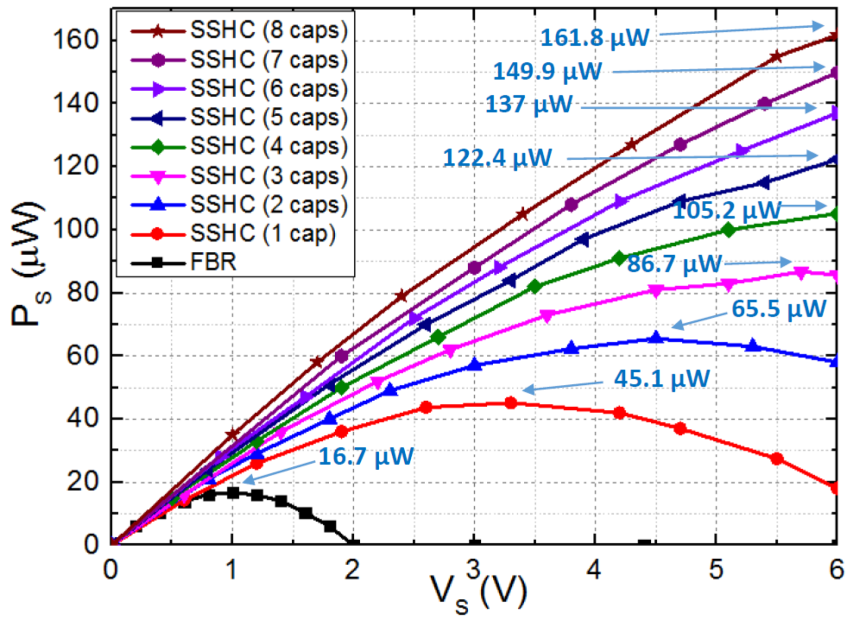
(a) 1 switched capacitor enabled.

(b) 2 switched capacitors enabled.

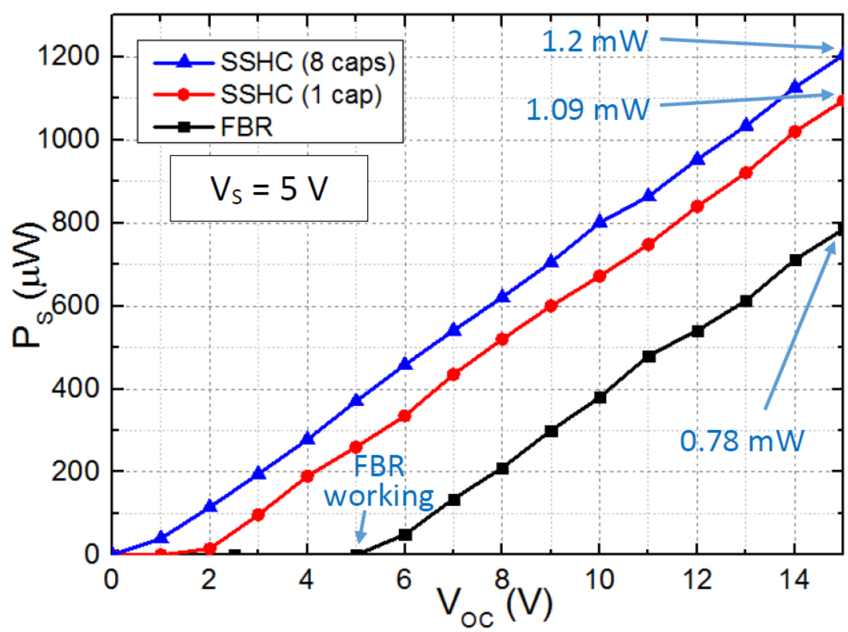
(c) 4 switched capacitors enabled.

(d) 8 switched capacitors enabled.

Fig. 14: Measured transient waveforms of V_{PT} and switch signals (some switch signals are ORed for display due to the limited number of oscilloscope channels).



(a)



(b)

Fig. 15: Measured electrical output power of a FBR and the proposed SSHC interface circuit with up to 8 switched capacitors. (a) Output power in a range of V_S with a fixed $V_{OC} = 2.5\,\mathrm{V}$ (equivalent to an acceleration level $1.2\,\mathrm{g}$). (b) Output power measured over a wide range of excitation levels (up to $V_{OC} = 15\,\mathrm{V}$, equivalent to $7.5\,\mathrm{g}$) with a fixed $V_S = 5\,\mathrm{V}$.

TABLE III: Performance comparison with state-of-the-art interface circuits

Publication	Technique	PT	Piezoelectric capacitance	Frequency	V_{OC}	Inductor	Normalized volume V_{NOR}	$\frac{P_{IC}}{P_{FBR}}$	FOM $= \frac{P_{IC}}{P_{FBR}} \frac{1}{V_{NOR}}$
JSSC2010 [9]	Bias-flip (SSHI)	Mide V22B	18 nF	225 Hz	2.4	820 µH	4.6	4	0.87
JSSC2012 [14]	PSCE	Mide V22B	19.5 nF	173 Hz	9 V	10 mH	46.1	2.1	0.045
JSSC2014 [21]	Energy-investing	Mide V22B	15 nF	143 Hz	2.6 V	330 µH	2.4	3.6	1.5
JSSC2014 [17]	SSHI	Custom MEMS	8.5 nF	155 Hz	8.2 V	470 µH	3	2.5	0.83
TPEL2015 [22]	SSHI	Mide V22B	18 nF	225 Hz	3.28 V	940 µH	5.2	5.8	1.12
TPEL2016 [10]	SECE	Q220-A4303YB	52 nF	60 Hz	2.35 V	560 µH	3.5	3	0.87
ISSCC2016 [23]	SSHI	MIDE V21B	26 nF	134 Hz	2.45 V	3.3 mH	15.9	4.4	0.28
This work	SSHC	Mide V21BL	45 nF	92 Hz	2.5 V	No	$1-1.6$	$2.7-9.7$	$2.7-6.1$

REFERENCES

[1] P. D. Mitcheson, E. M. Yeatman, G. K. Rao, A. S. Holmes, and T. C. Green, "Energy harvesting from human and machine motion for wireless electronic devices," *Proceedings of the IEEE*, vol. 96, no. 9, pp. 1457–1486, 2008.

[2] M. Belleville, H. Fanet, P. Fiorini, P. Nicole, M. J. M. Pelgrom, C. Piguet, R. Hahn, C. Van Hoof, R. Vullers, M. Tartagni, and E. Cantatore, "Energy autonomous sensor systems: Towards a ubiquitous sensor technology," *Microelectronics Journal*, vol. 41, no. 11, pp. 740–745, 2010.

[3] G. Tang, B. Yang, J.-q. Liu, B. Xu, H.-y. Zhu, and C.-s. Yang, "Development of high performance piezoelectric d33 mode mems vibration energy harvester based on pmn-pt single crystal thick film," *Sensors and Actuators A: Physical*, vol. 205, no. 0, pp. 150–155, 2014.

[4] N. Elvin and A. Erturk, *Advances in energy harvesting methods*. Springer Science & Business Media, 2013.

[5] H. S. Kim, J.-H. Kim, and J. Kim, "A review of piezoelectric energy harvesting based on vibration," *International journal of precision engineering and manufacturing*, vol. 12, no. 6, pp. 1129–1141, 2011.

[6] R. Yuan and D. P. Arnold, "An input-powered vibrational energy harvesting interface circuit with zero standby power," *Power Electronics, IEEE Transactions on*, vol. 26, no. 12, pp. 3524–3533, 2011.

[7] A. Harb, "Energy harvesting: State-of-the-art," *Renewable Energy*, vol. 36, no. 10, pp. 2641–2654, 2011.

[8] G. D. Szarka, B. H. Stark, and S. G. Burrow, "Review of power conditioning for kinetic energy harvesting systems," *Power Electronics, IEEE Transactions on*, vol. 27, no. 2, pp. 803–815, 2012.

[9] Y. K. Ramadass and A. P. Chandrakasan, "An efficient piezoelectric energy harvesting interface circuit using a bias-flip rectifier and shared inductor," *Solid-State Circuits, IEEE Journal of*, vol. 45, no. 1, pp. 189–204, 2010.

[10] M. Dini, A. Romani, M. Filippi, and M. Tartagni, "A nanopower synchronous charge extractor ic for low-voltage piezoelectric energy harvesting with residual charge inversion," *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 1263–1274, 2016.

[11] A. Romani, M. Filippi, and M. Tartagni, "Micropower design of a fully autonomous energy harvesting circuit for arrays of piezoelectric transducers," *Power Electronics, IEEE Transactions on*, vol. 29, no. 2, pp. 729–739, 2014.

[12] P. Gasnier, J. Willemin, S. Boisseau, G. Despesse, C. Condemine, G. Gouvernet, and J. J. Chaillout, "An autonomous piezoelectric energy harvesting ic based on a synchronous multi-shot technique," *Solid-State Circuits, IEEE Journal of*, vol. 49, no. 7, pp. 1561–1570, 2014.

[13] S. Du, Y. Jia, C. D. Do, and A. A. Seshia, "An efficient sshi interface with increased input range for piezoelectric energy harvesting under variable conditions," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 11, pp. 2729–2742, 2016.

[14] T. Hehn, F. Hagedorn, D. Maurath, D. Marinkovic, I. Kuehne, A. Frey, and Y. Manoli, "A fully autonomous integrated interface circuit for piezoelectric harvesters," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 9, pp. 2185–2198, 2012.

[15] A. Badel, D. Guyomar, E. Lefeuvre, and C. Richard, "Efficiency enhancement of a piezoelectric energy harvesting device in pulsed operation by synchronous charge inversion," *Journal of Intelligent Material Systems and Structures*, vol. 16, no. 10, pp. 889–901, 2005.

[16] Y. Ammar and S. Basrour, "Non linear techniques for increasing harvesting energy from piezoelectric and electromagnetic micro-power-generators," *arXiv preprint arXiv:0711.3308*, 2007.

[17] E. E. Aktakka and K. Najafi, "A micro inertial energy harvesting platform with self-supplied power management circuit for autonomous wireless sensor nodes," *Solid-State Circuits, IEEE Journal of*, vol. 49, no. 9, pp. 2017–2029, 2014.

[18] A. Badel, G. Sebald, D. Guyomar, M. Lallart, E. Lefeuvre, C. Richard, and J. Qiu, “Piezoelectric vibration control by synchronized switching on adaptive voltage sources: Towards wideband semi-active damping,” *The Journal of the Acoustical Society of America*, vol. 119, no. 5, pp. 2815–2825, 2006.

[19] S. Du, Y. Jia, and A. A. Seshia, “An efficient inductorless dynamically configured interface circuit for piezoelectric vibration energy harvesting,” *IEEE Transactions on Power Electronics*, vol. 32, no. 5, pp. 3595–3609, 2017.

[20] T. Tong, S. K. Lee, X. Zhang, D. Brooks, and G. Y. Wei, “A fully integrated reconfigurable switched-capacitor dc-dc converter with four stacked output channels for voltage stacking applications,” *IEEE Journal of Solid-State Circuits*, vol. 51, no. 9, pp. 2142–2152, 2016.

[21] D. Kwon and G. A. Rincon-Mora, “A single-inductor 0.35 um cmos energy-investing piezoelectric harvester,” *Solid-State Circuits, IEEE Journal of*, vol. 49, no. 10, pp. 2277–2291, 2014.

[22] L. Shaohua and F. Boussaid, “A highly efficient p-sshi rectifier for piezoelectric energy harvesting,” *Power Electronics, IEEE Transactions on*, vol. 30, no. 10, pp. 5364–5369, 2015.

[23] D. A. Sanchez, J. Leicht, E. Jodka, E. Fazel, and Y. Manoli, “A 4uw-to-1mw parallel-sshi rectifier for piezoelectric energy harvesting of periodic and shock excitations with inductor sharing, cold start-up and up to 681extraction improvement,” in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, Conference Proceedings, pp. 366–367.

List of Figures

List of Tables