LISA phasemeter development: Advanced prototyping

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LISA phasemeter development: Advanced prototyping

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Abstract.

We present the status of our investigations on the LISA Phasemeter. The new prototype is based on a custom-designed breadboard with four high-speed ADC and two DAC channels, extended readout capabilities and a large FPGA (field programmable gate array). The required main functionalities and performance of the prototype have been demonstrated in laboratory conditions.

1. Introduction

The main task to be implemented by the LISA Phase Measurement System (PMS) is the phase readout of the beat note coming from the photo-detectors on the optical benches. The required phase sensitivity is $2\pi \times 10^{-6}\,\mathrm{rad}/\sqrt{\mathrm{Hz}}$ on the frequency range from 0.1 mHz to 100 mHz. This corresponds to the detection of pathlength variations between the free floating test masses in the picometer range, required for the observation of gravitational waves. These accuracy in the phase measurements must be ensured over a frequency range of the heterodyne signal between 2 and 20 MHz. Apart from this, the PMS must be able to isolate and extract the phase from the various beat notes contained in the incoming photodiode signal. The most suitable phasemeter architecture, which can provide the required accuracy, is based on a so-called digital phase-locked loop (DPLL) [1, 2]. Once the phase readout has been performed, the back-end processing of the PMS must implement a high bandwidth laser phase-locking control system, as well as inter-spacecraft laser ranging, data communication and clock synchronization [4].

To achieve these goals, a new custom-designed prototype board has been recently manufactured taking as an starting point the experience from previous prototypes [3]. It consists of a multi-channel PMS with high-speed digital processing capabilities, high bandwidth analog input/output interfaces and full signal visibility.

2. Implementation of the digital phase-locked loop

Figure 1 shows a single channel of the developed phasemeter architecture. To avoid aliasing, the incoming signal is processed with an integrated analog LC-filter. After filtering, the signal is digitized in a low-noise analog-to-digital converter (ADC) at 50 MHz sampling rate and fed into the FPGA. Here, the phase detection begins with the multiplication of the incoming beat

note with a sine signal generated by a numerically controlled oscillator (NCO), consisting of a lookup sine table (LUT), phase accumulator (PA) and a phase increment register (PIR). The result of the multiplication, after a low-pass filter (LPF), is proportional to the phase difference between the input signal and the NCO. Therefore, this result can be used as error signal in a control loop to adjust the phase of the NCO to the incoming beat note. This is done with a proportional-integral controller (PIC) that transforms the phase error in a feedback signal for the PIR.

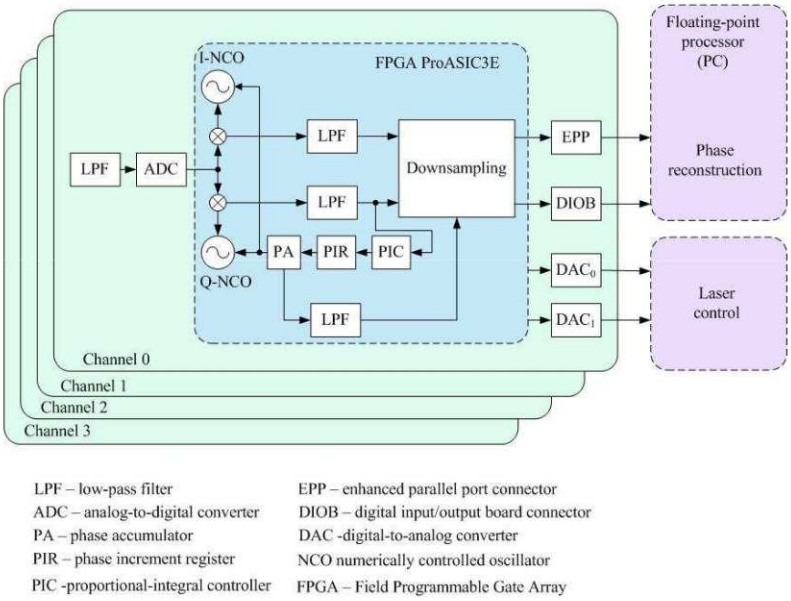

Figure 1. Block diagram of the phasemeter core design.

The primary results of the PMS are the values of the PIR and the PA registers, with correspond to frequency and phase of the input signal, respectively. Additionally, the filtered output signals of the I-LUT and Q-LUT branches can be used for phase measurement corrections. The downsampled data can be readout into a floating-point computing system (e.g. PC) through an integrated enhanced parallel port (EPP). It is also possible to employ a high-speed digital input/output board (DIOB) with direct memory access feature to test internal intermediate results of the PMS, thus providing extended opportunities for investigation of the system and efficient debugging.

3. Phase measurement technique

Figure 2 illustrates the detailed phase reconstruction of the DPLL algorithm presented previously in Section 2. The binary value stored in the phase accumulator (PA), consists of a fixed-point part A and fractional part B with a bit depth N. After multiplication by 2π and proper scaling, its results is the current phase value of the input signal in radians:

$$\varphi = 2A\pi + \frac{B}{2^N}. \tag{1}$$

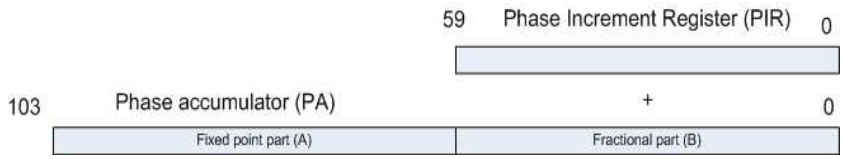

Figure 2. Phase reconstruction using phase accumulator.

4. Hardware Description

Figure 3 shows one of the prototypes of the design presented here that has been recently manufactured. This design implements four channels in one board and provides enhanced processing capabilities. For this purpose, ACTEL FPGAs are the most suitable choice due to their flexibility on design and space-flight compatibility. Our board supports up to 3 Million system gates with 147 high-performance inputs/outputs (I/Os). The software is designed in a very high speed integrated circuit hardware description languages (VHDL).

The digitization of the input beat note signals in the frequency range 2-20 MHz is performed by four A/D-converters (AD9446-100). The current prototype works with an unique internal quartz clock set at 50 MHz, but it is also possible to set an arbitrary clock by mean of an external port. Two D/A converters (AD9744) in combination with output filters are intended to be used for laser frequency stabilization purposes. The characteristics of the DAC enable also two important features for LISA: first, the control of different analog actuators in the LISA setup and second, the implementation of a laser-modulation unit with the use of an electro-optic modulator (EOM). This way, the breadboard can be used in a modulator/demodulator scheme to perform laser ranging [4]. Additionally, the four input channel can measure individually the phase of each quadrant of the photodiodes and deliver alignment signals for orientation control.

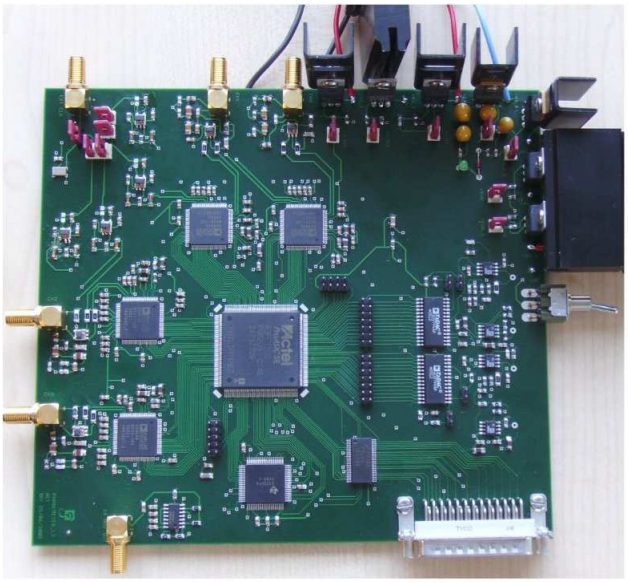

Figure 3. 4-channel prototype of LISA Phasemeter with extended signal processing and readout opportunities. EPP with output rate up to 1 MB/s. Digital input/output (DIO) with maximal rate of 2 GB/s.

5. Experimental results

In contrast to analog-based PMS implementations, a digital development makes it possible to update the firmware and eliminate the temperature drift. However, the digitization process suffers from quantization noise and subsequently the errors in the measurement need to be taken into consideration. In this section we present preliminary results in the assessment of the influence of these noise sources in our design.

Figure 4 presents the results of the first experiment, where the input signal was generated by an additional NCO implemented in the same FPGA as the PMS. The aim of the experiment was to verify the functionality and noise performance of the DPLL. The measurement shows a flat noise floor over the whole frequency range down to 1 mHz, limited only by the quantification noise of the ADC and the finite resolution inside the FPGA. The spikes at high frequencies are currently a subject of investigations, most probably being caused by suboptimal performance of the anti-aliasing filter applied to the output data before decimation.

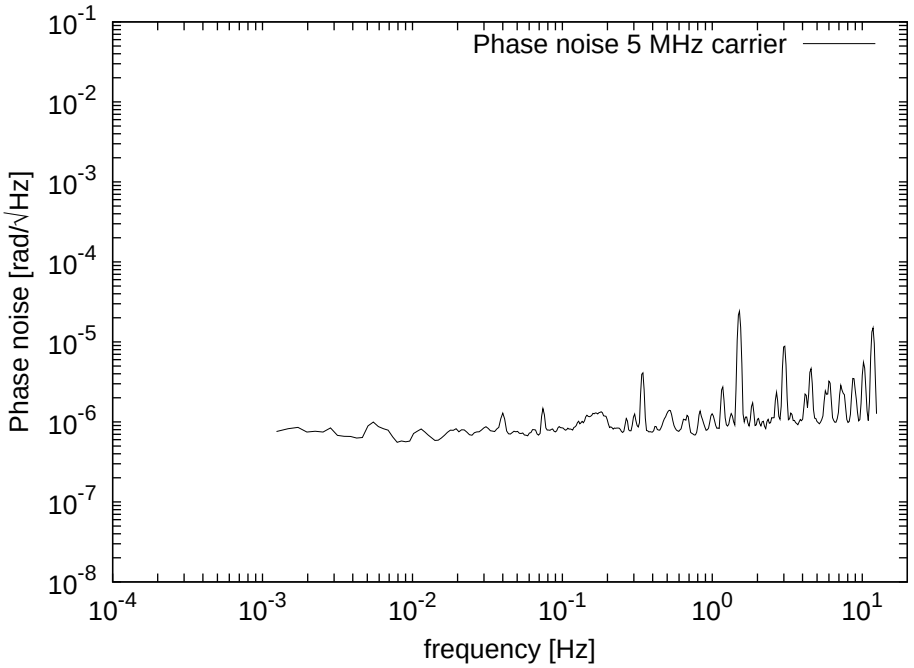

Figure 4. Noise performance of the phasemeter with 5 MHz input signal, generated by an additional NCO implemented in FPGA.

The next experiment was made in more realistic conditions: an external function generator, locked to the clock generator of the phasemeter, was used as input signal. In such conditions all the hardware was tested, including analog frontend and ADCs. The results of the experiment are shown in Figure 5. The noise behavior measured in this configuration is clearly limited by the performance of the external lock used by the PLL of the generator.

Another area of research concerns the back-end processing of the measured phase to perform ranging between the spacecraft: using the current breadboard, a delay-locked loop (DLL) system has been implemented. This system will enable to measure the light propagation time delay. For this purpose, the phase of laser carrier is modulated and a pseudo-random-noise codes (PRN)

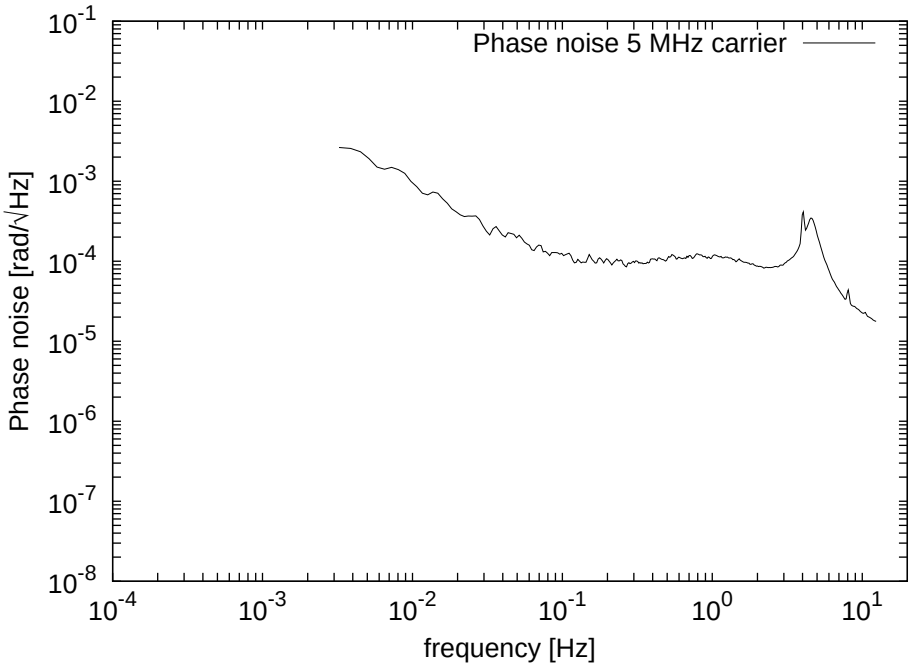

Figure 5. Noise performance of the phasemeter with 5MHz input signal, generated by an external function generator.

are transmitted to the remote satellites. The correlation properties of the PRN enable data communication and synchronization between different spacecraft[4].

6. Conclusions

A custom phasemeter prototype has been developed and its functionality demonstrated with electrical signals. The design aims to implement in a single platform the interferometric phase readout as core processing and a phase-locking control system, optical ranging, data transfer and clock synchronization as back end processing. The experimental results show that the new version of the phasemeter meets the requirement of $2\pi \times 10^{-6}\,\mathrm{rad}/\sqrt{\mathrm{Hz}}$ for the phase readout in the case of internally simulated input signals. We thus conclude that the current prototype can be expected to be a key component for the LISA interferometry test bench.

7. References

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