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Multi-time analysis of CMOS circuits

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MULTI-TIME ANALYSIS OF CMOS CIRCUITS

by

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Abstract

Transient simulation of circuits with widely separated time constants and fast periodic excitations is not efficient because a long simulation period with small time steps is required. One approach to simulate the transient behaviour more efficiently is known as the Multi Partial Differential Equation (MPDE). In the MPDE the system ordinary differential equations that describe a circuit is transformed into a system of partial differential equations with two time variables, one for the fast periodic variations and another for the slow transient evolution. This method has been implemented in a general-purpose circuit simulator program named Carrot. This thesis presents progress towards the development that simulator. The main contributions of this thesis are the implementation and validation of MOSFET models in the simulator and the study of the performance of the MPDE approach (as currently implemented in Carrot) applied to complex CMOS circuits. An overview of concepts relevant for this work is presented, followed by a detailed description of the MOSFET model implementation. Next, the design of an integrated CMOS ring voltage-controlled oscillator is presented. This is followed by simulation case studies. The simulation results indicate that the MPDE approach can achieve orders of magnitude of improvement in simulation speed compared to regular transient analysis. This thesis concludes with recommendations for future research.

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List of Symbols and Abbreviations

AM	Amplitude modulation
A_x	Drain/Source diffusion area
BE	Backward Euler
CAD	Computer-aided design
C_{bd}	Bulk-to-drain capacitance
C_{bs}	Bulk-to-source capacitance
Cd	Capacitance associated with the depleted region
CF	Correction factor
C_{gb}	Gate-to-bulk capacitance
C_{gbo}	Gate-to-bulk overlap capacitance per channel length
C_{gd}	Gate-to-drain capacitance
C_{gdo}	Gate-to-drain overlap capacitance per channel width
C_{gs}	Gate-to-source capacitance
C_{gso}	Gate-to-source overlap capacitance per channel width
CJ	Bulk-junction zero-bias bottom capacitance per area
$CJSW$	Bulk-junction zero-bias sidewall capacitance per length
Cox	Gate-oxide capacitance per unit area
$DELTA$	Empirical parameter
DIBL	Drain-induced barrier-lowing effect
EHB	Envelop harmonic balance
ESD	Electrostatic discharge
ETA	Static feedback on threshold voltage
f	Oscillation frequency
F_b	Taylor series expansion coefficient of bulk charge
FC	Bulk-junction forward-bias capacitance
Fs	Short channel effect correction factor
FM	Frequency modulation
Fn	Narrow channel effect correction factor
g	Transconductance
$GAMMA$	Body-effect parameter
gm	Transconductance
HB	Harmonic balance
I_{bd}	Drain-to-bulk current
I_{bs}	Bulk-to-source current
ICS	Independent current sources
I_{ds}	Drain-to-source current
I_{ss}	Bulk-junction saturation current

J_i	Jacobian matrix
K	Boltzmann's constant
k	Number of iteration
KAPA	Saturation field factor
Kvco	VCO gain
L	Channel length
L_{eff}	Lateral diffusion length
MIM	Metal-insulator-metal
MJ	Bulk-junction bottom grading coefficient
MJSW	Bulk-junction sidewall grading coefficient
MPDE	Multi-time partial differential equation
N	Number of delay cells
n	Number of nodes
n_i	Intrinsic carrier concentration for Si
NFS	Fast surface state density
NSS	Surface state density
NSUB	Substrate doping density
ODES	Ordinary differential equations
OO	Object oriented
PB	Bulk-junction bottom potential
PBSW	Bulk-junction sidewall potential
PHI	Surface inversion potential
PLL	Phase-locked loop
P_x	Drain/Source diffusion perimeter
q	Electronic charge
R_{ch}	Channel resistance
R_d	Drain ohmic resistance
R_s	Source ohmis resistance
S	Distance between the contact via and the channel
THET	Empirical coefficient
TOX	Thin oxide thickness
t_p	Propagation delay
TJ	Absolute temperature
type	Type of MOSFET
UML	Unified modeling language
U_s	Field-related mobility reduction
V	Voltage drop across the diode
V_{bj}	Built-in voltage
V_{bs}	Bulk-to-source voltage
VCCS	Voltage-controlled current sources
VCO	Voltage controlled oscillator
V_{ds}	Drain-to-source voltage

V_{fb}	Flat band voltage
V_{gs}	Gate-to-source voltage
V_{th}	Threshold voltage
$VMAX$	Maximum drift velocity of carriers
V_{on}	Weak inversion voltage
V_{ov}	Overdrive Voltage
VTO	Zero-bias threshold voltage
V_T	Thermal voltage
W	Channel width
WaMPDE	Warped multi-time partial differential equation
Wc	Thickness of the depleted cylindrical region of the source-substrate junction
XJ	Metallurgical junction depth
η	Ideality factor
Φ_{ms}	Work function
σ	Static feedback coefficient
ρ_s	Sheet resistance per square
τ_1	Warped time
τ_2	Slow time

Chapter 1

Introduction

1.1 Motivation

Various circuit simulators are available nowadays to help IC designers shorten their design period. Designers can test their design through simulation before they put their design into the production line. However, the simulation period can be time consuming. Therefore designers should choose simulation methods with caution. In a voltage controlled oscillator (VCO) circuit for example, the oscillation frequency is determined by the input voltage. Thus, if the input voltage and output oscillation frequency are slow varying and fast varying signals respectively, the amount of samples we need to generate a period of the slow time signal is large. This can be expensive in terms of simulation time as well as memory requirements. One remedy to this problem is to treat fast and slow signals separately. Instead of using one time dimension to describe a period of the slow time signal, fast and slow signals are described in two dimensions.

The main objective in this research is to develop a tool to efficiently simulate CMOS circuits with widely separately time variations. This was accomplished by implementing MOSFET transistors models and a circuit analysis based on the MPDE technique in a general-purpose simulation program named Carrot. The MPDE approach in Carrot is implemented in an analysis type named envelope harmonic balance (EHB). A ring voltage controlled oscillator (VCO) was implemented and designed as a case study. The VCO was first designed using the software provided by Cadence and was fabricated through TSMC (Taiwan Semiconductor Manufacturing Corporation). The tools developed in this thesis were used to analyze the VCO.

1.2 Overview

A literature review of MOSFET models, Multi-time simulation method, Object oriented (OO) program architecture, and concepts of companion models are given in Chapter 2. In Chapter 3, the implemented MOSFET models including both DC and AC components are explained. The ring VCO design procedures are given in Chapter 4 along with the simulation results. Due to errors in our design, we were not able to test our circuit so the experimental data is not available. The detailed design errors are given in Appendix A. Chapter 5 compares the performance of the EHB analysis using regular transient analysis as a reference. Since the MOSFET model is not suitable to describe the small geometry transistors built in the ring VCO as discussed in Chapter 4, similar ring VCO topology was redesigned using larger transistors. The design values are documented in Appendix B. The last chapter concludes the thesis and proposes the direction of future work.

Chapter 2

Literature Review

2.1 Introduction

Circuit simulators are essential tools for IC designers as they can predict the physical behaviour of circuits. A circuit simulator usually contains two parts: models and analyses. Models include basic electronic components such as resistors, capacitors, inductors, diodes, transistors and different sources. Models describe the physical behaviour of electronic components using mathematical formulas. Designers should understand what limitations are behind each model and select them carefully to meet design requirements. MOS transistors are one of the components that have been studied extensively after the size of transistors has been scaled down both vertically and horizontally. As the MOS technology trend goes toward nano-meter era, new models appeared to accurately represent the physical behaviour of MOSFETs. DC, AC, and transient analyses are three most commonly used methods to simulate circuits. Transient analysis consists in solving a system of ordinary differential equations (ODEs) in the time domain but it takes a long time to generate signals such as amplitude modulation (AM) signals and frequency modulation (FM) signals [2]. Thus, a multiple-time scale concept [1] is introduced to solve this problem by reducing number of required sampling points so that a shorter computation time is achieved. Multi-time partial differential equation (MPDE), Envelop harmonic balance (EHB), and Warped multi-time partial differential equation (WaMPDE) are methods under the multi-time scale category. This topic is discussed in Section 2.3.

As we mentioned above, each program simulator contains device models as well as analysis methods. In this chapter, the MOSFET models are explained in chronological order in Section 2.2. To further understand how components are implemented in circuit

simulators, concepts of companion models [12, 28] for linear and nonlinear elements are discussed. The architecture of the program simulator is very important as well because a program simulator should be maintained and modified easily if necessary. Lastly, object oriented (OO) practice [21] is one of the techniques being used in many program simulators so we will explain OO techniques which have been applied to some circuit program simulator.

2.2 MOSFET Modeling

Using mathematical models to predict MOS transistor behaviour has been intensively developed for a few decades. The MOS model infrastructure can be categorized into three generations.

The first-generation models are referred to Level 1, Level 2, and Level 3 models. Level 1 model is known as the Schichman-Hodges model [3] which is a simplified version of long-channel devices. Due to its simplicity, it is mainly used in quick hand calculation. Level 2 model is the Geometry-based model [4] and it takes several short-channel effects into account. The main drawback of this model is that the complex mathematical expression may lead to convergence problems. Level 3 model is a semi-empirical model [5], and it is also a simplified version of Level 2. Since this model is easier to handle compared to Level 2, it still remains popular.

The second-generation models include BSIM, HSPICE, and BSIM2 which shifted the focus to circuit simulation and parameter extraction. BSIM stands for Berkeley Short-Channel IGFET Model [6], also referred to as Level 4. It relies on empirical parameters and polynomial equations to handle various physical effects and placed less emphasis on the exact physical formulation. HSPICE (Level 28) [7] is developed by Meta-Software, Inc. and is currently owned by Avant. The model eliminates the negative conductances and derivative discontinuities in BSIM model so it becomes very suitable for analog

circuit design. BSIM2 [8] is an extension version of BSIM. Even thought it repairs problems in BSIM, it is not widely used as parameters are many and very empirical.

The third-generation models are constructed from the usage of a single equation to describe I-V and C-V characteristics along with smooth functions. It solves convergence and discontinuity problems around transition regions. Models are comprised of BSIM3, BSIM4, and EKV Model. BSIM3 model has evolved into three versions: BSIM3v1, BSIM3v2, and BSIM3v3. The first two have many mathematical problems. These are solved by the third one. This model features mobility reduction, carrier velocity saturation, substrate current, subthreshold current, parasitic resistance effects, etc. [9]. BSIM4 is a more advanced model in the BSIM family and many improvements are made over BSIM3 in I-V modeling of intrinsic transistor, noise modeling, extrinsic parasitics, etc. [10]. The EKV model is developed at the Swiss Federal Institute of Technology in Lausanne [11]. The model is uniquely designed from different approaches such that all the voltages are referenced to the substrate contact rather than the source contact. Based on this idea, the model structure is simplified with fewer physical parameters.

2.3 Multi-Time Simulation Methods

Transient analysis is a commonly used method to examine the dynamic behaviour of circuits whose signals are changing with respect to time. The initial condition is either defined by the user or determined from DC operating point analysis. The transient solutions are determined by solving the ordinary differential equations governing the circuit in the time-domain over a specific time period using a time-marching approach. However, this method becomes inefficient when two or more widely time-separated signals appear in the circuit. Many circuits appear to have this characteristic and VCOs are considered as an example. If a slow time-varying signal appears at the input of a VCO and its output signal is fast time-varying, lots of sampling points are required to cover a period of the slow time-varying signal and this results in an expensive computational cost. One solution to this problem is to separate fast and slow variations into different axes

corresponding to different time scales. We are introducing some methods that are based on this idea.

2.3.1 MPDE

MPDE (Multi-time Partial Differential Equation) uses at least two time axes to represent signals with widely separated rates in circuits. Examples are switched-capacitor filters, mixers and switching power converters. Traditional numerical solution of such circuits is difficult to obtain because circuit behaviours vary in different rates. We will use a two-tone quasi-periodic signal [1] as an example to explain how effective this method is compare to the traditional transient analysis. The signal consists of fast and slow time-varying signals at 50KHz and 1KHz respectively so there are 50 fast-varying sinusoids with a period of 20us modulated by a slow-varying sinusoid with a period of 1ms. This two-tone quasi-periodic signal is given as

$$y(t) = \sin\left(\frac{2\pi}{T_1}t\right)\sin\left(\frac{2\pi}{T_2}t\right) \tag{2.1}$$

With traditional transient analysis, if one period of fast time-varying signal contains n sample points, the total number of samples needed for one period of the slow modulation is $n \cdot (T_2/T_1)$. If n is equal to 20, total number of samples was 1000. This signal is shown in Fig. 2.1. If we transfer this signal into multi-time representation

$$\bar{y}(t_1, t_2) = \sin\left(\frac{2\pi}{T_1}t_1\right)\sin\left(\frac{2\pi}{T_2}t_2\right) \tag{2.2}$$

Fewer undulations and sample points are needed to characterize this signal. If 20 points were used in each signal, 400 samples were needed to plot both signals on a uniform 20x20 grid. This corresponding two-periodic bivariate waveform is given in Fig. 2.2.

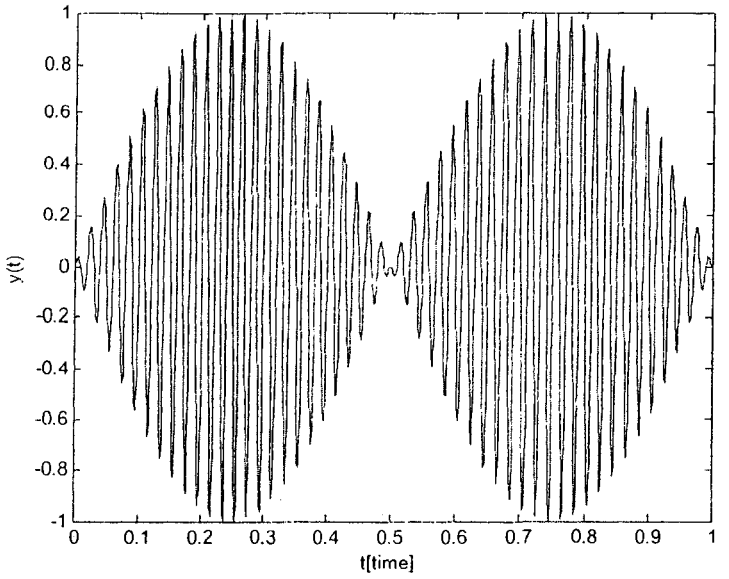

Figure 2.1 Example of two-tone quasi-periodic signal y(t)

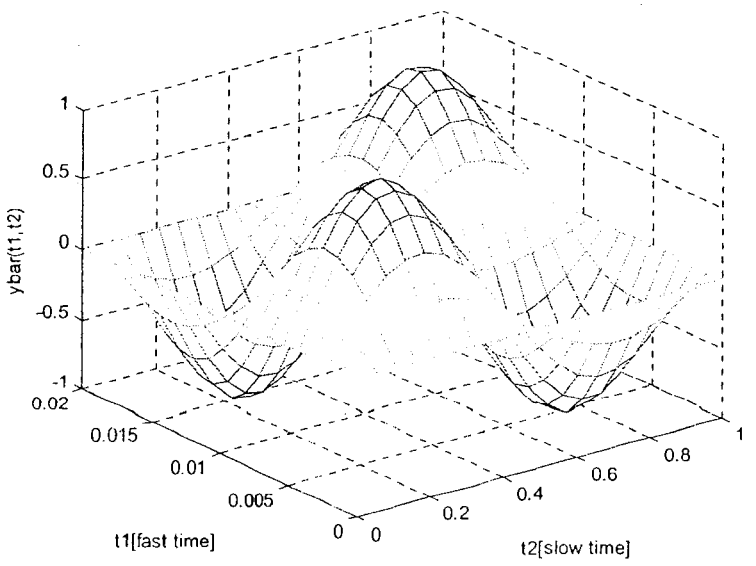

Figure 2.2 Example of two-periodic bivariate waveform

This method replaces the derivative of the system ODEs by

$$\frac{dx(t)}{dt} = \frac{\partial \bar{x}(t_1,t_2)}{\partial t_1} + \frac{\partial \bar{x}(t_1,t_2)}{\partial t_2} \tag{2.3}$$

where t_1 and t_2 represent fast time and slow time respectively

The main advantage of using this method is that it requires fewer sample points compared to the traditional transient analysis so less computation time is required. The above example indicates that this method is used to solve amplitude modulation (AM) signal when two signals have wide-separated rates. Expression $y(t)$ can be recovered by simply setting $t_1 = t_2 = t$ in $\bar{y}(t_1,t_2)$. However, this method is not efficient to solve frequency modulation (FM) signal referred to autonomous systems such as oscillators. Thus, the WaMPDE method is introduced next.

2.3.2 WaMPDE

WaMPDE (Warped Multi-time Partial Differential Equation) also uses at least two time axes to represent signals with widely separated rate in the circuit. Unlike an AM signal, the carrier frequency in the FM signal varies with time and this implies that the number of undulations along with the fast time axis will change with time. WaMPDE warps the fast time scale as a function of the slow time so the frequency is normalized to a constant value. The derivatives in the ODE are replaced by

$$\frac{dx(t)}{dt} = \omega(\tau_2)\frac{\partial \bar{x}(\tau_1,\tau_2)}{\partial \tau_1} + \frac{\partial \bar{x}(\tau_1,\tau_2)}{\partial \tau_2} \tag{2.4}$$

where τ_1 and τ_2 are the warped time and the slow time, respectively. $\omega(\tau_2)$ is an unknown warping function and is set to impose a smooth phase condition along the real

time axis. The result of WaMPDE is a multi-time partial differential equation in warped and real time scale, together with a warped function describing the relation of the two time axes. Consider a two-tone quasi-periodic FM signal shown in Fig. 2.3 [1]

$$x(t) = \cos(\varphi(t)) = \cos(2\pi f_0 t + k\cos(2\pi f_2 t)) \tag{2.5}$$

with $f_0 = 1MHz$ and $f_2 = 20KHz$ and modulation index $k = 8\pi$. The local frequency or instantaneous frequency is modulated by a slow sinusoidal signal

$$f(t) = \frac{1}{2\pi} \cdot \frac{\partial \varphi(t)}{\partial t} = f_0 - kf_2 \sin(2\pi f_2 t) \tag{2.6}$$

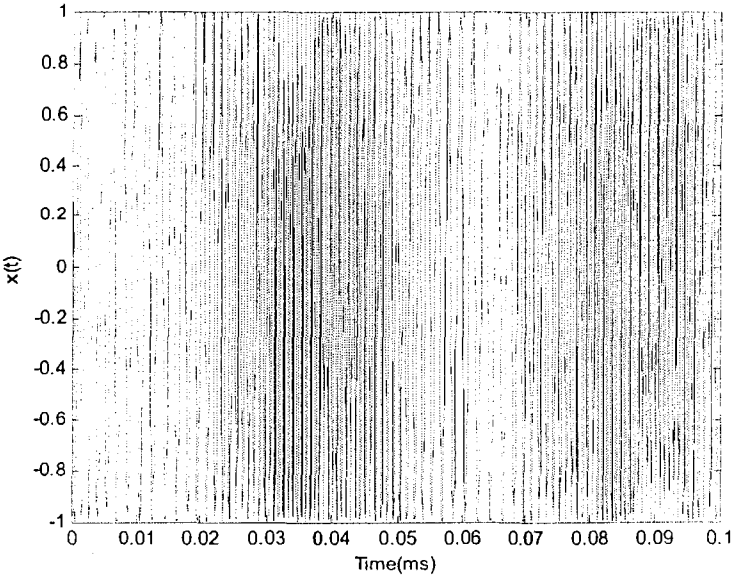

Figure 2.3 Example of the FM signal

We can see that the FM signal is hard to analyze with a two dimensional graph. Let's analyze this FM signal using MPDE method as the fast time and slow time axis represent the oscillation and modulation signals respectively.

The FM signal with multi-time axes is

$$\bar{x}(t_1,t_2)=\cos\left(2\pi f_0 t_1+k\cos\left(2\pi f_2 t_2\right)\right) \tag{2.7}$$

Fig. 2.4 gives a bivariate waveform along both axes. Since many undulations appear in both axes, the MPDE method is not suitable for analyzing FM type signal.

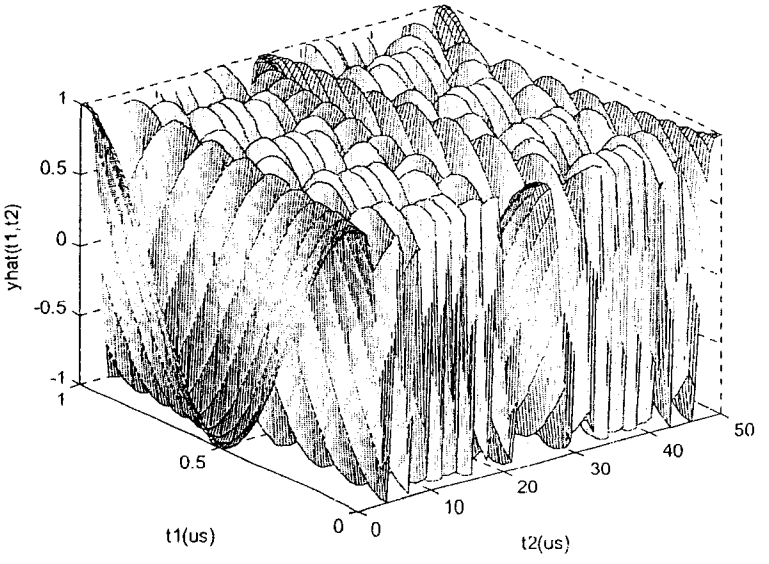

Figure 2.4 Example of the FM signal using MPDE method

If we resolve Eq (2.7) using WaMPDE method, the fast time t_1 is replaced by the warped time τ_1 to normalize the local frequency and τ_2 represents the slow time in real time domain. The new multivariate representation is

$$\bar{x}(\tau_1,\tau_2)=\cos(\tau_1) \tag{2.8}$$

and the warped time becomes a function of time

$$\tau_1 = \phi(\tau_2) = 2\pi f_0 \tau_2 + k\cos(2\pi f_2 \tau_2) \tag{2.9}$$

Eq. (2.8) expresses the FM signal as a function of warped and unwarped time scales. The warped time scale changes the time axis according to a time change to even out the period of the fast undulations. The result of this WaMPDE representation Fig. 2.5 also shows smooth curves on both axes.

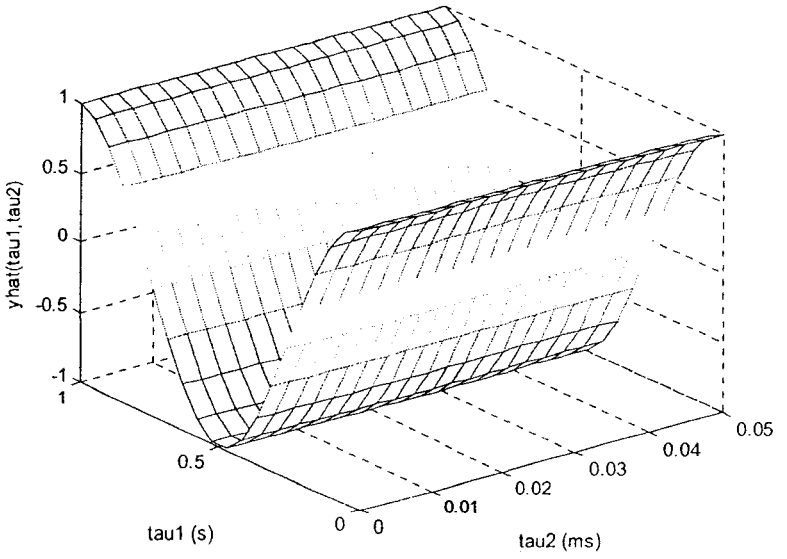

Figure 2.5 Example of the FM signal using WaMPDE method

The results of local frequency are similar between two warped time function. The WaMPDE is efficient to simulate FM signal when two frequencies vary at widely separated rate.

2.3.3 EHB

EHB (Envelope Harmonic Balance) [12] is a particular case of MPDE and it uses two time axes to describe signals with widely separated rates in the circuit. It uses t_1 and

t_2 to represent the fast and slow time axis. Solutions along the fast time axis are solved in the frequency domain using Harmonic Balance (HB) technique. Thus, a good initial guess is usually required for the HB analysis of oscillators to converge to the desired solution. The number of harmonics is usually the same for all state variables and this number is always fixed during the simulation. When a circuit presents strong nonlinearity in a certain node, lots of harmonics are needed for a particular node while other nodes do not need many harmonics. To save the computation effort, minimum harmonics are usually required for desired accuracy in each state variable. The unknowns are the Fourier Coefficients along t_1 corresponding to each value of t_2. The HB technique is based on a Fourier-series expansion of state equations. The key work of HB is to express the state variable x as a Fourier series:

$$x(t_1,t_2) = \Re\left\{\sum_{k=0}^{\infty} X_k(t_2)\, e^{jk\omega_0 t_1}\right\} \tag{2.10}$$

where X_k is the Fourier coefficient of the k_{th} harmonic. Large number of harmonics improves the accuracy but slow the computational speed.

2.4 Companion Models

Companion models [28] are equivalent circuits that represent each circuit component after numerical integration and Newton method are applied. The equivalent circuit can only contain DC current sources and linear transconductances. Thus, a nonlinear dynamic circuit is transformed into a linear DC circuit once the circuit elements are replaced by their companion models. In transient analysis the nonlinear differential equations that describe the circuit are converted into nonlinear algebraic equations by using numerical integration methods. Then the nonlinear algebraic equations are solved by the Newton-Raphson iteration method. This method finds a better estimate solution to the nonlinear equation after each iteration. Circuit components fall into two categories: linear and nonlinear. In addition they are further classified as static or dynamic

components. In this section, we describe some commonly used companion models in circuit simulators.

2.4.1 Linear Transconductances

The current in each branch is given by

$$i = g \cdot v \tag{2.11}$$

where g is a transconductance. i and v are current and voltage respectively. The companion model of a transconductance is shown in Fig. 2.6.

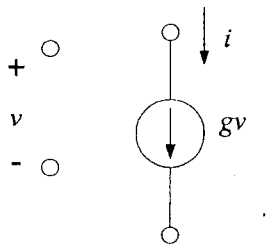

Figure 2.6 Companion model of a linear transconductance

2.4.2 Linear Capacitors

The companion model of a linear capacitor can be derived from the following expression.

$$i = C\frac{dv(t)}{dt} \tag{2.12}$$

The derivative is approximated by using the Backward Euler (BE) method

$$\frac{dv(t_{n+1})}{dt} \simeq \frac{v(t_{n+1}) - v(t_n)}{h} \tag{2.13}$$

Substituting Eq. (2.12) into Eq. (2.13) forms a companion model of linear capacitance

$$i_{n+1} = \frac{C}{h} v_{n+1} - \frac{C}{h} v_n \tag{2.14}$$

Since voltage v_n is known, the second term in Eq. (2.14) can be treated as an equivalent current source (i_{eq}). The voltage v_{n+1} is an unknown value, so the first term uses conductance to represent current flowing through the capacitor. The same idea is applied to express the vector form for this model. Fig. 2.7 gives the equivalent circuit for the capacitance model.

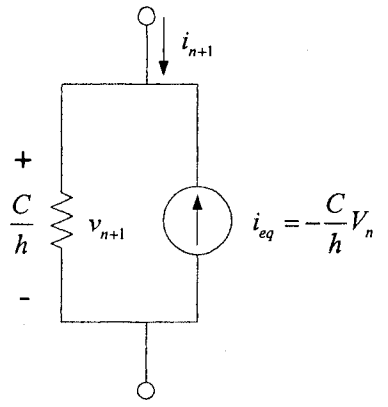

Figure 2.7 Companion model of a linear capacitor

2.4.3 Non-linear Current Sources

Companion models for nonlinear current source can be derived in a similar manner described in Section 2.4.1 with the addition of Newton method. The graphical representation of a non-linear current source controlled by three voltages is given in Fig. 2.8

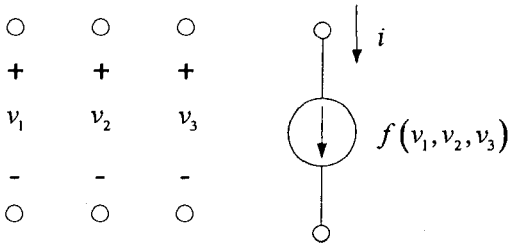

Figure 2.8 Non-linear current source

and its expression is given as $i = f(v_1, v_2, v_3)$. Apply Newton method to that and Eq. (2.15) is obtained.

$$i^{k+1} = i^k + \frac{\partial i}{\partial v}\left(v^{k+1} - v^k\right) \tag{2.15}$$

where k is the iteration number. Current i^{k+1} is a function of three voltages and can be expressed as $i^{k+1} = i\left(v_1^{k+1}, v_2^{k+1}, v_3^{k+1}\right)$ and current i^k is a function of three voltages as well. The partial derivative term is a row vector which is a Jacobian. Then we can write the Eq. (2.15) into its vector form as

$$i^{k+1} = i^k + \begin{bmatrix} \frac{\partial i^k}{\partial v_1} & \frac{\partial i^k}{\partial v_2} & \frac{\partial i^k}{\partial v_3} \end{bmatrix} \begin{bmatrix} v_1^{k+1} - v_1^k \\ v_2^{k+1} - v_2^k \\ v_3^{k+1} - v_3^k \end{bmatrix}$$

The companion model of a nonlinear current source is shown in Fig. 2.9

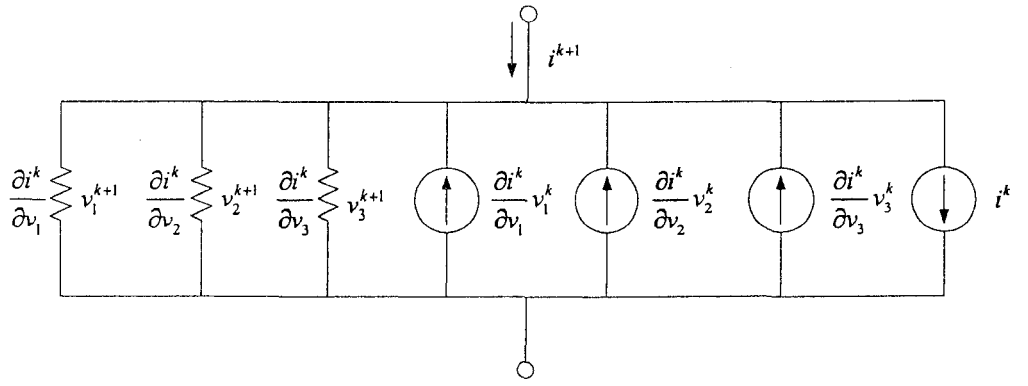

Figure 2.9 Companion model of a nonlinear current source

2.4.4 Non-linear Capacitances

To derive the companion model for a non-linear capacitance, we consider charge as a state variable. By definition, current is equal to the derivative of charge with respect to time and the derivative term is approximated using the BE method.

$$i_{n+1} = \frac{dq(t_{n+1})}{dt} \approx \frac{q(v_{n+1}) - q(v_n)}{h} \tag{2.16}$$

The unknown term $q(v_{n+1})$ can be solved by applying Newton method and its expression is given as

$$q\left(v_{n+1}^{k+1}\right) = q\left(v_{n+1}^{k}\right) + \frac{dq}{dv}\left(v_{n+1}^{k+1} - v_{n+1}^{k}\right) \tag{2.17}$$

Eq. (2.18) shows the mathematical expression of the nonlinear capacitance and this is done by substituting Eq. (2.17) into Eq. (2.16).

$$i_{n+1} = \frac{C_{eq}}{h} v_{n+1}^{k+1} - \frac{C_{eq}}{h} v_{n+1}^{k} + \frac{q\left(v_{n+1}^{k}\right)}{h} - \frac{q(v_n)}{h} \tag{2.18}$$

The term $\frac{dq}{dv}$ is treated as equivalent capacitance. Here, we show the graphical representation of the companion model for one nonlinear capacitance for one controlling voltage in Fig. 2.4.

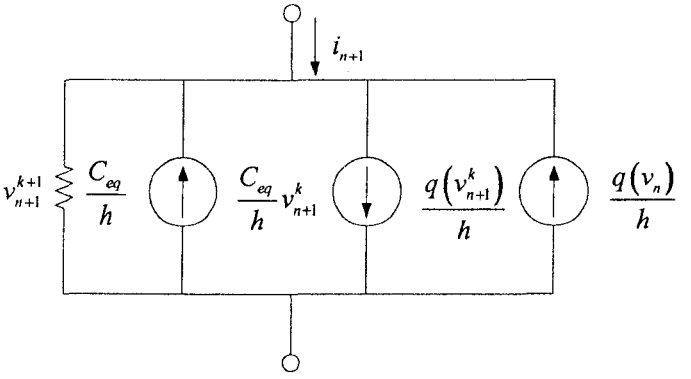

Figure 2.10 Companion model for a nonlinear capacitance

2.5 Object-Oriented Circuit Simulators

Object-oriented (OO) programming [13] uses *objects* to design computer programs. Each object is capable of receiving, processing, and sending data to other objects. An object can be seen as a packet containing data and procedures and may be created from a template such as *class*. A class describes the functionality and behaviour of objects and each object belonging to that class is defined as an *instance*. The procedures inside objects are defined as methods which are executed by sending messages to objects.

Some important features in OO programming are inheritance, polymorphism, and encapsulation. The use of inheritance forms a class hierarchy and allows the reuse of class specifications. Polymorphism is another important feature in OO languages and it allows different object types to share the same common interface. This means that the same message sent to different instances return different results appropriate for each

specific class. In other words, the code can issue the same command to a series of objects and get appropriately different results from each one. Encapsulation treats objects as the building blocks of a complex system and specifies which classes may use members of an object. Each object exposes a certain interface and hides implementation details. UML (Unified Modeling Language) [14] is commonly used language for creating models and describing relationships between models in OO design.

APLAC [21] is an OO circuit simulator implemented in the standard C language using macros. The most important feature of this software is that circuit elements are decomposed into independent and voltage-controlled current sources. Since all models in APLAC are eventually mapped to current sources, the simple nodal analysis is all that is needed to realize nonlinear DC, AC, transient and harmonic balance analyses. Other OO circuit simulators that adopted a common interface for all the circuit elements are ACS and Sframe [15]. The code for each circuit element is separated from the rest of the program. Therefore adding new elements and algorithms to the program requires less effort. ACS and Sframe are both written in C++ and allow one element to be composed of other basic elements. The Carrot simulator [22] developed by Dr. Christoffersen is a computer program simulator runs DC, transient, and multi-time scale analyses. The OO architecture implemented in the software ensures that this software is easy to maintain while new applications are required.

2.6 Reference Circuit Simulators

There are a variety of circuit simulators such as Spice, ngSpice, PSpice, Orcad and others, available in the market. We brief introduce two simulators that were used to verify results from the Carrot simulator. One is the Virtuoso Spectre circuit simulator and another is the Ngspice.

Virtuoso Spectre circuit simulator [29] is provided by Cadence and it combines the industry's leading simulation engines such as SPICE, RF and mixed-signal simulators.

It includes comprehensive device models and is capable of running DC, AC, transient analysis, sensitivity analysis, and others. The post layout verification is another important feature because designers can layout their designs for fabrication. This commercial program has become widely used among universities and industries.

Ngspice [30] is a mixed-mode, mixed signal circuit simulator used for electrical circuit design, simulation and prototyping. It is part of the EDA (electronic design automation) projects in which many people are involved. The project was started because of the lack of free EDA tools for UNIX . This simulator is based on three open source software packages: Spice3, Cider and Xspice.

Spice3 is a general-purpose circuit simulation program originating from the EECS Department of the University of California at Berkeley. It includes built-in models for discrete components such as resistors, capacitors, diodes, and transistors commonly found within integrated circuits Due to its popularity, it has become a standard for simulating circuits.

Cider is a mixed-level circuit and device simulator which was developed from Berkeley as well. It couples the latest version of Spice3 to internal C-based device simulator. It can be used to simulate all the basic types of semiconductor devices and has been ported to a variety of computing platforms.

XSpice is an extended version of the Berkeley's SPICE3 analog circuit simulator and was at the Georgia Tech Research Institute. It provides the ability to use code modeling techniques to add new models so users can create their own models by writing them in the C programming language.

Chapter 3

Mosfet Model Implementation and Testing

3.1 Introduction

Due to the improvement in technology, the size of MOS transistors has been scaled down in dimensions both vertically and horizontally. As the technology goes towards smaller device dimensions, the complexity of the model has increased significantly because some assumptions made in derivations of large transistors are no longer valid. Therefore, there is constant research on modeling small transistors. In general, the perspective of device modeling is to predict device performance with mathematical equations. In addition, modeling also plays an important role in the Computer-Aided Design (CAD) since it is cumbersome to analyze complex circuits using more advance models by hand calculation. Models should be chosen carefully so that their behaviour is close to the actual transistor behaviour over all regions of operation. Designers can use simulators to predict and optimize their chip performance under worst case conditions so that manufacturing tolerances can be incorporated into designs. It is imperative that designers understand the accuracy and limitation of device models in simulators so their designs will function closely to real device and development costs can be reduced.

Models can be derived using physical or empirical approaches or a combination of both. They are usually developed from basic principles and some empirical parameters are later added to improve their accuracy. Therefore, tradeoffs usually are made between the quality of approximation and its complexity. Each model works well with certain parameter values which can be obtained from device level simulator or from electrical

measurements on MOS transistors with different geometries. The accuracy of device models is fully dependent on the model parameters being used.

In this work, a semi-empirical MOS model is implemented into Carrot simulator. Even though this model is not suitable for small geometry devices, it is applicable to long-channel devices with the length greater than 2 μm [20]. Both I-V and C-V characteristics of each component of n-channel and p-channel transistors will be described from a mathematical point of view under different operating conditions. Some correction factors are introduced to modify the existing Level 3 model to ensure smoothness between transition regions. Those correction factors are obtained from the ngSpice source code. Lastly, simulation results for both I-V and C-V characteristics are presented and results are compared against other simulator programs such as ngSpice, and Spectre. Those results indicate how close the MOS model is being implemented in the Carrot simulator compared to others.

3.2 Circuit Simulation Program Architecture

Carrot simulator is a circuit simulator program that can perform DC, Transient, and Envelop Harmonic Balance analyses. It is modular and based on Objected-Oriented (OO) principles. New functionality can be added with no modification to the existing code. Like other simulators, it features standard circuit components such as resistors, capacitors, inductors, diodes, BJTs, MOSFETs, and voltage sources.

The transition from the circuit description to a system of equations is accomplished by decomposing each element in the circuit into either voltage-controlled current sources (VCCS) or independent current sources (ICS). To formulate the circuit equations, a similar current source approach technique as in the APLAC program [21] is used. To formulate the nodal equation at each node with different components, the companion model is applied and the system equation becomes

$$Gu(t) = S(t) \tag{3.1}$$

For example, if a circuit contains linear and nonlinear resistors, the transformation is taken care by the companion models. The above expressions demonstrate how system equations are formed and being solved from the mathematical perspective. Next, we look at how DC analysis is performed in the simulator from its UML class diagram as shown in Fig. 3.1 [22].

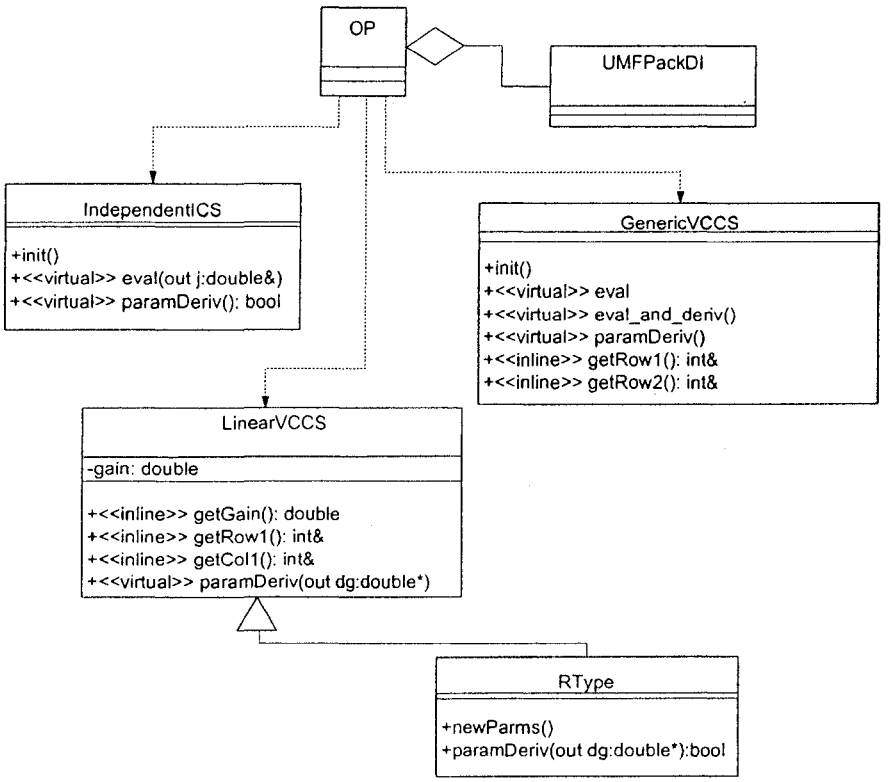

Figure 3.1 UML class diagram of OP class

GenericVCCS, LinearVCCS, and IndependentICS are three classes in the simulator to represent nonlinear, and linear VCCSs, and ICSs respectively. Those classes provide necessary interfaces to build the respective part of the Eq. (3.1). From the companion model point of view, the GeveraicVCCS is used for nonlinear VCCS that

requires Newton iterations. The operating point (OP) is a class that implements DC analysis using Newton method and its dependency to those classes is shown in the above UML diagram. Each class contains inline functions for efficiency where possible and different virtual functions are used for each device model. UMFPackDI is a class to solve linear systems of equations. The OP classes use the information provided by the *CS classes to generate a linear system of equation that is solved by UMFPackDI.

3.3 DC Component Implementation

When it comes to device modeling, more complex models can predict device performance more accurately while more model parameters are required for those models. If the model parameters are not correctly specified, errors may result in device characteristics. Thus, number of unknown parameters and complexity of the model are two important factors to be taken into account when it comes to device modeling. Based on those two factors, we chose to implement the Level 3 semi-empirical model in this work. The MOSFET model required for circuit simulation can be divided into two parts: a steady-state or DC model and a dynamic or AC model. The main difference between those two models is that the former does not vary with time while the later one does. Some of the components in those two models can be further specified as intrinsic and extrinsic parts. In this section, we will discuss only DC MOS transistor models for different regions of device operation.

A basic construction of the n-channel enhancement-type MOSFET has four terminals which are referred to as drain, source, gate, and bulk. The cross section of this typical model is shown in Fig. 3.2. A p-type material is formed from a silicon base and is referred to as the substrate and two n+ regions (the source and the drain) are formed into the substrate. The gate electrode is made of polysilicon on the insulator layer.

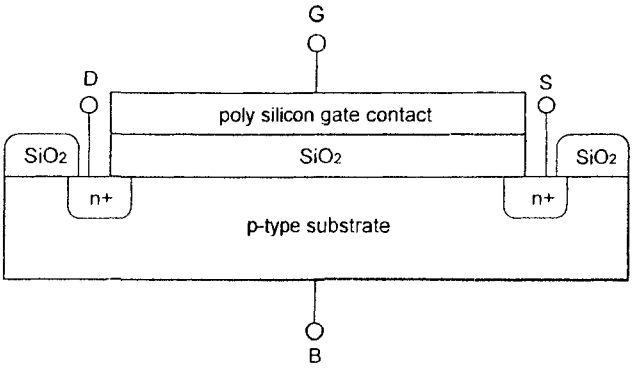

Figure 3.2 Typical enhancement-mode MOS structure

To understand this structure better, we can look at both intrinsic and extrinsic parts of this device. The DC equivalent circuit of this transistor can be seen from Fig. 3.3. For the p-channel MOSFET model, all the voltages and currents are reversed.

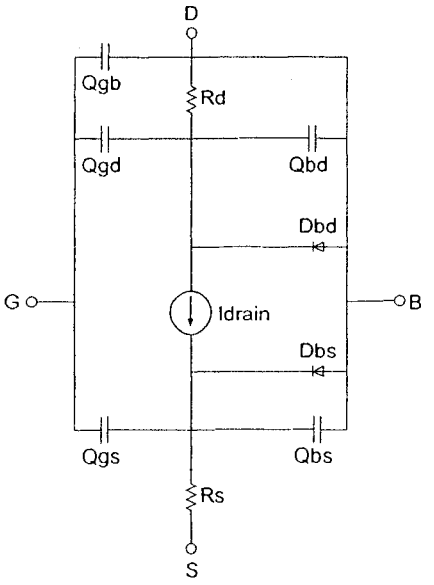

Figure 3.3 Intrinsic model of an n-Channel MOSFET

The extrinsic components are the voltage control current source (Idrain) and two pn junction diodes (Dbs) and (Dbd) connected between terminals from source to bulk and drain to bulk. Under forward operating conditions, it is assumed that the only current flowing through the device is the drain-source current (I_{ds}) and its current-voltage (I-V) form can be expressed as $I_{ds} = f(V_{gs}, V_{ds}, V_{bs})$. V_{gs}, V_{ds}, V_{bs} are gate-to-source, drain-to-source, and bulk-to-source voltage respectively. Under the same operating conditions, the source and drain voltages usually keep source and drain-to-bulk pn junctions reverse biased. The current-voltage relation for both junction diodes can be defined in the same manner such as $I_{bs} = f(V_{bs})$ and $I_{bd} = f(V_{bd})$. The intrinsic elements are also known as parasitic elements which are resistances at the drain, and source terminals. Those elements can limit the drive capability of the device and are usually minimized. For a long channel device, the series resistances R_s and R_d are small. However, as the channel length decreases, those two parasitic resistances can no longer be neglected.

The model equations are usually derived from an NMOS transistor under forward mode operation where drain-to-source voltage is greater than or equal to 0. Table 3.1 shows the drain current with respect to its controlling voltages under both forward and reverse operations. Under the reverse operation, the drain-to-source voltage is less than zero so the voltage is referenced to the drain terminal. The drain current is flowing form source to drain so the controlling voltages are changed accordingly. Current and Voltage values in either forward or reverse mode in the Table 3.1 are suitable for both DC and AC n-channel MOSFEF models

Table 3.1 Drain current and controlling voltages used in an n-channel MOSFET

Mode	I_{ds}	V_{gs}	V_{ds}	V_{bs}
Forward Mode	I_{ds}	V_{gs}	V_{ds}	V_{bs}
Reverse Mode	$-I_{ds}$	$V_{gs} - V_{ds}$	$-V_{ds}$	$V_{bs} - V_{ds}$

The model can be used to handle PMOS transistors as well if currents and controlling voltages are adjusted properly. All voltages are multiplied by -1 under the forward region of operation, so the current can be calculated using the NMOS equations. On the other hand, the roles of drain and source must be changed when the transistor is inverted. Table 3.2 shows modified PMOS current and controlling voltages referenced to an NMOS transistor under both operation conditions.

Table 3.2 Drain current and controlling voltages used in a p-channel MOSFET

Mode	I_{ds}	V_{gs}	V_{ds}	V_{bs}
Forward Mode	I_{sd}	V_{sg}	V_{sd}	V_{sb}
Reverse Mode	$-I_{sd}$	$V_{sg}-V_{sd}$	$-V_{sd}$	$V_{sb}-V_{sd}$

Once the currents and controlling voltages of transistors are specified, there is less chance of making mistakes when calculating currents in each model. To describe how DC models are implemented, we will use a mathematical formula to describe two pn junction diodes, drain-to-source current source, and resistors. Table 3.3 lists parameters used in the diode equations.

3.3.1 Diode Model

Table 3.3 Diode model parameters used in MOSFETs

Parameter	Description	Unit
I_{ds}	Drain-to-source current	(amp)
I_{ss}	Bulk-junction saturation current	(amp)
K	Boltzmann's constant	(CV/K)
q	Electronic charge	(C)

TJ	Absolute temperature	(K)
type	Type of MOSFET	-
V	Voltage drop across the diode	(V)
V_T	Thermal voltage	(V)
η	Ideality factor	-

A simplified mathematical form of diode currents produced from those p-n junctions from bulk (substrate) to source and bulk to drain is

$$I_d = I_{ss}\left[\exp\left(\frac{V}{\eta \cdot V_T}\right) - 1\right] \tag{3.2}$$

I_{ss} is the bulk-junction saturation current; η is the ideality factor which measures how close the ideal curve is to the real one; V is the voltage drop across the diode and V_T is the thermal voltage

$$V_T = \frac{K * TJ}{q} \tag{3.3}$$

To understand the amount of current flow produced at drain to source region, it is essential to specify which region is the transistor operating at. Threshold voltage is one of the most important physical parameters of a MOSFET because it defines the region at which the device starts to turn on. An estimate of threshold voltage can be obtained by extrapolating the region of a square root of I_{ds} versus V_{gs} curve for fixed V_s having maximum slope. As the device geometry is small enough to be comparable with the thickness of the depleted region, the threshold voltage is dependent on the channel width and length. Table 3.4 gives all parameters used in threshold voltage equations.

3.3.2 Threshold Voltage

Table 3.4 Threshold voltage parameters in MOSFETs

Parameter	Description	Unit
Cox	Gate-oxide capacitance per unit area	$(Farad/m^2)$
DELTA	Empirical parameter	-
E_{ox}	Permittivity of oxide	$(Farad/m)$
E_s	Permittivity of Si	$(Farad/m)$
ETA	Static feedback on threshold voltage	-
Fs	Short channel effect correction factor	-
Fn	Narrow channel effect correction factor	-
GAMMA	Body-effect parameter	$(\sqrt{V})$
LD	Lateral diffusion width	(m)
L_{eff}	Lateral diffusion length	(m)
n_i	Intrinsic carrier concentration for Si	$(1/m^3)$
NSUB	Substrate doping density	$(1/m^3)$
NSS	Surface state density	$(1/m^2)$
PHI	Surface inversion potential	(V)
TOX	Thin oxide thickness	(m)
U_s	Field-related mobility reduction	$(m^2/(V \cdot s))$
V_{bj}	Built-in voltage	(V)
V_{ds}	Drain-to-source voltage	(V)
V_{fb}	Flat band voltage	(V)
VMAX	Maximum drift velocity of carriers	(m/s)

V_{th}	Threshold voltage	(V)
VTO	Zero-bias threshold voltage	(V)
Wc	Wc is the thickness of the depleted cylindrical region of the source-substrate junction	(m)
Wp	The thickness of the depleted region on the flat source junction	(m)
XJ	Metallurgical junction depth	(m)
Φ_{ms}	Work function	(V)
σ	Static feedback coefficient	-

The threshold voltage equation given in Eq. (3.4) takes into account the short and narrow channel effects as well as the drain induced barrier lowering effect.

$$V_{th} = V_{bj} - \sigma \cdot Vds + GAMMA \cdot Fs \cdot \sqrt{PHI - V_{bs}} + Fn \cdot \left(PHI - V_{bs}\right) \tag{3.4}$$

The quantity $\sqrt{PHI - V_{bs}}$ used in this equation can cause computation errors if V_{bs} becomes positive and is greater than PHI so some modifications are made as follows.

$$\begin{aligned} &V_{bs} \le 0 \\ &phibs = PHI - V_{bs} \\ &sqphbs = \sqrt{PHI - V_{bs}} \\ \\ &V_{bs} > 0 \\ &phibs = PHI \\ &sqphbs = \frac{\sqrt{PHI}}{1 + 0.5 \cdot \frac{V_{bs}}{PHI}} \end{aligned} \tag{3.5}$$

Then the threshold voltage equation can be rewritten as

$$V_{th} = V_{bj} - \sigma \cdot Vds + GAMMA \cdot Fs \cdot sqphbs + Fn \cdot phibs \tag{3.6}$$

V_{bj} (the built-in voltage) is defined in Eq. (3.7). The parameter *type* represents the type of MOS transistor being selected and the value -1 is used for p-channel MOS transistor and value +1 for an n-channel MOS transistor.

$$V_{bj} = V_{fb} + type \cdot PHI = type \cdot \left(VTO - type \cdot GAMMA \cdot \sqrt{PHI} \right) \tag{3.7}$$

VTO is the extrapolated zero bias threshold voltage of a long and wide channel device and is usually a user defined variable. If not given, it can be obtain from Eq. (3.8).

$$type \cdot VTO = V_{fb} + type \cdot \left(GAMMA \cdot \sqrt{PHI} + PHI \right) \tag{3.8}$$

When the carrier concentration is the same at the surface and at the substrate in the semiconductor, this is called flat-band condition. By definition, the flat band voltage V_{fb} is the voltage difference between the gate and bulk terminals to maintain this condition and is equal to

$$V_{fb} = \Phi_{ms} - \frac{q \cdot NSS}{C_{ox}} \tag{3.9}$$

Φ_{ms} and NSS are the work function and surface state density respectively. Cox (the gate-oxide capacitance per unit area) is defined by the permittivity of oxide divides and the gate oxide thickness.

$$Cox = \frac{E_{ox}}{T_{ox}} \tag{3.10}$$

GAMMA is the body effect parameter and *PHI* is the surface potential for strong inversion. When the strong inversion region occurs in the semiconductor, the opposite type of carrier concentration at the surface is greater than the concentration in the substrate. Eq. (3.11) and Eq. (3.12) describe those two effects where *NSUB* is the substrate doping for either n-channel or p-channel MOS transistor and n_i is the intrinsic carrier concentration for Si.

$$GAMMA = \frac{\sqrt{2 \cdot q \cdot E_s \cdot NSUB}}{C_{ox}} \tag{3.11}$$

$$PHI = 2 \cdot V_T \cdot \left(\frac{NSUB}{n_i} \right) \tag{3.12}$$

In a long-channel device, the surface potential is relatively constant over the entire channel and is independent on changes in V_{ds}, while in the short-channel device, the change in surface potential is noticeable as V_{ds} changes. When V_{ds} increases, the barrier prevents the carriers in the drain from entering the channel diminishes. This results a smaller inversion potential so the device turns on earlier. Since the barrier lowering is caused by the drain-to-source voltage, the effect is so called the drain-induced barrier-lowing (DIBL) effect. σ (the static feedback coefficient) is introduced to describe this effect

$$\sigma = \frac{8.15 \cdot 10^{-22} \cdot ETA}{C_{OX} \cdot L_{eff}^{\ 3}} \tag{3.13}$$

A MOSFET can be defined as a short channel device if the effective channel length L_{eff} is approximately equal to the source and drain junction of XJ. Due to the overlap between the gate and the drain and source junctions, the gate-bulk electrical field depletes less charge resulting in a decrease in the threshold voltage. This effect is due to a share in the total depletion charge of the channel region by the depletion layers of the

source and the drain junctions. The correction takes account of the junction curvature. The short channel effect is calculated as

$$Fs = 1 - \frac{XJ}{L_{eff}} \cdot \left[\frac{LD + Wc}{XJ} \cdot \sqrt{1 - \left(\frac{Wp}{XJ + Wp} \right)^2} - \frac{LD}{XJ} \right] \tag{3.14}$$

The thickness of the depleted region on the flat source junction can be expressed as

$$Wp = XD \cdot sqphbs \tag{3.15}$$

with

$$XD = \sqrt{\frac{2 \cdot E_s}{q \cdot NSUB}} \tag{3.16}$$

Wc is the thickness of the depleted cylindrical region of the source-substrate junction and its empirical formula is given as

$$\frac{Wc}{XJ} = 0.0631353 + 0.8013292 \cdot \frac{Wp}{XJ} - 0.011107 \cdot \left(\frac{Wp}{XJ} \right)^2 \tag{3.17}$$

MOS transistors are referred to as narrow channel devices if they have channel width on the same order of magnitude as the maximum depletion region thickness X_{dm}. Then depletion charge occurs beyond the width of the channel. This additional charge force the gate-bulk filed to increase to balance this charge. Then the threshold voltage increases too. The narrow channel effect correction factor, Fn, models this effect with an empirical parameter *DELTA* introduced to allow flexibility in modeling.

$$Fn = \frac{E_s \cdot DELTA \cdot \pi}{2 \cdot C_{ox} \cdot W} \tag{3.18}$$

The threshold voltage gives designers an idea when the transistor operates in the strong inversion region if its value is less than the grate-to-source voltage. On the other hand, it

is assumed that the there is zero current flow from drain to source if the above condition is false. In fact, this is not true because a concentration of electrons near the surface still exists. A small amount of current flow increases exponentially when V_{gs} approaches V_{th}.

3.3.3 Subthreshold Voltage and Saturation Voltage

Table 3.5 Subthreshold and saturation voltage parameters in MOSFETs

Parameter	Description	Unit
Cd	Capacitance associated with the depleted region	-
F_b	Taylor series expansion coefficient of bulk charge	-
NFS	Fast surface state density	$(atoms/cm^2)$
$THET$	Empirical coefficient	-
V_{dsat}	Saturation Voltage	(V)
V_{on}	Subthreshold Voltage	(V)

In order to distinguish the boundary between the weak (subthreshold) and strong inversion regions, the voltage V_{on} is introduced as

$$V_{on} = V_{th} + n \cdot V_T \tag{3.19}$$

A variable n is used to help the subthreshold expression and is only calculated if the fast surface state density (NFS) is given and not equal to zero. Cd is the capacitance associated with the depleted region.

$$n = 1 + q \cdot \frac{NFS}{Cox} + Cd \tag{3.20}$$

$$Cd = \frac{GAMMA \cdot Fs \cdot sqphbs + Fn \cdot phibs}{2 \cdot phibs} \tag{3.21}$$

Before we explain drain current characteristics in MOS devices, we need to know whether the devices operate in the linear or saturation region. Small amount of drain voltages can induce a channel between source and drain and the channel behaves like a resistor. As the drain voltage increases further, the voltage drop across the oxide near the drain is further reduced to a level required to maintain an inversion layer. The drain voltage at which this happens is denoted by saturation voltage. At this voltage, the channel near the drain disappears and is referred to as pinch-off condition. Once the drain voltage exceeds the saturation voltage, any further increase in drain voltages will not affect the potential at the end of the inversion layer. Also the current will not change significantly under this condition because it depends on the potential drop from the beginning of the inversion layer at the source to the end of inversion layer. In this case, the potential drop remains constant. In short-channel devices, the saturation voltage is reached when the carriers reach the limit of velocity saturation which is before the pinch-off condition. If *VMAX* is not specified, saturation voltage is set to V_a given in Eq. (3.23) otherwise Eq. (3.22) is used.

$$V_{dsat} = V_a + V_b - \sqrt{V_a^2 + V_b^2} \tag{3.22}$$

$$V_a = \frac{V_{gs} - V_{th}}{1 + F_b} \tag{3.23}$$

$$V_b = \frac{VMAX \cdot L_{eff}}{U_s} \tag{3.24}$$

$$F_b = F_n + \frac{GAMA \cdot F_s}{4 \cdot \sqrt{PHI - V_{bs}}} \tag{3.25}$$

$$U_s = \frac{U0}{1 + THET \cdot \left(V_{gs} - V_{th}\right)} \tag{3.26}$$

F_b is the Taylor series expansion coefficient of bulk charge. U_s is the field-related mobility reduction and *THET* is an empirical coefficient. In the short channel device, the carrier velocity in the channel is also a function of the normal (vertical) electric-field component. Since the vertical field influences the scattering of carriers in the surface region, the surface mobility is reduced with respect to the bulk mobility.

3.3.4 Drain-to-Source Current

The drain-to-source current varies as the transistor operates in different regions. Basic drain-to-source current of a MOS transistor used in this model in the linear region is

$$I_{ds} = \frac{\beta \cdot \left(V_{gs} - V_{th} - \left(1 + F_b\right) \cdot V_{ds}/2\right) \cdot V_{ds}}{\left(1 + \frac{U_s \cdot V_{ds}}{L \cdot VMAX}\right) \cdot \left(1 + \theta \cdot \left(V_{gs} - V_{th}\right)\right)} \tag{3.27}$$

where $\beta = \mu_0 \cdot Cox \cdot W/L$. The effects of a short-channel influence the parameters V_{th}, F_s, and β while the narrow-channel effects influence the term F_n. Eq. (3.27) is valid only if the maximum carrier velocity $(VMAX)$ is not equal to zero. If the maximum carrier velocity is set to zero, the correction factor is introduced. Eq. (3.27) is rewritten as

$$I_{ds} = \frac{\beta \cdot \left(V_{gs} - V_{th} - \left(1 + F_b\right) \cdot V_{ds}/2\right) \cdot V_{ds}}{\left(1 + \frac{U_s \cdot V_{ds}}{L \cdot VMAX}\right) \cdot \left(1 + \theta \cdot \left(V_{gs} - V_{th}\right)\right)} \cdot \left(CF\right) \tag{3.28}$$

$$CF = \frac{L_{eff}}{L_{eff} - \sqrt{KAPA \cdot XD^2 \cdot V_{dsat}} \cdot \left(\frac{V_{ds}}{V_{dsat}}\right)^3}$$

The drain-to-source current of a MOS transistor in the saturation region is

$$I_{ds} = \frac{\beta \cdot \left(V_{gs} - V_{th} - \left(1 + F_b\right) \cdot V_{dsat}/2\right) \cdot V_{dsat}}{\left(1 + \frac{U_s \cdot V_{dsat}}{L \cdot VMAX}\right) \cdot \left(1 + \theta \cdot \left(V_{gs} - V_{th}\right)\right)} \cdot \left(\frac{L_{eff}}{L'}\right) \tag{3.29}$$

When the transistor is in the saturation mode, the channel pinch-off point, or the velocity pinch down point starts to move towards the source. This movement is usually referred to as the channel length modulation which is approximated by the last term of Eq. (3.29). The following expressions are used to solve the unknown term L'.

$$L_{eff} - L' = \Delta L \tag{3.30}$$

$$\Delta L = \sqrt{X^2 + KAPA \cdot XD^2 \cdot \left(V_{ds} - V_{dsat}\right)} - X \tag{3.31}$$

$$X = \frac{E_p \cdot XD^2}{2} \tag{3.32}$$

$$E_p = \frac{KAPA \cdot I_{ds} \mid V_{ds} = V_{dsat}}{G_D \mid V_{ds} = V_{dsat} \cdot Leff} \tag{3.33}$$

$$G_D = \frac{\partial I_{ds}}{\partial V_{ds}} \tag{3.34}$$

Once again if the maximum carrier velocity term is set to zero, Eq. (3.31) is replaced by the following expression

$$\Delta L = \sqrt{KAPA \cdot XD \cdot XD \cdot V_{dsat}/8} \cdot \left(V_{ds}/V_{dsat}\right)^3 \tag{3.35}$$

Punchthrough is a phenomena that the I_D increases linearly with the V_D even at gate voltage below an expected threshold voltage. If V_{gs} is held constant while V_{ds} keeps increasing, the drain depletion width will touch the source depletion width causing the level of the energy barrier of the source to drop. This will cause a large amount of current flow even though the gate has been biased to turn the device off. If the condition $\Delta L > 0.5 \cdot Leff$ is true, Eq. (3.31) is modified using the following expression

$$\Delta L = L_{eff}^3 / (4 \cdot \Delta L) \tag{3.36}$$

The above discussions explain the physical characteristic of MOSFETs operating in the strong inversion region. When gate-to-source voltage is less than threshold voltage, this condition is defined as the subthreshold or weak inversion region of operation. The drain-to-source current behaviour changes from square law to exponential in that the subthreshold region conduction is dominated by diffusion current, unlike the strong inversion region where drift current dominates. The current in weak inversion is

$$I_{ds} = I_{on} \cdot \exp\left(\frac{V_{gs} - V_{on}}{n \cdot V_T}\right) \tag{3.37}$$

where I_{on} is the current in strong inversion for $V_{gs} = V_{on}$

$$I_{on} = \frac{\beta \cdot \left(V_{on} - V_{th} - (1 + F_b) \cdot V_{dsx}/2\right) \cdot V_{dsx}}{\left(1 + \frac{U_s \cdot V_{dsx}}{L \cdot VMAX}\right) \cdot \left(1 + \theta \cdot (V_{on} - V_{th})\right)} \tag{3.38}$$

V_{dsx} is the voltage term chosen between the minimum value between drain-to-source voltage and saturation voltage. Fig. 3.4 shows the program code used to implement a pn junction diode in an n-channel transistor. Equations are inserted into corresponding sections. For example, the current equations are voltage dependent so they are placed into the "main evaluation function section". The thermal voltage is temperature dependent so that it is placed into the "variables change with temperature section".

```
// Comments

#ifndef IbdL3_H
#define IbdL3_H 1

class IbdL3_eval {

public:

  enum {vt, MAX_TVAR_INDEX};
  enum {dummy, MAX_CVAR_INDEX};

  IbdL3_eval(int *iparm) {}

  // Main evaluation function. Variable change with voltage
  template <typename currDouble, typename voltDouble, typename
            paramDouble, typename varDouble, typename cvarDouble>
  inline void operator()(currDouble& ibdL3, voltDouble* v,
            paramDouble* dparm, varDouble* tvar, cvarDouble* cvar)
  {

      paramDouble iss = dparm[IS];
      ibdL3 = iss * (safe_exp(v[0]/tvar[vt])-1.);

  }
  // Variables change with temperature
  template <typename tvarDouble, typename varDouble, typename
            tempDouble>
  inline void setTemp(tvarDouble* tvar, varDouble* dparm,
            varDouble* cvar, tempDouble& T)
  {

      tempDouble Tabs = T + tzero;
      tvar[vt] = kBoltzman * Tabs / eCharge;

  }
  // Variables do not change with voltage or temperature
  template <typename varDouble>
  inline void newParms(varDouble* cvar, varDouble* dparm)
  {

  }

};
  // No thermal port
  typedef FADBADGenericVCS<IbdL3_eval, GenericVCCS, 1,
                  MAX_DPARM_INDEX, TEMP, false> IbdL3;

#endif
```

Figure 3.4 Nonlinear voltage controlled current source template

3.3.5 Parasitic Resistors

Two pn junction diodes and the current sources are the intrinsic part of the DC equivalent circuit of the MOSFET. Two series resistances Rs and Rd are considered as parasitic components. They are usually negligible compared to the channel resistance R_{ch} and this is true for long channel devices as the channel resistance is directly proportional to channel length L. Parasitic resistances can be formulated by adding the sheet resistance, contact resistance, and spreading resistance together. For simplicity, these resistances can be specified in terms of the sheet resistance and the number of squares of diffused region in series to the drain and source regions. Table 3.6 summarized parameters used in those intrinsic resistors.

Table 3.6 Parasitic resistor parameters in MOSFETs

Parameter	Description	Units
N_{RD}	Relative resistivity of the drain	$(square)$
N_{RS}	Relative resistivity of the source	$(square)$
R_{ch}	Channel resistance	$(\Omega/square)$
R_d	Drain ohmic resistance	(Ω)
R_s	Source ohmis resistance	(Ω)
S	Distance between the contact via and the channel	(m)
ρ_s	Sheet resistance per square	$(\Omega/square)$

$$R_d = R_{ch} \cdot N_{RD} \tag{3.39}$$

$$R_s = R_{ch} \cdot N_{RS} \tag{3.40}$$

The sheet resistance R_{ch} can be defined by users or calculated using Eq. (3.41) and the relative resistivity of the drain and source depend on the transistor layout.

$$R_{ch} = \frac{\rho_s \cdot S}{W} \tag{3.41}$$

Those two parasitic resistances can be implemented as linear voltage controlled current sources. Instead using resistance value in the program, the transconductance will be used instead. The program template is shown in Fig. 3.5.

```
// Comments

#ifndef RdType_H
#define RdType_H 1

class Rd_eval {
public:

  Rd_eval(int *iparm) {} // iparm not needed here

  // Main evaluation function. Only voltage dependence considered here.
  template <typename myDouble>
  inline void operator()(myDouble& g, myDouble* dparm)
  {

  myDouble r;
  myDouble Rch;

      Rch = dparm[THOU]*dparm[S]/dparm[W];
      R = Rch*dparm[NRD];
      g = 1./r;
  }

};

typedef FADBADLinearVCS<RI_eval, LinearVCCS, MAX_DPARM_INDEX> RdType;

#endif
```

Figure 3.5 Linear voltage controlled current source template

3.4 AC Component Implementation

A capacitance model can be divided into two parts: the intrinsic part and extrinsic part. The intrinsic capacitances are those which form the channel region of the device such as C_{gs}, C_{gd}, and C_{gb}. The extrinsic or parasitic capacitances include the overlap capacitances and pn junction capacitances. Overlap capacitances (C_{gso}, C_{gdo}, and C_{gbo}) are the capacitances of the gate with respect to the other three terminals and the source and drain pn junction capacitances are C_{bs} and C_{bd}.

Meyer's capacitance model is a widely used capacitance model and has been adopted in the program simulator such as SPICE. However, some problems such as the non-conservation and discontinuity exist in this model [23,24]. Three nonlinear capacitance equations in this model are expressed as functions of the terminal voltages, so the charge is obtained through the expression of

$$Q = \int_{v1}^{v2} C(v)\,dv$$

For a nonlinear capacitance, even though the voltage starts at a particular point and ends at the same value, the computed charge is different if different intermediate voltage steps are taken. The discrepancy increases even more when nonlinear capacitances depend on more than one controlling voltage. Another problem of this capacitance model is that discontinuities occur between transition regions and this slows down the convergence process when Newton method is applied. To solve both charge conservation and discontinuity problems, we implemented the simplified Yang-Chatterjee charge model [24] into the program simulator to describe the behaviour of three nonlinear capacitors. The following equations are used to describe the NMOS transistor. To calculate the charge in PMOS transistor, the polarities of the charges in those equations remain unchanged but the source charge is calculated using the drain charge equation and vice versa. This capacitance model divides the MOS model into four different regions of

operation which uses the analytical equation for the charge instead of approximations. Some intermediate quantities are defined in Eq. (3.42) and Eq. (3.43) first.

$$V_{fb} = V_{t0} - GAMMA \cdot \sqrt{PHI} - PHI \tag{3.42}$$

$$C_0 = C_{OX} \cdot W \cdot L_{eff} \tag{3.43}$$

The charge equations are used to explain this MOS capacitor model under different bias conditions: accumulation, depletion, and inversion [25]. When a negative bias voltage is applied to the gate terminal, this results in a negative charge on the gate and then the positive charge is induced at the silicon surface. Then the excess hole concentration in the p-type silicon is created at the surface. This is referred to as the accumulation condition since holes are accumulated at the surface.

Table 3.7 Parameters used in the simplified Yang-Chatterjee charge model

Parameter	Description	Units
C_{gbo}	Gate-to-bulk overlap capacitance per channel length	$(Farad/m)$
C_{gdo}	Gate-to-drain overlap capacitance per channel width	$(Farad/m)$
C_{gso}	Gate-to-source overlap capacitance per channel width	$(Farad/m)$
Q_b	Bulk Charge	$(coulomb)$
Q_d	Drain Charge	$(coulomb)$
Q_s	Source Charge	$(coulomb)$

Accumulation region $V_{gs} \le V_{fb} + V_{bs}$

$$\begin{aligned} Q_d &= 0 \\ Q_s &= 0 \\ Q_b &= -C_0 \cdot \left(V_{gs} - V_{fb} - V_{bs}\right) \end{aligned} \tag{3.44}$$

As the gate voltage is slowly increased, a positive voltage at the gate places positive charge on it. Then, holes are repelled from the surface. In other words, a positive charge on the gate induces a negative charge at the silicon surface. Since holes are depleted at the surface, it is referred to as the depletion condition.

Depletion region $V_{fb} + V_{bs} < V_{gs} \le V_{th}$

$$\begin{aligned} Q_d &= 0 \\ Q_s &= 0 \\ Q_b &= -C_0 \cdot \frac{GAMMA^2}{2} \cdot \left\{ -1 + \sqrt{1 + \frac{4 \cdot \left(V_{gs} - V_{fb} - V_{bs}\right)}{GAMMA^2}} \right\} \end{aligned} \tag{3.45}$$

As the gate voltage increases further, electrons are attracted to the surface. At a particular voltage level, the electron density at the surface exceeds the hole density. The surface has inverted from the p-type polarity of the original substrate to an n-type. This is referred to as the inversion region. Saturation region and linear region are two regions under the inversion category.

Saturation region $V_{th} < V_{gs} \leq V_{ds} + V_{th}$

$$\begin{aligned} Q_d &= 0 \\ Q_s &= -\frac{2}{3} \cdot C_0 \cdot \left(V_{gs} - V_{th}\right) \\ Q_b &= C_0 \cdot \left(V_{fb} + PHI - V_{th}\right) \end{aligned} \tag{3.46}$$

Linear region $V_{gs} > V_{ds} + V_{th}$

$$\begin{aligned} Q_d &= -C_0 \cdot \left[\frac{V_{ds}^2}{8 \cdot \left(V_{gs} - V_{th} - 0.5 \cdot V_{ds}\right)} + \frac{V_{gs} - V_{th}}{2} - \frac{3}{4} \cdot V_{ds}\right] \\ Q_s &= -C_0 \cdot \left[\frac{V_{gs} - V_{th}}{2} + \frac{1}{4} \cdot V_{ds} - \frac{V_{ds}^2}{24 \cdot \left(V_{gs} - V_{th} - 0.5 \cdot V_{ds}\right)}\right] \\ Q_b &= C_0 \cdot \left(V_{fb} + PHI - V_{th}\right) \end{aligned} \tag{3.47}$$

The overlap capacitance can be treated as linear capacitance as charges are proportional to the voltage on the terminals. The amount of charge at drain, gate, and source terminals are

$$\begin{aligned} Q_s &= W \cdot C_{gso} \cdot V_{sg} \\ Q_d &= W \cdot C_{gdo} \cdot V_{dg} \\ Q_b &= L \cdot C_{gbo} \cdot V_{bg} \end{aligned} \tag{3.48}$$

Table 3.8 Parameters used in the depletion capacitance

Parameter	Description	Units
A_x	Drain/Source diffusion area	(m^2)
C_{bx}	Zero bias bulk-to-drain/source capacitance	$(Farad)$
C_{bxj}	Bulk-to-drain/source area capacitance	$(Farad)$
C_{bxs}	Bulk-to-drain/source sidewall capacitance	$(Farad)$
C_{gbo}	Gate-to-bulk overlap capacitance per channel length	$(Farad/m)$
C_{gdo}	Gate-to-drain overlap capacitance per channel width	$(Farad/m)$
C_{gso}	Gate-to-source overlap capacitance per channel width	$(Farad/m)$
CJ	Bulk-junction zero-bias bottom capacitance per area	$(Farad/m^2)$
$CJSW$	Bulk-junction zero-bias sidewall capacitance per length	$(Farad/m)$
MJ	Bulk-junction bottom grading coefficient	-
$MJSW$	Bulk-junction sidewall grading coefficient	-
P_x	Drain/Source diffusion perimeter	(m)

The bulk-source/drain depletion capacitances are composed of bulk-source/drain area capacitance and bulk-source/drain sidewall capacitance. Their mathematical expression is given in Eq. (3.49).

$$C_{bx} = A_x * CJ * C_{bxj} + P_x * CJSW * C_{bxs} \tag{3.49}$$

The charge are calculated by integration using the boundary condition

$$Q_{bx} = A_x * CJ * Q_{bxj} + P_x * CJSW * Q_{bxs} \tag{3.50}$$

Then the following equations show the capacitance models under different regions of operations

if $V_{bx} \le FC * PB$

$$C_{bx} = \frac{A_x \cdot CJ}{\left(1 - \frac{V_{bx}}{PB}\right)^{MJ}} + \frac{P_x \cdot CJSW}{\left(1 - \frac{V_{bx}}{PB}\right)^{MJSW}} \tag{3.51}$$

$$Q_{bx} = A_x * CJ * Q_{bxj} + P_x * CJSW * Q_{bxs} \tag{3.52}$$

with

$$Q_{bxj} = K2 * \left[1 - \left(1 - V_{bx}/PB\right)^{K1}\right]$$
$$K1 = 1 - MJ$$
$$K2 = PB/K1$$

$$Q_{bxs} = K6 * \left[1 - \left(1 - V_{bx}/PBSW\right)^{K5}\right]$$
$$K5 = 1 - MJSW$$
$$K6 = PBSW/K5$$

if $V_{bx} > FC * PB$

$$C_{bx} = \frac{A_x \cdot CJ}{\left(1 - FC\right)^{1+MJ}} \cdot \left(1 - FC \cdot \left(1 + MJ\right) + \frac{MJ \cdot V_{bx}}{PB}\right) + \frac{P_x \cdot CJSW}{\left(1 - FC\right)^{1+MJSW}} \cdot \left(1 - FC \cdot \left(1 + MJSW\right) + \frac{MJSW \cdot V_{bx}}{PB}\right) \tag{3.53}$$

$$Q_{bx} = A_x * CJ * Q_{bxj} + P_x * CJSW * Q_{bxs} \tag{3.54}$$

with

$$Q_{bxj} = K3 \cdot \left[K4 \cdot \left(V_{bx} - FC \cdot PB \right) + \frac{MJ}{2 \cdot PB \cdot \left(V_{bx}^2 - \left(FC - PB \right)^2 \right)} \right]$$

$$K3 = \left(1 - FC \right)^{-(1+MJ)}$$

$$K4 = 1 - FC * \left(1 + MJ \right)$$

$$Q_{bxs} = K7 * \left[K8 * \left(V_{bx} - FC * PB \right) + \frac{MJSW}{2 \cdot PBSW \cdot \left(V_{bx}^2 - \left(FC - PB \right)^2 \right)} \right]$$

$$K7 = \left(1 - FC \right)^{-(1+MJSW)}$$

$$K8 = 1 - FC * \left(1 + MJSW \right)$$

The capacitance models based on the charge equation are implemented into Carrot's simulator. Similar template is used to implement this charge model as we presented before.

3.5 Model Verification

To verify the accuracy of DC and AC components implemented in the Carrot simulator, we ran dc analysis to gather the operating points for both n-channel and p-channel MOFETs. Results were plotted and compared to two other program simulators which are ngspice and Spectre. Fig. 3.6 and Fig. 3.7 give the biasing voltage and current characteristic for an n-channel MOSFET under two different velocity saturations. Length of the transistor was set to 3 micrometers and its parameters were found in [26]. Drain-to-source voltage was set to 0.8 volt so that transistors were able to operate in all regions as the biasing voltage at the gate terminal was swept.

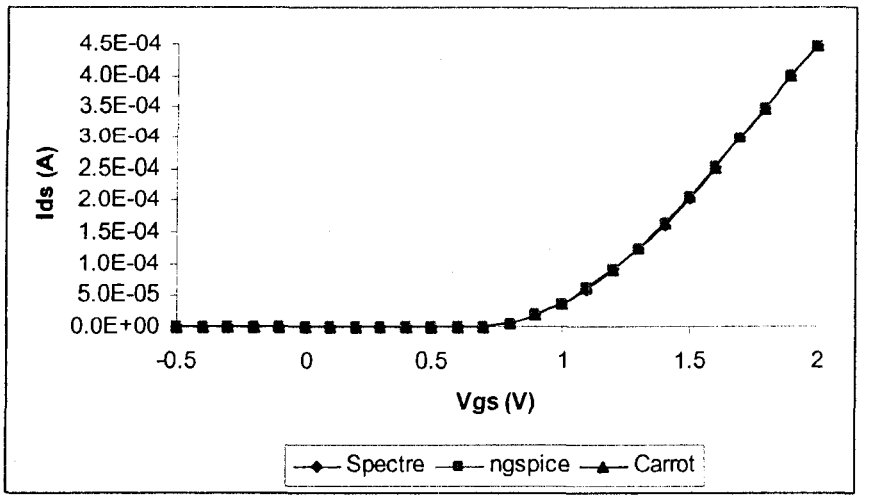

Figure 3.6 Vgs vs Ids at Vmax=1e5 and (W/L=30u/3u)

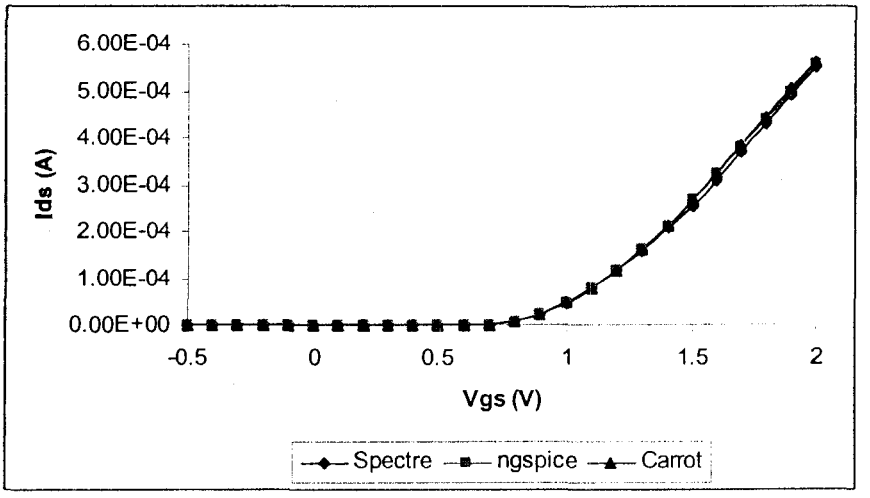

Figure 3.7 Vgs vs Ids at Vmax=0 and (W/L=30u/3u)

To test the p-channel MOSFET, the similar approaches taken in n-channel MOSFET simulations were used. The source-to-drain voltage was set to 0.8 volt in that this ensures that transistor will operate in all regions while biasing voltage at the gate terminal was

swept from -0.5 to 2 volts. Test results are shown in Fig. 3.8 and Fig. 3.9 with different velocity saturation setting.

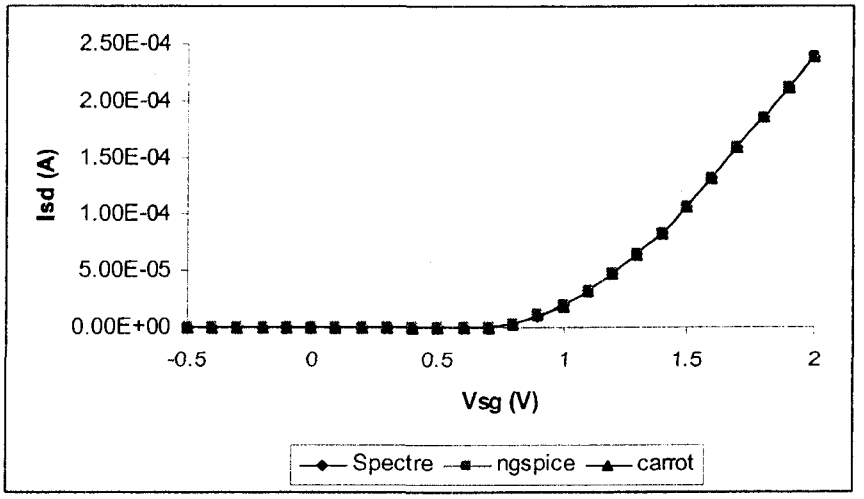

Figure 3.8 Vsg vs Isd at Vmax=1e5 and (W/L=30u/3u)

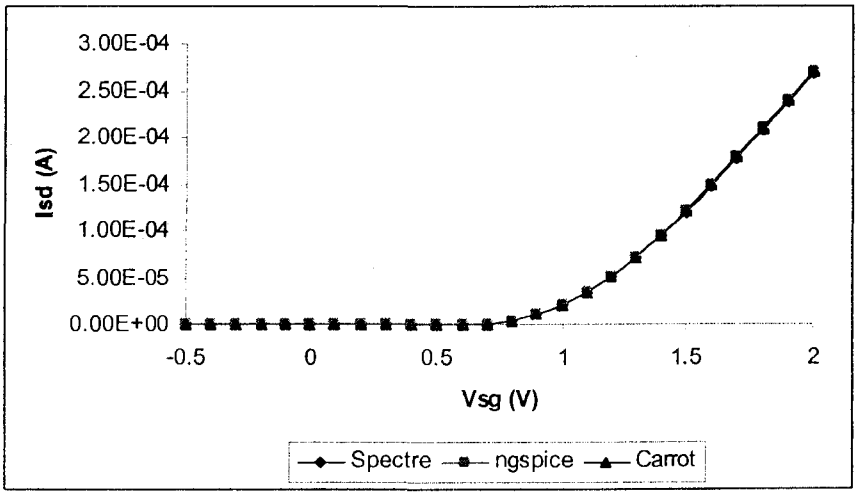

Figure 3.9 Vsg vs Isd at Vmax=0 and (W/L=30u/3u)

Above simulation results indicate that the dc equations being used in three different program simulators are the same for both transistors under this biasing condition. Once the dc model is being verified, we will verify the accuracy of the capacitance model next. Unlike the DC model, it is not straight forward to gather the data of capacitance model in MOSFETs because some capacitors depend on more than one controlling voltage. We will look at bulk-to-source and bulk-to-drain capacitors so called the depletion capacitors first. Since capacitors in this model are functions of one voltage, the capacitance value is defined as the derivative of the charge on the capacitor terminals with respect to the voltage difference between the two terminals. For example, to find out the bulk-to-drain capacitor value, we can run the DC analysis and look at derivative of Q_{bs} with respect to V_{bs}. We applied a bias voltage at the gate terminal and swept this voltage from -0.5 to 2 volts while drain voltage is kept at 0.8 volt. Similar procedures were used to test those two capacitance model in the PMOS transistors. We also found that simulation results are the same provided by three different program simulators. Results are given in Table 3.9

Table 3.9 Bulk-to-drain capacitors of p-channel and n-channel MOSFETs

Type	$C_{bd}\,(Farad)$
NMOS	$3.85*10^{-14}$
PMOS	$1.89*10^{-14}$

The distributed gate-channel capacitances are gate-to-source, gate-to-drain and gate-to-bulk capacitances which are function of three voltages and those three voltages are voltage at gate-to-source, drain-to-source, and bulk-to-source terminals. By definition, three gate capacitances can be expressed as

$$C_{gs} = \frac{\partial Q_s}{\partial V_{sg}} \qquad (3.55)$$

$$C_{gd} = \frac{\partial Q_d}{\partial V_{dg}} \tag{3.56}$$

$$C_{gb} = \frac{\partial Q_b}{\partial V_{bg}} \tag{3.57}$$

It is not possible to compare C_{gd} and C_{gb} in the Spice model with the derivation of charges in the Yang-Chatterjee model because the charge distribution is not the same. Meyer's capacitance model was implemented in ngSpice program simulator while the Yang-Chatterjee charge model was chosen in Carrot program simulator. Fig. 3.10 shows a comparison of gate-to-source capacitance of an n-channel MOSFET among three simulators. Results of those three graphs are similar. For example, the capacitances in the accumulation and saturation regions are the same. The minor difference is caused by the equation itself. P-channel capacitance model has similar capacitance behaviour as n-channel does and this can be seen in Fig. 3.11.

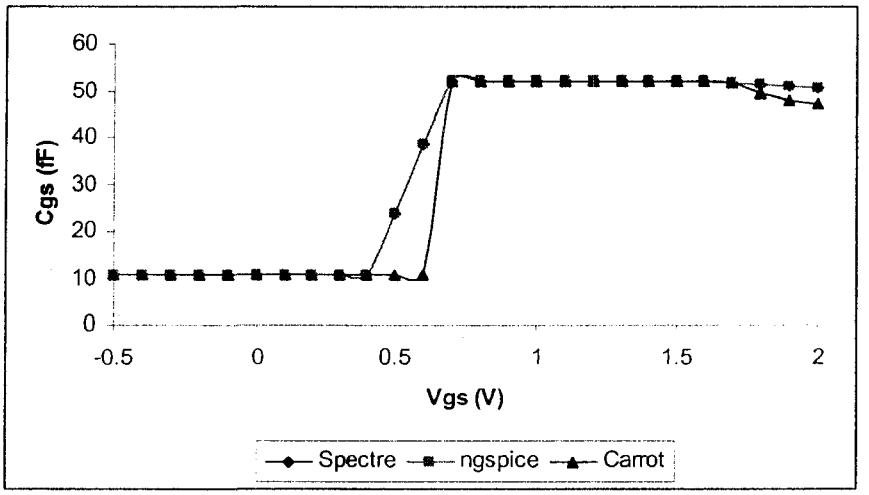

Figure 3.10 Cgs vs Vgs for NMOSFET at Vmax=1e5 and (W/L=30u/3u)

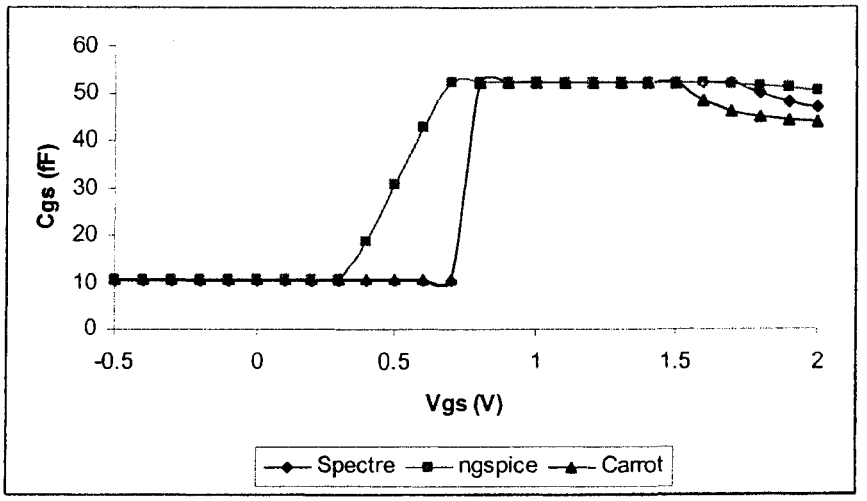

Figure 3.11 Cgs vs Vgs for PMOSFET at Vmax=1e5 and (W/L=30u/3u)

To further verify the accuracy of this implemented model, a three stage inverter was tested with a step input injected at the input of the first stage inverter and the output characteristic at each stage were plotted among Spectre, ngspice and Carrot. Results are given in Fig. 3.12, Fig. 3.13 and Fig. 3.14 respectively. As we can see that the waveform generated from the first stage of the inverter output seems to match pretty well among three simulations because same input sources are applied. As the output voltage at the first stage enters the second stage, more capacitors are involved in the transient analysis so minor discrepancy propagates through each stage. We can conclude that the capacitance model implemented in Carrot simulator is relatively close to the one in the ngspice simulator. Unlike results from Spectre, rising and falling time tended to be longer. Since we do not have access to the source code of Spectre, it is difficult to understand why the model disagree.

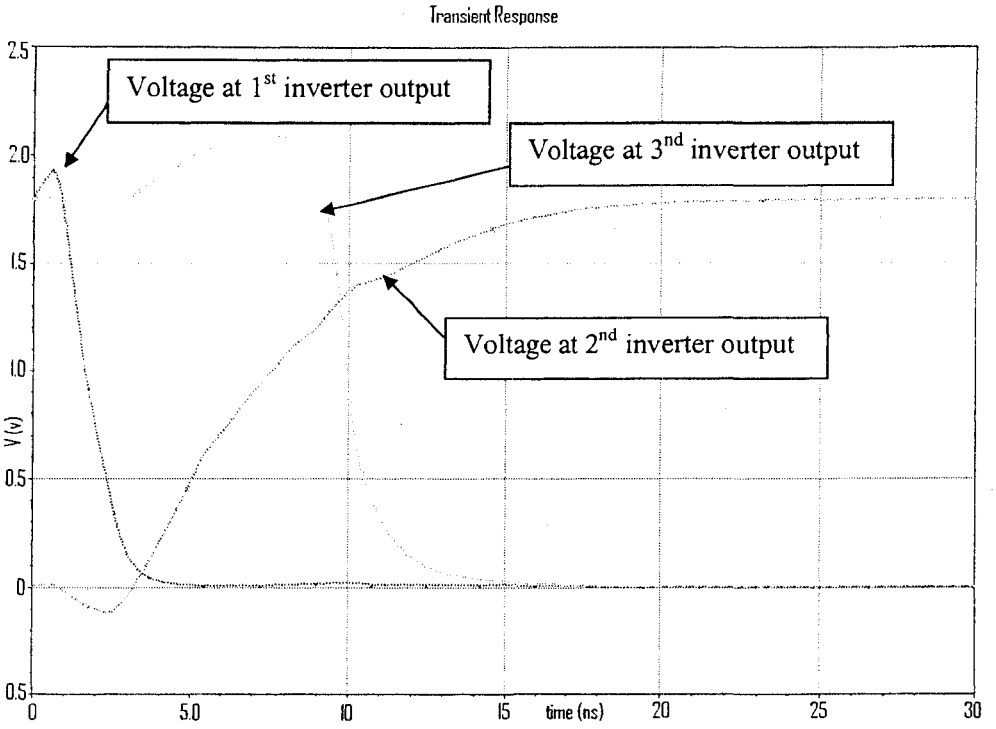

Figure 3.12 Three stage inverter transient simulation using Spectre

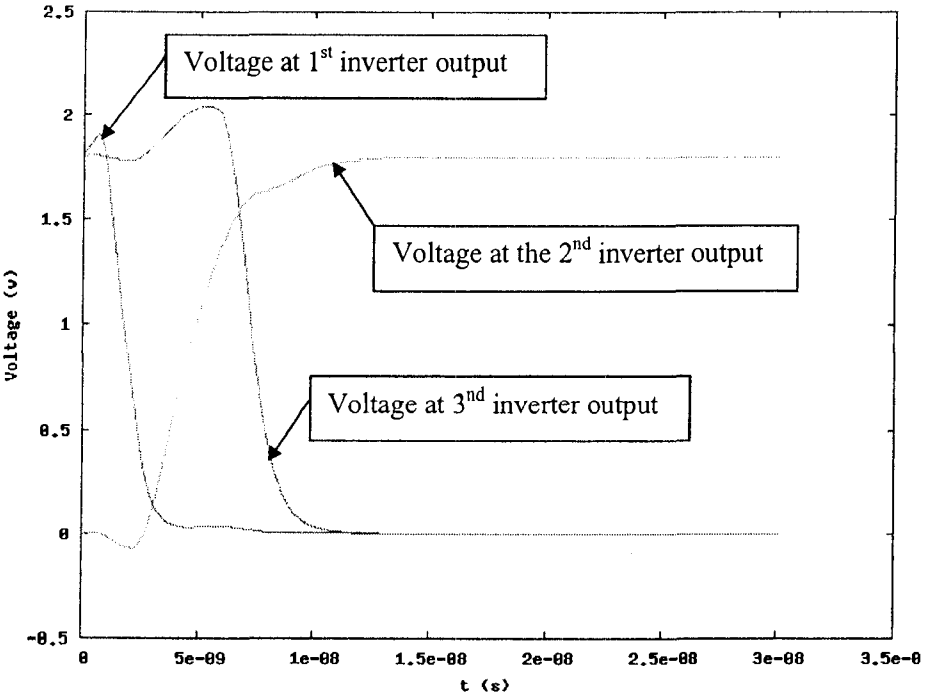

Figure 3.13 Three stage inverter transient simulation using Carrot

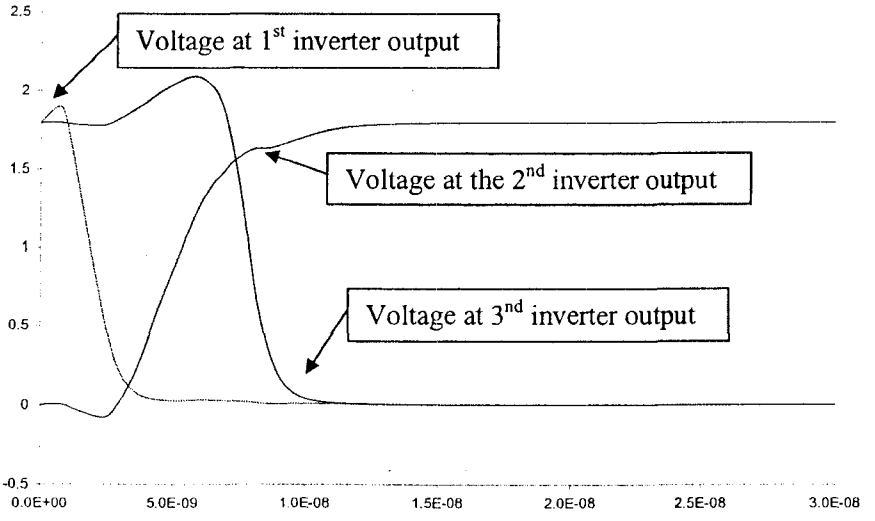

Figure 3.14 Three stage inverter transient simulation using ngspice

Chapter 4

Design of a Ring VCO

4.1 Introduction

A voltage-controlled oscillator (VCO) is a circuit whose output signal oscillates at a particular frequency which is based on the input control voltage. This can be described in a simple mathematical form as

$$f_{out} = f_0 + K_{vco} \cdot V_{cont} \tag{4.1}$$

f_0 is the center frequency or the free running frequency; K_{vco} is the gain of the VCO which controls how much is a change in frequency with respect to a change in voltage, V_{cont} is the control voltage that sets the output frequency to a desired value, and f_{out} is the oscillation frequency.

A VCO is a commonly used circuit due to its wide range of applications including phase-locked loops (PLLs), clock and data recovery (CDR) circuits, transmitters, and receivers. The ring and LC VCOs are two of the most popular oscillators selected to perform the above tasks. Each VCO depends on different methods to achieve oscillation, so its performance parameters are different. For examples, LC VCOs have advantages in phase noise and maximum frequency categories whereas ring VCOs are superior in tuning range and manufacturability. When choosing VCOs for certain applications, many factors in terms of power, speed, signal amplitude, and phase noise are considered.

This chapter starts with discussions related to general theory behind LC VCO. Next, general ring VCO design aspects are explained in details. A block diagram will give an idea what has been implemented in this design. Then, each individual circuit is designed along with detail discussions based on analytical analyses and simulation results. A circuit simulator (Spectre) is used to perform simulations throughout this work. The chip was fabricated by TSMC (Taiwan Semiconductor Manufacturing Corporation) through CMC. Layout considerations are discussed next followed by simulation results.

4.2 Voltage-Controlled Oscillator (VCO) Principles and Design Aspects

A voltage-controlled oscillator is commonly used in telecommunication devices such as Phase-locked loops (PLLs). Two commonly used VCO architectures are ring oscillators and LC oscillators and they function as controllers where their input and output variables are voltage and frequency, respectively.

When it comes to design a VCO, many trade off are made in terms of power consumption, speed, phase noise, jitter, process variations, etc. Layout is another important aspect should be planed in advance because it has a direct impact on the overall circuit performance. Mismatch and parasitic components are unavoidable in circuits so they should be minimized.

An ideal LC oscillator is mainly based on a LC tank which is composed of an inductor and a capacitor. For an ideal LC tank shown in Fig. 4.1, it achieves oscillation when the impedance of the inductor is equal and opposite to that of the capacitor. The oscillation frequency is given in Eq. (4.2).

$$\omega = \frac{1}{\sqrt{LC}} \tag{4.2}$$

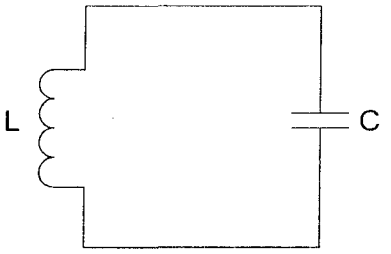

Figure 4.1 Ideal LC tank

In practice, inductors and capacitors suffer from resistive components. Fig. 4.2 shows a practical LC tank with resistive component R and a negative resistance -R. The loss in the tank is represented by a positive resistance and will attenuate the oscillation signal. Therefore it is important that a circuit would introduce a negative resistance to sustain oscillation signals.

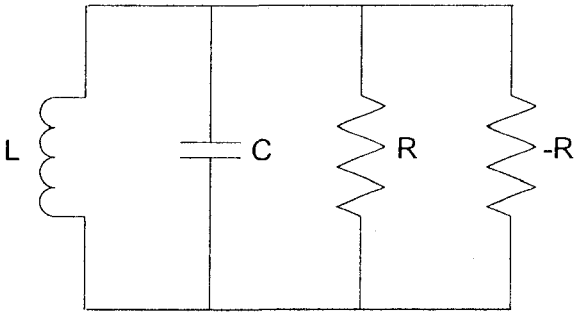

Figure 4.2 Practical LC tank with negative resistance

4.2.1 Ring VCO

Ring oscillators are waveform-based oscillators which consist of a number of delay stages where the output of the last delay stage is fed back to the input of the first stage. To achieve oscillation, the ring oscillator must provide a 2π phase shift and have a unity voltage gain at the oscillation frequency. Each delay stage provides a (π/N)

phase shift where N is the number of delay elements and the remaining π phase shift is provided by the DC inversion [16].

The topology of ring oscillators falls into two categories: the single-ended ring oscillator and differential ring oscillator. A simple single-ended ring oscillator is comprised of an odd number of inverters where the output of the last inverter is fed back to the input of the first stage. Therefore, the circuit provides the DC inversion which causes the oscillation in the circuit. This circuit is shown in Fig. 4.3.

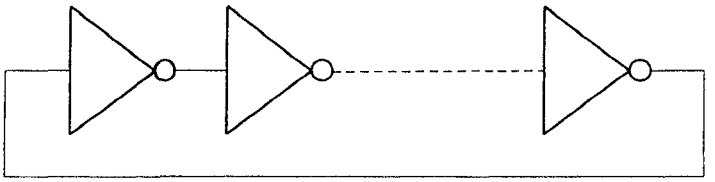

Figure 4.3 Single-ended ring oscillator block diagram

To calculate the frequency at which this circuit will oscillate, the total number of N inverters and the propagation delay t_p through each inverter should be determined. This expression is given in Eq. (4.3).

$$f = \frac{1}{2Nt_p} \tag{4.3}$$

The single-ended ring oscillator is modified so that its frequency is controllable. The method is to control the amount of current which is available to charge or discharge the capacitive load of each stage. Fig. 4.4 shows current starved inverter. If the control voltage Vcont increases, the reference current Iref will increase. The increasing current through M6 reduces the time to discharge the capacitive load at the next stage. Since the current through M1 mirrors the current through M3, the time to charge the capacitive load at the next stage also decreases as well. Therefore, an increase in control voltage results in a decrease in the propagation through each delay cell so the oscillation frequency increases.

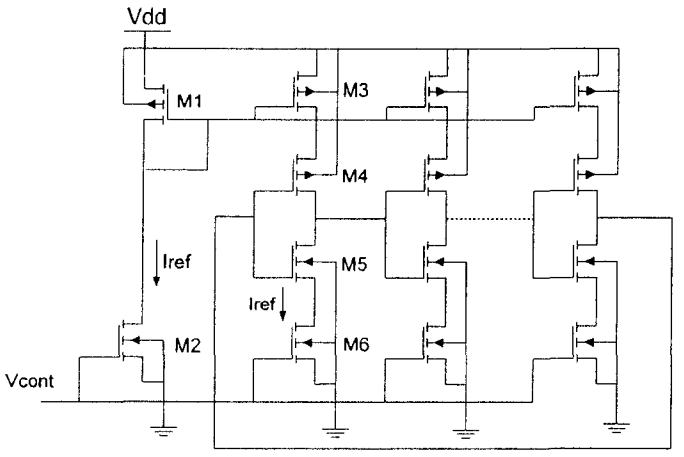

Figure 4.4 Single-ended ring VCO schematic

Since the single-ended ring VCO is susceptible to common-mode noise, many ring VCOs use the differential delay cell topology to alleviate this problem. The differential ring VCO is illustrated in Fig. 4.5.

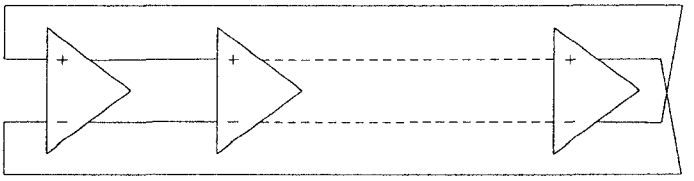

Figure 4.5 Differential ring oscillator block diagram

A common topology for a cell of a differential ring VCO is comprised of a resistive load, a source-coupled pair, and a current source. This circuit is shown in Fig. 4.6 [17].

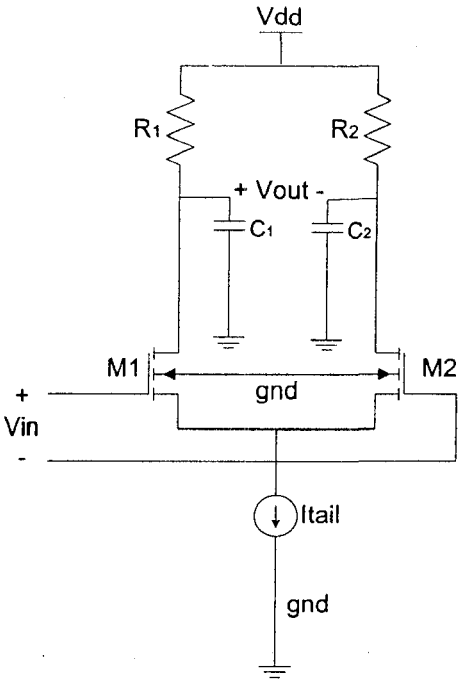

Figure 4.6 Simplified differential delay cell circuit schematic

To determine the oscillation frequency in this circuit, the propagation time in each delay cell is derived here. The propagation time is defined as the time between the zero cross of the differential output voltage. The output voltage at zero cross is equal to $V_{dd} - \left(V_{swing}/2\right)$ and V_{swing} is the voltage drop across the resistive load. Assume the input voltage is positive so that the tail current switches from M2 to M1. This results in a voltage drop across R1 and no voltage drop across R2. To analyze this circuit during switching, the left-hand side of the source-coupled pair differential delay cell is shown in Fig. 4.7. M1 is replaced by a current source.

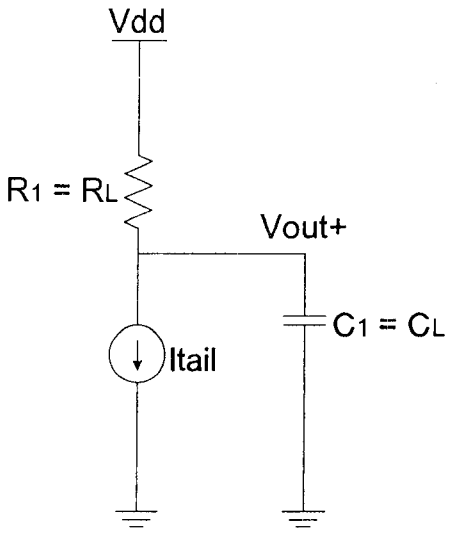

Figure 4.7 Left-hand side of the source-coupled pair differential delay cell

The output voltage of a first order RC circuit is

$$V_{out}^{+}(t) = V_{out}^{+}(final) + \left[V_{out}^{+}(initial) - V_{out}^{+}(final)\right] \cdot e^{\frac{-t}{R_L C_L}} \tag{4.4}$$

with $V_{out}^{+}(initial) = V_{dd}$, $V_{out}^{+}(final) = V_{dd} - V_{swing}$ and $V_{swing} = I_{tail} \cdot R_L$ Thus the propagation through each delay is

$$t = t_p = R_L C_L \ln(2)$$

Then, the frequency at which the circuit will oscillate is

$$f = \frac{1}{2NR_L C_L \ln(2)} \tag{4.5}$$

and the resistive load value is equal to

$$R_L = \frac{V_{sw}}{I_{tail}} \tag{4.6}$$

To make the differential ring oscillator voltage controllable, a circuit to control R_L is needed. A replica biasing circuit keeps V_{sw} constant as the tail current increases and this makes R_L to be inversely proportional to I_{tail}. With the replica biasing circuit shown in Fig. 4.8, the voltage swing is relatively constant and the oscillation frequency increases as the control voltage increases. The PMOS transistors M3, M4, and M5 are in the deep triode region of operation so that they act as linear resistors. The replica circuit works as follows. If the control voltage increases, the control current will increase as well as the tail current. The voltage drop across the PMOS transistors will also increase. Due to the negative feedback loop, the potential at the drain of M5 remains constant equal to Vref. The equivalent resistance of the PMOS load reduces accordingly. The PMOS bias voltage will set the voltage swing to the desired level. Therefore, as the tail current increases with a constant voltage swing, the oscillation frequency increases.

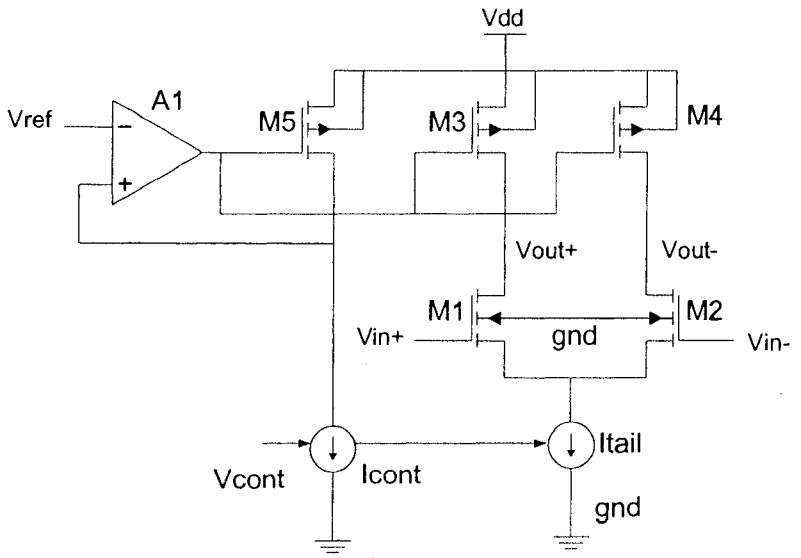

Figure 4.8 VCO with replica biasing circuit schematic

4.3 Ring VCO Schematic Design

Many factors in terms of center frequency, tuning range, tuning linearity, manufacturability, output amplitude, power dissipation, phase noise, and jitter are involved in the VCO design because they play a huge role in oscillator performance. If the output amplitude is small and the noise signal is large, oscillations are hard to distinguish.

A differential ring voltage-controlled oscillator is designed to provide a 1.8 GHz center frequency through the coarse tuning circuit. Then a replica biasing circuit and fine tuning circuit are designed so the frequency is a function of control voltage. The rail to rail output signal is achieved on output buffer. Fig. 4.9 is a block diagram of the ring VCO. Each block is discussed in the following section.

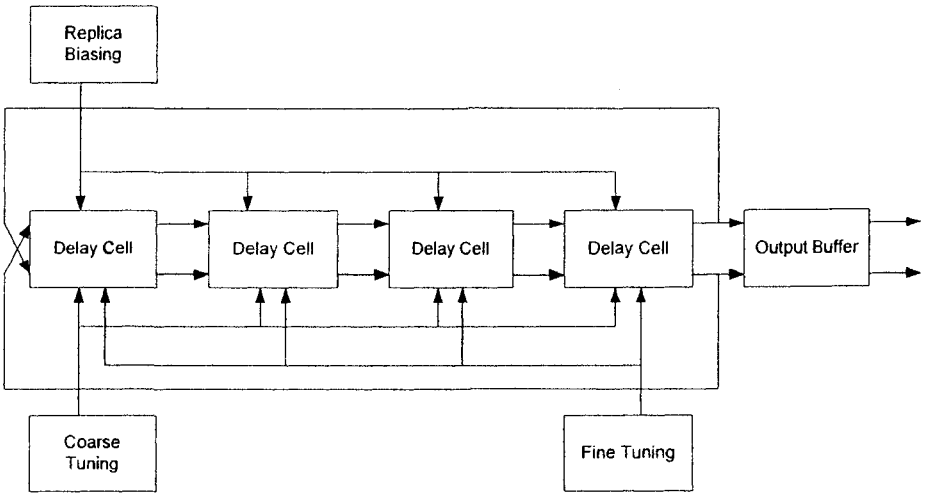

Figure 4.9 Differential ring VCO block diagram

4.3.1 Differential Delay Circuit Design

A basic differential delay cell shown in Fig. 4.10 features a source coupled differential pair with two resistive loads. The loads are implemented by PMOS transistors operating in the deep triode region. When the PMOS transistor is in the deep triode region of operation, they operate as linear resistors. The loads are biased by a replica biasing circuit which is used to generate the appropriate voltage value Vbias to ensure a constant voltage swing at the output. A source coupled differential pair is driven by two current sources controlled by the coarse tuning and fine tuning circuit. The coarse tuning circuit determines the center frequency of the ring VCO by steering a fixed amount of current into the delay cells whereas the fine tuning circuit determines the tuning range of the VCO by steering a smaller current into the delay cells.

Based on the above discussion, the circuit will analyzed with the following sequences.

- Choose center frequency
- Choose output swing
- Set tail current in delay cell
- Determine sizes of PMOS loads $(W/L)_1$
- Determine sizes of NMOS differential pairs $(W/L)_3$
- Determine sizes of current sources $(W/L)_5$, $(W/L)_6$

This design is based on a $0.18\,\mu m$ CMOS process. The supply voltage is 1.8V and the center frequency is around 1.8 GHz. The 0.4V output swing is chosen in this design and will be amplified by the output buffer. The tail current in each delay cell is set to $200\,\mu A$ which corresponds to a total of $800\,\mu A$ for a four stage ring oscillator. If a very small current is chosen, the circuit will become sensitive to changes due to process errors and susceptible to noise.

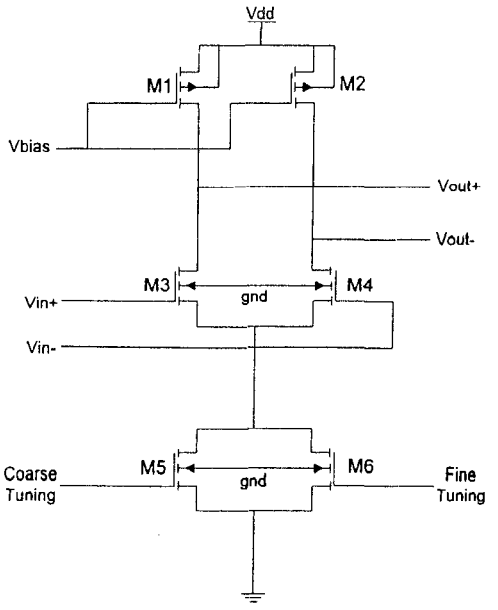

Figure 4.10 Basic differential delay cell schematic

The next step is to determine the PMOS load device sizes which can be determined either from the current equation for a device in the deep triode region or from the I-V characteristic curve through simulations or measurements. The current equation is used to estimate resistive load values in this research. The resistance of a PMOS transistor operating in the deep triode region is given by Eq. (4.7) where μ_p, C_{ox}, and V_{thp} are the hole mobility, gate-oxide capacitance per unit area and the threshold voltage respectively. Eq. (4.7) gives a rough idea of the width to length ratio of the p-channel transistor.

.

$$R_L = \frac{1}{\mu_p C_{ox} \frac{W}{L}\left(|V_{gs}| - |V_{thp}| - |V_{ds}|\right)} \tag{4.7}$$

The load capacitance values are determined next. The first stage of the inverter output is connected to the second stage of the inverter input, so the load capacitance value is mainly dominated by the gate-source capacitance at the input of the second delay stage. Other capacitors such as parasitic capacitors are not considered in this calculation. As discussed in Section 4.2.1, the oscillation frequency can be determined by

$$f = \frac{1}{2NR_L C_L \ln(2)}$$

so the equation of the load capacitance can be formulated by rearranging the above expression which yields the following equation

$$C_L = \frac{1}{2NR_L \ln(2) \cdot f} \tag{4.8}$$

The load capacitance of MOS transistors in the saturation region given in [17] is

$$C_L = \frac{2}{3} WLC_{ox} \tag{4.9}$$

The device size M3 is obtained by Eq. (4.8) and Eq. (4.9). Lastly, tail currents flowing into M5 and M6 are evaluated here. Even though both M5 and M6 are acting as current sources, their influence to the circuit in terms of oscillation frequency is different. The drain current in M5 sets the center frequency in the VCO while the tuning range is set by the drain current in M6. Based on this idea, the drain current in M5 has a major effect on the oscillator and should be much greater compared to that of M6. Since both transistors operate in saturation region, the biasing voltages $\left(V_{gs}\right)$ at both inputs should be greater than their overdrive voltages

$$V_{ov} = V_{gs} - V_{th}$$

Their device sizes can be analytically calculated from Eq. (4.10) with the above observation.

$$V_{bias} = \sqrt{\frac{2I_d}{\mu_n C_{ox}\left(\frac{W}{L}\right)}} + V_{thn} \tag{4.10}$$

The initial design is then fine-tuned using simulations. Then final device sizes in delay cell are summarized in Table 4.1.

Table 4.1 Transistor W to L ratio in delay cell

M1, M2	M3, M4	M5	M6
(1.5u/0.18u)	(17.5u/0.18u)	(4u/0.18u)	(1u/0.18u)

Fig. 4.11 shows the pre-layout simulation at output of the ring VCO oscillating at 1.8 GHz. The common-mode voltage is 1.58V with a voltage swing of 0.38V.

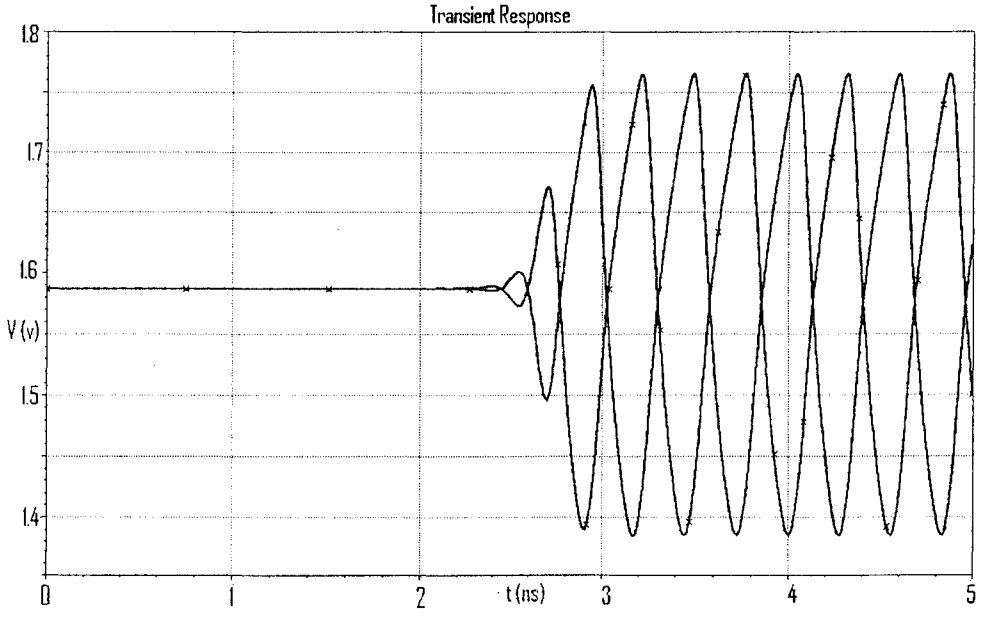

Figure 4.11 Pre-layout simulation of delay cells

The reason of having different results between the simplified analytical analysis and simulation is that the analytical equations are derived from Level 1 MOSFET equations and the implemented models are BSIM3v3 model. Another reason is that derivations of the frequency equation do not include parasitic components such as overlap, junction, and sidewall capacitances. For example, the drain-to-bulk capacitances of M1 and M3 transistors and gate-to-drain and gate- to-drain overlap capacitances of M3 should be taken into account. Other important factors that affect MOS transistor behaviour operating at high frequency are the substrate network and the gate resistance [27] as shown in Fig. 4.12. The gate resistance consists of the physical gate resistance and another part is due to nonquasi-static (NQS) effects. The physical gate resistance depends on the length of poly layer in the transistor and the NQS component is related to a time that charge underneath the gate will need to respond to the applied voltage. This distributed channel resistance is related to the finite response time and it also increases the gate resistance. Thus, both parasitic capacitances and resistances should be taken into account when dealing with circuit of having high frequency signal.

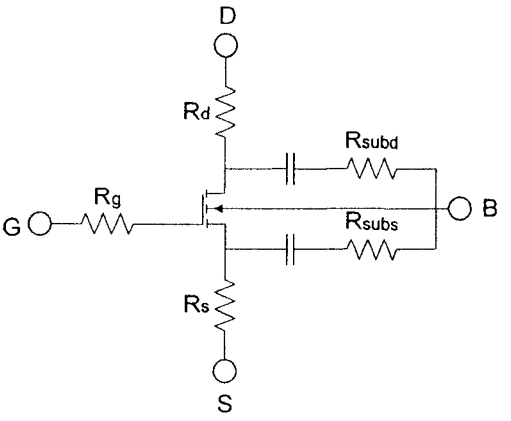

Figure 4.12 A MOSFET RF model based on BSIM3v3

4.3.2 Coarse Tuning Circuit Design

The coarse tuning circuit is designed to achieve the desired bias value at the node "Coarse Tuning". As illustrated in **Fig. 4.13,** this circuit contains a resistor R in series with a diode-connected NMOS transistor M7.

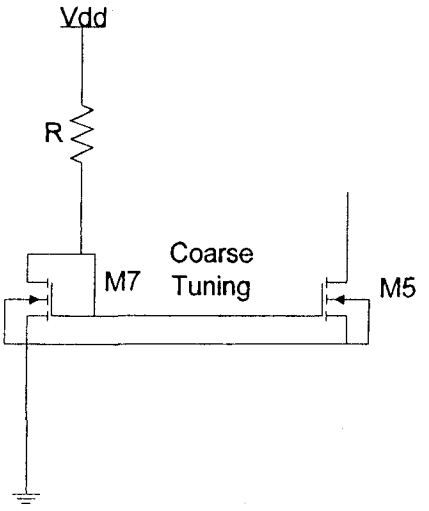

Figure 4.13 Coarse tuning cell schematic

The current that flows in the drain of M7 is mirrored to the drain of M5 in **Fig 4.10**. The resistor value is equal to a voltage difference between the supply voltage and the node Coarse Tuning over the current in M7. The bias voltage is equal to 0.68V and this value is determined from Eq. (4.10). Table 4.2 shows parameters used in this circuit.

Table 4.2 Transistor W to L ratio and resistor value in coarse tuning circuit

R	M7
$3.4k\Omega$	(7u/0.18u)

4.3.3 Fine Tuning Circuit Design

The fine tuning circuit defines the VCO gain and its schematic diagram is shown in **Fig 4.14**. The transistor M8 is a current source and its gate is connected to ground to keep it operating in the saturation region. A differential input voltage plus common mode voltage set both transistors M9 and M10 into saturation region so the desired current can flow through M9. Then current will mirror into the delay cell through M11. This additional current steered into the delay cell determines the tuning range of VCO because the oscillation frequency is proportional to this tail current. The VCO gain is expressed in Eq. (4.11).

$$Kvco = \frac{\partial f}{\partial V_{control}} = \frac{\partial f}{\partial I_{M6}} \frac{\partial I_{M11}}{\partial V_{control}} X = \frac{\partial f}{\partial I_{M6}} \frac{gm_{M9}}{2} X \tag{4.11}$$

where I_{M6} is the amount of additional current being supplied to delay cells. The gm_{M9} is the transconductance of M9 and X is a ratio of device size M6 to M11.

$$gm = \frac{\partial I_{ds}}{\partial V_{gs}} = \sqrt{2 \cdot \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot I_D} = \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot \left(V_{gs} - V_{th}\right)$$

The oscillation frequency can be rewritten as

$$f = \frac{I_{M5} + I_{M6}}{2 \cdot N \cdot C_L \cdot \ln(2) \cdot V_{sw}}$$

Then the VCO gain is

$$K_{VCO} = \frac{\mu_p \cdot \left(\frac{W}{L}\right)_{M9} \cdot (V_{ov})_{M9}}{3.6968 \cdot W_{M3} \cdot L_{M3} \cdot V_{sw}} = 0.355\text{GHz/V}$$

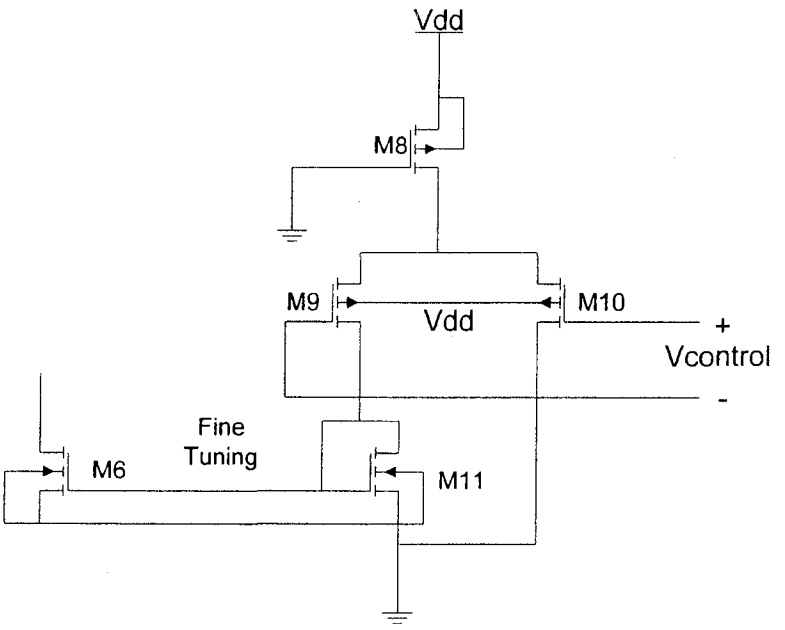

Figure 4.14 Fine tuning cell schematic

The device sizes given in Table 4.3 are determined from simulations such that the tuning circuit provides a 0.1 GHz tuning range by a ± 200 mV tuning voltage with a common-mode voltage at 0.95V.

Table 4.3 Transistor W to L ratio in fine tuning circuit

M8, M9, M10	M11
(0.5u/0.18u)	(0.5u/0.18u)

4.3.4 Replica Biasing Circuit Design

A replica biasing circuit uses a copy of the half delay cell and an operational amplifier to hold the signal amplitude constant. The circuit is shown in **Fig 4.15**.

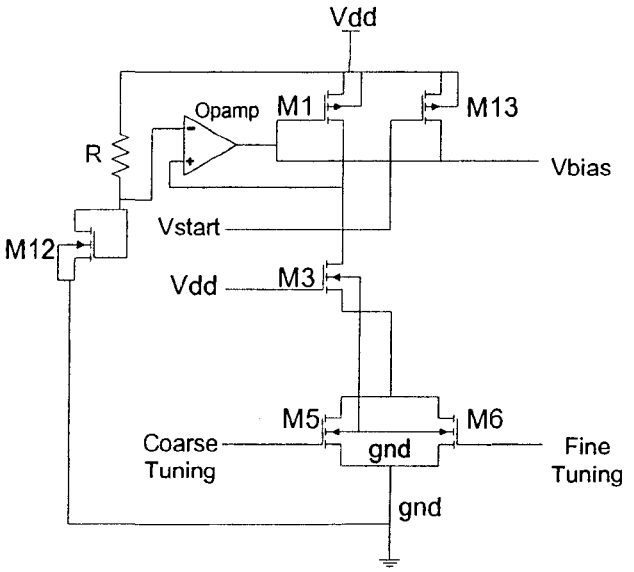

Figure 4.15 Replica biasing cell schematic

The amplifier is designed to have a high gain such that it applies a negative feedback at the node "Vbias". Since the amplifier gain is large, the differential input voltage of the operational amplifier must be small. Therefore, the signal amplitude is approximately equal to Vdd-Vref. Vref is the voltage at the inverting input of the amplifier. Then, a circuit with a resistor R in series with a diode-connected n-channel transistor M12 is designed to generate a reference voltage equal to 1.4V.

The replica biasing circuit also includes a transistor M13 to use as a switch which sets an on-off state of the oscillator. The reason to have this switch is because an LC oscillator will be fabricated into the same chip. This switch is used to enable one oscillator at a time and thus avoid interference between two. If M13 is in the cut-off region, the oscillator is on. To turn off the oscillator, M13 must be turned on to cause M1 into the cut-off region. Therefore, by setting Vstart to 1 or 0 will set the oscillator to the off and on stage accordingly. The device sizes and resistor value is given in Table 4.4.

Table 4.4 Transistor W to L dimensions and resistor values

R	M12	M13
$3.5k\Omega$	(0.5u/0.18u)	(1.5u/0.18u)

A two stage CMOS operational amplifier [18], illustrated in **Fig. 4.16**, is designed to provide negative feedback in the replica biasing circuit. The first stage consists of a current mirror load M14-M15 and a differential pair M16-M17 biased by a tail current source M18. The second stage consists of a common-source amplifier M21 and M22 as an active load. In the biasing circuit, the current source is generated by a resistor with 2 diode-connected n-channel transistors M19 and M20 to provide proper biasing current for the amplifier.

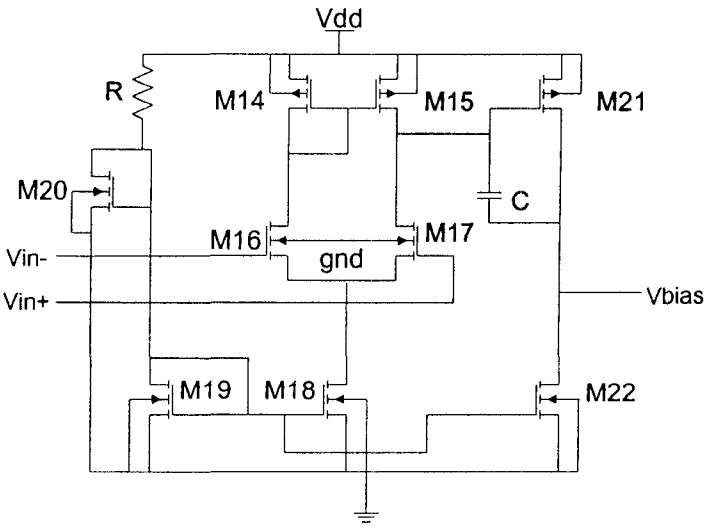

Figure 4.16 Operational amplifier cell schematic

The overall voltage gain in the amplifier depends on both first and second stages. The first-stage voltage gain is a multiplication of the transconductance and the output resistance of the first stage and the second-stage voltage gain is can be calculated in the same fashion. This results an overall gain of

$$A_v = A_{v1} \cdot A_{v2} = gm_{16}\left(r_{o15} // r_{o17}\right) \cdot gm_{21}\left(r_{o21} // r_{o22}\right) \tag{4.12}$$

To ensure the gain in the amplifier is relatively constant, the output voltage swing

$$V_{ov22} \le V_{bias} \pm V_{swing} \le V_{dd} - |V_{ov21}| \tag{4.13}$$

is limited to a voltage range given in Eq. (4.13) for which both M21 and M22 operate in the saturation region. If output voltage is outside this range, one of the output transistors will enter the triode region. As a result, the overall gain of the amplifier will be degraded

The following discussion gives an idea how the dimensions should be sized in a certain ratio. With zero input voltage and perfect matching, overdrive voltages in transistors M14, M15, and M21 are equal. Eq. (4.14) gives a ratio of drain currents versus transistor size.

$$\frac{I_{d14}}{\left(\frac{W}{L}\right)_{14}} = \frac{I_{d15}}{\left(\frac{W}{L}\right)_{15}} = \frac{I_{d21}}{\left(\frac{W}{L}\right)_{21}} \tag{4.14}$$

Drain currents in M14 and M15 are equal to one half of drain currents in M18. Also M21 and M22 have equal drain currents and M18 and M22 have equal gate-source voltages. Based on those conditions, Eq. (4.14) can be rewritten as

$$\frac{(W/L)_{14}}{(W/L)_{21}} = \frac{(W/L)_{15}}{(W/L)_{21}} = \frac{(W/L)_{18}}{2(W/L)_{22}} \tag{4.15}$$

Lastly, the compensation capacitor is used to prevent the circuit from oscillating when connected in a feedback loop. Without a compensation capacitor in the circuit, the oscillation will occur if the phase margin is negative. The phase margin is 180 degrees minus the phase at unity loop gain. To meet this requirement, we selected the compensation capacitor based on the open loop response of the operational amplifier. This simulation result is plotted in **Fig 4.17**. By running numerous simulations, we chose the capacitor value to be 950fF. This not only ensures a positive phase margin, but also gives the necessary value to pass layout versus schematic (LVS) rule check in the software. The components values used in the amplifier design are summarized in Table 4.5.

Table 4.5 Transistor W to L ratio, resistor and capacitor values

M14 M15	M16 M17	M18 M19	M20
(8u/1u)	(8u/1.5u)	(4u/1u)	(40u/0.18u)
M21	M22	R	C
(16u/1u)	(4u/1u)	$3.5k\Omega$	950fF

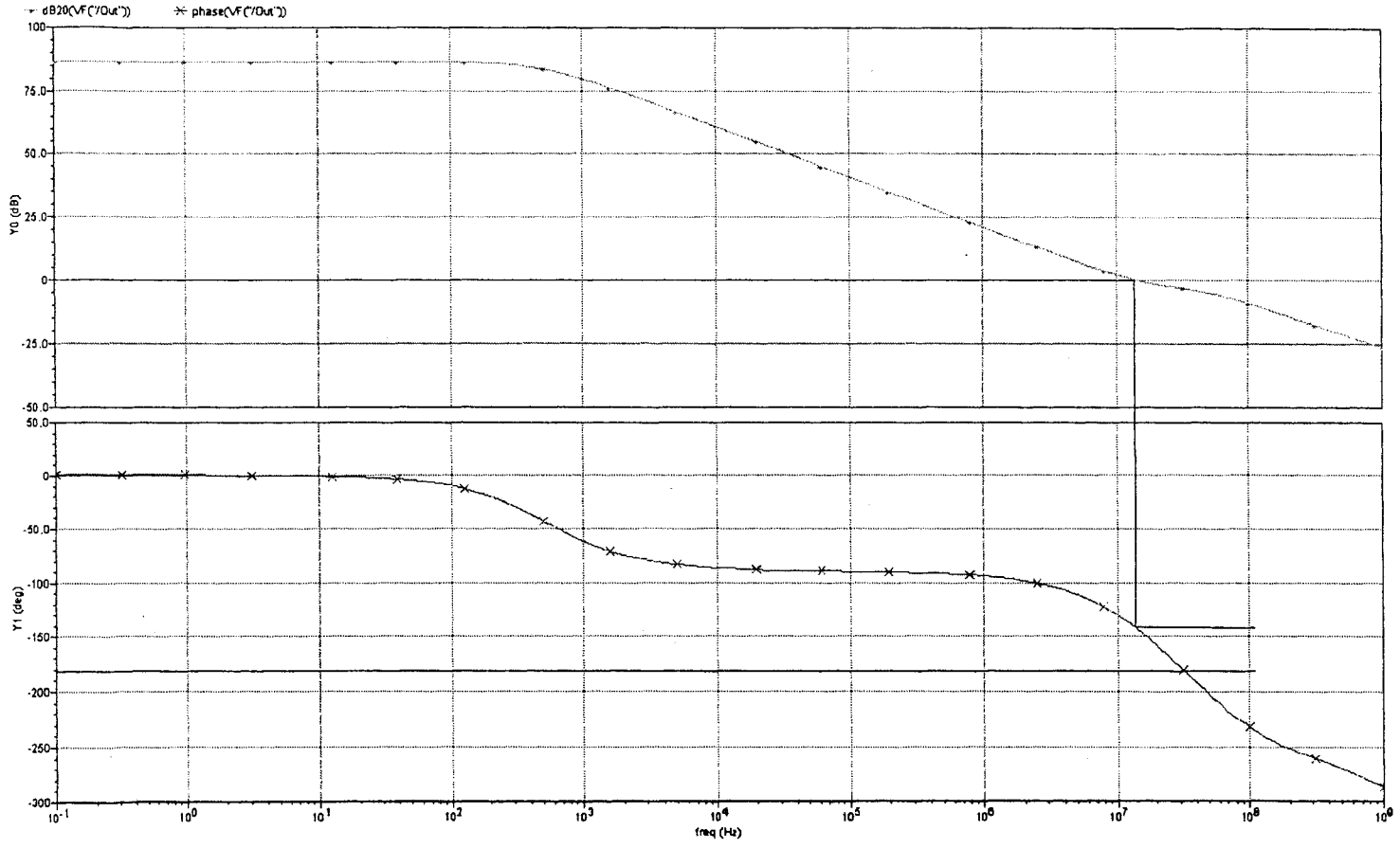

Figure 4.17 The open-loop frequency response of the op-amp

4.3.5 Output Buffer Circuit Design

The output buffers are utilized to optimally drive bigger loads such as pads, test fixtures, and the spectrum analyzer input impedance without degrading the oscillator performance. The CMOS inverter can provide a full output voltage swing between zero and supply voltage if the inverter threshold voltage was set to a desired voltage value. The input voltage versus output voltage characteristics of a CMOS inverter is given Fig. 4.18 and the inverter gain is referred to the slope in the figure. This indicates that region C provides a maximum gain to the circuit. To obtain the maximum inverter gain, both transistors are designed to operate at the saturation region. If transistors operate outside region C, the output voltage signal will be degraded.

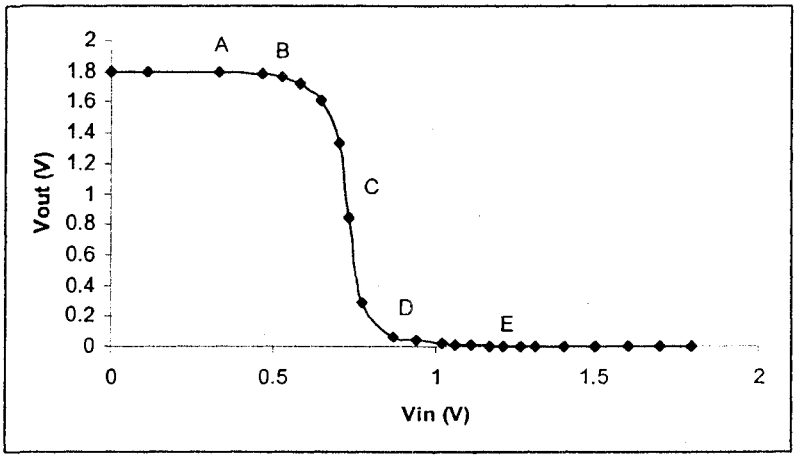

Figure 4.18 Operating regions of the nMOS and the pMOS transistors

In addition to above discussions, lowering the common mode voltage at the oscillator outputs is necessary before designing an inverter chain. If the outputs of delay cells are connected to an inverter chain without the first stage buffer, it takes more inverters or it may be impossible to achieve maximum swing because the common mode voltage is not near the C region. Thus, the common mode voltage is lowered to near 1V by means of a differential buffer design given in Fig. 4.19.

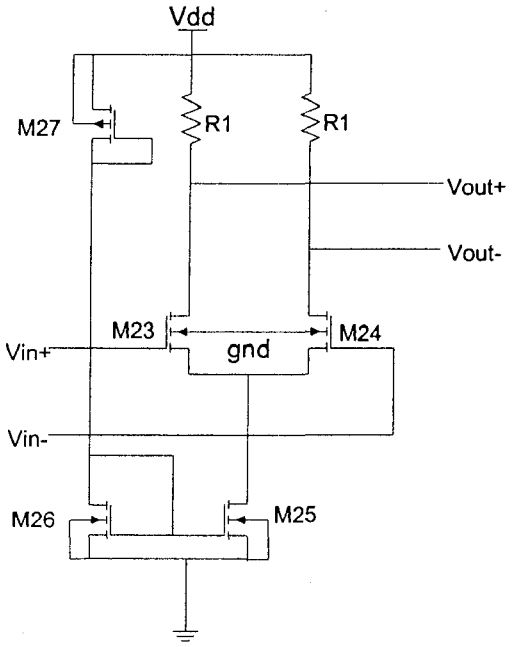

Figure 4.19 The 1st stage differential output buffer cell schematic

The current source M25 is biased by two diode-connected MOS transistors in series. The resistor value R1 is calculated using ohm's law with an assumption that currents in the drain of M23 and M24 are both $100\,\mu A$. Table 4.6 shows the parameters used in this circuit.

Table 4.6 Transistor W to L ratio and resistor values

M23 M24	M25 M26	M27	R1
(2.5/0.18)	(6/0.4)	(3/0.18)	$8\,k\Omega$

Fig. 4.20 shows the effectiveness of the differential output buffer which produces a 0.6V output signal at a common-mode voltage of 0.98V.

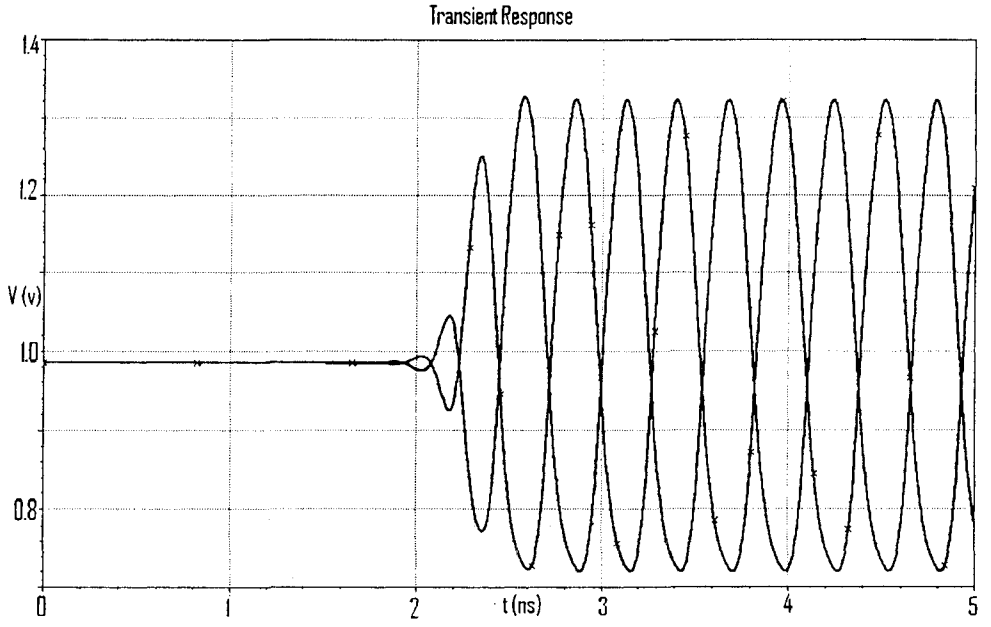

Figure 4.20 Pre-layout simulation at the 1st buffer output

Next, an inverter chain is designed through simulations. As the chain becomes longer, the input voltage increases as well as the width for both transistors. The inverter is first fine tuned to the region C referred to Fig. 4.18 and its width is double through each stage. A series of inverter chain and its output signals are given in Fig. 4.21 and Fig 4.22.

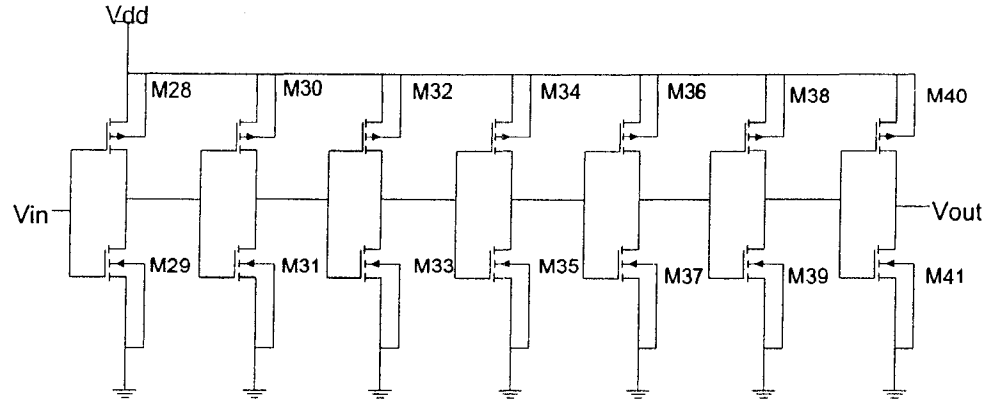

Figure 4.21 The 2nd stage output buffer cell schematic

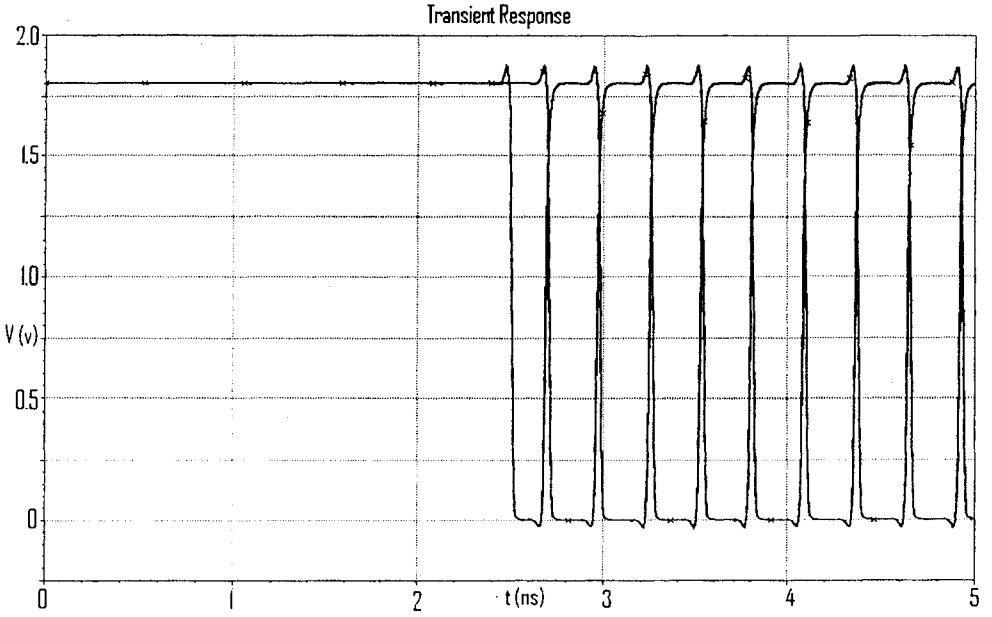

Figure 4.22 Pre-layout simulation at the 2nd buffer output

The device dimensions are given in Table 4.7 and all dimensions are in micros

Table 4.7 Transistor W to L ratio in the inverter chain

M28	M29	M30	M31	M32	M33	M34
(3.5/0.18)	(0.5/0.18)	(3/0.18)	(1/0.18)	(6/0.18)	(2.5/0.18)	(18/0.18)
M35	M36	M37	M38	M39	M40	M41
(7.5/0.18)	(54/0.18)	(22.5/0.18)	(108/0.18)	(45/0.18)	(216/0.18)	(90/0.18)

4.4 Ring VCO Layout Design

The layout has a great effect on the overall circuit performance. When designing a circuit contains large MOS transistors, the parasitic components should be minimized by using folding technique [19]. For MOS transistor with a large width, the folding technique is applied. The length of the MOS transistor is the same as the length of poly whereas the MOSFET's overall width is set by the width of poly over the active region times the number of poly fingers. Fig. 4.23 gives an equivalent layout of a large-width MOSFET where A, B, and C are referred to Source, Gate, and Drain in the n-channel MOS transistor. This will reduce the gate resistance and drain to bulk capacitances. The p-channel MOS transistor can be designed in the same manner.

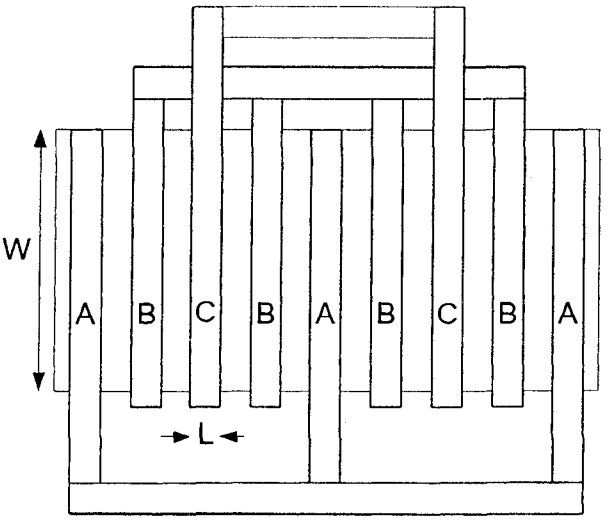

Figure 4.23 Equivalent layout of a large-width MOSFET

The common-centroid geometry is the technique to reduce mismatch caused by process variations. It is used to layout a differential pair of transistors so that any variations in process parameters will affect both transistors in the same fashion. For example, a differential pair of NMOS transistors is folded into 2 fingers and laid out using this method. Its general layout diagram is shown in Fig. 4.24. Any changes in M1 will affect M2 the same way, so those two transistors will remain match.

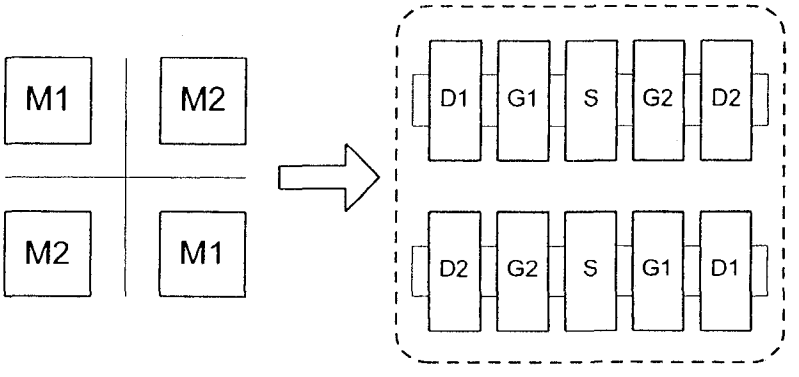

Figure 4.24 NMOS differential pair layout using common-centroid geometry

In our design, the folding technique is applied to all of the large size transistors such as differential cells and inverters and we also should have laid out differential pairs with the common-centroid geometry to ensure the reduce mismatch problem due to process variations.

The ring VCO layout design is based on a $0.18\,\mu m$ n-well CMOS technology offered by TSMC. This process includes six metal layers and one poly layer. The Metal 1 and poly layer are mainly used to design NMOS and PMOS transistors. The Metal 2, Metal 3, and Metal 4 layers are used to route signals while Metal 5 and 6 layers are used to lay out the power and ground. N-implant resistors, P-implant resistors, and a Metal-Insulator-Metal (MIM) capacitor are also built in the layout design. Lastly, the pads with the electrostatic discharge (ESD) circuit are implemented as this protects thin gate oxides from ESD damage.

A single delay cell layout is shown in Fig. 4.25 and the fine tuning layout is given in Fig. 4.26. Coarse tuning, replica biasing and output buffer layouts are given in Fig. 4.27, Fig. 4.28, and Fig. 4.29 respectively. Lastly, Fig. 4.30 and Fig. 4.31 show the overall ring VCO layout and the test chip layout.

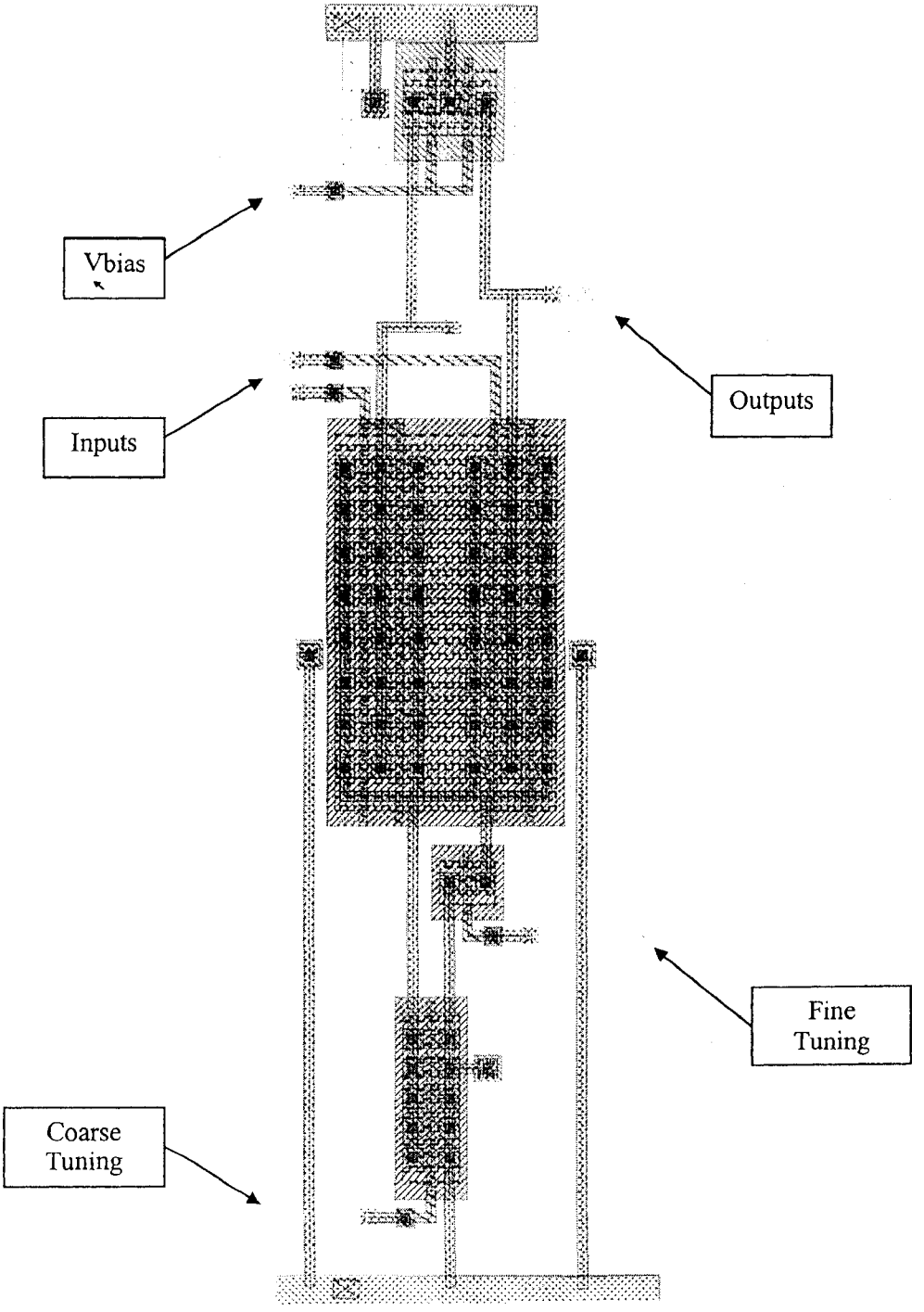

Figure 4.25 Single delay cell layout

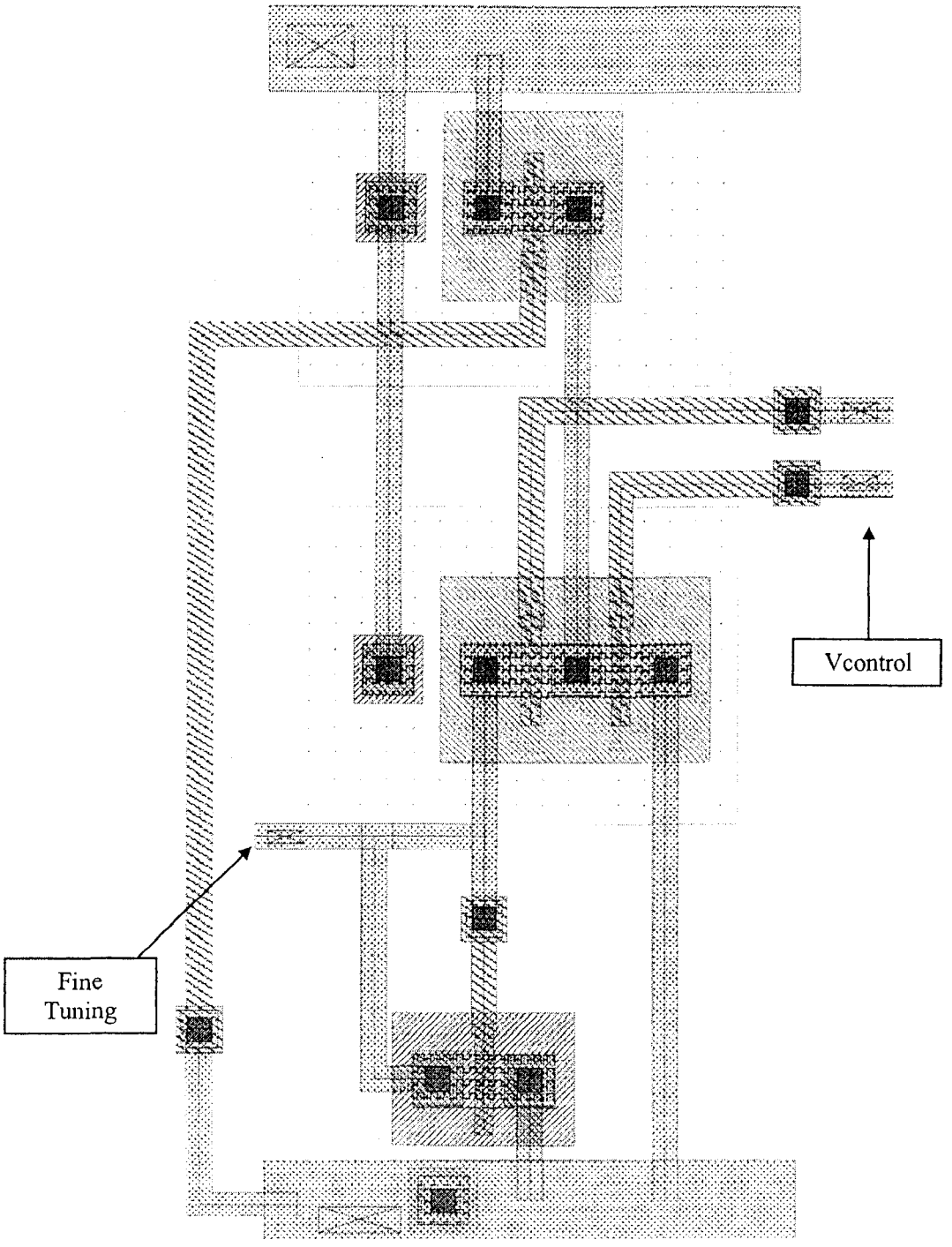

Figure 4.26 Fine tuning layout

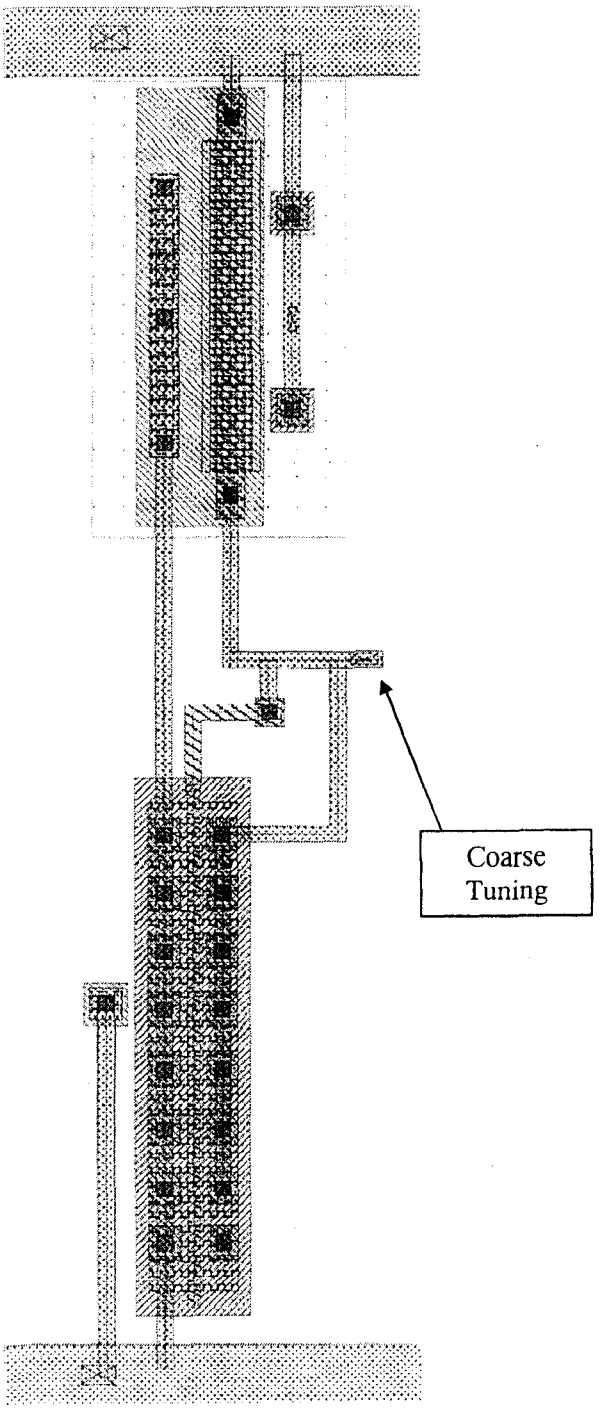

Figure 4.27 Coarse tuning layout

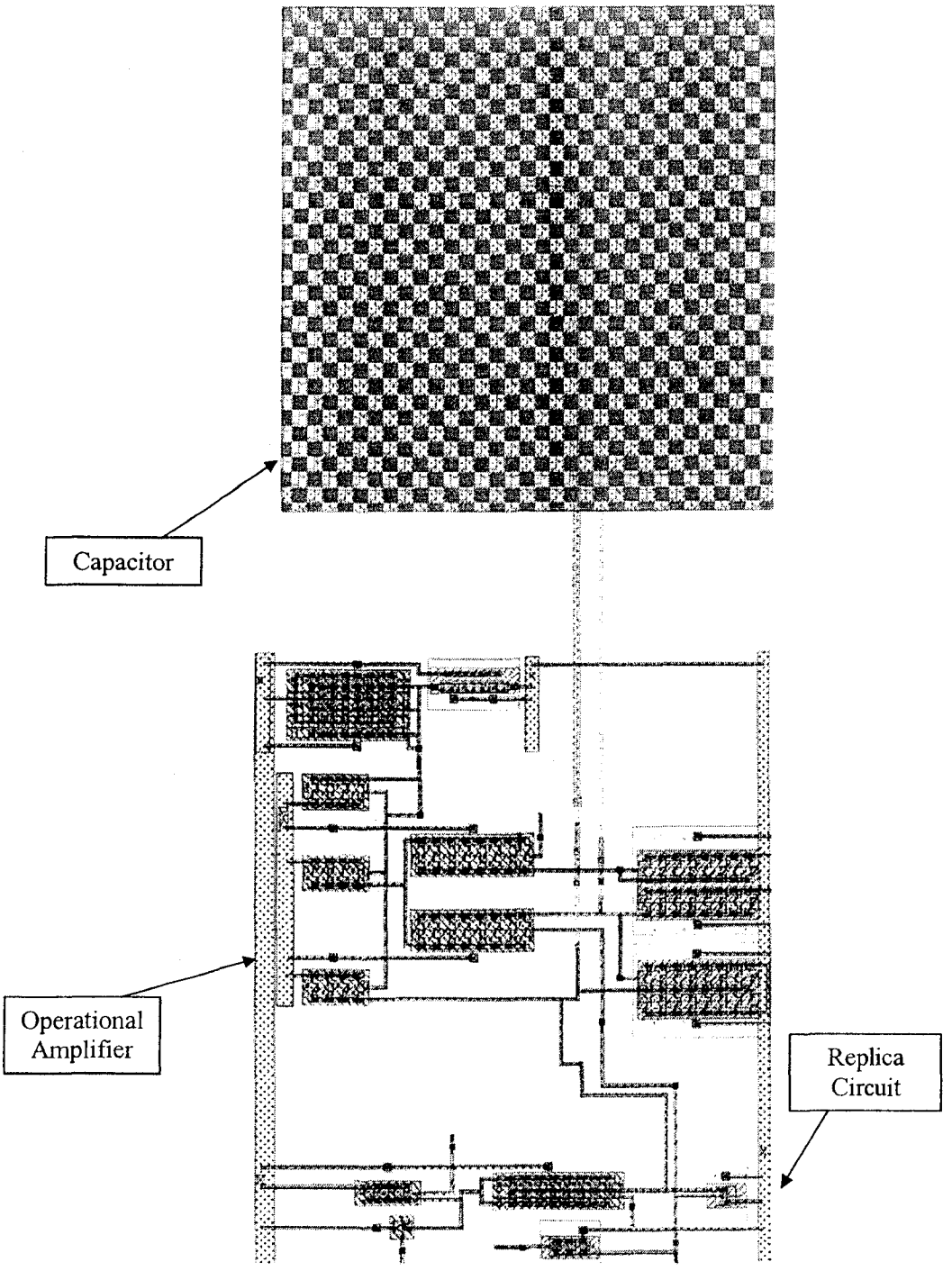

Figure 4.28 Replica biasing layout

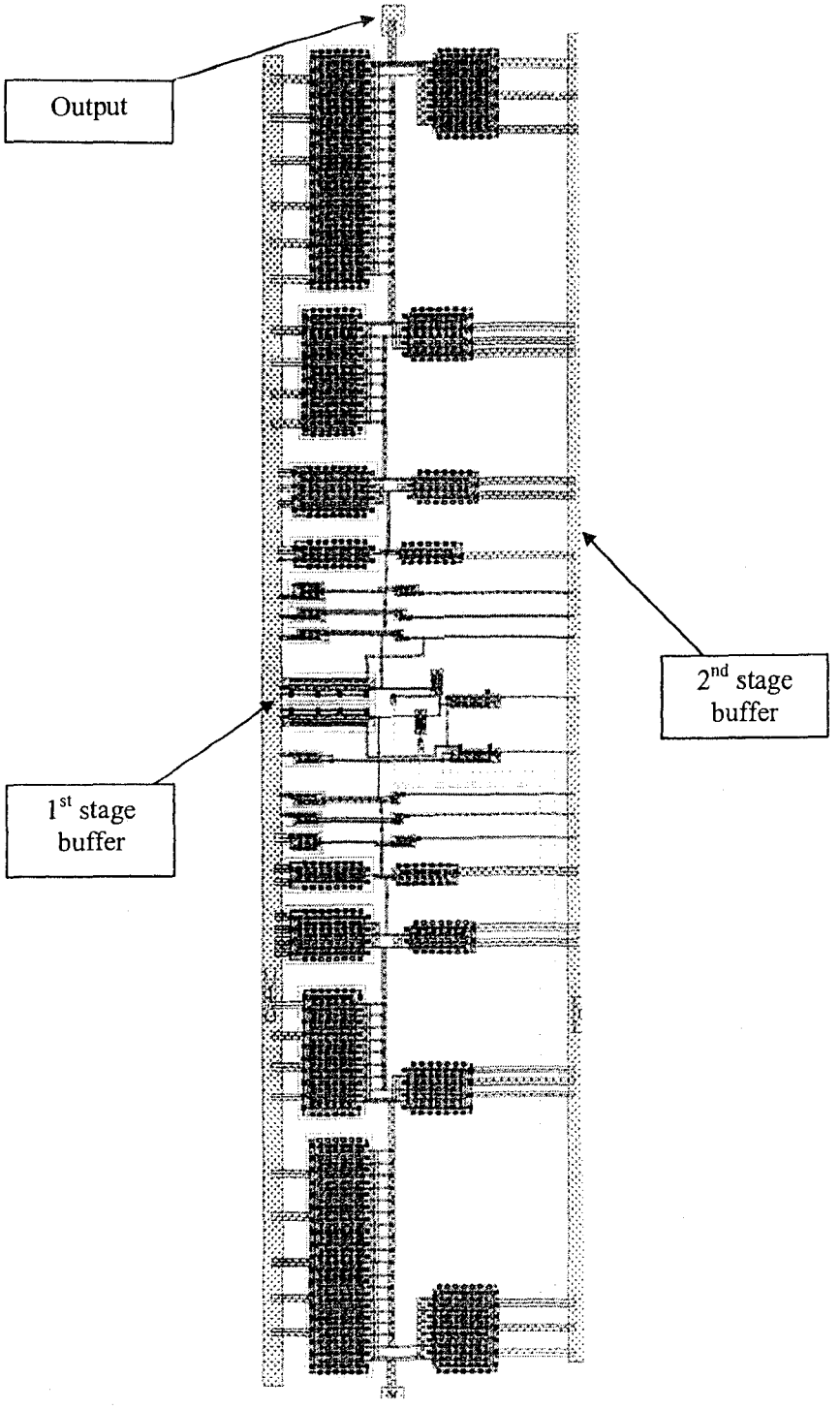

Figure 4.29 Output Buffer layout

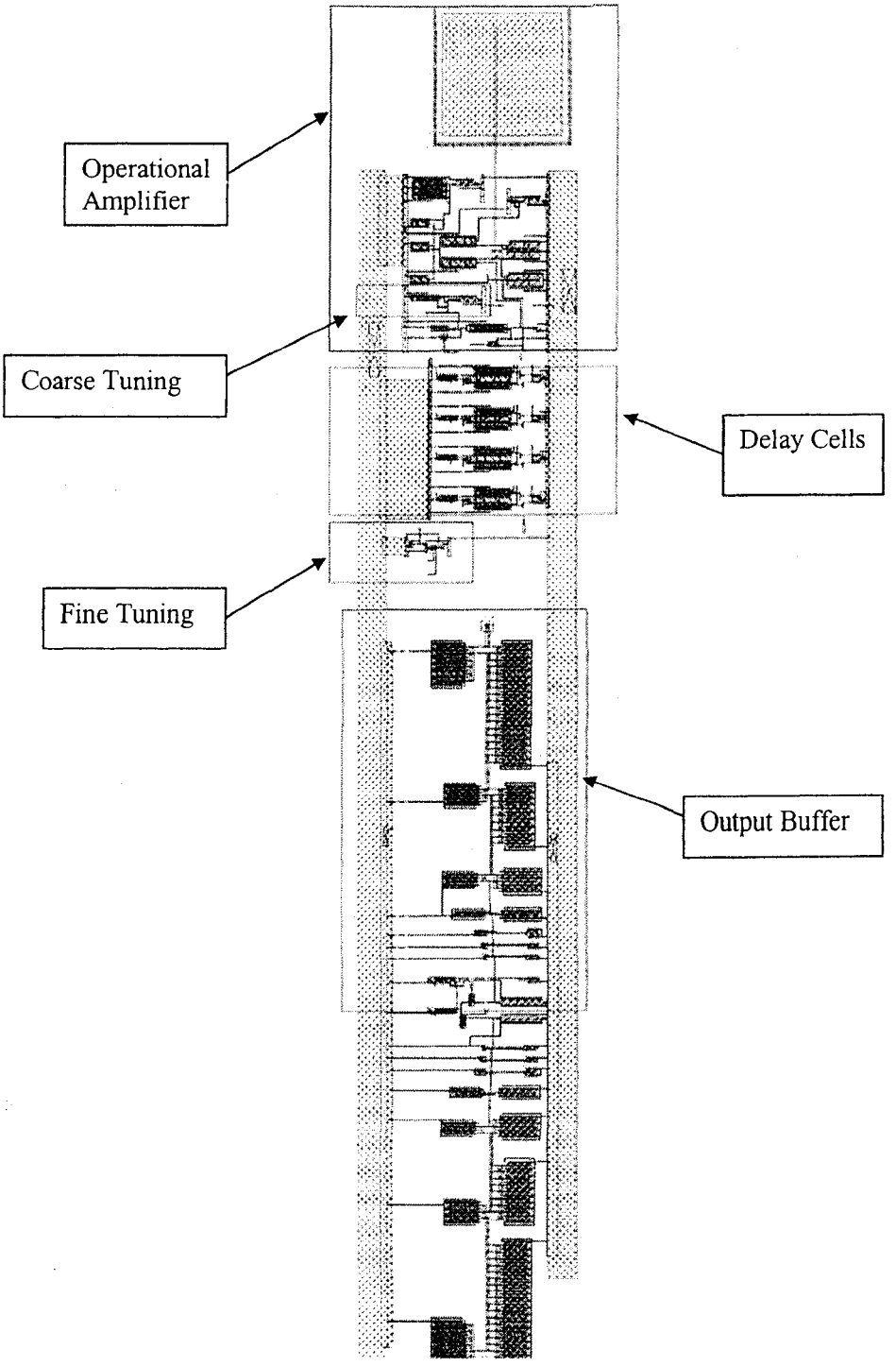

Figure 4.30 Overall ring VCO layout

The chip layout is shown in Fig. 4.31. The differential ring VCO described in this chapter and a cross-coupled LC VCO are implemented in this chip. The cross-coupled LC VCO was designed by another graduated student. The on-off state of the ring and LC oscillator is controlled by two separated external signals labelled as Vcontrol and Vc. respectively. The ring VCO inputs and outputs are labelled as Vtune+, Vtune- and VCO+, VCO- respectively. Before sending the chip for fabrication, the chip must contain a certain amount of density in all 6 metal layers, poly layer, and capacitance layer. To meet the density requirement, the chip is filled up with dummy layers. The test chip layout is 1000um x 1000um.

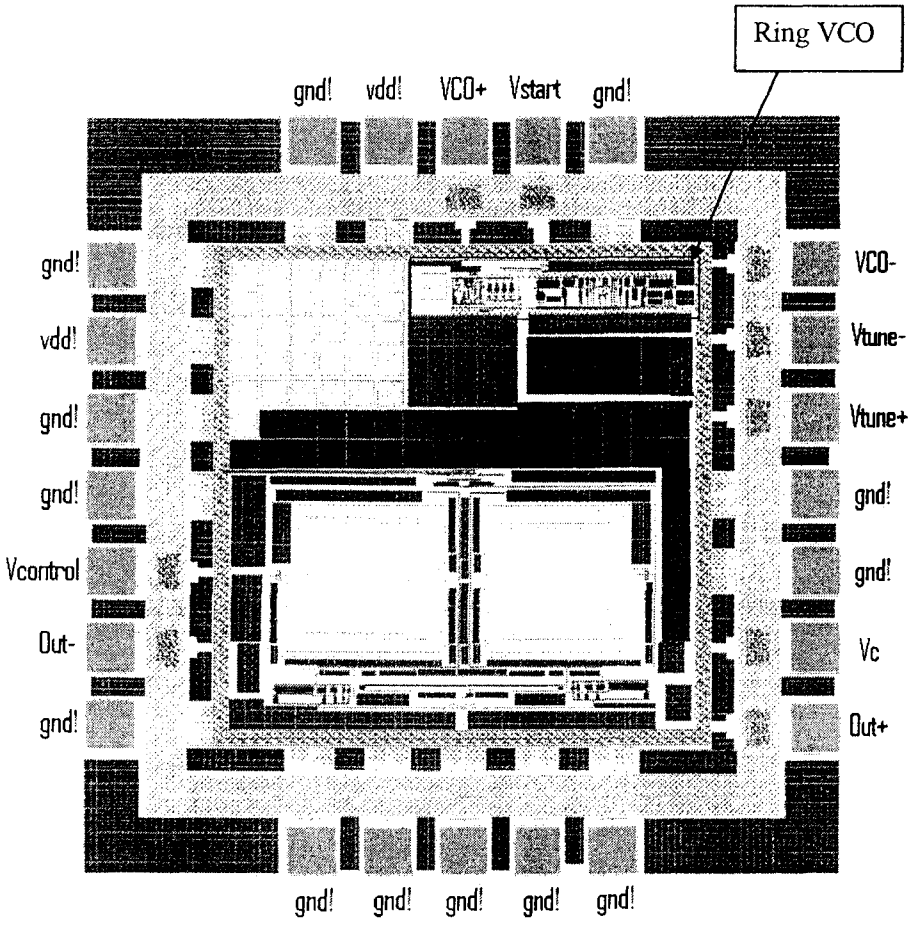

Figure 4.31 Test chip layout

4.5 Simulation Results

The difference between pre-layout simulation and post-layout simulation is that the former does not take parasitic components into account. The range of oscillation frequencies attainable through changing differential control voltages is plotted. The overall design with loads was pre-layout simulated. Loads include package, test fixture and a 50 ohm resistor. Note the load should also include pads for more accurate simulation.

The input voltage versus the output frequency is shown in Fig. 4.32. Both simulation results indicate similar range of oscillation frequency. The VCO gain is 0.3GHz/V. The VCO gain can also be obtained by the analytical calculation using Eq. (4.11) which gives a gain of 0.355GHz/V. There are some discrepancies among these results due to the fact that the result from using the analytical simulation is just an approximation. The results from pre-layout and post-layout simulation are different because pre-layout elements do not include some parasitic elements as we discussed in Section 4.3.1.

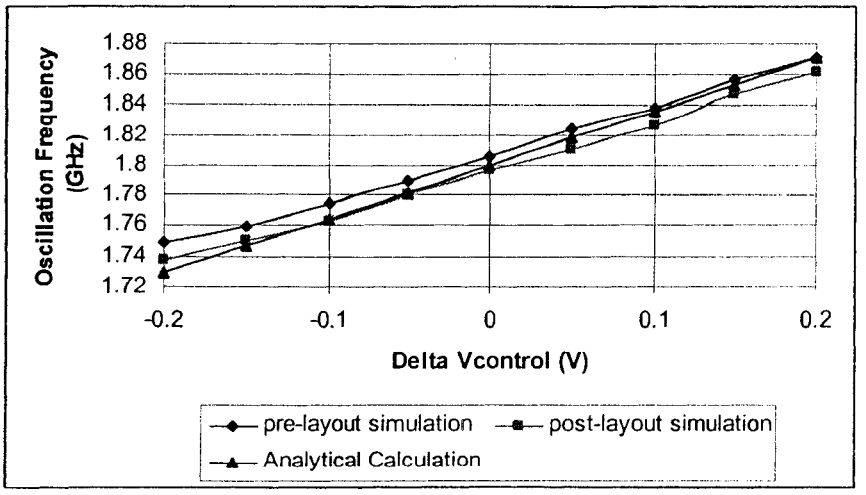

Figure 4.32 Oscillation frequencies versus control voltages

Lastly, simulation results from the post-layout simulation at the 2nd buffer output are shown in Fig. 4.33. The pre-layout simulation with load gives in Fig. 4.34.

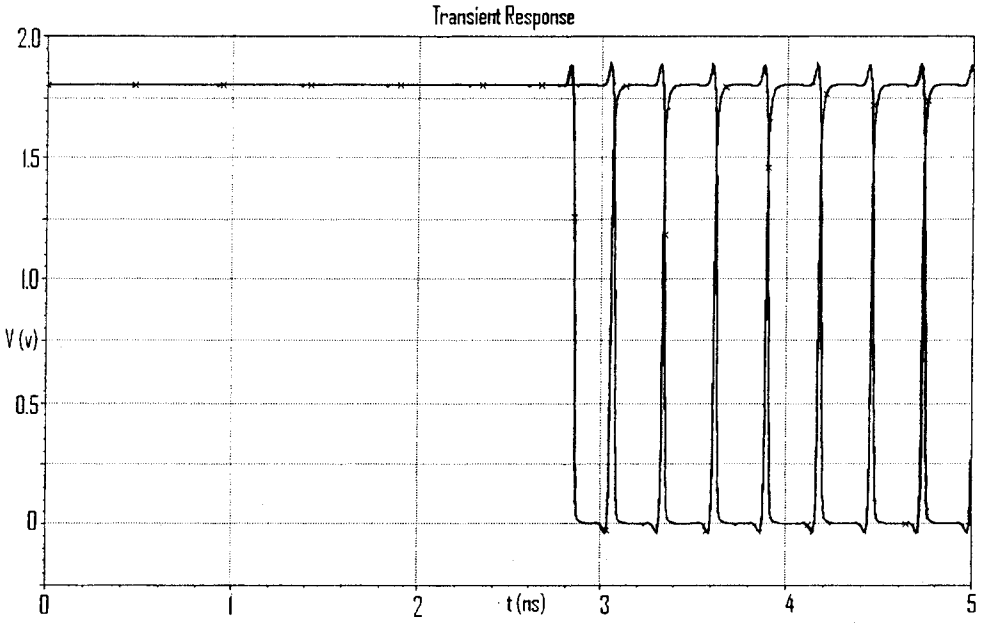

Figure 4.33 Post-layout simulation at the 2nd buffer output

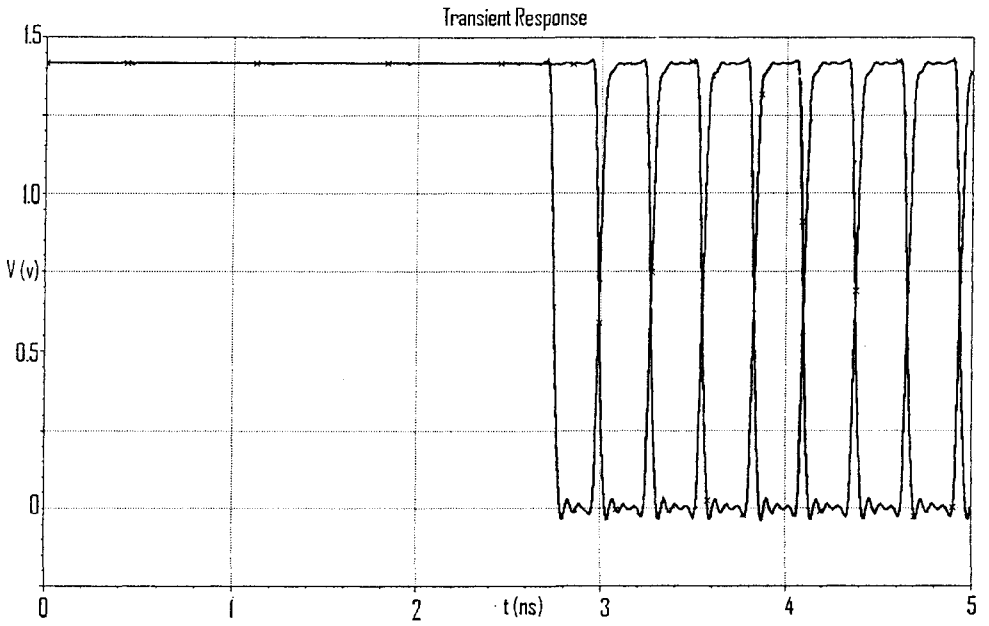

Figure 4.34 Pre-layout simulation with package, test fixture, and 50 ohm resistor

Due to some errors in our layout design, we were not able to provide experimental results. To verify those layout errors, test procedures are described in **Appendix A**

Chapter 5

Multi-Time Analysis / Envelope Harmonic Balance

5.1 Introduction

Transient simulation of circuits with widely separated time constants and fast periodic excitations is not efficient because a long simulation period with small time steps is required. As explained in Chapter 2, the MPDE approach allows a more efficient simulation circuits with AM signals. If FM signals are present, the WaMPDE method can be used. This work will focus on the EHB analysis which is a particular implementation of the MPDE method with the periodic time dimension treated in frequency domain, as explained in Section 2.3.3. In this chapter the companion models for the EHB analysis are presented. To test how efficient this method is compared to the traditional transient analysis, simulations of a VCO with both methods are presented.

5.2 Companion Models for EHB Analysis

In Section 2.4, companion models for transient analysis were explained and in this section, we derive the companion models for linear and nonlinear elements used in the EHB method. We will discuss linear components first followed by nonlinear components.

5.2.1 Linear Transconductances

As we mentioned before, linear resistances in the time domain can be described as

$$i = g \cdot v$$

To express transconductances in the frequency domain, the following expression is used

$$\bar{I} = G\bar{V} \Leftrightarrow \begin{bmatrix} I_0 \\ I_1 \\ \vdots \\ \vdots \\ I_N \end{bmatrix} = \begin{bmatrix} g & 0 & \cdots & \cdots & 0 \\ 0 & g & 0 & \cdots & 0 \\ \vdots & 0 & \ddots & 0 & \vdots \\ \vdots & \vdots & 0 & \ddots & 0 \\ 0 & \cdots & \cdots & 0 & g \end{bmatrix} \begin{bmatrix} V_0 \\ V_1 \\ \vdots \\ \vdots \\ V_N \end{bmatrix} \tag{5.1}$$

where $\bar{I}$ and $\bar{V}$ are current and voltage respectively in the frequency domain and G is a diagonal matrix. The subscript N represents number of harmonics. The companion model of a resistor is illustrated in Fig. 5.1.

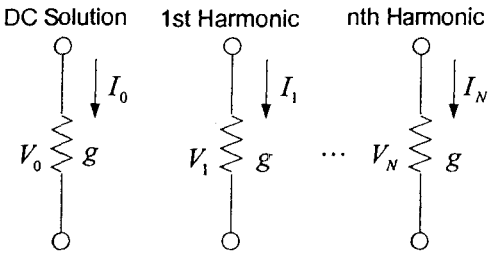

Figure 5.1 Companion model of a linear transconductance used in EHB

5.2.2 Linear Capacitor

The current in a capacitor is given by

$$i = C\frac{dv(t)}{dt}$$

Next, we re-formulate the voltage term into two time dimensions so the voltage term $v(t)$ is expressed as $\hat{v}(t_1,t_2)$. The derivative term in frequency domain using two-time dimensions is

$$\frac{d\overline{V}(t)}{dt} = \frac{\partial \overline{V}(t_1)}{\partial t_1} + F\frac{\partial \hat{v}(t_1,t_2)}{\partial t_2}$$

The term $\overline{V}(t_1)$ is a time-varying phasor in the mixed time and frequency domain. The partial derivative of this function with respect to t_1 is solved by the BE method.

$$\frac{\partial \overline{V}(t_1)}{\partial t_1} \simeq \frac{\overline{V}\left(t_{1(n)}\right) - \overline{V}\left(t_{1(n-1)}\right)}{h} \tag{5.2}$$

where $n-1$ and n are the last calculated sample and the next calculated sample respectively. The term h is the chosen time step. The derivative term with respect to t_2 is perform by a multiplication of $j\Omega$

$$\frac{\partial \hat{v}(t_1,t_2)}{\partial t_2} \rightarrow j\Omega \cdot \overline{V}(t_1) \tag{5.3}$$

where the matrix Ω can be expressed as

$$\Omega = \begin{bmatrix} 0 & 0 & 0 & \cdots & 0 \\ 0 & \omega_1 & 0 & \cdots & 0 \\ 0 & 0 & \ddots & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & N\omega_1 \end{bmatrix}$$

with ω_1 being the fundamental angular frequency and N is the harmonic number. Then the companion model of a capacitor is equal to

$$\bar{I}_n = C\left[j\Omega\bar{V}_n + \frac{\bar{V}_{n+1} - \bar{V}_n}{h} \right] \tag{5.4}$$

and can be rewritten as

$$\bar{I}_n = C\begin{bmatrix} 0 \\ j\omega_1 V_n \\ \vdots \\ jN\omega_1 V_{Nn} \end{bmatrix} + \begin{bmatrix} \frac{V_{0(n)} - V_{0(n-1)}}{h} \\ \frac{V_{1(n)} - V_{1(n-1)}}{h} \\ \vdots \\ \frac{V_{N(n)} - V_{N(n-1)}}{h} \end{bmatrix} = C\left(j\Omega + \frac{1}{h}U \right)\bar{V}_n - C\frac{1}{h}\bar{V}_{n-1}$$

where U is the identity matrix

The equivalent circuit representation of the companion model for a single linear capacitor in the time-frequency domain is

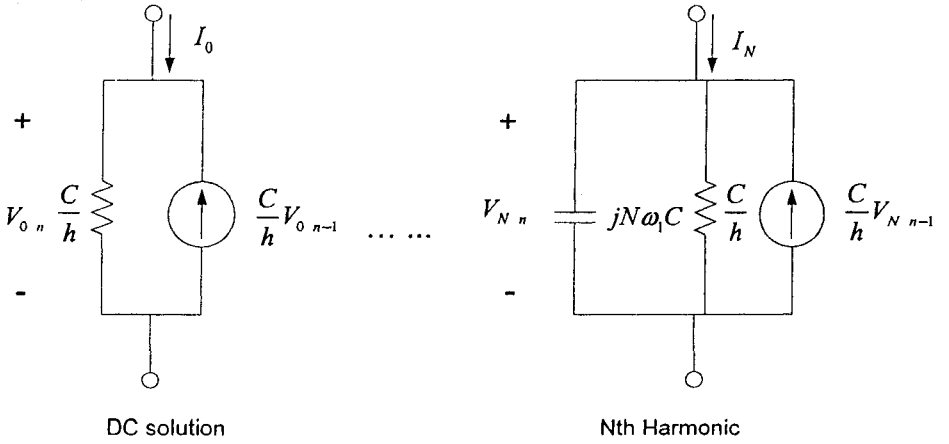

Figure 5.2 Companion model of a capacitance in EHB

5.2.3 Nonlinear Current Sources

Companion models for nonlinear resistors and capacitors can be derived in a similar manner to the methods used above with the addition of a nonlinear method. As we discussed in Chapter 2, Newton's method applied to a nonlinear current source results in

$$i\left(v^{k+1}\right) = i\left(v^{k}\right) + \frac{di}{dv}\left(v^{k+1} - v^{k}\right)$$

To describe the nonlinear current sources in the time-frequency domain, the derivative term in Newton's method is replaced by the Jacobian matrix J_i. The expression above can be rewritten as

$$\bar{i}\left(\bar{v}^{k+1}\right) = \bar{i}\left(\bar{v}^{k}\right) + J_i\left(\bar{v}^{k+1} - \bar{v}^{k}\right) \tag{5.5}$$

The Jacobian matrix J_i for a one period in fast time dimension is given as

$$J_i = \begin{bmatrix} \dfrac{di\left(v^k(t_0)\right)}{dv} & 0 & 0 & \cdots & 0 \\ 0 & \ddots & 0 & \cdots & 0 \\ 0 & 0 & \ddots & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & \dfrac{di\left(v^k(t_m)\right)}{dv} \end{bmatrix}$$

and the index m corresponds to the number of voltage samples in time domain..

To convert the expression above from the time domain into the frequency domain, DFT method is applied and the above expression in the frequency domain can be rewritten as

$$\bar{I}\left(\bar{V}^{k+1}\right) = F\bar{i}\left(F^{-1}\bar{V}^{k}\right) + FJ_iF^{-1}\left(\bar{V}^{k+1} - \bar{V}^{k}\right)$$

where $\bar{I}$ and $\bar{V}$ are current and voltage in the frequency domain; F and F^{-1} are DFT and IDFT respectively. This expression can be expanded to

$$\bar{I}\left(\bar{V}^{k+1}\right) = \left(FJ_iF^{-1}\right)\bar{V}^{k+1} + F\bar{i}\left(F^{-1}\bar{V}^{k}\right) - \left(FJ_iF^{-1}\right)\bar{V}^{k}$$

Fig. 5.3 shows the DC solution to the companion model of a nonlinear current source. There is a similar companion model for each considered frequency. For convenience, we set the matrix term $\left(FJ_iF^{-1}\right)$ equal to [y] where N is the number of harmonics.

$$[y] = \begin{bmatrix} y_{00} & y_{01} & \cdots & \cdots & y_{0N} \\ y_{10} & \ddots & \cdots & \cdots & y_{1N} \\ \vdots & \vdots & \ddots & \cdots & \vdots \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ y_{N0} & \cdots & \cdots & \cdots & y_{NN} \end{bmatrix}$$

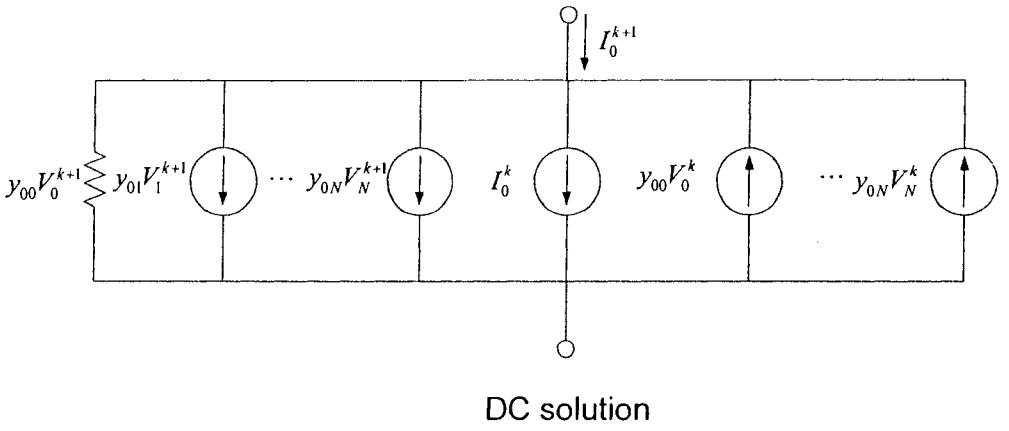

Figure 5.3 Companion model of a nonlinear resistor used in EHB

5.2.4 Nonlinear Capacitors

Lastly, to derive the companion model for nonlinear capacitors, charge is chosen instead of voltage as a state variable to avoid numerical errors in calculations [7]. The HB method is applied by taking partial derivative of the charge function with respect to t_2 and this gives

$$\frac{\partial \bar{q}(t_1, t_2)}{\partial t_2} \rightarrow j\Omega \cdot \bar{Q}(t_1) \tag{5.6}$$

The partial derivative of the charge function with respect to t_1 is given as

$$\frac{\partial \bar{q}(t_1)}{\partial t_1} \simeq \frac{\bar{q}(t_{1n}) - \bar{q}(t_{1(n-1)})}{h} \tag{5.7}$$

Applying DFT to Eq. (5.6) and Eq. (5.7), the analytical expression of the companion model of a nonlinear capacitor in time-frequency domain can be written as

$$\bar{I}_n = j\Omega \cdot \bar{Q}_n + \frac{\bar{Q}_n - \bar{Q}_{n-1}}{h} = \left[j\Omega + \frac{1}{h} \cdot U \right] \cdot \bar{Q}_n - \frac{\bar{Q}_{n-1}}{h} \tag{5.8}$$

where U is the identity matrix and

$$j\Omega + \frac{1}{h}U = \begin{bmatrix} 1/h & 0 & \cdots & 0 \\ 0 & 1/h + j\omega_1 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & 1/h + jN\omega_1 \end{bmatrix}$$

The unknown term $\bar{Q}_n$ can be solved using the Newton method which is the same approach we used to solve the charge term in time domain. Here the charge solved by the Newton method can be expressed as

$$\bar{Q}_n = \bar{Q}\left(F^{-1}\bar{V}_n^k\right) + \left(FJ_Q F^{-1}\right)\bar{V}_n^{k+1} - \left(FJ_Q F^{-1}\right)\bar{V}_n^k$$

Then Eq. (5.8) can be expanded into the following form

$$\bar{I} = \left[\left(j\Omega + \frac{1}{h} \cdot U \right) FJ_Q F^{-1} \right] \bar{V}_n^{k+1} + \left(j\Omega + \frac{1}{h} \cdot U \right) \cdot \left(\bar{Q}\left(F^{-1}\bar{V}_n^k \right) - FJ_Q F^{-1}\bar{V}_n^k \right) - \frac{\bar{Q}_{n-1}}{h}$$

Fig. 5.4 shows the companion model for the DC circuit of a nonlinear capacitor and also there is a similar companion model for each considered frequency. For convenience, we set the matrix term $\left(FJ_Q F^{-1}\right)$ equal to [y] and $\left(j\Omega + \frac{1}{h} \cdot U \right)$ equal to [x].

$$[x] = \begin{bmatrix} x_{00} & x_{01} & \cdots & \cdots & x_{0N} \\ x_{10} & \ddots & \cdots & \cdots & x_{1N} \\ \vdots & \vdots & \ddots & \cdots & \vdots \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ x_{N0} & \cdots & \cdots & \cdots & x_{NN} \end{bmatrix}$$

$$[y]=\begin{bmatrix} y_{00} & y_{01} & \cdots & \cdots & y_{0N} \\ y_{10} & \ddots & \cdots & \cdots & y_{1N} \\ \vdots & \vdots & \ddots & \cdots & \vdots \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ y_{N0} & \cdots & \cdots & \cdots & y_{NN} \end{bmatrix}$$

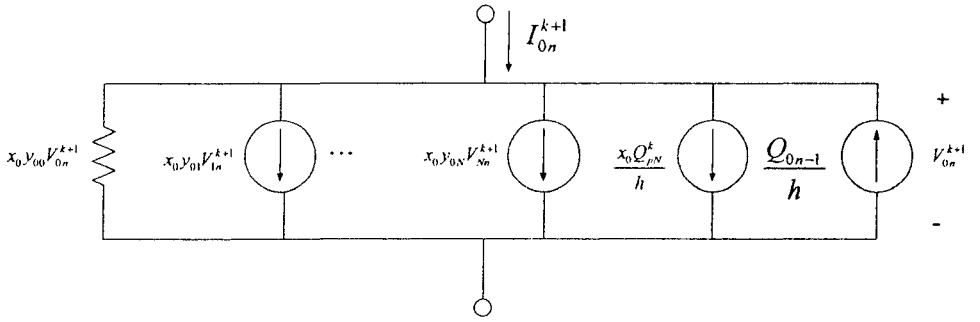

Figure 5.4 Companion model of a nonlinear capacitance used in EHB

5.3 Ring Oscillator with Open Loop Test

Due to some limitations to the Level 3 MOS model, our goal is to design a ring oscillator which oscillates at its highest frequency with similar circuitry discussed in Chapter 4 but with larger geometries. Transistor parameters were chosen with a minimum length of 0.4 μm. Then a procedure similar to the one described in Chapter 4 was used to design this ring VCO using Cadence. Next, the same circuit was simulated with ngspice and Carrot. Results are shown in Fig. 5.5, Fig. 5.6 and Fig. 5.7 with oscillation frequency of 1.94GHz, 2.5GHz, and 2.7GHz based on the Spectre, ngspice, and Carrot simulator programs respectively. The carrot and ngspice netlists are in Appendix B and all the design values are documented in netlists.

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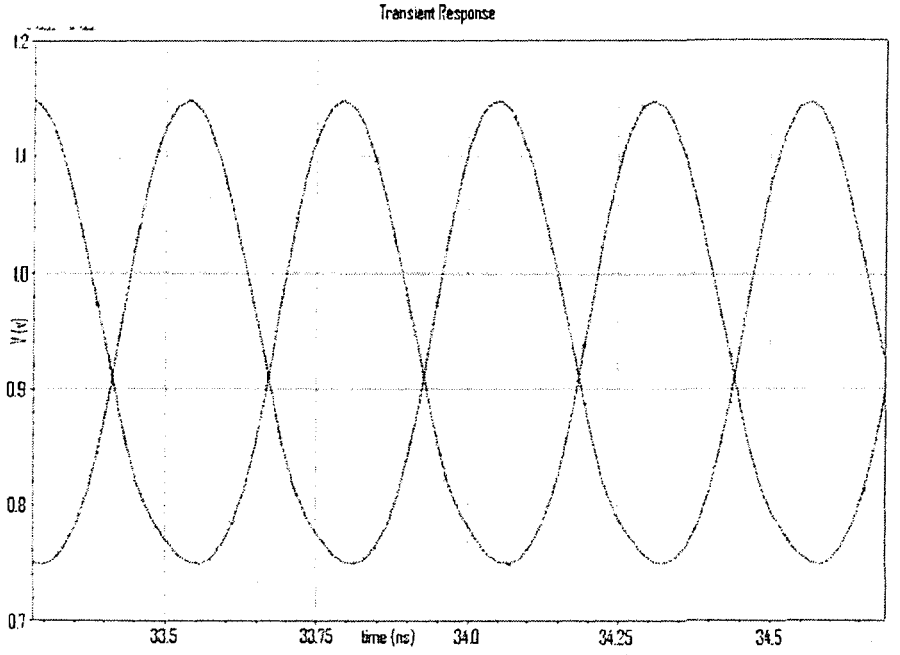

Figure 5.5 Ring VCO output waveforms from Spectre

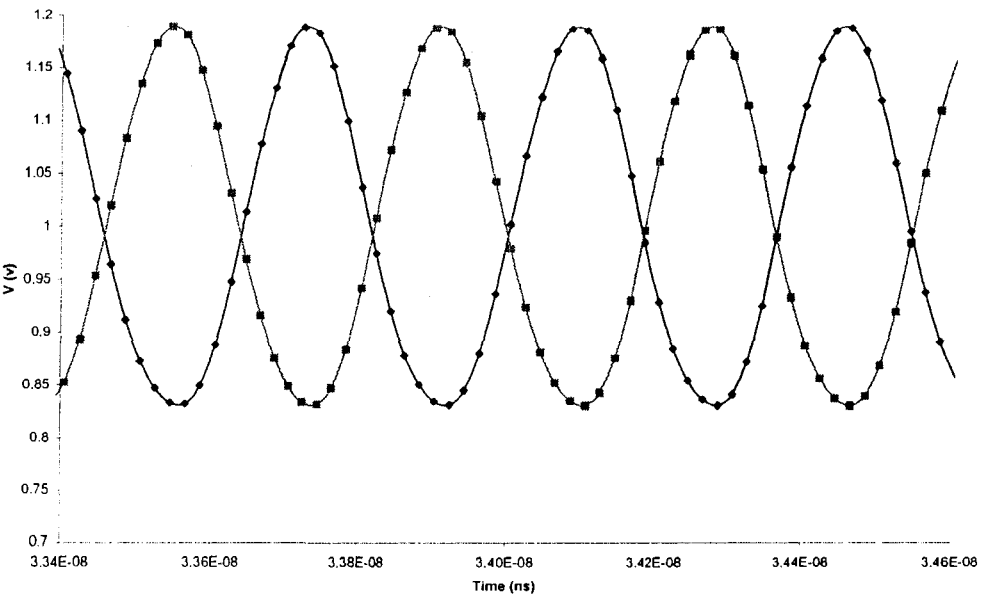

Figure 5.6 Ring VCO output waveforms from ngspice

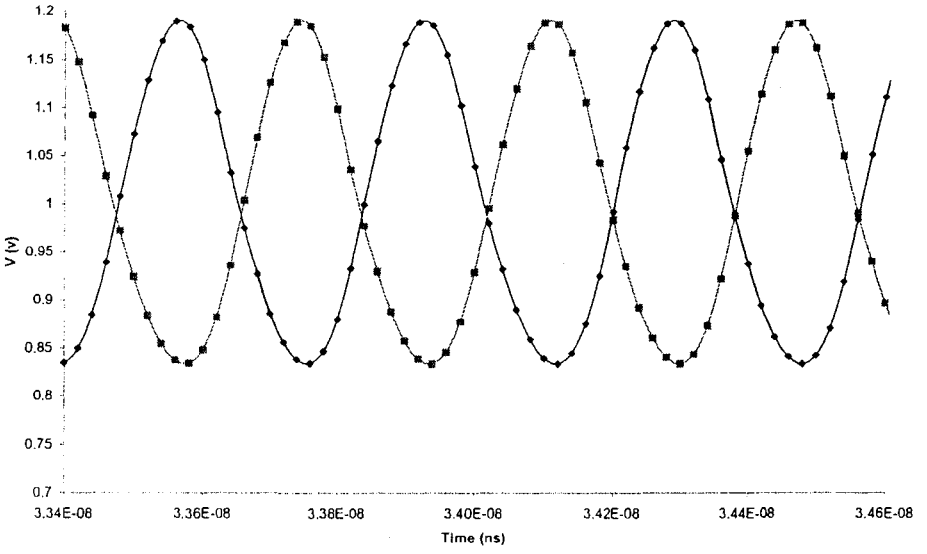

Figure 5.7 Ring VCO output waveforms from Carrot

One of the reasons for the discrepancies is that even though I-V characteristics are the same with a minimum transistor length of 3 μm, it is not necessary true that they will give same results as transistor sizes are scaled down to 0.4 μm. After we generated the I-V graphs from three simulators presented in Fig. 5.8, we discovered that drain current from Spectre are lower than those of from other two simulators. This is an indication that Level 3 model in Spectre is not the same as in ngSpice. In addition capacitance models are implemented differently in Carrot and ngspice, therefore the oscillation frequency is not exactly the same either even with the same DC characteristics. Also, if we look at results of the replica biasing voltage given in Fig. 5.9, Fig. 5.10, and Fig. 5.11, it is evident that the transistors are not equally biased in the three simulations, but the differences are most pronounced in Spectre, due to different DC characteristics. Results from ngspice and Carrot tend to be closer but results are different after 1 μs simulation time. This is possible due to different capacitance model being implemented in two program simulations.

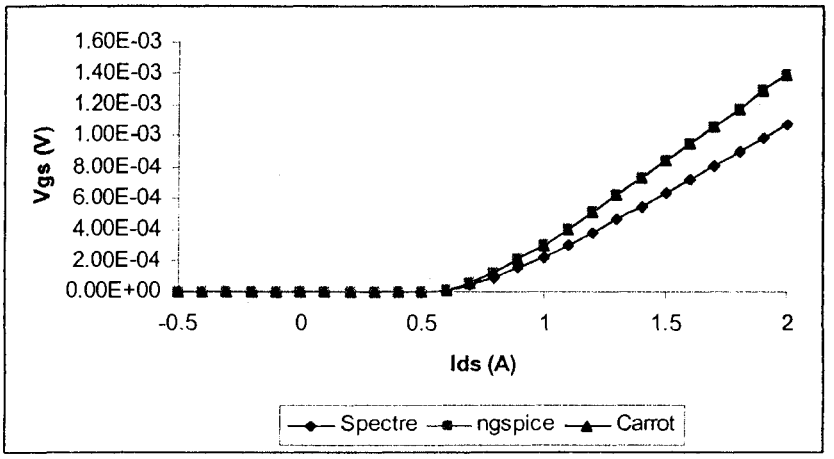

Figure 5.8 Vgs vs Ids at Vmax=1e5 and (W/L=4/0.4)

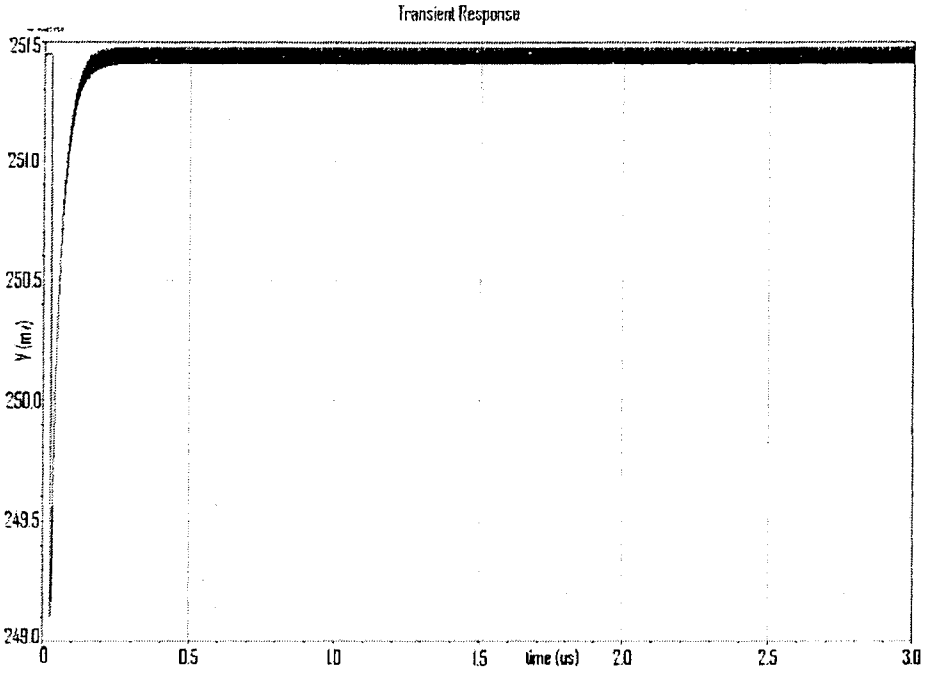

Figure 5.9 Replica biasing voltage from Spectre

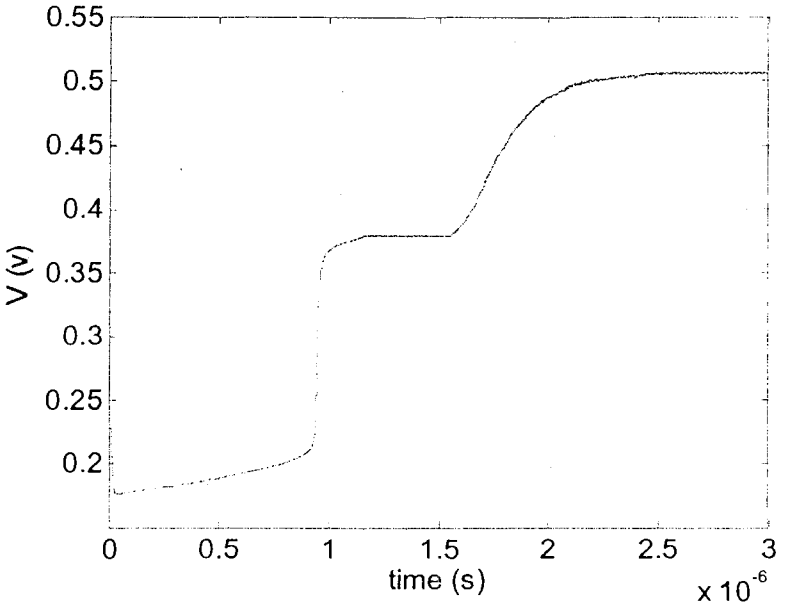

Figure 5.10 Replica biasing voltage from ngspice

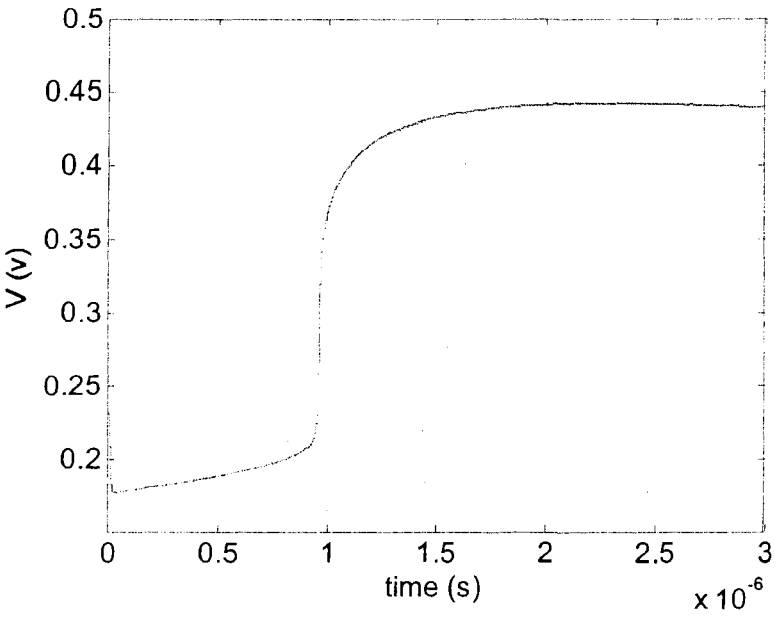

Figure 5.11 Replica biasing voltage from Carrot

Since the WaMPDE is not currently implemented in Carrot, it is not possible to analyze the unmodified VCO circuit with multiple time dimensions. However if the feedback loop is opened as shown in Fig. 5.13, the circuit is no longer autonomous and can be analyzed with the EHB analysis. Simulated oscillation signals are injected at the inputs of the first delay cell. A problem in the original replica biasing circuit design is that this voltage increases abruptly at 1 μs and this cause the PMOS resistive load transistors operated in the wrong region. The oscillation frequency can vary and this causes stability problem in both EHB and transient analysis while running the opened-loop test. Therefore, the replica biasing circuit is modified so that the voltage stays at the right region and its output characteristic is in Fig. 5.12.

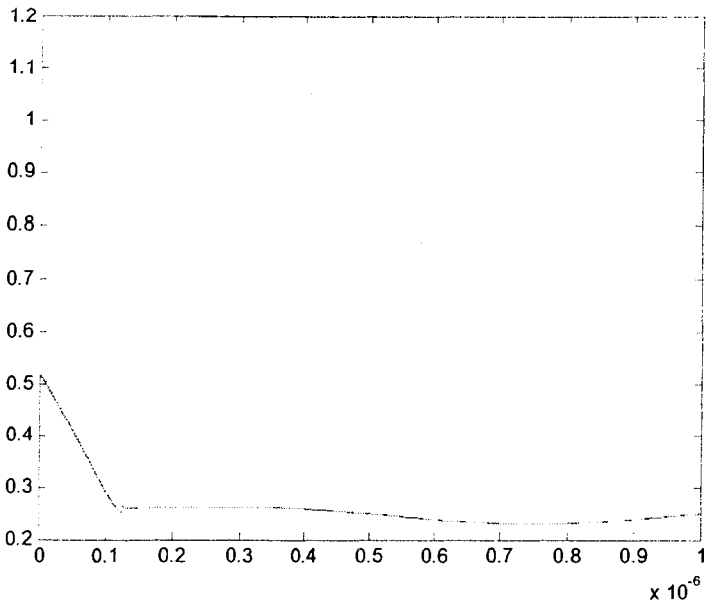

Figure 5.12 Replica biasing voltage with modify circuit

Two sinusoidal signals similar to the oscillation frequency signals are injected into the VCO inputs. The oscillation frequency is around 2.7 GHz with a voltage swing of 0.248V and a common mode voltage of 1.622V. To generate slow time vary signals at the fine tuning input, two 1 MHz sinusoidal signals with amplitude of 0.1V and common mode voltage at 0.85V are selected. Next, tests are made to evaluate how effectiveness of the EHB is compared to the transient analysis.

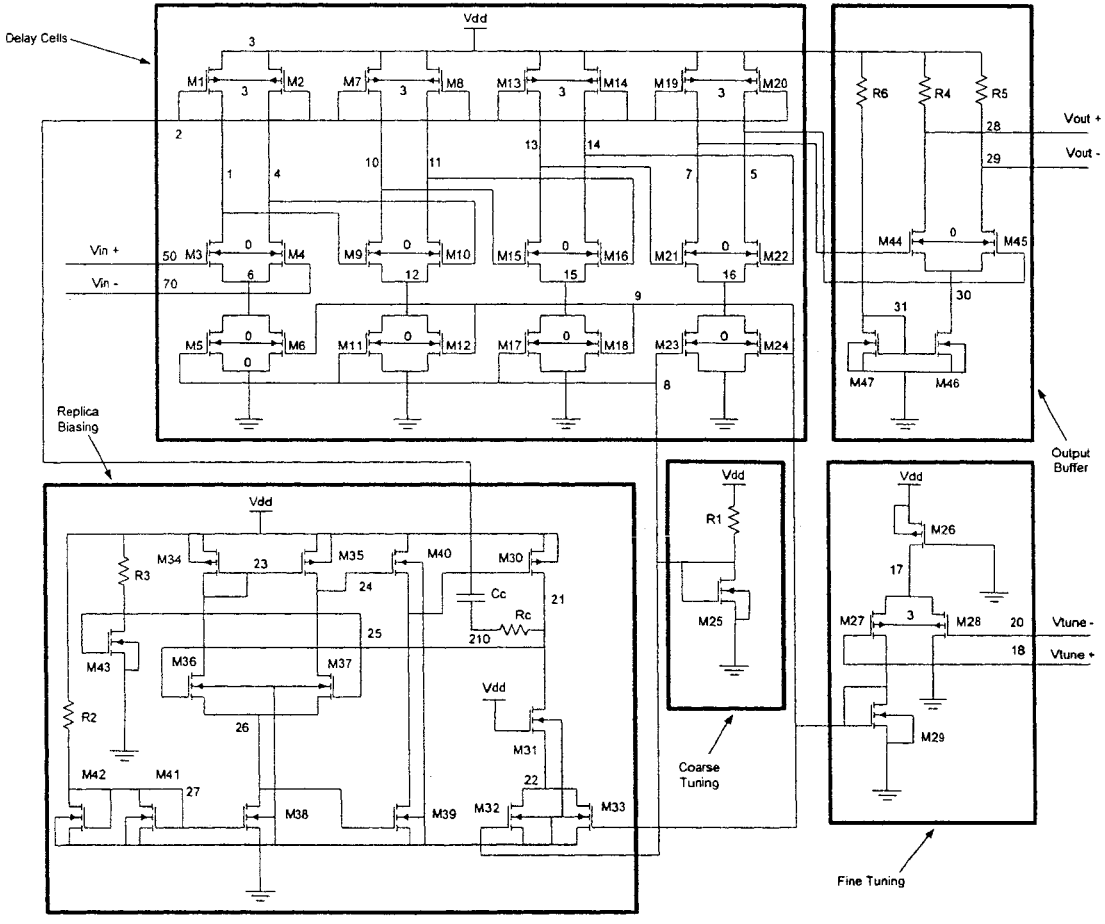

Figure 5.13 VCO Opened-loop test circuit

5.4 Simulation Results

This section shows simulation results to compare the performances of EHB with $1\,ns$ sampling time and traditional transient analysis with $20\,ps$ sampling time. As we discussed in Chapter 2, multi-time scale simulation method usually require less sample points to reproduce signals having widely separated rates. Results of opened-loop test using traditional transient analysis and EHB method are shown in Fig. 5.14, and Fig. 5.15 respectively. Next, we extracted the result at the replica biasing output from the EHB simulation to be compared with the results of the regular transient simulation. This is done by taking a set of data from the fast time axis and using IDFT method to convert data from the frequency to time domain. This is given in Fig. 5.16.

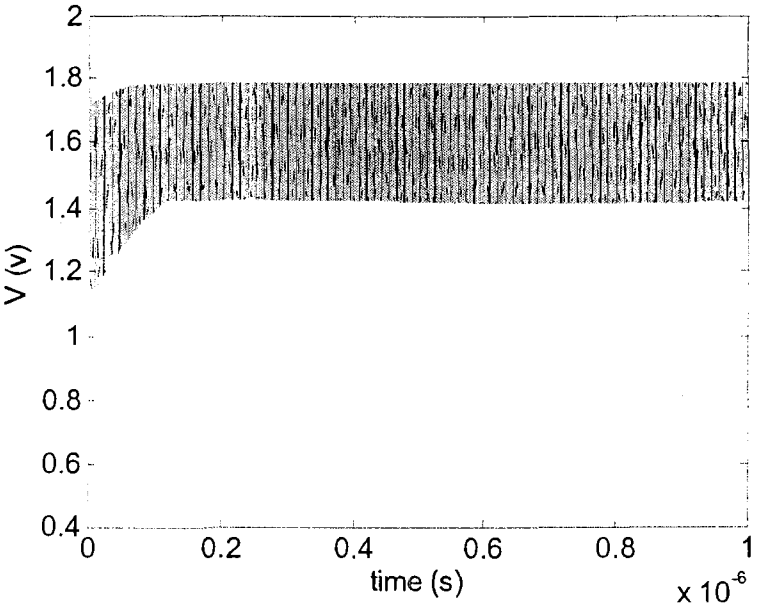

Figure 5.14 Voltage at the delay cell using regular transient analysis

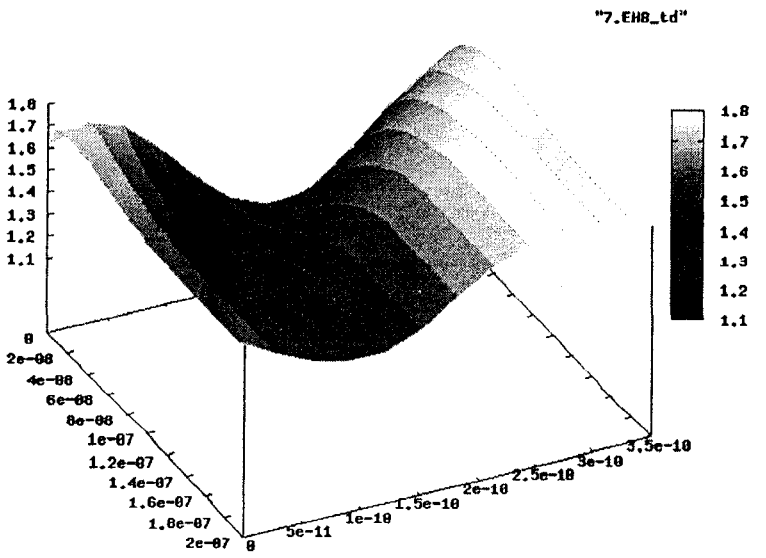

Figure 5.15 Voltage at the delay cell output using EHB method

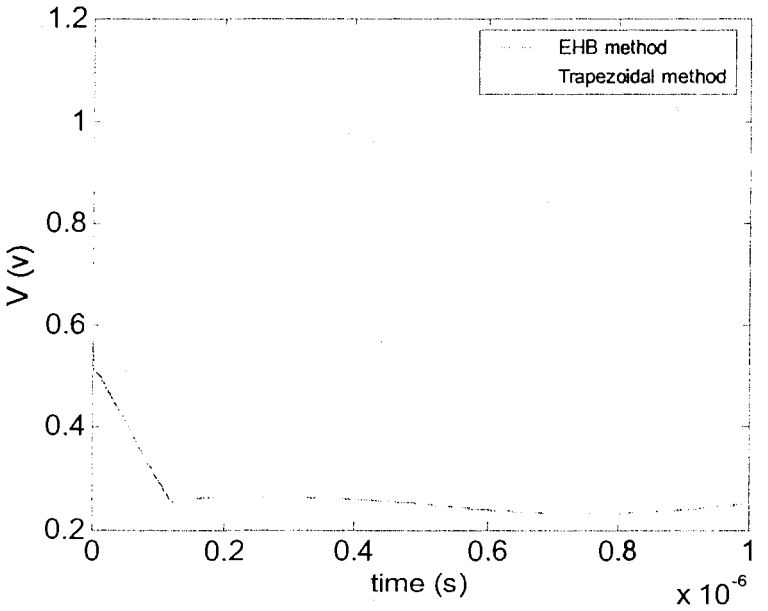

Figure 5.16 Comparison between two simulators at the replica biasing output

To verify results in Fig. 5.15 agrees with the one in Fig 5.14, we can compare the peak-to-peak voltage of the fast transient signal between the last line of the 3-D plot and the signal from Fig. 5.14 From Fig. 5.17 and Fig. 5.18, the peak-to-peak voltage values between two graphs are identical so we know that results are correct in EHB method. The frequency values in two graphs are different because we did not calculate the real time values and the phase information was lost.

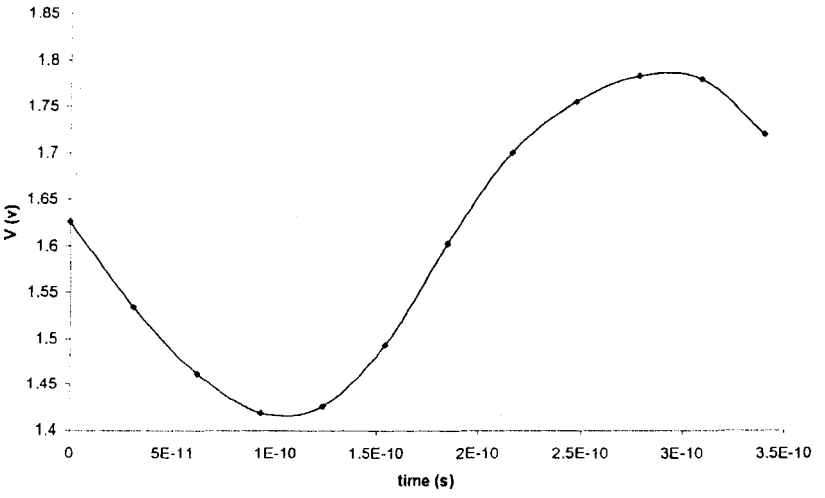

Figure 5.17 Voltage at the delay cell output using EHB method in 2-D expression

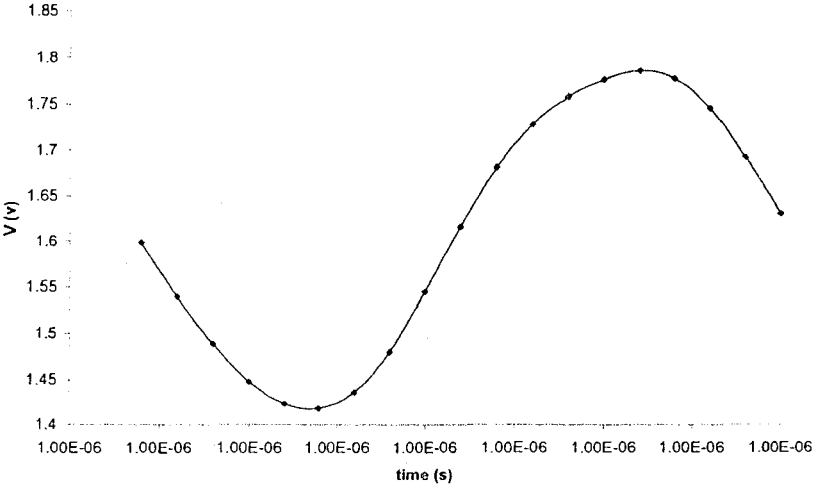

Figure 5.18 Voltage at the delay cell output using transient analysis

One advantage of EHB method is that the selected time step is independent of the high frequency signal because high frequency signal is handled in t_2 dimension. Thus, time step can be made very long compare to one period of the high frequency signal whereas when a long time step is used, the initial transient evolution is lost. Another advantage is that this method uses less CPU time than traditional transient method does. This is not only memory saving, but also time saving for designers. A total CPU time to run the EHB simulation for 4 harmonic numbers and 1 μs simulation period with 1 ns and 20 ns sampling time is given in Table 5.1. For comparison, a traditional transient analysis with 20 ns sampling time was simulated.

Table 5.1 CPU time comparison using EHB method with different sampling time

Sampling TIme	1 ns	20 ns	20 ns
CPU time	8min 5sec	1min 46sec	35min 48sec

The extracted results at node 2 are shown in Fig. 5.18. We can see that the result with 20 ns sampling time is not very accurate at first during the initial fast transient but it gets better with time. Thus to utilize the full potential of this method, it is necessary to implement a variable time step option in simulation

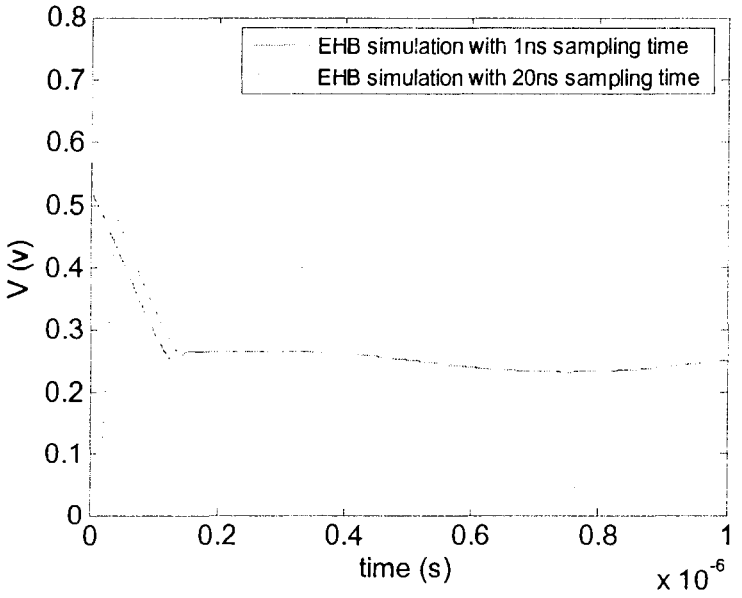

Figure 5.19 Extracted results from EHB method at the replica bias output

Chapter 6

Conclusion and Future Work

6.1 Conclusion

In this work, a Level 3 MOSFET model included both static and dynamic parts was successfully implemented into the Carrot simulator program. This requires an understanding of the theory behind MOSFETs. For the static model, correction factors based on the ngSpice source code were added to ensure the smoothness of DC characteristics. Meanwhile, the simplified Yang-Chatterjee charge model was used in the dynamic model to resolve discontinuity and charge conservation problem in Meyer's models. Both I-V and C-V characteristics for both N and P MOSFETs were compared with the ones in Spectre and ngspice. The I-V characteristics in the three simulators match well for medium channel lengths. The C-V characteristics were compared as well. There were discrepancies in the capacitances for some operating voltages but that is to be expected since the implemented charge model is different. However a transient analysis of a small circuit showed reasonable agreement. This is one of the issues that should be addressed in future work.

A 1.8 GHz differential ring VCO was fully designed initially using the TSMC 0.18 μm technology and Cadence tools. This provided a deep understanding of the circuit. The VCO was fabricated but due to errors in the layout it was not possible to test it. This circuit presents variations in widely separated time scales and so was used to evaluate the efficiency of the EHB method implemented in Carrot applied to complex CMOS circuits Due to limitations in the Level 3 MOSFET models, the ring VCO was scaled to a larger size.

The longer simulation periods of the EHB analysis evident a stability problem in the biasing network that was not detected before with regular transient analysis shorter simulations. The problem was solved by modifying parts in the existing replica circuitry.

The EHB simulation results were verified with the results of transient analysis. The current implementation of the EHB method only supports fixed time step. The results of an EHB simulation using a time step of $1\,ns$ agreed very well with the transient analysis results using a time step of $20\,ps$. An EHB simulation with a long time step of $20\,ns$ showed that the initial value was not very accurate during the initial fast transient but it became more accurate with time. Even if the chosen fixed time step is too long, the simulation has poor accuracy during the instants of fast variations but later the accuracy improves when variations become slower. This indicates that significant performance improvements can be achieved if an adaptive time step is implemented. It was shown that CPU time could be reduced by an order of magnitude or more with the EHB method if the variation scales are very different.

6.2 Future Work

A few improvements can be done to this work in the future. In the oscillator design, a reference circuit should be added to supply the required biasing current and the circuit will be independent of process variations. The replica biasing circuit should be modified according to what we discussed in the Section 5.3 to ensure the stability. Pads can be built in the schematic diagram so the same layout errors can be avoided in the future.

Next, for the MOSFET model, to compare the accuracy of the capacitor model in Carrot with other simulators, we can choose simulators that have the same capacitor model such as APLAC or Freeda. Another improvement to the current model is to implement more advanced models as we mentioned in Chapter 2. This will allow us to

simulate circuits containing small geometry transistors and we will be able to understand physical characteristics of MOSFETs with respect to changes in sizes.

Lastly, even though the EHB method can generate multi-rate signals more efficiently then the traditional transient does, to fully understand the potential of the EHB method, the adaptive time step option is required to be implemented into the simulator. The WaMPDE can be implemented in Carrot in the future, so the autonomous circuits like the unmodified VCO circuit will be possible to analyze with multiple time dimensions.

Appendix A

Experimental Results

To test the ring VCO performance, the package was mounted on top of a test fixture. This was done by James Dietrich (CMC Testing Collaboratory) in the University of Manitoba. He modified the test fixture as the power pins and ground pins are not compatible between the test fixture and the package. He spent a few days on this modification and this modified circuit is shown in Fig. A.1.

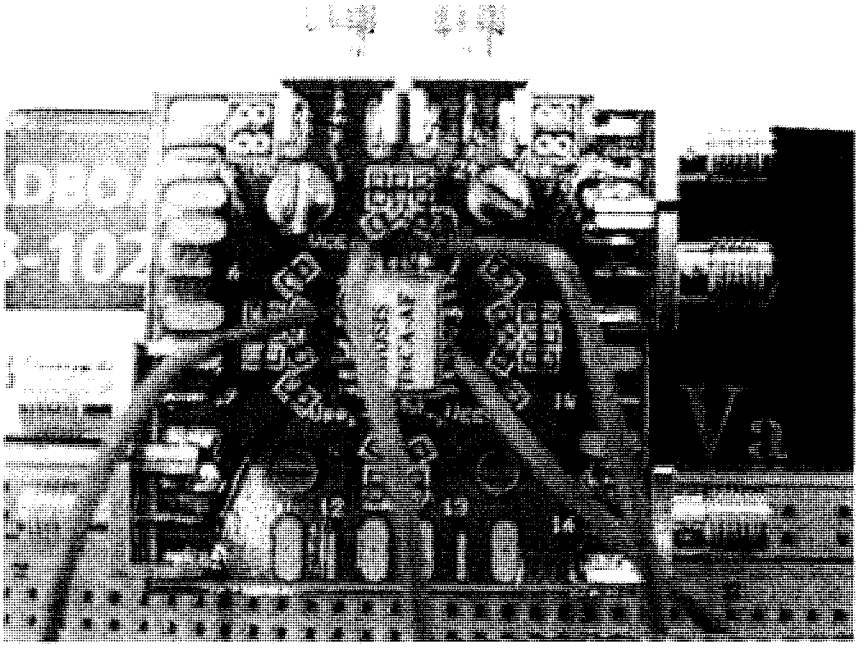

Figure A.1 Modified Tested Circuit

He also did a pre-test for us and the circuit was wired as given in Fig. A.2. We were informed that the chip did not consume any power because the chip and pads are not connected. We tested the circuit shown in Fig. A.2 with multi-meters and power supplies. There was no current flow to the multi-meter. Also, the infinity impedance between ground pins was measured. Thus we can conclude that the pads and circuits are not connected. After re-exam the layout diagram shown in Fig. 4.21, we found out that pads and circuits were not connected and Fig. A.3 shows a portion of this disconnect between pads and circuit. Even though the final design passed the design rule check (DRC) test, the layout versus schematic (LVS) test was not performed. This critical mistake would have been avoided if the pads were built in the schematic.

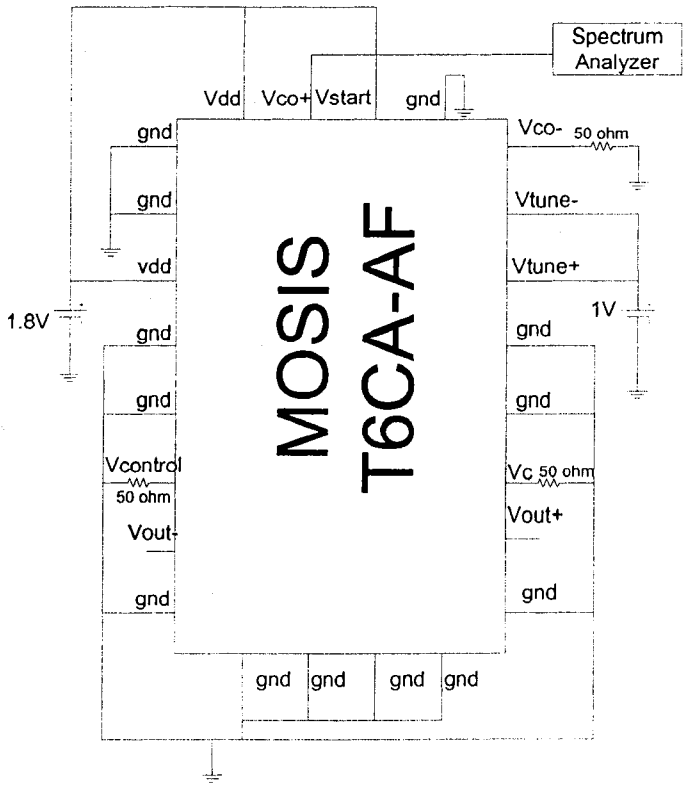

Figure A.2 Test Circuit

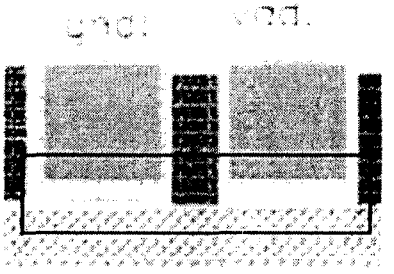

Figure A.3 Disconnections between Pads and Circuits

Appendix B

Netlists include all of the transistor dimensions, the resistor values and a capacitor value used in the new closed-loop and open-loop ring VCO design.

```
// Close loop ring VCO design in Carrot simulator
// Model definitions

.model mosfetl3:mypmos type=1 tox=80e-10 ld=0.09e-6 nsubp=4e22 cj=0.2e3
cjsw=1.2e-9 cgso=0.35e-9 cgdo=0.35e-9 cgbo=1e-10 xj=1.8e-7 nfs=1e14
u0p=0.015 vmax=1e5 vt0p=-0.8 vtc=1 w=20e-6 l=0.4e-6 ad=1.8e-12
as=1.8e12 pd=40.18e-6 ps=40.18e-6

.model mosfetl3:mynmos tox=80e-10 ld=0.09e-6 nsubn=5e21 cjsw=1.2e-9
cgso=0.35e-9 cgdo=0.35e-9 cgbo=1e-10 xj=1.5e-7 nfs=1e14 u0n=0.045
vmax=1e5 vt0n=0.6 vtc=1 w=45e-6 l=0.4e-6 ad=4.05e-12 as=4.05e-12
pd=90.18e-6 ps=90.18e-6

// The First Delay cell

mosfetl3:m1 1 2 3 3 model=mypmos
mosfetl3:m2 4 2 3 3 model=mypmos
mosfetl3:m3 1 5 6 0 model=mynmos
mosfetl3:m4 4 7 6 0 model=mynmos
mosfetl3:m5 6 8 0 0 model=mynmos w=10e-6 l=0.4e-6 ad=9e-13 as=9e-13
pd=20.18e-6 ps=20.18e-6
mosfetl3:m6 6 9 0 0 model=mynmos w=7.5e-6 l=0.4e-6 ad=6.75e-12
as=6.75e-12 pd=15.18e-6 ps=15.18e-6

// The Second Delay cell

mosfetl3:m7 10 2 3 3 model=mypmos
mosfetl3:m8 11 2 3 3 model=mypmos
mosfetl3:m9 10 1 12 0 model=mynmos
mosfetl3:m10 11 4 12 0 model=mynmos
mosfetl3:m11 12 8 0 0 model=mynmos w=10e-6 l=0.4e-6 ad=9e-13 as=9e-13
pd=20.18e-6 ps=20.18e-6
mosfetl3:m12 12 9 0 0 model=mynmos w=7.5e-6 l=0.4e-6 ad=6.75e-12
as=6.75e-12 pd=15.18e-6 ps=15.18e-6

// The Third Delay cell

mosfetl3:m13 13 2 3 3 model=mypmos
mosfetl3:m14 14 2 3 3 model=mypmos
mosfetl3:m15 13 10 15 0 model=mynmos
mosfetl3:m16 14 11 15 0 model=mynmos
mosfetl3:m17 15 8 0 0 model=mynmos  w=10e-6 l=0.4e-6 ad=9e-13 as=9e-13
pd=20.18e-6 ps=20.18e-6
mosfetl3:m18 15 9 0 0 model=mynmos  w=7.5e-6 l=0.4e-6 ad=6.75e-12
as=6.75e-12 pd=15.18e-6 ps=15.18e-6
```

```
// The Fourth Delay cell

mosfetl3:m19 7 2 3 3 model=mypmos
mosfetl3:m20 5 2 3 3 model=mypmos
mosfetl3:m21 7 13 16 0 model=mynmos
mosfetl3:m22 5 14 16 0 model=mynmos
mosfetl3:m23 16 8 0 0 model=mynmos  w=10e-6 l=0.4e-6 ad=9e-13 as=9e-13
pd=20.18e-6 ps=20.18e-6
mosfetl3:m24 16 9 0 0 model=mynmos  w=7.5e-6 l=0.4e-6 ad=6.75e-12
as=6.75e-12 pd=15.18e-6 ps=15.18e-6

// Coarse Tuning

mosfetl3:m25 8 8 0 0 model=mynmos w=10e-6 l=0.4e-6 ad=9e-13 as=9e-13
pd=10.18e-6 ps=10.18e-6
res:r1 3 8 r=400

// Fine Tuning

mosfetl3:m26 17 0 3 3 model=mypmos w=1e-6 l=0.4e-6 ad=9e-14 as=9e-14
pd=2.18e-6 ps=2.18e-6
mosfetl3:m27 9 18 17 3 model=mypmos w=1e-6 l=0.4e-6 ad=9e-14 as=9e-14
pd=2.18e-6 ps=2.18e-6
mosfetl3:m28 0 20 17 3 model=mypmos w=1e-6 l=0.4e-6 ad=9e-14 as=9e-14
pd=2.18e-6 ps=2.18e-6
mosfetl3:m29 9 9 0 0 model=mynmos w=1e-6 l=0.4e-6 ad=9e-14 as=9e-14
pd=2.18e-6 ps=2.18e-6

// Replica Biasing

mosfetl3:m30 21 2 3 3 model=mypmos
mosfetl3:m31 21 3 22 0 model=mynmos
mosfetl3:m32 22 8 0 0 model=mynmos w=10e-6 l=0.4e-6 ad=9e-13 as=9e-13
pd=20.18e-6 ps=20.18e-6
mosfetl3:m33 22 9 0 0 model=mynmos w=7.5e-6 l=0.4e-6 ad=6.75e-12
as=6.75e-12 pd=15.18e-6 ps=15.18e-6

//Opamp

mosfetl3:m34 23 23 3 3 model=mypmos w=8e-6 l=1e-6 ad=7.2e-13 as=7.2e-13
pd=16.18e-6 ps=16.18e-6
mosfetl3:m35 24 23 3 3 model=mypmos w=8e-6 l=1e-6 ad=7.2e-13 as=7.2e-13
pd=16.18e-6 ps=16.18e-6
mosfetl3:m36 23 25 26 0 model=mynmos w=8e-6 l=1.5e-6 ad=7.2e-13
as=7.2e-13 pd=16.18e-6 ps=16.18e-6
mosfetl3:m37 24 21 26 0 model=mynmos w=8e-6 l=1.5e-6 ad=7.2e-13
as=7.2e-13 pd=16.18e-6 ps=16.18e-6
mosfetl3:m38 26 27 0 0 model=mynmos w=6e-6 l=1e-6 ad=5.4e-13 as=5.4e-13
pd=12.18e-6 ps=12.18e-6
mosfetl3:m39 2 27 0 0 model=mynmos w=6e-6 l=1e-6 ad=5.4e-13 as=5.4e-13
pd=12.18e-6 ps=12.18e-6
mosfetl3:m40 2 24 3 3 model=mypmos w=16e-6 l=1e-6 ad=1.44e-12 as=1.44e-
12 pd=32.18e-6 ps=32.18e-6
mosfetl3:m41 27 27 0 0 model=mynmos w=6e-6 l=1e-6 ad=5.4e-13 as=5.4e-13
pd=12.18e-6 ps=12.18e-6
cap: cc 24 2 c=500e-12
```

```
// Opamp Bias

res:r2 3 27 r=24e3
mosfetl3:m42 27 27 0 0 model=mynmos w=20e-6 l=1e-6 ad=1.8e-12 as=1.8e-
12 pd=40.18e-6 ps=40.18e-6

// Reference Voltage

res:r3 3 25 r=800
mosfetl3:m43 25 25 0 0 model=mynmos w=4e-6 l=0.4e-6 ad=3.6e-13 as=3.6e-
13 pd=8.18e-6 ps=8.18e-6

// Buffer

mosfetl3:m44 28 7 30 0 model=mynmos w=5e-6 l=0.4e-6 ad=4.5e-13 as=4.5e-
13 pd=10.18e-6 ps=10.18e-6
mosfetl3:m45 29 5 30 0 model=mynmos w=5e-6 l=0.4e-6 ad=4.5e-13 as=4.5e-
13 pd=10.18e-6 ps=10.18e-6
mosfetl3:m46 30 31 0 0 model=mynmos w=15e-6 l=0.4e-6 ad=1.35e-12
as=1.35e-12 pd=30.18e-6 ps=30.18e-6
mosfetl3:m47 31 31 0 0 model=mynmos w=15e-6 l=0.4e-6 ad=1.35e-12
as=1.35e-12 pd=30.18e-6 ps=30.18e-6

res:r4 3 28 r=2300
res:r5 3 29 r=2300
res:r6 3 31 r=1000

vdc:vdd 3 0 val=1.8
vdc:vtune_n 18 19 val= -0.1
vdc:vtune_p 20 19 val= 0.1
vdc:vtune_cm 19 0 val=0.85


// transient analysis

.analysis tran tstep=20e-12 tstop=2e-7 im=0
.options tol=1e-10 scale=1e3
.end
```

Figure B.1 The netlist for the closed-loop ring VCO in Carrot simulator

```
* Close loop ring VCO design in ngspice simulator
* Model definitions

.model mypmos pmos level=3 tox=80e-10 ld=0.09e-6 nsub=4e16 cj=0.2e-3
+ cjsw=1.2e-9 cgso=0.35e-9 cgdo=0.35e-9 cgbo=1e-10 xj=1.8e-7 nfs=1e14
+ u0=150 vmax=1e5 vt0=-0.8

.model mynmos nmos level=3 tox=80e-10 ld=0.09e-6 nsub=5e15 cjsw=1.2e-9
+ cgso=0.35e-9 cgdo=0.35e-9 cgbo=1e-10 xj=1.5e-7 nfs=1e14 u0=450
+ vmax=1e5 vt0=0.6

* The First Delay cell

m1 1 2 3 3 mypmos w=20e-6 l=0.4e-6 ad=1.8e-12 as=1.8e-12 pd=40.18e-6
ps=40.18e-6
m2 4 2 3 3 mypmos w=20e-6 l=0.4e-6 ad=1.8e-12 as=1.8e-12 pd=40.18e-6
ps=40.18e-6
m3 1 5 6 0 mynmos w=45e-6 l=0.4e-6 ad=4.05e-12 as=4.05e-12 pd=90.18e-6
ps=90.18e-6
m4 4 7 6 0 mynmos w=45e-6 l=0.4e-6 ad=4.05e-12 as=4.05e-12 pd=90.18e-6
ps=90.18e-6
m5 6 8 0 0 mynmos w=10e-6 l=0.4e-6 ad=9e-13 as=9e-13 pd=20.18e-6
ps=20.18e-6
m6 6 9 0 0 mynmos w=7.5e-6 l=0.4e-6 ad=6.75e-12 as=6.75e-12 pd=15.18e-6
ps=15.18e-6

* The Second Delay cell

m7 10 2 3 3 mypmos w=20e-6 l=0.4e-6 ad=1.8e-12 as=1.8e-12 pd=40.18e-6
ps=40.18e-6
m8 11 2 3 3 mypmos w=20e-6 l=0.4e-6 ad=1.8e-12 as=1.8e-12 pd=40.18e-6
ps=40.18e-6
m9 10 1 12 0 mynmos w=45e-6 l=0.4e-6 ad=4.05e-12 as=4.05e-12 pd=90.18e-
6 ps=90.18e-6
m10 11 4 12 0 mynmos w=45e-6 l=0.4e-6 ad=4.05e-12 as=4.05e-12
pd=90.18e-6 ps=90.18e-6
m11 12 8 0 0 mynmos w=10e-6 l=0.4e-6 ad=9e-13 as=9e-13 pd=20.18e-6
ps=20.18e-6
m12 12 9 0 0 mynmos w=7.5e-6 l=0.4e-6 ad=6.75e-12 as=6.75e-12
pd=15.18e-6 ps=15.18e-6

* The Third Delay cell

m13 13 2 3 3 mypmos w=20e-6 l=0.4e-6 ad=1.8e-12 as=1.8e-12 pd=40.18e-6
ps=40.18e-6
m14 14 2 3 3 mypmos w=20e-6 l=0.4e-6 ad=1.8e-12 as=1.8e-12 pd=40.18e-6
ps=40.18e-6
m15 13 10 15 0 mynmos w=45e-6 l=0.4e-6 ad=4.05e-12 as=4.05e-12
pd=90.18e-6 ps=90.18e-6
m16 14 11 15 0 mynmos w=45e-6 l=0.4e-6 ad=4.05e-12 as=4.05e-12
pd=90.18e-6 ps=90.18e-6
m17 15 8 0 0 mynmos w=10e-6 l=0.4e-6 ad=9e-13 as=9e-13 pd=20.18e-6
ps=20.18e-6
m18 15 9 0 0 mynmos w=7.5e-6 l=0.4e-6 ad=6.75e-12 as=6.75e-12
pd=15.18e-6 ps=15.18e-6
```

```
* The Fourth Delay cell

m19 7 2 3 3 mypmos w=20e-6 l=0.4e-6 ad=1.8e-12 as=1.8e-12 pd=40.18e-6
ps=40.18e-6
m20 5 2 3 3 mypmos w=20e-6 l=0.4e-6 ad=1.8e-12 as=1.8e-12 pd=40.18e-6
ps=40.18e-6
m21 7 13 16 0 mynmos w=45e-6 l=0.4e-6 ad=4.05e-12 as=4.05e-12
pd=90.18e-6 ps=90.18e-6
m22 5 14 16 0 mynmos w=45e-6 l=0.4e-6 ad=4.05e-12 as=4.05e-12
pd=90.18e-6 ps=90.18e-6
m23 16 8 0 0 mynmos w=10e-6 l=0.4e-6 ad=9e-13 as=9e-13 pd=20.18e-6
ps=20.18e-6
m24 16 9 0 0 mynmos w=7.5e-6 l=0.4e-6 ad=6.75e-12 as=6.75e-12
pd=15.18e-6 ps=15.18e-6

* Coarse Tuning

m25 8 8 0 0 mynmos w=10e-6 l=0.4e-6 ad=9e-13 as=9e-13 pd=10.18e-6
ps=10.18e-6
R1 3 8 400

* Fine Tuning

m26 17 0 3 3 mypmos w=1e-6 l=0.4e-6 ad=9e-14 as=9e-14 pd=2.18e-6
ps=2.18e-6
m27 9 18 17 3 mypmos w=1e-6 l=0.4e-6 ad=9e-14 as=9e-14 pd=2.18e-6
ps=2.18e-6
m28 0 20 17 3 mypmos w=1e-6 l=0.4e-6 ad=9e-14 as=9e-14 pd=2.18e-6
ps=2.18e-6
m29 9 9 0 0 mynmos w=1e-6 l=0.4e-6 ad=9e-14 as=9e-14 pd=2.18e-6
ps=2.18e-6

* Replica Biasing

m30 21 2 3 3 mypmos w=20e-6 l=0.4e-6 ad=1.8e-12 as=1.8e-12 pd=40.18e-6
ps=40.18e-6
m31 21 3 22 0 mynmos w=45e-6 l=0.4e-6 ad=4.05e-12 as=4.05e-12
pd=90.18e-6 ps=90.18e-6
m32 22 8 0 0 mynmos w=10e-6 l=0.4e-6 ad=9e-13 as=9e-13 pd=20.18e-6
ps=20.18e-6
m33 22 9 0 0 mynmos w=7.5e-6 l=0.4e-6 ad=6.75e-12 as=6.75e-12
pd=15.18e-6 ps=15.18e-6

* Opamp

m34 23 23 3 3 mypmos w=8e-6 l=1e-6 ad=7.2e-13 as=7.2e-13 pd=16.18e-6
ps=16.18e-6
m35 24 23 3 3 mypmos w=8e-6 l=1e-6 ad=7.2e-13 as=7.2e-13 pd=16.18e-6
ps=16.18e-6
m36 23 25 26 0 mynmos w=8e-6 l=1.5e-6 ad=7.2e-13 as=7.2e-13 pd=16.18e-6
ps=16.18e-6
m37 24 21 26 0 mynmos w=8e-6 l=1.5e-6 ad=7.2e-13 as=7.2e-13 pd=16.18e-6
ps=16.18e-6
m38 26 27 0 0 mynmos w=6e-6 l=1e-6 ad=5.4e-13 as=5.4e-13 pd=12.18e-6
ps=12.18e-6
m39 2 27 0 0 mynmos w=6e-6 l=1e-6 ad=5.4e-13 as=5.4e-13 pd=12.18e-6
ps=12.18e-6
```

```
m40 2 24 3 3 mypmos w=16e-6 l=1e-6 ad=1.44e-12 as=1.44e-12 pd=32.18e-6
ps=32.18e-6
m41 27 27 0 0 mynmos w=6e-6 l=1e-6 ad=5.4e-13 as=5.4e-13 pd=12.18e-6
ps=12.18e-6
cc 24 2 500e-12

* Opamp Bias

R2 3 27 24e3
m42 27 27 0 0 mynmos w=20e-6 l=1e-6 ad=1.8e-12 as=1.8e-12 pd=40.18e-6
ps=40.18e-6

* Reference Voltage

R3 3 25 800
m43 25 25 0 0 mynmos w=4e-6 l=0.4e-6 ad=3.6e-13 as=3.6e-13 pd=8.18e-6
ps=8.18e-6

* Buffer

m44 28 7 30 0 mynmos w=5e-6 l=0.4e-6 ad=4.5e-13 as=4.5e-13 pd=10.18e-6
ps=10.18e-6
m45 29 5 30 0 mynmos w=5e-6 l=0.4e-6 ad=4.5e-13 as=4.5e-13 pd=10.18e-6
ps=10.18e-6
m46 30 31 0 0 mynmos w=15e-6 l=0.4e-6 ad=1.35e-12 as=1.35e-12
pd=30.18e-6 ps=30.18e-6
m47 31 31 0 0 mynmos w=15e-6 l=0.4e-6 ad=1.35e-12 as=1.35e-12
pd=30.18e-6 ps=30.18e-6

R4 3 28 2300
R5 3 29 2300
R6 3 31 1000

vdd 3 0 DC 1.8
vtune_n 18 19 DC -0.1
vtune_p 20 19 DC 0.1
vtune_cm 19 0 DC 0.85

* transient analysis

.tran 20e-12 4e-7 0 20e-12
.end
```

Figure B.2 The netlist for the closed-loop ring VCO in ngspice simulator

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