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DESIGN AND MODELING OF A CMOS VCO USING WAVE DIGITAL FILTERS

By

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Abstract

WEIBO LI. Design and Modeling of A CMOS VCO Using Wave Digital Filters (Under the Supervision of Dr. Carlos E. Christoffersen).

Wave digital filters (WDFs) transform an analog network into a topologically equivalent digital structure. A natural application of WDF is the simulation of electric circuits since measurements of any desired node voltages and branch currents are available during all time-steps in WDF structures. WDF structures tend to preserve most of the good properties of their analog counterpart.

In this work, WDF techniques applied to transient simulation are studied. After a review of the basic theory of WDFs and the treatment of nonlinear elements in WDFs, WDF simulations for different circuits, including a simple RC circuit, an anharmonic oscillator and a CMOS LC voltage controlled oscillator (VCO), are presented. Special detail is put on the design and modeling of the LC VCO. The LC VCO was designed and fabricated using the TSMC (Taiwan Semiconductor Manufacturing Co., LTD) CMOS 0.18um technology. The linear frequency tuning range of the LC VCO is from 2.526 GHz to 3.015 GHz for control voltages from 0 to 1 V with a 1.712 mA tail current. WDF simulation results are compared with the exact solution if possible or otherwise with the results obtained with other simulation methods. The comparison shows that WDF techniques are efficient for the simulations of linear circuits and circuits with one nonlinear element. The potential of WDF for the simulation of large networks with many nonlinear elements is also discussed in this thesis.

Acknowledgments

I have had the privilege of learning form Dr. Carlos E. Christoffersen during my graduate studies at Lakehead University. I would like to express my deep appreciation to his generous support, patient guidance and gentle encouragement. It was my great pleasure to study in his research group.

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WeiBo Li

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Contents

List of Acronyms

VCO	Voltage Controlled Oscillator
WDF	Wave Digital Filter
TSMC	Taiwan Semiconductor Manufacturing Co., LTD
KVL	Kirchhoff's Voltage Law
KCL	Kirchhoff's Current Law
DRC	Design Rule Check
LVS	Layout vs. Schematic

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List of Symbols

A_i - Incident wave in z domain

B_i - Reflected wave in z domain

a_i - Incident wave in time domain

b_i - Reflected wave in time domain

$\underline{S}$ - Scattering Matrix

L_s - Overall inductance of spiral inductor

R_s - Conductor loss of spiral inductor

R_p -Substrate loss of spiral inductor

C_s - Overall capacitance of spiral inductor

C_v - Capacitance of NMOS varactor

$C_{gd,n}$ - The gate-drain capacitance of NMOS transistors

$C_{gs,n}$ - The gate-source capacitance of NMOS transistors

$C_{db,p}$ - The drain-bulk capacitance of PMOS transistors

T - Time step

α - Coefficient of parallel adaptors

β - Coefficient of Series adaptors

t_j - Discrete time

Vc - Voltage turns on and off the LC VCO

V_c - Capacitor voltage

Chapter 1

Introduction

1.1 Motivation and Objectives of This Study

Simulation is a well-known technique to study complex systems. A digital signal processing methodology known as wave digital filters (WDFs) transforms an analog network into a topologically equivalent digital structure. WDFs are a natural implementation for the simulation of electric circuits. Measurements of any desired node voltages and branch currents are available during all time-steps, due to the topological relationship between the original circuit and the WDF. WDFs are well known for possessing many desirable properties over other digital filter implementations. In fact, WDF structures tend to preserve most of the good properties of their analog counterpart. For example, passivity and losslessness of analog circuits are preserved by their wave digital implementation. Furthermore, the behavior of WDFs is less sensitive to the quantization of the coefficients; therefore, WDFs exhibit modest accuracy requirements without giving up good dynamic range performance. In some situations, WDF principles can also be successfully used for modeling circuits in which a nonlinear circuit element is present under mild conditions on its characteristic. In addition, they show advantages compared with other simulation methods such as fast algorithm and simple models of electric components.

Most of the simulation methods based on the WDF principles can only solve the specific circuits or networks with only one nonlinear element. It would be of great interest to find a more efficient simulation method for large networks with more than one nonlinear element. The WDF principles show the potential to solve this problem. In addition, they also show the potential for parallel processing.

In this thesis, the goal is to study transient simulation of electric circuits based on

the WDF principles. The wave digital technique applied to circuit simulation is first reviewed. Next, some simulations in the literature are reproduced based on wave digital technique and compared with the original results in the literature and the results from other simulation methods. A CMOS LC voltage controlled oscillator (VCO) is designed and WDF principles are applied for modeling and simulating this circuit. Lastly, the simulation results are compared to see if the results are close enough.

1.2 Thesis Overview

The thesis is composed of five chapters. A review of the basic principles of WDFs and the transient simulation methods based on wave digital technique is presented in Chapter 2. Chapter 3 shows the design procedure and the simulation results of LC VCO. In Chapter 4, the simulations based on wave digital technique for different circuits, including the LC VCO of Chapter 3, are shown. The simulation results are discussed and compared with the exact solution or the results from other simulation methods. In the last chapter we summarize the conclusion and propose the direction of future work.

Chapter 2

Literature Review

2.1 Introduction

WDFs transform analogue network components into digital form using scattering wave variables. They were developed initially by Alfred Fettweis in the late 1960s for digitizing lumped electrical circuits composed of inductors, capacitors, resistors, transformers, gyrators and other elements of classical networks. WDFs can be considered as digital models of their continuous-time reference network. The discretization is performed by the well-known bilinear transformation and the forward and backward traveling wave quantities which are used to replace voltage and current variables.

WDFs offer a set of advantages, like coefficient accuracy, dynamic range, stability under finite-arithmetic conditions and the structure preserving implementation of the reference network.

The basic principle involved in deriving digital filters from a classical analogue network is to represent the lumped or distributed component by wave variables instead of the customary voltage and current [1, 2]. It can be divided into three steps:

- Taking each lumped component and transforming the voltage-current relationship into an incident-reflected wave relationship.
- Applying the bilinear transformation to yield a simple digital building block with one input and one output.
- Interconnecting the building blocks by using a circuit called an adaptor which is a representation of Kirchhoff's laws at a junction.

In this chapter, we first review the basic theory and concept of the WDFs, such as scattering transformation, bilinear transform, linear building blocks and adaptors.

Secondly we review the treatment of nonlinear elements in WDF. Nonlinear elements include nonlinear resistors, nonlinear capacitors and nonlinear inductors.

2.2 Scattering Transformation

In order to apply the bilinear transformation, it is necessary to transform voltages and currents into waves. If V denotes the voltage and I the current at a port, the waves traveling in the forward and the backward directions are defined by the following relationships [1, 2],

$$\begin{cases} A = V + RI \\ B = V - RI \end{cases} \tag{2.1}$$

where A is the incident wave, B is the reflected wave and R is a constant which has the dimensions of resistance and so will be called the port resistance.

For impedance Z, substituting $V = IZ$ for V in Equation (2.1), the following equations are obtained,

$$\left.\begin{cases} A = IZ + RI \\ B = IZ - RI \end{cases}\right\} \Rightarrow S = \frac{B}{A} = \frac{Z - R}{Z + R} \tag{2.2}$$

This is the reflection coefficient, S for the impedance Z. Equation (2.2) can be rewritten as $B = SA$. A as input, B as output and S as the transfer function which depends on impedance Z and port resistance R only.

Signal parameters A and B are chosen as linear combination of V and I. Equation (2.1) also can be expressed as follows,

$$\begin{cases} V = \frac{A + B}{2} \\ I = \frac{A - B}{2R} \end{cases} \tag{2.3}$$

2.3 Bilinear Transformation

WDFs are based on the application of bilinear transformation which is a particular type of spectral mapping between the analog frequency variable s and discrete frequency variable z [1, 3]. The bilinear transformation is a first-order approximation of the natural logarithm function that is an exact mapping of the z-plane to the s plane.

When the Laplace transform is performed on a discrete-time signal, the result is precisely the Z transform of the discrete-time sequence with the substitution of

$$z = e^{sT} = \frac{e^{\frac{sT}{2}}}{e^{-\frac{sT}{2}}}$$

$$\text{since } e^{x} = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \cdots$$

$$\text{therefore, } z \approx \frac{1 + \frac{sT}{2}}{1 - \frac{sT}{2}}$$

$$\text{and } s \approx \frac{2}{T}\frac{1 - z^{-1}}{1 + z^{-1}} \tag{2.4}$$

T is sampling time, z^{-1} is interpreted as a unit delay of duration T. The mapping affects only reactive ports whose behavior is frequency-dependent, such as inductor and capacitor. Memoryless elements, such as transformer, gyrator and resistor which are frequency-independent, will not be affected by such a transformation.

It is important to mention that the time-domain interpretation of the bilinear mapping is called the trapezoidal rule for numerical integration. The bilinear transformation takes the left-half plane in s to the inside of unit circle in z, and the right-half plane in s to the outside the unit circle in z [27]. This is shown in Fig. 2.1. This implies that stable, causal transfer function in s will be mapped to stable and causal transfer function in the discrete variable z. In some sense, the mapping preserves passivity or energetic properties of the original system.

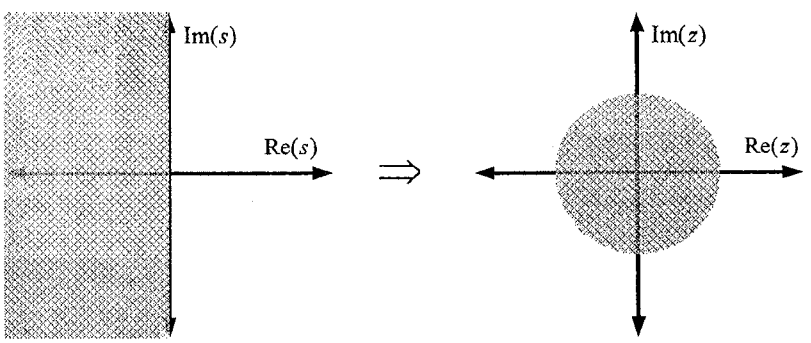

Figure 2.1: Spectral mapping corresponding to the Trapezoidal rule

The Trapezoidal rule for numerical integration meets the requirements of a fast solution within an acceptable precision. It presents very good characteristics in terms of low distortion and numerical stability, being A-stable [5]. Those reasons explain its choice as the basic integration rule for most general purpose simulation programs, where a great number of possible network conditions must be satisfied.

2.4 Linear Building Blocks

All linear elements used in classical passive analogue circuits (resistances capacitances, inductances, gyrators, ideal transformers and unit elements) and resistive sources can be digitally simulated by obeying the scattering and bilinear transformations [2, 4]. As examples, we consider only a capacitance, an inductance and a resistance.

2.4.1 Inductors

Consider an inductor, for which the voltage-current relationship is shown below,

$$V = (sL)I \tag{2.5}$$

Applying the bilinear transformation Equations (2.4) to (2.5), we get

$$Z(s) = Ls = \frac{2L}{T}\frac{1-z^{-1}}{1+z^{-1}} \tag{2.6}$$

Substituting Equation (2.6) into (2.2), the following is obtained,

$$\frac{B}{A} = \frac{\frac{2L}{T}\frac{1-z^{-1}}{1+z^{-1}} - R}{\frac{2L}{T}\frac{1-z^{-1}}{1+z^{-1}} + R}$$

By setting port resistance $R = 2L/T$, we get

$$B = -z^{-1}A \tag{2.7}$$

As shown in Equation (2.7), the reflected wave B is equal to the incident wave A multiplying by a minus unit delay z^{-1}. In other words, the reflected wave B is equal to the negative of the previous step value of incident wave A.

The inductors can also be derived by using the trapezoidal rule which is

equivalent to applying the bilinear transformation in continuous time domain.

According to the trapezoidal rule, the inductor current can be expressed as follows,

$$i(t) = i(t-T) + \frac{1}{L}\int_{t-T}^{t} v(\tau)d\tau \tag{2.8}$$

Equation (2.8) is approximated by

$$i(t) = i(t-T) + \frac{T}{2L}[v(t) + v(t-T)] \tag{2.9}$$

According to Equation (2.3), perform the wave variables substitution into Equation (2.9),

$$v(t) = \frac{a(t)+b(t)}{2} \quad , \quad i(t) = \frac{a(t)-b(t)}{2R}$$

where a(t) and b(t) are the incident and the reflected waves in time domain. The result is

$$\frac{a(t)-b(t)}{2R} = \frac{a(t-T)-b(t-T)}{2R} + \frac{T}{2L}\left(\frac{a(t)+b(t)}{2} + \frac{a(t-T)+b(t-T)}{2}\right)$$

Choosing $R = 2L/T$ to obtain the inductor instantaneous wave quantities in the time domain, we obtain:

$$b(t) = -a(t-T) \tag{2.10}$$

Comparing Equation (2.10) with (2.7), both equations are same but in different domain.

2.4.2 Capacitors

For a capacitor, the voltage-current relationship is

$$V = \left(\frac{1}{sC}\right)I \tag{2.11}$$

By applying bilinear transform, we have

$$Z(s) = \frac{1}{sC} = \frac{T}{2C}\frac{1+z^{-1}}{1-z^{-1}} \tag{2.12}$$

Replacing Z From equation (2.2) in Equation (2.12),

$$\frac{B}{A}=\frac{\frac{T}{2C}\frac{1+z^{-1}}{1-z^{-1}}-R}{\frac{T}{2C}\frac{1+z^{-1}}{1-z^{-1}}+R}$$

By setting the port resistance $R=T/2C$, we obtain

$$B=z^{-1}A \tag{2.13}$$

According to the Trapezoidal rule, the capacitor in the continuous time domain is shown below,

$$v(t)=v(t-T)+\frac{1}{C}\int_{t-T}^{t} i(\tau)d\tau \tag{2.14}$$

By using wave quantities to replace voltages and currents, we obtain:

$$\frac{a(t)+b(t)}{2}=\frac{a(t-T)+b(t-T)}{2}+\frac{T}{2C}\left(\frac{a(t)-b(t)}{2R}+\frac{a(t-T)-b(t-T)}{2R}\right)$$

By setting $R=T/2C$, the above equation becomes

$$b(t)=a(t-T), \tag{2.15}$$

which is the same as Equation (2.13).

2.4.3 Resistors

From the voltage-current characteristic of a resistance R_1, $V=R_1I$, the equation (2.1) becomes

$$B=\frac{R_1-R}{R_1+R}A \tag{2.16}$$

If the port resistance R is chosen equal to the element value R_1, we obtain

$$B=0$$

Fig. 2.2 shows the major elements and their equivalences in the WDF domain.

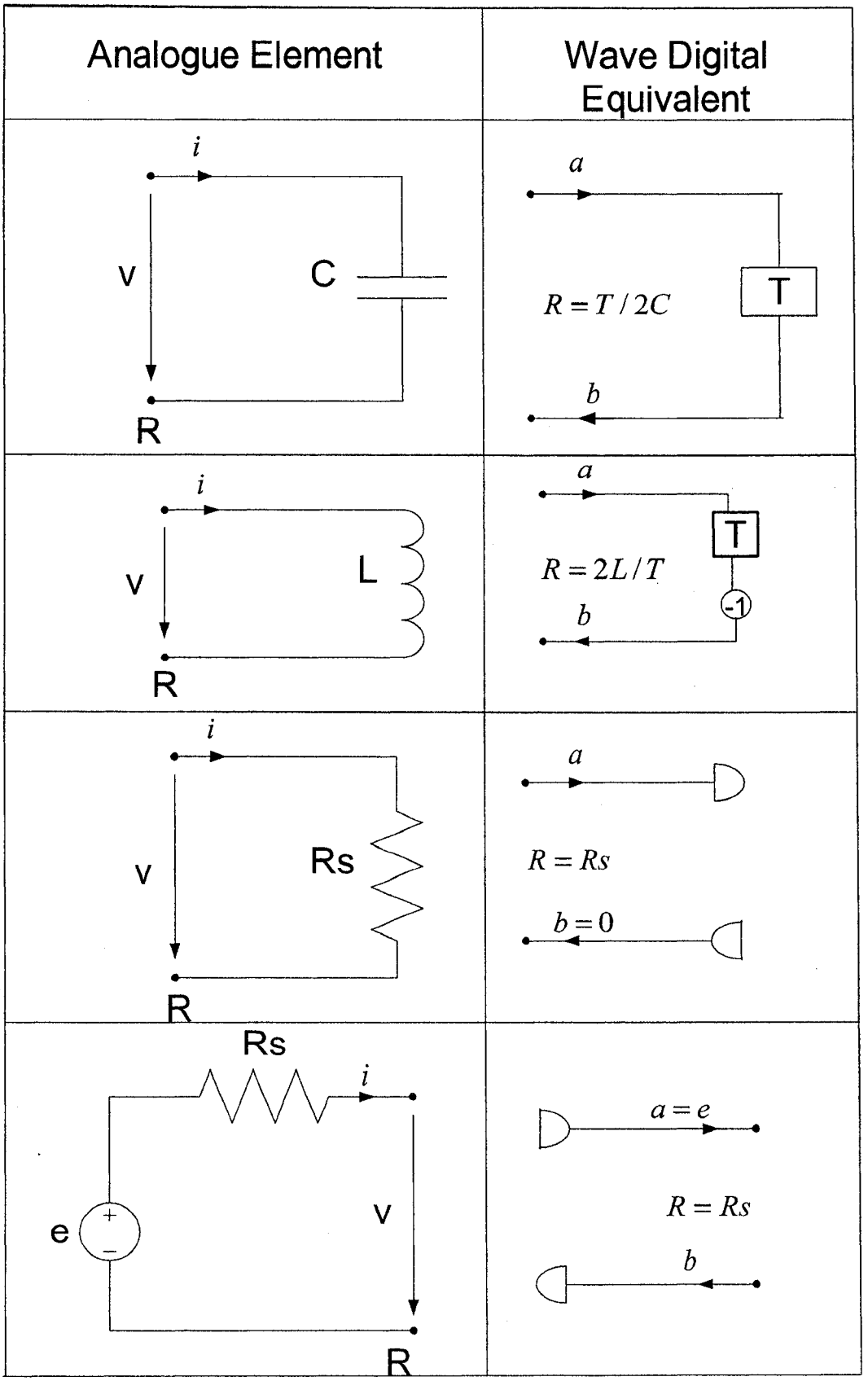

Figure2.2: Major elements and their realization in the WDF Domain.

2.5 Interconnections and Adaptors

In order to fully establish equivalence with a classical circuit, the interconnections (Kirchhoff's laws) should be simulated. Interconnection is achieved by the use of adaptors which are digital representations of Kirchhoff's laws [1]. The adaptors of WDF are memoryless devices whose task is to perform transformations between pair of wave variables that are referred to different levels of port resistance. The most important of these adaptors are parallel adaptors and series adaptors.

2.5.1 Parallel Adaptors

The following figure shows a parallel connection with n ports and the symbol for parallel adaptor with one reflection-free port.

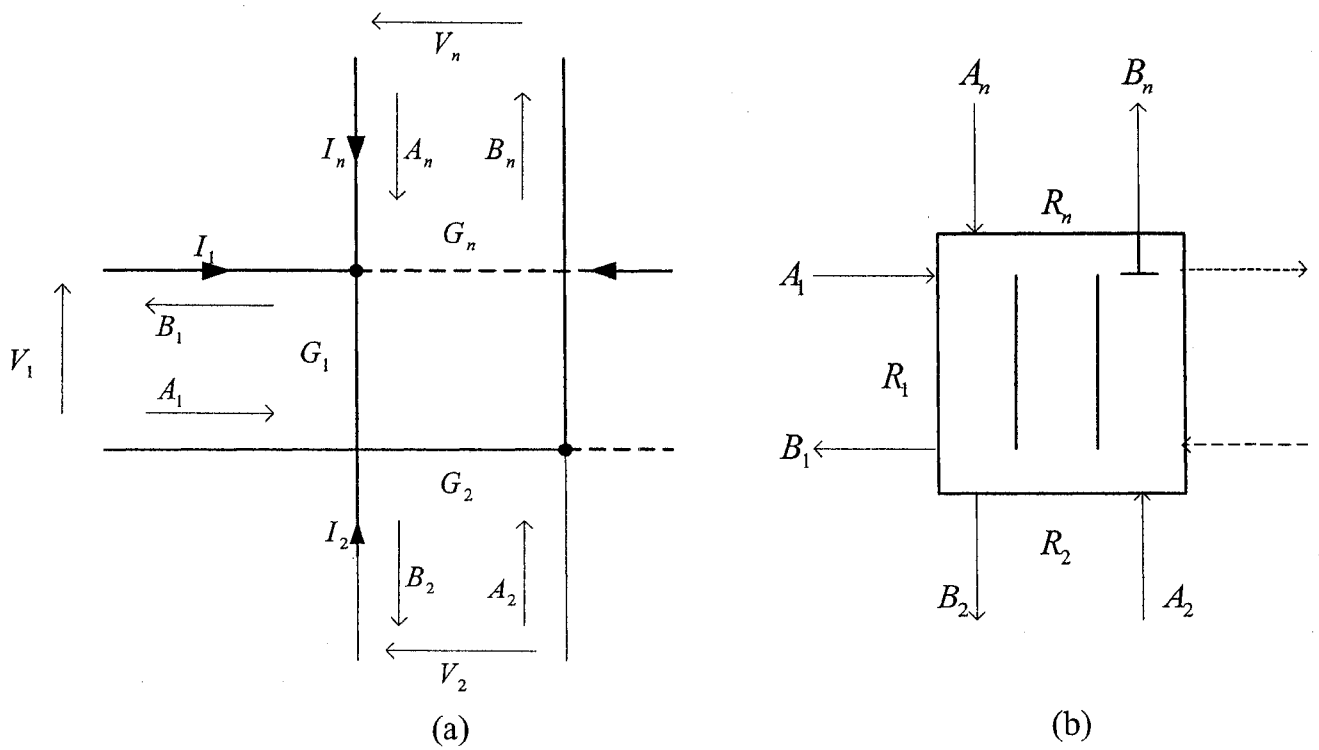

Figure 2.3: (a) Parallel connections of n ports and (b) n-port parallel adaptor whose Port n is reflection-free

The equations of the parallel connection are shown below

$$V_1 = V_2 \cdots\cdots\cdots = V_n$$
$$I_1 + I_2 \cdots\cdots\cdots + I_n = 0$$

The following equations are achieved for the reflected wave B_k in matrix form

$$\begin{bmatrix} B_1 \\ B_2 \\ \vdots \\ B_{n-1} \\ B_n \end{bmatrix} = \begin{bmatrix} (\alpha_1 - 1) & \alpha_2 & \cdots & \alpha_{n-1} & \alpha_n \\ \alpha_1 & (\alpha_2 - 1) & \cdots & \alpha_{n-1} & \alpha_n \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ \alpha_1 & \alpha_2 & \cdots & (\alpha_{n-1} - 1) & \alpha_n \\ \alpha_1 & \alpha_2 & \cdots & \alpha_{n-1} & (\alpha_n - 1) \end{bmatrix} \begin{bmatrix} A_1 \\ A_2 \\ \vdots \\ A_{n-1} \\ A_n \end{bmatrix}$$

$$\alpha_k = \frac{2G_k}{(G_1 + G_2 \cdots\cdots + G_n)} \qquad k = 1, 2, \cdots n. \qquad G_k = 1/R_k$$

Since $\sum_{k=1}^{n} \alpha_k = 2$, the coefficient α_k of one of the ports, called the dependent port, can be eliminated. By choosing port n as the dependent port, the equations become,

$$\begin{bmatrix} B_1 \\ B_2 \\ \vdots \\ B_{n-1} \\ B_n \end{bmatrix} = \begin{bmatrix} (\alpha_1 - 1) & \alpha_2 & \cdots & \alpha_{n-1} & 2 - \sum_{k=1}^{n-1} \alpha_k \\ \alpha_1 & (\alpha_2 - 1) & \cdots & \alpha_{n-1} & 2 - \sum_{k=1}^{n-1} \alpha_k \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ \alpha_1 & \alpha_2 & \cdots & (\alpha_{n-1} - 1) & 2 - \sum_{k=1}^{n-1} \alpha_k \\ \alpha_1 & \alpha_2 & \cdots & \alpha_{n-1} & (1 - \sum_{k=1}^{n-1} \alpha_k) \end{bmatrix} \begin{bmatrix} A_1 \\ A_2 \\ \vdots \\ A_{n-1} \\ A_n \end{bmatrix}$$

If one of the coefficients α_k is equal to one, the corresponding port is reflection-free. If Port n is reflection-free, i.e., $\alpha_n = 1$, the reflected wave at port n is independent of the incident wave at Port n. In this case, Port n is reflection-free and Port n-1 is a dependent port. The following show the equations in matrix form.

$$\begin{bmatrix} B_1 \\ B_2 \\ \vdots \\ B_{n-1} \\ B_n \end{bmatrix} = \begin{bmatrix} (\alpha_1 - 1) & \alpha_2 & \cdots & 1-\sum_{k=1}^{n-2}\alpha_k & 1 \\ \alpha_1 & (\alpha_2 - 1) & \cdots & 1-\sum_{k=1}^{n-2}\alpha_k & 1 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ \alpha_1 & \alpha_2 & \alpha_3 & (-\sum_{k=1}^{n-2}\alpha_k) & 1 \\ \alpha_1 & \alpha_2 & \alpha_3 & 1-\sum_{k=1}^{n-2}\alpha_k & 0 \end{bmatrix} \begin{bmatrix} A_1 \\ A_2 \\ \vdots \\ A_{n-1} \\ A_n \end{bmatrix}$$

2.5.2 Series Adaptors

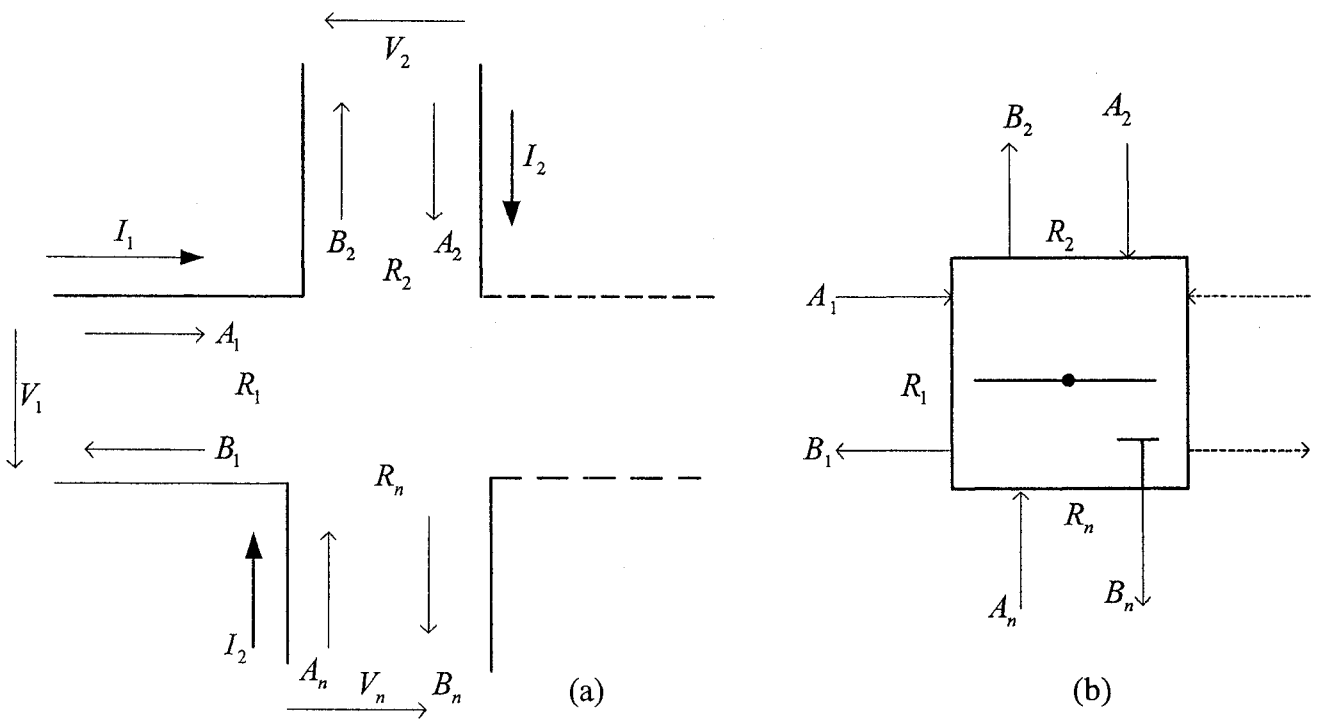

Figure 2.4: (a) Series connection of n ports and (b) n-port series adaptor whose Port n is reflection-free

Figure 2.4 shows the series connection of n ports and the symbol for n-port series adaptor with Port n as reflection-free port.

The equations of the parallel connection are shown below

$$V_1 + V_2 \cdots\cdots + V_n = 0$$
$$I_1 = I_2 \cdots\cdots = I_n$$

The following equations are achieved for the reflected wave B_k in matrix form

$$\begin{bmatrix} B_1 \\ B_2 \\ \vdots \\ B_{n-1} \\ B_n \end{bmatrix} = \begin{bmatrix} (1-\beta_1) & -\beta_1 & \cdots & -\beta_1 & -\beta_1 \\ -\beta_2 & (1-\beta_2) & \cdots & -\beta_2 & -\beta_2 \\ \vdots & -\beta_3 & \ddots & -\beta_3 & -\beta_3 \\ -\beta_{n-1} & -\beta_{n-1} & \cdots & (1-\beta_{n-1}) & -\beta_{n-1} \\ -\beta_n & -\beta_n & \cdots & -\beta_n & (1-\beta_n) \end{bmatrix} \begin{bmatrix} A_1 \\ A_2 \\ \vdots \\ A_{n-1} \\ A_n \end{bmatrix}$$

$$\beta_k = \frac{2R_k}{R_1 + R_2 \cdots + R_n} \qquad k = 1, 2, \ldots n.$$

If Port n is chosen as a dependent port to eliminate the corresponding β_n, since $\sum_{k=1}^{n} \beta_k = 2$, we obtain the following,

$$\begin{bmatrix} B_1 \\ B_2 \\ \vdots \\ B_{n-1} \\ B_n \end{bmatrix} = \begin{bmatrix} (1-\beta_1) & -\beta_1 & \cdots & -\beta_1 & -\beta_1 \\ -\beta_2 & (1-\beta_2) & \cdots & -\beta_2 & -\beta_2 \\ \vdots & \vdots & \ddots & -\beta_3 & -\beta_3 \\ -\beta_{n-1} & -\beta_{n-1} & \cdots & \vdots & \vdots \\ \sum_{k=1}^{n-1}\beta_k - 2 & \sum_{k=1}^{n-1}\beta_k - 2 & \cdots & \sum_{k=1}^{n-1}\beta_k - 2 & \sum_{k=1}^{n-1}\beta_k - 1 \end{bmatrix} \begin{bmatrix} A_1 \\ A_2 \\ \vdots \\ A_{n-1} \\ A_n \end{bmatrix}$$

Setting Port n as reflection-free and Port n-1 as dependent port, the equations are as shown below,

$$\begin{bmatrix} B_1 \\ B_2 \\ \vdots \\ B_{n-1} \\ B_n \end{bmatrix} = \begin{bmatrix} (1-\beta_1) & -\beta_1 & \cdots & -\beta_1 & -\beta_1 \\ -\beta_2 & (1-\beta_2) & \cdots & -\beta_2 & -\beta_2 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ \sum_{k=1}^{n-2}\beta_k - 1 & \sum_{k=1}^{n-2}\beta_k - 1 & \cdots & \sum_{k=1}^{n-2}\beta_k & \sum_{k=1}^{n-2}\beta_k - 1 \\ -1 & -1 & \cdots & -1 & 0 \end{bmatrix} \begin{bmatrix} A_1 \\ A_2 \\ \vdots \\ A_{n-1} \\ A_n \end{bmatrix}$$

The series and parallel adaptors fully establish equivalence between the modeled network and its digital implementation. For this reason, the concept of reflection-free ports is important to assure that a WDF can be realized. The solution of non-linear

and time varying circuits without a reflection-free port would require an iterative numerical method, which is time consuming and inadequate for real-time simulation. Also, the interconnection of two adaptor ports without a reflection-free port would create a delay-free directed loop [3]. This is shown in Fig. 2.5. As we can see from Fig. 2.5, the reflected wave B depends on the instantaneous incident wave A, and the incident wave A also depends on the instantaneous reflected wave B. This creates a delay-free loop that makes the WDF unrealizable. In the delay-free loop, the wave B depends on the unknown wave A which also depends on the unknown wave B. Thus, it is impossible to calculate wave B in one iteration and the WDF becomes unrealizable. When a reflection-free port is introduced, the reflected wave B does not depend on the incident wave A anymore. This makes the WDF realizable.

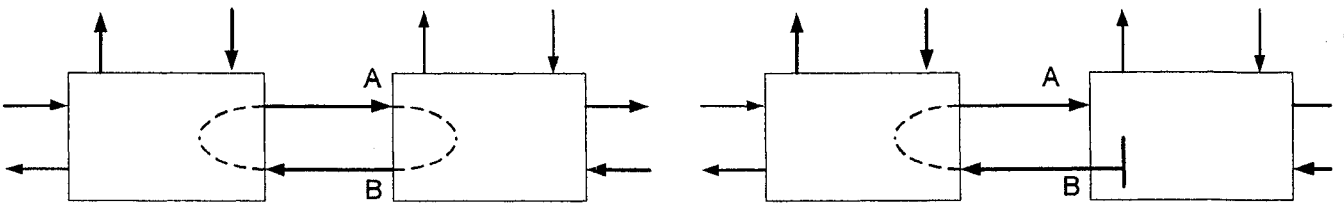

Figure 2.5: Delay-free loop due to direct interconnection of adaptors and its interruption by a reflected-free port

2.5.3 Two-Port Adaptors

The simplest adaptors are those with $n = 2$. They are of particular importance in the design of WDFs [6]. We consider first a parallel connection of two ports with port resistance R_1 and R_2. From the parallel adaptor equations, the following equations are obtained if Port 2 is dependent

$$B_2 = A_2 - \alpha_1 (A_2 - A_1)$$
$$B_1 = B_2 + (A_2 - A_1)$$
$$\alpha_1 = \frac{2R_2}{R_1 + R_2}$$

If Port 1 is chosen as dependent port, we obtain the follows,

$$B_1 = A_1 - \alpha_2(A_1 - A_2)$$
$$B_2 = B_1 + (A_1 - A_2)$$
$$\alpha_2 = \frac{2R_1}{R_1 + R_2}$$

A more symmetrical way of writing the above equations is

$$B_1 = A_2 + \alpha(A_2 - A_1)$$
$$B_2 = A_1 + \alpha(A_2 - A_1) \qquad (2.17)$$

$$\alpha = \frac{(R_1 - R_2)}{(R_1 + R_2)}$$

We also have

$$\alpha = 1 - \alpha_1 = \alpha_2 - 1$$

The symmetrical way introduces the equations of two-port adaptor. The symbol of two-port adaptor is shown in Fig. 2.6(c).

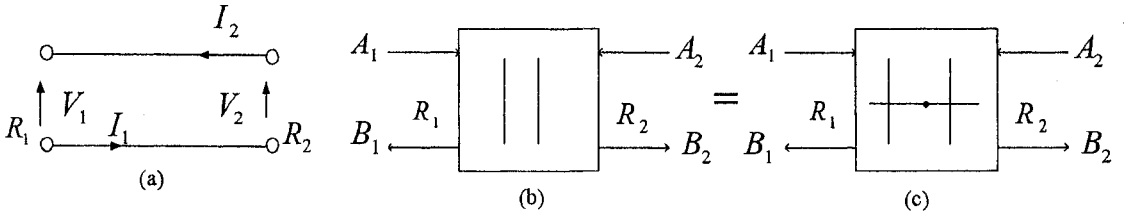

Figure 2.6: (a) Parallel connection of two ports (b) two-port parallel adaptor (c) the corresponding two-port adaptor

As two ports connected in parallel can also be considered to be connected in series, the adaptor is also a series two-port adaptor. One might expect two-port series and two-port parallel adaptors to be the same. This is essentially true, but the orientation of voltage and current at one of the ports, say Port 2, has to be reversed if one passes from the parallel to the series connection. This can be seen from Fig. 2.6(a) and Fig. 2.7(a).

Since the voltage and current are reversed, the corresponding wave quantities signs should be changed. Fig. 2.7(b) and (c) shows the relations between two-port series adaptor and two-port adaptor.

For the two-port series adaptor, the reflection coefficients are given as follows,

$$\beta_1 = \frac{2R_1}{R_1 + R_2}$$

$$\beta_2 = \frac{2R_2}{R_1 + R_2}$$

$$\alpha = \beta_1 - 1 = 1 - \beta_2$$

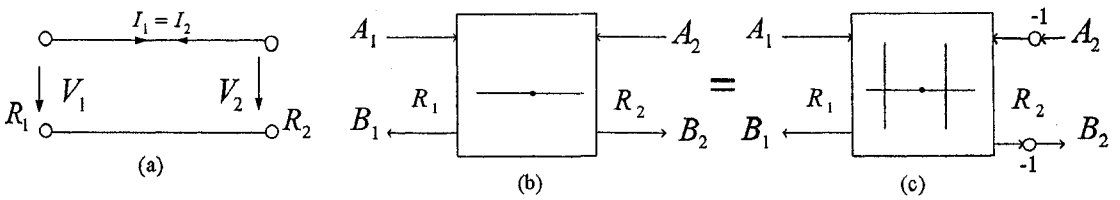

Figure 2.7: (a) Series connection of two ports (b) two-port series adaptor (c) the corresponding two-port adaptor

2.5.4 Derivation of Adaptors

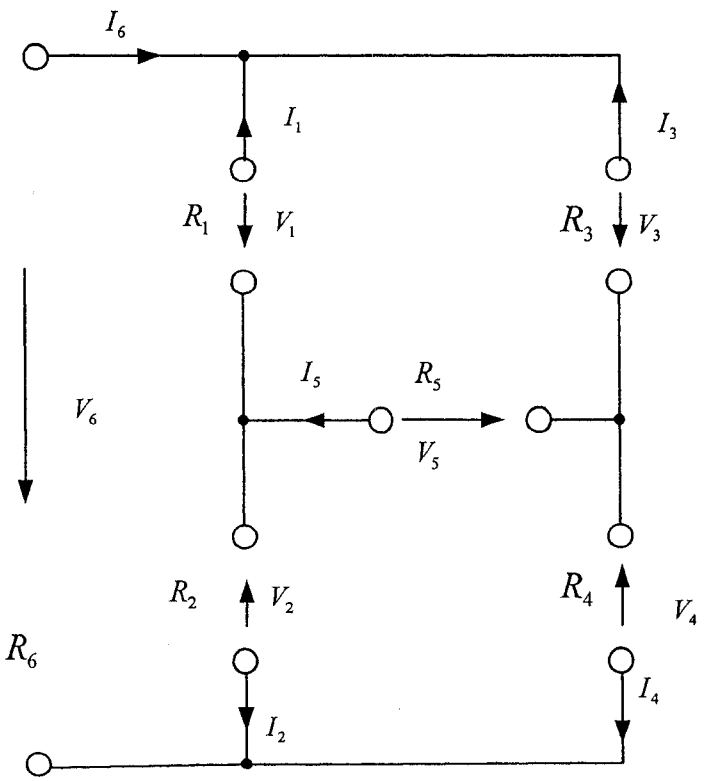

Figure 2.8: Wiring diagram of a bridge structure

Generally adaptors may be derived from Kirchhoff's laws. As an example, the scattering matrix of a lattice adaptor is calculated [7]. Fig. 2.8 depicts the corresponding wiring diagram of a bridge structure. The definitions of the wiring diagram are given

$$\vec{V}=[V_1, \quad \cdots \quad ,V_6]^T$$
$$\vec{I}=[I_1, \quad \cdots \quad ,I_6]^T$$
$$\vec{A}=[A_1, \quad \cdots \quad ,A_6]^T$$
$$\vec{B}=[B_1, \quad \cdots \quad ,B_6]^T$$
$$\underline{G}=diag\left(\frac{1}{R_1}, \quad \cdots \quad ,\frac{1}{R_6}\right)$$

$$\begin{cases} V_1-V_2-V_6=0 \\ V_1-V_3+V_5=0 \\ V_2-V_4+V_5=0 \end{cases}$$

$$\begin{cases} I_1+I_3+I_6=0 \\ I_2+I_4-I_6=0 \\ I_3+I_4+I_5=0 \end{cases}$$

With the above definitions, voltage and current rules from the bridge structure can be written as

$$\underline{M_V}=\begin{bmatrix} 1 & -1 & 0 & 0 & 0 & -1 \\ 1 & 0 & -1 & 0 & 1 & 0 \\ 0 & 1 & 0 & -1 & 1 & 0 \end{bmatrix} \Leftrightarrow \underline{M_V}\vec{V}=\vec{0}$$

$$\underline{M_I}=\begin{bmatrix} 1 & 0 & 1 & 0 & 0 & 1 \\ 0 & 1 & 0 & 1 & 0 & -1 \\ 0 & 0 & 1 & 1 & 1 & 0 \end{bmatrix} \Leftrightarrow \underline{M_I}\vec{I}=\vec{0}$$

In the case of vectors, the equations (2.3) of voltages and currents related to the wave quantities may be written as

$$\vec{V}=\frac{\vec{A}+\vec{B}}{2} \Rightarrow \underline{M_V}\left(\vec{A}+\vec{B}\right)=\vec{0}$$
$$\vec{I}=\underline{G}\frac{\vec{A}-\vec{B}}{2} \Rightarrow \underline{M_I}\,\underline{G}\left(\vec{A}-\vec{B}\right)=\vec{0}$$
$$\Rightarrow \begin{bmatrix} \underline{M_V} \\ \underline{M_I}\,\underline{G} \end{bmatrix}\vec{A}+\begin{bmatrix} \underline{M_V} \\ -\underline{M_I}\,\underline{G} \end{bmatrix}\vec{B}=\vec{0}$$

$$\Rightarrow \vec{B}=\underline{S}\vec{A} \Rightarrow \underline{S}=-\begin{bmatrix} \underline{M_V} \\ -\underline{M_I}\,\underline{G} \end{bmatrix}^{-1}\begin{bmatrix} \underline{M_V} \\ \underline{M_I}\,\underline{G} \end{bmatrix} \qquad (2.18)$$

In the above derivation, Kirchhoff's laws describe an interconnection in the voltage and current domain. These equations are transformed to the scattering matrix $\underline{S}$ that describes the interconnection in the WDF domain by equivalence.

2.5.5 Trees and Kirchhoff's Laws

As we can see from the equation (2.18), the most important part is to obtain the matrices $\underline{M_v}$ and $\underline{M_i}$. It would be a problem to obtain the matrices for a large network. The tree of a graph is one of the most important concepts in graph theory applied to circuit analysis [22]. This concept provides a convenient solution to the problem in a large network. Before introducing the concept, I will review several definitions in graph theory [22].

Graph: A graph Γ is a set of branches $B_r = \{B_{r1}, \ldots, B_{r2}\}$ together with a set of nodes $\{v_1, \ldots, v_n\}$ such that every branch in B_r is incident with two nodes in N.

Subgraph: $\Gamma_1 = (B_{r1}, N_1)$ is a subgraph of $\Gamma = (B_r, N)$ if Γ_1 is a graph, B_{r1} is a subset of B_r and N_1 is a subset of N.

Connected graph: A connected graph is said to be connected when there is at least one path between every pairs of nodes.

Cut set: Given a connected graph Γ, a cut set X is a set of branches $\{b_{r1}, \ldots, b_{rc}\}$ in Γ such that:

- The removal of all braches in X results in a graph that is not connected;
- The removal of all but one branch in X leaves the graph connected.

Loop: Let Γ be a connected graph. A loop Λ is a connected subgraph of Γ in which precisely two branches are incident with each node.

Kirchhoff's Voltage Law (KVL) and Kirchhoff's Current Law (KCL) are based on loops and cut sets respectively. To make those definitions clear, an example is presented. Fig. 2.9 shows a connected graph with 4 nodes and 6 braches. The following cut sets are identified in the graph:

$$X_1 = \{2,3,4\}$$
$$X_2 = \{1,2,5\}$$
$$X_3 = \{1,3,6\}$$
$$X_4 = \{4,5,6\}$$
$$X_5 = \{1,2,4,6\}$$
$$X_6 = \{1,3,4,5\}$$
$$X_7 = \{2,3,5,6\}$$

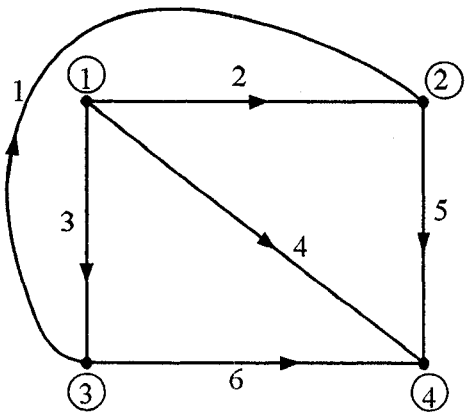

Figure 2.9: A connected graph

If all KCL equations based on cut sets for the graph of Fig. 2.9 are expressed in matrix form, the result is

$$\begin{bmatrix} 0 & 1 & 1 & 1 & 0 & 0 \\ -1 & -1 & 0 & 0 & 1 & 0 \\ 1 & 0 & -1 & 0 & 0 & 1 \\ 0 & 0 & 0 & -1 & -1 & -1 \\ 1 & 1 & 0 & 1 & 0 & 1 \\ 1 & 0 & -1 & -1 & -1 & 0 \\ 0 & 1 & 1 & 0 & -1 & -1 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \\ I_6 \end{bmatrix} = \vec{0} \tag{2.19}$$

or

$$Q_a \vec{I} = \vec{0} \tag{2.20}$$

where Q_a is the full cut-set matrix. In fact, there are always only n-1 linearly independent rows that can be selected in Q_a, where n is the number of nodes in the

graph. Therefore the maximum number of linearly independent rows that can be selected in (2.19) is three.

The loops in the graph of Fig. 2.9 are composed of the following branches:

$$\Lambda_1 : \{1,2,3\}$$
$$\Lambda_2 : \{1,5,6\}$$
$$\Lambda_3 : \{1,2,4,6\}$$
$$\Lambda_4 : \{1,3,4,5\}$$
$$\Lambda_5 : \{2,3,5,6\}$$
$$\Lambda_6 : \{2,4,5\}$$
$$\Lambda_7 : \{3,4,6\}$$

All loop-based KVL equations for the graph of Fig. 2.9 can be grouped in matrix form as

$$\begin{bmatrix} 1 & -1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 1 & -1 \\ 1 & -1 & 0 & 1 & 0 & -1 \\ 1 & 0 & 1 & -1 & 1 & 0 \\ 0 & 1 & -1 & 0 & 1 & -1 \\ 0 & 1 & 0 & -1 & 1 & 0 \\ 0 & 0 & 1 & -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \end{bmatrix} = \vec{0} \tag{2.21}$$

or

$$B_a \vec{V} = \vec{0} \tag{2.22}$$

where B_a is the full loop matrix. There are only $\ell = b-(n-1)$ linearly independent rows in B_a for a graph with n nodes and b branches. Therefore the maximum number of linearly independent rows in (2.21) is three.

The key issue is the selection of cut sets and loops that result in linearly independent rows of Q_a and B_a respectively. The tree of a graph provides the solution to the problems of determining a linearly independent cut set-based KCL equations and loop-based KVL equations. These equations are provided by the unique groups of cut sets and loops that are always associated with a tree.

The theory of the concept, the tree of a graph, is first reviewed.

Tree: Let Γ be a connected graph. A tree T_r is subgraph of Γ such that:

- T_r is connected
- T_r contains all node of Γ
- T_r has no loops

The branches of a connected graph are divided in two groups: those branches that belong to the tree, called tree branches, and those that are not in the tree, called links. The main results that relate trees with cut sets and loops are grouped in the following theorem [23].

Fundamental theorem of graphs: Let Γ be a connected graph with n nodes and b branches and T_r a tree of Γ. Then:

- There is a unique path along the tree between any pair of nodes;
- There are n-1 tree branches and $\ell = b-(n-1)$ links;
- Every tree branch of T_r together with some links defines a unique cut set;
- Every link of T_r and the unique path on the tree between its two nodes defines a unique loop.

The orientation for cut sets is defined by the associated tree branch. Fig. 2.10 is a graph used to illustrate the use of trees to obtain KCL and KVL equations. The tree branches are indicated by thicker lines. The cut sets associated with tree branches and loops associated with links are indicated in this graph. According to the theorem, there will be $n-1=3$ tree branches and $\ell = b-(n-1)=3$ links. KCL equations for the three cut sets in Fig. 2.10 are written as

$$C_1 : I_2 + I_3 + I_4 = 0$$
$$C_2 : -I_1 - I_2 + I_5 = 0$$
$$C_3 : I_1 - I_3 + I_6 = 0$$

or, in matrix form

$$\begin{bmatrix} 0 & 1 & 1 & 1 & 0 & 0 \\ -1 & -1 & 0 & 0 & 1 & 0 \\ 1 & 0 & -1 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \\ I_6 \end{bmatrix} = \vec{0}$$

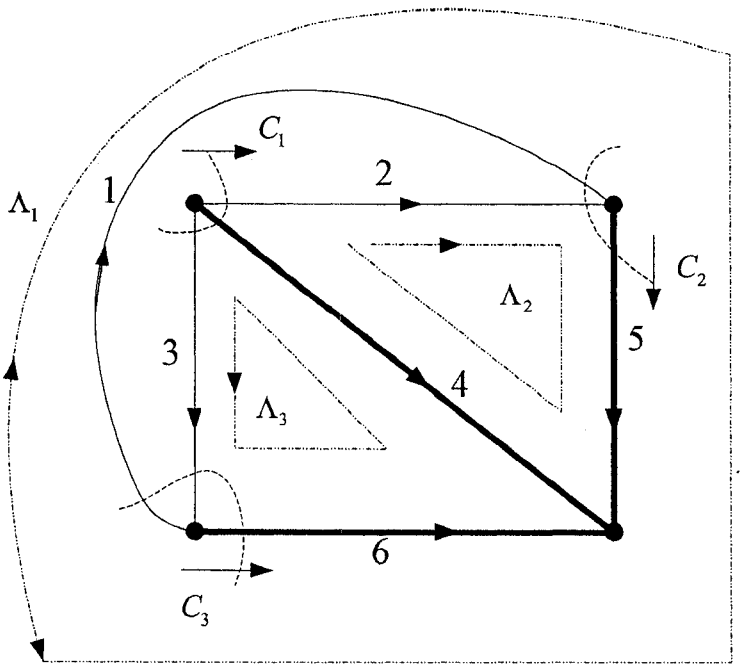

Figure 2.10: Graph used to illustrate the use of trees to obtain KCL and KVL equations.

The orientation for loops is defined by the associated link. The KVL equations derived from the loops are

$$\Lambda_1 : V_1 + V_5 - V_6 = 0$$
$$\Lambda_2 : V_2 - V_4 + V_5 = 0$$
$$\Lambda_3 : V_3 - V_4 + V_6 = 0$$

or, in matrix form,

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 1 & -1 \\ 0 & 1 & 0 & -1 & 1 & 0 \\ 0 & 0 & 1 & -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \end{bmatrix} = \vec{0}$$

2.6 Nonlinear Elements in Wave Digital Filters

Modeling nonlinear elements in the wave domain is possible in many cases where the nonlinear element is memoryless [8], in which case its nonlinear characteristic can be mapped directly into the wave domain through the affine transformation that defines the wave variables as a function of the Kirchhoff variables. Nonlinear elements with memory are described by a differential equation rather than an algebraic one. In order to model nonlinear elements with memory, classical WDF principles are no longer adequate. Based on the classical WDF theory, a new class of wave variables and generalized adaptors are used to model a variety of nonlinear elements with memory in the wave domain [9].

2.6.1 Nonlinear Resistors

Under mild conditions we can simulate the behavior of a circuit containing a nonlinear resistor by connecting an appropriate instantaneous map with a reflection-free port of an adaptor [8].

A nonlinear resistor is generally defined as an algebraic relationship of the form $F(v,i)=0$ in the Kirchhoff variables. The Kirchhoff characteristic of the resistor can be transformed into a wave characteristic of the form $f(a,b)=0$ through the following mapping:

$$f(a,b) = F(\frac{a+b}{2}, \frac{a-b}{2R}) = 0 \tag{2.23}$$

The conditions that allow us to write the reflected wave b as an explicit function

$b = \tilde{f}(a)$ of the incident wave a are provided by the implicit function theorem.

In fact, if the characteristic function of the resistor $f(a,b)$ with its derivatives are continuous and if the point (a_0, b_0) lies on the characteristic of the resistor, then the condition

$$\left.\frac{\partial f}{\partial b}\right|_{(a_0,b_0)} \neq 0 \tag{2.24}$$

guarantees the existence of a function $\tilde{f}(\bullet)$ such that $f(a,\tilde{f}(a)) = 0$ in a neighborhood of a_0.

The nonlinear characteristic $F(v,i) = v - v(i) = 0$ of a current-controlled nonlinear resistor is mapped onto the wave characteristic

$$f(a,b) = \frac{a+b}{2} - v\left(\frac{a-b}{2R}\right) = 0$$

To check if it guarantees the existence of a function $\tilde{f}(\bullet)$,

$$\frac{\partial f}{\partial b} = \frac{\partial}{\partial b}\left\{\frac{a+b}{2} - v\left(\frac{a-b}{2R}\right)\right\}$$

$$= \frac{1}{2} - \frac{\partial v}{\partial i}\frac{\partial i}{\partial b} = \frac{1}{2} + \frac{1}{2R}v'\left(\frac{a-b}{2R}\right)$$

$$v'(i) = \frac{dv}{di}$$

As a result, the local invertibility of the characteristic $v = v(i)$, i.e., the possibility of rewriting it in the form $b = \tilde{f}(a)$, is guaranteed by the condition $v'(i) \neq -R$.

The same procedure can also be applied to a voltage-controlled resistor with characteristic $F(v,i) = i - i(v) = 0$. The local invertibility condition is given by $i'(v) \neq -1/R$.

2.6.2 Nonlinear Elements with Memory

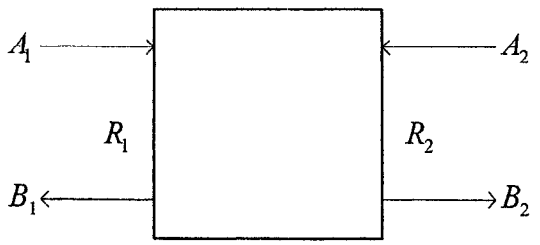

Figure 2.11: Scattering junction

Fig. 2.11 shows a scattering junction of two-port element which can transform the wave pair (A_1,B_1), which is referred to the reference transfer function (RTF) $R_1(z)$, into the wave pair (A_2,B_2), which is referred to $R_2(z)$. $R_1(z)$ and $R_2(z)$ are the Z transformation of arbitray port "impedance" $R_1(s)$ and $R_2(s)$. Let

$$\begin{aligned} A_1(z) &= V_1(z) + R_1(z) I_1(z) \\ B_1(z) &= V_1(z) - R_1(z) I_1(z) \\ A_2(z) &= V_2(z) + R_2(z) I_2(z) \\ B_2(z) &= V_2(z) - R_2(z) I_2(z) \end{aligned}$$

Where $A_1(z)$ and $A_2(z)$ are the waves that enter the junction, and $B_1(z)$ and $B_2(z)$ are the corresponding reflected waves. The scattering junction is then characterized by the continuity constraints $V_1(z) = V_2(z)$ and $I_1(z) + I_2(z) = 0$.

$$\begin{aligned} I_1(z) = -I_2(z) &= \frac{A_1(z) - A_2(z)}{R_1(z) + R_2(z)} \\ \left.\begin{aligned} B_1(z) - A_2(z) \\ B_2(z) - A_1(z) \end{aligned}\right\} &\Rightarrow \begin{cases} B_1(z) = K(z) A_1(z) + (1 - K(z)) A_2(z) \\ B_2(z) = (1 + K(z)) A_1(z) - K(z) A_2(z) \end{cases} \end{aligned} \tag{2.25}$$

where

$$K(z) = \frac{R_2(z) - R_1(z)}{R_2(z) + R_1(z)} \tag{2.26}$$

The transfer function $K(z)$ characterizes the scattering junction with memory, which

is expected to be causal and stable.

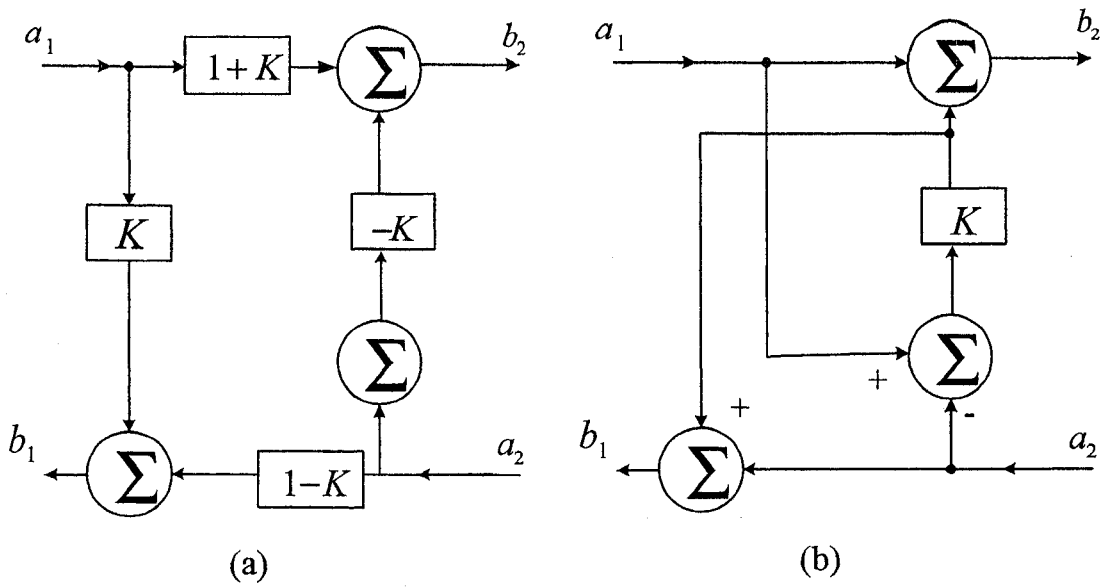

Figure 2.12: (a) Direct implementation of the scattering junction (b) the simplified mode

A direct implementation of equations (2.25) is shown in Fig. 2.12 (a), which can be simplified as shown in Fig. 2.12 (b). From Fig. 2.12, we notice that the wave a_1 that enters port 1 is partially reflected through the transfer function $K(z)$ and partially transmitted to port 2 through $1+K(z)$, whereas the wave a_2 entering port 2 is partially reflected through $-K(z)$ and partially transmitted through $1-K(z)$.

When considering the digital implementation of a scattering junction, it is of crucial importance to derive the conditions under which any of its ports do not exhibit any instantaneous reflection, as its interconnection with other circuit ports might give rise to delay free loops. In order to avoid instantaneous reflection of the waves entering the two ports of a digital scattering junction, it is necessary and sufficient for $K(z)$ to exhibit no instantaneous input/output connection, i.e., $K(z)=z^{-1}\hat{K}(z)$, with $\hat{K}(z)$ causal and stable.

A particular case of wave scattering junctions with memory is represented by the wave digital mutators [11], which are intimately related to a class of two-port analog

elements [10] called mutators, which are built using only operational amplifiers and linear passive resistors and capacitors. Mutators can be used to transform a nonlinear capacitor into a nonlinear resistor while preserving the nonlinear characteristic in the transformed Kirchoff domain. This property can be quite useful as, for example, synthesizing a nonlinear capacitor with prescribed $v-q$ characteristic is much more difficult than implementing a nonlinear resistor with the same characteristic in the $v-i$ plane.

The scattering junction with memory represents a direct extension of the concept of mutator because it is suitable for modeling a wide class of dynamic nonlinear elements.

The wave R-C mutator is simply a scattering junction between a capacitive RTF and resistive one. With reference to the equation $K(z)$, the situation can be dealt with by letting $R_1(s)=R$ and $R_2(s)=1/sC$, $C>0$. By applying bilinear transformation, the transfer function $K(z)$ becomes

$$K(z)=\frac{R_2(z)-R}{R_2(z)+R} \qquad R_2(z)=\frac{T}{2C}\frac{1+z^{-1}}{1-z^{-1}}$$

Let $R=T/2C$ to eliminate the instantaneous reflections at both ports. In this case, we have $K(z)=z^{-1}$.

In order to adapt a capacitive RTF to a resistive one, we can use a scattering junction whose reflection coefficient is replaced by a pure delay and whose second port is left unconnected. As a consequence, the whole scattering junction may be replaced with just one delay element, which is how the classical WDF theory deals with linear capacitors. The following figure shows the structure of R-C mutator.

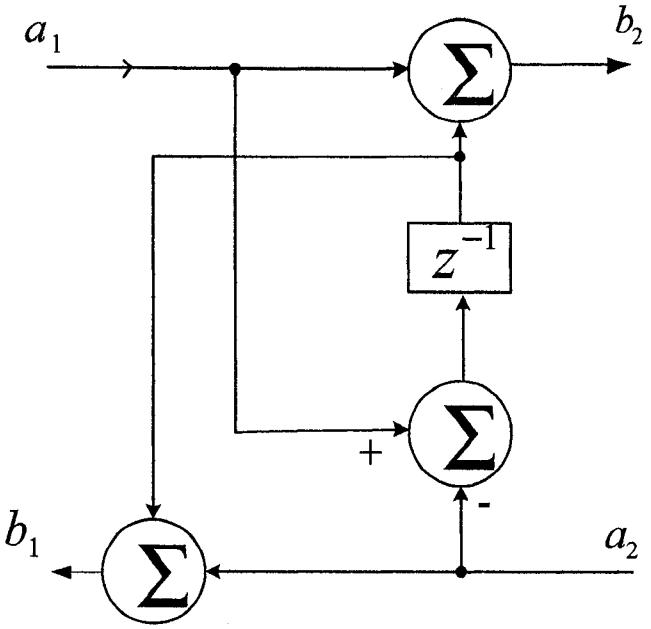

Figure 2.13: Structure of the R-C mutator

The wave R-C mutator can be used to extend the results on nonlinear resistors to the case of nonlinear capacitors. In fact, the waves at port 2 of the R-C mutator are

$$\begin{aligned} A_2(z) &= V(z) + \frac{T}{2C}\frac{1+z^{-1}}{1-z^{-1}} I(z) = V(z) + \frac{1}{C} Q(z) \\ B_2(z) &= V(z) - \frac{T}{2C}\frac{1+z^{-1}}{1-z^{-1}} I(z) = V(z) - \frac{1}{C} Q(z) \end{aligned} \tag{2.27}$$

where $Q(z)$ is associated with the electrical charge $q(t)$, $\dot{q}(t) = i(t)$. A nonlinear capacitor can be described by an algebraic relationship of the form $P(v,q) = 0$ between the electrical charge q and the voltage v. C plays the role of reference capacitance in the linear transformation that maps the Kirchhoff characteristic of the nonlinear capacitor onto the wave domain. In order to implement the nonlinear capacitor in the wave domain, we only need to implement a nonlinear map of the form $b = \tilde{f}(a)$ and connect it with the capacitive port of the R-C mutator by letting $a = b_2$ and $a_2 = b$.

The wave R-L mutator is simply a scattering junction between an inductive RTF and a resistive one. With reference to the equation $K(z)$, let $R_1(s) = R$ and

$R_2(s) = sL$, $L > 0$. After bilinear transformation, the transfer function becomes

$$K(z) = \frac{R_2(z) - R}{R_2(z) + R} \qquad R_2(z) = \frac{2L}{T}\frac{1+z^{-1}}{1-z^{-1}}$$

We may eliminate the instantaneous reflection at both ports by letting $R = 2L/T$, in which case we have $K(z) = -z^{-1}$. This is expected from the classical WDF theory. The corresponding R-L mutator results as being a dynamic scattering junction, whose transfer function is just a delay element with sign change. The R-L mutator is shown in Fig. 2.14.

The R-L mutator can be employed for implementing nonlinear inductors of the form $M(v, j) = 0$. The waves at port 2 of the R-L mutator are

$$\begin{aligned} A_2(z) &= V(z) + \frac{2L}{T}\frac{1-z^{-1}}{1+z^{-1}} I(z) = V(z) + LJ(z) \\ B_2(z) &= V(z) - \frac{2L}{T}\frac{1-z^{-1}}{1+z^{-1}} I(z) = V(z) - LJ(z) \end{aligned} \tag{2.28}$$

where $J(z)$ is the Z-transform of the discretized version of $j(t) = di(t)/dt$, and L is a constant parameter that plays the role of a reference inductance.

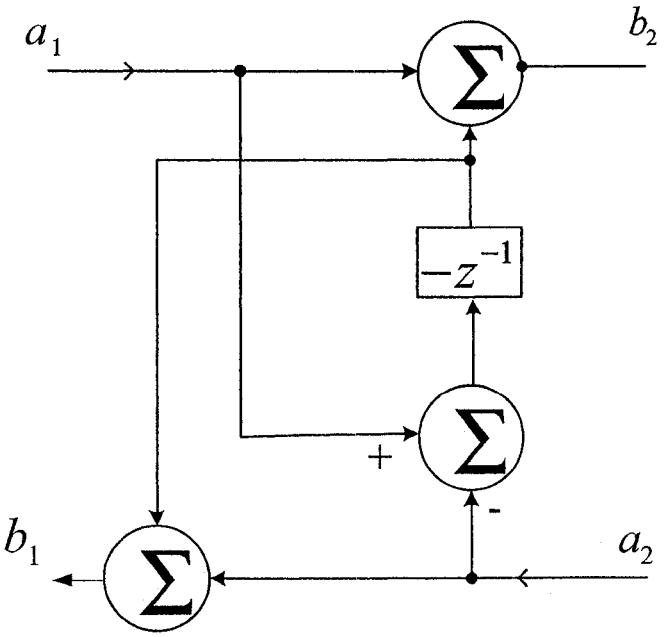

Figure 2.14: Structure of the R-L mutator

2.6.3 Circuits with More Than One Nonlinearity

Most of methods concerning nonlinear networks can only work for the circuits that contain a single nonlinearity. In [24], the author proposed a method based on the usage of a vector approach. Any arbitrary number of nonlinearities can be modeled by one single vector-nonlinearity, so that the complete network is the combination of one nonlinear vector-WDF with a delay free feedback, adapted to the linear part of the network which includes a delay. This method is implemented by using the look-up-tables of the nonlinearities. But this method is not useful for networks that contain many nonlinearities since the size of the vector-nonlinearity table will grow exponentially when more nonlinearities are added to the network.

In [25], Felderhoff proposed a convergent relaxation method that can be used to systematically generate a massive parallel algorithm, and simulate the networks with many nonlinear devices. But so far it was only applied for the simulation of a nonlinear transmission line.

Fiedler and Grotstllen [7] proposed a method to treat some special types of nonlinearities in WDF, but this can not be used for nonlinear circuits in general.

Chapter 3

LC VCO Design

3.1 Introduction

VCOs are widely used in wireless and optical communication systems. In wireless transmission systems, the VCO is used for the frequency synthesizer to generate the local oscillating signal for the modulation and demodulation of the RF signal. In digital optical transmission systems, VCOs are used as the core circuit of the clock recovery circuit, whose output signal is used for data decision and regeneration.

A general VCO can be treated as a black box with an input V_{tune} and a periodic oscillating output $V_{out}(t)$. The VCO is connected to the power supply through V_{ss} and V_{dd} [12]. The output voltage ($V_{out}(t)$, differential or single ended), is periodic:

$$V_{out}(t) = V_0 \sin(\omega_c t + \varphi) \tag{3.1}$$

where φ is the phase and V_0 the amplitude. The angular carrier frequency,

$$\omega_c(V_{tune}) = 2\pi f_c(V_{tune}) \tag{3.2}$$

is dependent on the tuning voltage input (V_{tune}).

We will first review two types of oscillator: ring oscillators and LC oscillators. Secondly an LC VCO is designed. The detailed design process along with simulation results is presented. At last, the layout of the LC VCO is described.

3.2 Ring Oscillators and LC Oscillators

According to the structure, the VCO can be divided into two types: ring oscillators and LC Oscillators.

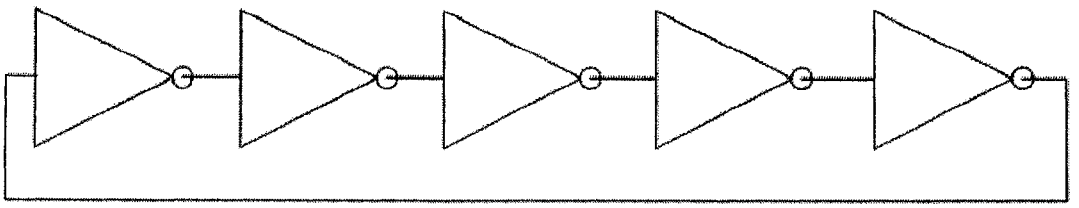

Figure 3.1: Ring oscillator topology

A classical ring oscillator circuit is the connection of amplifiers or inverters in a ring structure. If the phase shift over the ring at one frequency is 360°, the ring will oscillate at that frequency. Fig. 3.1 shows an exemplary ring oscillator topology. Ring oscillators have a very small area and are easy to integrate and design. They feature wide tuning ranges. Their main disadvantage is phase noise.

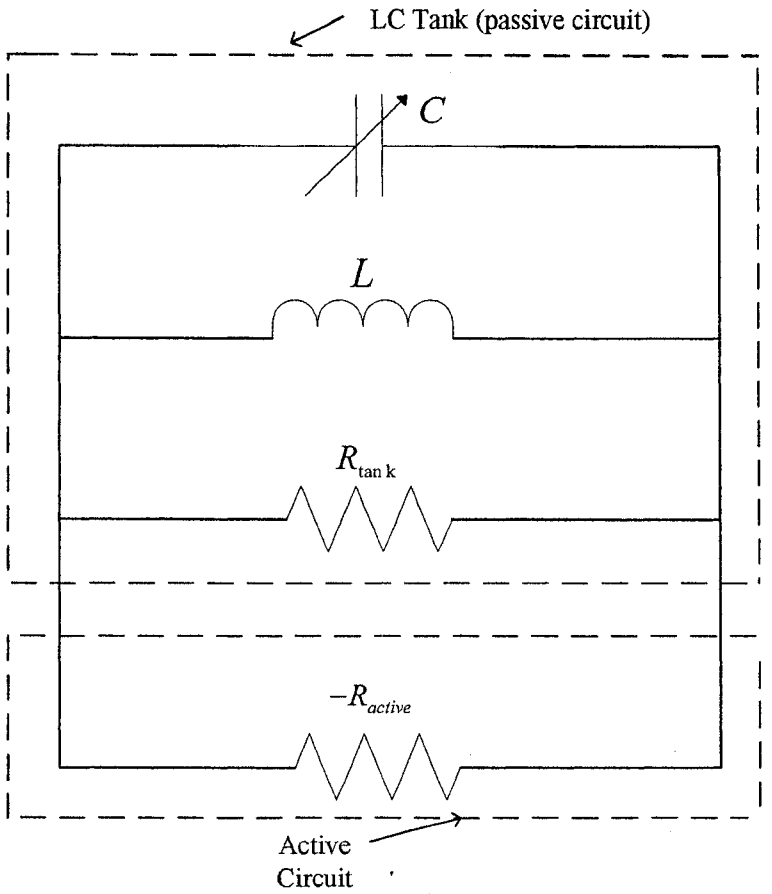

Figure 3.2: Basic LC VCO

The LC VCO consists of an inductor L and a variable capacitor C, building a parallel resonance tank, and an active element –R, compensating the losses of the

resonance tank, which are losses of inductor and the losses of the capacitor. The basic LC oscillator circuit is shown in Fig. 3.2. The circuit results in an oscillator with angular center frequency.

$$\omega_c = \frac{1}{\sqrt{LC}} \tag{3.3}$$

If the capacitance C is proportional to the tuning voltage V_{tune}, ω_c is dependent on V_{tune}. The capacitor C not only consists of a variable capacitor to tune the oscillator, it also includes the parasitic or fixed capacitances of the inductor, the active elements, and of any load connected to the VCO. The advantages of LC VCOs are their outstanding phase noise and jitter performance at high frequency. Their main disadvantages are high power consumption and large area.

3.3 LC VCO Design

An LC VCO circuit is designed as a case study for WDF simulation. The design uses TSMC CMOS 0.18 μm technology available through CMC Microsystems. The supply voltage is 1.8 V. The design goal is to tune the frequency from 2.5 GHz to 3.0 GHz. The reason for this tuning range is to achieve the highest frequency possible with the 24-pin package which has the limitation of 3 GHz. The following Cadence tools will be used in this design:

- Virtuoso Composer for schematic design
- Analog Environment (Spectre) for schematic simulation and post-layout simulation
- Virtuoso Layout for layout
- Diva for DRC (design rule checking), extraction and LVS (layout vs. schematic)

There are many things which need to be considered in the design procedure. Fig. 3.3 shows the flow chart for designs by Cadence tools to make the whole design procedure more understandable.

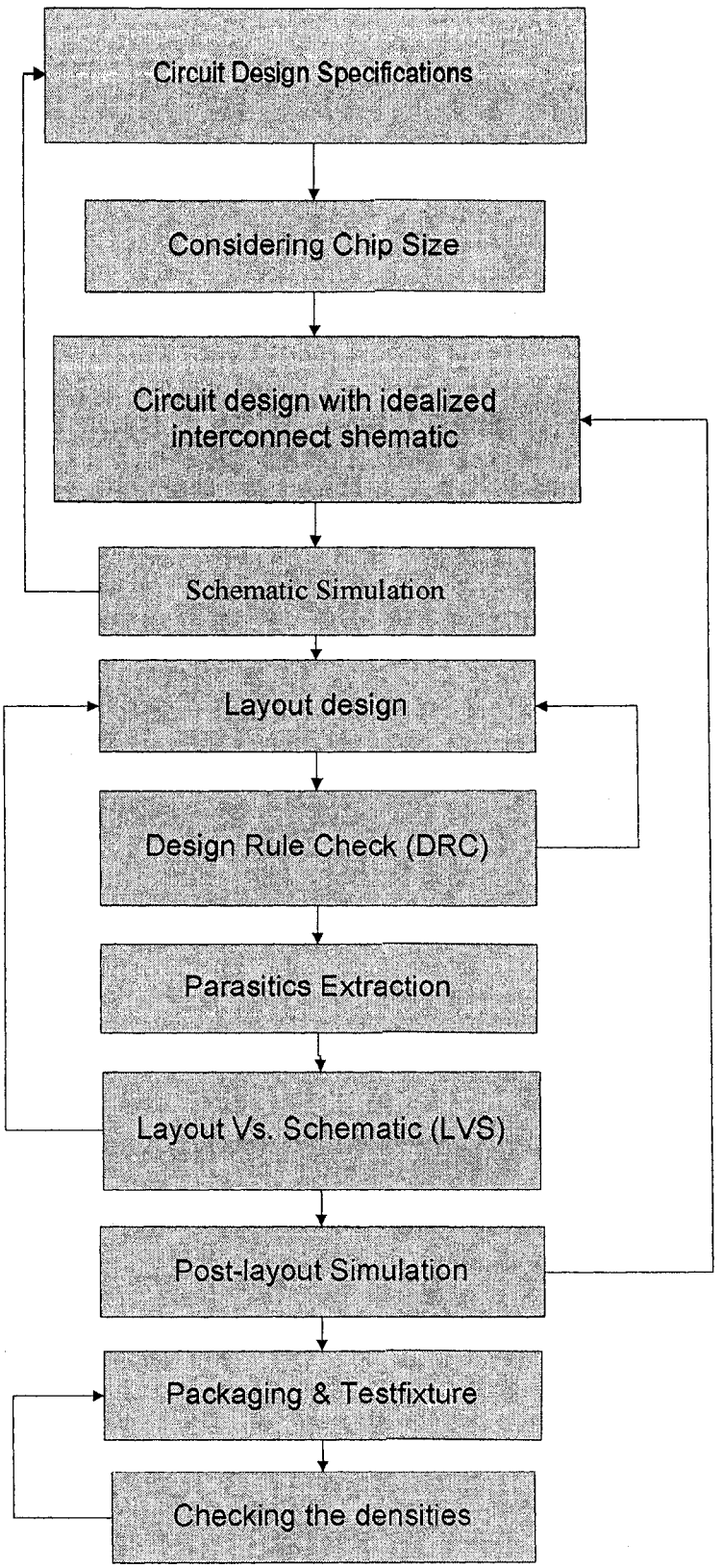

Figure 3.3: The flow chart for designs by Cadence tools.

3.3.1 LC VCO Topology

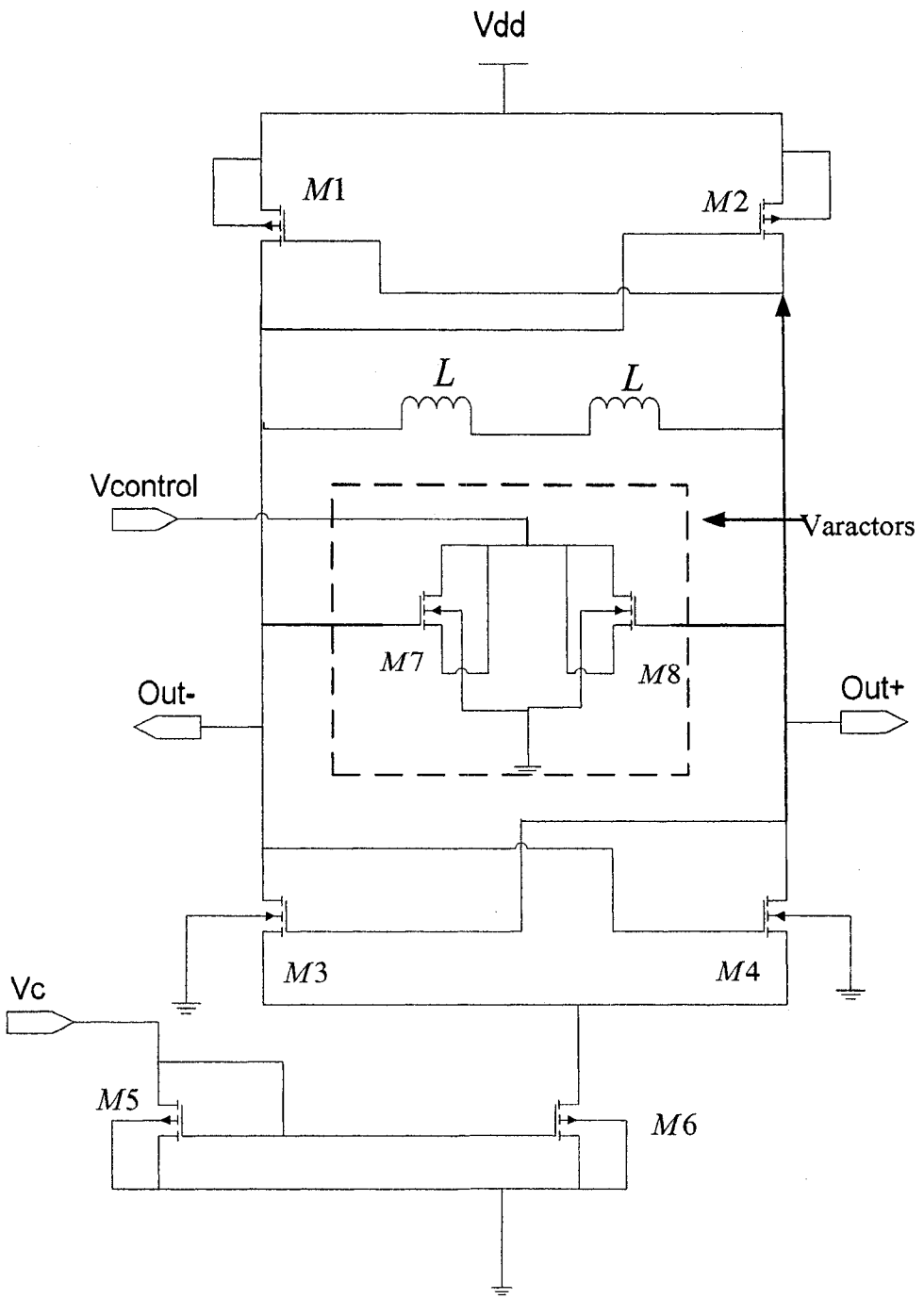

Figure 3.4: LC VCO Schematic ($Vc=V_{dd}$)

Many circuits can provide the negative resistance of Fig. 3.2 to compensate for the tank losses. A standard approach for differential VCOs is the use of cross-coupled transistors to generate a negative resistance. The negative resistance should be large enough to overcome the equivalent parallel resistance of the VCO tank circuit to generate the desired oscillation. The complementary cross-coupled oscillator circuit is

the result of using both PMOS and NMOS cross coupled pairs in parallel to generate the negative resistance. Figure 3.4 shows the schematic view of the designed complementary cross-coupled LC VCO. Since the same bias current flows through both the PMOS and NMOS pairs, the negative resistance can be twice as large for the same power. In the complementary circuit, the amplitude is limited by both supply voltage and tail current source. The differential voltage swing is limited to the supply voltage.

In Fig. 3.4, the transistors M5 and M6 compose the current mirror to provide the tail current. The PMOS pair (M1, M2) and NMOS pair (M3, M4) form the negative resistance compensating the VCO losses. Two spiral inductors L have the same values. NMOS transistors M7 and M8 are the NMOS varactors.

The design variables obviously are the inductor parameters, the total tank capacitance C, the width and the length of the transistors and the bias current. Since the interdependences of the design parameters are very complex, it is hard to calculate all parameters according to the equations. Fine tuning is necessary according to simulation results of the DC operating point in the Spectre. The LC VCO design follows the steps shown below,

- Design the spiral inductor
- Design NMOS and PMOS transistors according to the model of Spiral inductor
- Design varactor according to the oscillating frequency range and the parasitic capacitances
- Design the current mirror that can provide enough tail current

3.3.2 Spiral Inductor

An on-chip planar spiral inductor can be made with many different layout structures. In this design, a square-shaped spiral inductor is employed. This is shown in Fig. 3.5. Any device below the inductor is forbidden due to the magnetic flux that penetrates into the silicon substrate. This flux would affect the device behavior when the device is under spiral inductor. Increasing the turns of spiral inductor will increase the inductance value. In Fig. 3.5, the key parameters of the spiral inductor layout are

depicted:

- N: number of coil turns
- W: metal width of top metal
- S: metal space of top metal
- R: radius inside inner coil

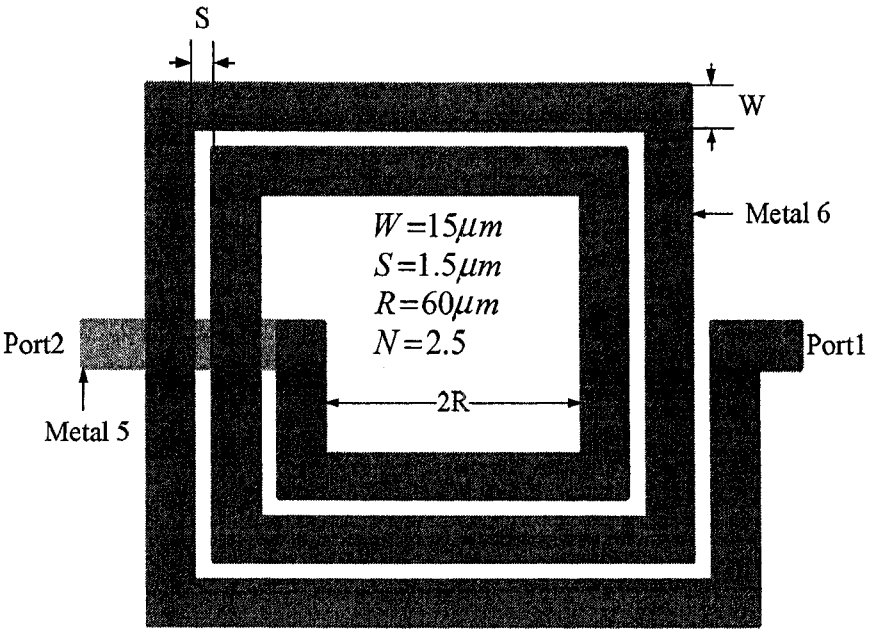

Figure 3.5: Square spiral inductor layout

A two-port π-type circuit used to model the spiral inductor is shown in Fig. 3.6. The following is a short explanation of the various components found in the equivalent circuit model [12]:

- L_s : caused by the magnetic flux density of the electromagnetic field
- R_{sub} : is used to model the ohmic losses in the silicon substrate
- R_s : characterizes series resistance of the metal traces.
- C_s : overlap capacitance between the spiral and the center tap underpass
- C_{ox} : The oxide capacitance between the spiral and substrate
- C_{sub} : is used to characterize the capacitance in substrate.

The expressions that calculate the lumped elements in Fig. 3.6 vary considerably from one model to the other. In [13, 14], they give expressions of L, Rs, Cs, Cox, Rsub, Csub are given as functions of the inductor's geometry. These expressions can be used to approximate the values of those parameters.

For convenience and accuracy, the expressions of those parameters are adopted directly from [15]. Since these expressions are measured and tested by TSMC, they provide a more accurate approximation. The values of these parameters for N=2.5 are shown in Table 3.1 with $W = 15\mu m$, $S = 1.5\mu m$ *and* $R = 60\mu m$.

L_s	R_s	C_s	C_{ox1}	C_{ox2}	C_{sub1}/C_{sub2}	R_{sub1}/R_{sub2}
2.307nH	2.01Ω	18.68fF	63.99fF	54.5fF	37.63fF	444Ω

Table 3.1: The values of spiral inductor parameters

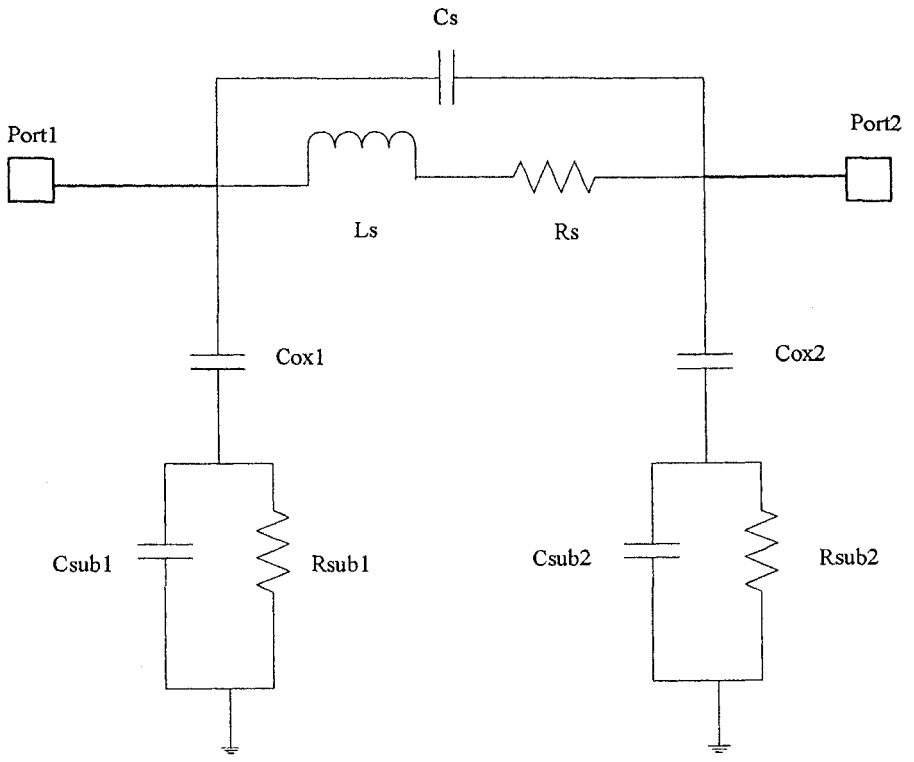

Figure 3.6: Spiral inductor equivalent circuit model

The energy storage and loss mechanisms in an inductor on silicon, L_s, R_s, $R_{p(1 \text{ and } 2)}$ and $C_L = C_{p(1 \text{ and } 2)} + C_s$, represent the overall inductance, conductor loss, substrate loss, and overall capacitance respectively in Fig. 3.7. The parameters in

Figure 3.7 will be used to calculate the conductance and parasitic capacitance in the tank model. Note that $R_{p(1 \text{ and } 2)}$ and $C_{p(1 \text{ and } 2)}$ represent the combined effects of $C_{ox(1 \text{ and } 2)}$, $C_{sub(1 \text{ and } 2)}$ and $R_{sub(1 \text{ and } 2)}$, and hence are frequency dependent [16, 17]. The equations are as follows,

$$R_{p(1 \text{ or } 2)} = \frac{1}{\omega^2 \cdot C_{ox(1 \text{ or } 2)}^{\ 2} \cdot R_{sub(1 \text{ or } 2)}} + \frac{R_{sub(1 \text{ or } 2)}(C_{ox(1 \text{ or } 2)} + C_{sub(1 \text{ or } 2)})^2}{C_{ox(1 \text{ or } 2)}^{\ 2}} \tag{3.4}$$

$$C_{p(1 \text{ or } 2)} = C_{ox(1 \text{ or } 2)} \cdot \frac{1 + \omega^2 (C_{ox(1 \text{ or } 2)} + C_{sub(1 \text{ or } 2)}) C_{sub(1 \text{ or } 2)} \cdot R_{sub(1 \text{ or } 2)}^{\ 2}}{1 + \omega^2 (C_{ox(1 \text{ or } 2)} + C_{sub(1 \text{ or } 2)})^2 \cdot R_{sub(1 \text{ or } 2)}^{\ 2}} \tag{3.5}$$

Since the values of C_{ox1} and C_{ox2} are slightly different, we can assume the following equations for calculation purpose,

$$\begin{aligned} C_p &= C_{p1} \cong C_{p2} \\ R_p &= R_{p1} \cong R_{p2} \end{aligned} \tag{3.6}$$

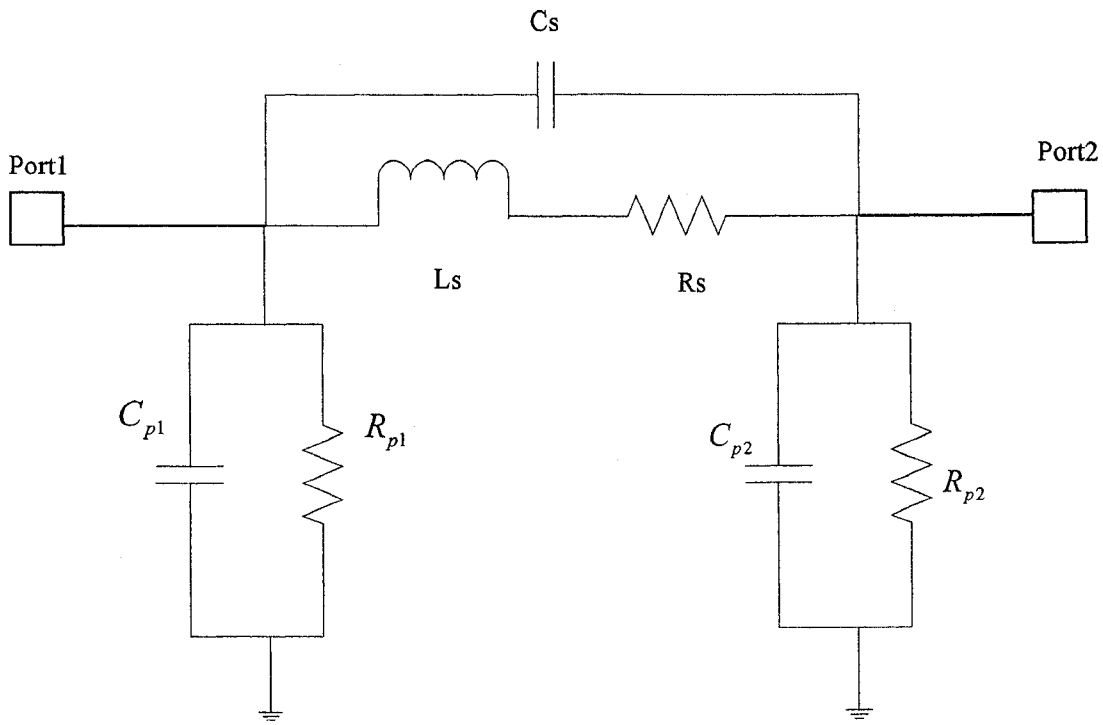

Figure 3.7: Simplified spiral inductor equivalent circuit model

3.3.3 NMOS Varactors

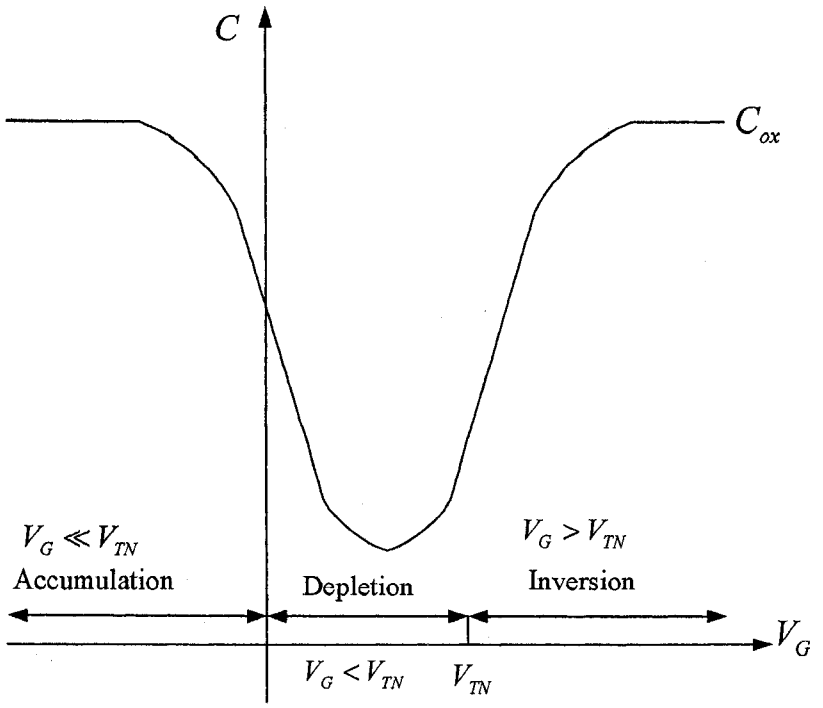

Figure 3.8: Capacitance NMOS structure with gate voltage (V_G)

NMOS varactors are variable, voltage-controlled capacitors based on the NMOS structure. Figure 3.8 depicts the variation of the capacitance of the NMOS structure with gate voltage. At voltages well below the threshold voltage V_{TN}, the surface is in accumulation and the capacitance is high and determined by the oxide thickness. As the gate voltage increases, the surface depletion layer forms. In this region, the effective separation of the capacitor plates increases, and the capacitance decrease steadily. The inversion layer forms at the surface as V_G exceeds the threshold voltage, and the capacitance rapidly increases back to the value determined by the oxide layer thickness.

Figure 3.9 shows a cross-section of an inversion mode NMOS varactor. The NMOS varactor is not a four-terminal device as the transistor but a three-terminal device. The source and drain regions are shorted to apply the voltage V_{tune} that tunes the variable capacitance. The bulk is grounded and the voltage V_G is applied to the gate node.

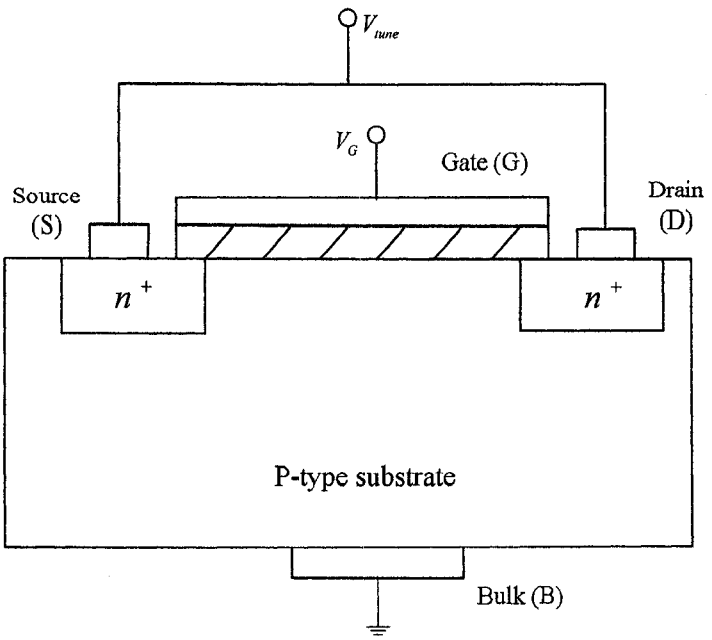

Figure 3.9: Cross section of the inversion mode NMOS varactor

C_{ox} represents the oxide capacitance of the transistor, which is given as

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} W \cdot L \quad , \tag{3.7}$$

with t_{ox} being the thickness and ε_{ox} being the dielectric constant of the oxide. C_{ox} is directly proportional to the transistor area, expressed through the factors W (width of the NMOS) and L (length of the NMOS). The silicon substrate is connected to the lowest potential to prevent the transistor from entering accumulation region since we need a linear capacitance range. The upper limit of the capacitance is determined by C_{ox}. The capacitance value changes depending on the voltage across the gate and shorted Drain-Source terminals. Increasing the voltage towards the threshold voltage results in establishing a surface layer between gate and shorted Drain-source. The total capacitance is a combination of a voltage dependent depletion-layer capacitance C_d in series to the oxide capacitance [12] [18]. This is shown in Fig. 3.10(a).

Therefore,

$$\frac{1}{C_v} = \frac{1}{C_{ox}} + \frac{1}{C_d} \tag{3.8}$$

The generally assumed model of the NMOS varactor is shown in Fig. 3.10(b) [12].

R_v is variable resistance. The relationship between the variable capacitance of the NMOS varactor and the voltage between gate and source/drain terminals is shown in Fig. 3.11.

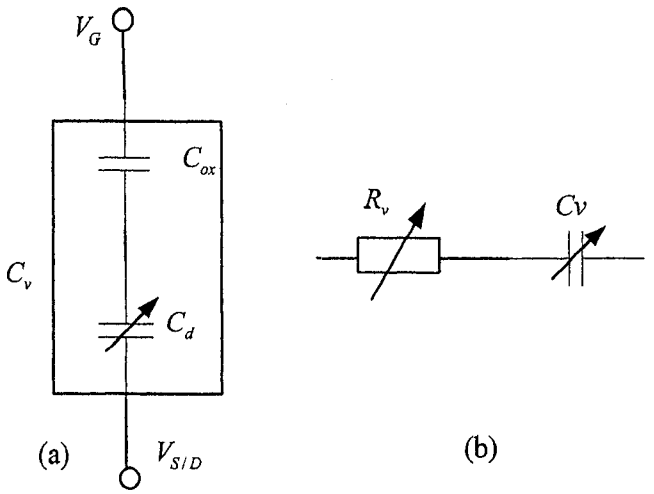

Figure 3.10: (a)Total capacitance of the NMOS varactor in depletion; (b)the generally assumed model of NMOS varactor.

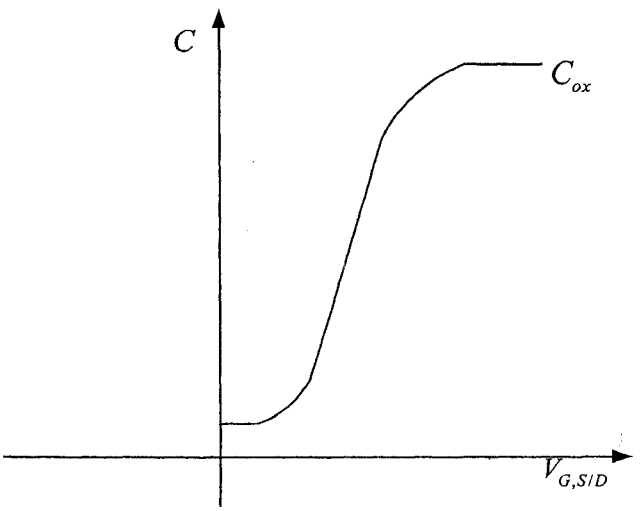

Figure 3.11: Variable capacitance of the NMOS Varactor

3.3.4 Tank Model Calculation Along with Simulation Results

The equivalent circuit model for the complementary cross-coupled LC VCO of Fig. 3.4 is depicted in Fig. 3.12. There are four primary parameters that are closely related to the oscillator behavior and will be helpful in the derivation of the constraints. These parameters are the effective tank conductance g_{tank}, the effective

negative conductance g_{active}, the tank capacitance C_{tank}, and the tank inductance L_{tank} [19, 20, 21].

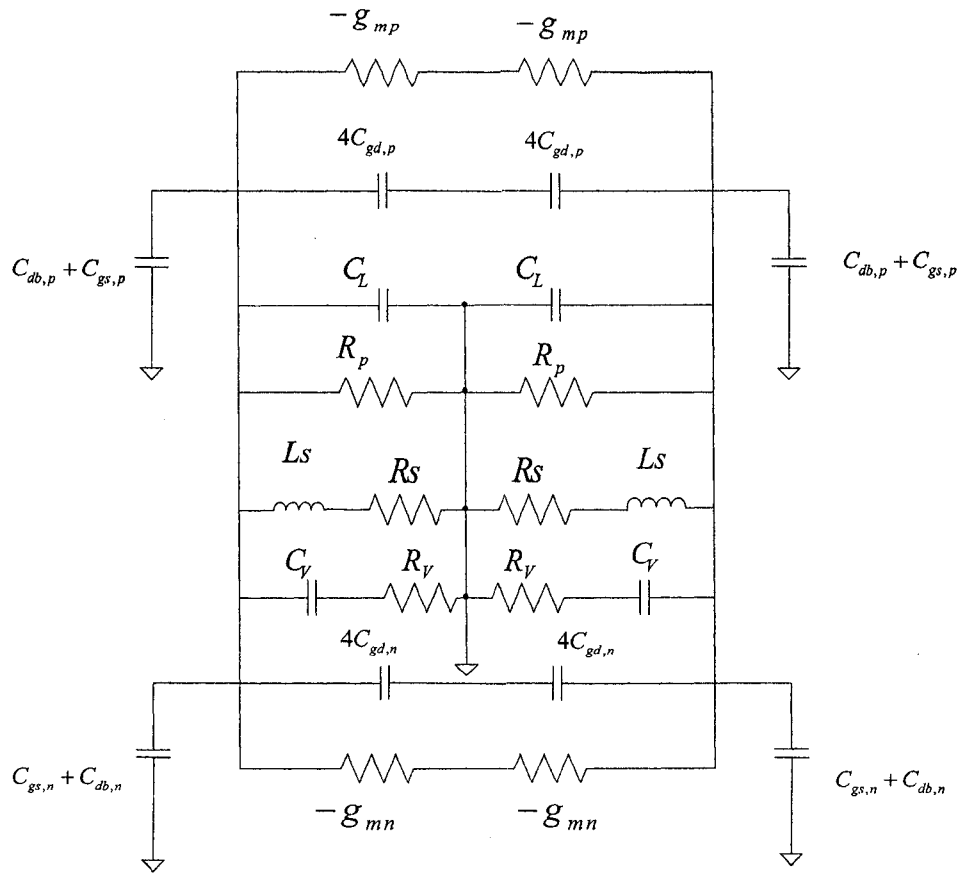

Figure 3.12: The tank model of the LC VCO

The equations for those parameters are shown as follows,

$$f = \frac{1}{2\pi\sqrt{L_{\text{tank}}C_{\text{tank}}}} \tag{3.9}$$

$$L_{\text{tank}} = 2Ls \tag{3.10}$$

$$C_{\text{tank}} = \frac{1}{2}(4C_{gd,n} + C_{gs,n} + C_{db,n} + 4C_{gd,p} + C_{gs,p} + C_{db,p} + C_L + C_V) \tag{3.11}$$

$$g_{\text{tank}} = \frac{g_{on} + g_{op} + g_v + g_L}{2}, \tag{3.12}$$

where g_v is the effective parallel varactor conductance and g_L is the effective parallel inductor conductance, which are respectively given by

$$g_L = \frac{1}{R_p} + \frac{R_s}{(L_s\omega)^2} \tag{3.13}$$

$$g_v = (C_V\omega)^2 \cdot R_v \tag{3.14}$$

g_{on} is the output conductance of the NMOS transistors and g_{op} is the output conductance of the PMOS transistors. Usually these two conductances are low enough compared with g_L to be neglected.

$$g_{active} = \frac{g_{mn} + g_{mp}}{2} \tag{3.15}$$

$$g_{mn} = \frac{\partial I_D}{\partial V_{GS\ VDScont}} = \sqrt{2\mu_n C_{ox}\frac{W}{L} I_D}\ , \tag{3.16}$$

where g_{mn} and g_{mp} are the transconductance of the NMOS and PMOS transistors. μ_n and I_D are the hole mobility and drain current respectively.

$$g_{active} \geq K \cdot g_{\text{tank,max}} \tag{3.17}$$

where K usually has a value of 2 to 3 to guarantee reliable start-up.

$$I_{\text{tank,max}} \cong I_{tail} \tag{3.18}$$

$$V_{out+/out-} \cong \frac{I_{tail}}{g_L/2} \tag{3.19}$$

where $V_{out+/out-}$ is a peak to peak voltage amplitude from a single-ended at node Out- or Out+ of the LC VCO.

The calculation steps of this design are shown as follows,

- Obtain C_{tank} using Equation (3.9) since we know the frequency range and the value of L_{tank}.
- Approximate the value of g_{tank} with Equations (3.12) and (3.13), and approximate the size of NMOS and PMOS transistors with Equations (3.15), (3.16) and (3.17).
- Obtain the varactor capacitance with Equation (3.11) since we know the size of

NMOS and PMOS transistor and total capacitance of the spiral inductor C_L.

- Obtain the size of the varactor using Equation (3.7) since we know the upper capacitance limitation of the varactor.
- Adjust the size of the current mirror to obtain the proper tail current with Equations (3.18) and (3.19) using simulation results from DC operating point.

Notice that g_{mn} and g_{mp} should be equal to reduce the contribution of 1/f noise to the phase noise [26]. The size of NMOS and PMOS transistors are fine-tuned according to simulation results from DC operating points. The tail current is $I_{tail} = 1.712mA$ and the transconductance is $g_{mn} = g_{mp} = 4mS$. Table 3.2 shows the sizes of those transistors in Fig. 3.4

M1, M2	M3, M4	M5	M6	M7, M8
$98\mu m / 0.5\mu m$	$19.8\mu m / 0.5\mu m$	$4\mu m / 0.5\mu m$	$24\mu m / 0.5\mu m$	$210\mu m / 0.5\mu m$

Table 3.2: The sizes of transistors in LC VCO

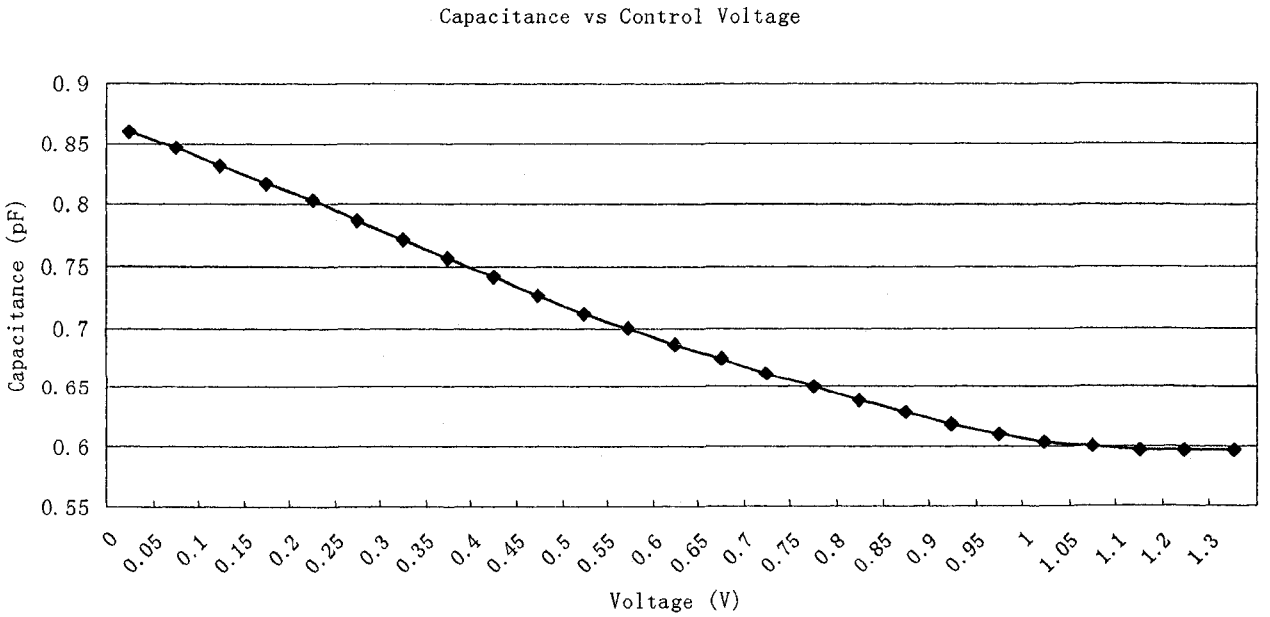

Figure 3.13: Variable capacitance of LC VCO

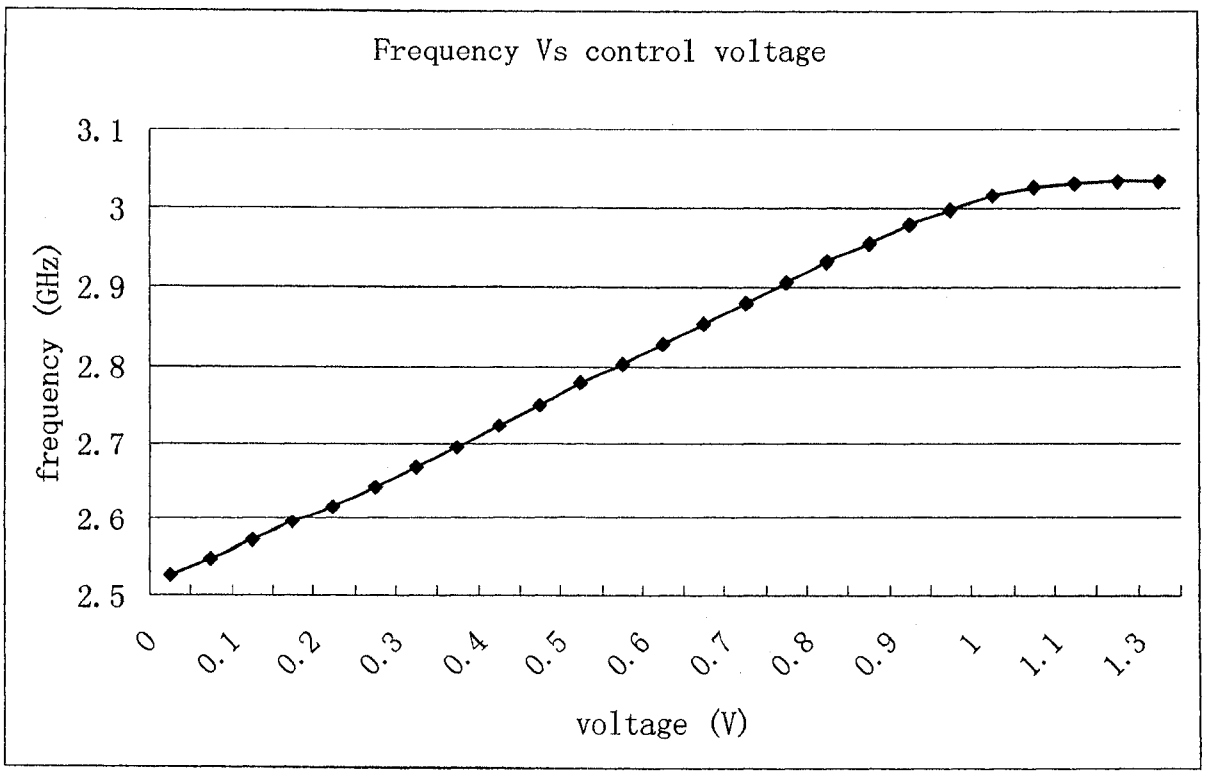

Figure 3.14: Frequency versus the control voltage

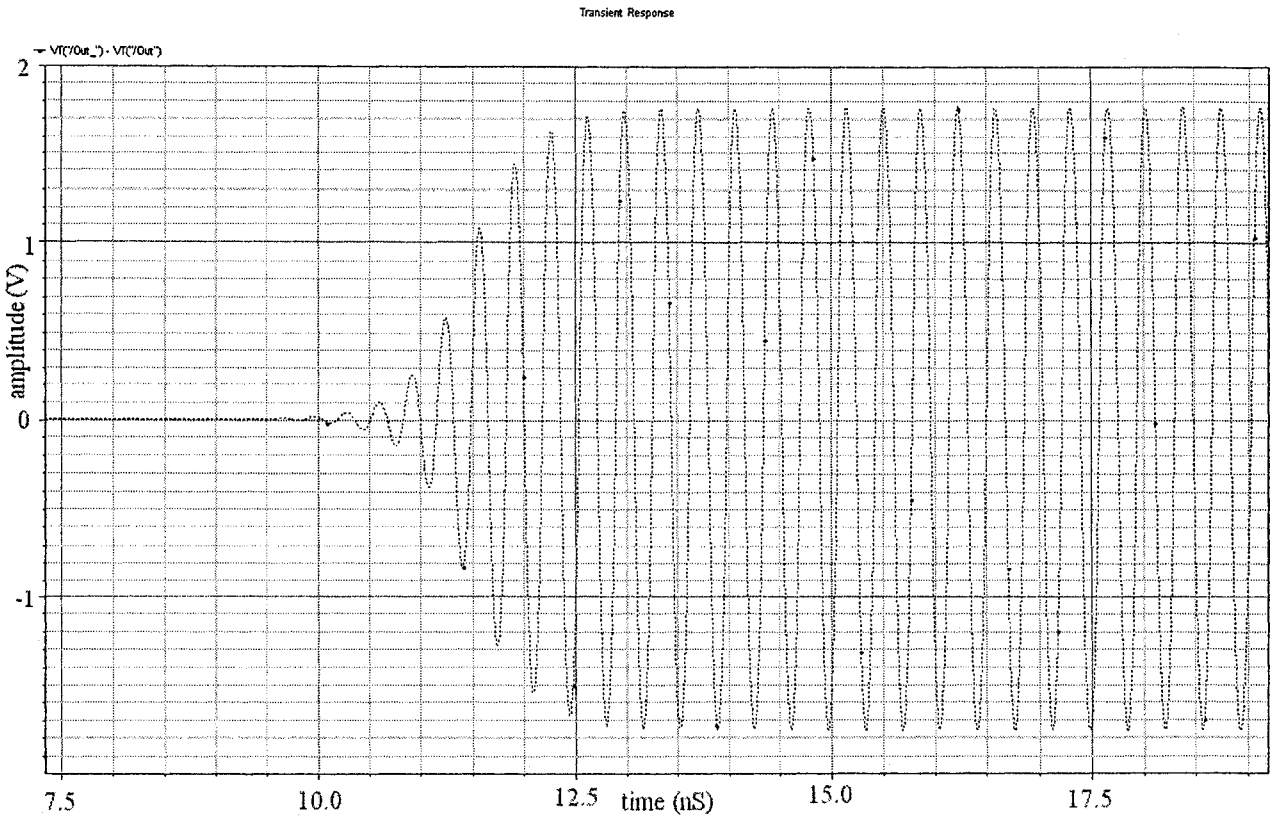

Figure 3.15: Transient response of the LC VCO with a control voltage of 0.5 V

Figure 3.13 shows the simulation of the total tank capacitance (C_{tank}) of the LC VCO. As we can see from this figure, the capacitance decreases as the control voltage increases. When the control voltage changes from 0 to 1 V, the changing of the total capacitance is approximately linear. The frequency versus the control voltage is shown in Fig. 3.14. The linear frequency tuning range is from 2.526 GHz to 3.015 GHz for control voltages from 0 to 1 V. Fig. 3.15 shows the simulation results of the differential output voltage of the LC VCO schematic with a control voltage of 0.5 V.

3.4 Layout of the LC VCO

Layout design is a very delicate and difficult task in radio-frequency because effects, such as capacitive and resistive parasitics degrade the performance of the system. For example, transistors with a very large gate width present an important gate resistance value due to the resistivity of poly-silicon and the contacts. A multi-fingered layout has been made, which means that N transistors with a width $W_i = W / N$ are all connected in parallel, as it is shown in Fig. 3.16. As the gate resistance of each transistor is in parallel with the other gates, the resulted gate resistance is around N times smaller than the simple structure.

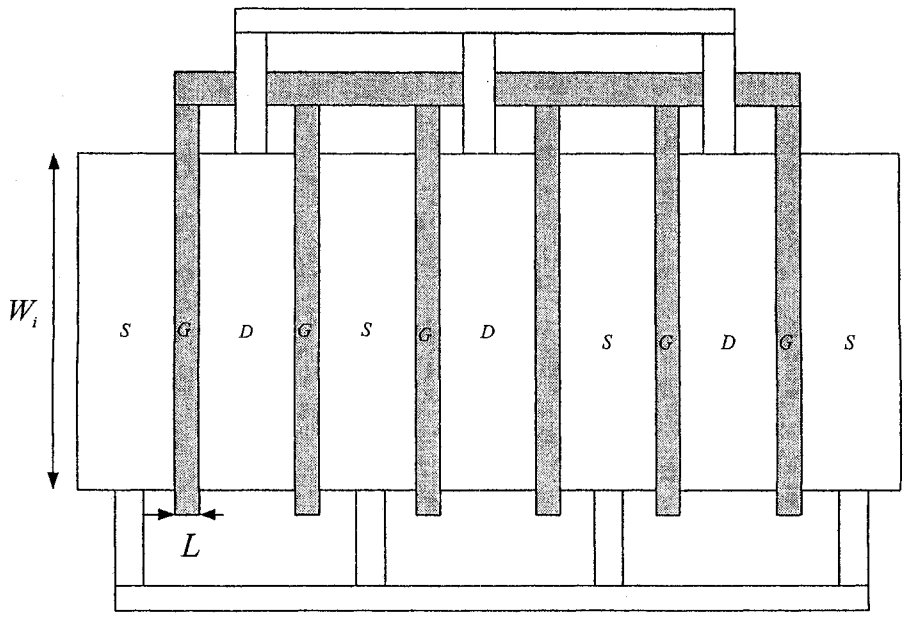

Figure 3.16: Multi-fingered layout of a transistor with width W

Figure 3.17 shows the layout of the LC VCO with output buffers. As we can see from this figure, the spiral inductors occupy most of the area. This design also includes the output buffer, test chip layout and test fixture. These parts are described in Appendix A.

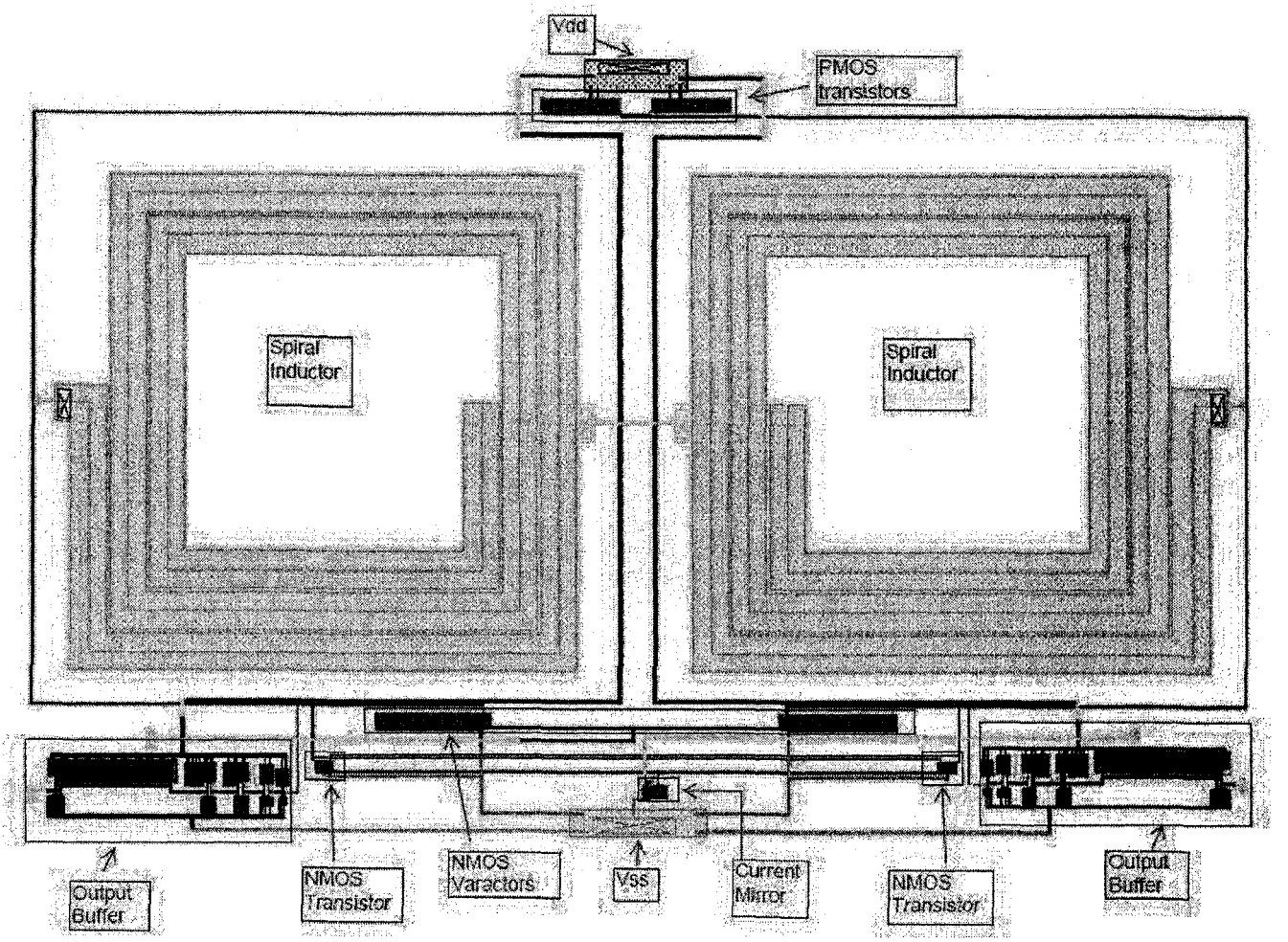

Figure 3.17: The layout of the LC VCO

Chapter 4

Simulations Based on WDF Technique

4.1 Introduction

In this chapter, linear and nonlinear circuits are simulated using WDF principles. In simulations, all the incident and reflected waves are denoted by lower case. WDF simulation results are compared with the exact solution if possible or otherwise with the result obtained with other simulation methods.

We will first present the simulation result of a simple RC circuit as a sample of linear circuit. Secondly an anharmonic oscillator that contains a nonlinear capacitor is simulated by WDF techniques. Lastly, models of the LC VCO with ideal inductors and inductor models are simulated and compared with the simulation results obtained with spectre.

4.2 Simulations of a Linear RC Circuit

WDFs can be used as the basic tool for a general purpose circuit simulator program. Any linear circuit can be simulated with this approach. Figure 4.1 shows a simple RC circuit which will be used to test simulation using WDF principles and the WDF implementation of this circuit.

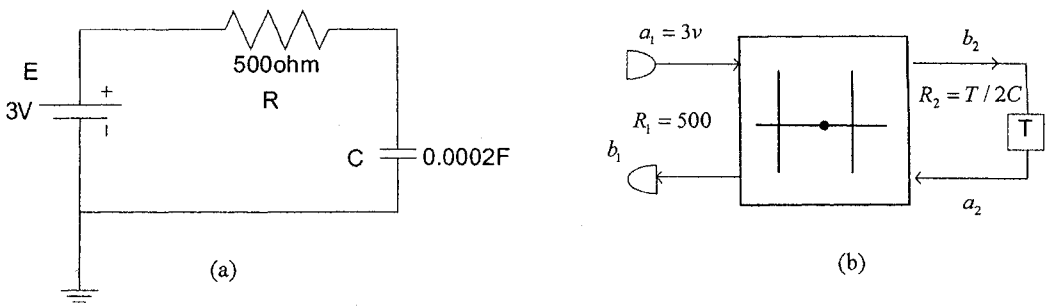

Figure 4.1: (a) RC circuit and (b) WDF implementation of the RC circuit

The following equation is the exact solution of the RC circuit:

$$V_c = E\left(1 - e^{\frac{-t}{RC}}\right),$$

where V_c is the voltage of capacitor.

The following are the equations arising from the WDF analysis of the RC circuit:

$$R_2 = T/2C$$

$$\alpha = \frac{R_1 - R_2}{R_1 + R_2}$$

$$b_2(t_j) = a_1 + \alpha(a_2(t_j) - a_1)$$

$$a_2(t_j) = b_2(t_j - T)$$

$$V_3(t_j) = \frac{a_2(t_j) + b_2(t_j)}{2}$$

$$I_3(t_j) = \frac{b_2(t_j) - a_2(t_j)}{2R_2}$$

When the circuit is simulated, the procedure of the simulation can be divided into the following steps,

- Initialize the devices L, C, R,··· describing the circuit.
- Calculate the port resistances
- Calculate the adaptor coefficients
- Initialize the signal variables, like a_2 and b_2, with appropriate values.
- Simulate the circuit and store the state variables.

The simulation is implemented in Matlab. Time step (T) is set to be 0.05s and 0.002s. As we can see from the simulation results in Fig. 4.2, the simulation with T=0.05s has a larger error than the simulation with T=0.002s. To make the difference between the simulation with T=0.002s and the exact solution clear, the error between them is plotted in Fig. 4.3.

The time step affects the simulation results. When a smaller time step is applied, a more accurate result is obtained. With a small step size, the simulation shows a good approximation to the exact solution. WDF techniques offer a similar trade off between time step size and accuracy as other integration techniques. It takes longer simulation

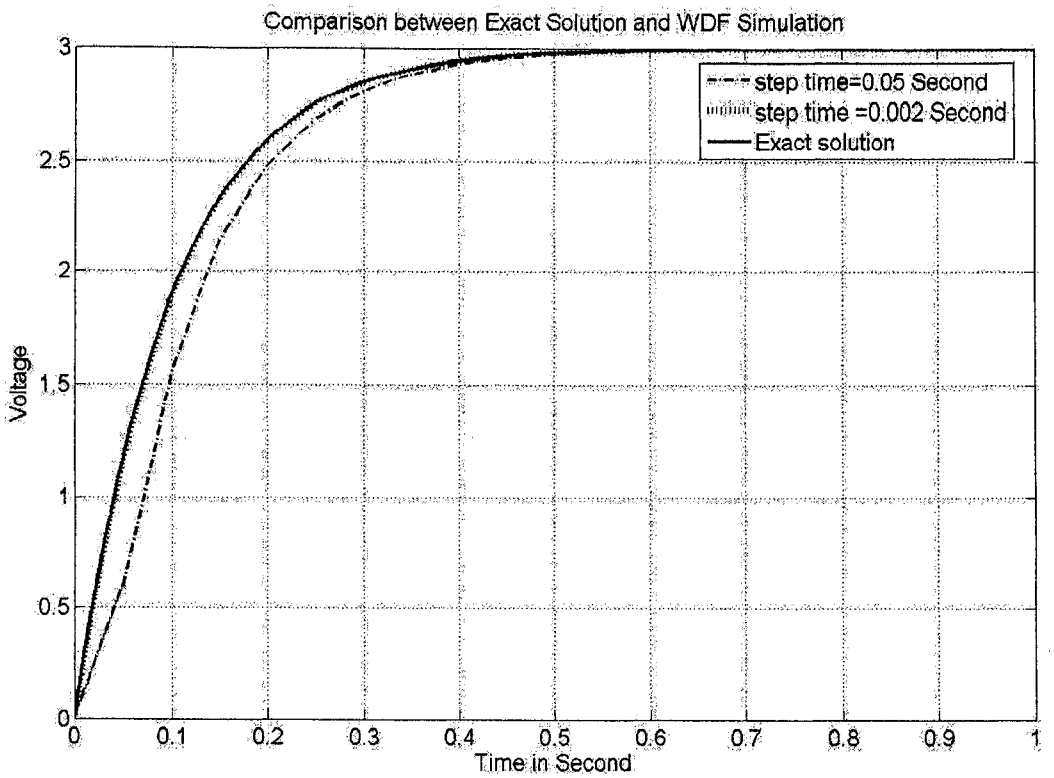

Figure 4.2: Comparison between exact solution and WDF simulation of the RC circuit

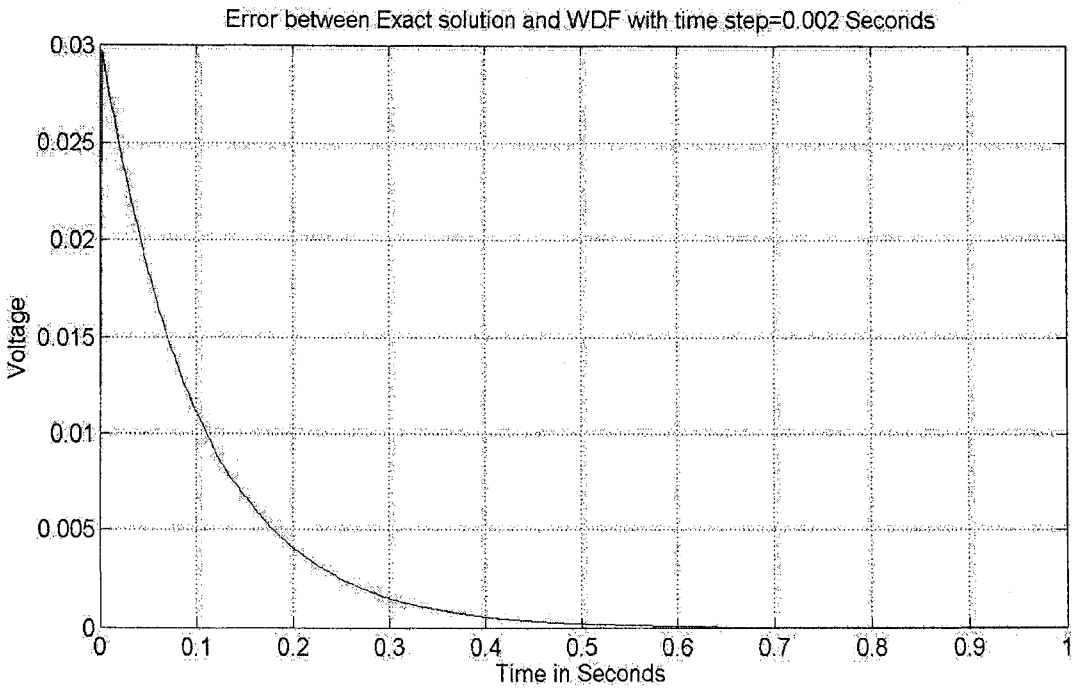

Figure 4.3: Error plot between exact solution and WDF with $T = 0.002$ s.

time as a smaller time step is applied since a smaller time step requires more sampling points.

4.3 Simulation of an Anharmonic Oscillator

An anharmonic oscillator shows chaotic behavior. It is composed of a voltage-controlled capacitance, an inductor and a resistor. The accuracy of a computer simulation of this oscillator is usually quite sensitive to the errors caused by discretization [9].

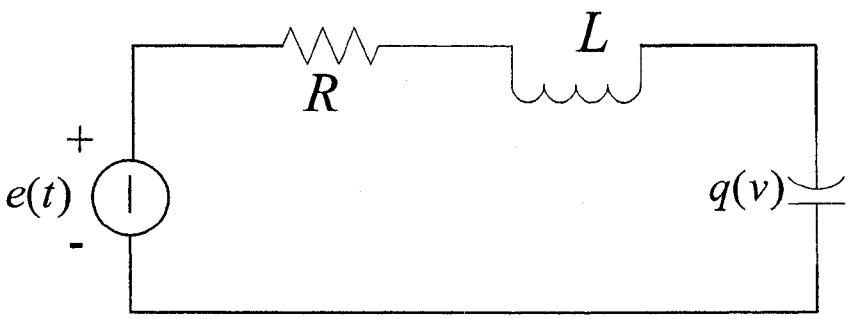

Figure 4.4: The anharmonic oscillator circuit

The following conditions are given [9]

$$q = C_0 \frac{v}{\sqrt{1+\frac{v}{v_0}}}, \qquad v > -v_0$$

$$e(t) = e_0 \sin(2\pi f_0 t), \qquad f_0 = \frac{1}{2\pi\sqrt{LC_0}}$$

$$v_0 = 0.6V, \quad R = 180\Omega, \quad L = 100uH, \quad C_0 = 80pF$$

For $v \le -v_0$ the nonlinear element behaves like an active resistive source $i = \dot{q} = (v + v_0)G$, $G > 0$. We can assume $v > -v_0$ holds throughout the simulation.

Fig. 4.5 shows the $q - v$ characteristic. In order to implement the nonlinear capacitor in the circuit, we need to map the characteristic of the nonlinear of capacitor into the wave domain by adopting the equation (2.23). This is shown in Fig. 4.6.

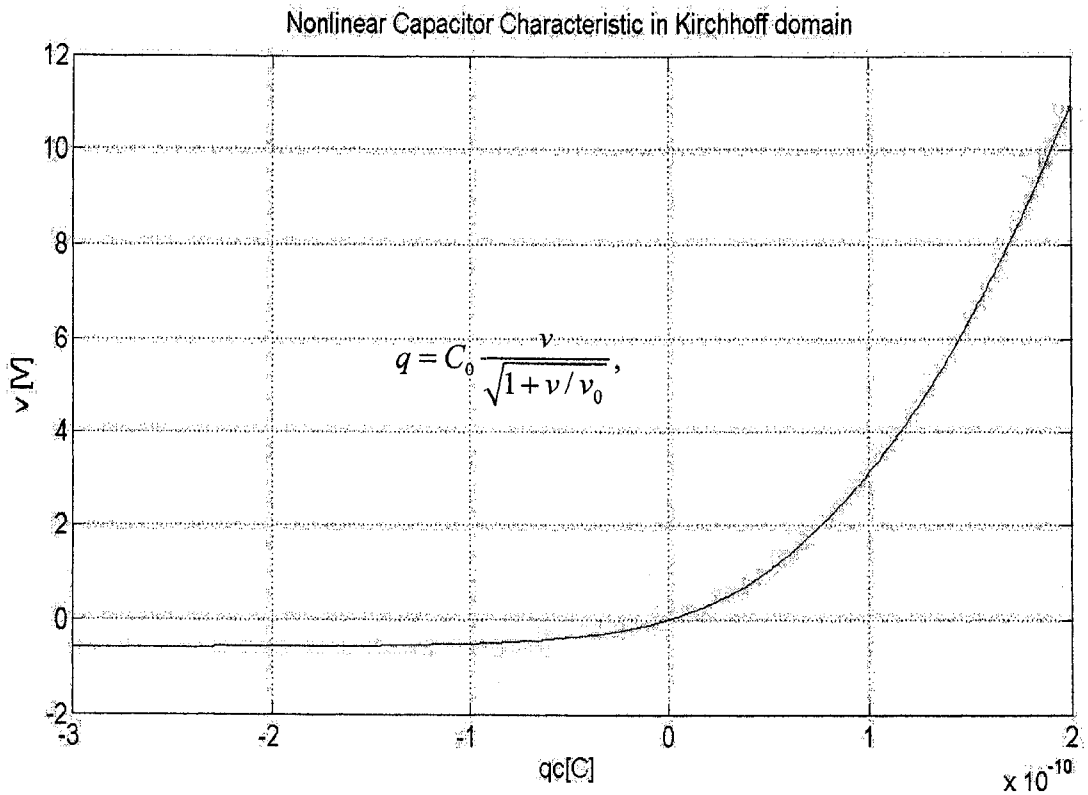

Figure 4.5: Nonlinear characteristic of the capacitor of the anharmonic oscillator in the Kirchhoff domain.

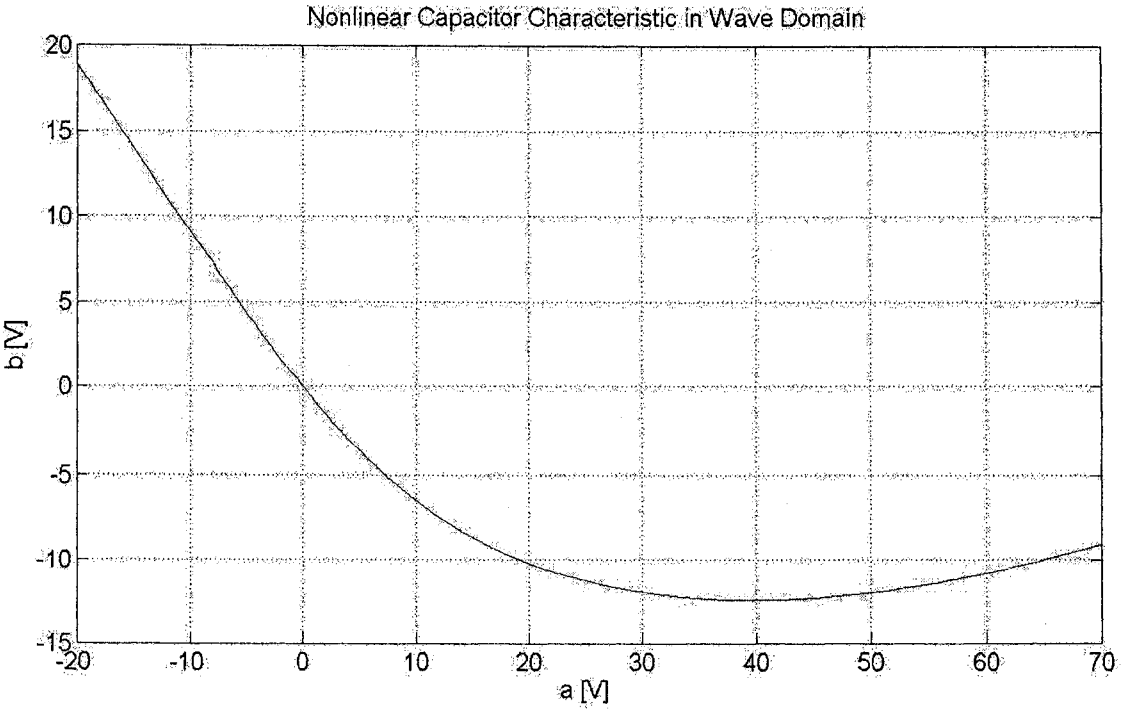

Figure 4.6: Nonlinear Characteristic of the capacitor of the anharmonic oscillator in the wave domain.

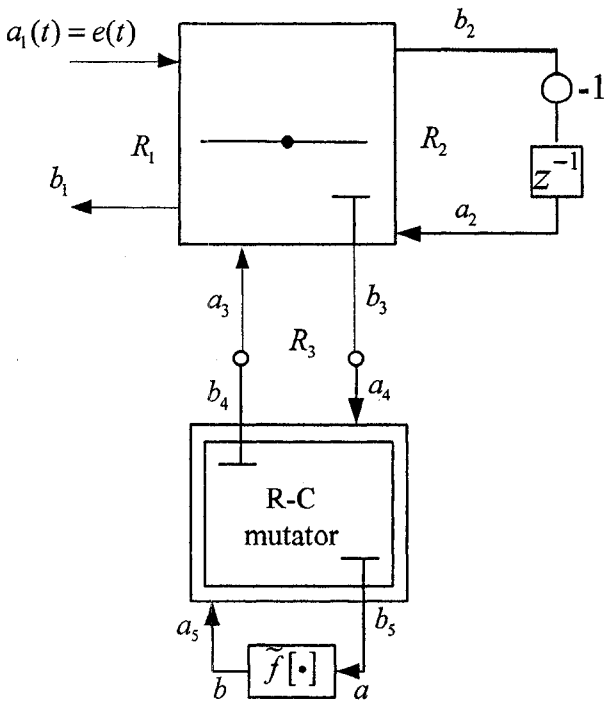

Figure 4.7: Wave implementation of the anharmonic oscillator based on instantaneous adaption.

Performing instantaneous adaption allows us to implement the linear portion of the circuit as a classical WDF structure. Fig. 4.7 shows the complete wave implementation of the oscillator. Two scattering junctions are used. One is a standard three-port series adaptor with port 3 as reflection-free. The first port resistance is set as $R_1 = R$ in order to include the resistor. The second port resistance is set as $R_2 = 2L/T$ in order to model the linear inductor as simple delay with sign change. Since the third port is reflection-free, the port resistance is set as $R_3 = R_1 + R_2$ in order to eliminate the delay-free loops with nonlinearity through the scattering junction with memory. The second scattering junction is R-C mutator whose transfer function is $K = z^{-1}$. In order for this to be true, we need to let

$$R_3 = \frac{T}{2C} \Rightarrow C = \frac{T}{2R_3} = \frac{T/2}{R + 2L/T}$$

where C is the reference capacity that is used to determine the wave equivalent of the nonlinear characteristic of the capacitor. To find the reflected wave at the port of a nonlinear element, a linear interpolation is adopted. The data points for the linear

interpolation are obtained according to the following procedure.

- Obtain all the possible combinations of a nonlinear element in Kirchhoff domain (Fig. 4.5)
- Obtain all the combinations of the incident wave and reflected wave by mapping the nonlinear characteristic of a nonlinear elements in Kirchhoff domain into the wave domain (Fig. 4.6)

The following equations are the WDF analysis of the nonlinear circuit.

$$C = \frac{T}{2R_3} = \frac{T/2}{R + 2L/T}$$

$$\beta_1 = \frac{R}{R + 2L/T}$$

$$a_1(t_j) = e(t_j)$$

$$a_2(t_j) = -b_2(t_{j-1})$$

$$b_3(t_j) = -a_1(t_j) - a_2(t_j)$$

$$a_4(t_j) = b_3(t_j)$$

$$b_5(t_j) = a_4(t_j) + a_4(t_{j-1}) - a_5(t_{j-1})$$

$$a(t_j) = b(t_j)$$

$$b(t_j) = \tilde{f}[a(t_j)]$$

$$a_5(t_j) = b(t_j)$$

$$b_4(t_j) = a_5(t_j) + a_4(t_{j-1}) - a_5(t_{j-1})$$

$$a_3(t_j) = b_4(t_j)$$

$$b_2(t_j) = \beta_1(a_1(t_j) + a_2(t_j) + a_3(t_j)) - a_1(t_j) - a_3(t_j)$$

$$b_1(t_j) = a_1(t_j) - \beta_1(a_1(t_j) + a_2(t_j) + a_3(t_j))$$

$$i(t_j) = \frac{a_2(t_j) - b_2(t_j)}{4L/T}$$

$$q(t_j) = \frac{a(t_j) - b(t_j)}{2/C}$$

The simulations are implemented in Matlab. The time steps are set to be $T=1/(32f_0)$ and $T=1/(128f_0)$. The voltage generator amplitude is set to $e_0 = 3.57V$. Fig. 4.8 and Fig. 4.9 show the phase portraits of the anharmonic oscillator obtained with WDF simulation. Fig. 4.10 and Fig. 4.11 show the phase portraits of the

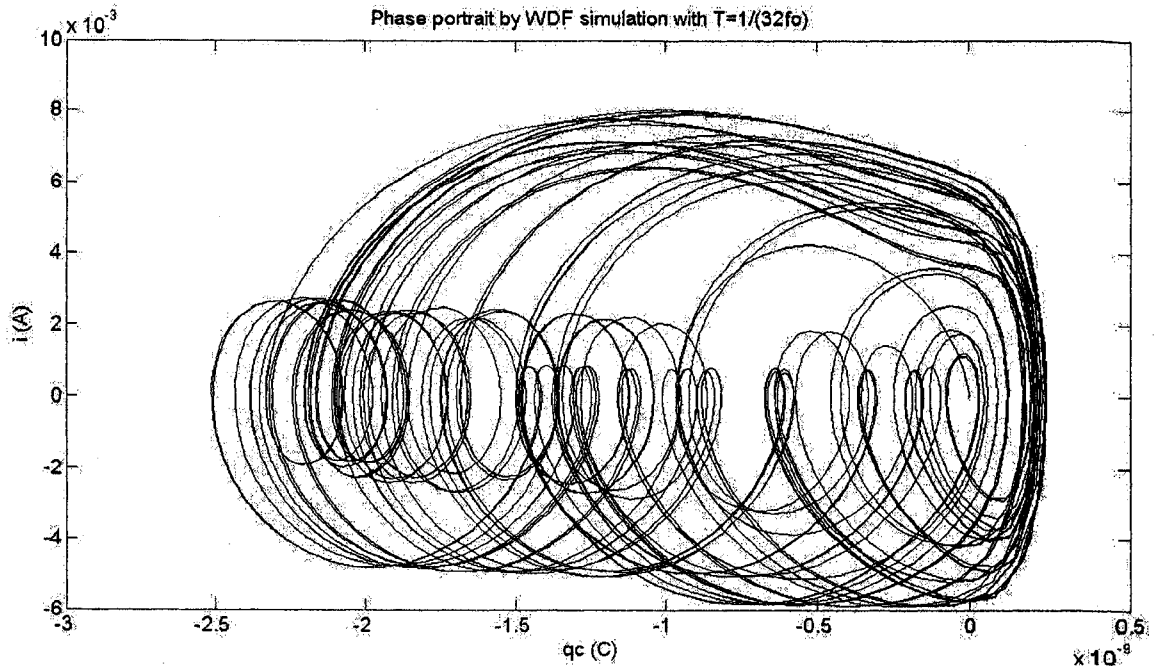

Figure 4.8: Phase portrait of $e_0 = 3.57V$ using R-C mutator and $T=1/(32f_0)$

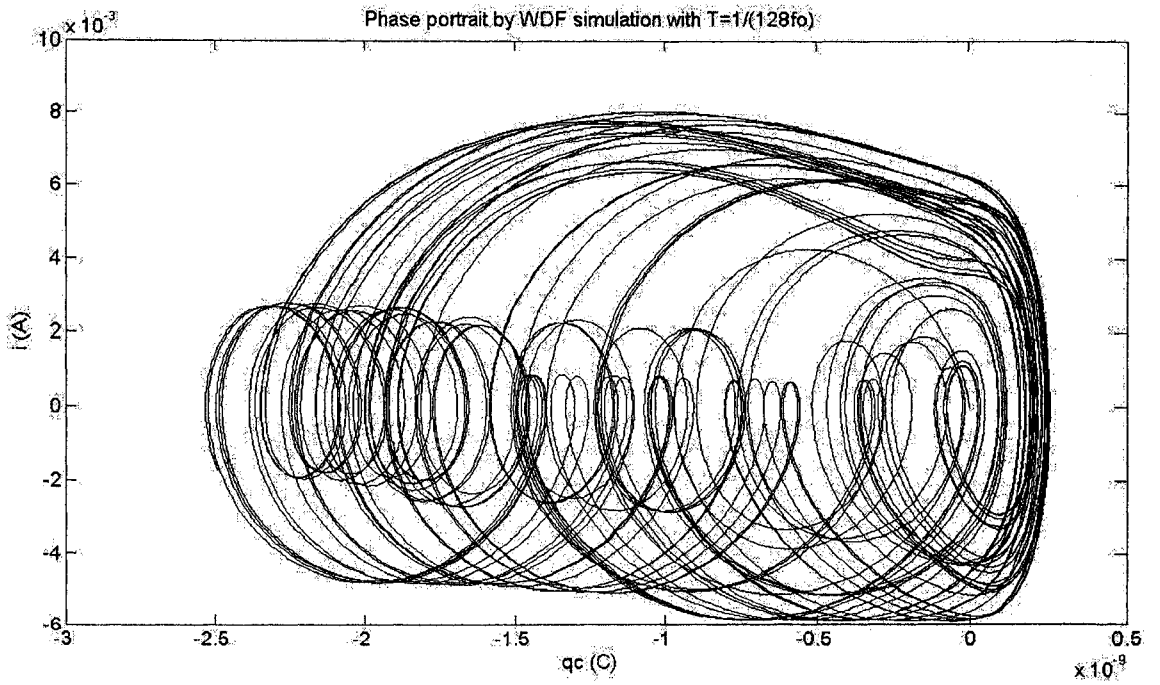

Figure 4.9: Phase portrait of $e_0 = 3.57V$ using R-C mutator and $T=1/(128f_0)$.

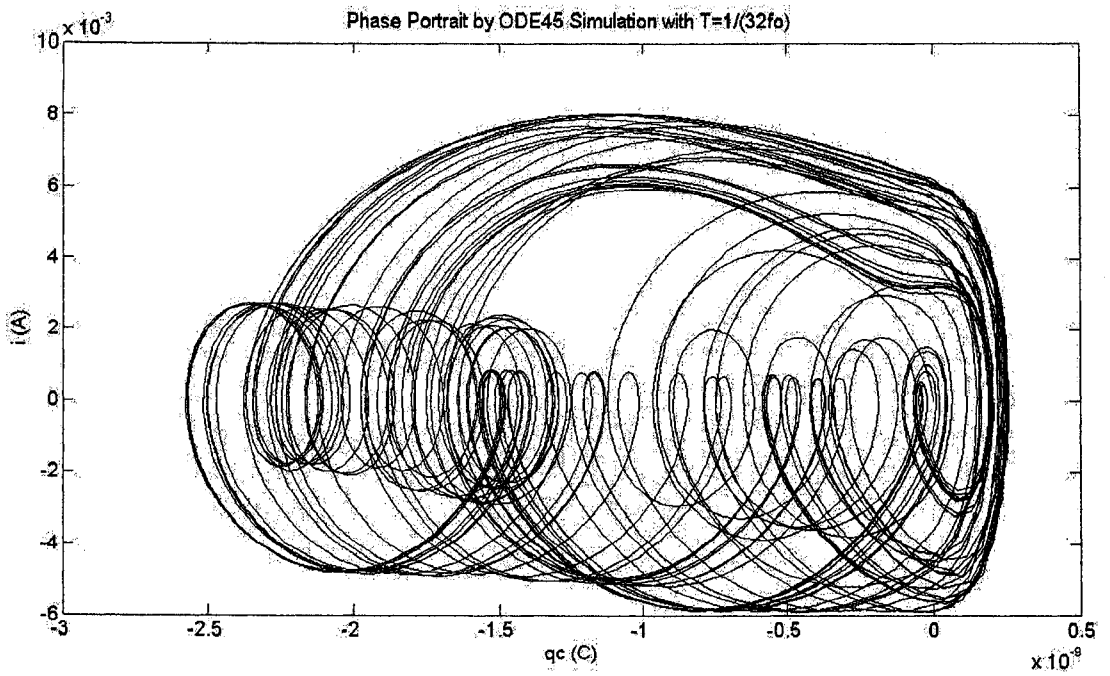

Figure 4.10: Phase portrait of $e_0 = 3.57V$ using ODE45 and $T=1/(32f_0)$.

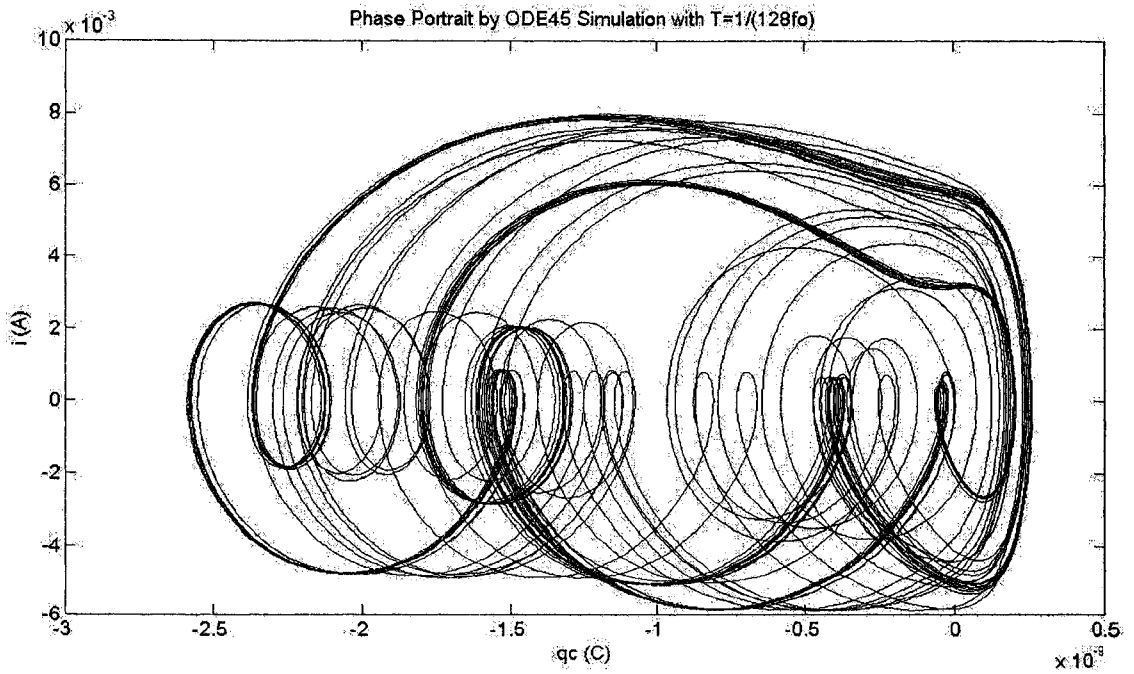

Figure 4.11: Phase portrait of $e_0 = 3.57V$ using ODE45 and $T=1/(128f_0)$.

anharmonic oscillator obtained with ODE45 simulation. The different time step sizes are used to see if the result is independent of the chosen time step.

WDF and ODE45 simulations use different integration methods. WDF uses the trapezoidal rule as the integration, while ODE45 uses the Runge-Kutta method. The circuit is very sensitive to the integration methods. Different simulation results are obtained by using different methods.

For the WDF simulation, we only find small differences for $e_0 = 3.57V$ when we change the operating period from $T=1/(32f_0)$ to $T=1/(128f_0)$. These observations are shown in Figs. 4.8 and 4.9.

As we can see from Figs. 4.10 and 4.11, the ODE45 simulation results show larger differences when the operating period is changed from $T=1/(32f_0)$ to $T=1/(128f_0)$. We can conclude that WDF simulation produces consistent results with a wider range of time-step values compared to traditional integration methods.

Comparing both simulation results with the results in [9] for $T=1/(32f_0)$, none of the results are exactly same. But WDF simulation is more similar. Possible reasons for the difference between WDF simulation and results in [9] are that different samples are chosen in the look-up tables and also different interpolation methods are used. The anharmonic oscillator is very sensitive to the step and range of the look-up table.

4.4 Modeling and Simulation of an LC VCO Circuit

It is very difficult to simulate the original LC VCO circuit by WDF principles since the models of the MOS transistor contain many nonlinear elements. However, the circuit can be simplified. As we know, the combination of NMOS and PMOS transistors generates a negative resistance from the two pairs of MOS transistors.

Fig. 4.12 shows the circuit setup which is used to obtain the $i-v$ characteristic of the nonlinear resistance. The characteristic in Fig. 4.13 is obtained by performing a DC sweep in Spectre. The applied DC sweep voltage is from $-1.8V$ to $1.8V$.

The characteristic shown in Fig. 4.13 can be approximated by the following equation,

$$i(v) = -0.0024 \sin\left(\frac{2\pi v}{3.6}\right) \tag{4.1}$$

Equation (4.1) shows the approximation of the nonlinear voltage-controlled current source in Fig. 4.13. The plot of the nonlinear voltage-controlled current source in Matlab according to Equation (4.1) is shown in Fig. 4.14.

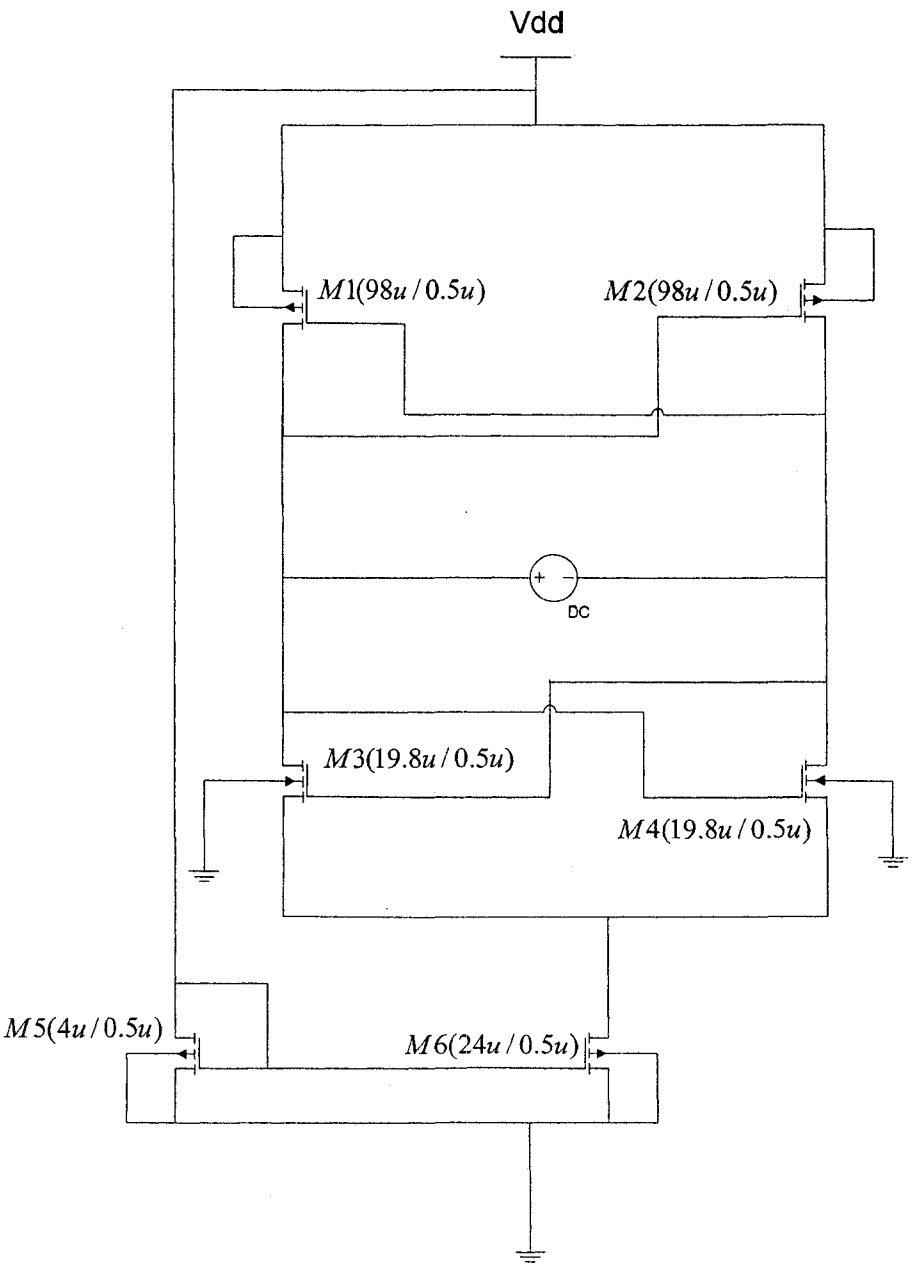

Figure 4.12: Determination of the nonlinear resistor

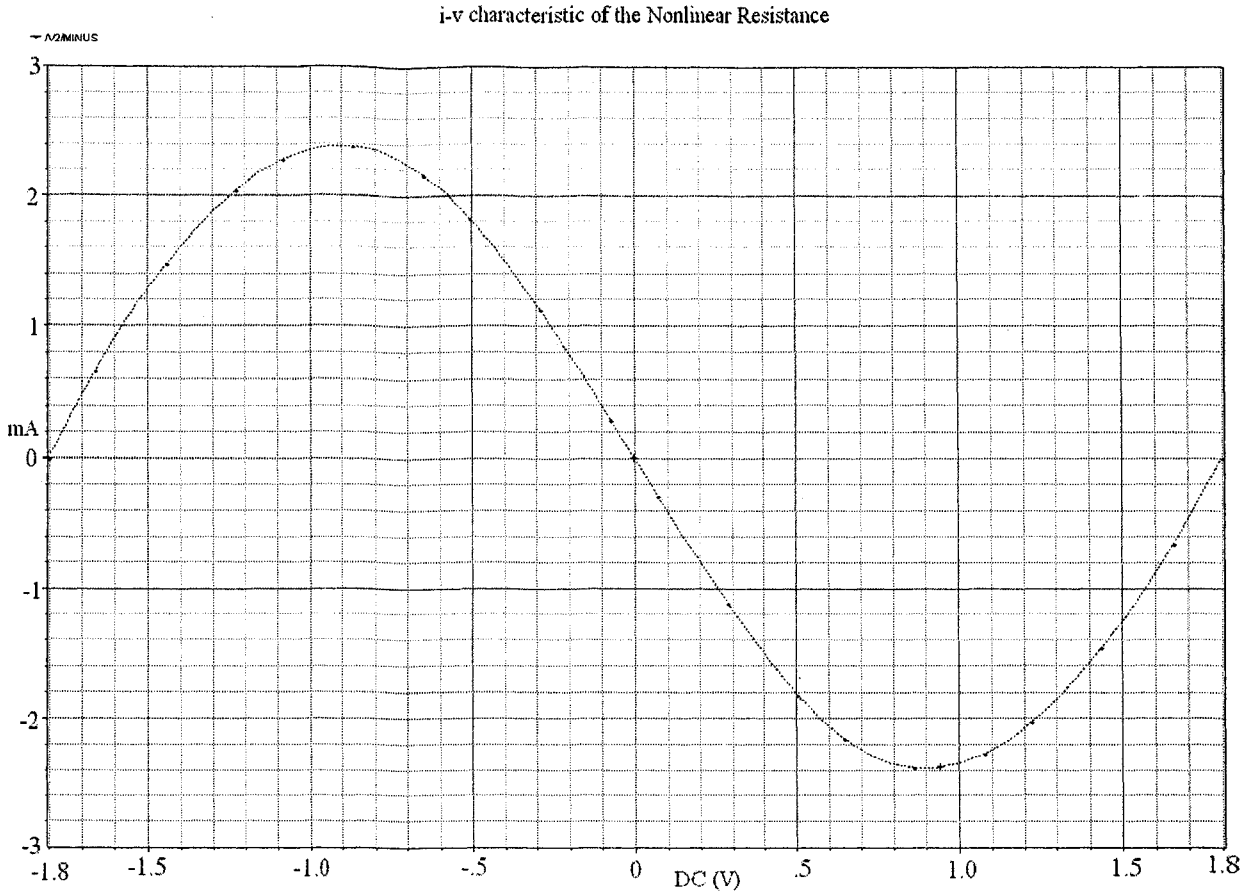

Figure 4.13: $i - v$ characteristic of the nonlinear resistance using approximation

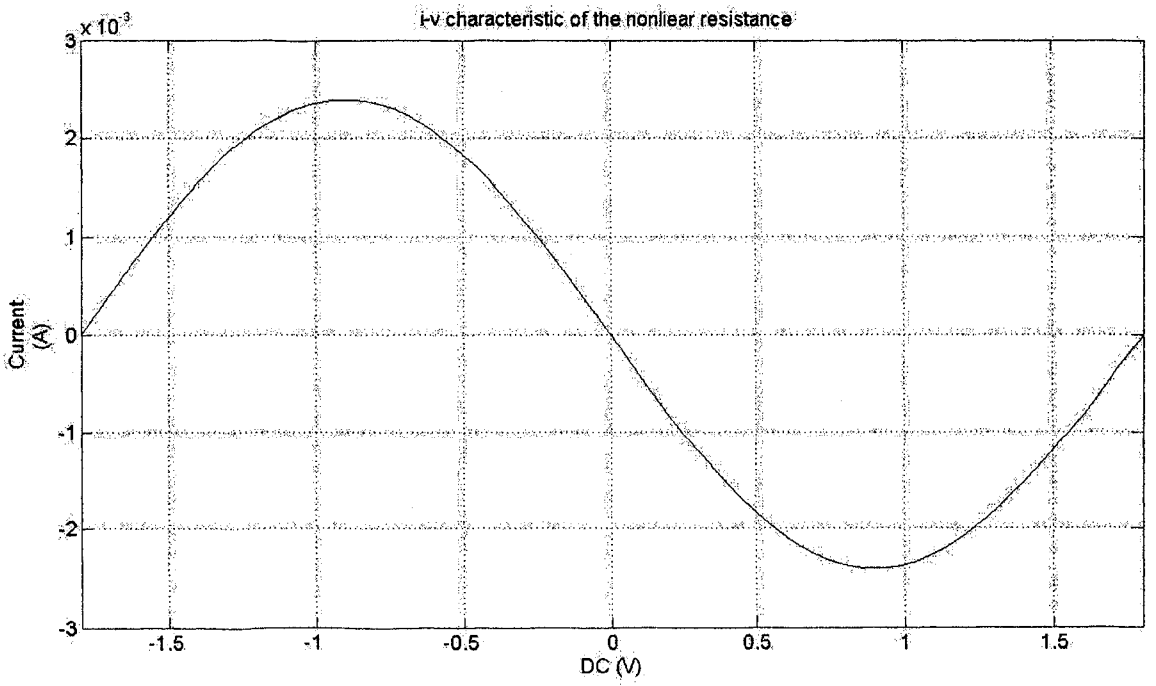

Figure 4.14: The i-v characteristic of the nonlinear resistance using Matlab

4.4.1 Simulation with Simple Inductor Model

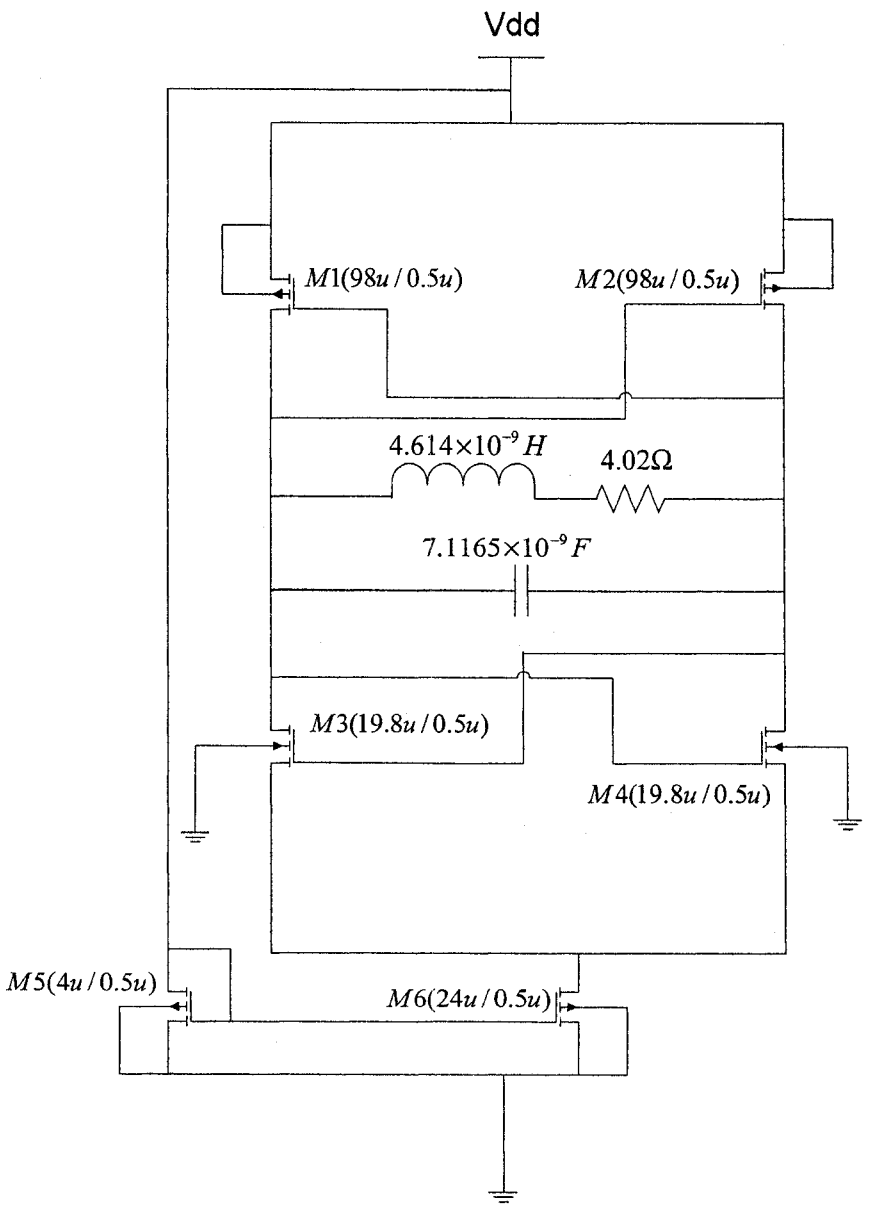

Figure 4.15: The circuit performed in Spectre

The circuit shown in Fig. 4.12 has parasitic capacitances from the NMOS and PMOS transistors that can affect the simulation results. It is important to obtain the exact value of the total parasitic capacitance. In Fig. 4.15, the value of the capacitor is arbitrary. The models of the inductor are replaced by an ideal inductor in series with a resistor. The simulation results of Fig. 4.15 performed in Spectre are used to calculate the total capacitance and total parasitic capacitance in Fig. 4.15. The simulation is shown in Fig. 4.16. The simulated frequency in Fig. 4.16 is 2.215 GHz. The peak value of the voltage is 1.7 V. The equations used to calculate the total capacitance and

total parasitic capacitance are shown as the following:

$$C_{total} = \frac{1}{(2\pi f)^2 L}$$
$$C_{parasitic} = C_{total} - C_{cap} \tag{4.2}$$

where C_{total}, $C_{parasitic}$ and C_{cap} are the total capacitance, total parasitic capacitance and capacitor value in Fig. 4.15 respectively. According to the above equations, the calculated values of the capacitances are:

$$C_{total} \cong 1.118962 \times 10^{-12} F$$
$$C_{parasitic} \cong 4.07312 \times 10^{-13} F$$

Since the equation of the nonlinear resistance and the total capacitance are obtained, the LC VCO circuit in Fig. 4.15 can be simplified to the ideal circuit shown in Fig. 4.17. N_R represents the nonlinear resistance composed of the cross-coupled NMOS and PMOS transistors that are shown in Fig. 4.12. Equation (4.1) is the equation that relates voltage and current in the resistor. The capacitor value in Fig. 4.17 is the total capacitance in Fig. 4.15. The values of other components are shown in Fig. 4.17.

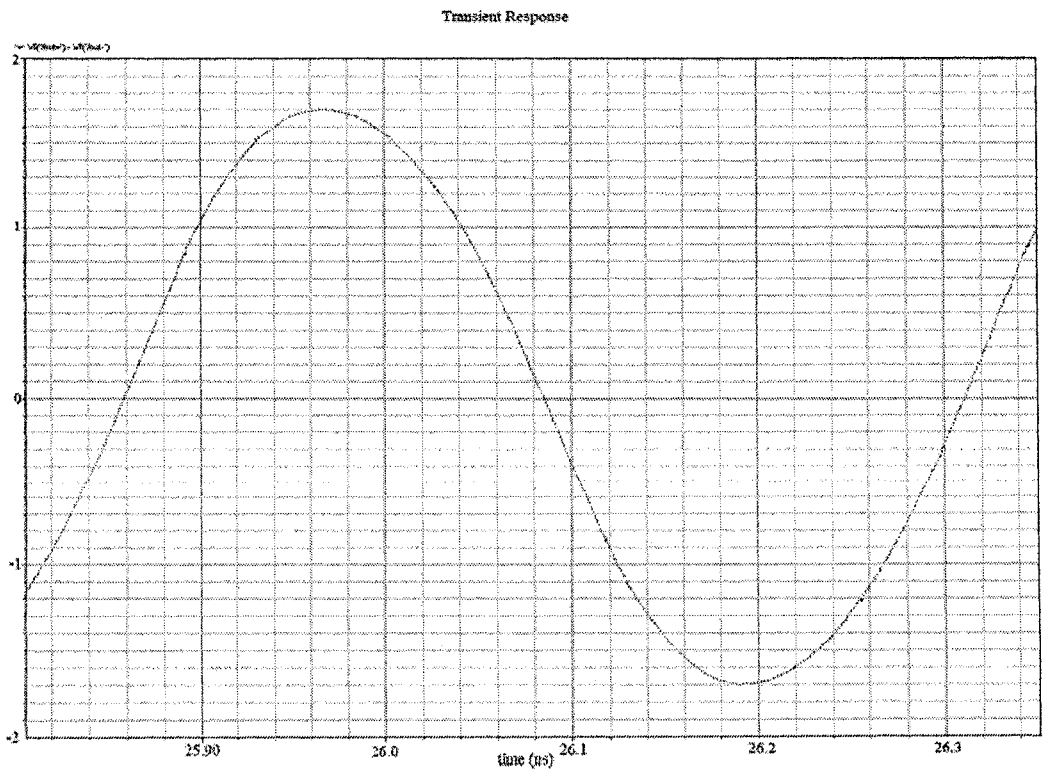

Figure 4.16: Simulation of Fig. 4.15 in Spectre

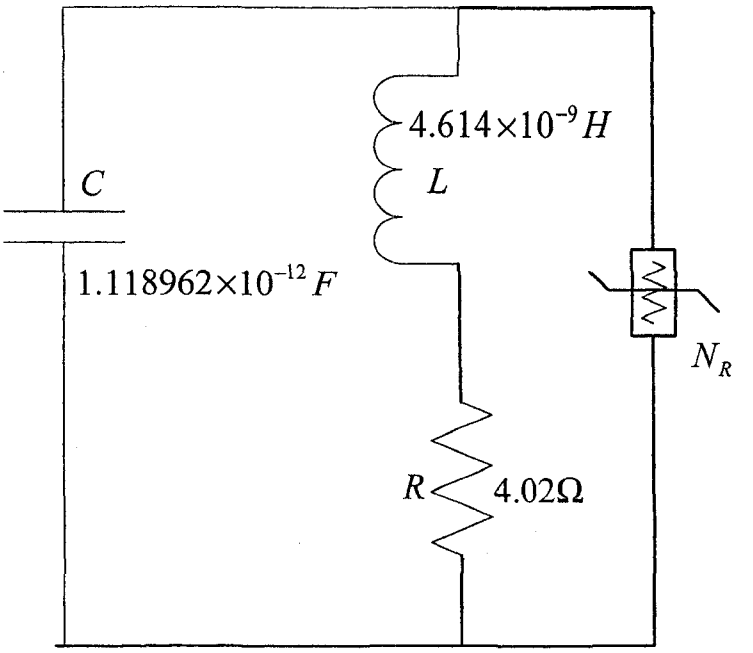

Figure 4.17: the simplified circuit of the LC VCO

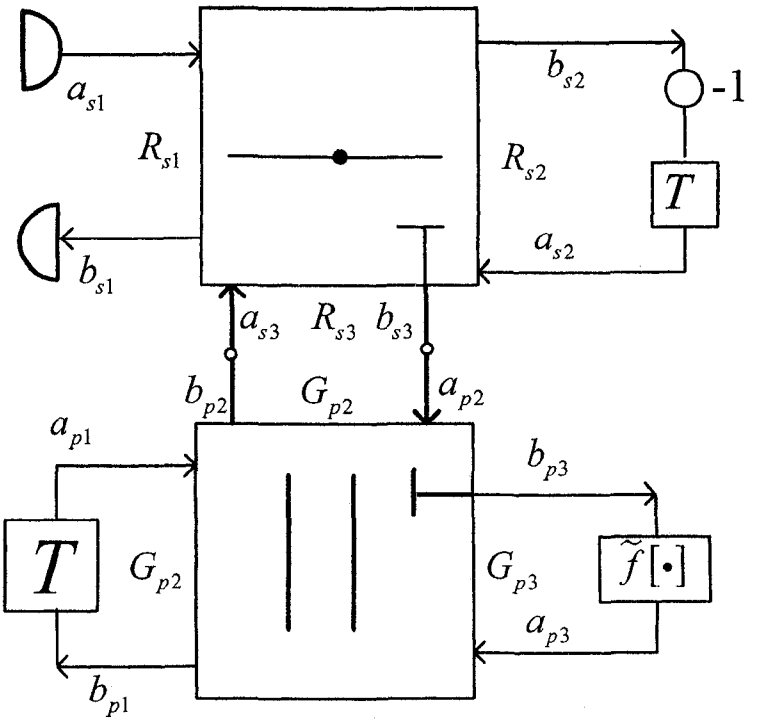

Figure 4.18: WDF implementation of the LC VCO circuit in Fig. 4.15.

Figure 4.18 shows the WDF implementation of the LC VCO simplified circuit in Fig. 4.17. For the nonlinear resistance, the transformation that defines the incident and reflected waves as a function of voltage and current is used for mapping the characteristic of a nonlinear resistor onto the WDF domain. The following equations are the WDF analysis of the simplified circuit,

$$G_{p3} = G_{p1} + G_{p2}$$

$$\alpha_1 = \frac{G_{p1}}{G_{p1} + G_{p2}}$$

$$R_{s3} = R_{s1} + R_{s2}$$

$$\beta_1 = \frac{R_{s1}}{R_{s1} + R_{s2}}$$

$$a_{s1}(t_j) = 0$$

$$a_{s2}(t_j) = -b_{s2}(t_{j-1})$$

$$b_{s3}(t_j) = -a_{s1}(t_j) - a_{s2}(t_j)$$

$$a_{p2}(t_j) = b_{s3}(t_j)$$

$$a_{p1}(t_j) = b_{p1}(t_{j-1})$$

$$b_{p3}(t_j) = \alpha_1 \cdot a_{p1}(t_j) + a_{p2}(t_j) \cdot (1 - \alpha_1)$$

$$a_{p3}(t_j) = \tilde{f}\left[b_{p3}(t_j)\right]$$

$$b_{p2}(t_j) = \alpha_1 \cdot \left[a_{p1}(t_j) - a_{p2}(t_j)\right] + a_{p3}(t_j)$$

$$a_{s3}(t_j) = b_{p2}(t_j)$$

$$b_{s2}(t_j) = (\beta_1 - 1) \cdot a_{s1}(t_j) + \beta_1 \cdot a_{s2}(t_j) + (\beta_1 - 1) \cdot a_{s3}(t_j)$$

$$b_{p1}(t_j) = (\alpha_1 - 1) \cdot a_{p1}(t_j) + (1 - \alpha_1) \cdot a_{p2}(t_j) + a_{p3}(t_j)$$

$$V_c = \frac{a_{p1}(t_j) + b_{p1}(t_j)}{2}$$

Figure 4.19 shows the comparison between the ODE45 and WDF simulations. In both simulations, the time steps are equal to 10 ps. As we can see from Fig.4.19, the result of WDF simulation is very close to that of ODE45 simulation. Both simulations are implemented in Matlab. The oscillating frequency in Fig. 4.18 is 2.208 GHz. The peak voltage is 1.707 V. As a comparison with the simulation result from Spectre in Fig. 4.16, the error of the two frequencies is 0.316%, and the error of the two peak voltages is 0.412%.

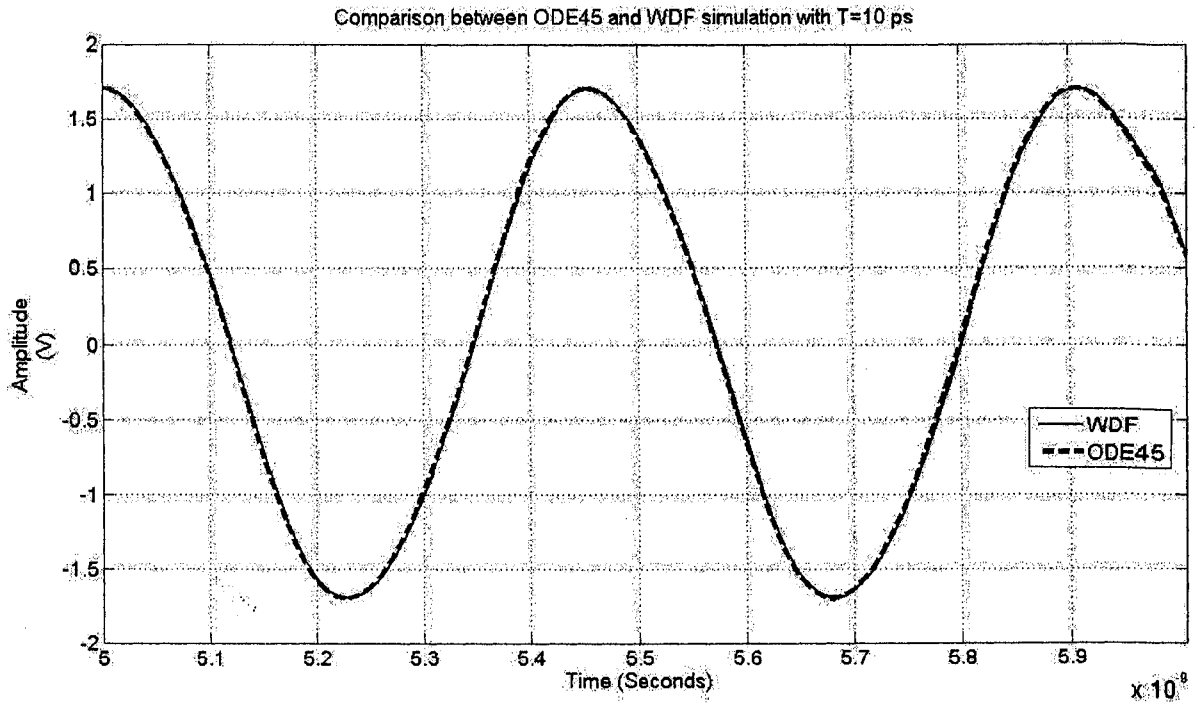

Figure 4.19: Comparison between ODE45 and WDF simulations of the LC VCO simplified circuit

4.4.2 Simulation with Detailed Inductor Model

Since the LC VCO has two spiral inductors connected in symmetrical form, the simplified circuit in Fig. 4.20 employs the equivalent models of the two spiral inductors in symmetrical form. The series and parallel adaptors are not enough to describe the connections of the two equivalent models of the spiral inductors. But the connections can be described as a bridge circuit which is introduced in Chapter 2. The capacitor value is the total capacitance of the measured value of the varactors at 0.5 V and the parasitic capacitance obtained from equations (4.2). This capacitor value makes the comparison between WDF simulation of Fig. 4.20 and the simulation results of the LC VCO at 0.5 V in Fig. 3.15.

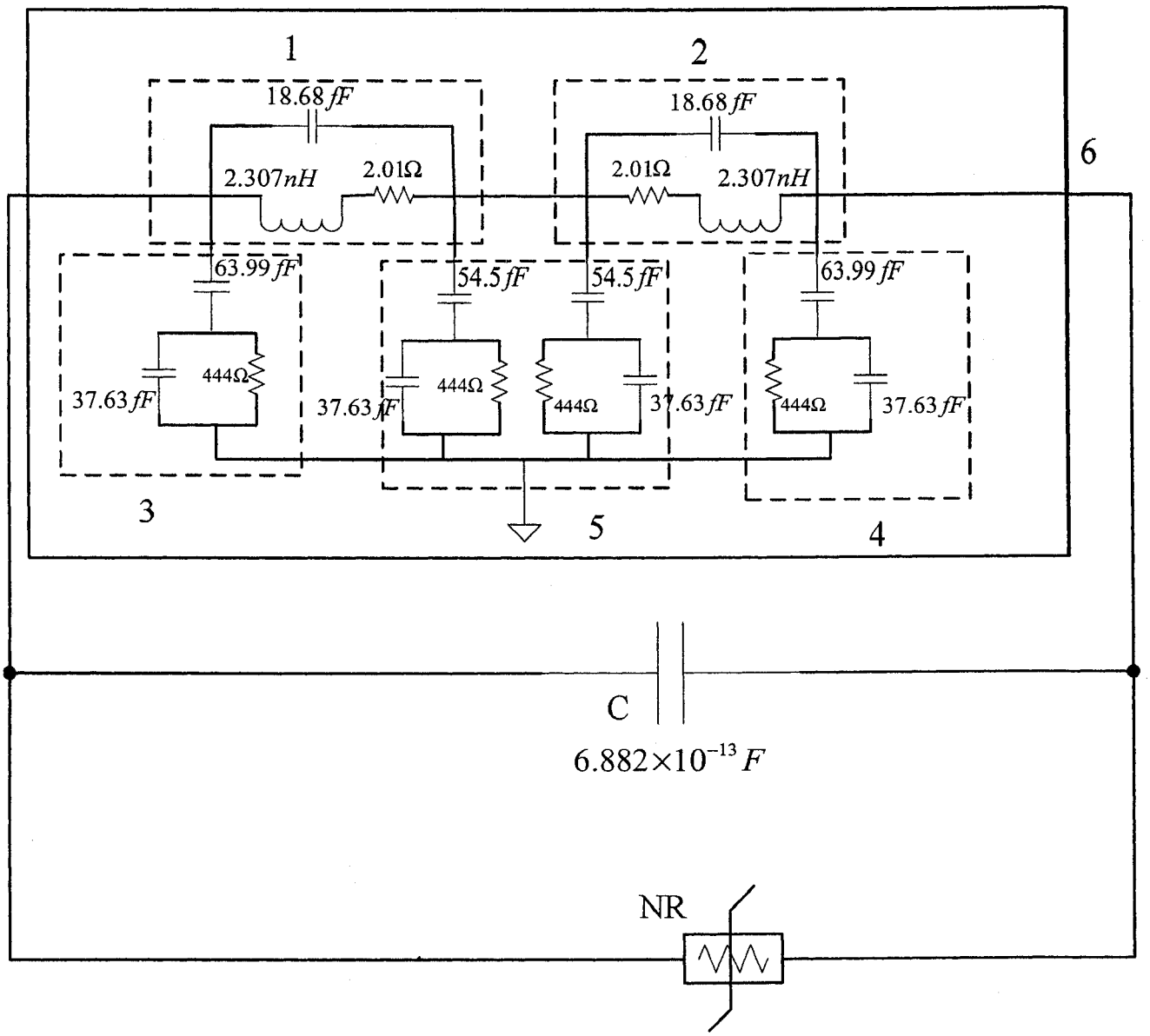

Figure 4.20: Model of the LC VCO with equivalent models of spiral inductors

As shown in Fig. 4.20, the connections of the equivalent models are divided into 6 parts which represent 6 ports of the bridge circuit. The port resistance of each port can be obtained by using regular series and parallel adaptors. In Fig. 4.20, Part 1 and Part 2 have the same topology. Part 3 and Part 4 are same. Part 6 is the port which is in parallel with the capacitor and nonlinear resistance. The following will show how to obtain the port resistance, incident wave and reflected wave by combining the components of each part.

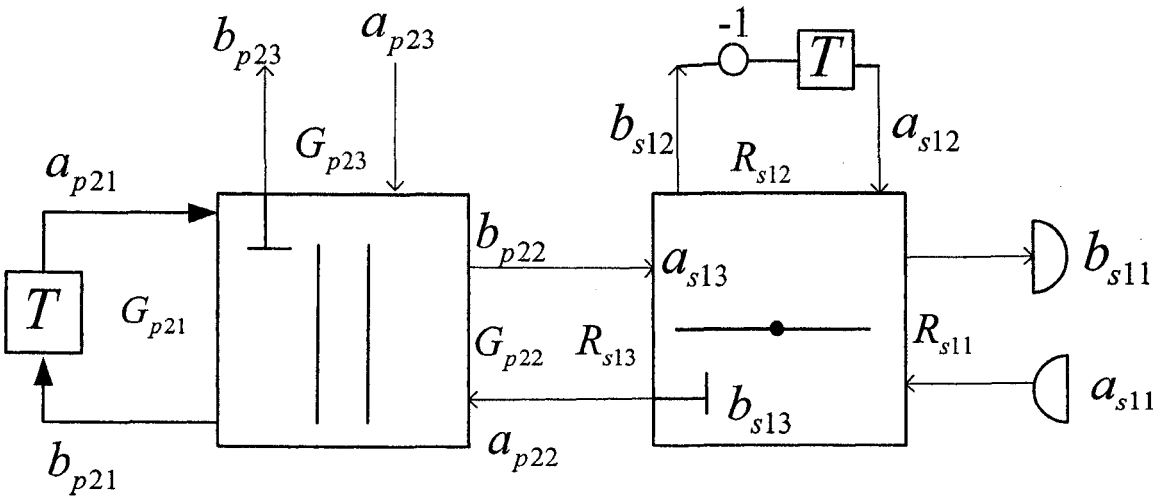

Figure 4.21: The WDF implementation for Part 1 and Part 2

Fig.4.21 shows the implementation of Part 1 and Part 2 by WDF principles. The details of the WDF analysis are shown in Appendix B.1.

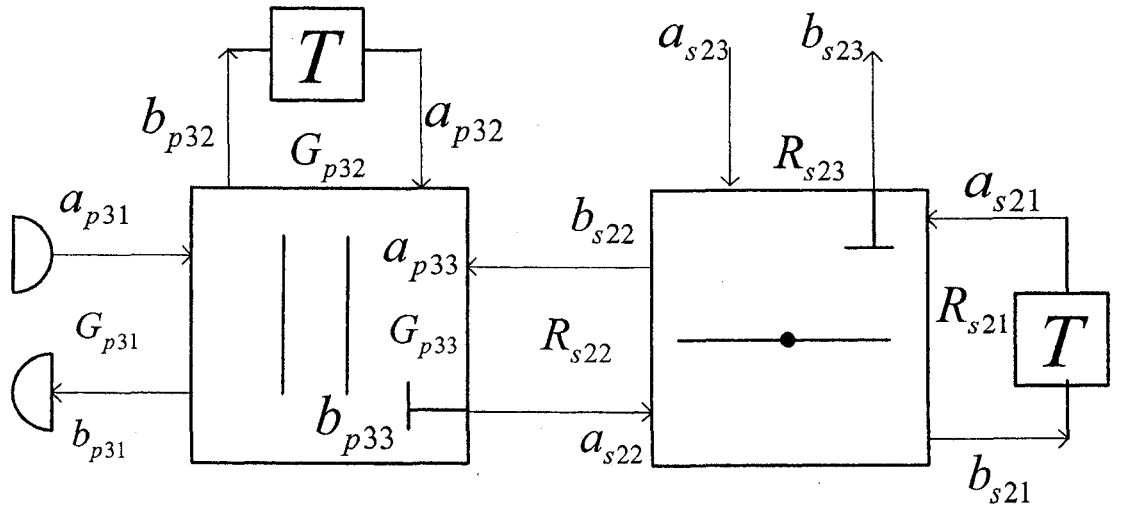

Figure 4.22: The WDF implementation for Part 3 and Part 4

Fig. 4.22 shows the WDF implementation of Part 3 and Part 4. The equations of the WDF analysis of Fig. 4.21 are shown in Appendix B.2,

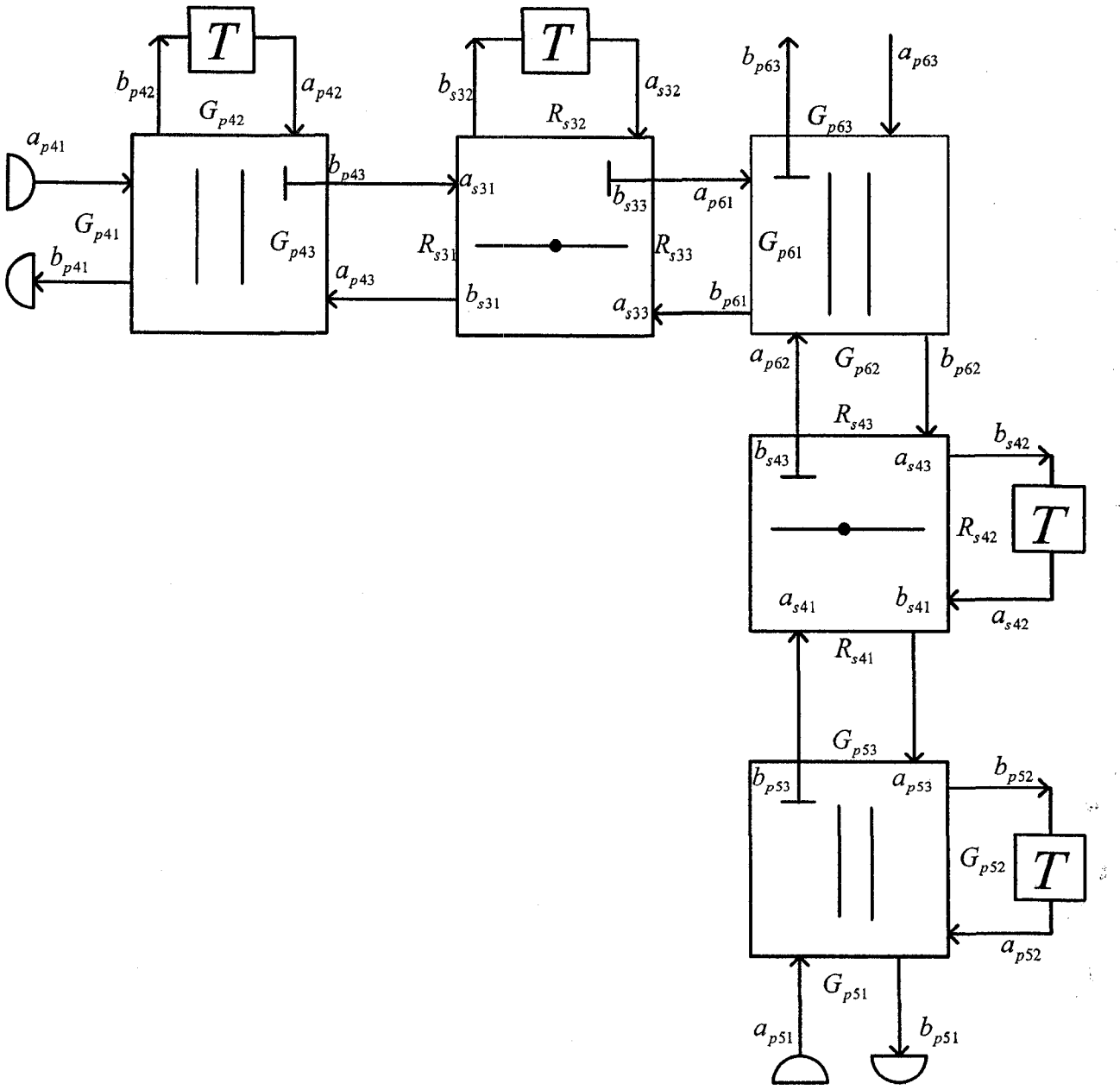

Figure 4.23: The WDF implementation for Part 5

Fig. 4.23 shows the WDF implementation of Part 5. The equations of the WDF analysis of Part 5 are shown in Appendix B.3.

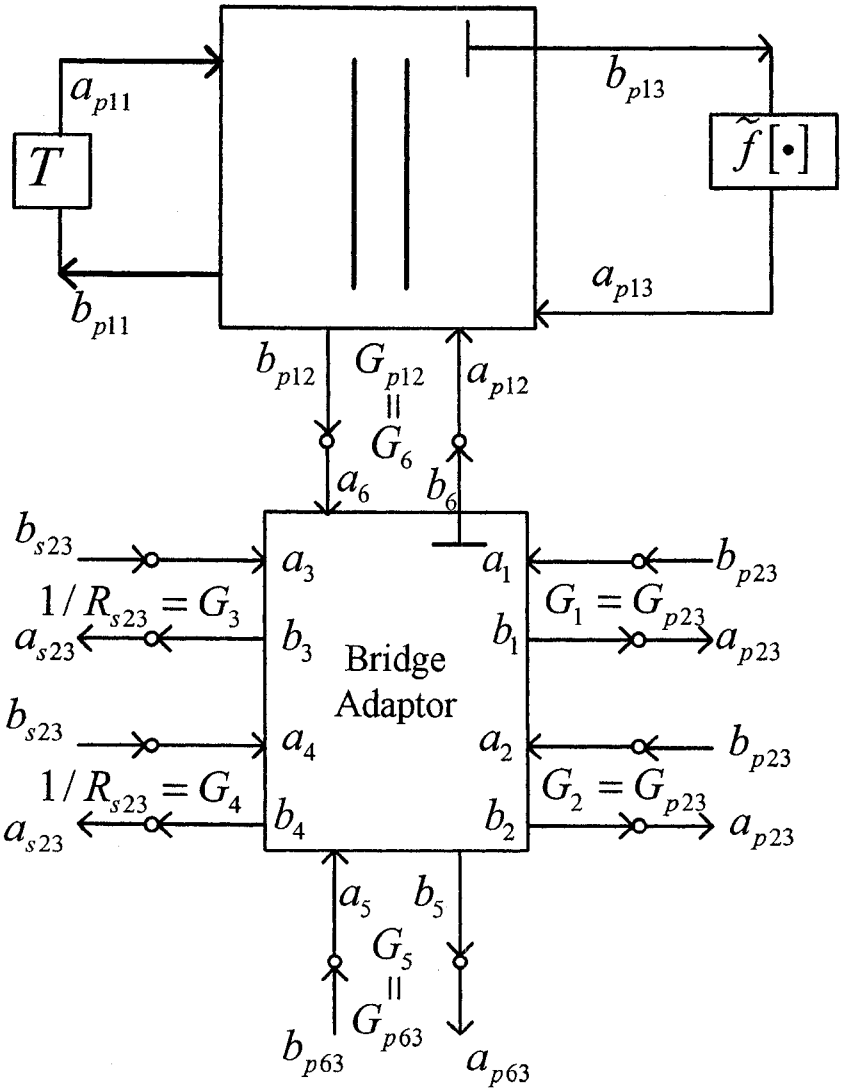

Figure 4.24: The WDF implementation for the LC VCO with equivalent inductor models

By applying the WDF principles to the five parts, we obtain the incident wave and port resistance of the five ports of the bridge adaptor. The detailed connections are shown in Fig. 4.24. As we can see from the figure, the port resistance of Port 6 and the reflected waves of the six ports are unknown. To obtain the reflected waves, the scattering matrix of the bridge adaptor must be obtained by the principles introduced in Chapter 2. The port resistance of Port 6 is very important since only the right port resistance can make Port 6 to be a reflection-free port (i.e., $S_{66} = 0$). In other words, the right port resistance makes the reflected wave of Port 6 depend on only the other five ports in order to avoid delay-free loops.

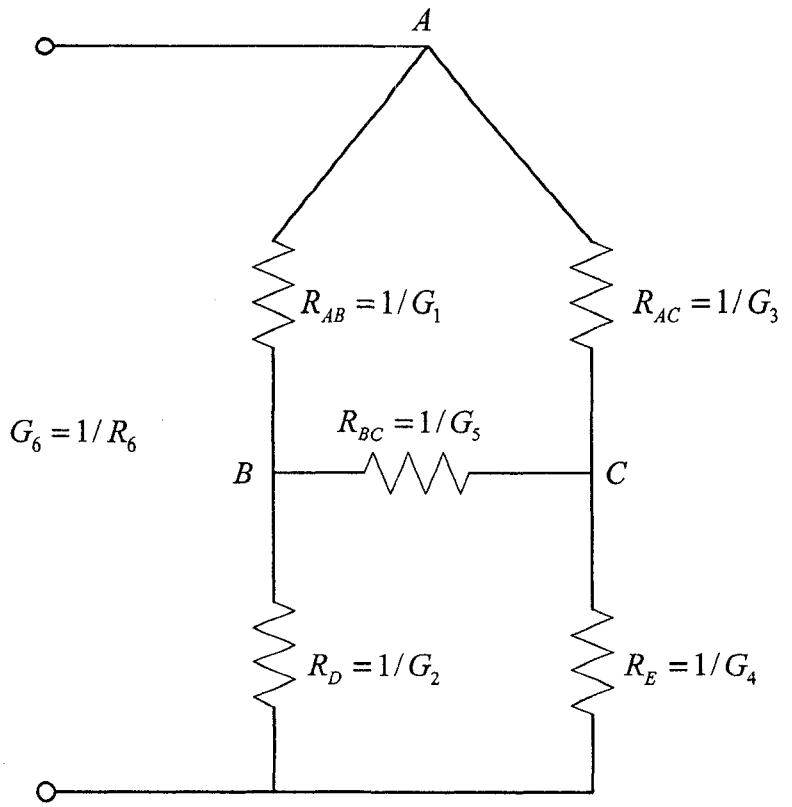

Figure 4.25: The bridge circuit with Δ connection

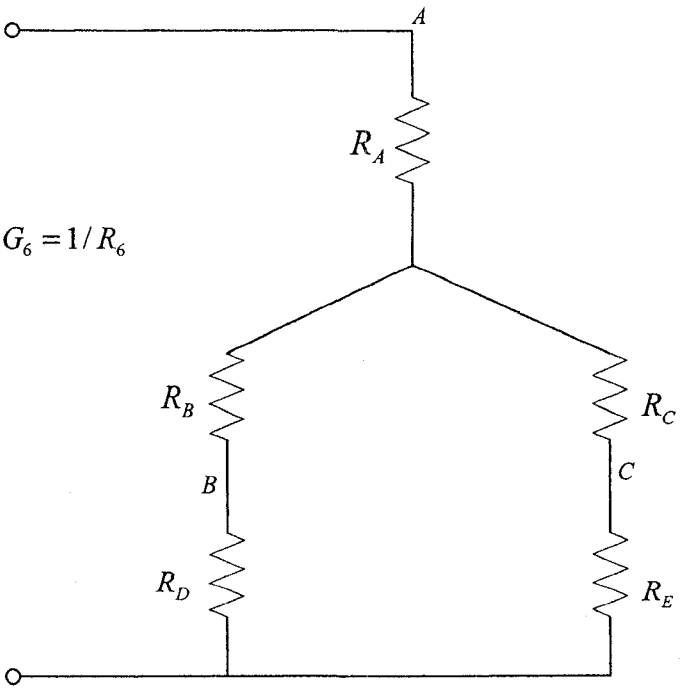

Figure 4.26: The bridge circuit with Y connection

To obtain the port resistance of Port 6, a Δ to Y transformation is used. Fig. 4.25 shows the bridge circuit with Δ connection. R_6 is the total resistance of the bridge circuit. According to Δ-Y conversion, the circuit can be redrawn as Fig. 4.26. The following equations show the details of the conversion.

$$R_A = \frac{R_{AB} \cdot R_{AC}}{R_{AB} + R_{AC} + R_{BC}}$$

$$R_B = \frac{R_{AB} \cdot R_{BC}}{R_{AB} + R_{AC} + R_{BC}}$$

$$R_C = \frac{R_{AC} \cdot R_{BC}}{R_{AB} + R_{AC} + R_{BC}}$$

$$R_6 = \frac{(R_B + R_D) \cdot (R_C + R_E)}{(R_B + R_D) + (R_C + R_E)} + R_A$$

The wiring diagram of the bridge circuit is shown in Fig. 4.27. The equation of the scattering matrix is the same as equation (2.18). But the currents and voltages references are different. The details are given as,

$$\underline{S} = -\begin{bmatrix} \underline{M_V} \\ -\underline{M_I}\,\underline{G} \end{bmatrix}^{-1} \begin{bmatrix} \underline{M_V} \\ \underline{M_I}\,\underline{G} \end{bmatrix}$$

$$\underline{M_V} = \begin{bmatrix} 1 & 1 & 0 & 0 & 0 & -1 \\ 1 & 0 & -1 & 0 & 1 & 0 \\ 0 & -1 & 0 & 1 & 1 & 0 \end{bmatrix}$$

$$\underline{M_I} = \begin{bmatrix} 1 & 0 & 1 & 0 & 0 & 1 \\ 0 & -1 & 0 & -1 & 0 & -1 \\ 0 & 0 & 1 & -1 & 1 & 0 \end{bmatrix}$$

$$\underline{G} = diag(G_1, \quad \cdots \quad , G_6)$$

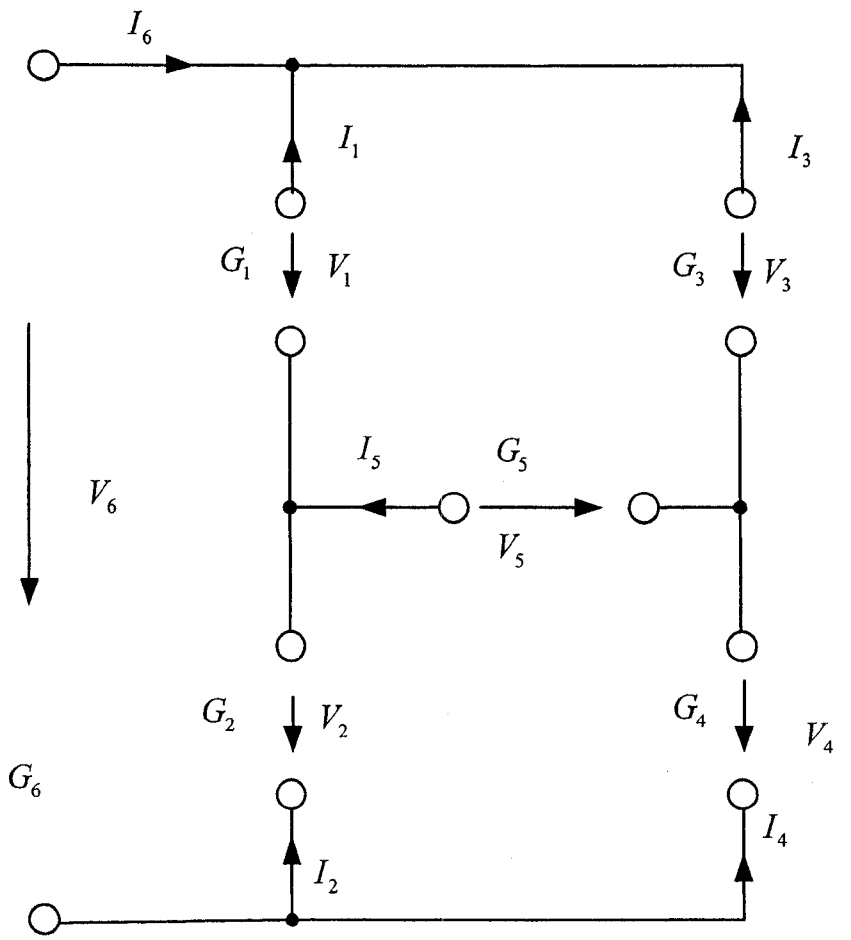

Figure 4.27: The wiring diagram of the bridge circuit of LC VCO

Since the scattering matrix is obtained, we can calculate the reflected waves of the six ports and connect Port 6 to the nonlinear resistance and the capacitor. This configuration is shown in Fig. 4.24. The WDF analysis is given as,

$$G_{p13} = G_{p11} + G_{p12}$$

$$\alpha_{11} = \frac{G_{p11}}{G_{p11} + G_{p12}}$$

$$a_{p11}(t_j) = b_{p11}(t_{j-1})$$

$$a_{p12}(t_j) = b_6(t_j)$$

$$\begin{bmatrix} b_1(t_j) \\ b_2(t_j) \\ b_3(t_j) \\ b_4(t_j) \\ b_5(t_j) \\ b_6(t_j) \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} & S_{15} & S_{16} \\ S_{21} & S_{22} & S_{23} & S_{24} & S_{25} & S_{26} \\ S_{31} & S_{32} & S_{33} & S_{34} & S_{35} & S_{36} \\ S_{41} & S_{42} & S_{43} & S_{44} & S_{45} & S_{46} \\ S_{51} & S_{52} & S_{53} & S_{54} & S_{55} & S_{56} \\ S_{61} & S_{62} & S_{63} & S_{64} & S_{65} & S_{66} \end{bmatrix} \begin{bmatrix} a_1(t_j) \\ a_2(t_j) \\ a_3(t_j) \\ a_4(t_j) \\ a_5(t_j) \\ a_6(t_j) \end{bmatrix}$$

$$b_{p13}(t_j) = \alpha_{11} \cdot a_{p11}(t_j) + (1-\alpha_{11}) a_{p12}(t_j)$$

$$a_{p13}(t_j) = \tilde{f}\left[b_{p13}(t_j)\right]$$

$$b_{p11}(t_j) = (\alpha_{11}-1) \cdot a_{p11}(t_j) + (1-\alpha_{11}) \cdot a_{p12}(t_j) + a_{p13}(t_j)$$

$$b_{p12}(t_j) = \alpha_{11} \cdot a_{p11}(t_j) - \alpha_{11} \cdot a_{p12}(t_j) + a_{p13}(t_j)$$

$$V_c = \frac{a_{p11}(t_j) + b_{p11}(t_j)}{2}$$

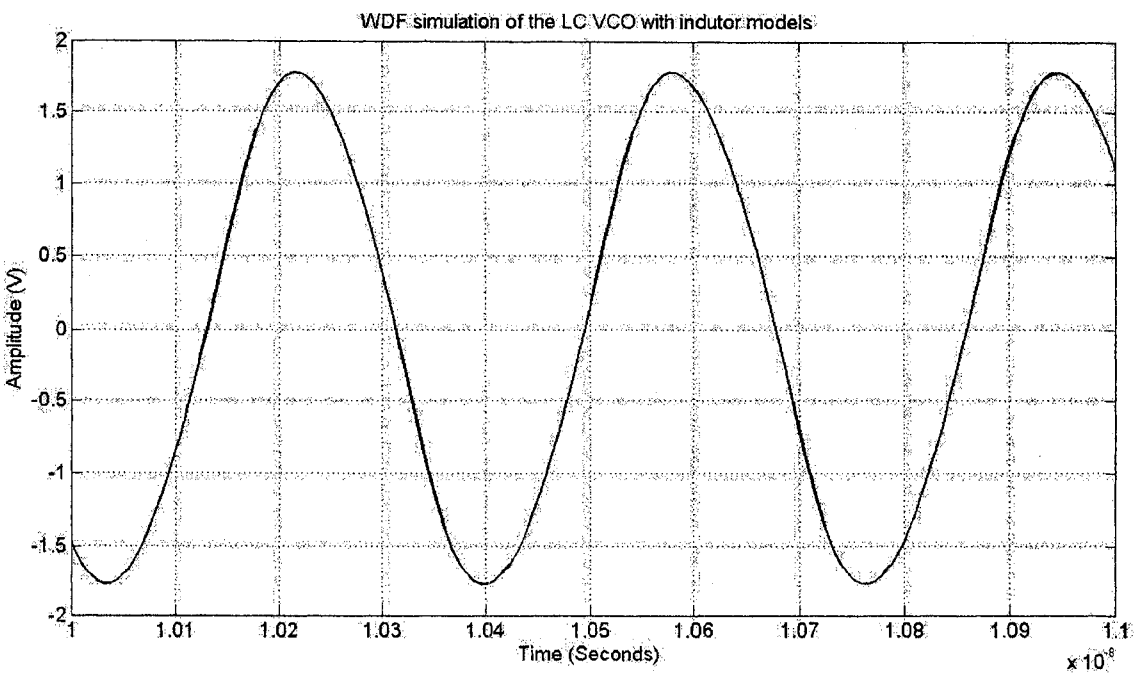

Figure 4.28: WDF simulation result of the LC VCO model with detailed inductor models

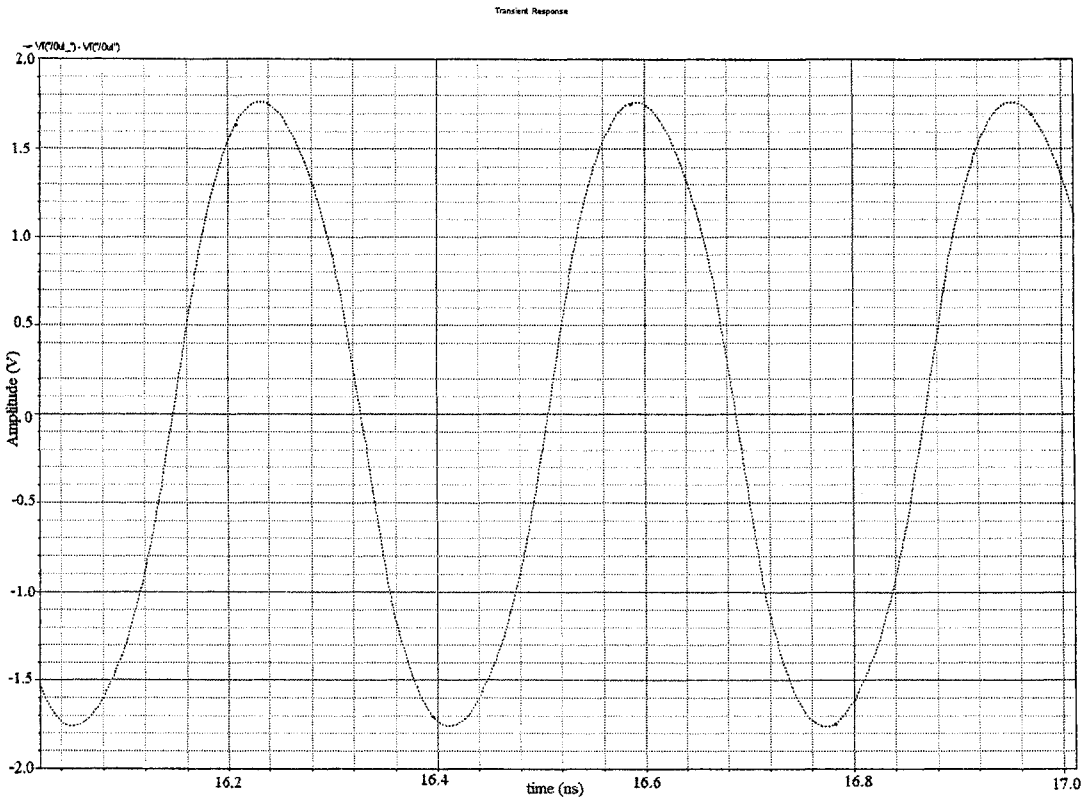

Figure 4.29: LC VCO simulated at 0.5 V in spectre

The value of S_{66} is zero since Port 6 is reflection-free. This is shown in Matlab simulation result. The simulation time step is 7 ps. The WDF technique based simulation result of the model in Fig. 4.20 is shown in Fig. 4.28. The oscillating frequency is 2.778 GHz. The peak voltage is 1.78 V. Fig. 4.29 shows the simulation results of LC VCO at 0.5 V controlled voltage in spectre. The simulation time and time step are 20 ns and 10 ps. The measured oscillating frequency and the peak voltage are 2.775 GHz and 1.764 V respectively. The error of the oscillating frequencies is 0.108%. The error of the peak voltages is 0.907%. Both simulation results are very close. We can conclude that the LC VCO model based on WDF principles is accurate.

A larger error of peak voltage 0.907% by using the detailed inductor model is obtained comparing with the error 0.412% by using simplified inductor model. The reason is that the simulation result in Fig. 4.29 with detailed inductor model has the varactors whose nonlinear characteristic can affect the peak voltage of the LC VCO.

Chapter 5

Conclusions and Future Work

5.1 Conclusions

In this thesis, WDF based transient simulations of different circuits were studied. Published simulation results of an anharmonic oscillator were confirmed in this thesis. An integrated CMOS LC VCO was designed, fabricated and modeled with a WDF structure. The WDF simulation of the LC VCO model shows a good agreement compared with the simulation results obtained with spectre. The following are the main conclusions:

- For linear circuits, especially for large linear networks, the application of WDF technique is straightforward since models of linear electric components are easily obtained. WDF techniques applied to linear circuits offer a similar trade off between time step size and accuracy as other integration techniques.
- Trees and Kirchhoff's laws are very useful to derive general adaptors. The combination of general adaptors, parallel adaptors and series adaptors is enough to describe the topology of a large and complicated network.
- WDF techniques are efficient for circuits with one nonlinear element since iterations can be avoided by using a reflection-free port to break delay-free loops. Simulation results show a good agreement compared with other simulation methods.
- For circuits with more than one nonlinear element WDF techniques are not yet mature. In principle iteration can not be avoided in this case
- The proper values of port resistances are very important since they can be used to avoid unwanted delay-free loops.

- Modeling and simulation of the designed LC VCO based on WDF techniques are successful.

5.2 Future Work

Following the studies described in this thesis, a new simulation method for solving networks with many nonlinear elements could be developed in the future. The method can be a combination of Newton's method and relaxation techniques based on scattering waves that has the potential of being more efficient for very large circuits. In addition, this method can be easily parallelizable. For example, this method can be applied to a CMOS inverter shown in Fig. 5.1.

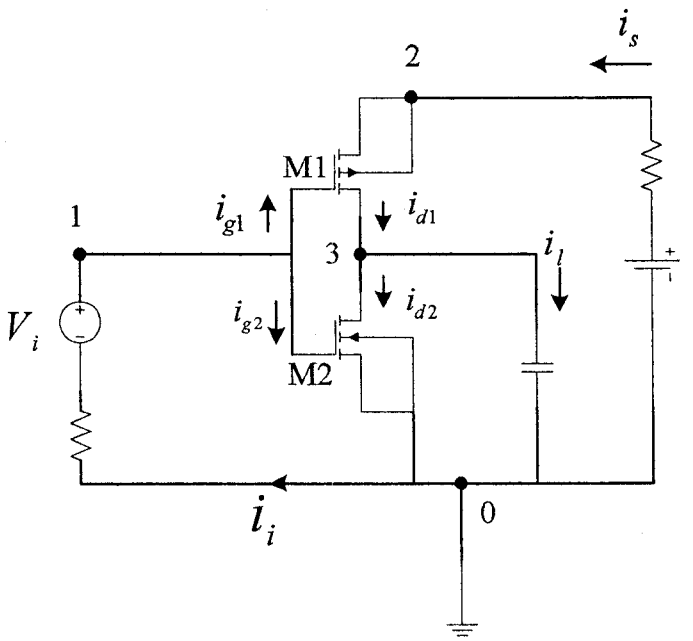

Figure 5.1: A CMOS inverter

The NMOS and PMOS transistors can be treated as a two-port element shown in Fig. 5.2.

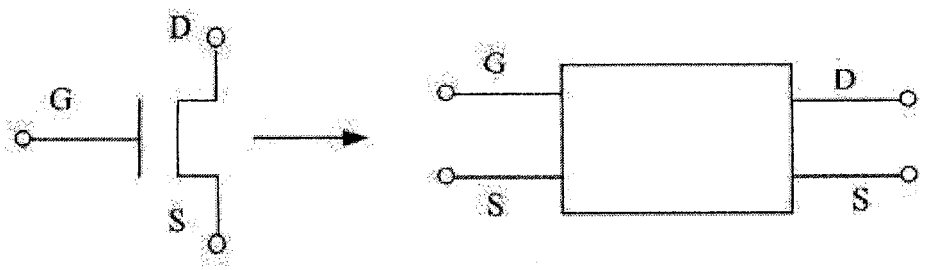

Figure 5.2: Transistor as a two-port element

We first replace the voltages and currents with incident and reflected waves. For example, the currents and voltages of NMOS transistor are replaced as shown,

$$i_d = \frac{a_{ds} - b_{ds}}{2z_0}$$

$$v_{ds} = \frac{a_{ds} + b_{ds}}{2}$$

$$v_{gs} = \frac{a_{gs} + b_{gs}}{2}$$

$$i_{gs} = 0 \Rightarrow a_{gs} = b_{gs}$$

and then we write the implicit equation for i_d,

$$\begin{aligned} i_d &= i_d(v_{gs}, v_{ds}) \\ &\Rightarrow \left(\frac{a_{ds} - b_{ds}}{2z_0} \right) - i_d(a_{gs}, \frac{a_{ds} + b_{ds}}{2}) = 0 \end{aligned} \tag{5.1}$$

Applying Newton's method to solve b_{ds}.

A connected graph of Fig. 5.1 is shown in Fig. 5.3.

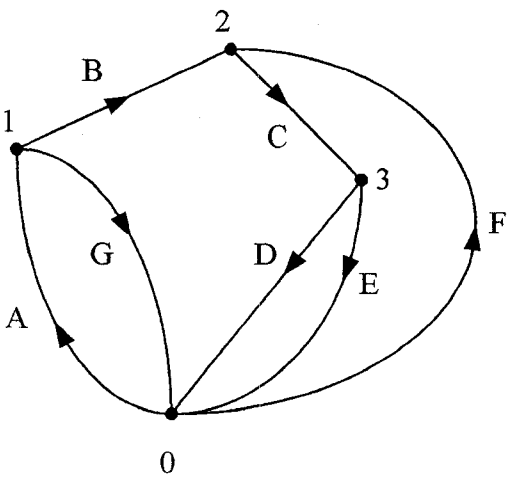

Figure 5.3: A connected graph of the inverter

Obtain the scattering matrix $\underline{S}$ by Trees and Kirchhoff's laws,

$$\underline{S} = -\begin{bmatrix} \underline{M_V} \\ -\underline{M_I G} \end{bmatrix}^{-1} \begin{bmatrix} \underline{M_V} \\ \underline{M_I G} \end{bmatrix}$$

The connection of the general adaptor according to scattering matrix is shown in Fig. 5.4,

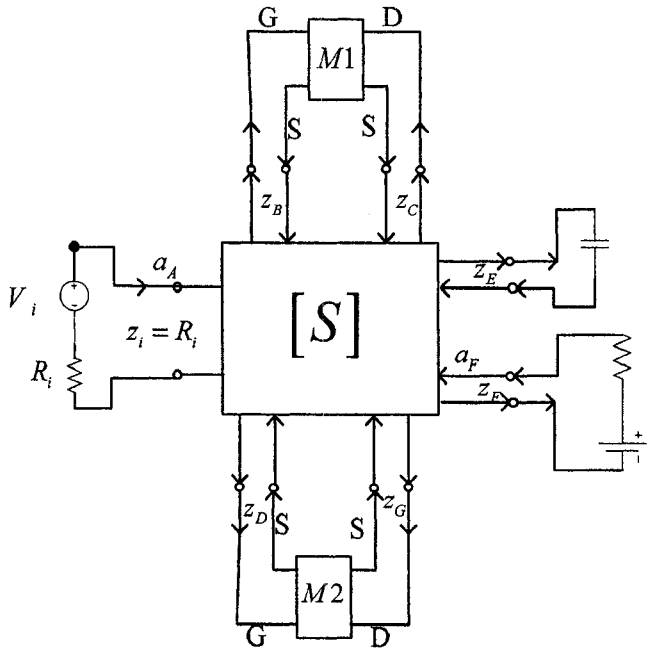

Figure 5.4: The connection of the general adaptor

According to Fig. 5.4, the initial conditions of incident and reflected waves of the general adaptor can be written in matrix form,

$$\begin{bmatrix} b_A \\ b_B \\ b_C \\ b_D \\ b_E \\ b_F \\ b_G \end{bmatrix} = [S] \begin{bmatrix} a_A \\ 0 \\ 0 \\ 0 \\ 0 \\ a_F \\ 0 \end{bmatrix}$$

Since the reflected waves of general adaptor are the incident waves of the elements, we can calculate the reflected waves of the elements according to their incident waves. For the nonlinear elements, we use Newton's method to solve the reflected wave as the example shown in Equation (5.1).

The advantage of this approach is that the Newton iterations for each nonlinear device are independent of each other and thus the computation can be performed in parallel.

Appendix A

The Details of LC VCO Design

A.1 Buffer Design

Since the output of the LC VCO is connected to the pad, package, test fixture and 50 ohm resistor in the spectrum analyzer as in Fig. A.1, a buffer is necessary to avoid degradation of the LC VCO performance. CMOS devices have a high input impedance, high gain, and high bandwidth. These characteristics are similar to ideal amplifier characteristics and, hence, CMOS inverters can be used as buffers in the LC VCO circuit in conjunction with other passive components. A CMOS inverter transfers characteristic in Fig. A.2 can be used to determine the bias point of the inverter. In the oscillator application, the inverter operates in the transition region C. The transition region is defined as the region where the slope of the curve is maximum and both PMOS and NMOS transistors are in saturation.

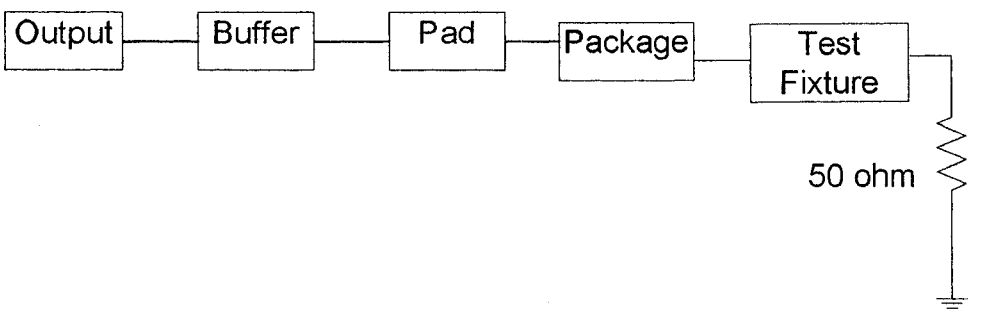

Figure A.1: Output connections of the LC VCO

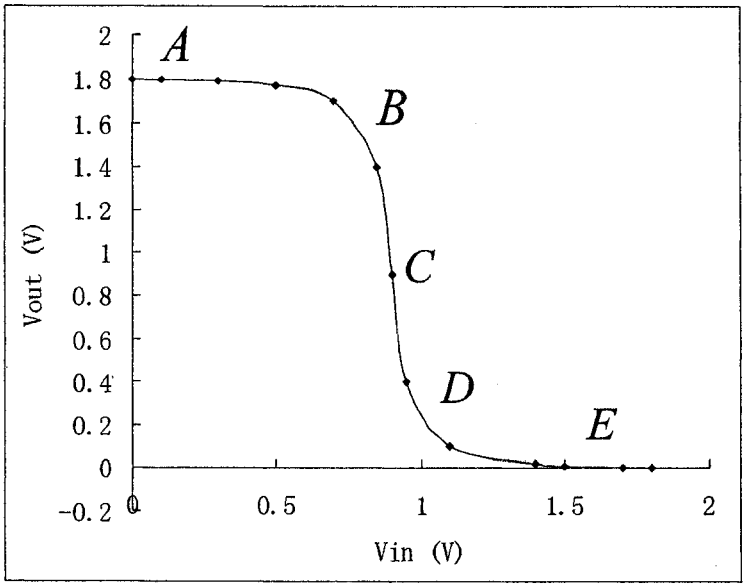

Figure A.2: CMOS inverter transfer characteristics

In this design, the inverters have 5 stages and the size of the inverters increases in each stage as well as the input voltage swing. The buffer circuit and the sizes are shown in Fig. A.3 and Table A.1.

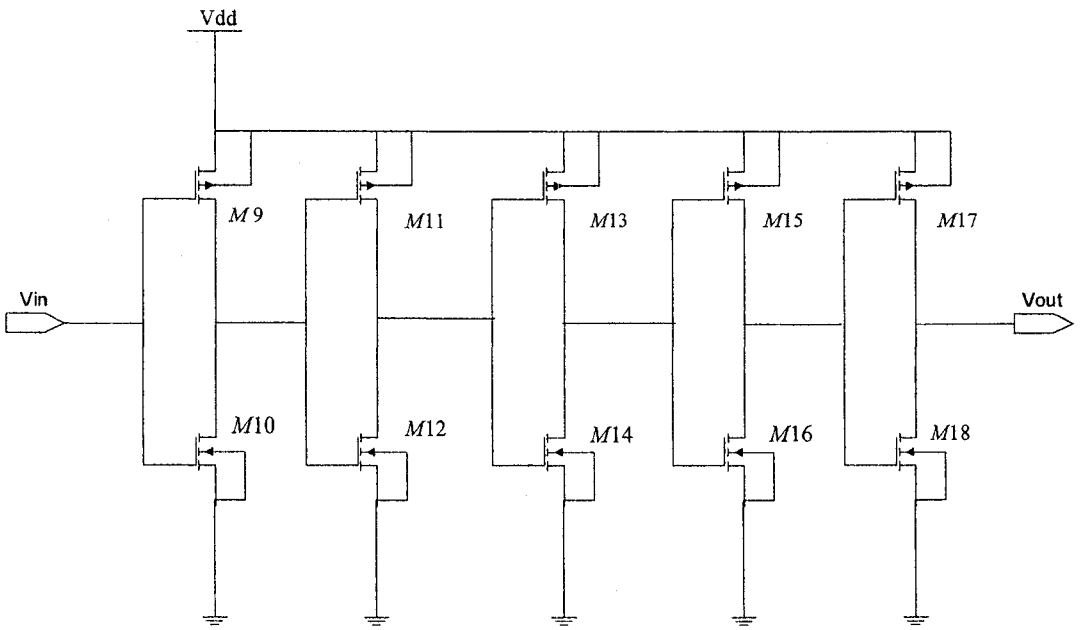

Figure A.3: The buffer circuit

*M*9	*M*10	*M*11	*M*12	*M*13
8.7u/180n	1.6u/180n	15u/180n	4.8u/180n	45u/180n
*M*14	*M*15	*M*16	*M*17	*M*18
15u/180n	60u/180n	20u/180n	300u/180n	30u/180n

Table A.1: The transistor sizes of the buffer circuit

A.2 Loose Die Chip

The 24-pin loose die chip in Fig. A.4 contains two oscillators. They are LC VCO and ring VCO. The ring VCO is designed by another graduate student. In this chip, both VCOs can not work at the same time. The on-off state of the two VCOs is controlled by two separated external voltage sources, Vstart and Vc. Vc is to turn on the LC VCO by turning on the tail current source. The inputs and outputs of the LC VCO are Vcontrol, Vc and Out-, Out+ respectively.

All the six metal and poly layers must meet certain density requirements before fabrication. The chip is filled up with dummy layers to meet the density requirements. The area of the loose die chip is $1mm \times 1mm$.

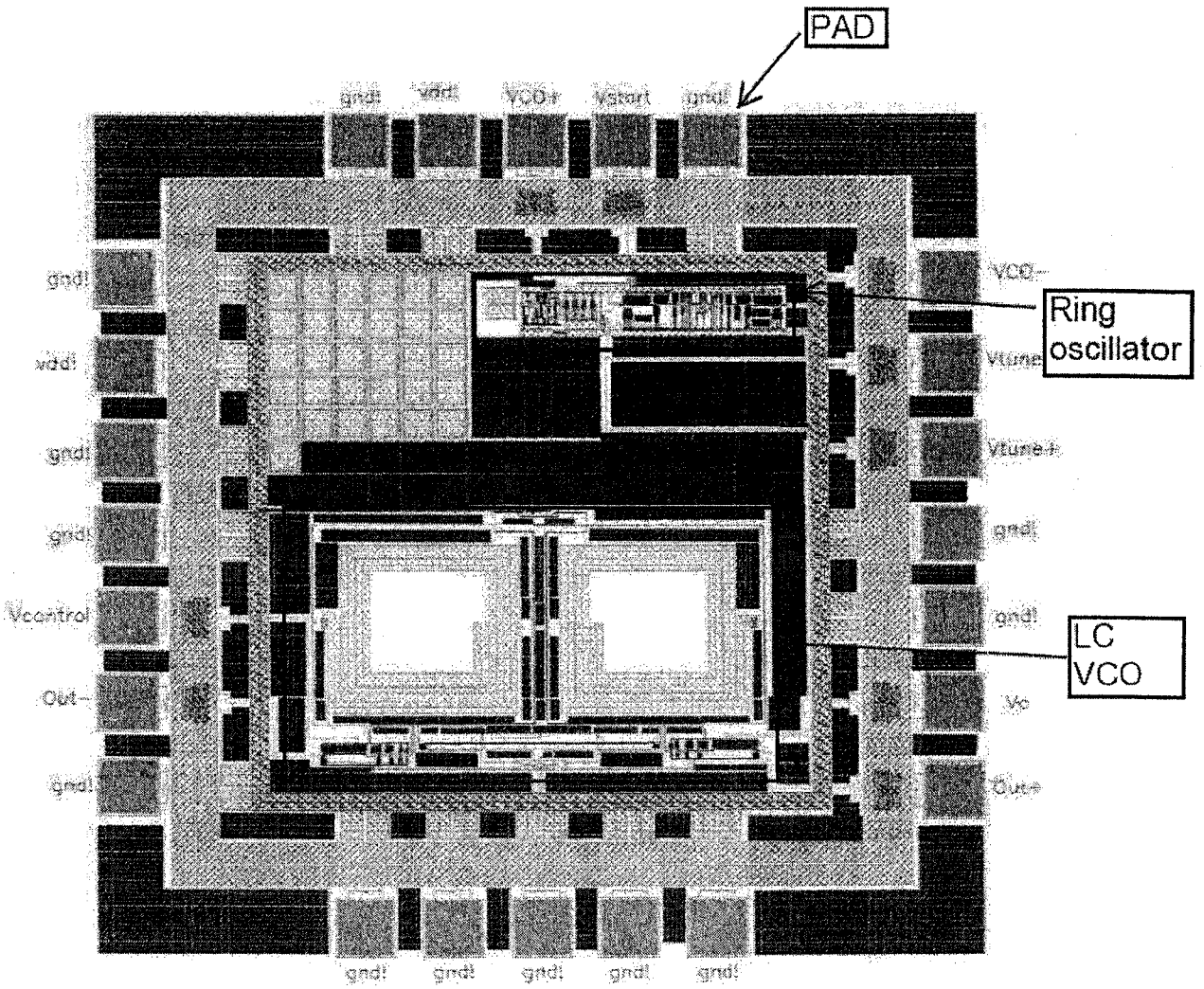

Figure A.4: The loose die chip

A.3 Packaging and Fixture

In order to test the chip, a 24- pin package is adopted for this design. Fig. A.5 (a) is the bonding diagram between the die chip and 24-pin package. Fig. A.5 (b) shows the 24-pin package with the die chip inside.

Since the package can not be directly probed, a test fixture is used. Test fixtures can provide more flexibility to the RF port location. With a test fixture, the matching and bias circuitry can be located near the device under test. Fig. A.6 shows the test fixture for the 24-pin package.

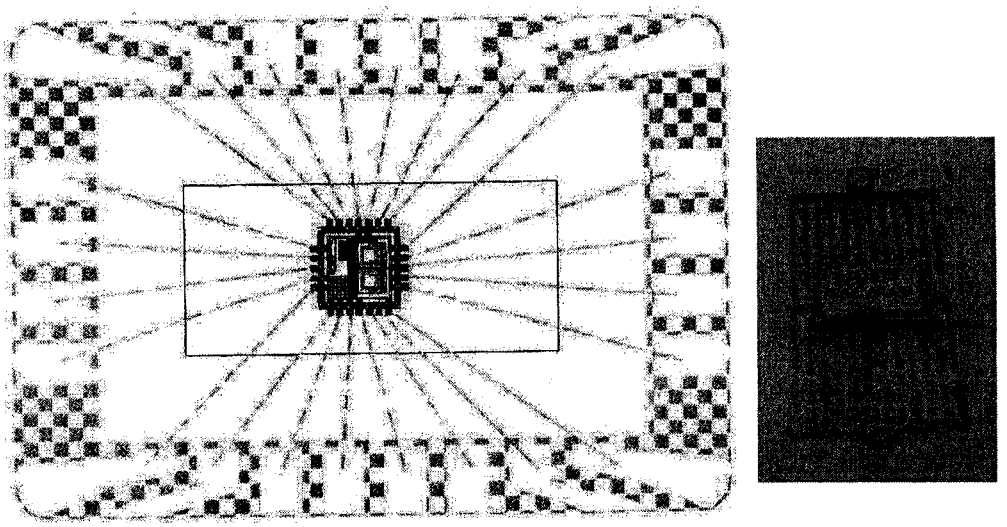

Figure A.5: (a) The bonding diagram (b) the loose die chip with 24-pin package

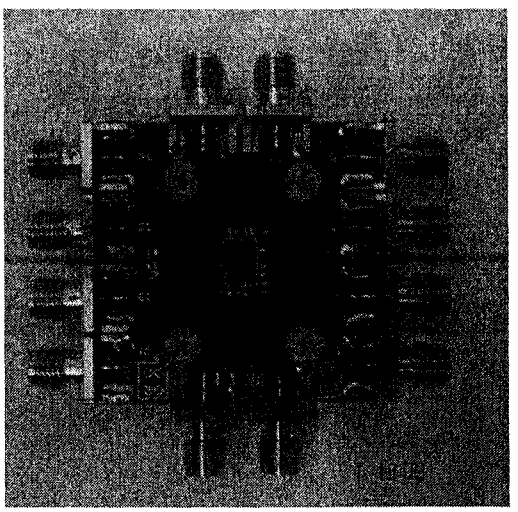

Figure A.6: Test fixture

A.4 Simulation Results

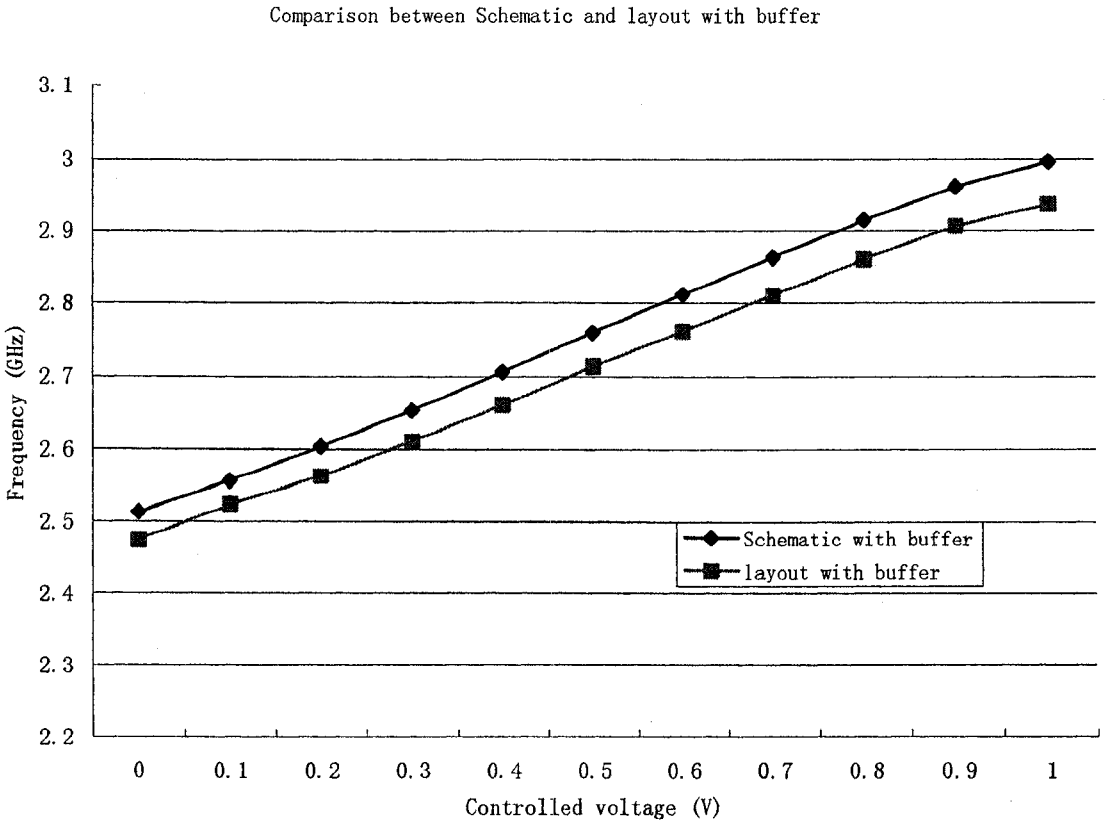

Figure A.7: Frequency comparison between schematic and layout with buffer

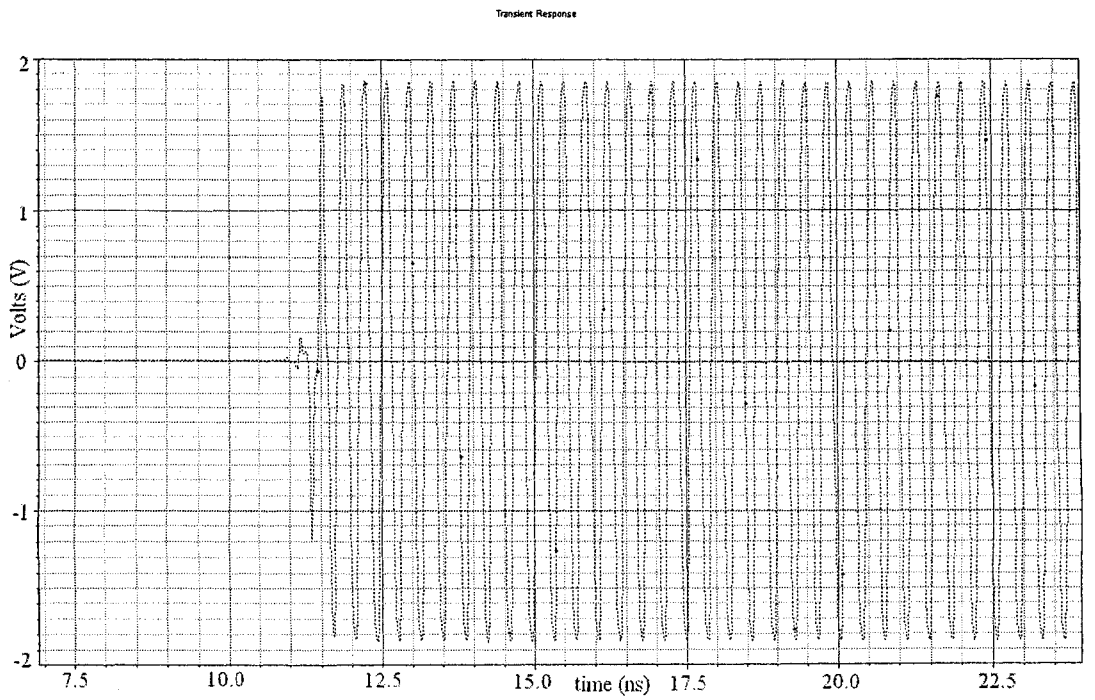

Figure A.8: Simulation of the schematic with buffer at 0.5 V controlled voltage

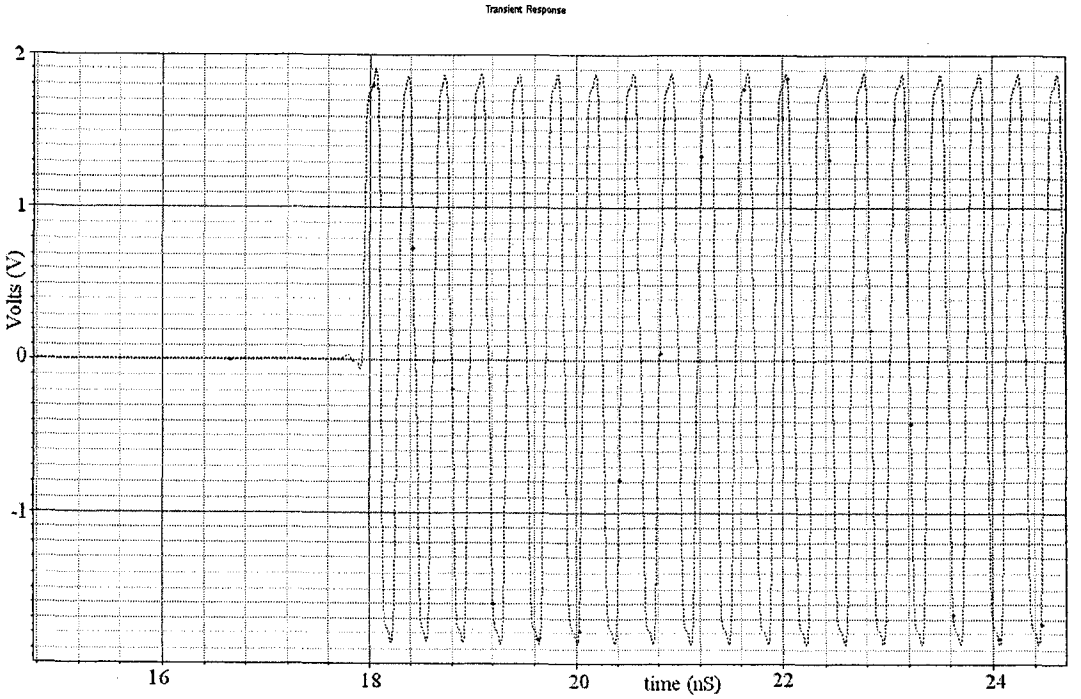

Figure A.9: Simulation of layout with buffer at 0.5 V controlled voltage

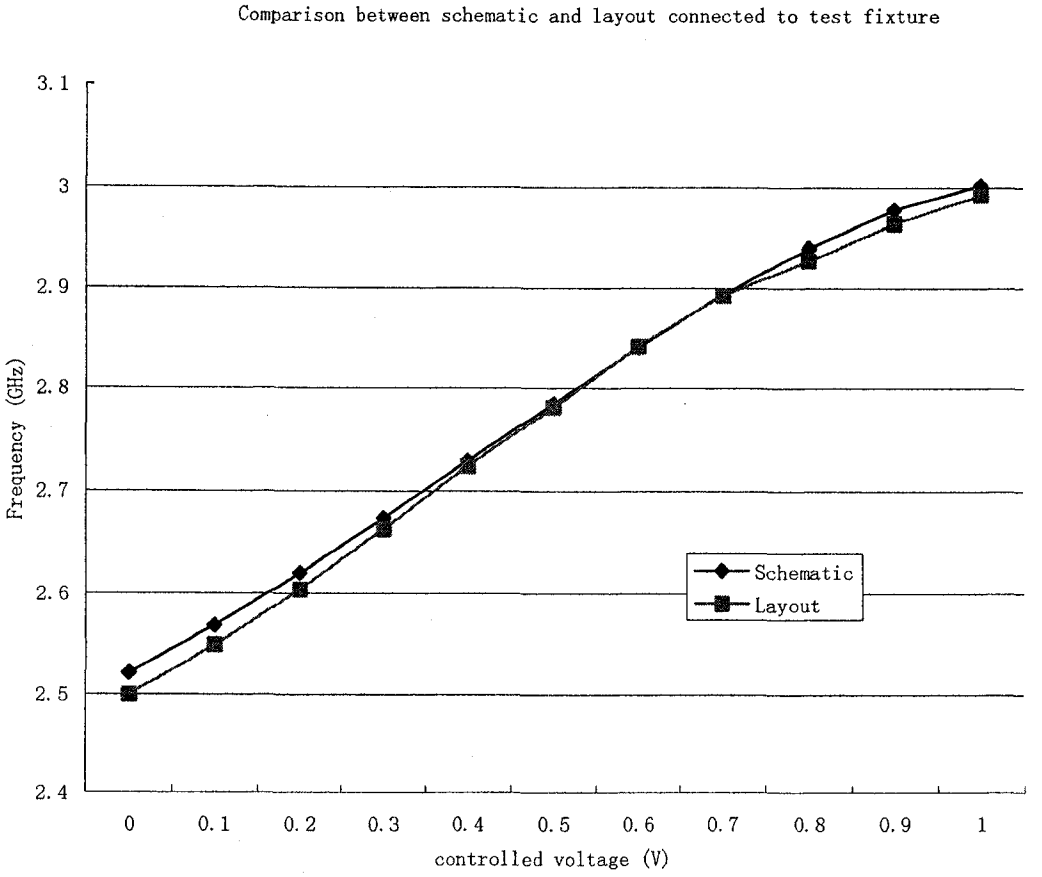

Figure A.10: Frequency comparison between schematic and layout connected to the test fixture.

Figure A.11: Simulation of the schematic with buffer connected to the test fixture

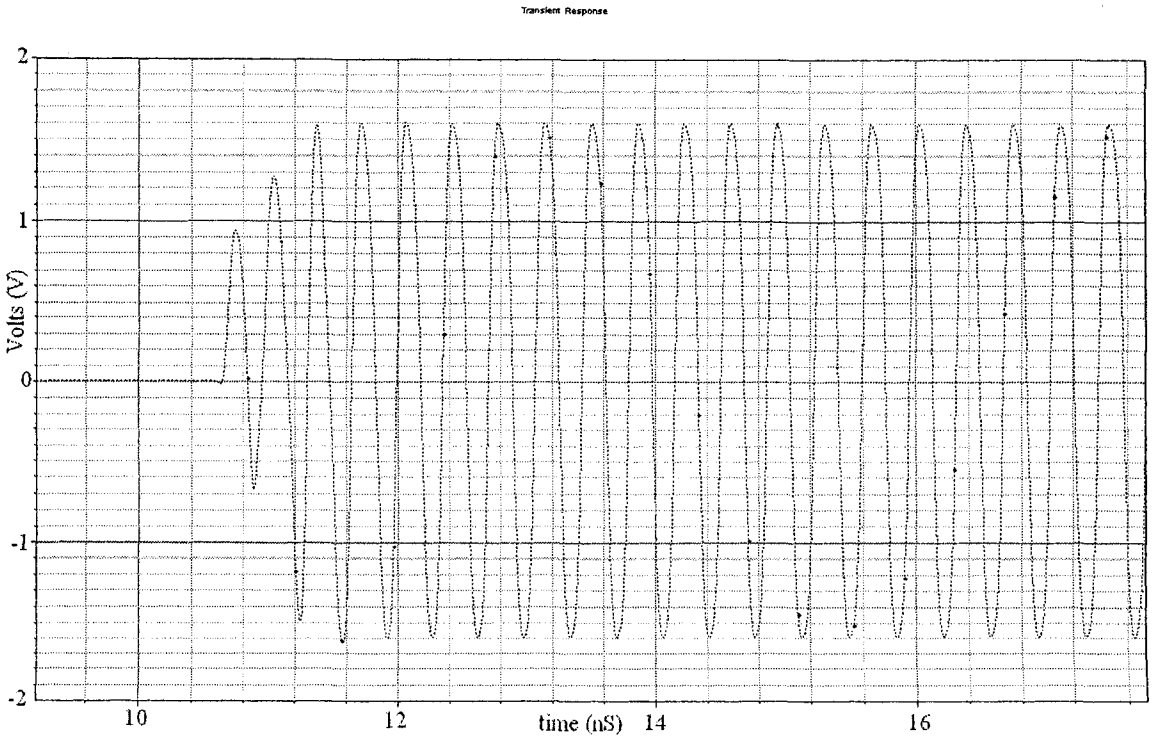

Figure A.12: Simulation of the layout with buffer connected to the test fixture

As we can see from the above simulation results, the frequencies of the layouts are lower than that of the schematics since the layouts have more parasitic capacitance than the schematics. When the test fixture is connected with 50 ohm load resistance (Fig.A.1), the amplitude of the layout is lower than that of the schematic. Those results are shown in Fig. A.11 and Fig. A.12.

A.5 Experimental Results

To test the LC VCO performance, the package has to be mounted on the top of the test fixture. This was done by James Dietrich (CMC Testing Collaboratory) in the University of Manitoba. He modified the test fixture since the power pin and ground pin on the test fixture are not compatible with those of on the package. The modified test fixture with the package is shown in Fig. A.13.

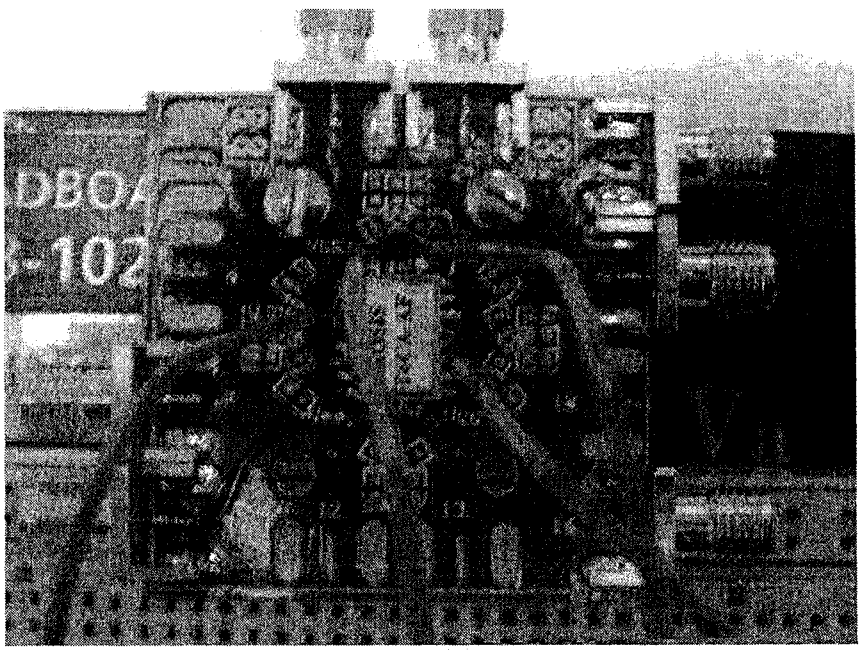

Figure A.13: The modified test fixture with package.

We tested the circuit shown in Fig.A.14 with multi-meters and power supplies. To measure the amount of power consumed by the chip, an amp meter was connected between the ground pad and ground. We found out that the chip would not draw any power. We further test the impedance between the ground pins on the package. The

impedances between the ground pins are equal to infinity. This problem is caused by no connection between the pad and the circuit itself. Even though the final design passed the design rule check (DRC) test, the layout versus schematic (LVS) with the pads was not performed. This critical mistake would have been avoided if the pads would have been included in the schematic.

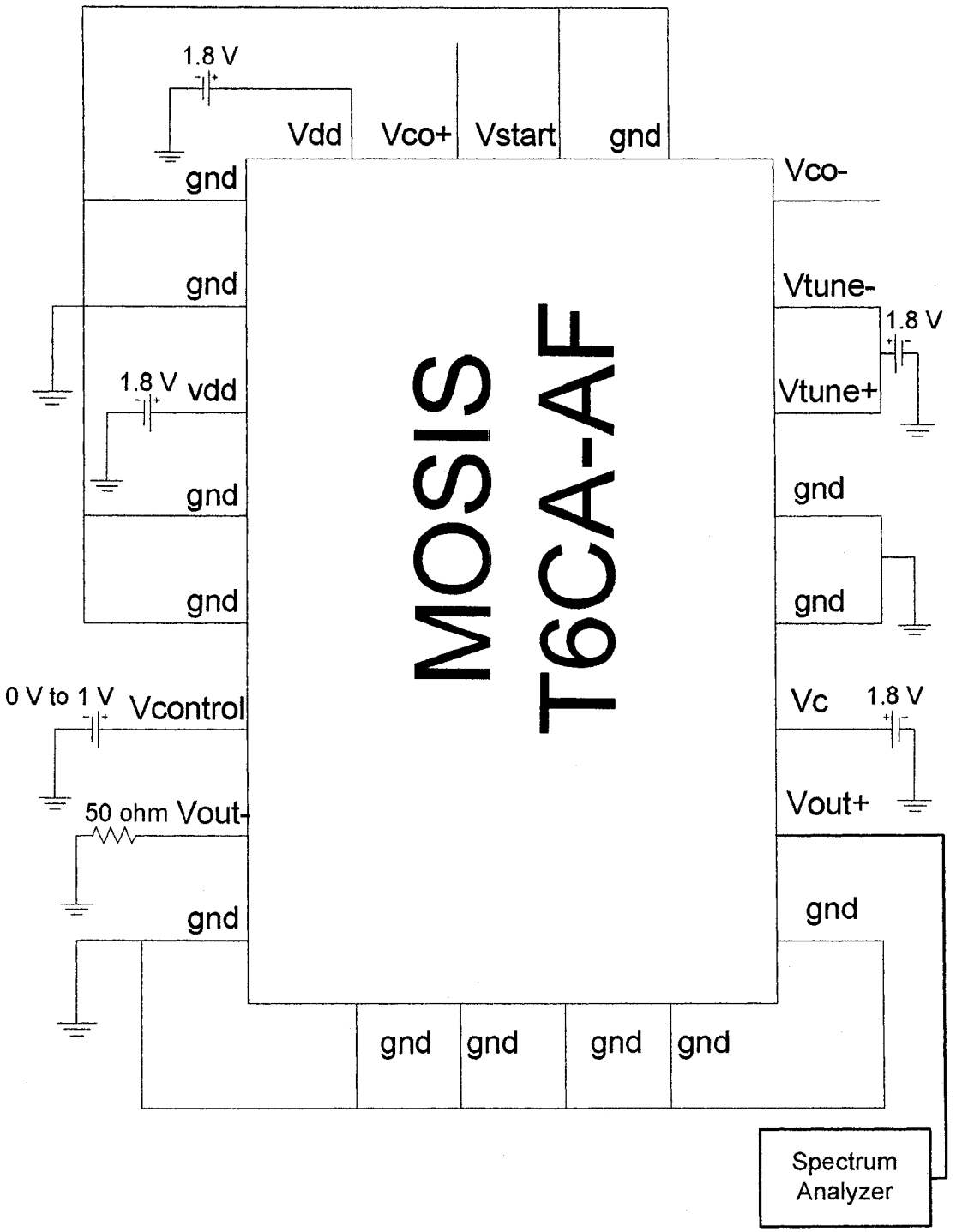

Figure A.14: The diagram of the tested circuit

Appendix B

WDF Analysis of Section 4.4.2

B.1 WDF Analysis of Part 1 and Part 2

$$G_{p23} = G_{p21} + G_{p22}$$

$$\alpha_{21} = \frac{G_{p21}}{G_{p21} + G_{p22}}$$

$$R_{s13} = R_{s11} + R_{s12}$$

$$\beta_{11} = \frac{R_{s11}}{R_{s11} + R_{s12}}$$

$$G_{p22} = 1 / R_{s13}$$

$$a_{s11}(t_j) = 0$$

$$a_{s12}(t_j) = -b_{s12}(t_{j-1})$$

$$b_{s13}(t_j) = -a_{s11}(t_j) - a_{s12}(t_j)$$

$$a_{p22}(t_j) = b_{s13}(t_j)$$

$$a_{p21}(t_j) = b_{p21}(t_{j-1})$$

$$b_{p23}(t_j) = \alpha_{21} \cdot a_{p21}(t_j) + (1 - \alpha_{21}) \cdot a_{p22}(t_j)$$

$$b_{p21}(t_j) = (\alpha_{21} - 1) \cdot a_{p21}(t_j) + (1 - \alpha_{21}) \cdot a_{p22}(t_j) + a_{p23}(t_j)$$

$$b_{p22}(t_j) = \alpha_{21} \cdot a_{p21}(t_j) - \alpha_{21} \cdot a_{p22}(t_j) + a_{p23}(t_j)$$

$$a_{s13}(t_j) = b_{p22}(t_j)$$

$$b_{s12}(t_j) = (\beta_{11} - 1) \cdot a_{s11}(t_j) + \beta_{11} \cdot a_{s12}(t_j) + (\beta_{11} - 1) \cdot a_{s13}(t_j)$$

B.2 WDF Analysis of Part 3 and Part 4

$$R_{s23} = R_{s21} + R_{s22}$$

$$\beta_{21} = \frac{R_{s21}}{R_{s21} + R_{s22}}$$

$$G_{p33} = G_{p31} + G_{p32}$$

$$\alpha_{31} = \frac{G_{p31}}{G_{p31} + G_{p32}}$$

$$R_{s22} = 1 / G_{p33}$$

$$a_{p31}(t_j) = 0$$

$$a_{p32}(t_j) = b_{p32}(t_{j-1})$$

$$b_{p33}(t_j) = \alpha_{31} \cdot a_{p31}(t_j) + (1 - \alpha_{31}) \cdot a_{p32}(t_j)$$

$$a_{s22}(t_j) = b_{p33}(t_j)$$

$$a_{s21}(t_j) = b_{s21}(t_{j-1})$$

$$b_{s23}(t_j) = -a_{s21}(t_j) - a_{s22}(t_j)$$

$$b_{s22}(t_j) = (\beta_{21} - 1) \cdot a_{s21}(t_j) + \beta_{21} \cdot a_{s22}(t_j) + (\beta_{21} - 1) \cdot a_{s23}(t_j)$$

$$a_{p33}(t_j) = b_{s22}(t_j)$$

$$b_{p32}(t_j) = \alpha_{31} \cdot a_{p31}(t_j) - \alpha_{31} \cdot a_{p32}(t_j) + a_{p33}(t_j)$$

$$b_{s21}(t_j) = (1 - \beta_{21}) \cdot a_{s21}(t_j) - \beta_{21} \cdot a_{s22}(t_j) - \beta_{21} \cdot a_{s23}(t_j)$$

B.3 WDF Analysis of Part 5

$$G_{p43} = G_{p41} + G_{p42}$$

$$\alpha_{41} = \frac{G_{p41}}{G_{p41} + G_{p42}}$$

$$R_{s31} = 1 / G_{p43}$$

$$R_{s33} = R_{s31} + R_{s32}$$

$$\beta_{31} = \frac{R_{s31}}{R_{s31} + R_{s32}}$$

$$G_{p61} = 1 / R_{s33}$$

$$G_{p53} = G_{p51} + G_{p52}$$

$$\alpha_{51} = \frac{G_{p51}}{G_{p51} + G_{p52}}$$

$$R_{s41} = 1 / G_{p53}$$

$$R_{s43} = R_{s41} + R_{s42}$$

$$\beta_{41} = \frac{R_{s41}}{R_{s41} + R_{s42}}$$

$$G_{p62} = 1 / R_{s43}$$

$$G_{p63} = G_{p61} + G_{p62}$$

$$\alpha_{61} = \frac{G_{p61}}{G_{p61} + G_{p62}}$$

$$a_{p41}(t_j) = 0$$

$$a_{p42}(t_j) = b_{p42}(t_{j-1})$$

$$b_{p43}(t_j) = \alpha_{41} \cdot a_{p41}(t_j) + (1 - \alpha_{41}) \cdot a_{p42}(t_j)$$

$$a_{s31}(t_j) = b_{p43}(t_j)$$

$$a_{s32}(t_j) = b_{s32}(t_{j-1})$$

$$b_{s33}(t_j) = -a_{s31}(t_j) - a_{s32}(t_j)$$

$$a_{p61}(t_j) = b_{s33}(t_j)$$

$$a_{p51}(t_j) = 0$$

$$a_{p52}(t_j) = b_{p52}(t_{j-1})$$

$$b_{p53}(t_j) = \alpha_{51} \cdot a_{p51}(t_j) + (1 - \alpha_{51}) \cdot a_{p52}(t_j)$$

$$a_{s41}(t_j) = b_{p53}(t_j)$$

$$a_{s42}(t_j) = b_{s42}(t_{j-1})$$

$$b_{s43}(t_j) = -a_{s41}(t_j) - a_{s42}(t_j)$$

$$a_{p62}(t_j) = b_{s43}(t_j)$$

$$b_{p63}(t_j) = \alpha_{61} \cdot a_{p61}(t_j) + (1 - \alpha_{61}) \cdot a_{p62}(t_j)$$

$$b_{p61}(t_j) = (\alpha_{61} - 1) \cdot a_{p61}(t_j) + (1 - \alpha_{61}) \cdot a_{p62}(t_j) + a_{p63}(t_j)$$

$$a_{s33}(t_j) = b_{p61}(t_j)$$

$$b_{s31}(t_j) = (1 - \beta_{31}) \cdot a_{s31}(t_j) - \beta_{31} \cdot a_{s32}(t_j) - \beta_{31} \cdot a_{s33}(t_j)$$

$$a_{p43}(t_j) = b_{s31}(t_j)$$

$$b_{p62}(t_j) = \alpha_{61} \cdot a_{p61}(t_j) - \alpha_{61} \cdot a_{p62}(t_j) + a_{p63}(t_j)$$

$$a_{s43}(t_j) = b_{p62}(t_j)$$

$$b_{s41}(t_j) = (1 - \beta_{41}) \cdot a_{s41}(t_j) - \beta_{41} \cdot a_{s42} - \beta_{41} \cdot a_{s43}(t_j)$$

$$a_{p53}(t_j) = b_{s41}(t_j)$$

$$b_{p42}(t_j) = \alpha_{41} \cdot a_{p41}(t_j) - \alpha_{41} \cdot a_{p42}(t_j) + a_{p43}(t_j)$$

$$b_{s32}(t_j) = (\beta_{31} - 1) \cdot a_{s31}(t_j) + \beta_{31} \cdot a_{s32}(t_j) + (\beta_{31} - 1) \cdot a_{s33}(t_j)$$

$$b_{p52}(t_j) = \alpha_{51} \cdot a_{p51}(t_j) - \alpha_{51} \cdot a_{p52}(t_j) + a_{p53}(t_j)$$

$$b_{s42}(t_j) = (\beta_{41} - 1) \cdot a_{s41}(t_j) + \beta_{41} \cdot a_{s42}(t_j) + (\beta_{41} - 1) \cdot a_{s43}(t_j)$$

Bibliography

[1] Alfred Fettweis, "Wave digital filters: Theory and practice," Proceedings of the IEEE, vol. 74, no. *2,* pp. 270-327, February 1986.

[2] Lawson, Stuart and Ahmad Mirzai. Wave Digital Filters. London: E. Horwood, 1990

[3] M Roitman, P S R Diniz - "Power System Simulation based on Wave Digital Filters" -IEEE Transactions on Power Delivery, v.11, n.2, pp.1098-1104, April 1996.

[4] T. Felderhoff, "Simulation of nonlinear circuits with period doubling and chaotic behavior by wave digital principles," *Trans. Circuits Syst.I,* vol. 41, pp. 485–491, July 1994.

[5] J. Marti, J. Lin - "Supression of Numerical Unstabilities in the EMTP" - IEEE Transactions on Power Systems, v. 4, n.2, pp. 739-747, May 89.

[6] A. Fettweis and K. Meerkotter, "On adaptors for wavedigital filters", *IEEE Trans. Accoust., Speech, Signal Processing,* Vol.ASSP-23, No.6, pp.516-525, December 1975.

[7] A. Fiedler and H. Grotstollen, "Simulation of power electronic circuits with principles used in wave digital filters"- IEEE Transaction on Industry Applications, v.33, n.3, pp.49-57, Jan,-Feb 1997

[8] K. Meerk¨otter and R. Scholtz, "Digital simulation of nonlinear circuits by wave digital filter principles," in Proc. IEEE Intl. Symp. Circuits Syst., Portland, OR, May 8–11, 1989, vol. 1, pp. 720–723.

[9] A. Sarti and G. De Poli, "Toward nonlinear wave digital filters"- IEEE Transactions on Signal Processing, v 47, n 6, p 1654-68, June 1999

[10] L. O. Chua, "Nonlinear circuits," *IEEE Trans. Circuits Syst.*, vol. CAS-31, pp. 69–87, Jan. 1984.

[11] A. Sarti and G. De Poli, "Generalized adaptors with memory for nonlinear wave digital structures," in *Proc. EUSIPCO, Eighth EuroSignal Process. Conf.*, Trieste, Italy, Sept. 10–13, 1996, vol. 3, pp.1941–1944.

[12] M. Tiebout. Low Power VCO design in CMOS. New York: Springer, 2006.

[13] P. Yue, C. Ryu, JackLau, T. Lee, and S. Wong, "A physical model for planar spiral inductors on silicon," 1996 International Electron Devices Meeting Technical Digest, pp. 155–158, Dec. 1996.

[14] P. Yue and S. Wong, "Physical modelling of spiral inductor on silicon," IEEE Transactions on Electron Devices, vol. 47, no. 3, pp. 560–568, Mar. 2000.

[15] TSMC 0.18UM MIXED SIGNAL 1P6M SALICIDE 1.8V/3.3V RF SPICE MODELS

[16] C. P. Yue and S. S. Wong, "On-chip spiral inductors with patterned ground shields for Si-based RF ICs," IEEE J. Solid-State Circuits, vol. 33, pp. 743–752, May 1998.

[17] Post, J. E., "Optimizing the design of spiral inductors on silicon," IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, Vol. 47, No. 1, 15-17, 2000.

[18] G. Konstanznig, T. Pappenreiter, L. Maurer, A. Springer, R. Weigel, "Design of a 1.5 V, 1.1mA Fully Integrated LC-tuned Voltage Controlled Oscillator in the 4 GHz- Band using a 0.12µm CMOS-Process", Proc. Asia-Pacific Microwave Conference 2002, pp. 1471-1474, November 2002.

[19] D. Ham and A Hajimiri, "Design and Optimization of a Low Noise 2.4GHz CMOS VCO with Integrated LC Tank and MOSCAP Tuning," Proc. of IEEE International Symposium on Circuits and Systems, pp. 331-334, May 2000.

[20] Maria del Mar Hershenson, Ali Hajimiri, Sunderarajan S. Mohan, Stephen P. Boyd, and Thomas H. Lee, "Design and optimization of LC oscillators," in IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, pp. 65–69, 1999.

[21] D. Ham and A. Hajimiri, "Concepts and Methods in Optimization of Integrated LC VCOs," IEEE Journal of Solid-State Circuits, vol. 36, no. 6, pp. 896-909, June 2001.

[22] Paulo J. C. Rodrigues, Computer-Aided Analysis of Nonlinear Microwave Circuits. London: Artech House, 1998.

[23] Chua, L.O., and Lin, P.-M., Computer-Aided Analysis of Electronic Circuits, Englewood Cliffs, NJ, Prentice-Hall, 1975.

[24] P. Stefan & R. Rudolf, "Wave Digital Filter with Multiple Nonlinearities," In 12th European Signal Processing Conf. Vienna, Austria Sep. 2004

[25] T. Felderhoff, " Jacobi's method for massive parallel wave digital filter algorithm," Proc. Of the IEEE Conference on Acoustic, Speech and Signal Processing, vol. 3, May 1996, pp. 1621-1624.

[26] A. Hajimiri and T. H. Lee, The Design of Low Noise Oscillators, Kluwer Academic, 1999.

[27] http://www-ccrma.stanford.edu/~jos/Meshes/Discretization.html