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ADAPTIVE HIGH VOLTAGE PULSE SIGNAL GENERATOR CIRCUIT DESIGN

A Thesis Presented

by

Lixi Tao

to

The Faculty of the Graduate College

of

The University of Vermont

In Partial Fulfillment of the Requirements
for the Degree of Master of Science
Specializing in Electrical Engineering

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ABSTRACT

Ground Penetrating Radar (GPR) is widely used in area of geologic exploration, hidden stationary subject detection and quality inspection on various infrastructures. The pulse generator, which offers very accurate timing information, is the most cardinal component in GPR systems. It is easy to design a pulse generator which produces pulse with pre-settled peak value and pulse width in nanosecond scale. However, since the system is working in complicated environments, various pulses in different pulse widths and amplitudes are needed. In this background, pulse generators in tunability and stability are precious in value and universal in use. Indeed, a few adaptive high voltage pulse signal generators in UWB circuit level have been developed.

A pulse generator with tunable pulse width and controllable voltage amplitude is proposed under these demands. The proposed circuit implementation combines System-On-Chip (SOC) design with Printed Circuit Board (PCB) design because we intend to realize modulation separately. We also design an easy input console named Binary Input Array in the research to realize control simplicity. Furthermore, we employ mathematical model to optimize parameters in each component in order to have an improved performance. Simulation data are obtained from Cadence Virtuoso and OrCAD Capture.

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CHAPTER 1: Introduction

1.1. Background and motivation

Ground-penetrating radar is geophysical method which uses high-frequency pulse to image the subsurface. As a part of Ground penetrating radar system, pulse generator plays a critical role in the whole system that it offers very accurate timing information. Meanwhile it generates specific pulse signal for radar which substantially determines the quality of the ground-penetrating radar obtained raw data. Moreover, ground-penetrating radar system is widely used in areas of geologic exploration, hidden stationary subject detection and quality inspection of high way, bridge, etc. To satisfy the demand of complicated working environment such as construction area, natural region and building debris, pulse generator should be versatile in functionality. Due to the requirement, researchers mainly focus on tunable pulse generator realization and performance improvement. Typically, pulse amplitude, pulse width and transition time are three important parameters of the pulse generator in ground-penetrating radar system.

Various of tunable pulse generator designs are published. The primary choice is to increase the pulse width by combining more pulses using PIN-diode or MOSFET [1-2]. The pulse is with low distortion, but pulse shape, or Gaussian symmetry, is often loosened [3]. Another choice is introduced that a pulse generator with tunable pulse-duration can be developed using a variable edge-rate signal. Edge-rate variability is realized by using a simple RC network to adjust edge-rate. The output pulse is with good symmetry and low distortion over tunable range [3]. However, the range of pulse width is extremely limited. Besides, another design is presented in [4] which realizes tunable

pulse width by controlling difference between the delayed pulse and the reference pulse. The pulse is generated by inputting two pulses into an Exclusive OR gate [4-6].

However, some designs introduce a problem that voltage amplitude drops apparently when pulse is in narrow width [3-4]. In each of these designs, a variable capacitor plays a critical role in pulse width modulation that pulse width is in direct proportion to capacitance. However, it is not simply controls pulse width of the signal in the pulse generator and it also determines stored energy which contributes pulse amplitude. The pulse amplitude is related to the performance of ground penetrating radar system because the voltage amplitude determines penetrating depth of system. As a result, high-amplitude pulse is always demanded because it can highly amplify the detecting range and improve performance of receiver by increasing the signal-to-noise ratio.

The amplification for pulse amplitude can be achieved in many ways. Generally, voltage amplitude can be modulated by level shifter in on-chip design [7-9] or amplifier in off-chip design. In level shifter design, the performance is based on technology process and it is always used in low voltage circuits and systems. For 180-nm technology, level shifter has limited operating ranges on pulse amplitude amplification [9]. Meanwhile, the amplifier design is plentiful in board level and it is common for high voltage pulse designs [10-13]. Using avalanche transistor in Marx circuit design, high output amplitude can be realized easily on 50 Ohms resistive load with nanosecond pulse width [14-15]. More classic amplifier designs described, such as operational amplifier and bipolar-junction-transistor amplifier topologies, also have great potential to realize pulse amplification.

In order to realize a pulse generator with versatility and stability, a general design with tunability and linearity in both pulse width and pulse amplitude is desired.

1.2. Thesis Objective

The primary objective of the research is to present an adaptive high voltage pulse generator design. Versatility and stability are two main considerations in the research and they are detailed in following requirements.

First, tunable pulse width with nanosecond scale is required. The proposed pulse width of output is ranging from 1 nanosecond to 10 nanoseconds with linear step size. Because transition time is an important part of pulse width [16], fast switching speed in the pulse generator is needed in order to realize pulse width in nanosecond scale.

Secondly, controllable voltage amplitude is needed. It is well established that the radiated power of signal may limit the effective depth range of ground-penetrating radar investigation. In order to design a versatile pulse generator, the module with voltage amplitude controllability is essential. The proposed voltage amplitude of output signal is from 5 Volt to 30 Volt while it is controlled with linear increment.

In the third, independence in output modulation is desired. The design modulates two parameters of a pulse separately which decreases negative interactions between modules. As it is described, some designs regulate pulse width with obvious loss in pulse amplitude [3-4]. In these designs, capacitance plays a critical role in pulse width modulation. They control the transition time as part of pulse width of output by changing output capacitance. However, they introduce a problem that output voltage varies in

different pulse width apparently and it is deficient for following part in ground-penetrating radar system. The uniqueness of the proposed circuit comes from the fact that these two important parameters of a pulse are controlled independently, which significantly reduce negative interaction and the energy consumption.

Additionally, operation with simplicity is highly valuable. In the working environment, easy operation apparently decreases workloads and unnecessary turnovers for users. It also prevents majority of unpredictable damage for ground-penetrating radar systems. The proposed design introduces a binary code as input to control the pulse generator in Pulse Width Control Module. Operation simplicity is not widely concerned in former designs.

Overall, the proposed design in the research mainly focuses on a general solution with these four targets.

1.3 Thesis structure

The structure of this thesis is as follows:

Chapter 1 introduces background for pulse generator and main concentrations of the research.

Chapter 2 introduces an architecture based on a popular structure of on-chip design which has capability to realize pulse width controllability. Also, its mathematical model is described in the discussion.

Chapter 3 proposes the Pulse Width Control Module design including schematic and layout. It also addresses algorithm for performance improvement.

Chapter 4 explains simulation settings for the Pulse Width Control Module and presents simulation results of pulse width and power consumption.

Chapter 5 proposes the Pulse Amplitude Control Module and describes the schematic implementation.

Chapter 6 explains simulation settings for the Pulse Amplitude Module and presents simulation results for each code along with data reviews.

Chapter 7 concludes the thesis and discusses future work regarding pulse generator in ground-penetrating radar system.

CHAPTER 2: CURRENT STARVED CIRCUIT

2.1. Introduction

Current starved technique is popular for realization of a variable delay element. In contrast to shunt capacitor technique [4] with several disadvantages described in Chapter 1, current starved technique has capability for realizing different pulse widths with stable amplitude of output.

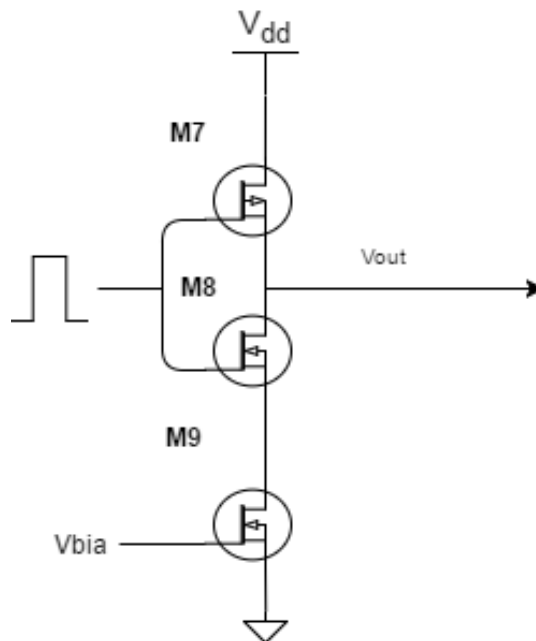


Figure 1: Basic Current starved circuit [17]

Figure 1 is the basic block of a current starved circuit. As it is shown, there is an inverter, composed of M7 and M8, between source signal and delayed signal V_{out} in the circuit. The circuit is different from an inverter in that a NMOS transistor, M9, controls discharging current of the output capacitance by changing the equivalent resistance between ground and the source of NMOS device, M8. Respectively, discharging current

depends on the gate voltage, V_{bia} , of M9 transistor. As a result, the falling edge of clock signal through the inverter is controlled.

In the design, the pulse width of final output is based on the pulse delay in source signal. However, the performance is limited. Neither pulse delay nor the range of tunable pulse width is qualified for requirements of research. As it is described, we require outputs ranging from 1ns to 10 ns.

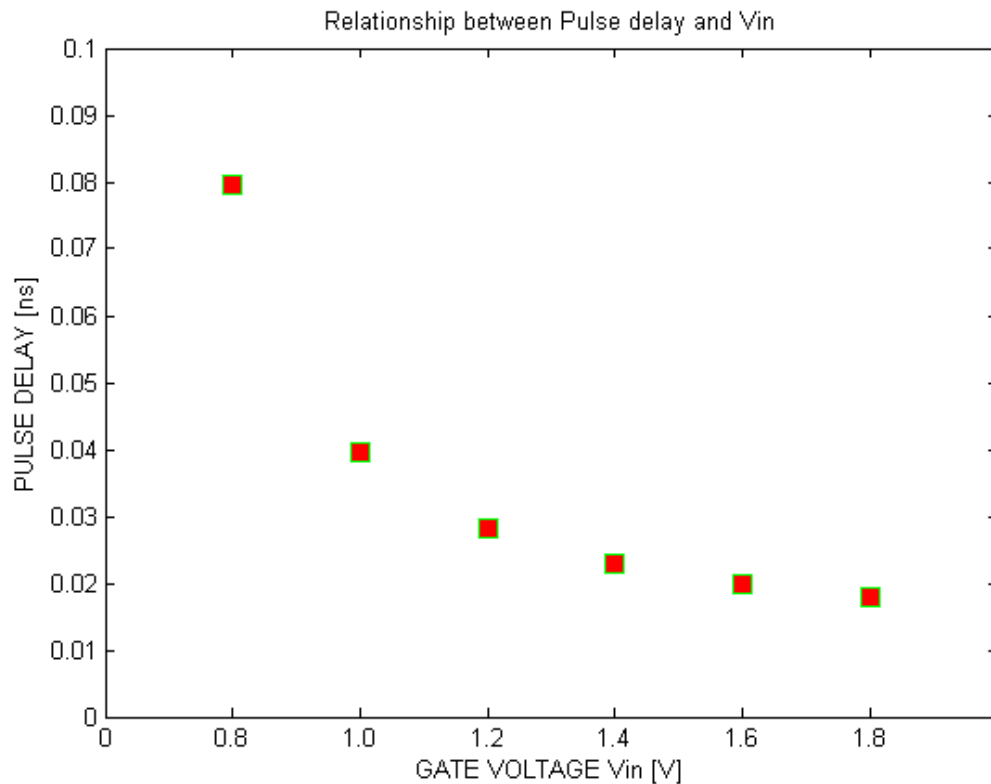


Figure 2: Simulation result of basic current starved circuit

In Figure 2, the simulation result shows the relationship between V_{in} and the pulse delay where V_{in} sweeps from 0.8 Volt to 1.8 Volt. Apparently, the pulse delay is in picosecond scale and the range is less than 80 picoseconds. Meanwhile, the curve connecting all points is rugged so that the linearity of the result is good for the design.

2.2. Current Starved Circuit

The current starved circuit is designed combining with a capacitor [18] to satisfy the proposed objective in the research. Figure 3 shows the architecture of the circuit.

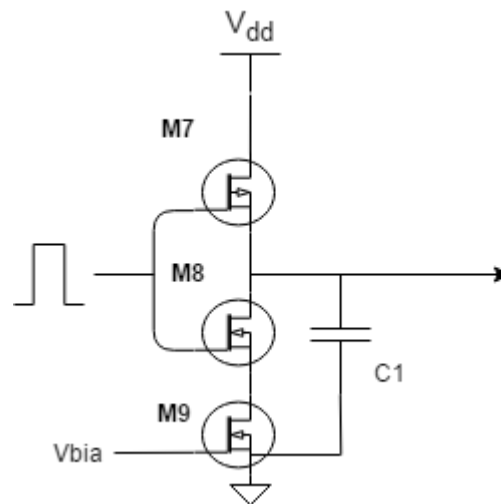


Figure 3: Current Starved Circuit with a capacitor

In the current starved circuit, an extra constant capacitor $C1$ is added between output and ground nodes to extend the width of the output pulse signal.

As we know, the pulse width is measured between the rising and falling edges of a single pulse that the 50% power level as reference points is used [16]. We noticed that the pulse width can be changed by controlling the fall time of the output signal. While pulse width is modulated by controlling the falling edge of output signal in the basic current

starved circuit, it is natural for us to consider extending fall time by output capacitance for pulse width modulation in the circuit. It is known that the fall time can be simply represented as

$$t_f = 2.2 \tau \quad (2.1)$$

where

$$\tau = R * C \quad (2.2)$$

is the time constant. R is the equivalent output resistance and C is the equivalent output capacitance. The equation shows that the fall time is in direct proportion to output capacitance. As a result, an extra capacitor can apparently increase the fall time of output. To be mentioned, the rise time is also increased.

And, in the circuit, transistor M7 is a PFET while transistor M8 and M9 are NFET.

The circuit can be viewed as Figure 4.

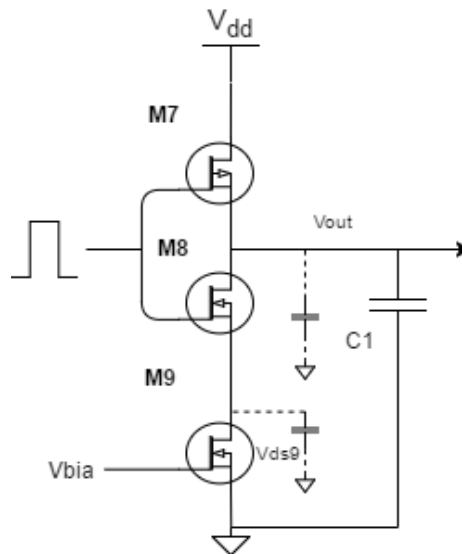


Figure 4: Current Starved Circuit equivalent

In order to have a good performance, the W/L ratio of transistor M8 should be large because the discharging speed of circuit is determined by current through transistor M9 and M8. The time taken to discharge output capacitance from V_{DD} to V_M is simply given by

$$t = C_{out} * \frac{V_{DD}-V_M}{I_{D9}} \quad (2.3)$$

where V_M is the midpoint voltage to define logic 0 and 1.

Because I_{D9} is a variable in the equation, a wide range of the I_{D9} makes a wide range of the fall time of output. Also, it is known that the current of NFET in saturation condition can be represented as

$$I_d = \frac{\beta_n}{2} (V_{GS} - V_{tn})^2 * (1 + \lambda_9 V_{DS9}) \quad (2.4)$$

where

$$\beta_n = k_n \frac{W_{n9}}{L_9} \quad (2.5)$$

The W/L ratio of the transistor partly determines the flowing current.

Also, in equation (2.3), the fall time can be changed by output capacitance. The W/L ratios of transistor M7 and M8 are adjusted based on the simulation result. In this design, M7 is set to 16 μ m wide and 180 nm long while M8 and M9 is set to 12 μ m wide and 180 nm long.

2.3. Calculation on Current Starved Circuit

The fall time of output pulse depends on two parameters, discharging current and output capacitance. In order to find a relationship between V_{bia} , the gate voltage of

transistor M9, and the fall time t_f , we should focus on the calculation of the current passing through transistor M9. In the proposed current starved circuit, the current is controlled by transistor M9. Also, due to Global Foundries 180 nm CMOS technology used in the design, velocity saturated behavior is shown when gate voltage is more than the V_{tn} which is 0.431 V. Therefore, we can consider the following equation to represent the discharging current of output capacitance:

$$i_d = \frac{k_n * W_{n9}}{2L_9} * (V_{bia} - V_{tn})^2 * (1 + \lambda_9 V_{DS9}) \quad (2.6)$$

where k_n is the process transconductance parameter and V_{tn} is the threshold voltage in the saturation regime. Empirical quantity λ_9 is a channel-length modulation parameter with unit of V^{-1} . The equation characterizes the transistor current when the transistor is operating in the saturation region, and it is valid in most of the transition time as the gate voltage of transistor M9 is not much bigger than the threshold voltage V_{tn} . We assume V_{DS9} equals to V_{out} for calculation simplicity because the discharge rate depends mainly on the input voltage of transistor V_{bia} controlling the current limiting transistor M9 [19]. The relationship of V_{out} and the discharging current can be defined by

$$-C \frac{dV_{out}}{dt} = i_d \quad (2.7)$$

where C is output capacitance. And, with initial condition of $V_{out} = V_{dd}$ at $t = 0$, the V_{out} is given in this form:

$$V_{out} = \left(V_{dd} + \frac{1}{\lambda_9} \right) e^{-\frac{t}{c/kn\lambda_9}} - \frac{1}{\lambda_9} \quad (2.8)$$

so that

$$\frac{1 + \lambda_9 V_{out}}{1 + \lambda_9 V_{dd}} = e^{-\frac{t}{c/kn\lambda_9}} \quad (2.9)$$

Moreover

$$-\frac{t}{\frac{c}{kn\lambda_9}} = \ln \frac{1 + \lambda_9 V_{out}}{1 + \lambda_9 V_{dd}} \quad (2.10)$$

At $t = t_f$, $V_{out} = V_m$ [19]. Hence

$$t_f = \frac{C}{K_1 \lambda_9} \ln \frac{1 + \lambda_9 V_{dd}}{1 + \lambda_9 V_m} \quad (2.11)$$

where K_1 is defined by

$$K_1 = \frac{k_n * W_9}{2L_9} (V_{bia} - V_{tn}) \quad (2.12)$$

According to equations shown, we confirm that the output capacitance is in direct proportion to the fall time of output pulse signal while V_{bia} is in inverse proportion to that.

Additionally, in the research, the control unit does not input a voltage source to transistor M9 directly. A Binary Input Array is introduced in Pulse Width Control Module which is described in Chapter 3.

CHAPTER 3: PULSE WIDTH CONTROL MODULE

3.1. Introduction

Pulse Width Control Module is the first part in proposed pulse generator. This is an on-chip design using 180 nm CMOS technology from Global Foundries. By applying binary code and source pulse, pulse width control module outputs pulse in 16 variable widths and adjacent coded output is in approximately linear change. Because the console, the Binary Input Array, is implemented and represented by binary code, the operation is quite straightforward. The input source is a square pulse whose frequency is 2 MHz in the research. To be mentioned, the frequency can be chosen from 0.5 MHz to 10MHz.

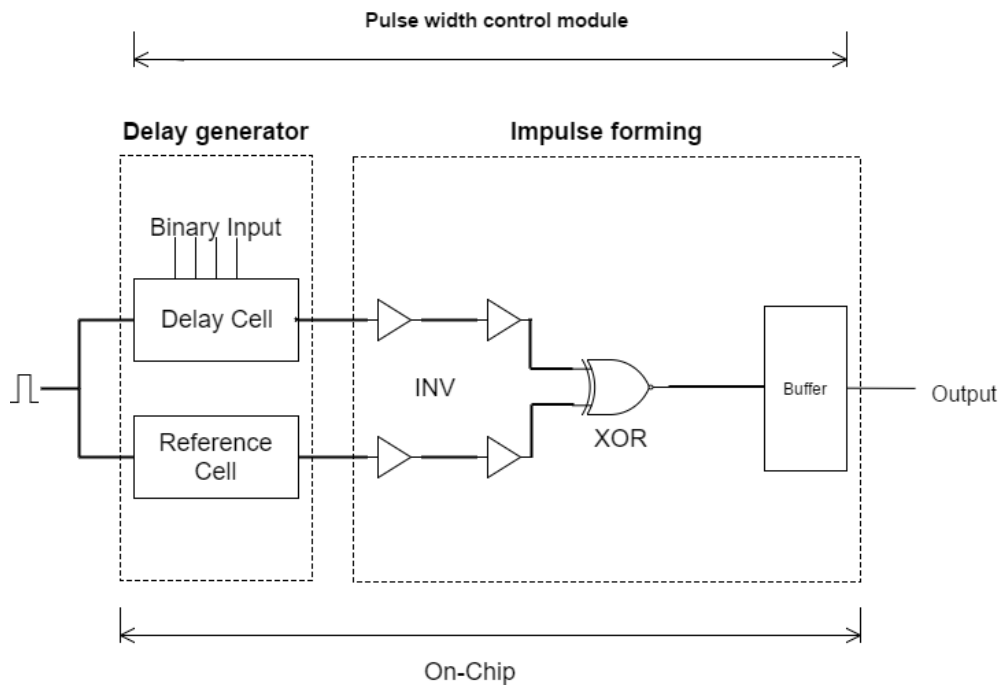


Figure 5: Diagram of Pulse Width Control Module

As Figure 5 shows, the Pulse Width Control Module consists of two essential components, delay generator and impulse forming part. Inputting source signal into delay cell and reference cell, two pulses with different widths are generated. Then, they are transmitted to the Pulse Forming part. Based on a foundational logical operation in Pulse Forming block, a new pulse is generated using exclusive OR gate [4-6]. The pulse width of the output is based on the width difference between two pulses from delay generator. The schematic of Pulse Width Control Module shows as below.

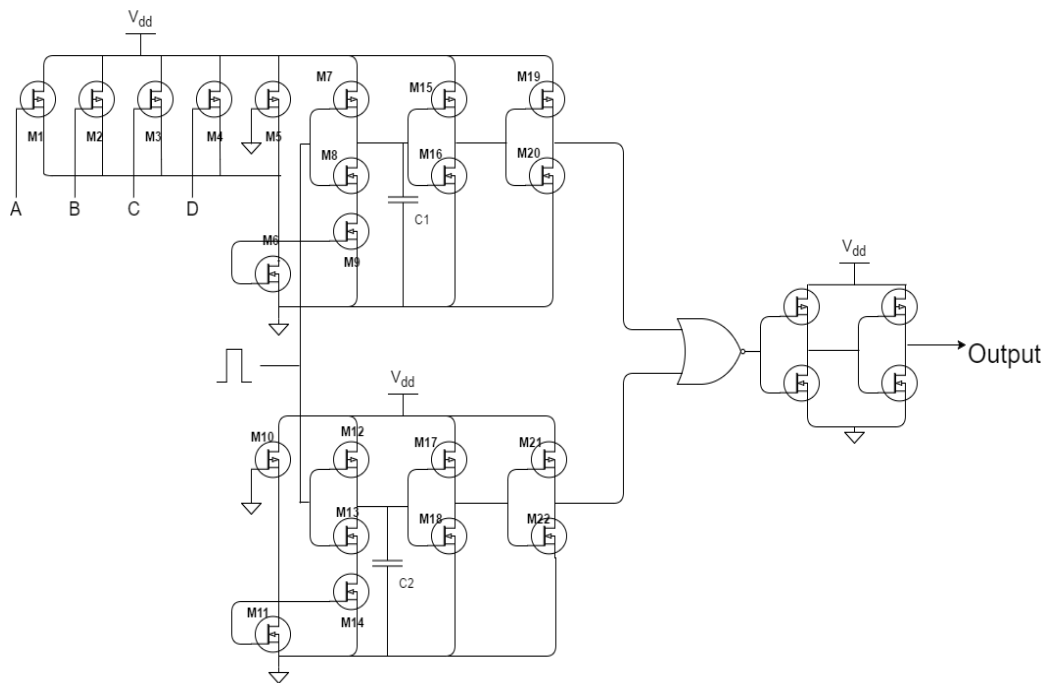


Figure 6: Schematic of Pulse Width Control Module

3.2. Delay Generator

The Delay generator has two components. Delay cell contributes pulse in variable

width while reference cell offers pulse in constant width. They work synchronously and pass processed signals to pulse forming part. Then, the designed pulse is generated and buffered as output signal of Pulse Width Control Module. Delay generator is a critical part for pulse width modulation.

Delay cell and reference cell have similar structure where a proposed current starved circuit and a current mirror circuit are implemented in each cell. Moreover, an extra component named Binary Array Input is designed in the delay cell.

3.2.1 Binary Input Array

The Binary Input Array is the controller in the delay cell, which is also represented as a four-digit binary code. As Figure 7 shows, the controller includes 4 ports. Port A represents the lowest order digit of input code while port D represents the highest order digit, and each port controls a PMOS transistor, from M1 to M4 respectively.

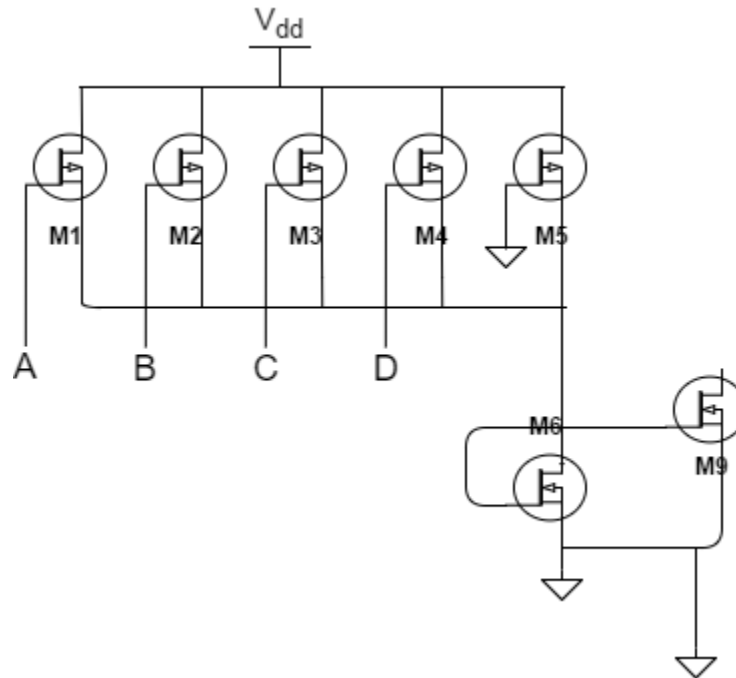


Figure 7: Schematic of Binary Input Array

According to the electrical characteristics of MOEFET, each transistor in Binary Input Array contributes an appropriate current when it is on. According to equation 2.4, we have a function for the current. Because a part of the equation is constant parameter and we intend to find configuration relationship between transistor M1 to M4, the current can be given in the square-law expression equation [18]

$$I_p = \frac{\beta_p}{2} (V_{sg} - |V_{tp}|)^2 \quad (3.1)$$

where

$$\beta_p = k_p \left(\frac{W}{L}\right) \quad (3.2)$$

The equation shows each current through the transistor can be adjusted based on Width/Length ratio of the transistor and we assume that $V_{sg} \approx V_{dd}$ ideally. The proposed design is binary-coded so that transistors M1 to transistor M4 is set in geometric proportions as the Table 1 shows. Additionally, a transistor M5 is added which introduces a basic current as M5 is always on. The size of M5 is detailed in chapter 3.3.

Table 1: Configuration of transistors in input unit

Transistor	W/L ratio
M1	500nm/500nm
M2	1000nm/500nm
M3	2000nm/500nm
M4	4000nm/500nm
M5	2500nm/500nm

A specific current is adjusted and merged by turning on these transistors which will be transmitted to transistor M6. The manipulative current in the circuit is represented as

$$I_{total} = AI_1 + BI_2 + CI_3 + DI_4 + I_5 \quad (3.3)$$

And

$$I_1 : I_2 : I_3 : I_4 = 1 : 2 : 4 : 8 \quad (3.4)$$

In the equation, variable A, B, C and D are the digits of the four-digits binary array and they individually represent whether each transistor is open or not. In other words, they are either one or zero in digital logic. As a conclusion, the array digitally controls the current flowing through NMOS transistor M6.

Further, as it is shown in Figure 7, the current mirror circuit composed of NMOS transistors M6 and M9 is implemented in the module that mirrors the current generated in the Binary Input Array to the current starved circuit. For the better performance, transistor M6 and M9 are in the same configuration. As the current passing through the drain of transistor M6, the gate voltage of M6 is determined. Then, transistor M6 mirrors a constant current based on its gate voltage to transistor M9. The mirrored current, in turn, plays a role in controlling passing current through transistor M9 which is vital in proposed current starved circuit. Hence, we say that the Binary Input Array, which has 16 different codes, controls the proposed current starved circuit in the delay cell.

3.2.2 Delay Cell

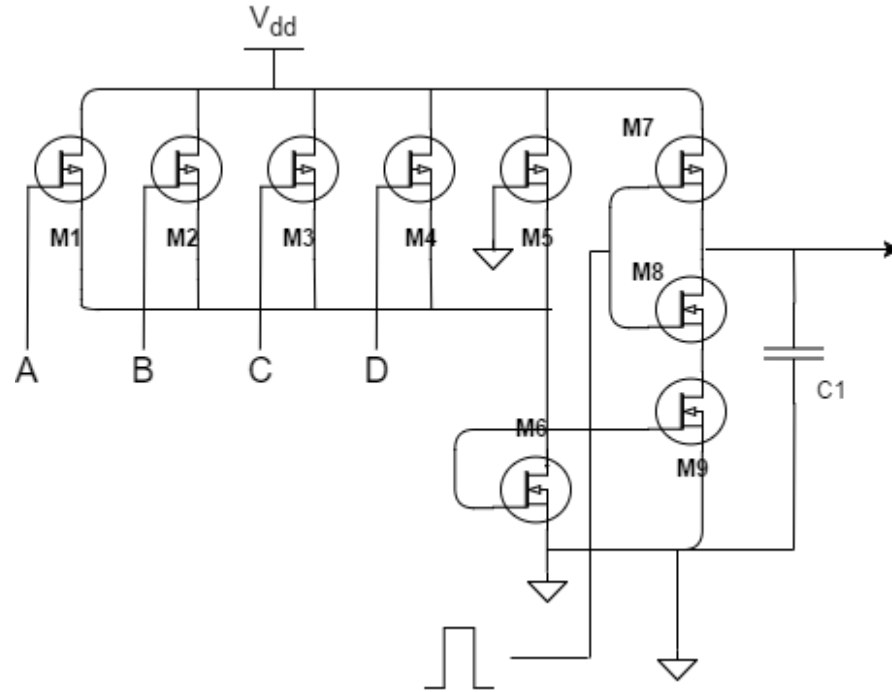


Figure 8: Schematic of Delay Cell

Generally, the delay cell consists of Binary input array and the improved current starved circuit. It is known that Binary Input Array controls discharging current in the improved current starved circuit. So, the improved current starved circuit produces pulses in different delays by controlling discharging current.

We take the whole system into account. In the moment when transistor M8 is on, the output capacitor starts discharging. The discharging current is determined by the passing current through transistor M9 and the passing current is controlled by the gate voltage of M6. As it is described, the current passing through the drain of transistor M6 determines this gate voltage. And we know that the appropriate current consists of current

flows passing through transistor M1 to M5. Besides, transistor M1-M4 is digitally controlled by 4 ports. Thereby, combining four labeled ports (ABCD), the delay cell facilitates the production of 16 different delay values. These ports can be represented together as a four-digit binary code.

To compute the fall time of output pulse generated in delay cell, we can model the system using equations, 2.11 and 2.12. We know that the current passing through transistor M6 is mirrored to transistor M9 so that the discharging current of output capacitance is represented by

$$I_{d1} = I_{total1} \quad (3.5)$$

and we have

$$I_{total1} = AI_1 + BI_2 + CI_3 + DI_4 + I_5 \quad (3.6)$$

$$I_1 : I_2 : I_3 : I_4 = 1 : 2 : 4 : 8 \quad (3.7)$$

then it can be viewed as

$$I_{d1} = (A + 2B + 4C + 8D) * I_1 + I_5 \quad (3.8)$$

Also, we know relationship between gate voltage and I_d of the NMOS transistor in saturation mode is given by

$$I_{d1} = \frac{k_n \left(\frac{W_9}{L_9}\right)}{2} (V_g - V_{tn})^2 * (1 + \lambda_9 V_{DS_9}) \quad (3.9)$$

Thus, V_{g1} can be found from the following

$$V_{g1} = V_{tn} + m_1 \sqrt{I_{d1}} \quad (3.10)$$

where m_1 is

$$m_1 = \sqrt{\frac{2L_9}{k_n * W_9 * (1 + \lambda_9 V_{DS_9})}} \quad (3.11)$$

Based on the configuration of transistor M5, V_{g1} is always bigger than V_{tn} as the prerequisites in this model.

Also, the fall time can be given in a function of the gate voltage of transistor M9.

That is the combination of equation 2.9 and 2.10:

$$t_{f1} = \frac{C_1}{\frac{k_n * W_9}{2L_9} (V_{g1} - V_{tn}) \lambda_9} \ln \frac{1 + \lambda_9 V_{dd}}{1 + \lambda_9 V_m} \quad (3.12)$$

and it can be written in a simple form

$$t_{f1} = \frac{m_2}{V_{g1} - V_{tn}} \quad (3.13)$$

where m_2 is constant that

$$m_2 = \frac{2C_1 * L_9}{k_n * W_9 * \lambda_9} \ln \frac{1 + \lambda_9 V_{dd}}{1 + \lambda_9 V_m} \quad (3.14)$$

And the delay cell generates outputs based on the 4 input ports. So that we can have the fall time of output in a function of input variables, and it can be represented by integrating t_{f1} function and V_{g1} function. And we have

$$t_{f1} = \frac{m_2}{m_1 \sqrt{(A+2B+4C+8D) * I_1 + I_5}} \quad (3.15)$$

Nevertheless, the output pulse of Pulse Width Control Module does not simply depend on the delay cell. The reference cell also plays a critical role in the whole module. And, the pulse width of output is generated in impulse forming part based on difference between two cells.

3.2.3 Reference Cell

Reference cell is similar to delay cell in the structure. It processes the source pulse using proposed current starved circuit. Also, the current starved circuit is indirectly

controlled by the passing current of transistor M10, which is the same as how delay cell works. The architecture of the reference cell shows in Figure 9,

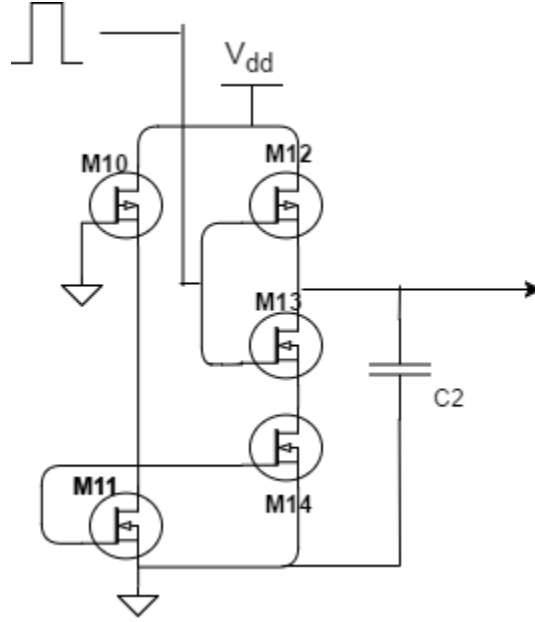


Figure 9: Schematic of Reference Cell

As we see in the Figure 9, because the gate connects to ground, the PMOS transistor M10 whose width/length ratio is set to 2000nm/500nm, is always on. The constant current passing through the M10 can be represented as

$$I_{total2} = I_{10} \quad (3.16)$$

and with $I_{total2} = I_{d2}$, we can have a function for the gate voltage of NMOS transistor M14

$$V_{g2} = V_{tn} + n_1 \sqrt{I_{d2}} \quad (3.17)$$

where n_1 is

$$n_1 = \sqrt{\frac{2L_{14}}{k_n * W_{14} * (1 + \lambda_{14} V_{DS14})}} \quad (3.18)$$

Further, the fall time can be given in a function of the gate voltage of transistor M14. That is

$$t_{f2} = \frac{C_2}{\frac{k_n * W_{14}}{2L_{14}} * (V_{g2} - V_{tn}) * \lambda_{14}} \ln \frac{1 + \lambda_{14} V_{dd}}{1 + \lambda_{14} V_m} \quad (3.19)$$

and the simple form is

$$t_{f2} = \frac{n_2}{V_{g2} - V_{tn}} \quad (3.20)$$

that

$$n_2 = \frac{2C_2 * L_{14}}{k_n * W_{14} * \lambda_{14}} \ln \frac{1 + \lambda_{14} V_{dd}}{1 + \lambda_{14} V_m} \quad (3.21)$$

Likewise, t_{f2} can be represented in a simple form

$$t_{f2} = \frac{n_2}{n_1 * \sqrt{I_{10}}} \quad (3.22)$$

Thus, two pulses are generated synchronously in Delay Generator and they are transmitted separately into Impulse Forming part as inputs in the same time.

3.3. Impulse Forming

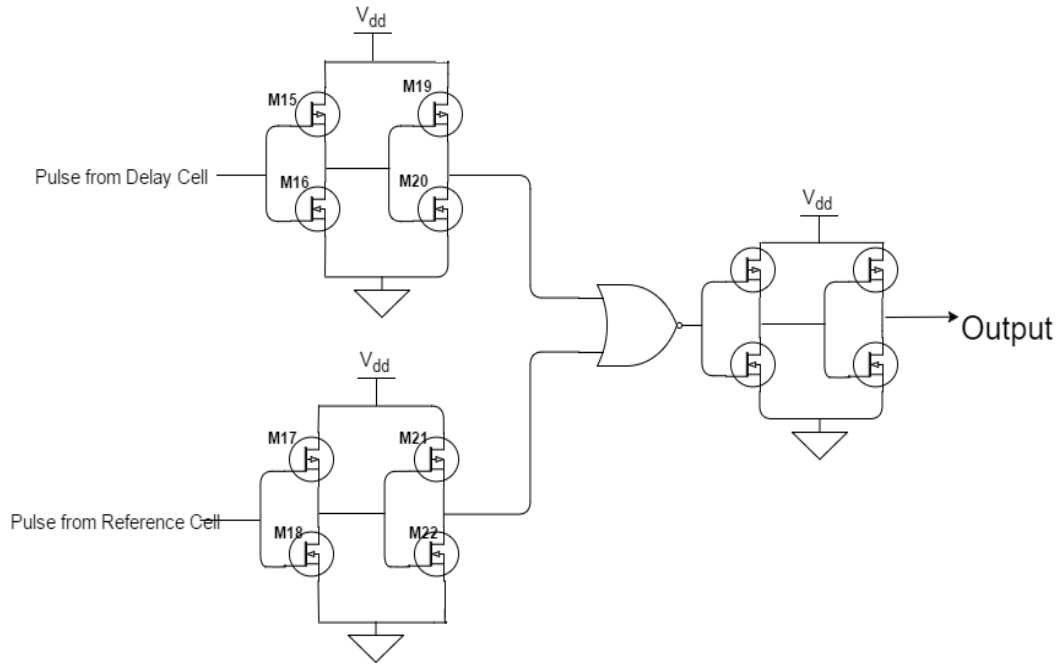


Figure 10: Schematic of Impulse Forming

The Impulse Forming part consists of two parallel inverters, Exclusive OR gate and a pair of inverters. Pulses from the delay cell and the reference cell are transmitted into inverters, continuously. Each block of inverters works as square wave generation which is to generate a square-wave signal. Each input signal will be sharpened through these inverters. In other words, input pulse with large transition time will be a signal with very short transition time, and the pulse width is approximately same. In Figure 11, the brown line shows the output signal of delay cell and the red one is the square-wave pulse. The midpoint of the falling edge is almost same so we can confirm that these pulses are in the equal pulse width. Besides, these inverters increase the driving capabilities to the following part.

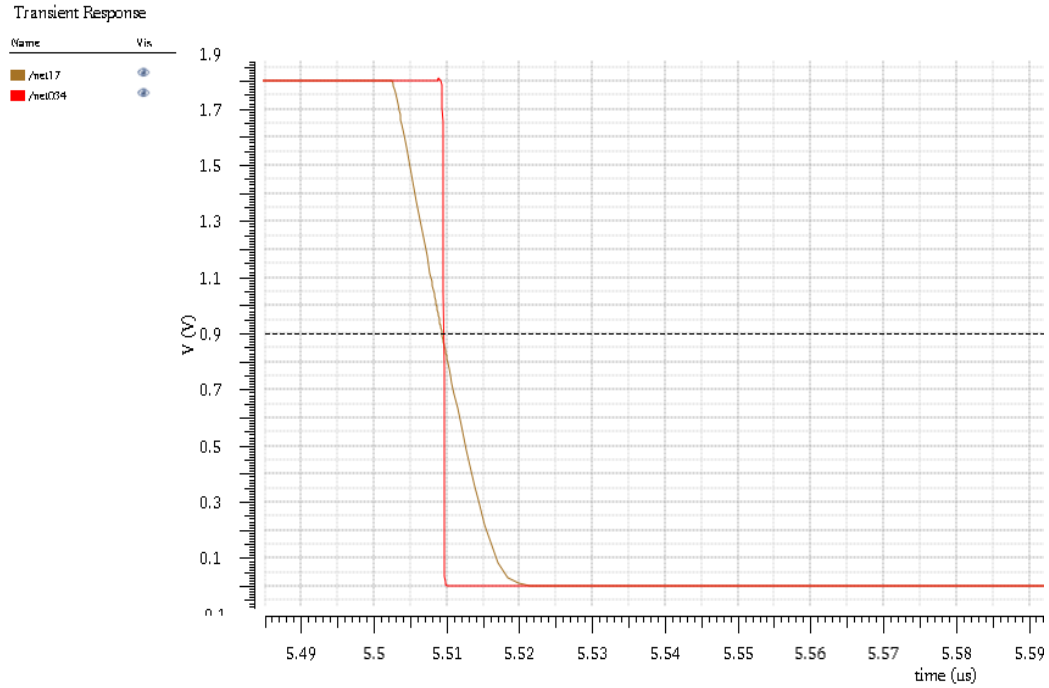


Figure 11: Difference between the falling edges of input signal and square-wave signal

The next stage is the key part in the Pulse Width Control Module which generates pulse in desired pulse width. Two pulses with different widths are inputted to Exclusive OR gate, and output is generated by the gate. The pulse width of output is based on the difference between pulse widths of two inputs. The detailed schematic of Exclusive OR gate is shown in Figure 12, and all transistors are in same the Width/Length ratio. The transition time of mirror circuit design is smaller than that of AND-OR-Invert network design because it has smaller parasitic capacitance. Additionally, the layout of circuit is more symmetric [19].

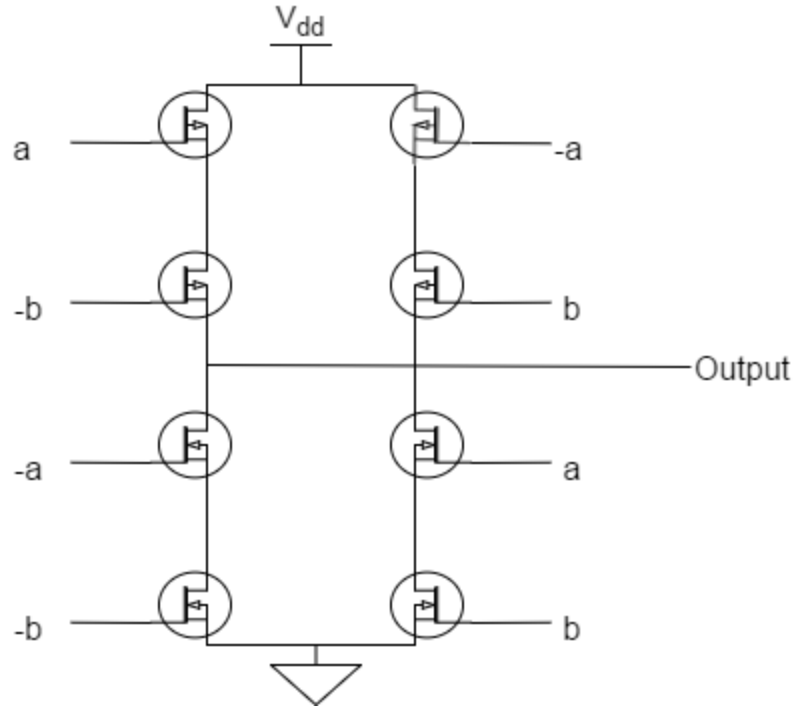


Figure 12: Schematic of Exclusive OR gate

Also, the logical operation of Exclusive OR gate is shown in Table 2 and it is confirmed by the simulation result shown in Figure 13.

Table 2: True Table of Exclusive OR gate

Input		Output
A	B	A XOR B
0	0	0
0	1	1
1	0	1
1	1	0

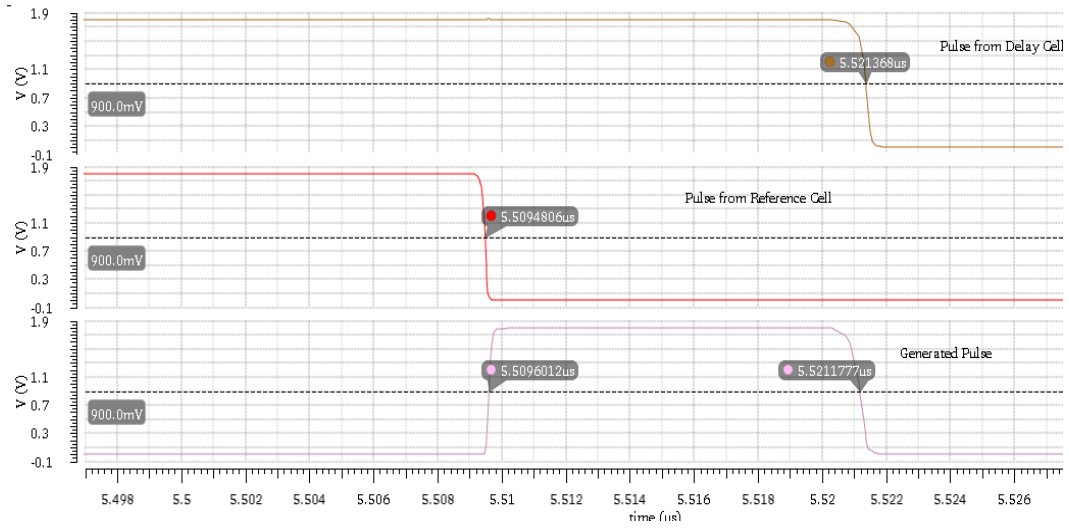


Figure 13: Logic simulation of Impulse Forming part

For the better performance, optimization is needed. To optimize the module, we figure out calculations on it. According to result shown in Figure 13, we can assume that the pulse width of output can be ideally represented as

$$t_{width} = |t_{f1} - t_{f2}| \quad (3.23)$$

combing with equation 3.15 and equation 3.22, it can be written as

$$t_{width} = \left| \frac{m_2}{m_1 \sqrt{(A+2B+4C+8D)*I_1+I_5}} - \frac{n_2}{n_1 * \sqrt{I_{10}}} \right| \quad (3.24)$$

Meanwhile, we know the NMOS transistor M9 is in the same size of NMOS transistor M14. Then, we can simplify the equation as

$$t_{width} = p * \left| \frac{C_1}{\sqrt{(A+2B+4C+8D)*I_1+I_5}} - \frac{C_2}{\sqrt{I_{10}}} \right| \quad (3.25)$$

where p is constant.

In the equation, proposed pulse width is in inverse proportion to current which is in direct proportion to binary code. The completely linearity increment for outputs is

impossible to realize in the design. However, the approximately linearity can be achieved by optimization.

The equation shows that optimization depends on two output capacitors and two base currents I_5 and I_{10} . As a result, we set them as Table 3:

Table 3: Proposed setting

C1	5p
C2	1p
W/L ratio of M5	2500n/500n
W/L ratio of M10	2000n/500n

In figure 14, the last stage of impulse forming part is a pair of inverters which increases driving capability for the following module. Because of impedance mismatch, the output amplitude drops intensely without using buffer circuit. As a result, generated pulse cannot drive Pulse Amplitude Control Module directly.

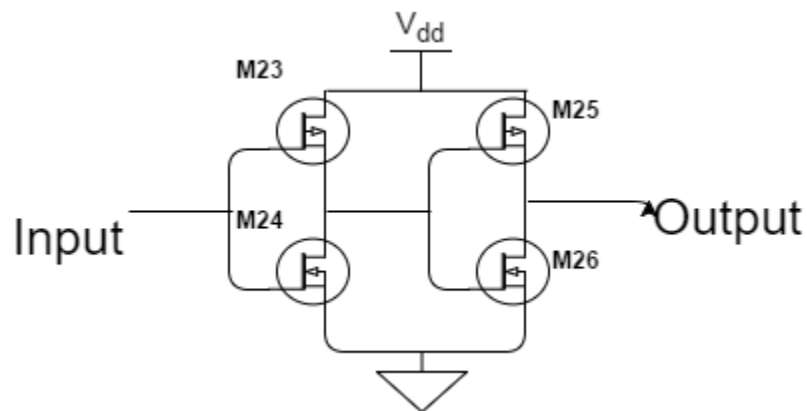


Figure 14: Schematic of Buffer circuit

And

Table 4: Configuration of Buffer circuit

M23	500n/180n
M24	500n/180n
M25	3000n/180n
M26	2000n/180n

Figure 15 shows output in open load and output which is transmitted to a NPN transistor. We confirm that Pulse Width Control Module has capability to generate a 1.18V pulse in designed pulse width (it is almost same as the pulse generated by Exclusive OR gate).

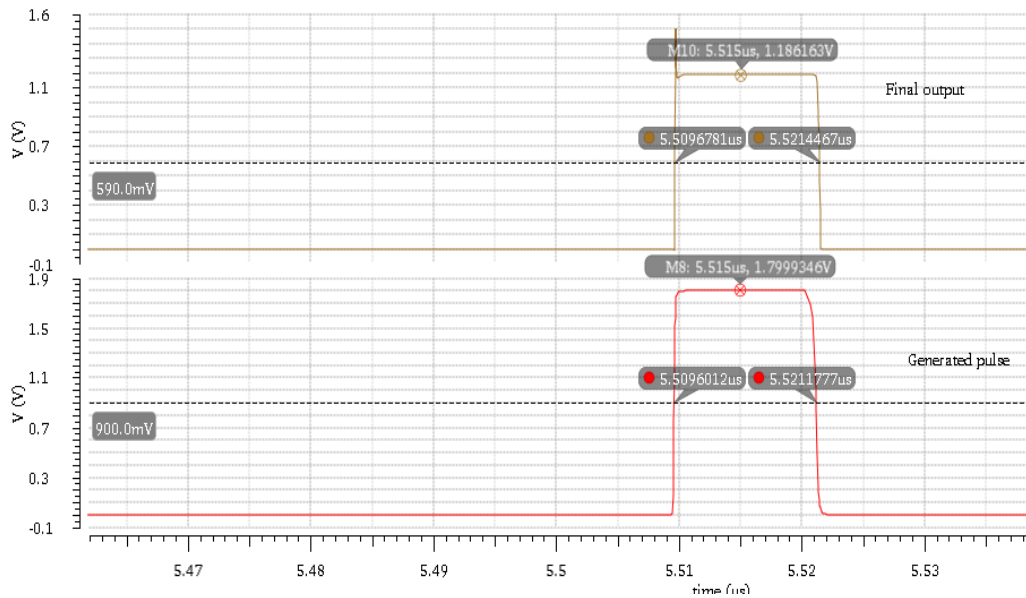


Figure 15: Final pulse and generated pulse

3.4. Layout

The Pulse Width Control Module is an On-chip design so that layout is essential in this research. The layout is designed based on the CMHV7SF design manual from GlobalFoundries. The layout includes four levels, AM, MT, M1 and M2, and its length is 282 μm while the width is 168 μm . Figure 16 shows the whole view. The layout utilized multi-fingered design which provides more flexibility and better matching of transistors. The size of the layout is smaller than that of the layout using single finger.

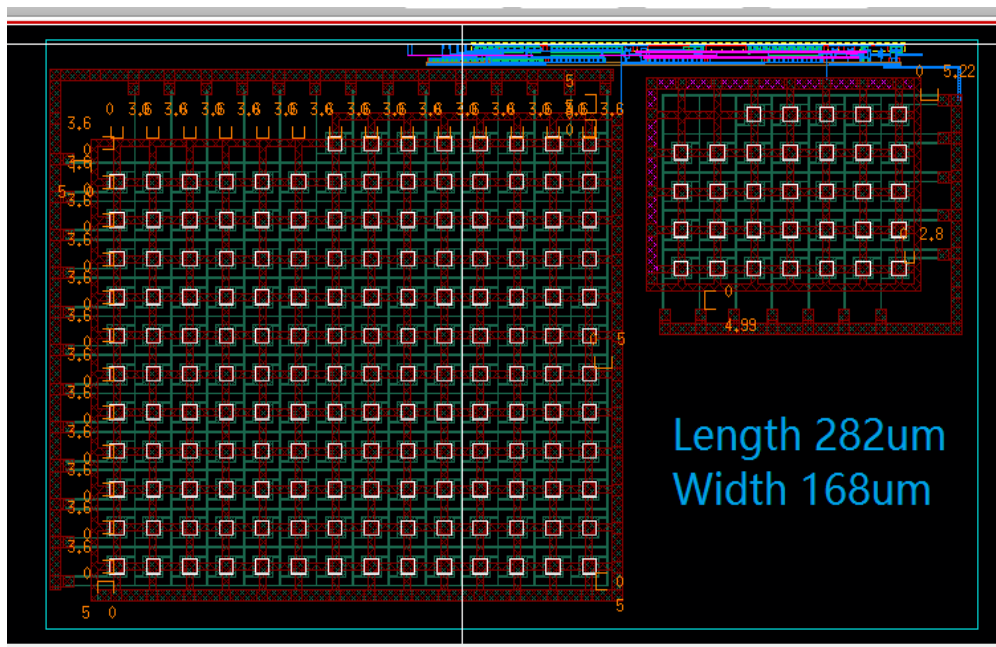


Figure 16: Layout of Pulse Width Control Module

In Figure 16, two capacitors occupy most area of the module. Several Metal-Insulator-Metal capacitors are connected to work as one high-value capacitor for performance improvement, as Figure 17 shows. In a single MIM capacitor, MT is the bottom level and AM is the top level.

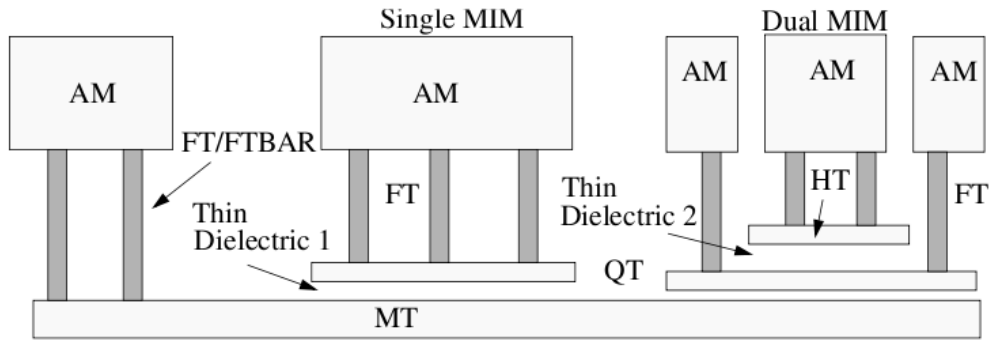


Figure 17: Cross Section of a MIM capacitor structure [21]

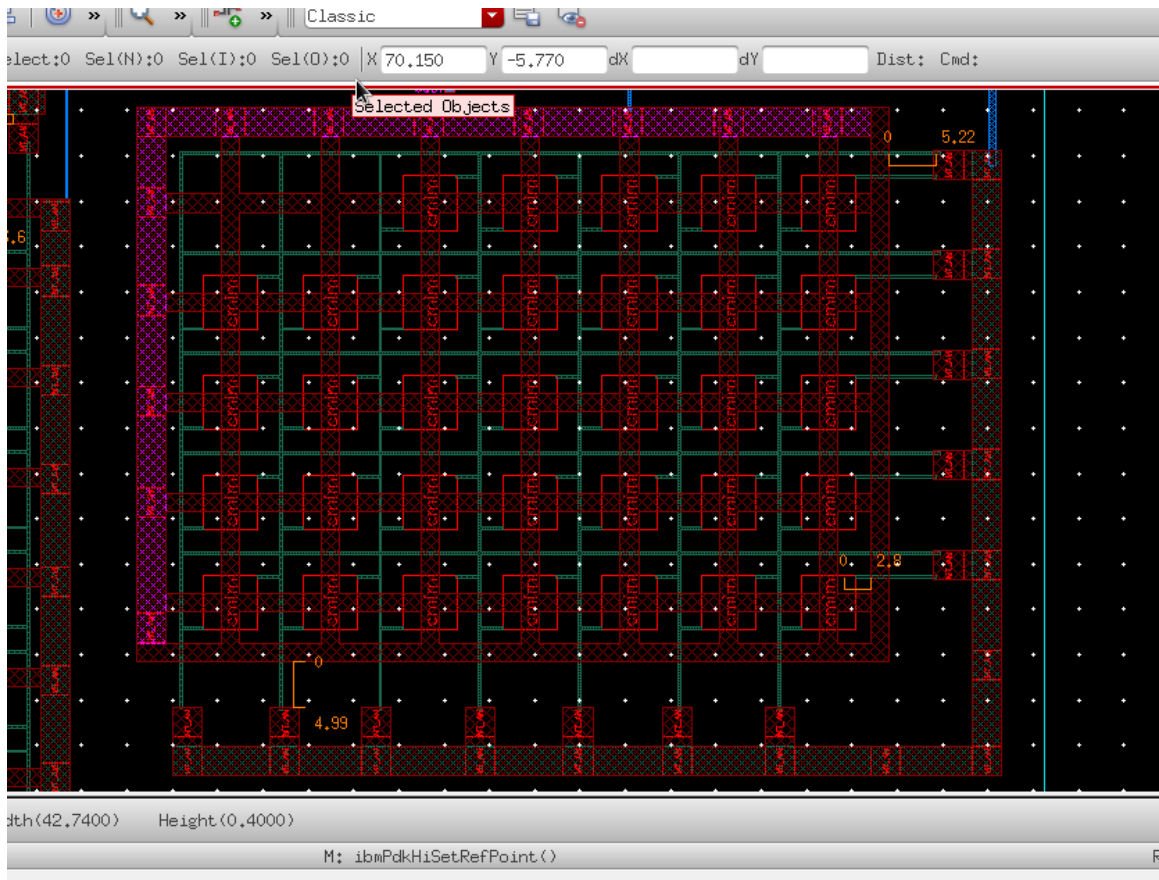


Figure 18: Layout of capacitors

For avoiding charging damage during processing, it is required that the MT level of MIM capacitor must connect to the level of metal which is wired to the AM level before connecting to lower metal levels [22], as Figure 18 shows.

Compact PFET layout is supported by the technology and it is utilized in the design, as Figure 19-21 show. By placing multiple PFETs in a common N-well, the layout is more compact which means smaller size.

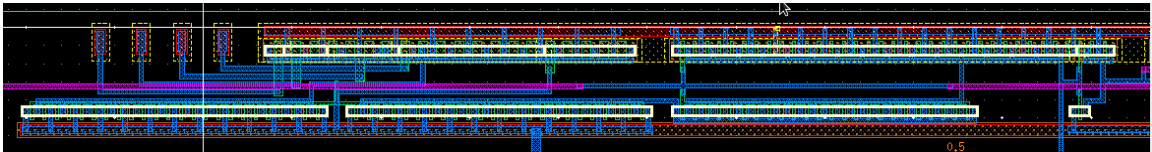


Figure 19: Layout of Delay Cell

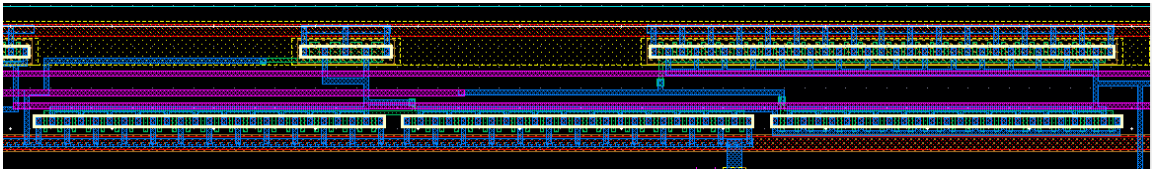


Figure 20: Layout of Reference Cell

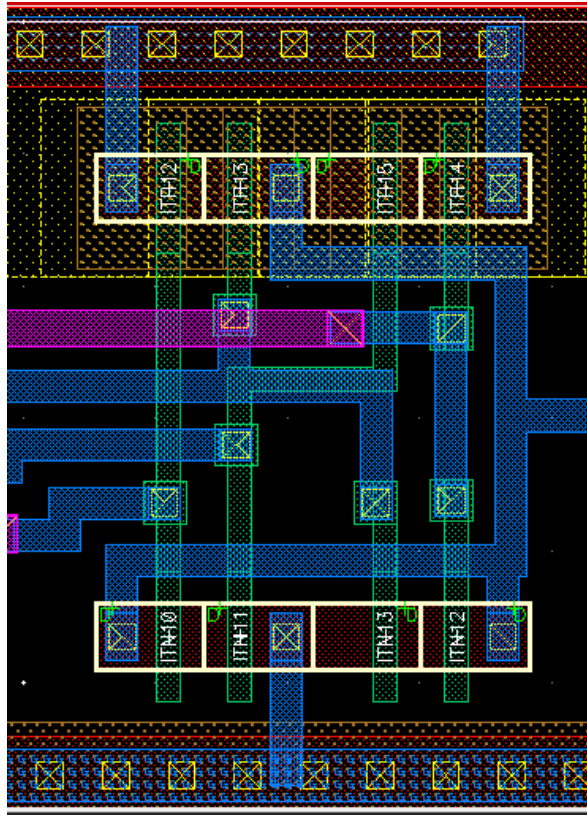


Figure 21: Layout of Exclusive OR gate

Both DRC (design rule checking) and LVS (layout versus schematic) are clean which are confirmed by following figures. The checking is operated using Assura tool.

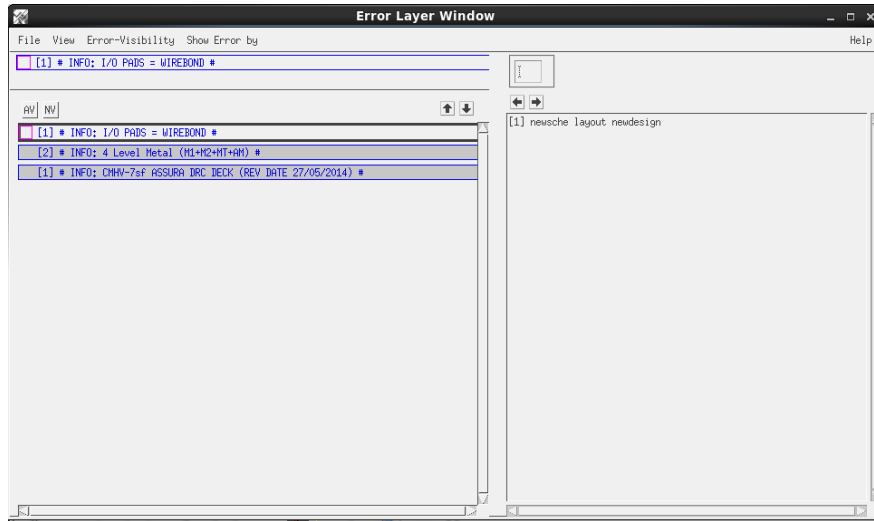


Figure 22: Design Rule Checking

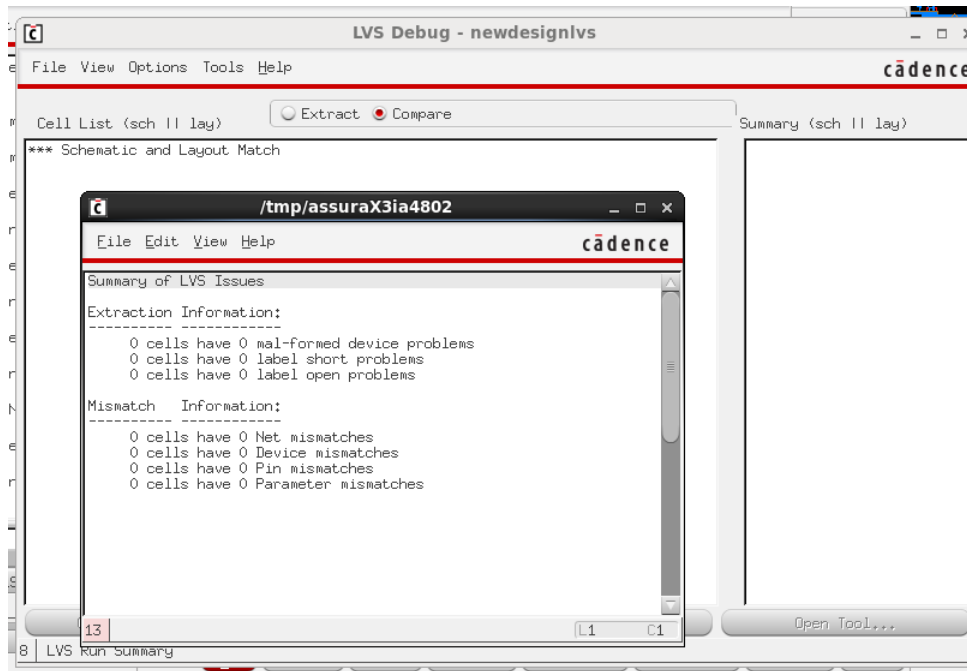


Figure 23: Layout Versus Schematic

CHAPTER 4: SIMULATION OF PULSE WIDTH CONTROL MODULE

4.1. Introduction

The module is an On-chip design and the simulation result is captured by Cadence Virtuoso. Virtuoso Analog Design Environment is the advanced design and simulation tool. It offers advanced parasitic estimation and comparison flow and optimization that help users to center design better for yield improvement and advanced matching and sensitivity analyses. Also, it is with an easy function to export data points which can be used as input data for the following module simulation.

4.2. Simulation Setting

The module is connected to an amplifier using NPN transistor in CM7HVSF technology in order to measure the practical output, the result data are captured in the output node between the buffer and the amplifier. The simulation setting is shown in Figure 24.

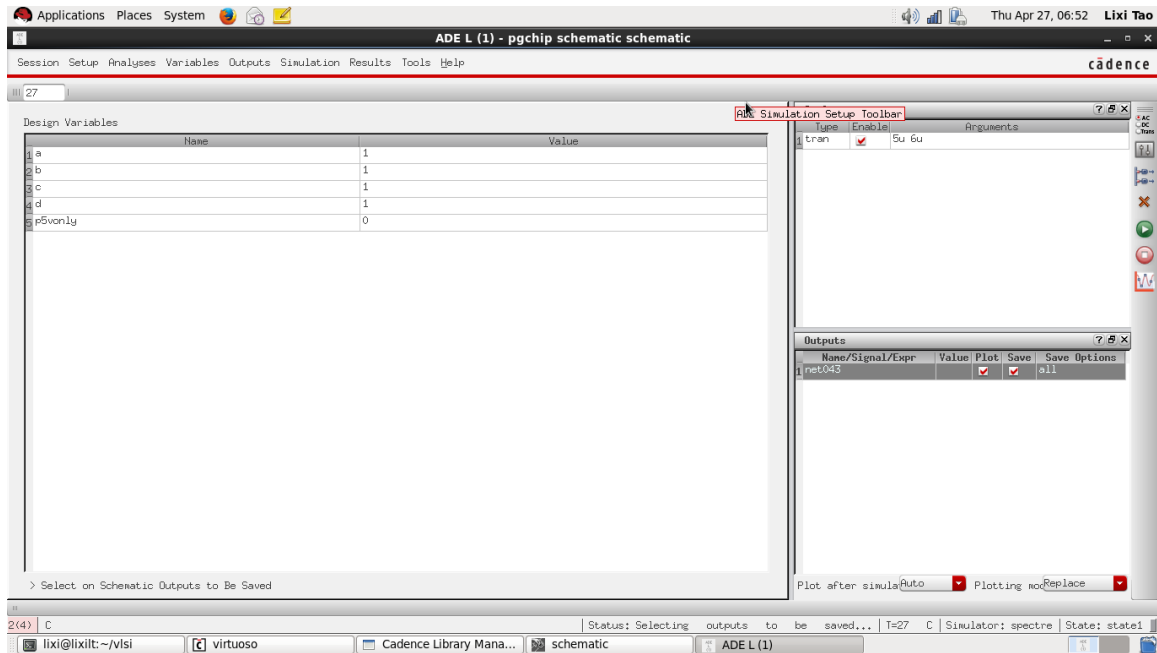


Figure 24: Simulation setting

It is simulated by Spectre, a circuit simulator, implanted in Cadence Virtuoso where the transient mode is applied. The simulation is operated under the default temperature, as Figure 25 shows. Four variable, a and b and c and d, represents the Binary Input Array. Variables are set to either one or zero, one represents high level while zero is low. Also, parametric analysis tool is used in the simulation in order to compare all results.

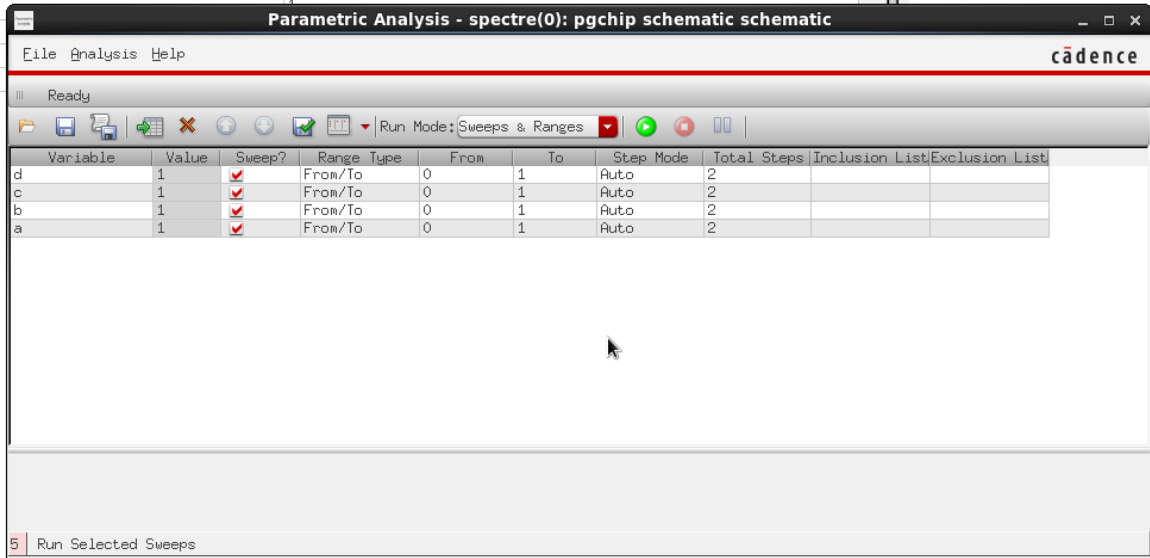


Figure 25: Parametric Analysis setting

4.3. Result

Because the module contains four variable inputs, 16 different pulses can be generated and they are shown in simulation by using parametric analysis tool. In Figure 26, the pulses are labelled from 0000 to 1111.

4.3.1 Pulse width

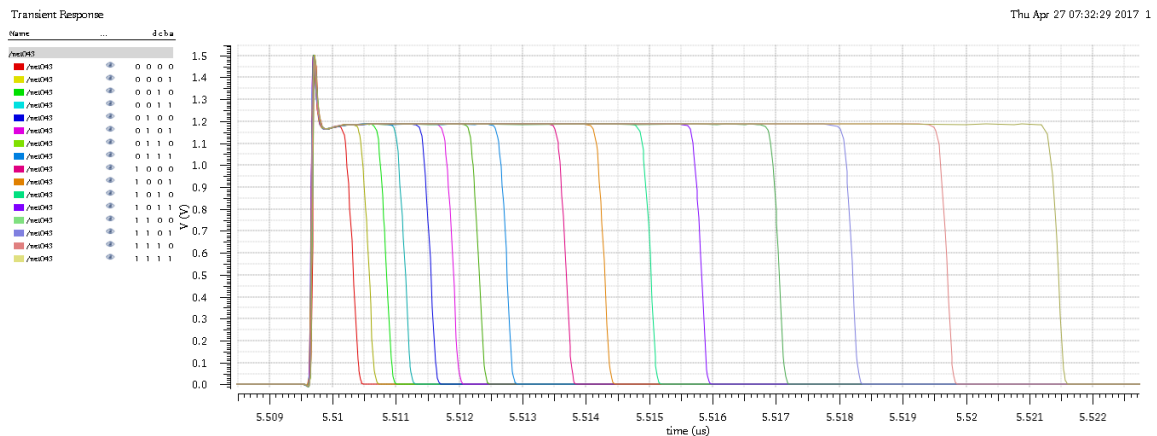


Figure 26: Output results

In Figure 26, each pulse is with low transition time which is a tiny part of pulse width. The rise time is 0.0325 ns while the fall time is 0.2096 ns so that pulses are in symmetric shape and sharp edge, respectively. The transition time is mainly dependent on the buffer circuit and the electrical characteristics of transistor.

As it is proposed in chapter 1, the Pulse Width Control Module is to realize tunable pulse width with linearity and its range is from 1ns to 10ns. In the simulation, the module generates 16 pulses with different pulse width ranging from 0.6333 ns to 11.7678 ns. The data are listed in Table 5.

Table 5: Pulse width of outputs

Binary Code	Pulse width(ns)	Binary Code	Pulse width(ns)
0000	0.6333	1000	4.017
0001	0.8918	1001	4.6245
0010	1.1736	1010	5.3361
0011	1.4616	1011	6.1481
0100	1.8769	1100	7.3743
0101	2.235	1101	9.1316
0110	2.6422	1110	10.0239
0111	3.0853	1111	11.7678

Due to relationships between discharging current and fall time of output in proposed current starved circuit, it is impossible to realize completely linear increment in pulse width. However, output is in approximate linearity as Figure 27 shows.

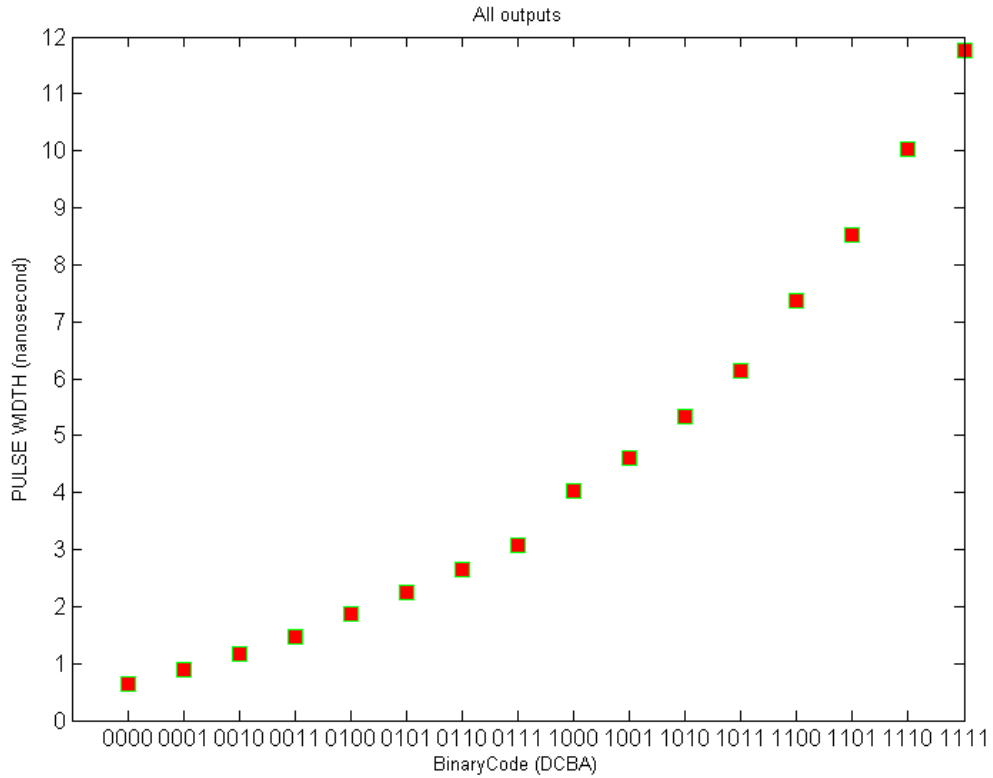


Figure 27: pulse width of outputs

Increment of pulse width increases as code increase. Because the fall time of pulse is in inverse proportion to the discharging speed of transistor in current starved circuit, the shape of wire connecting all pulse points tends to be curved. By optimizing the parameters of transistors and capacitor as we described in chapter 3, the curve can be adjusted to an approximately straight shape.

4.3.2 Power consumption

Power consumption is an important parameter of the model. Power consumption in each transistor can be given in the form

$$P = P_{DC} + P_{dyn} \quad (4.1)$$

that P_{DC} is the static term and P_{dyn} is the dynamic term. They can be represented in following equations

$$P_{DC} = I_{DD} * V_{DD} \quad (4.2)$$

where I_{DD} is DC current from power supply. And

$$P_{dyn} = C * V_{DD}^2 * f \quad (4.3)$$

Thus, total power is

$$P = I_{DD} * V_{DD} + C * V_{DD}^2 * f \quad (4.4)$$

In simulation, the total power consumption can be presented in Virtuoso Analog Design Environment, as Figure 28 shows.

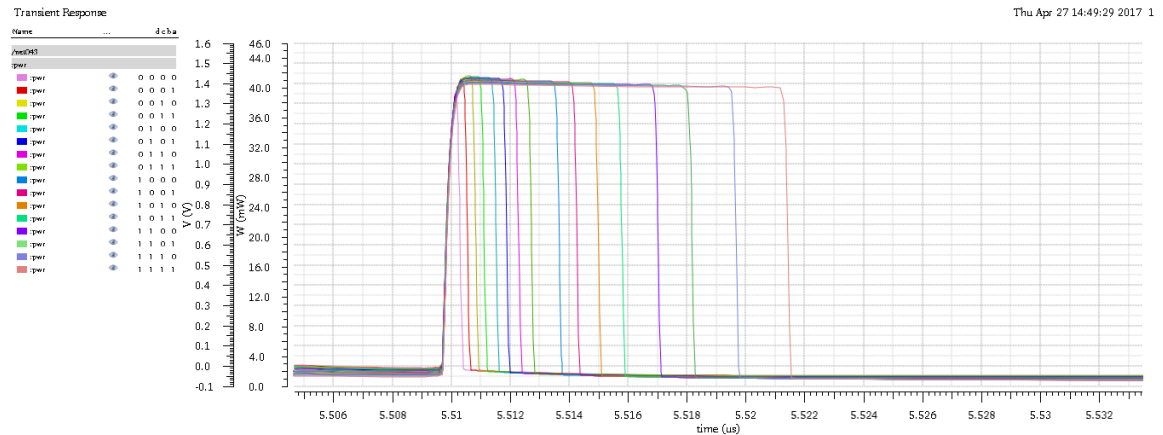


Figure 28: Power consumptions in a period

Data is captured using Calculator in Virtuoso Analog Design Environment. It is shown in Table 6.

Table 6: Total power consumption

Binary Code	Power consumption	Binary Code	Power consumption
0000	1.461 mW	1000	1.025 mW
0001	1.414 mW	1001	0.978 mW
0010	1.365 mW	1010	0.927 mW
0011	1.318 mW	1011	0.879 mW
0100	1.257 mW	1100	0.817 mW
0101	1.210 mW	1101	0.769 mW
0110	1.160 mW	1110	0.718 mW
0111	1.113 mW	1111	0.669 mW

In the Table 6, the power consumption of the module ranges from 0.669 mW to 1.461 Mw. As it is described in chapter 3, PFET is the basic element in Binary Input Array so that the power consumption of the module is highest when 0000 is applied.

4.3.3 Post Layout Simulation

The post layout simulation is also taken into account and it is shown in Figure 29.

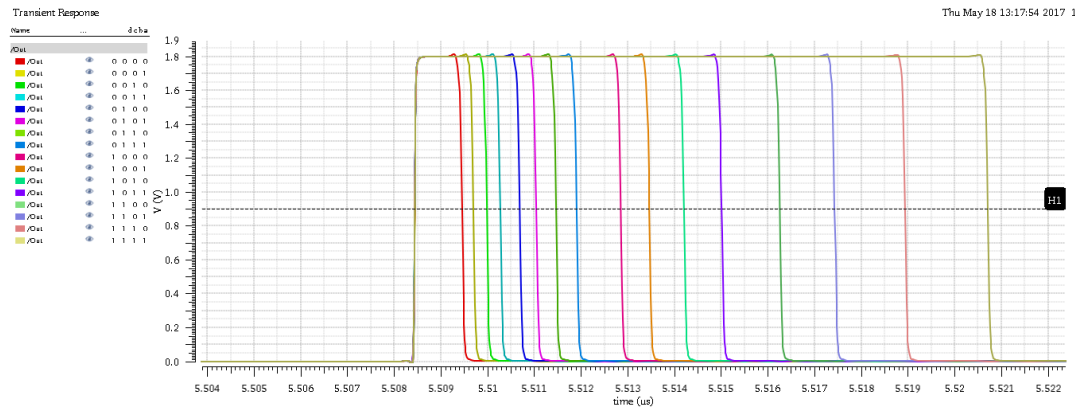


Figure 29: Result of Post layout simulation

Two groups of samples are showed in Figure 30 for showing the difference between pre-layout simulation and post-layout simulation.

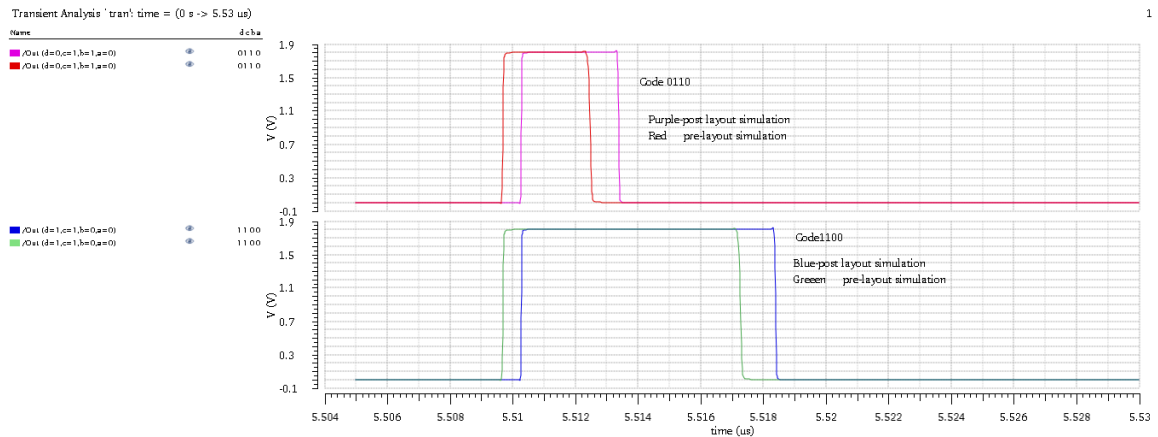


Figure 30: Layout based simulation Versus Schematic based simulation

Obviously, pulses are shifted as Figure 30 shows. In layout based simulation, capacitance of each element is changed. This also introduces the gently increment in transition time. The result of the layout-based simulation is addressed in Table 7.

Table 7: Pulse width of the layout based outputs

Binary Code	Pulse width(ns)	Binary Code	Pulse width(ns)
0000	0.6890	1000	4.1714
0001	1.0221	1001	4.7832
0010	1.3050	1010	5.5195
0011	1.5962	1011	6.3293
0100	2.0102	1100	7.5750
0101	2.3673	1101	8.7542
0110	2.7816	1110	10.2657
0111	3.2237	1111	12.0473

Increments are shown by comparing Table 5 and Table 7. The maximum is about 0.2795 ns which is 2.37% based on pulse width of output in the schematic-based simulation. And, the minimum is about 0.0557 ns which is 8.79% based on data in Table 5. As a conclusion, the layout-based simulation presents similar result as the schematic-based simulation does.

CHAPTER 5: PULSE AMPLITUDE CONTROL MODULE

5.1. Introduction

The Pulse Amplitude Control Module is an off-chip design following the Pulse Width Control Module, as Figure 31 shows. Pulse is amplified in this module using NPN transistor 2SC5551A and the output is in variable amplitude based on the power supply value applied. Meanwhile, output is in low distortion when relatively low pulse width change is produced.

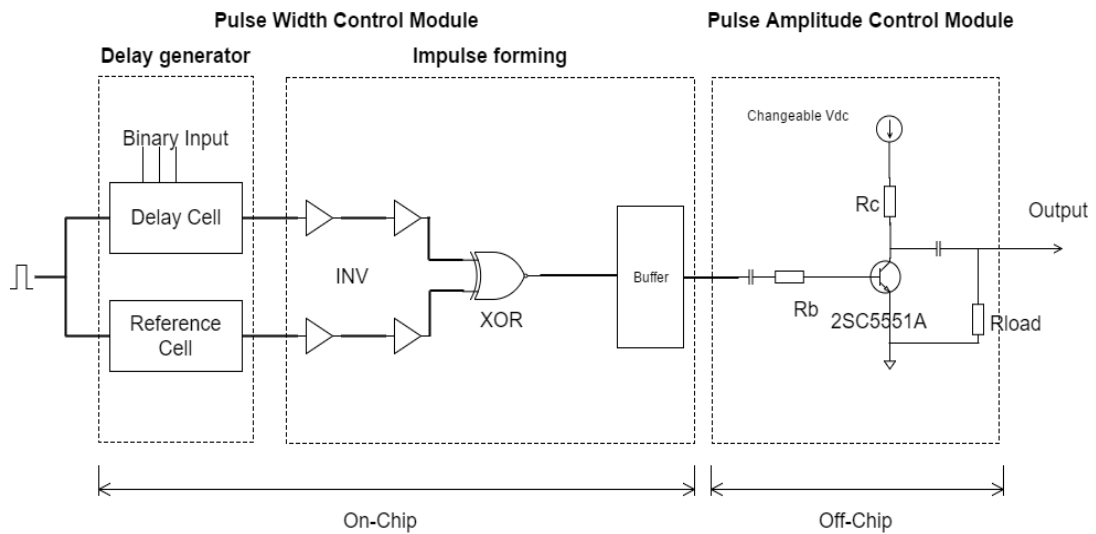


Figure 31: Diagram of Proposed pulse generator

5.2 Proposed Design

The Figure 32 shows that the schematic of design is a bipolar junction transistor-based circuit and it is implemented in Printed Circuit Board (PCB).

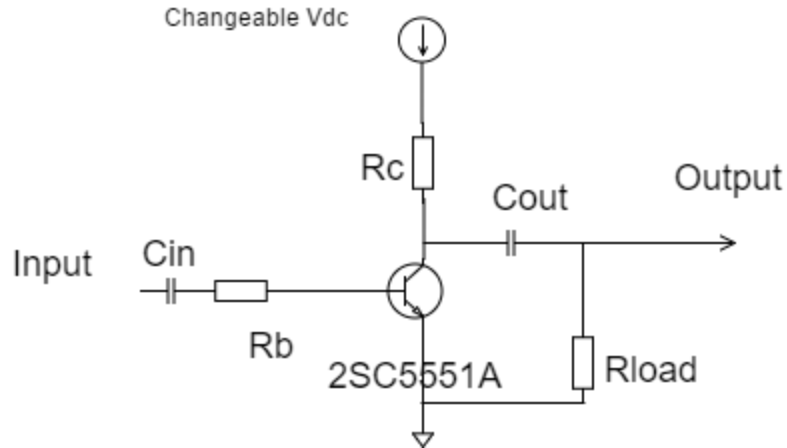


Figure 32: Schematic of amplifier

The module can be viewed as an amplifier using NPN bipolar junction transistor. Initially, when the input signal is zero, the transistor is in OFF-state and the capacitor C_{out} charged through power supply V_{dc} . Via resistor R_c and R_{load} , it is charged to approximately the supply voltage V_{dc} . After the input signal reaches positive threshold value, the transistor is suddenly switched to ON-state. Simultaneously, the capacitor C_{out} starts discharging and the stored energy is released through the transistor and R_{load} . A high current is flowing in this time and a negative voltage pulse is produced on R_{load} . In the design, the rise time of output pulse is mainly dependent on the switching speed of the transistor, while the pulse amplitude and the fall time are determined by V_{dc} , C_{out} and R_{load} . In Ground Penetrating Radar System, antenna is the R_{load} to pulse generator and it is typically designed of 50Ω impedance. Also, C_{in} and R_b determine the trigger signal in the circuit.

There are a lot of choices for transistor as the main body of the module. According

to the objectives described in Chapter 1, a transistor with wide range of pulse amplitude and high sensitivity is needed in the design. 2SC5551A is chosen under these constraints. The transistor 2SC5551A is a RF transistor which supports high frequency up to 3.5 GHz. Meanwhile, the current passing through the transistor is up to 300 mA and the maximum power is 1.3 Watt which is acceptable. The data measured at 25 °C are detailed in Table 8 and Table 9:

Table 8: Absolute Maximum Ratings of 2SC5551A [23]

Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	V_{CBO}		40	V
Collector-to-Emitter Voltage	V_{CEO}		30	V
Emitter-to-Base Voltage	V_{EBO}		2	V
Collector Current	I_C		300	mA
Collector Current (Pulse)	I_{CP}		600	mA
Collector Dissipation	P_C	When mounted on ceramic substrate	1.3	W
Junction Temperature	T_j		150	°C
Storage Temperature	T_{stg}		-55 to +150	°C

Table 9: Electrical Characteristics of 2SC5551A [23]

Parameter	Symbol	Conditions	Ratings			Unit
Collector Cutoff Current	I_{CBO}	$V_{CB} = 20V$ $I_E = 0A$			1.0	μA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 1V$ $I_C = 0A$			5.0	μA
DC Current Gain	h_{FE}^1	$V_{CE} = 5V$ $I_C = 50mA$	90		270	
	h_{FE}^2	$V_{CE} = 5V$ $I_C = 300mA$	20			
Gain-Bandwidth Product	f_T	$V_{CE} = 5V$ $I_C = 50mA$		3.5		GHZ
Output Capacitance	C_{ob}	$V_{CB} = 10V$		2.9	4.0	pF
Reverse Transfer Capacitance	C_{re}	$f = 1MHz$		1.5		pF
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	$I_C = 50mA$ $I_B = 5mA$		0.07	0.3	V
Base-to-Emitter Saturation Voltage	$V_{BE}(at)$	$I_C = 50mA$ $I_B = 5mA$		0.8	1.2	V

Based on the simulation, an extremely small current is observed which is passing through resistor R_c and R_{load} when the transistor is in OFF-state. As a result, the output pulse has a positive value for the current flowing through Resistor R_{load} . The constant current is similarly represented as

$$I_i = \frac{V_{dc}}{(R_c + R_L)} \quad (5.1)$$

Because of the constant current flowing through R_c , the capacitor C_{out} and R_{load} , the initial voltage of the capacitor C_{out} is represented as

$$V_{c_{out}} = V_{dc} - I_i * R_c \quad (5.2)$$

which is almost same as the voltage amplitude of the output. Based on equation 5.1 and 5.2, the resistor R_c is set to have the current as tiny as possible and the initial voltage of the output capacitor as large as possible. In the research, resistor R_c is set to 300 Ω .

The pulse amplitude in stable working situation is less than that in early time as Figure 33 shows

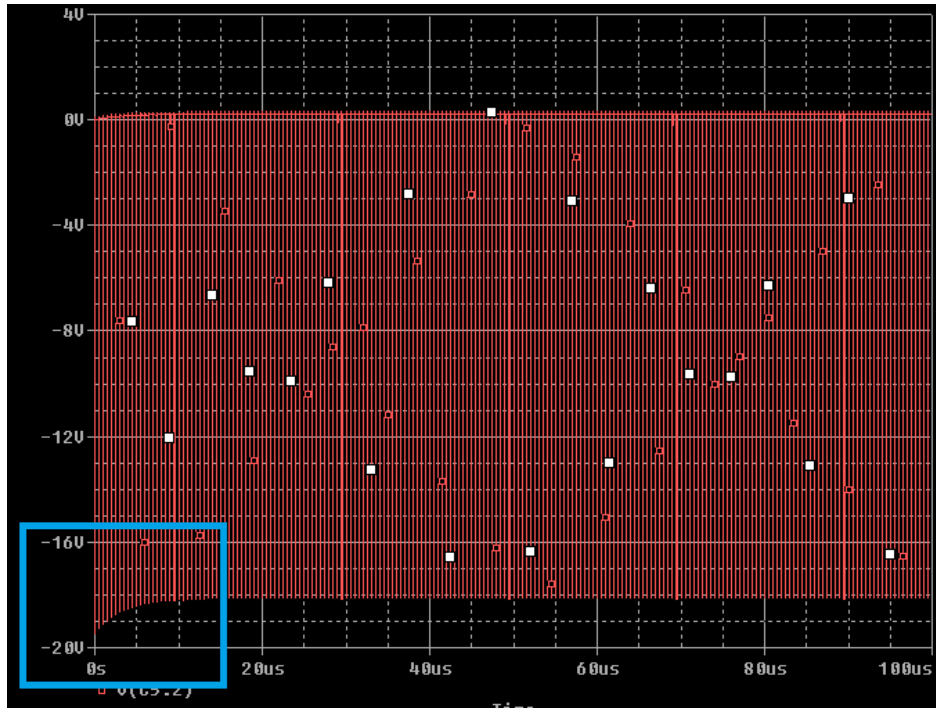


Figure 33: Drawback in the Pulse Amplitude Control Module

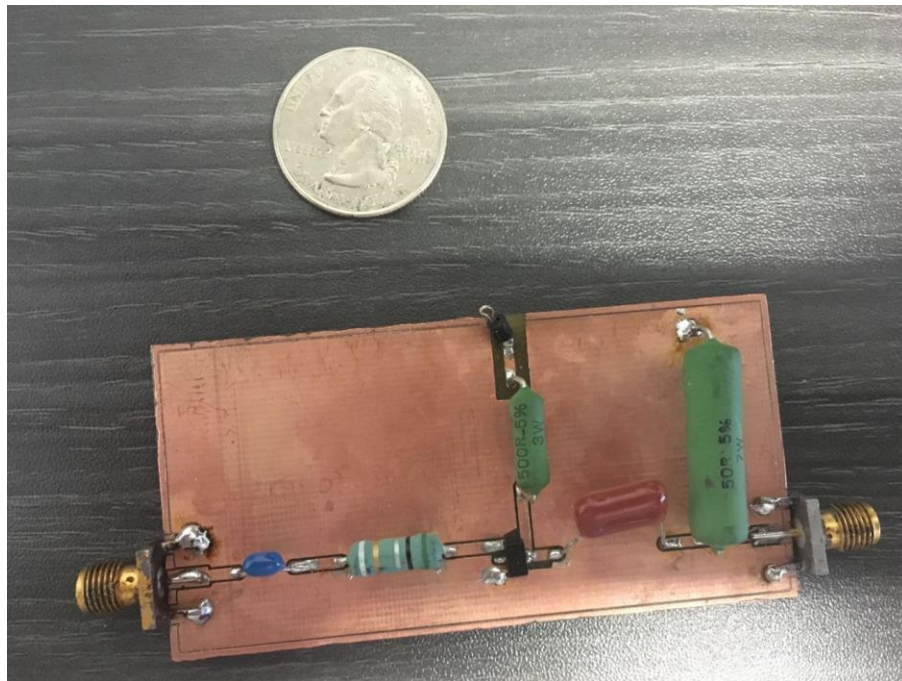


Figure 34: Circuit of Pulse Amplitude Control Module

It is described that the output capacitor C_{out} determines the pulse amplitude and fall time. According to the simulation results, C_{out} is set to 10 nF for adequate stored energy. In Figure 35, the output has a flat voltage amplitude when a large capacitor is used.

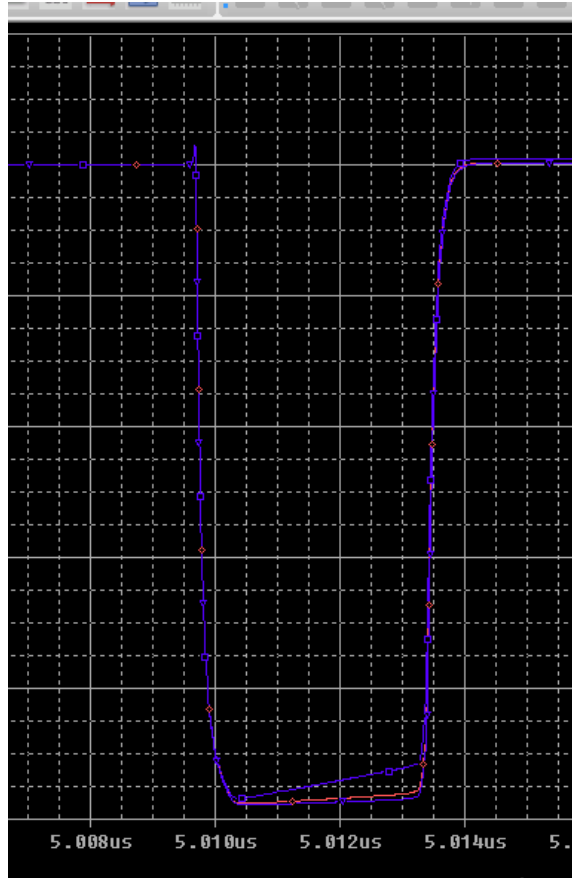


Figure 35: Output in different output capacitor

C_{in} is 47 μ F and R_b is 0.5 Ω as a filter network. We need a low input impedance in 2MHz frequency in order to have the base drive current sufficient to keep the transistor turned ON. The RC network also guarantees the input current is no more than the requirement of transistor 2SC5551A.

CHAPTER 6: SIMULATION OF PULSE AMPLITUDE CONTROL MODULE

6.1. Introduction

The module is a board level design and the results are captured by OrCAD Capture. OrCAD Capture is a widely used schematic design solution for the creation and documentation of electrical circuit. Coupled with OrCAD component information system for data management, OrCAD Capture is a powerful design environment for this module. It offers an input interface for data importing. In this simulation, the simulation data from on-chip design is applied as the input.

6.2. Simulation setting

The simulation schematic is shown in Figure 36.

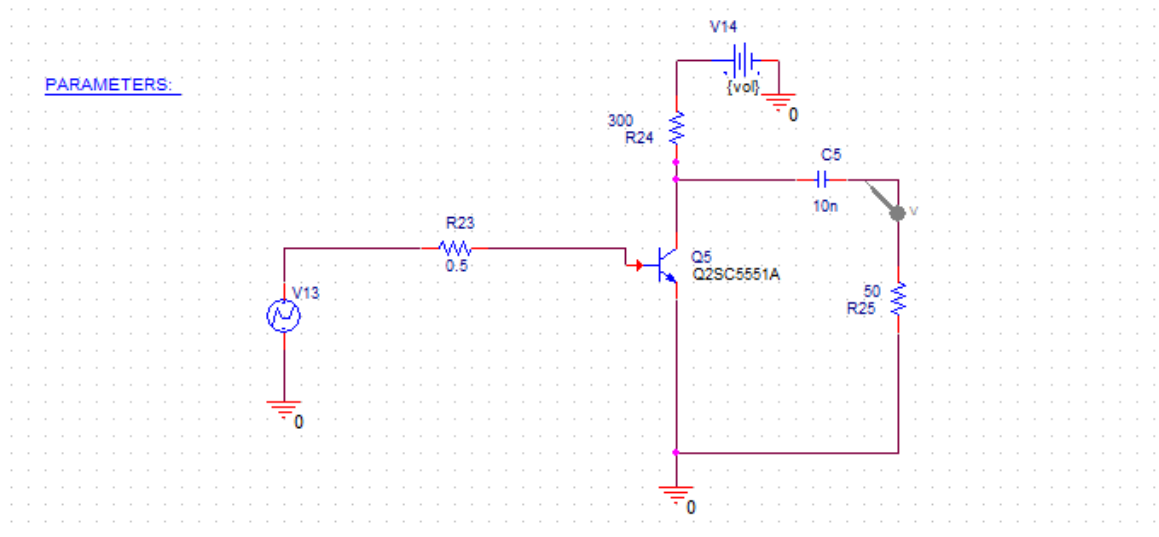


Figure 36: Simulation schematic

Based on the variable power supply in the module, simulations are using parameter sweep function in transient mode. The power supply value changes from 5 Volt to 30 Volt and the increment step is 5 Volt for result presentation. The result data are captured from $t = 5 \mu\text{s}$ to $t = 5.030\mu\text{s}$ to show a single pulse in stable condition. The settings are shown in Figure 37.

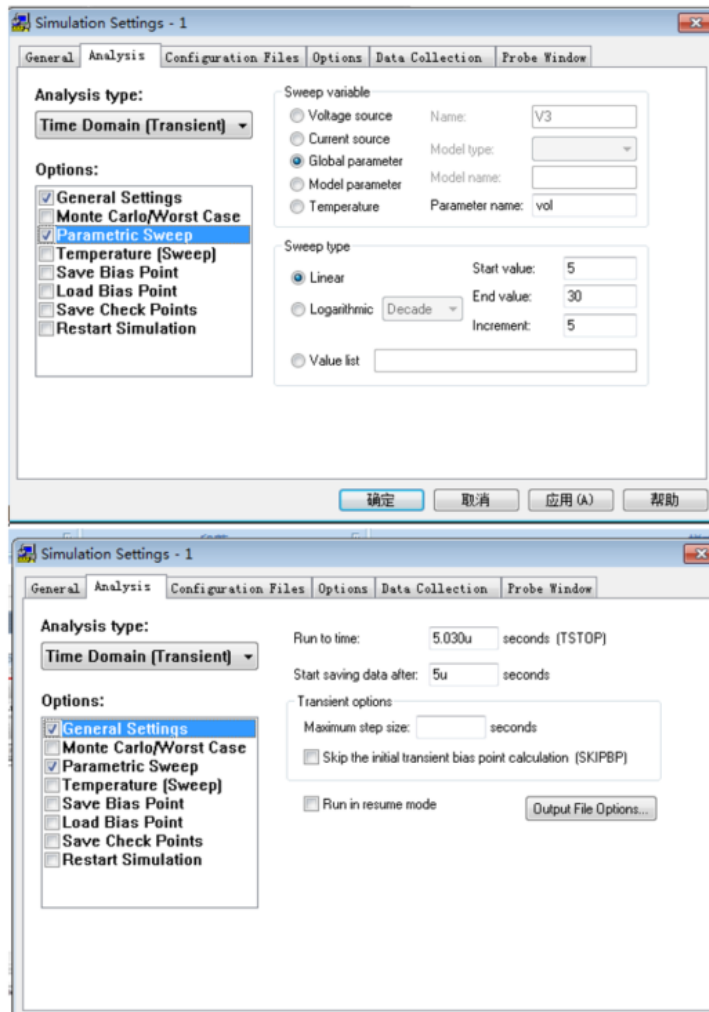


Figure 37: Simulation settings

In Figure 36, V13 is the pulse source using data exported from Cadence Virtuoso.

The interface is shown in Figure 38.

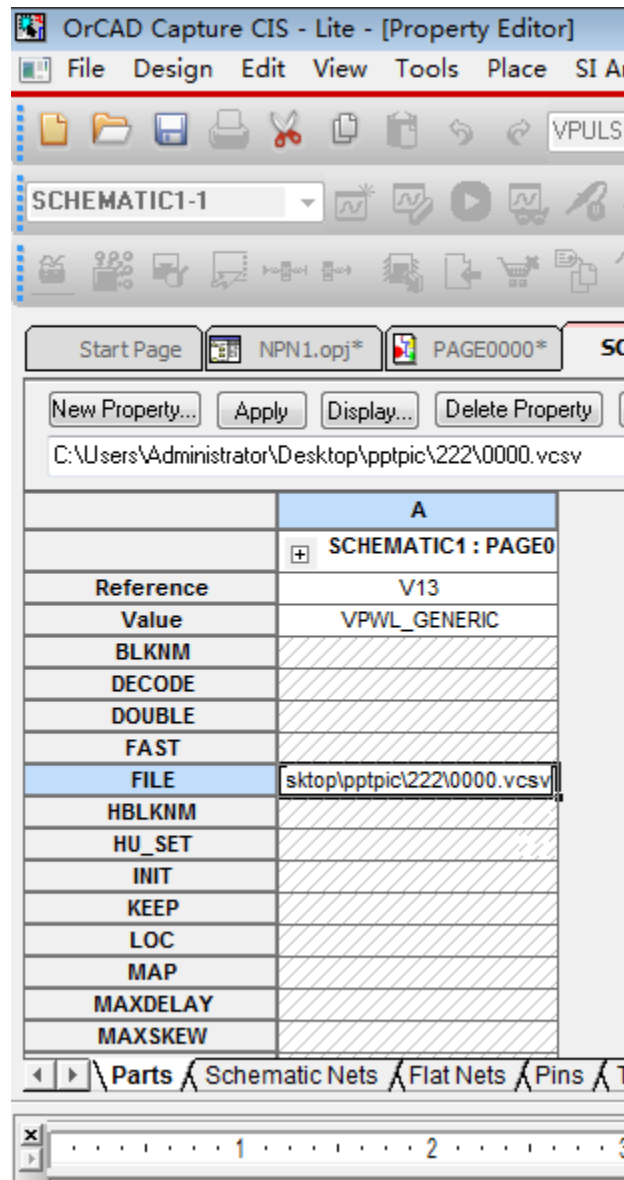


Figure 38: Data Interface in OrCAD

And, the power spectral density is an essential parameter for the Ground-penetrating Radar pulse signal. We generate the spectrum of output voltage amplitude by

using Fast Fourier Transfer function in OrCAD. Then, we compute power spectral density based on the equation

$$PSD = \sum_N^{N+10e6} \frac{2}{F_s} * V_{dft}^2 \quad (6.1)$$

where F_s is the sample frequency, N is the frequency in the unit of MHz and V_{dft} is the instantaneous voltage amplitude in the spectrum of output voltage amplitude. And, it can be represented in the unit of dBm by

$$PSD_{db} = 10 * 10 \log_{10} \frac{PSD}{0.001 W} \quad (6.2)$$

As a conclusion, we calculate the power spectral density by following steps:

First, we convert the signal from time domain to a representation in the frequency domain by Fourier transform.

Secondly, we calculate power using signal data which is represented in frequency domain.

Third, we convert the unit of power spectral density to dBm/MHz

Results are printed by MATLAB and the sampling frequency is 1.6 GHz. The code is attached in the Appendix.

6.3. Result

As we know, the Pulse Width Control Module generates 16 different outputs in terms of pulse width. As a result, 16 groups of pulses are generated in the Pulse Amplitude Control Module using 6 different power supplies. In other words, 96 different pulses are realized in the whole system and they are sorted into 16 groups labelled by binary code. The results are shown in figures and data are shown in tables.

6.3.1. Code 0000

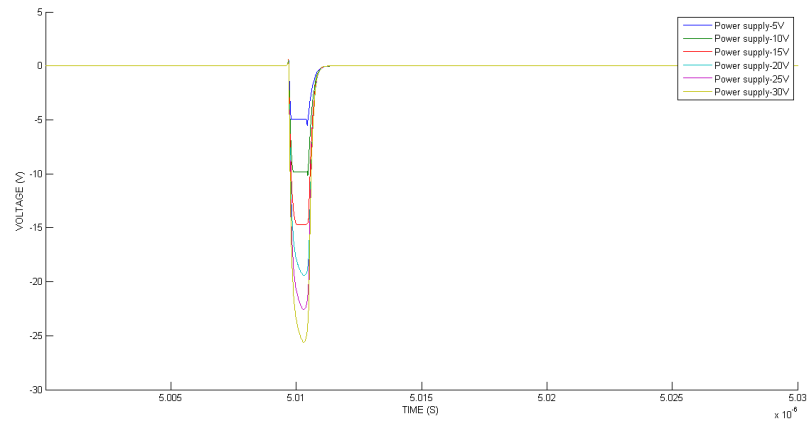


Figure 39: Outputs of Code 0000

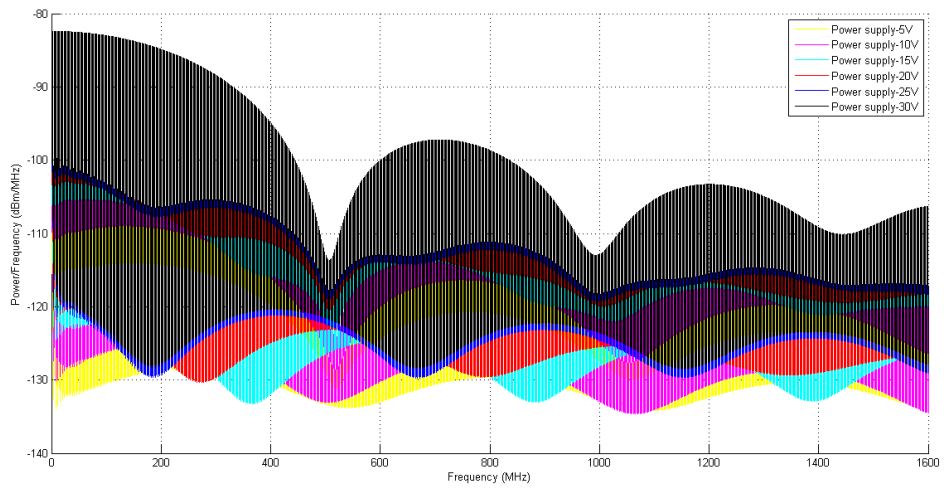


Figure 40: Power spectral density of Code 0000

Table 10: Data of Code 0000

Power supply(V)	Pulse width (ns)	Power consumption(W)	Pulse amplitude(V)
5	0.86405	0.0030	4.9378
10	0.84520	0.0117	9.8298
15	0.84033	0.0259	14.7123
20	0.82484	0.0439	19.4081
25	0.81124	0.0628	22.5716
30	0.80323	0.0846	25.5975

6.3.2. Code 0001

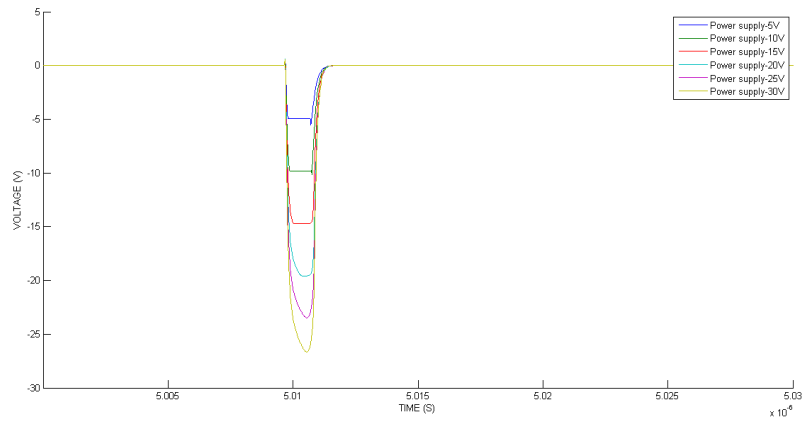


Figure 41: Outputs of Code 0001

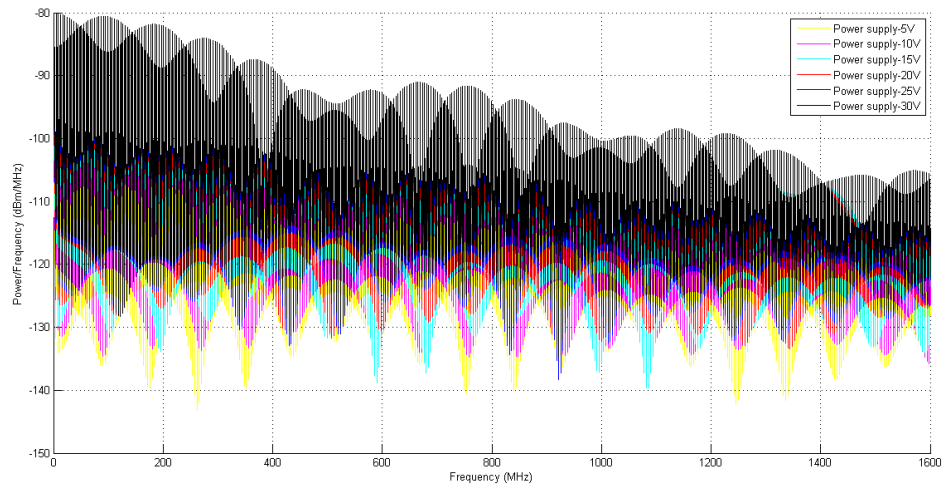


Figure 42: Power spectral density of Code 0001

Table 11: Data of Code 0001

Power supply(V)	Pulse width(ns)	Power consumption(W)	Pulse amplitude(V)
5	1.14787	0.0032	4.9379
10	1.13844	0.0125	9.8300
15	1.14755	0.0279	14.7136
20	1.14668	0.0486	19.5770
25	1.13411	0.0713	23.4772
30	1.12731	0.0966	26.6623

6.3.3. Code 0010

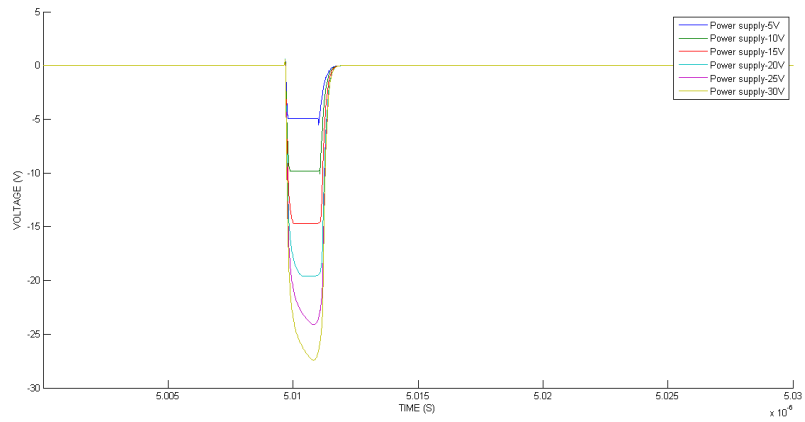


Figure 43: Outputs of Code 0010

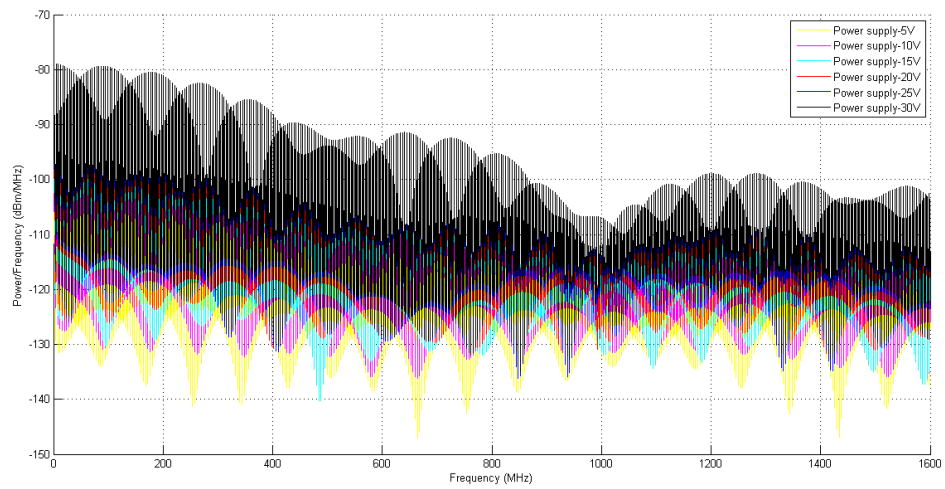


Figure 44: Power spectral density of Code 0010

Table 12: Data of Code 0010

Power supply(V)	Pulse Width(ns)	Power consumption(W)	Pulse amplitude(V)
5	1.44841	0.0032	4.9382
10	1.45236	0.0126	9.8299
15	1.47353	0.0286	14.7136
20	1.48872	0.0506	19.5852
25	1.48627	0.0758	24.1177
30	1.47988	0.0988	27.4280

6.3.4. Code 0011

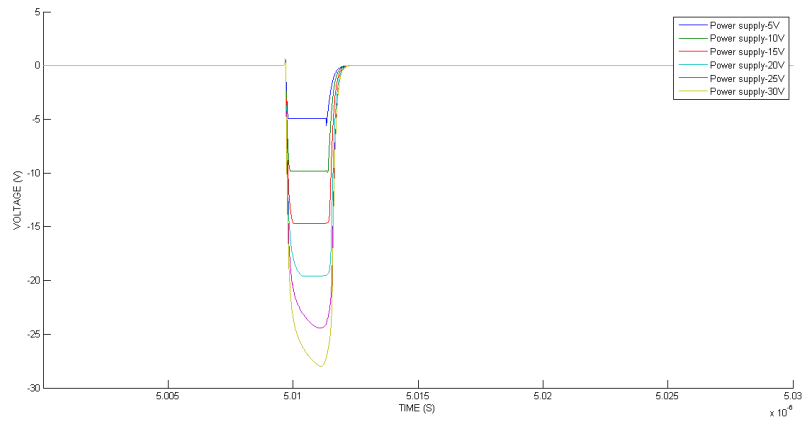


Figure 45: Outputs of Code 0011

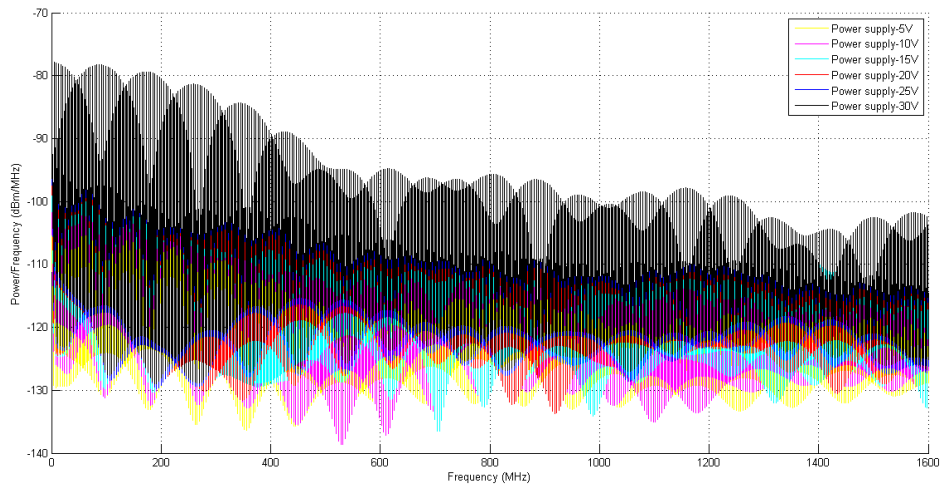


Figure 46: Power spectral density of Code 0011

Table 13: Data of Code 0011

Power supply(V)	Pulse Width(ns)	Power consumption(W)	Pulse amplitude(V)
5	1.75672	0.0037	4.9382
10	1.77394	0.0148	9.8299
15	1.80548	0.0339	14.7136
20	1.83422	0.0611	19.5854
25	1.84821	0.0944	24.4139
30	1.84323	0.1282	27.9919

6.3.5. Code 0100

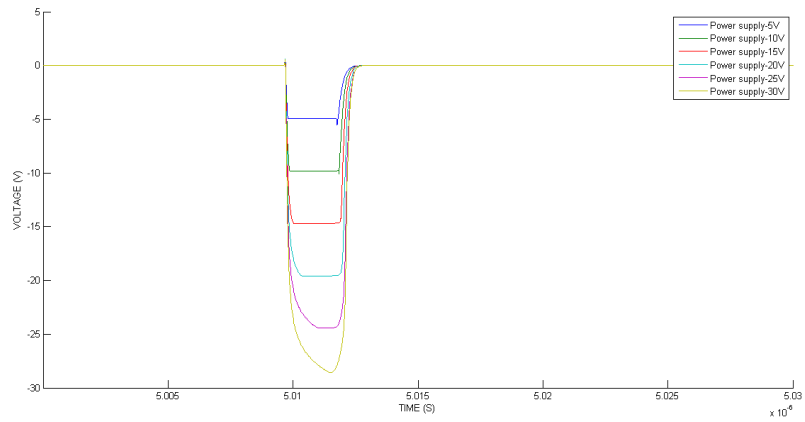


Figure 47: Outputs of Code 0100

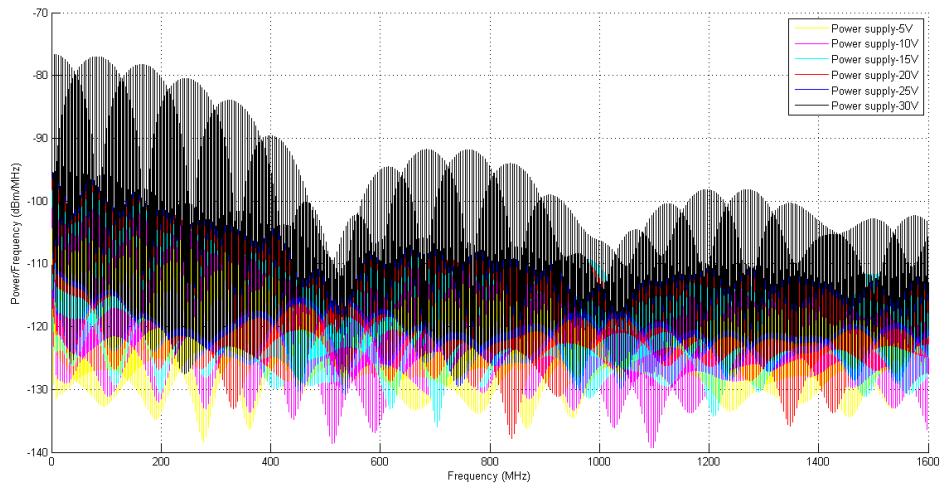


Figure 48: Power spectral density of Code 0100

Table 14: Data of Code 0100

Power supply(V)	Pulse Width(ns)	Power consumption(W)	Pulse amplitude(V)
5	2.19336	0.0049	4.9382
10	2.22270	0.0199	9.8302
15	2.27302	0.0468	14.7136
20	2.32301	0.0861	19.5854
25	2.35896	0.1344	24.4347
30	2.36341	0.1858	28.5897

6.3.6. Code 0101

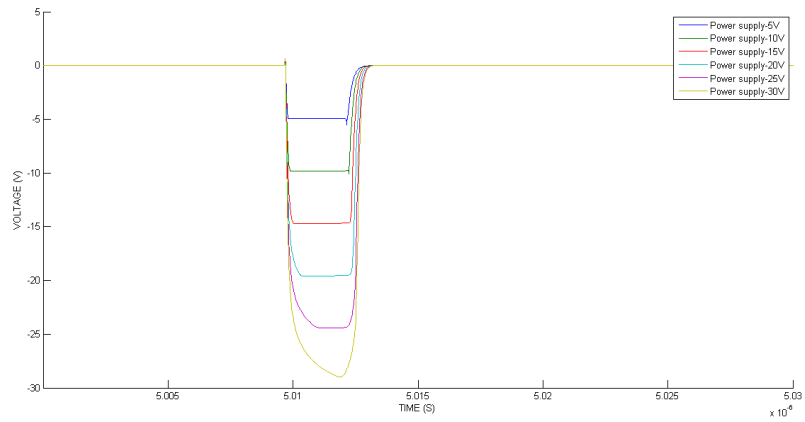


Figure 49: Outputs of Code 0101

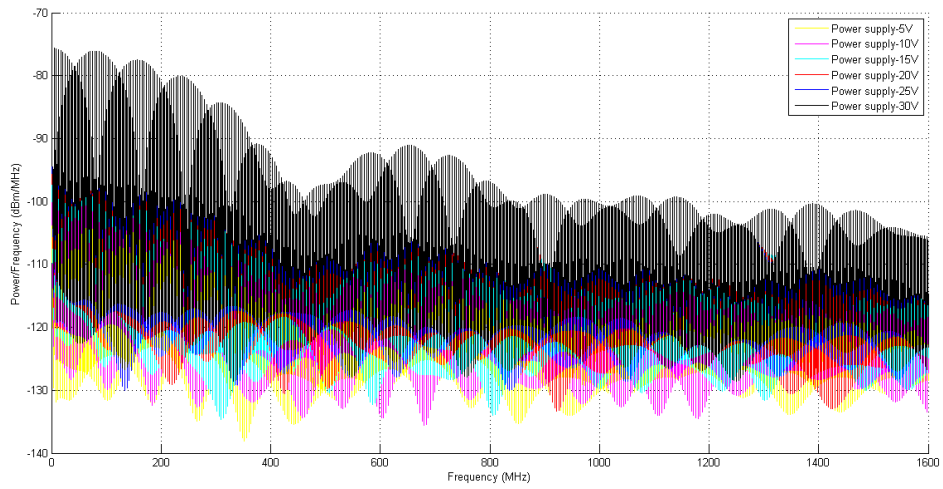


Figure 50: Power spectral density of Code 0101

Table 15: Data of Code 0101

Power supply(V)	Pulse Width(ns)	Power consumption(W)	Pulse amplitude(V)
5	2.57314	0.0060	4.9382
10	2.61214	0.0239	9.8302
15	2.67515	0.0545	14.7136
20	2.73719	0.0982	19.5854
25	2.79446	0.1540	24.4351
30	2.81611	0.2168	28.9844

6.3.7. Code 0110

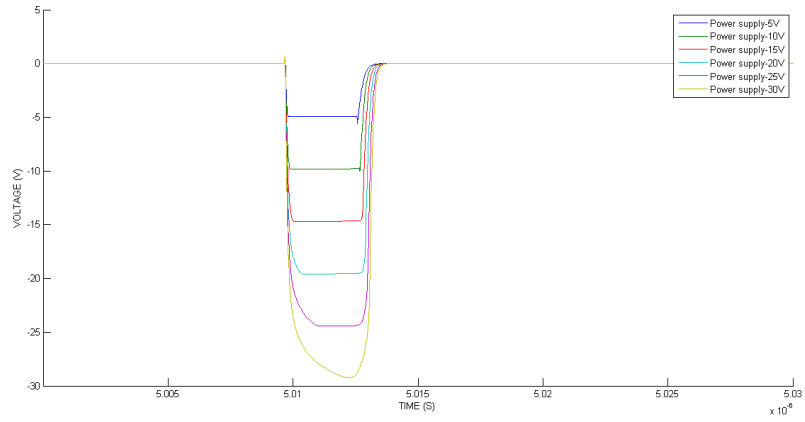


Figure 51: Outputs of Code 0110

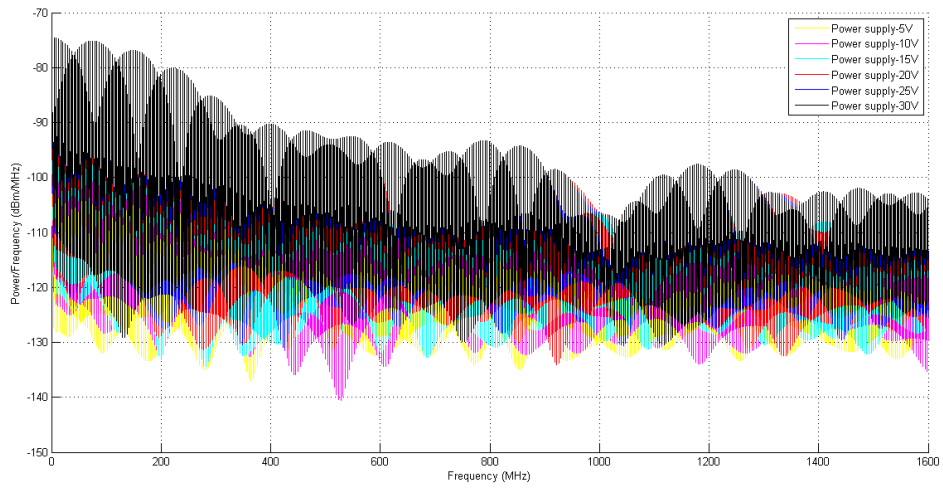


Figure 52: Power spectral density of Code 0110

Table 16: Data of Code 0110

Power supply(V)	Pulse width(ns)	Power consumption(W)	Pulse amplitude(V)
5	3.00901	0.0062	4.9382
10	3.06700	0.0249	9.8304
15	3.14130	0.0566	14.7136
20	3.22377	0.1021	19.5854
25	3.29202	0.1607	24.4351
30	3.34057	0.2292	29.2315

6.3.8. Code 0111

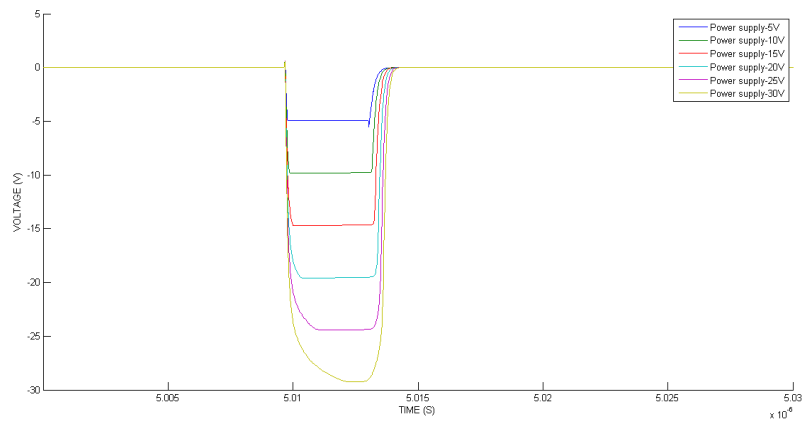


Figure 53: Outputs of Code 0111

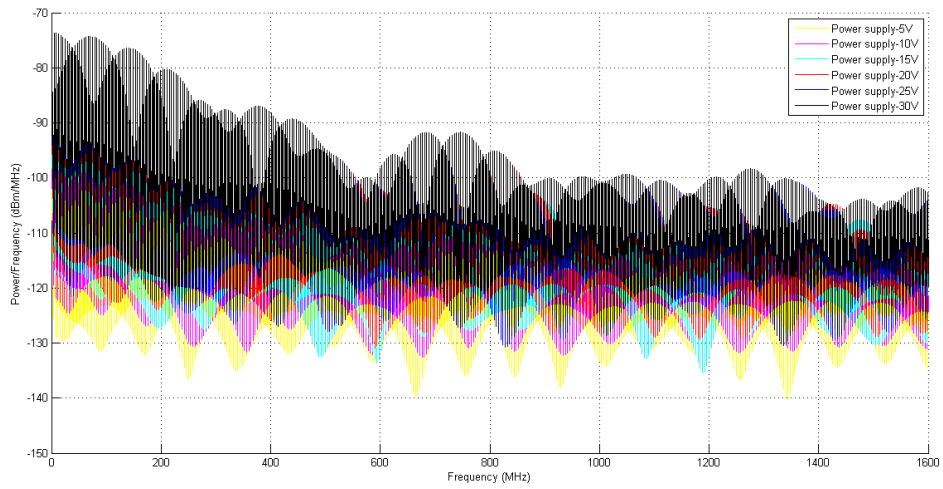


Figure 54: Power spectral density of Code 0111

Table 17: Data of Code 0111

Power supply(V)	Pulse Width(ns)	Power consumption(W)	Pulse amplitude(V)
5	3.46905	0.0065	4.9382
10	3.53950	0.0262	9.8304
15	3.62353	0.0597	14.7136
20	3.72251	0.1074	19.5854
25	3.80957	0.1684	24.4351
30	3.88386	0.2412	29.2479

6.3.9 Code 1000

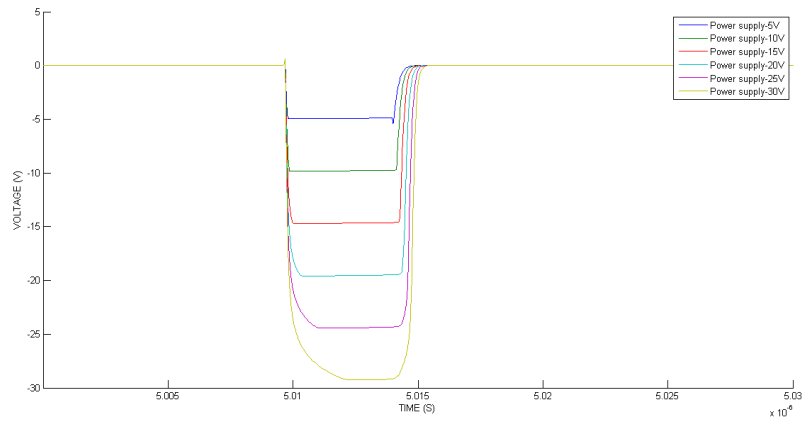


Figure 55: Outputs of Code 1000

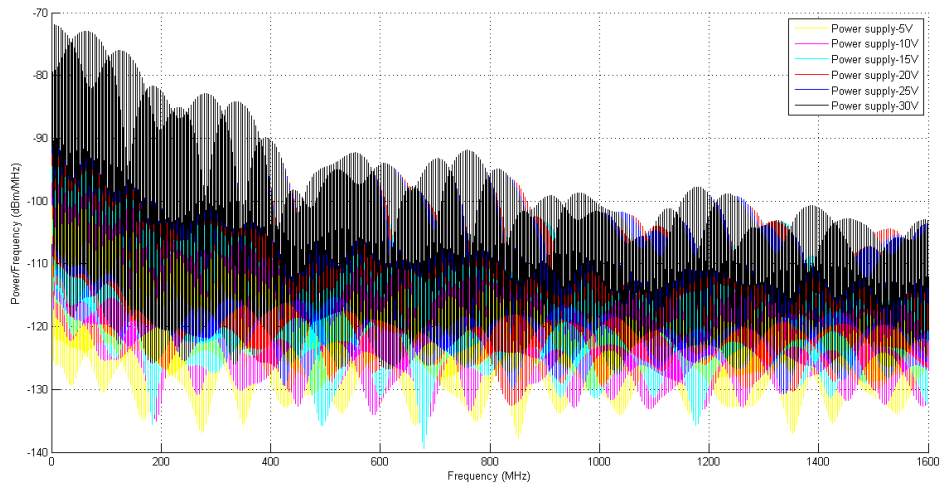


Figure 56: Power spectral density of Code 1000

Table 18: Data of Code 1000

Power supply(V)	Pulse width(ns)	Power consumption(W)	Pulse amplitude(V)
5	4.44452	0.0070	4.9382
10	4.52564	0.0282	9.8305
15	4.64236	0.0643	14.7136
20	4.77235	0.1153	19.5853
25	4.90699	0.1820	24.4351
30	5.01965	0.2616	29.2480

6.3.10. Code 1001

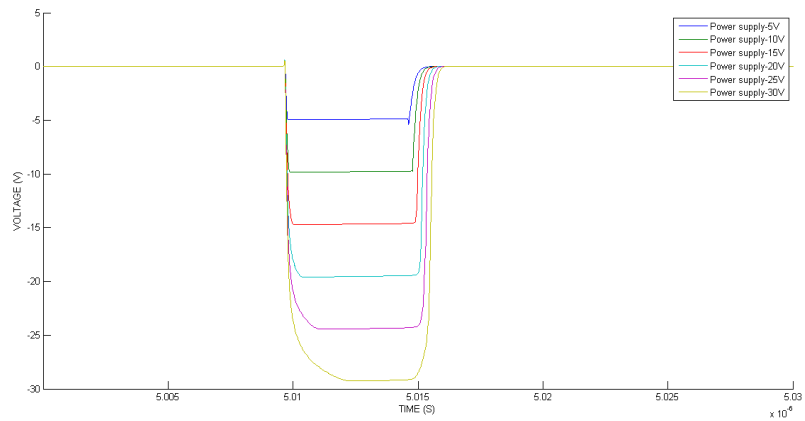


Figure 57: Outputs of Code 1001

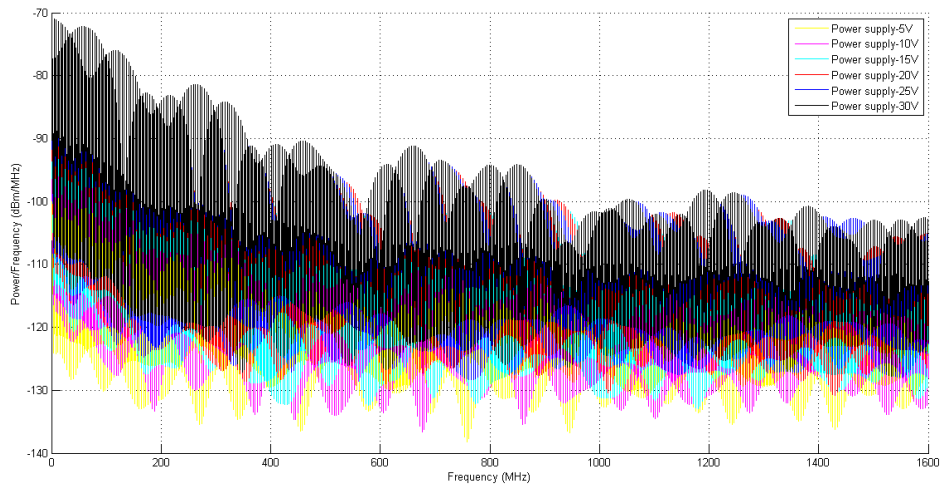


Figure 58: Power spectral density of Code 1001

Table 19: Data of Code 1001

Power supply(V)	Pulse width(ns)	Power consumption(W)	Pulse amplitude(V)
5	5.07053	0.0070	4.9382
10	5.16963	0.0283	9.8359
15	5.29772	0.0648	14.7136
20	5.44752	0.1170	19.5854
25	5.59381	0.1841	24.4351
30	5.74436	0.2660	29.2480

6.3.11. Code 1010

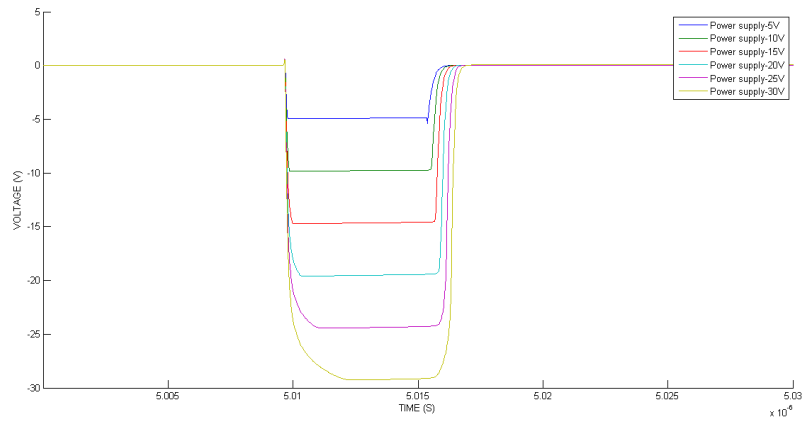


Figure 59: Outputs of Code 1010

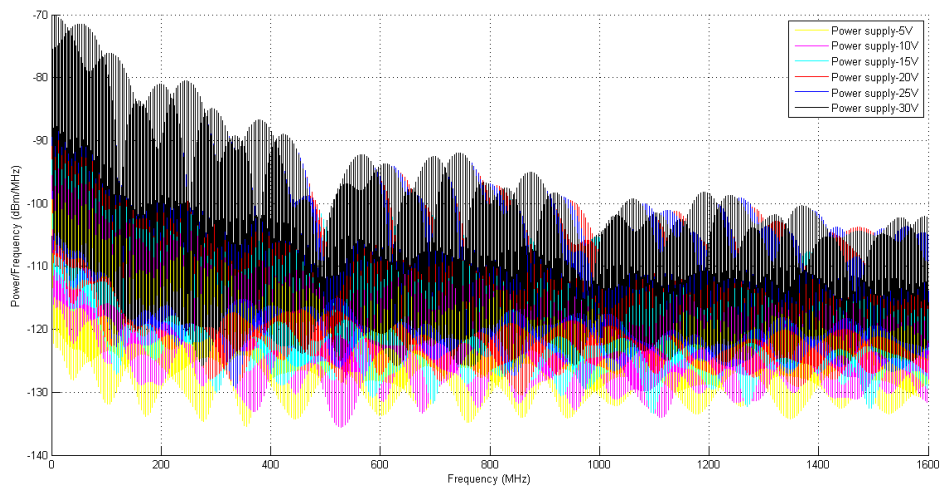


Figure 60: Power spectral density of Code 1010

Table 20: Data of Code 1010

Power supply(V)	Pulse width(ns)	Power consumption(W)	Pulse amplitude(V)
5	5.81806	0.0074	4.9382
10	5.93496	0.0300	9.8285
15	6.07732	0.0688	14.7136
20	6.24463	0.1246	19.5853
25	6.42640	0.1964	24.4351
30	6.59777	0.2847	29.2479

6.3.12. Code 1011

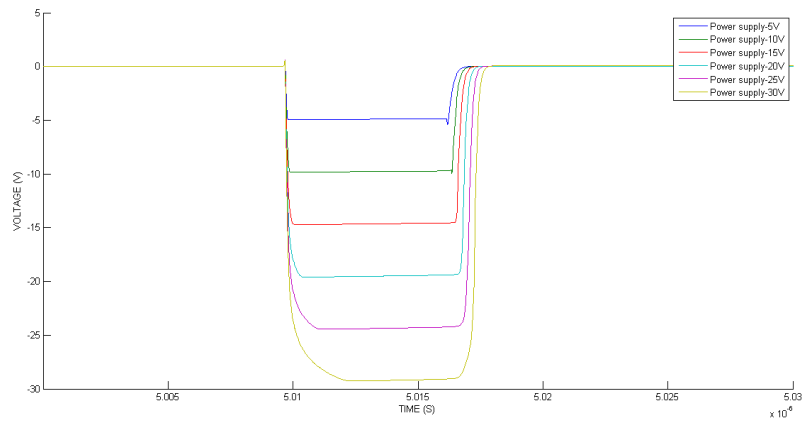


Figure 61: Outputs of Code 1011

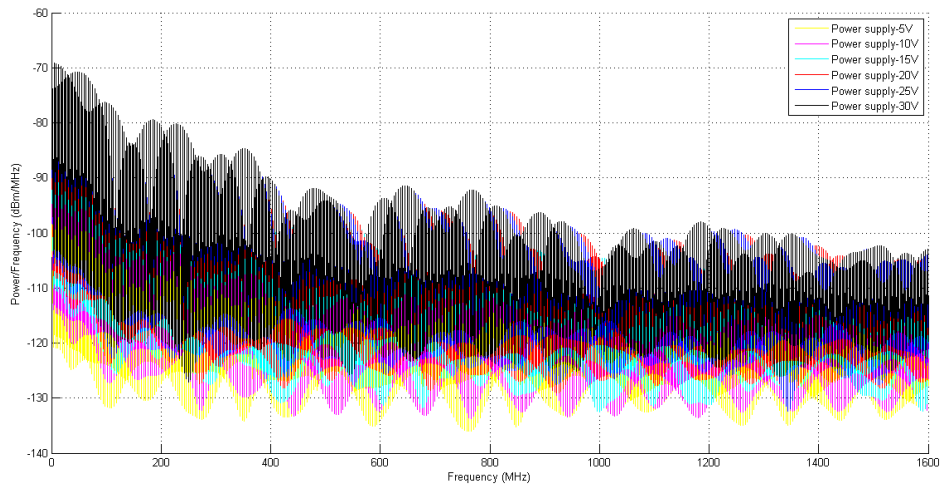


Figure 62: Power spectral density of Code 1011

Table 21: Data of Code 1011

Power supply(V)	Pulse width(ns)	Power consumption(W)	Pulse amplitude(V)
5	6.63437	0.0078	4.9382
10	6.75608	0.0316	9.8301
15	6.91613	0.0725	14.7138
20	7.10448	0.1307	19.5853
25	7.30196	0.2070	24.4351
30	7.51416	0.3010	29.2480

6.3.13. Code 1100

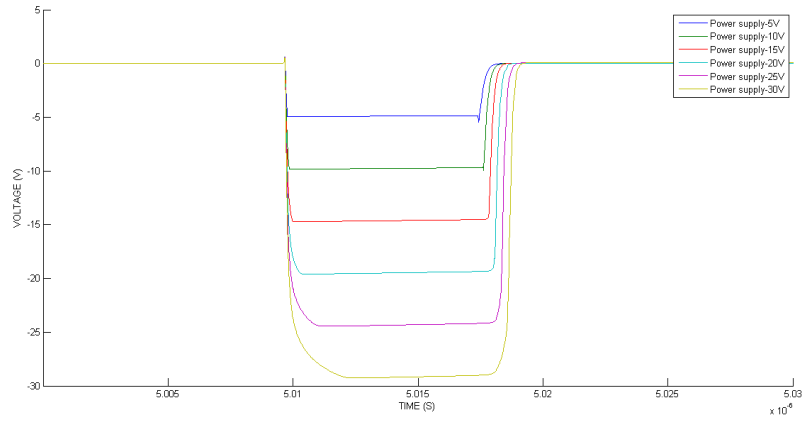


Figure 63: Outputs of Code 1100

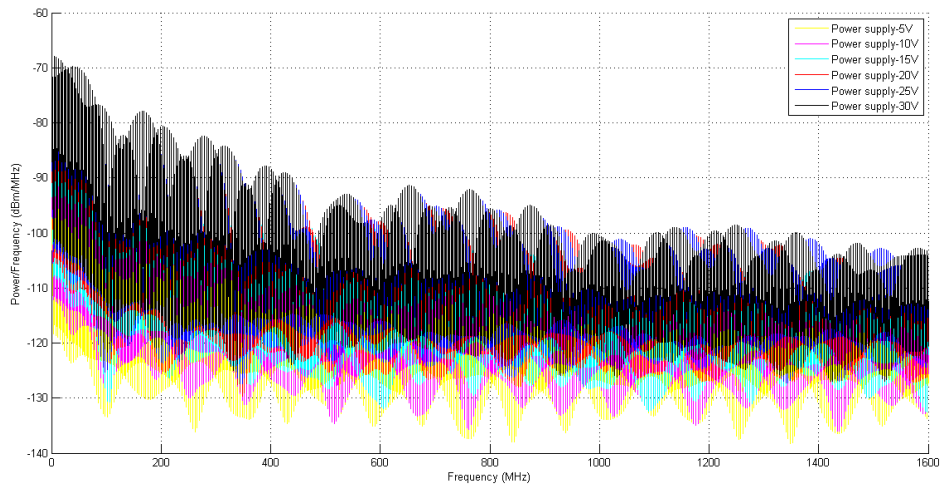


Figure 64: Power spectral density of Code 1100

Table 22: Data of Code 1100

Power supply(V)	Pulse width(ns)	Power consumption(W)	Pulse amplitude(V)
5	7.87744	0.0079	4.9382
10	8.02001	0.0324	9.8301
15	8.20694	0.0764	14.7137
20	8.42474	0.1463	19.5854
25	8.66102	0.2392	24.4310
30	8.90986	0.3486	29.2479

6.3.14. Code 1101

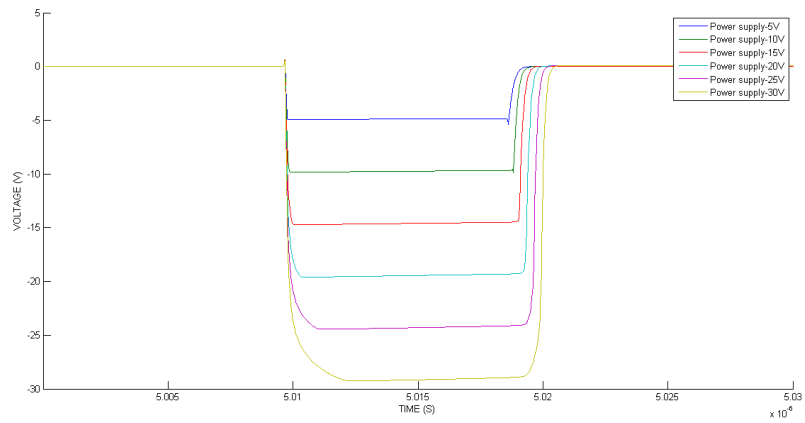


Figure 65: Output of Code 1101

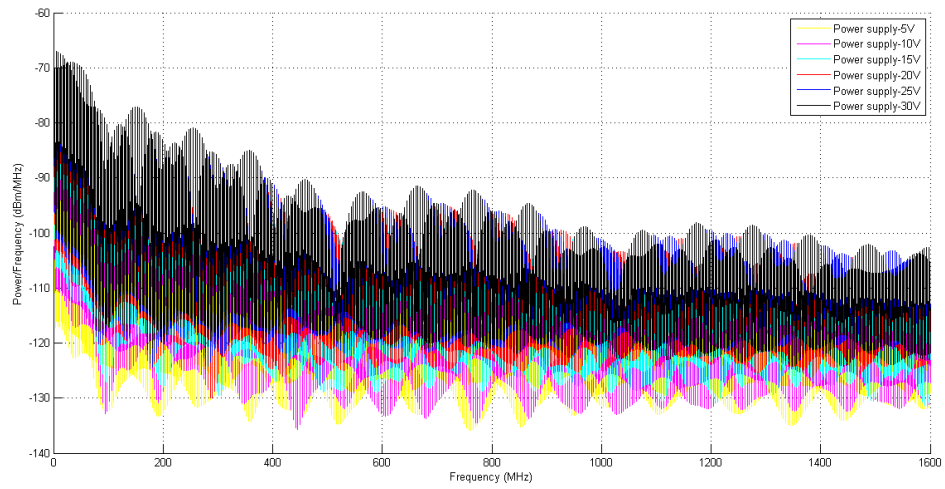


Figure 66: Power spectral density of Code 1101

Table 23: Data of Code 1101

Power supply(V)	Pulse width(ns)	Power consumption(W)	Pulse amplitude(V)
5	9.04935	0.0099	4.9382
10	9.20792	0.0402	9.8302
15	9.41407	0.0927	14.7137
20	9.65496	0.1671	19.5854
25	9.92699	0.2649	24.4351
30	10.20260	0.3873	29.2479

6.3.15. Code 1110

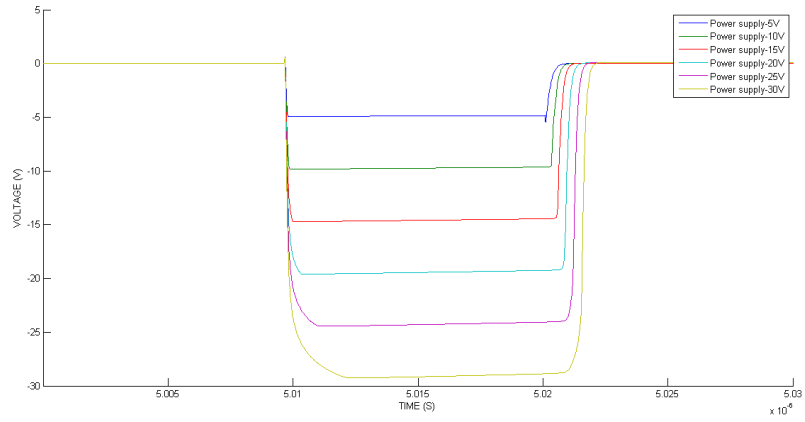


Figure 67: Outputs of Code 1110

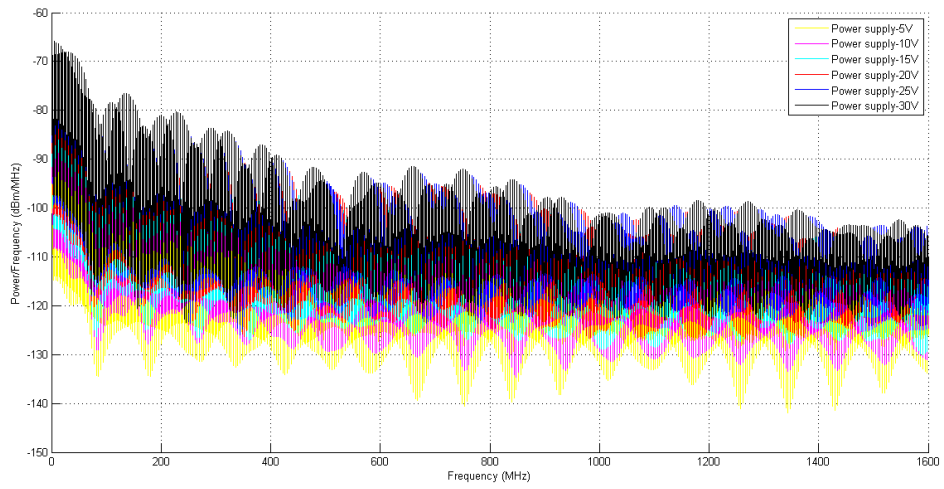


Figure 68: Power spectral density of Code 1110

Table 24: Data of Code 1110

Power supply(V)	Pulse width(ns)	Power consumption(W)	Pulse amplitude(V)
5	10.54580	0.0104	4.9382
10	10.71831	0.0422	9.8301
15	10.94079	0.0972	14.7137
20	11.21187	0.1770	19.5854
25	11.57242	0.2858	24.4351
30	11.83214	0.4389	29.2480

6.3.16. Code 1111

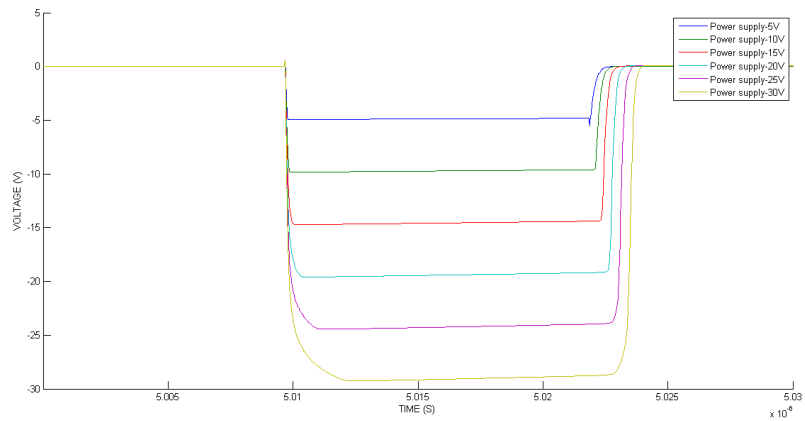


Figure 69: Outputs of Code 1111

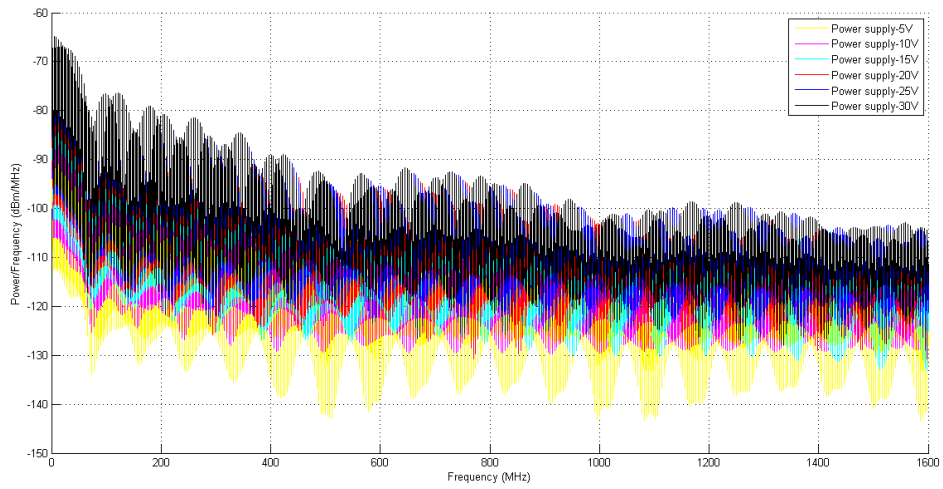


Figure 70: Power spectral density of Code 1111

Table 25: Data of Code 1111

Power supply(V)	Pulse width(ns)	Power consumption(W)	Pulse amplitude(V)
5	12.29683	0.0124	4.9382
10	12.48648	0.0501	9.8302
15	12.72990	0.1145	14.7136
20	13.02972	0.2067	19.5853
25	13.36089	0.3268	24.5451
30	13.72554	0.4739	29.2480

6.4 Result reviews

In tables, the total power of the circuit and power spectral density are presented. The presented data are obtained by calculation in MATLAB.

The power consumption is calculated using the voltage of the power supply and the current passing through the power supply. The instantaneous current data is obtained through simulation in OrCAD CAPTURE. The power consumption is calculated based on the equation

$$P = \frac{1}{T} \int_n^{n+T} I(t) * V_{dc} dt \quad (6.3)$$

In figures, the module generates pulse with flat amplitude in most cases and the pulse amplitude is dependent on the choice of power supply. According to all results, we can conclude that pulse amplitude in most cases reaches voltage level of power supply. Some special cases show that pulse amplitude is less than power supply obviously. Owing to limited pulse width of trigger signal in code 0000, the transistor is switched to OFF-state while capacitor is not fully discharged.

Based on data of each code shown in tables, the module generates pulses with extra pulse width. The extra value varies in different situation but it relatively small. The maximum is addressed in Code 1111 which is about 1.5 ns. In this condition, the pulse width of output in 30V as power supply is 12% more than that in 5V as power supply.

CHAPTER 7: CONCLUSION

This thesis sets out to design an adaptive high voltage pulse generator for ground-penetrating radar system. Ground-penetrating radar system is widely used in complicated environment such as construction field, undeveloped area or mining area. Pulse generator with general purpose is highly required in these situations. In accomplishing this mission, this work seeks to build a general pulse generator which generates tunable pulse in width and amplitude. We also presented unabridged calculation for optimization of result in the thesis.

7.1. Contributions

The thesis presents a general pulse generator combining system-on-chip technology with board level design to realize pulse with tunable amplitude and pulse width. It consists of two major modules, Pulse Width Control Module and Pulse Amplitude Control Module, for functions realization. Each module is designed based on electrical characteristics of components and optimization calculation with electrical principle. Also, output data of the Pulse Amplitude Control module are presented based on simulation using raw data from the Pulse Width Control Module in order to realize consistency and reality in the design.

According to the results presented, objectives we proposed is realized theoretically. The pulse generator is able to realize variable pulse ranging from 0.80323 ns to 13.72554 ns in pulse width and 4.9 Volt to 29.2 Volt in amplitude. Meanwhile, two parameters of output pulse are controlled independently by a simple 4-bits console. This is

unique from many designs which do not concentrate on simplicity in operation and independence in modulation.

7.2. Limitations

The design remains several limitations.

First, experimental validation is needed. Although the design realized objectives theoretically, experimental testing is still needed. The simulation cannot reveal all problems in real-world design.

Secondly, switching speed of transistors is limited. In ideal, transistor can be switched instantaneously. In that case, the Pulse Amplitude Control Module introduces little noise in pulse width of output which is hardly possible in real world. However, it is not a significant problem since the noise is relatively small in most cases.

7.3. Future Research

Although multiple types are presented in former works, the pulse generator still has the great potential for future development.

First, in section 7.2 Limitations, it is indicated that switching speed of transistor limits pulse width consistency in a tunable pulse amplitude design. The CMOS integrated design is an area of current research. The advanced CMOS technology has an adequate capability for fast speed design and high voltage design.

Secondly, in the tunable pulse generator design, linearity is an important capability which is not concerned in most research. This is a complicated problem in most

proposed designs because the output is generated depends on several transistors in a pulse generator. In other words, numerous parameters are necessary to be considered in optimization calculation which can be seen in Chapter 3. Therefore, a novel architecture for linear pulse width realization is needed.

References

- 1, Jeongwoo Han and Cam Nguyen. "Ultra-Wideband Electronically Tunable Pulse Generator." IEEE Microwave and Wireless Components Letter, vol. 14. No. 3, Mar. 2004.
- 2, Jeongwoo Han and Cam Nguyen. "Microstrip Impulse Generators with Tunable Pulse Duration for Ultra-Wideband Applications." 2003 Asia Pacific Microwave Conference, Seoul, Korea, Nov. 2003.
- 3, Erick Maxwell, Thomas Weller and Jeffery Harrow. "A Tunable Ultra-Wideband Pulse Generator Using a Variable Edge-Rate Signal." Circuits and Systems, 2006 IEEE Asia Pacific Conference on, Dec. 2006.
- 4, Meng Miao and Cam Nguyen. "On the Development of an Integrated CMOS-Based UWB Tunable-Pulse Transmit Module." IEEE Transactions and Microwave Theory and Techniques, vol. 54, no. 10, Oct. 2006.
- 5, Sarika Tyagi, et al. "Revisiting Performance of Various Delay Elements to Realize a Trigger Pulse Generator." Smart Sensors and Systems(IC-SSS), International Conference on, Dec. 2015.
- 6, Jian Sen The, et al. "Review of Pulse Generator for Gated Ring Oscillator Based Time-to-Digital Converters." Integrated Circuits(ISIC), 2016 International Symposium on, Dec. 2016.
- 7, Jun Zhou, et al. "An Ultra-Low Voltage Level Shifter Using Revised Wilson Current Mirror for Fast and Energy-Efficient Wide-Range Voltage Conversion from Sub-Threshold to I/O Voltage." IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 62, no. 3, Mar. 2015.
- 8, Shien-Chun Luo, Ching-Ji Huang and Yuan-Hua Chu. "A Wide-Range Level Shifter Using a Modified Wilson Current Mirror Hybrid Buffer." IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 61, no. 6, Jun. 2014.
- 9, Sven Lutkemeier and Ulrich Ruckert. "A Subthreshold to Above-Threshold Level Shifter Comprising a Wilson Current Mirror." IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 57, no. 9, Sep. 2010.
- 10, V. P. Dyakonov. "Avalanche transistors and their application in impulse generating circuits." Sovetskoe Radio, 1993.
- 11, J. Millman and H. Taub. "Pulse, Digital, and Switching Waveforms." New York, McGraw-Hill, 1965.

- 12, J. R. Andrews. "Picosecond Pulse Generation Techniques and Pulser Capabilities." Application Note AN-19,2008.
- 13, Ai-min. Zou, Hui-bo Wang, Yan-zhang Wang and De-fu. Cheng. "Nanosecond Pulser Based on Serial Connection of Avalanche Transistors." Measuring Technology and Mechatronics Automation (ICMTMA), 2010 international Conference on, Mar. 2010.
- 14, Jiangtao Li, et al. "Theoretical Analysis and Experimental Study on an Avalanche Transistor-Based Marx Generator." IEEE Transactions on Plasma Science, vol. 43, no. 10, Oct. 2015.
- 15, Weidong Ding, et al. "A Subnanosecond Jitter Trigger Generator Utilizing Trigatron Switch and Avalanche Transistor Circuit." IEEE Transactions on Plasma Science, vol. 43, no. 4, Apr. 2015.
- 16, IEEE. "IEEE Standard for Transitions, Pulses, and Related Waveforms." Sep. 2011.
- 17, H. Pekau, A. Yousif and J. W. Haslett. "A CMOS integrated linear voltage-to-pulse-delay-time converter for time based analog-to-digital converters." Circuits and Systems, 2006 IEEE International Symposium on, May. 2006.
- 18, Ali H. Hassan, et al. "An ultra-low power voltage-to-time converter(VTC) circuit for low power and low speed applications." System-on-Chip Conference(SOCC), 2016 29th IEEE International, Sep. 2016
- 19, John P. Uyemura. "Introduction to VLSI Circuits and Systems." Wiley, 1st edition, July 30, 2001.
- 20, Przemyslaw Mroszczyk and Piotr Dudek. "Tunable CMOS Delay Gate with Improved Matching Properties." IEEE Transactions on Circuits and Systems I:
- 21, IBM. "Design Kit and Technology Training, CMHV7SF, V1100" IBM Foundry and Manufacturing Service Education, Revision 2.0., Jun. 2011.
- 22, IBM. "CMHV7SF Design Manual." May. 2014.
- 23, ON Semiconductor. "2SC5551A datasheet." Aug. 2013.

Appendix

PSD calculation code

```
clear all;

% filepath_source

filepath_source = ['C:\Users\Administrator\Documents\MATLAB\formatlab\file\tst\'];

%load data from 1 to 16

code_num = 16;

load_data = xlsread([filepath_source num2str(code_num) '.xlsx']);

% length

N = 8000;

%sample frequency

Fs = 1.6*10e9;

%matrix initial

array_psd = zeros(N,6);

array_psdmhz = zeros(1600,6);

% calculations for 5V to 30V data

for count = 1:6

    %amplitude fft data point

    xdft = load_data(1: N,count+1);

    %power calculation

    psdx = (1/(Fs)). * abs(xdft) . ^ 2;

    array_psd( : , count) = psdx * 2;
```

```

%integral of all points within 1 MHz
for i = 1 : 1600
    array_psdmhz( i ,count) = sum(array_psd((5*(i-1)+1):1:5 * i, count));
end
end
%print out figure
hold on
% Fs = 1.6GHz & repetition frequency is 1MHz
freq = 1:1:1600;
plot(freq,10*log10(array_psdmhz( : ,1)/0.001),'y');
plot(freq,10*log10(array_psdmhz( : ,2)/0.001),'m');
plot(freq,10*log10(array_psdmhz( : ,3)/0.001),'c');
plot(freq,10*log10(array_psdmhz( : ,4)/0.001),'r');
plot(freq,10*log10(array_psdmhz( : ,5)/0.001),'b');
plot(freq,10*log10(array_psdmhz( : ,6)/0.001),'k');
grid on;
xlabel('Frequency (MHz)');
ylabel('Power/Frequency (dBm/MHz)')
legend('Power supply-5V','Power supply-10V','Power supply-15V','Power supply-
20V','Power supply-25V','Power supply-30V')
hold off;

```