Has Silicon Reached Its Limit?

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Abstract. *In light of the rapidly increasing demand for ultra-high speed data transmission, data centres are under pressure to provide ever increasing data transmission through their networks and at the same time improve the quality of data handling in terms of reduced latency, increased scalability and improved channel speed for users. However as data rates increase, present electronic switching technology using current data centre architecture is becoming increasingly difficult to scale despite improvements in data management. In this paper the tremendous bandwidth potential of optical fibre based networks will be explored alongside the issues of electronic scalability and switching speed. A resulting need for alternative optical solutions for all-optical signal processing systems will be discussed. With this in mind, progress in the form of a novel and highly scalable optical interconnect will be reviewed.*

Keywords

Data centre network, electronic bottleneck, OCDMA, optical interconnect, optical switching, scalability.

1. Introduction

The volume of data passing through communication networks is rising at a phenomenal rate. Global data centre IP traffic is forecast to reach 7.7 Zetabytes per year by 2017 - 69 % of which will be cloud traffic, from its present level of 2.6 Zetabytes per year. This is a compound annual growth rate of 25 % [1]. To maintain this rapidly increasing demand, data centres must scale to provide higher bandwidths while maintaining low latency and improved scalability. This expansion is attributable to the rise of smart phones/tablets, e-services and the emergence of the cloud. Smart phones alone generate between 10 and 20 times more data traffic than conventional mobile phones [2]. These current trends have resulted in electronic bottlenecks in data networks. New developments in cloud computing will compound this problem even more.

The growing demand for high speed, low latency data transmission has generated a need for substantially increased capacity and improved connectivity within data centres. However current data centres performing all data processing based on electronic switching are incapable of sustaining these demands into the future [3] and therefore new technological solutions are required. It has been suggested that the fundamental limits of data centre switching which relies on bandwidth limited CMOS electronics is now perhaps being reached [4]. It is believed that all-optical systems using photonic integrated circuits and highly scalable optical interconnects may provide an answer with the promise of data rates exceeding Terabits per second.

2. Optical Networking

Invented in the early 1960s by Charles K. Kao, optical fibre has ushered in a new paradigm in data transmission and since then, optical fibre has become ubiquitous for long haul communications with present transmission rates exceeding 1 Tb·s^{-1} over long distances on a single fibre. The motivation for the use of optical fibre is based on the severely limited bandwidth and high attenuation in copper based links which require regular repeaters. For example, twisted wire pair cable is capable of a maximum bandwidth of around 100 MHz while coaxial cable has a maximum bandwidth of around 1 GHz. Optical fibre on the other hand has a bandwidth far in excess of this. In addition, attenuation in optical fibre is much lower than copper cables, requiring fewer repeaters.

The very high bandwidth of optical fibre cable and the rapid increase in demand for data transmission bandwidth have resulted in fibre optics technology be-

coming a major building block in data networks. In fact optical fibre has become one of the fastest growing transmission media for new data network installations and upgrades [5]. In addition to high bandwidth, optical fibre has several significant advantages over traditional copper cabling including:

- Low attenuation allowing much longer distances between repeaters.
- Improved data security.
- Immunity to electromagnetic interference, crosstalk and corrosion.
- More durable, compact and lighter in weight.
- Lower overall cost in the long term.

To take full advantage of the low attenuation of around 0.15 dB·km^{-1} to 0.2 dB·km^{-1} in the 3rd window C-band frequency range (1525 nm–1565 nm) and the development of the Erbium Doped Fibre Amplifier (EDFA), Dense Wavelength Division Multiplexing (DWDM) was developed. Today, modern transmission systems can easily transmit 160 wavelength data channels at 10 Gb·s^{-1} each over a single fibre, creating aggregate throughput of 1.6 Tb·s^{-1}. Despite the low attenuation and without the availability of optical amplifiers, signal regeneration was required particularly in long haul fiber optic systems. Around 1990, the EDFA became available allowing optical signal amplification without the need for Optical/Electronic/Optical (O/E/O) transceivers. By a happy coincidence the EDFA wavelength range matches the minimum attenuation of fibre at the 3rd window, and it can therefore be used across the entire C-band occupied by DWDM systems. To further increase the capacity of DWDM systems, research efforts have been made to increase the amplification bandwidth by either shifting the gain spectrum of conventional EDFAs to longer wavelengths, developing new dopants and glasses to provide amplification at other wavelength bands or by using Raman Amplifiers [6].

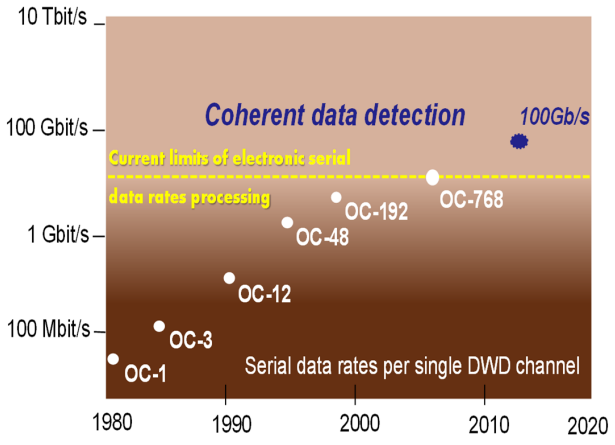


Fig. 1: Serial data rate growth per a single optical wavelength channel.

In today's networks the use of state of the art optical technologies has vastly improved single wavelength channel data rates. Figure 1 illustrates the growth of serial data rates per a single optical wavelength channel from 1980 until today. OC-n refers to the serial data capacity $n \cdot 51.84$ Mb·s^{-1} of each optical carrier in a DWDM configuration. For example OC-768 corresponds to a serial data rate of about 40 Gb·s^{-1}.

It is worth noting that these serial data rates are predominantly governed and limited by the bandwidth limited electronics available at fibre ends used for the data processing.

As an example of the current state of the art, DWDM systems are commercially available which use OC-768 across 80 channels with a 50 GHz ITU grid. The bandwidth used is therefore 4 THz and the total bit rate achieved is $80 \cdot 768 \cdot 51.48$ Mb·s^{-1} or approximately 3.2 Tb·s^{-1}.

The following analysis illustrates the theoretically immense capacity of optical fibre. The theoretical maximum capacity at the maximum sampling rate (or symbol rate) of a band-limited noise free channel is given by the well- known Nyquist theorem:

$$C = 2B \log_2 (2^n), \tag{1}$$

where C is the channel capacity in bits per second [b·s^{-1}]; B is the bandwidth (in this case of the fibre) in Hertz [Hz]; and n is the number of bits used to describe each symbol. This theorem states that the maximum symbol transmission rate is twice the bandwidth of the channel to avoid inter-symbol interference (ISI) with neighbouring samples. Apparently the channel can carry an infinite amount of information by simply increasing n, however, a noise free channel is unattainable. In the presence of noise the theoretical maximum capacity is given by a well known Shannon-Hartley theorem:

$$C = B \log_2 (1 + \mathrm{SNR}), \tag{2}$$

where C is the channel capacity in bits per second [b·s^{-1}]; B is the bandwidth of the fibre in Hertz [Hz]; and SNR is the signal to noise ratio of the channel measured as the ratio of the average received signal power to channel quantum shot noise at the receiver. The SNR is given by:

$$\mathrm{SNR} = \sqrt{\frac{\mathfrak{P}}{Bh\gamma_0}}, \tag{3}$$

where $\mathfrak{P}$ is the power guided by the fibre in Watts [W]; B is the bandwidth as before, h is Planck's constant; and γ_0 is the centre frequency of the fibre bandwidth in Hz.

The potential bandwidth of fibre is assumed to be of the order of 50 THz. The use of this figure assumes a sharp roll-off limited by attenuation in the fibre medium increasing outside its transmission window. The centre frequency γ_0 is taken to be that corresponding to the minimum attenuation of fibre at a wavelength of 1550 nm. As a rule of thumb the maximum value of $\mathfrak{P}$ is around 100 W. This limitation is due mainly to heating in the fibre around imperfections that will result in the eventual catastrophic destruction of the fibre at power input levels above the rate at which the fibre can dissipate heat. High powers will also cause dispersion through nonlinear refractive index dependence on the input power resulting in a reduction in capacity. In addition, stimulated Brillouin and Raman scattering will result in an increase in noise proportional to $\mathfrak{P}^2$ that will quickly outweigh the quantum shot noise and therefore result in a reduction in maximum channel capacity. Substitution of these values into the above equations results in an ideal theoretical maximum value of C at about 600 Tb·s^{-1} for a single mode fibre. It's worth noting that the capacity of a very long fibre will be reduced due to attenuation. The present experimental limit is around 100 Tb·s^{-1} using multi-core fibre over many 10's of kilometres [7]. It is therefore clear that optical fibre has the potential to meet future demand for very high data rates.

However, while the transmission and routing of WDM channels in long haul and metro transport systems look set to continue to deliver ever increasing transmission rates, the electronic signal processing, serial MUX/DEMUX and buffering necessary can currently only be achieved using conventional electronic hardware systems. As will be shown, electronics based processing cannot continue to scale to sustain the ever increasing serial data rates that WDM backbones and metro networks will deliver and as a result, electronic bottlenecks will result.

3. Limits to Electronic Scalability

In 1974 Robert Dennard described the MOSFET scaling rules crucial to reducing transistor size while at the same time increasing switching speed and reducing power consumption [8]. These scaling principles were adopted by the semiconductor industry to develop and improve silicon devices and the terms 'Dennard Scaling' and 'Dennard's Law' were coined. Dennard scaling states that as transistor size reduces, power consumption will reduce while maximum switching speed can be increased. An important observation of Dennard scaling is that power density (Watts/unit chip area) has remained constant as transistor density has increased. In addition, the density of transistors has been increasing by a factor of about two every 18 months for over 40 years. Gordon Moore first suggested such an exponential improvement in transistor density back in 1965 with an estimated doubling of transistor density every two years [9]. What has actually happened to date has validated what became known as 'Moore's law' despite the increasing technical challenges of integration. This trend is forecast by Intel to continue until around 2020 [10].

However, despite the continuation of Moore's law, Dennard scaling came to an end in 2005 with the development of 90 nm lithography. At this level, transistor gates become too thin to prevent current from leaking into the substrate, resulting in a rise in power density. The well-known relationship $P_d = CV^2 f$ illustrates the relationship between clock speed and power consumption where P_d is the transistor dynamic switching power consumption; C is the CMOS switch lumped capacitance which is the sum of the junction capacitances and gate capacitances; V is the supply voltage; and f is the clock frequency. The above expression for P_d can be justified by considering a CMOS inverter for example. Here a $1-0$ transition charges the equivalent capacitance through the source-drain of the PMOS type transistor, dissipating half the energy and in the $0-1$ transition the capacitor dumps the stored charge through the source-drain of the NMOS transistor resulting in an approximate total energy dissipation of $2 \cdot 1/2CV^2$ over one cycle.

There is also a brief short-circuit dynamic power consumption due to both transistors conducting simultaneously for a short time. This is due to the finite rise and fall time during a state transition which results in an input gate voltage range where both NMOS and PMOS transistors are open simultaneously.

Before leakage current became a problem at around 90 nm, as transistor dimensions reduced, C reduced allowing f to be increased and V to be reduced while at the same time reducing the power consumption P_d and maintaining the overall power density of the chip about constant. This power scaling is also true of the short-circuit power. Performance per watt rose as transistor density increased and therefore the energy per bit reduced. However, leakage current due to gate oxide tunnelling has become an issue due to the scaling of the gate oxide thickness. In addition, a reduction in the threshold voltage has resulted in increasing sub-threshold leakage currents. As a result, power consumption has been increasing dramatically and the performance per watt, while still rising, is doing so at a slower rate. However the resulting increased power density runs the risk of causing thermal runaway and destruction of the chip in addition to creating cooling challenges and power consumption cost issues when scaled to the size of a data centre.

In the absence of a mature alternative technology to overcome the leakage current problem it is necessary to reduce power consumption by reducing the clock frequency and therefore the processing speed. Consequently, since 2005 chip manufacturers Intel and AMD have concentrated on introducing parallel processing CPUs using multicore processors to increase processing power. While parallel processing can, to a degree compensate for limited clock frequencies, it clearly results in at least a linear increase in power consumption since an effective doubling in performance requires at least two processors.

However, Amdahl's parallelism law states that 'If a computation has a serial component S % and a parallel component P %, then the maximum speed-up given an infinite number of processors is $(S+P)/S$'. Clearly, the greater the parallel portion P [11], the higher the speed-up. Amdahl's law says that there is a fundamental maximum improvement in computational speed that is dependent upon the proportion of serial computation, beyond which further additional parallel processors will contribute a rapidly diminishing improvement in processing speed.

Consequently the performance per watt which is initially constant will eventually decrease rapidly as the number of processors is increased beyond the optimum number. This principle is illustrated in Fig. 2 for four parallel processing portions P. As the number of parallel processors increases, a maximum speed-up is achieved, beyond which the addition of further processors provides no additional computational advantage and only serves to increase power consumption. As demand grows, a data bottleneck will result with increases in contention and an associated increase in latency. It is therefore expected that data centres will become unable to comply with the minimum quality of service they are contracted to provide. In the longer term, the answer to satisfying the rapid increase in demand for processing power in data centres will therefore not be found using present MOSFET electronic technology. The fundamental limits of data switching in this bandwidth limited technology may be reached sooner rather than later. In the short term, while Moore's law holds and effective cooling can be achieved, processing speeds can continue to rise. However power density will no longer be constant as previously predicted by Dennard's Law but will increase with processor density. However, the energy consumed per bit will continue to reduce, albeit at a slower rate than before.

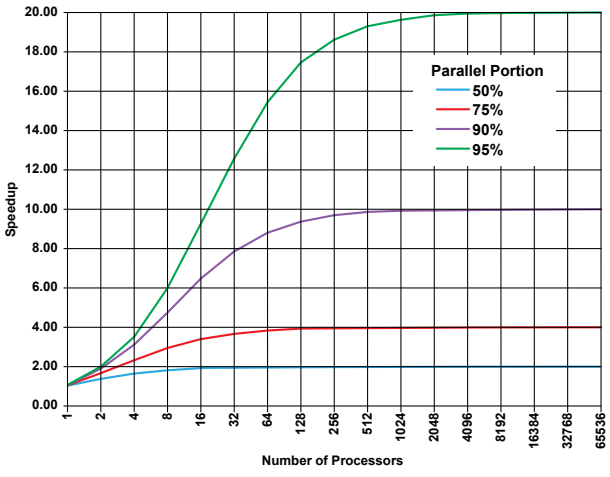


Fig. 2: The effect of Amdahl's law.

The fundamental limits to parallelism indicated by Amdahl's law (assuming that there will always be a serial computation portion) and limits to the sustainable power density in MOSFET based processors dictated by thermal runaway and processor/cooling power consumption concerns lead to a fundamental limit on the processing power of present electronic data centres.

In the short term, increasing clock speeds to satisfy demand is therefore not a realistic solution. Research into reducing CMOS leakage currents has demonstrated improvements in data handling capacity and power efficiency [12]. However, these improvements have been slow with only modest gains in reduced leakage current achieved. Graphene [13] and nanowire [14] technologies are being investigated as a replacement for current CMOS based devices. However, research in these areas is in its infancy and operational devices are many years from market. As a mature technology, photonics may hold the key to enabling data networks meet growing demand in the long term.

4. From Electronics to Photonics

It is therefore clear that optical fibre has the potential to meet future demand for very high serial data rates; and given the necessary serial WDM channel MUX/DEMUX and optical switching technology, optical fibre could be utilised to provide highly scalable, high speed all-optical interconnects in data networks.

Despite the many technical challenges to the realisation of all-optical data networks, advances have been made in the use of optical routing in data networks. The recent development of the reconfigurable optical add/drop multiplexer (ROADM) has allowed the reduction in use of power hungry and band limited O/E and E/O transceivers in optical cross connects for data network metro and long haul nodes [15]. ROADMs allow individual DWDM wavelengths to be added or dropped. However wavelength granularity is low and the best systems use 80 channel wavelengths. Electronic time division MUX/DEMUX for example al-

lows the capacity of each channel to be better utilised. However, electronic switching speed limits full use of the channel bandwidth available. For example, using a 50 GHz ITU grid, the theoretical capacity of each channel is around 0.5 Tb·s^{-1} per wavelength channel based on the capacity calculation in section 2. The best OC-768 systems presently manage only $768 \cdot 51.84$ Mb·s^{-1} or around 40 Gb·s^{-1} due to bandwidth limited electronic switching.

Within the data centre, optical interconnects in the form of Intel's Light Peak technology using silicon photonics are available for use in interconnecting servers to the top of the rack (TOR) switch with data rates of 10 Gb·s^{-1} over many tens of metres [16]. While this technology can overcome the attenuation and bandwidth limits of copper cables, it still requires bandwidth-limited and power hungry E/O and O/E transceivers.

Clearly the all-optical data network where all processing is done optically has yet to be realised and many technical barriers have yet to be overcome. However, in the meantime improvements in reduced contention and latency and reduced cost and power consumption are promised by the development of hybrid systems such as HELIOS and c-Through [17]. HELIOS is a 2-layer WDM based architecture using modular POD (performance optimised data centre) units. At the POD layer, packet switching is achieved using commodity switches; and at the core layer, optical circuit switching is used in parallel with commodity packet switching. Optical circuit switching is achieved using MEMS switches in DWDM links, facilitating the use of optical interconnects and reducing the requirement for power hungry transceivers and commodity switches. However, ultimately both systems are limited by the need for electronic packet switching since the optical buffering required for all-optical packet switching (OPS) has not yet been realised.

A recent approach to achieving a form of optical packet switching is the DOS (Datacentre Optical Switch) architecture [18]. Here the switching of optical packets is based on an arrayed waveguide grating router (AWGR) switching fabric where different inputs can reach the same output simultaneously using different wavelengths avoiding contention in the wavelength domain. This non-blocking switching is achieved using a tunable wavelength converter at each node. By selectively tuning the wavelength converter, a node can access any other node via the AWGR and packets are therefore routed accordingly. This system is power efficient too since the signal is delivered to the output port via a specific wavelength rather than using broadcast and select where associated power dividing losses occur. In simulations low latency, high-throughput switching were reported. In addition, latency was found to be almost independent of the number of input ports and saturation did not occur even at 90 % input loads.

5. The Future

It is clear from the discussion that the fundamental limits on electronic switching speeds and parallel processing will in the near future severely affect the ability of data networks to satisfy, both quantitatively and qualitatively, the exponentially increasing demand for data. A new solution is required to greatly improve available bandwidth and serial processing speed. The requirement for a new disruptive technology is therefore inevitable. Ideally, development of a photonic transistor allowing faster switching based on silicon photonics and present CMOS fabrication techniques would allow cheaper to market solutions than developing an all new ground-up fabrication technology. Silicon photonics devices can be fabricated using present CMOS fabrication techniques and therefore this technology is being investigated for the development of future optical signal processing systems [19].

However, a fundamental problem to developing the all-optical CPU is the difficulty in developing a silicon photonic transistor and optical interconnect technology necessary to carry out logic operations and provide the buffering necessary. To perform as a logic element, an optical transistor must especially satisfy the conditions of gain for fan-out and be able to be cascaded. Research in this area is in its infancy however, some progress in the development of the optical transistor has been reported and several research groups have been successful in demonstrating what may become possible future solutions to this problem.

Chen et al. have demonstrated an optical transistor where a single stored gate photon can control the transmission of applied source photons [20] (where the terms 'gate' and 'source' are used as an analogue to the CMOS FET transistor). The gate photon is effectively the analogue of the gate voltage in a CMOS transistor. Here, a weak light gate pulse is stopped and stored inside an optical resonator. A single stored gate photon controls the transmission of applied source photons resulting in an 80 % source attenuation. One stored gate photon was shown to switch many hundreds of source photons. In fact more gate photons can be stored resulting in an improved efficiency in source attenuation. The construction consists of an optical resonator formed by two mirrors at either side of a high finesse sealed optical cavity containing super-cooled caesium gas. The mirror separation is precisely calibrated for the wavelength of light to allow resonance while preserving phase. The source photons pass through the first mirror, entering the resonator and reflecting back and forth. This process allows the creation of a

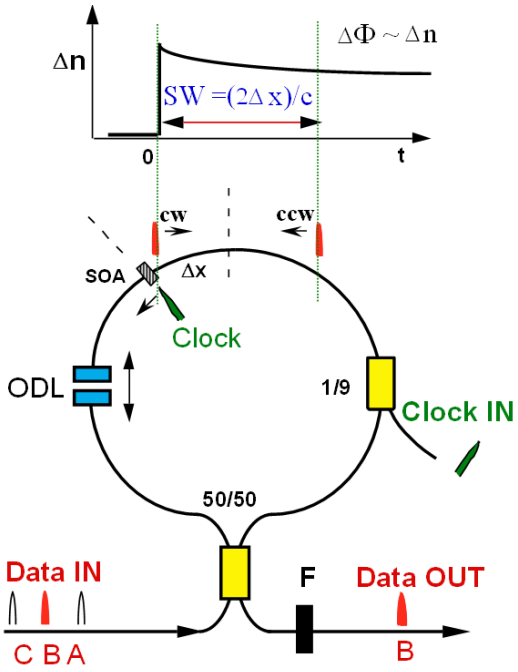
large electromagnetic field overcoming the confinement of the resonator and allows the light to pass through. When a single gate photon is fired into the resonator, it is absorbed and re-emitted many times as it reflects back and forth between the mirrors. Eventually the entire cloud of Caesium gas behaves like it is in an excited state, blocking the resonator transmission and effectively switching the transistor to the off state. The transistor is switched back on again by applying another gate pulse to the caesium gas.

This result has demonstrated a key requirement of the ability to turn a strong signal on and off using a weak one thereby allowing fan out where a single output could be used to control hundreds of other transistors. Also, since the source requires only one photon to control the source output, the potential exists for extremely low switching power consumption. In addition, since photons are effectively stored, this principle may be applicable to the development of the much sought after optical memory necessary for buffering data in data networks. However, the transistor is clearly not compatible with CMOS fabrication and since it requires three lasers for the gate and source; and lasers to allow super-cooling of the caesium gas, it is unlikely to provide a practical solution in the foreseeable future.

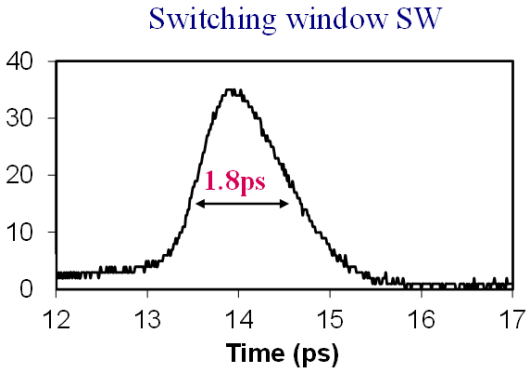
Another approach by Varghese et al. [21] is the development of a silicon optical transistor which uses an asymmetric coupled add/drop filter consisting of a micro-ring resonator next to an optical waveguide representing the source. Normally light will pass through the source waveguide and exit unaffected since weak source coupling with the micro-ring ensures that nonlinear effects are negligible. Its resonance will therefore remain unaffected. However, at a specific resonant frequency the light will interact with the micro-ring resonator greatly reducing the output and changing the state to off. This change in resonant frequency is achieved using another optical waveguide representing the gate. The input of the required light power to the gate waveguide couples in enough power to cause non-linear effects (e.g. the Kerr effect) in the micro-ring introducing an appreciable red-shift through the thermo-optic effect. This has the effect of changing the resonant frequency to that required to switch the source state from on to off. Since the source frequency is identical to the gate frequency, the cascadability requirement is satisfied. The ratio of the gate to source signals is reported to be nearly 6 dB which allows fan-out to at least two other optical transistors. In addition, the device is reported to operate at 10 GHz. A notable advantage of this technology is compatibility with current state of the art CMOS fabrication techniques allowing scalability and avoiding the need to develop new fabrication techniques from the ground up.

Given a future where networks will need to perform ultra high speed serial data processing all optically, there will be basic requirements for all optical MUX/DEMUX devices capable of performing at such speeds. One very effective all-optical technique uses an ultrafast all-optical gate known as Terahertz Optical Asymmetric Demultiplexer, TOAD [22] (see Fig. 3(a)). TOAD is based on a semiconductor optical amplifier (SOA) placed asymmetrically inside of the Sagnac interferometer.

However SOAs fundamentally suffer from gain recovery limitations [23], [24] which can be clearly seen in Fig. 3(b). To overcome this bottleneck ultimately limiting the width of the TOAD gating/demultiplexing

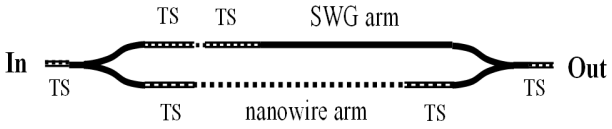


(a) Schematic diagram of TOAD

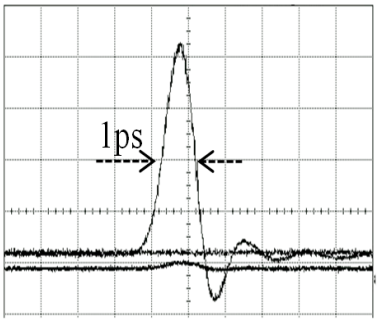


(b) TOAD measured switching window

Fig. 3: Top: indication of all optically induced SOA index change Δn, ODL: optical delay line, OM: Sagnac loop optical midpoint, SOA: optical semiconductor amplifier, F: optical clock blocking filter, c: speed of light, SW: the width of the switching window.



(a) Schematic diagram of Timing Gate (TG)



(b) Experimental demonstration of its picosecond switching capabilities

Fig. 4: TS: tapered section, SWG: subwavelength waveguide gating.

window SW, thus setting the minimum bit-width to be demultiplexed to a few picoseconds, Glesk et al. developed and demonstrated an ultrafast all optical time gate (TG). This TG is effectively a picosecond all-optical photonic switch [25] which does not suffer from the limitation imposed on TOAD by the SOA and is capable of sub picosecond switching operations. The schematic diagram of the TG is shown in Fig. 4(a). Its performance has been tested and sub picosecond switching capabilities were confirmed (Fig. 4(b)).

TG has a Mach-Zehnder interferometric structure with one arm composed of a nanowire while the second arm is a subwavelength waveguide grating (SWG) structure. Tapered sections marked TS are added to properly balance the device properties and the loss to help achieve complete interferometric switching.

6. Conclusion

Optical fibre networks have a vast potential data handling capacity. However this capability is becoming severely hampered by the serial data processing speed limitation of currently available CMOS electronics. Speed-up using parallel processing is confounded by the fundamental limits of Amdahl's Law. This scenario will soon hinder the ability of data networks to scale up to meet exponentially increasing demand for capacity. While all-optical wavelength routing can help improve data network throughput, ultimately at network endpoints any such improvement will be choked by fundamentally limited CMOS electronic signal processing capabilities. There is a need for the development of a disruptive technology to overcome this bottleneck. A promising candidate is all-optical signal processing. Progress has been made in the development of the photonic devices necessary to achieve this goal. However any further progress will require speedy development of ultrafast "all-optical transistor" based photonic logic gates.

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