VDCC Based Dual-Mode Quadrature Sinusoidal Oscillator with Outputs at Appropriate Impedance Levels

Mayank SRIVASTAVA[1], *Dinesh PRASAD*[2]

[1]Department of Electrical, Electronics and Communication Engineering, The Northcap University, HUDA Sector-23 A, 122017 Gurgaon, India
[2]Department of Electronics and Communication Engineering, Faculty of Engineering and Technology, Jamia Millia Islamia, 110025 New Delhi, India

mayank2780@gmail.com, dprasad@jmi.ac.in

DOI: 10.15598/aeee.v14i2.1611

Abstract. *This article presents a new dual-mode (i.e. both current-mode and voltage-mode) quadrature sinusoidal oscillator using two Voltage Differencing Current Conveyors (VDCCs), two resistors and two capacitors. The proposed configuration use only grounded passive elements and enjoys independent resistor/electronic tuning of both Condition of Oscillation (CO) as well as Frequency of Oscillation (FO). The quadrature current and voltage mode outputs of this circuit are available at appropriate impedance terminals. The behavior of presented oscillator is also examined under non ideal/parasitic conditions. The validity of the proposed configuration has been confirmed by SPICE simulations with TSMC 0.18 µm process parameters.*

Keywords

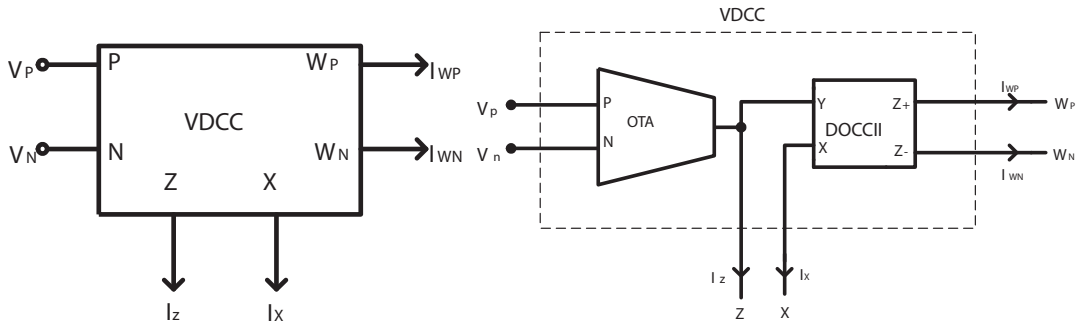
Dual-mode oscillator, electronic control, high impedance CM outputs, low impedance VM output, VDCC.

1. Introduction

Oscillator is an important circuit configuration, which finds several applications in measurement, signal processing, communication, instrumentation and control systems [1], [2], [3], [4], [5]. A quadrature sinusoidal oscillator which provides two 900 phase shifted sinusoidal outputs simultaneously is widely used in telecommunication engineering applications such as in quadrature mixers, single sideband modulators and direct-conversion receivers or for measurement purpose in selective voltmeters and vector generators [6], [7], [8]. Several VM and CM quadrature sinusoidal oscillators employing different Active Building Blocks (ABBs) have been reported in open literature. Careful investigation of literature available on quadrature oscillators reveals that most of the oscillators provide either voltage mode quadrature outputs or current mode quadrature outputs but only very few circuits are those which provide voltage mode and current mode quadrature outputs simultaneously. This simultaneous availability of quadrature outputs is very useful in mixed mode applications where current and voltage signals are required together.

The earlier work on dual-mode quadrature sinusoidal Oscillators employing different active element(s) has been reported in [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21]. Unfortunately, these reported circuits suffer from one or more of following drawbacks: (i) presence of floating passive component(s), which is not desirable from the viewpoint of monolithic integration (ii) lack of independent electronic control of both FO and CO (iii) lack of independent resistive control of both FO and CO (iv) non-availability of quadrature VM outputs at low impedance terminals (which need additional voltage followers for cascading) and (v) non-availability of high impedance explicit quadrature CM outputs (which need additional current followers for sensing and taking out the currents) (vi) use of ABB with current copy terminal(s) to get explicit CM outputs (which need additional MOSFETs/BJTs to realize current copy terminal(s).

Therefore, the purpose of this article is to present a new CM/VM sinusoidal quadrature oscillator employing two VDCCs, two resistors and two capacitors which enjoys following advantageous features simultaneously



(a) Circuit symbol of VDCC. (b) Behavioral model of VDCC.

Fig. 1: VDCC circuit symbol and behavioral model.

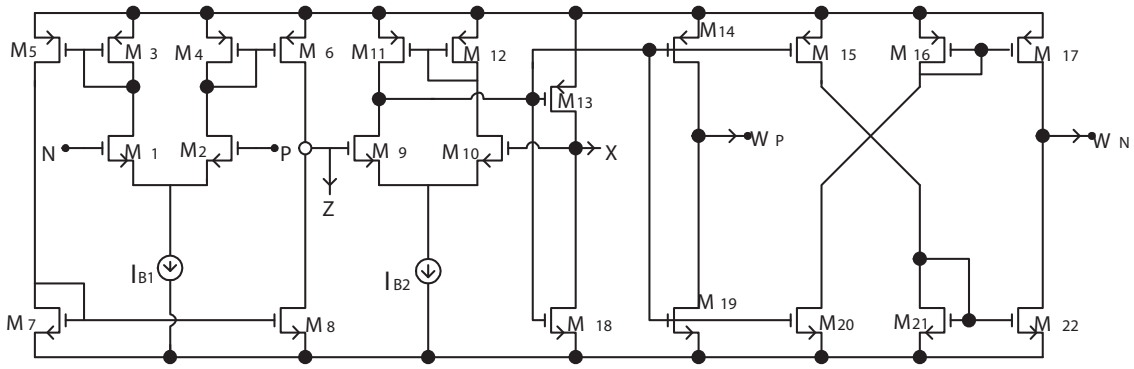


Fig. 2: CMOS implementation of VDCC [23].

which are not available with any of the previously proposed quadrature oscillator configurations;

- Use of all grounded passive components.
- Independent electronic control of both FO and CO.
- Independent resister control of both FO and CO.
- Independent tuning of FO and CO under non-ideal conditions.
- Independent tuning of FO even under the influence of parasitics.
- Availability of high impedance explicit CM quadrature outputs.
- Availability of low impedance quadrature VM outputs.
- Low active/passive sensitivities.
- Good frequency stability.

VDCC is a versatile ABB proposed by Biolek in 2008, which provides electronically tunable transconductance gain in addition to transferring both current and voltage in its relevant terminals [22]. Some applications of VDCC as grounded/floating inductor simulators [23], [24], Single Resistance Controlled Oscillator (SRCO) [25] and voltage mode biquad filter [26] have been reported in available literature.

The circuit symbol and behavioral model of VDCC are shown in Fig. 1, where P and N are input terminals and Z, X, WP and WN are output terminals. The terminals Z, X, WP and WN exhibit high impedances while X is a low impedance terminal. The CMOS implementation of VDCC [23] has been shown in Fig. 2. The ideal terminal characteristics of VDCC can be defined by the hybrid matrix as given by Eq. (1):

$$\begin{bmatrix} I_N \\ I_P \\ I_Z \\ V_X \\ I_{W_P} \\ I_{W_N} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -1 \end{bmatrix} \cdot \begin{bmatrix} V_P \\ V_N \\ V_Z \\ I_X \end{bmatrix}. \quad (1)$$

2. Proposed Quadrature Oscillator

The proposed dual-mode quadrature oscillator is shown in Fig. 3.

The routine circuit analysis of proposed dual mode quadrature oscillator configuration as shown in Fig. 3,

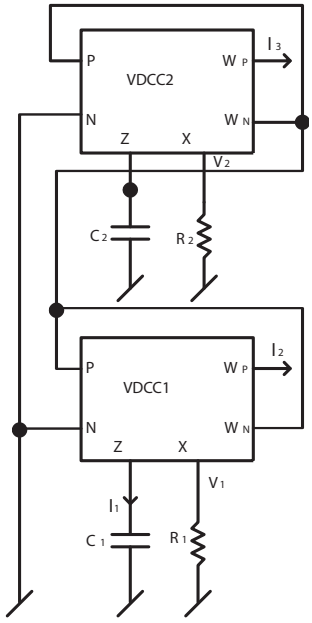


Fig. 3: The proposed dual-mode quadrature oscillator configuration.

yields the following characteristic equation:

$$s^2 + s\frac{1}{C_2}\left(\frac{1}{R_2} - g_{m_2}\right) + \frac{g_{m_1}}{R_1 C_1 C_2} = 0. \tag{2}$$

Thus, from Eq. (2), are the CO Eq. (3) and FO Eq. (4).

$$\left(\frac{1}{R_2} - g_{m_2}\right) \leq 0. \tag{3}$$

$$\omega_0 = \sqrt{\frac{g_{m_1}}{R_1 C_1 C_2}}. \tag{4}$$

From Eq. (3) and Eq. (4) it is clear that CO can be set by R_2 or g_{m_2} and FO is tuned by R_1 or g_{m_1}. Hence, CO and FO both enjoy the independent electronic as well as resistive tuning.

The expressions of CO and FO do not have any common term. Thus, the proposed circuit has the feature of completely non-interactive control of CO and FO. The current relationships derived from Fig. 3 are:

$$\frac{I_2(s)}{I_1(s)} = \frac{1}{sR_1C_1}. \tag{5}$$

$$\frac{I_2(s)}{I_3(s)} = \frac{g_{m_1}R_2}{sC_1R_1}. \tag{6}$$

For sinusoidal steady state, Eq. (5) and Eq. (6) become:

$$\frac{I_2(j\omega)}{I_1(j\omega)} = \frac{1}{\omega R_1 C_1} e^{-j90^\circ}. \tag{7}$$

$$\frac{I_2(j\omega)}{I_3(j\omega)} = \frac{g_{m_1}R_2}{\omega C_1 R_1} e^{-j90^\circ}. \tag{8}$$

It is evident from Eq. (7) and Eq. (8) that the phase difference between currents (I_{o2} and I_{o1}) and (I_{o2} and I_{o3}) is -90°. Hence, the currents (I_{o1} and I_{o2}), and (I_{o2} and I_{o3}) are in phase quadrature. The currents I_{o2} and I_{o3} are explicit quadrature current outputs at high impedance terminals.

The voltage transfer function from V_1 (voltage at "X" terminal of VDCC1) to V_2 (voltage at "X" terminal of VDCC2) is:

$$\frac{V_1(s)}{V_2(s)} = \frac{g_{m_1}}{sC_1}. \tag{9}$$

In sinusoidal steady state:

$$\frac{V_1(j\omega)}{V_2(j\omega)} = \frac{g_{m_1}}{\omega C_1} e^{j-90^\circ}. \tag{10}$$

Hence, the phase difference between V_1 to V_2 is -90° i.e. V_2 and V_1 are in quadrature form and are available at low impedance terminals. Thus, the proposed circuit configuration can provide both VM and CM quadrature signals simultaneously at appropriate impedance levels.

3. Effects of VDCC Parasitics

In this section, the proposed quadrature oscillator is investigated under the influence of VDCC terminal parasitics. In CMOS VDCC (shown in Fig. 2) parasitic resistance R_x appears in series with X terminal, parasitic resistance R_P and parasitic capacitance C_P appears in parallel between W_P terminal and ground,parasitic resistance R_N and parasitic capacitance C_N appears in parallel between W_N terminal and ground and a grounded parasitic resistance R_Z appears at Z terminal. The proposed oscillator configuration including VDCC terminal parasitics has been shown in Fig. 4.

The effect of low resistance parasitic resistors R_{X1} and R_{X2} can be eliminated by merging them with external resistors R_1 and R_2 respectively. It is further noted the low parasitic capacitances C_{N1} and C_{N2} are in parallel with external capacitor C_2. So, the effects of C_{N1} and C_{N2} can be alleviated by merging them with C_2. Therefore, the influence of parasitic capacitances can be completely removed from the proposed oscillator configuration but grounded parallel parasitic resistances R_{N1}, R_{N2}, R_{Z1} and R_{Z2} cannot be balanced and will affect the circuit. To minimize the influence of theses parasitic resistances, the operating frequency can be chosen as Eq. (11).

$$\omega_0 >> \max\left\{\frac{1}{(C_{N1}+C_{N2}+C_2)\left(\frac{1}{\frac{1}{R_{N1}}+\frac{1}{R_{N2}}+\frac{1}{R_{Z2}}}\right)}, \frac{1}{C_1R_{Z1}}\right\}. \tag{11}$$

$$\max\left\{\frac{1}{(C_{N1}+C_{N2}+C_2+)\left(\frac{1}{\frac{1}{R_{N1}}+\frac{1}{R_{N2}}+\frac{1}{R_{Z2}}}\right)}, \frac{1}{C_1R_{Z1}}\right\} << \omega_0 << \min\frac{1}{R_{P1}C_{P1}}, \frac{1}{R_{P2}C_{P2}}. \tag{12}$$

$$\frac{1}{C_1R_{Z1}}+\frac{\left(\frac{1}{R_{N1}}+\frac{1}{R_{N2}}+\frac{1}{R_{Z2}}\right)}{(C_{N1}+C_{N2}+C_2)}+\frac{\frac{1}{R_2+R_{X2}}}{C_{N1}+C_{N2}+C_2}-\frac{g_{m_2}}{C_{N1}+C_{N2}+C_2}\leq 0. \tag{13}$$

$$\omega_0=\sqrt{\frac{\frac{g_{m_1}}{(R_1+R_{X1})}-\frac{g_{m_2}}{R_{Z1}}+\frac{1}{R_{Z1}}\left(\frac{1}{R_{N1}}+\frac{1}{R_{N2}}+\frac{1}{R_{Z2}}\right)+\frac{1}{R_{Z1}}\left(\frac{1}{R_2+R_{X2}}\right)}{(C_{N1}+C_{N2}+C_2)\,C_1}}. \tag{14}$$

The parasitic resistance R_{P1} (or R_{P2}) and parasitic capacitance C_{P1} (or C_{P2}) appear between W_p terminal of VDCC1 (or W_p terminal of VDCC2) and ground. The phase relationship between current I_2 and I_3 will be changed due to these parasitic components. So, to reduce the effect of these parasitics, the operating frequency (ω_0) has to be chosen as:

$$\omega_0 << \min\left\{\frac{1}{R_{P1}C_{P1}}, \frac{1}{R_{P2}C_{P2}}\right\}. \tag{15}$$

Therefore, the useful operating frequency range of presented quadrature oscillator circuit can be described by combining conditions given in Eq. (11) and Eq. (15) we obtain Eq. (12)

The CO and FO of oscillator shown in Fig. 4 are given for CO Eq. (13) and for FO Eq. (14).

From Eq. (13) and Eq. (14) it is clear that even under the influence of parasitics the FO can be independently tunable by g_{m_1}. So, proposed configuration exhibits low parasitic effects.

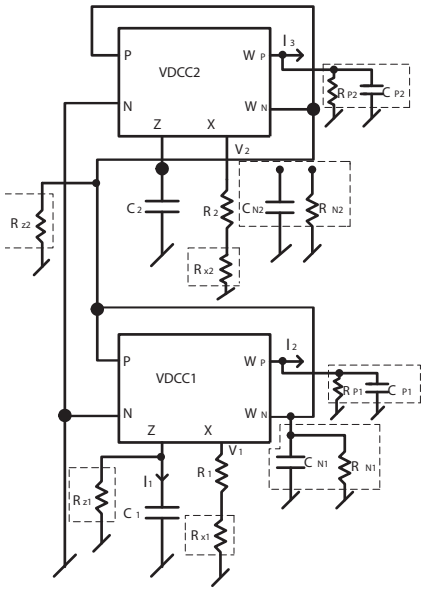


Fig. 4: The proposed dual-mode quadrature oscillator configuration with VDCC terminal parasitics.

4. Non-Ideal Analysis and Sensitivity Calculations

In the non-ideal case, the VDCC can be characterized by the following equations:

$$I_Z = \alpha g_{m_1} (V_P - V_N), \tag{16}$$

$$V_Z = \beta V_X, \tag{17}$$

$$I_{WP} = \gamma_{WP} I_X, \tag{18}$$

$$I_{WN} = -\gamma_{WN} I_X, \tag{19}$$

where α, γ_{WP}, γ_{WN} are current tracking errors and β is voltage tracking error.

Considering the non-idealities of VDCC-1 and VDCC-2, the characteristic equation of circuit shown in Fig. 4 becomes:

$$s^2 + s\frac{1}{C_2\beta_1\beta_2}\left(\frac{\beta_1\gamma_{WN_2}}{R_2} - \beta_1\beta_2\alpha_2 g_{m_2}\right) + \ldots \\ \ldots + \frac{g_{m_1}\alpha_1\gamma_{WN_1}}{R_1C_1C_2\beta_1} = 0, \tag{20}$$

where (α_1, β_1, γ_{WP_1}, γ_{WN_1}) and (α_2, β_2, γ_{WP_2}, γ_{WN_2}) are tracking errors of VDCC-1 and VDCC-2 respectively.

The CO and FO of proposed circuit under non ideal conditions can be found from Eq. (20), for CO: Eq. (21) and for FO: Eq. (22):

$$\left(\frac{\beta_1\gamma_{WN_2}}{R_2} - \beta_1\beta_2\alpha_2 g_{m_2}\right) \leq 0. \tag{21}$$

$$\omega_0 = \sqrt{\frac{g_{m_1}\alpha_1\gamma_{WN_1}}{R_1C_1C_2\beta_1}}. \tag{22}$$

It is noted from Eq. (21) and Eq. (22) that CO and FO are independently tunable under non-ideal conditions as well, CO by g_{m_2} or β_2 or α_2 or γ_{WN_2} and FO by g_{m_1} or α_1 or γ_{WN_2}, which confirm the good non-ideal behavior of presented oscillator. The sensitivities of ω_0 with respect to R_1, R_2, C_1, C_2, g_{m_1}, g_{m_2} under the influence of terminal parasitics of VDCCs are given by Eq. (23).

Also under non-ideal conditions, the sensitivities of ω_0 with respect to various active and passive elements are obtained in Eq. (24).

So, it can be seen from Eq. (24), that all the sensitivities under non-ideal conditions are low and not more than half in magnitude.

The frequency Stability Factor S^F of proposed oscillator is found to be $2\sqrt{n}$ for $C_1 = C_2$, $1/R_2 = g_{m_2}$, and $1/R_1 = ng_{m_1}$. Therefore, a high value of frequency stability can be achieved by selecting large value of n.

5. Simulation Results

The performance of proposed oscillator has been verified by SPICE simulations using TSMC CMOS 0.18 µm processes parameters. Simulations have been performed using CMOS VDCC (shown in Fig. 3) with supply voltages ±0.9 VDC and transconductances gains $g_{m_1} = g_{m_2} = 277$ µA·V^{-1}. The passive component values were chosen as: $R_1 = 5$ kΩ, $R_2 = 3.65$ kΩ, $C_1 = C_2 = 0.05$ nF. The dimensions of MOS transistors used in simulation have been given in Tab. 1.

Tab. 1: Dimensions of MOS transistors.

Transistor	W/L (µm)
M_1, M_2, M_3, M_4	3.6/1.8
M_5, M_6	7.2/1.8
M_7, M_8	2.4/1.8
M_9, M_{10}	3.06/1.72
M_{11}, M_{12}	9.0/1.72
M_{13}, M_{14}, M_{15}, M_{16}	14.4/1.72
M_{17}	13.85/1.72
M_{18}, M_{19}, M_{20}, M_{21}, M_{22}	0.72/0.72

Simulated current and voltage responses have been shown in Fig. 5 and Fig. 6 respectively. The lissajous figures shown in Fig. 7 and Fig. 8 are ellipses with no tilt in axis which confirm the quadrature relationship of current I_2 with current I_3 and voltage V_1 with V_2. Output spectrum of current I_2 is shown in Fig. 9, where the frequency of oscillation equals to 737.8 kHz and the Total Harmonic Distortion (THD) is found to be 2.66 %. Figure 10 shows the variation of amplitude and frequency of current output I_2 on varying resistance R_1. The electronic control of FO (of I_2) with the bias current I_{B1} was shown in Fig. 11. The THD values of current I_2 for different values of bias current I_{B1} havebeen shown in Fig. 12 and it is clear here that except $I_{B1} = 55$ µA (for which THD is 3.55 %), for all other values of I_{B1} THD is less than 3 % which is under expectable range.

The robustness of proposed configuration has been checked by Monte-Carlo simulations on ±10 % variation of R_2 and the sample results are shown in Fig. 13.

It can be illustrated from Fig. 13 that, the frequency of oscillation varies from 721.176 kHz (minimum value) to 739.103 kHz (maximum value) with mean value of 732.578 kHz. So, the variation from mean frequency is 1.5 % (lower side) and 0.088 % (upper side), which confirms the good frequency stability.

These results thus validate the feasibility of proposed configuration.

A comparison of proposed oscillator configuration with previously reported second order dual mode quadrature sinusoidal oscillators has been summarized in Tab. 2.

$$S_{R_1}^{\omega_0} = \frac{g_{m_1} R_1}{2\left[\frac{g_{m_1}}{R_1+R_{X1}} - \frac{g_{m_2}}{R_{Z1}} + \frac{1}{R_{Z1}}\left(\frac{1}{R_{N1}}+\frac{1}{R_{N2}}+\frac{1}{R_{Z2}}\right) + \frac{1}{R_{Z1}}\left(\frac{1}{R_2+R_{X2}}\right)\right]} \left(R_1+R_{X1}\right)^2.$$

$$S_{R_2}^{\omega_0} = \frac{R_2}{2\left[\frac{g_{m_1}}{R_1+R_{X1}} - \frac{g_{m_2}}{R_{Z1}} + \frac{1}{R_{Z1}}\left(\frac{1}{R_{N1}}+\frac{1}{R_{N2}}+\frac{1}{R_{Z2}}\right) + \frac{1}{R_{Z1}}\left(\frac{1}{R_2+R_{X2}}\right)\right]} \left(R_2+R_{X2}\right)^2 R_{Z1}.$$

$$S_{C_1}^{\omega_0} = -\frac{1}{2}.$$

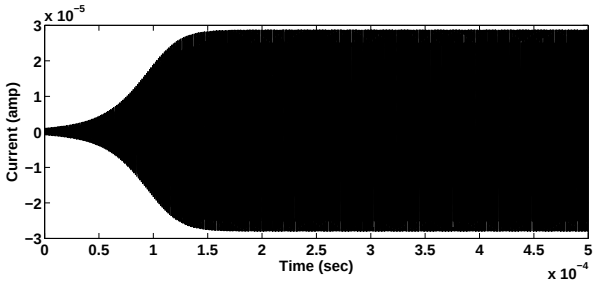
$$S_{C_1}^{\omega_0} = -\frac{C_2}{2\left(C_{N1}+C_{N2}+C_2\right)}. \tag{23}$$

$$S_{g_{m_1}}^{\omega_0} = \frac{g_{m_1}}{2\left[\frac{g_{m_1}}{R_1+R_{X1}} - \frac{g_{m_2}}{R_{Z1}} + \frac{1}{R_{Z1}}\left(\frac{1}{R_{N1}}+\frac{1}{R_{N2}}+\frac{1}{R_{Z2}}\right) + \frac{1}{R_{Z1}}\left(\frac{1}{R_2+R_{X2}}\right)\right]} \left(R_1+R_{X1}\right).$$

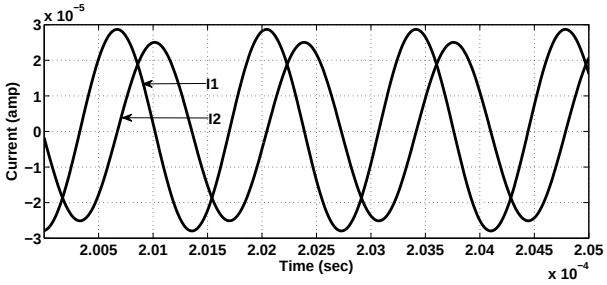
$$S_{g_{m_2}}^{\omega_0} = \frac{g_{m_2}}{2\left[\frac{g_{m_1}}{R_1+R_{X1}} - \frac{g_{m_2}}{R_{Z1}} + \frac{1}{R_{Z1}}\left(\frac{1}{R_{N1}}+\frac{1}{R_{N2}}+\frac{1}{R_{Z2}}\right) + \frac{1}{R_{Z1}}\left(\frac{1}{R_2+R_{X2}}\right)\right]} R_{Z1}.$$

$$S_{R_1}^{\omega_0} = -\frac{1}{2},\ S_{R_2}^{\omega_0} = 0,\ S_{g_{m_1}}^{\omega_0} = \frac{1}{2},\ S_{g_{m_2}}^{\omega_0} = 0,\ S_{C_1}^{\omega_0} = -\frac{1}{2},\ S_{C_2}^{\omega_0} = -\frac{1}{2},\ S_{\alpha_1}^{\omega_0} = \frac{1}{2},$$

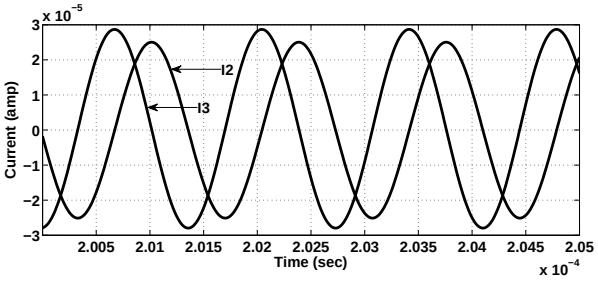
$$S_{\alpha_2}^{\omega_0} = 0,\ S_{\beta_1}^{\omega_0} = -\frac{1}{2},\ S_{\beta_2}^{\omega_0} = 0,\ S_{\gamma_{WP_1}}^{\omega_0} = 0,\ S_{\gamma_{WP_2}}^{\omega_0} = 0,\ S_{\gamma_{WN_1}}^{\omega_0} = 0,\ S_{\gamma_{WN_2}}^{\omega_0} = 0. \tag{24}$$



(a) Transient response of I_1, I_2 and I_3.

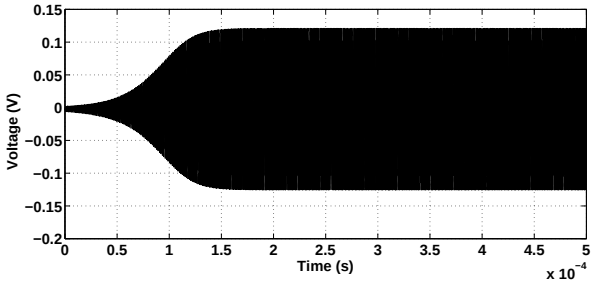


(b) Steady state response of I_1 and I_2.

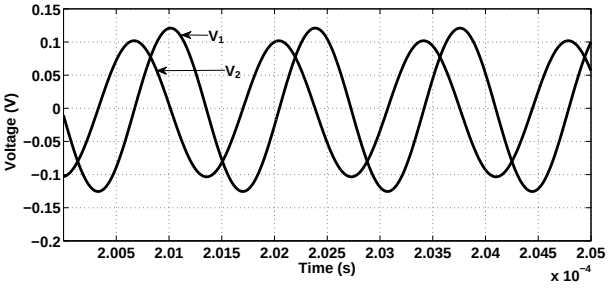


(c) Steady state response of I_2 and I_3.

Fig. 5: Simulated current responses.



(a) Transient response of V_1 and V_2.



(b) Steady state response of V_1 and V_2.

Fig. 6: Simulated voltage responses.

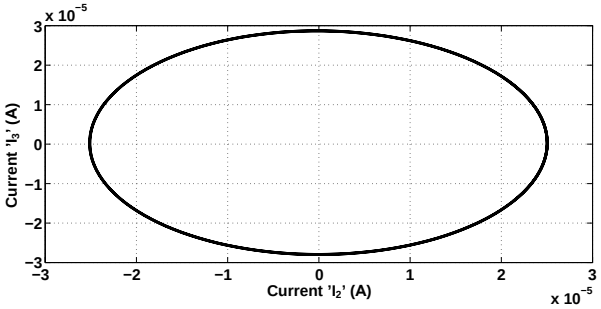


Fig. 7: Lissajous figure showing quadrature relationship between current I_2 and I_3.

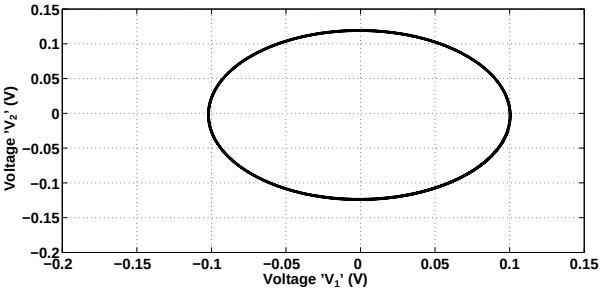


Fig. 8: Lissajous figure showing quadrature relationship between voltage V_1 and V_2.

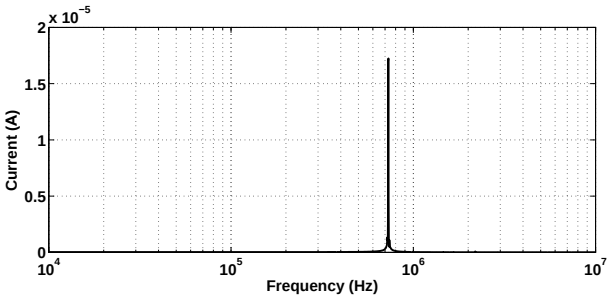


Fig. 9: Output spectrums of current I_2.

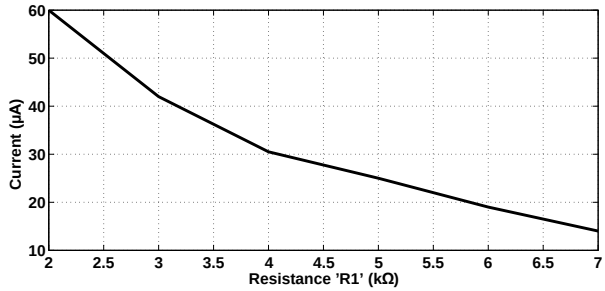


Fig. 10: Variation of of output current I_2 amplitude with resistance R_2.

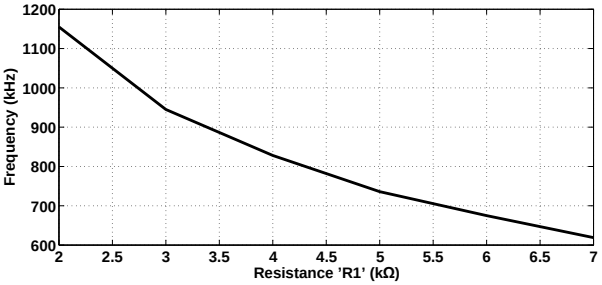


Fig. 11: Electronic tuning of operational frequency with bias current I_{B1}.

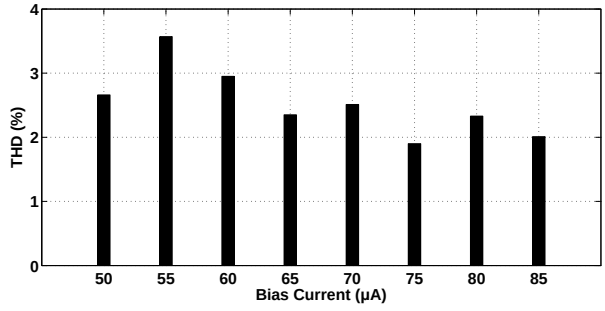


Fig. 12: THD at different values of bias current I_{B1}.

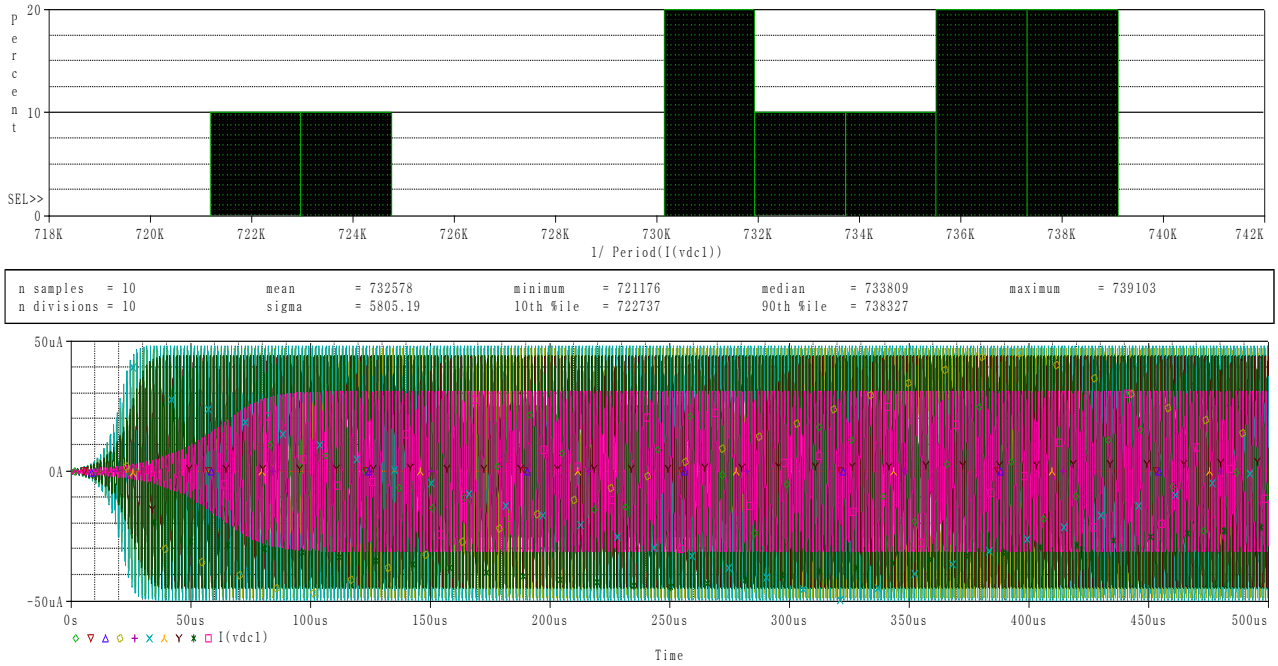


Fig. 13: Results of Monte-Carlo simulation of proposed oscillator.

Tab. 2: Comparison with other previously reported second order dual-mode quadrature oscillators.

Ref.	Number and name of active building blocks (ABBs)	Number of passive elements	All the passive elements grounded	Independent electro. tunability in both FO and CO	Independent resistor tunability in both FO and CO	Availability of VM quadrature outputs at low impedance terminals	Availability of explicit CM quadrature outputs at high impedance terminals	Use of ABB with additional copy terminal(s) to get explicit CM outputs
[9]	2-CDTA	3	Yes	No	No	No	Yes	Yes
[10]	1-MO-CCCDTA	3	Yes	No	No	No	Yes	Yes
[11]	3-CCII	5	No	No	Yes	No	Yes	Yes
[12]	1-FDCCII	5	Yes	No	Yes	No	Yes	Yes
[13]	1-FDCCII	4	Yes	No	No	No	No	Yes
[14]	3-DVCC	5	Yes	No	Yes	No	Yes	Yes
[15]	3-CCII	5	Yes	No	Yes	Yes	Yes	Yes
[16]	2-ZC-CG-CDBA	5	No	No	Yes	Yes	Yes	Yes
[17]	1- DO-CCCDTA	2	Yes	Yes	No	No	No	Yes
[18]	1-MCDTA + I-CFTA	2	Yes	Yes	No	No	Yes	Yes
[19]	2-CCCDTA+ 1-Voltage Buffer	2	Yes	Yes	No	No	No	No
[20]	3-CCCII	2	Yes	Yes	No	No	Yes	Yes
[21]	1-DVCCCTA	2	Yes	Yes	No	No	Yes	Yes
Prop.	**2-VDCC**	**4**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**No**

6. Conclusions

A new CM/VM quadrature sinusoidal oscillator employing two VDCCs, two grounded resistors and two grounded capacitors has been proposed. Use of grounded resistors and capacitors make the proposed configuration suitable for monolithic integration. The presented circuit configuration enjoys several advantageous features expected from a dual mode quadrature oscillator such as: independent electronic tuning of FO and CO, independent resistive control of FO and CO, explicit quadrature current outputs at high impedance terminals, quadrature voltage outputs at low impedance terminals, independent control of FO even under the influence of VDCC port parasitics, low active/passive sensitivities, good frequency stability and low non ideal effects. The SPICE simulation results confirm the validity of theoretical predictions.

References

[1] SENANI, R. New types of sine wave oscillators. *IEEE Transactions on Instrumentation and Measurement.* 1985, vol. 34, iss. 3, pp. 461–463. ISSN 0018-9456. DOI: 10.1109/TIM.1985.4315370.

[2] SENANI, R. and D. R. BHASKAR. Single op-amp sinusoidal oscillators suitable for generation of very low frequencies. *IEEE Transactions on Instrumentation and Measurement.* 1991, vol. 40, iss. 4, pp. 777–779. ISSN 0018-9456. DOI: 10.1109/19.85353.

[3] CHEN, J. J., C. C. CHEN, H. W. TSAO and S. I. LIU. Current-mode oscillators using single current follower. *Electronics Letters.* 1991, vol. 27, iss. 22, pp. 2056–2059. ISSN 0013-5194. DOI: 10.1049/el:19911276.

[4] ABUELMATTI, M. T. Grounded-capacitor current-mode oscillator using single current follower. *IEEE Transactions on Circuits and Systems.* 1992, vol. 39, iss. 12, pp. 1018–1020. ISSN 1057-7122. DOI: 10.1109/81.207726.

[5] BHASKAR, D. R. and R. SENANI. New CFOA-based single-element-controlled sinusoidal oscillators. *IEEE Transactions on Instrumentation and Measurement.* 2006, vol. 55, iss. 6, pp. 2014–2021. ISSN 0018-9456. DOI: 10.1109/TIM.2006.884139.

[6] GIBSON, J. D. *Communications handbook.* New York: CRC Press, 2002. ISBN 0-8493-0967-0.

[7] KHAN, I. A. and S. KHAWAJA. An integrable gm-C quadrature oscillator. *International Journal of Electronics.* 2001, vol. 87, iss. 11, pp. 1353–1357. ISSN 0020-7217. DOI: 10.1080/00207210750000150.

[8] BOLTON, W. *Measurement and Instrumentation Systems.* Oxford: Newnes, 1996. ISBN 978-0750631143.

[9] LAHIRI, A. Novel voltage/current-mode quadrature oscillator using current differencing transconductance amplifier. *Analog Integrated Circuits and Signal Processing.* 2009, vol. 61, iss. 2, pp. 1–8. ISSN 0925-1030. DOI: 10.1007/s10470-009-9291-0.

[10] CHEN, H. P. Electronically tunable quadrature oscillator using grounded components with current and voltage outputs. *The Scientific World Journal.* 2014, vol. 2014, ID 572165, pp. 1–8. ISSN 1537-744X. DOI: 10.1155/2014/572165.

[11] HORNG, J. W., H. P. CHOU and J. C. SHIU. Current-mode and voltage-mode quadrature oscillator employing multiple outputs CCIIs and grounded capacitors. In: *Proceeding of ISCAS-2006.* Island of Kos: IEEE, 2006, pp. 441–444. ISBN 0-7803-9389-9. DOI: 10.1109/ISCAS.2006.1692617.

[12] HORNG, J. W., C. L. HOU, C. M. CHANG, H. P. CHOU, C. T. LIN and Y. H. WEN. Quadrature oscillators with grounded capacitors and resistors using FDCCIIs. *ETRI Journal.* 2006, vol. 28, no. 4, pp. 486–494. ISSN 1225-6463. DOI: 10.4218/etrij.06.0105.0181.

[13] HORNG, J. W., C. L. HOU and C. M. CHANG. Current or/and voltage-mode quadrature oscillators with grounded capacitors and resistors using FDCCIIs. *WSEAS Transactions on circuits and Systems.* 2008, vol. 7, iss. 3, pp. 129–138. ISSN 1109-2734. DOI: 10.1.1.588.9029.

[14] MAHESHWARI, S. and B. CHATURVEDI. Versatile quadrature oscillator with grounded components. In: *International Conference IMPACT-2009.* Aligarh: IEEE, 2009, pp. 209–212. ISBN 978-1-4244-3602-6. DOI: 10.1109/MSPCT.2009.5164212.

[15] ABDALLA, K. K., D. R. BHASKAR and R. SENANI. Configuration for realising a current-mode universalfilter and dual-mode quadrature single resistor controlled oscillator. *IET Circuits, Devices and Systems.* 2012, vol. 6, iss. 3, pp. 159–167. ISSN 1751-858X. DOI: 10.1049/iet-cds.2011.0160.

[16] BIOLEK, D., A. LAHIRI, W. JAIKLA, M. SIRIPRUCHYANUN and J. BAJER. Realization of electronically tunable voltage-mode/current-mode quadrature sinusoidal oscillator using

ZC-CG-CDBA. *Microelectronics Journal.* 2011, vol. 42, iss. 10, pp. 1116–1123. ISSN 0026-2692. DOI: 10.1016/j.mejo.2011.07.004.

[17] JAIKLA, W. and M. SIRIPRUCHYANUN. A versetile quadrature oscillator and universal biquad filter using dual-output current controlled current differencing transconductance amplifier. In: *International Symposium on Communications and Information Technologies.* Bangkok: IEEE, 2006, pp. 1072–1075. ISBN 0-7803-9740-1. DOI: 10.1109/ISCIT.2006.339942.

[18] LAHIRI, A. Resistor-less mixed-mode quadrature sinusoidal oscillator. *International Journal of Computer and Electrical Engineering.* 2010, vol. 2, no. 1, pp. 63–66. ISSN 1793-8163. DOI: 10.7763/IJCEE.2010.V2.114.

[19] JAIKLA, W. and M. SIRIPRUCHYANUN. CCCDTAs-based versatile quadrature oscillator and universal biquad filter. In: *Proceedings of ECTI conference.* Chiang Rai: ETCI association, 2007, pp. 1065–1068. ISBN 978-1-4244-2101-5.

[20] MAHESHWARI, S. and I. A. KHAN. Mixed-mode quadrature oscillator using translinear conveyors and grounded capacitors. In: *International Conference on Multimedia, Signal Processing and Communication Technologies (IMPACT).* Aligarh: IEEE, 2011, pp. 153–156. ISBN 978-1-4577-1105-3. DOI: 10.1109/MSPCT.2011.6150462.

[21] JAIKLA, W., M. SIRIPRUCHYANUN and A. LAHIRI. Resistor-less dual mode quadrature sinusoidal oscillator using a single active building block. *Microelectronics Journal.* 2011, vol. 42, iss. 1, pp. 135–140. ISSN 0026-2692. DOI: 10.1016/j.mejo.2010.08.017.

[22] BIOLEK, D., R. SENANI, V. BIOLKOVA and Z. KOLKA. Active elements for analog signal processing; classification, review and new proposals. *Radioengineering.* 2008, vol. 17, no. 4, pp. 15–32. ISSN 1210-2512. DOI: 10.1.1.476.9997.

[23] KACAR, F., A. YESIL, S. MINAEI and H. KUNTMAN. Positive/ negative lossy/ lossless grounded inductance simulators employing single VDCC and only two passive elements. *International Journal of Electronics and Communication (AEU).* 2014, vol. 68, iss. 1, pp. 73–78. ISSN 1434-8411. DOI: 10.1016/j.aeue.2013.08.020.

[24] PRASAD, D. and J. AHMAD. New electronically-controllable lossless synthetic floating inductance circuit using single VDCC. *Circuits and Systems.* 2014, vol. 5, no. 1, pp. 13–17. ISSN 1549-8328. DOI: 10.4236/cs.2014.51003.

[25] PRASAD, D., D. R. BHASKAR and M. SRIVASTAVA. New single VDCC-based explicit current-mode SRCO employing all grounded passive components. *Electronics Journal.* 2014, vol. 18, no. 2, pp. 81–88. ISSN 2079-9292. DOI: 10.7251/ELS1418081P.

[26] KACAR, F., A. YESIL and K. GURKAN. Design and experiment of VDDC-based voltage mode universal filter. *Indian Journal of Pure and Applied physics.* 2015, vol. 53, no. 5, pp. 341–349. ISSN 0218-1266.

About Authors

Mayank SRIVASTAVA was born on in Agra, Uttar Pradesh, India. He obtained B. E. degree in Electronics and Communication Engineering from Dr. B. R. A. University, Agra, M. Tech. with specialization in Engineering Systems from Dayalbagh Educational Institute (Deemed University) Agra and Ph.D. in Analog integrated circuits and signal processing from Jamia Millia Islamia, New Delhi, India. Currently he is working as an Associate Professor with Department of Electrical Electronics and Communication Engineering, The Northcap University, Gurgaon (Haryana), India. His research interests are in the areas of Bipolar and CMOS Analog Integrated Circuits and Current Mode Signal Processing. Dr. Srivastava has authored or co-authored 19 research papers in International Journals and Conferences.

Dinesh PRASAD was born on 5. July 1977 in Gorakhpur, Uttar Pradesh, India. He obtained B. Tech. degree from the Institute of Engineering and Technology (IET), Lucknow, M. Tech. with specialization in Electronic Circuits and Systems Design from Aligarh Muslim University, Aligarh, India, and Ph.D. in the area of Analog Integrated Circuits and Signal Processing, from Jamia Millia Islamia (a Central University). Dr. Prasad joined the Electronics and Communication Engineering Department of the Faculty of Engineering and Technology, Jamia Millia Islamia, in February 2002 as a Lecturer. He became Sr. Lecturer on February 2007. His teaching and current research interests are in the areas of Bipolar and CMOS Analog Integrated Circuits, Current Mode Signal Processing and Circuits and Systems. Dr. Prasad has authored or co-authored 30 research papers, all in international journals. Dr. Prasad acted as reviewer of various international journal of repute, on invitation of editor.