Realization of OFCC based Transimpedance Mode Instrumentation Amplifier

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Abstract. *The paper presents an instrumentation amplifier suitable for amplifying the current source transducer signals. It provides a voltage output. It has a high gain, common mode rejection ratio and gain independent bandwidth. It uses three Operational Floating Current Conveyors (OFCCs) and four resistors. The effect of nonidealities of OFCC on performance of proposed Transimpedance Instrumentation Amplifier (TIA) is also analyzed. The proposal has been verified through SPICE simulations using CMOS based schematicThe paper presents an instrumentation amplifier suitable for amplifying the current source transducer signals. It provides a voltage output. It has a high gain, common mode rejection ratio and gain independent bandwidth. It uses three operational floating current conveyors (OFCCs) and four resistors. The effect of nonidealities of OFCC on performance of proposed Transimpedance Instrumentation Amplifier (TIA) is also analyzed. The proposal has been verified through SPICE simulations using CMOS based schematic.*

Keywords

Difference amplifier, operational floating current conveyor, transimpedance instrumentation amplifier.

1. Introduction

The Operational Floating Current Conveyor (OFCC) [1], [2] is a versatile active building block which provides flexibility to the circuit designer. It inherits the features of current conveyor and the current feedback op-amp with additional current output terminal. The availability of both high and low impedance ports at input and output provides flexibility to circuit designer. The OFCC has been used for implementing instrumentation amplifier [3], read out circuit [4], logarithmic amplifier [5], rectifier [6], filters [7], [8], [9], [10], [11], variable gain amplifier [12], and wheatstone bridge [13].

An Instrumentation Amplifier (IA) is invariably used as an input block in applications such as automotive transducers [14], industrial process control [15], [16], [17], linear position sensing [18] and bio-potential acquisition systems [19], [20], [21], [22], [23], [24] to amplify differential signals and to suppress unwanted common mode signals. Generally the operational amplifier based IA are classified as Voltage Mode IA (VMIA) whereas current mode building block based IA are referred as Current Mode IA (CMIA). Another way to classification is based on the type of input and output signal on which IA is working. The Transimpedance IA (TIA) is one among such classification where the sensed current is amplified and converted into a voltage. There is limited literature available on TIAs [25], [26], [27], and no OFCC based TIA is available in open literature to the best of author's knowledge. The details of available TIAs are comprehended in Tab. 1 according to the number and type of active and passive elements used along with the impedance presented at input and output. The following points are observed from Tab. 1:

- The opamp based topology [26] uses excessive number of resistors.
- The input impedance is low for [27] which is ideal for current sensing whereas a high input impedance is presented for [25], [26].

- The output impedance of [26], [27] is proper i.e. low in contrast to the one provided by [25].
- Extra active elements are required for impedance matching at input [25], [26] and output [25].

Tab. 1: Characteristics of available instrumentation amplifiers.

Ref. no.	Active elements	No. of resistors	Input impedance	Output impedance
[25]	2 CCII+	3	High	High
[26]	3 opamps	10	High	Low
[27]	3 OTRA	5	Low	Low

It is clear from the above discussion that only topology [27] provides proper input and output impedance levels and does not require additional circuitry for impedance matching. The aim of this paper is to present an OFCC based TIA offering proper input/output interface. It uses three active blocks and four resistors i.e. same number of active blocks as [27] and the lesser passive components than [27]. Both input and output impedances of proposed topology are low.

The paper is organized in five sections as follows: Section 2. briefly discusses the basic characteristics of OFCC and detailed description of proposed TIA structure. Section 3. describes behavior of proposed TIA in presence of nonidealities. The simulation results are presented in Section 4. followed by conclusions in Section 5.

2. Proposed Circuit

The key component of the proposed circuit is the OFCC block as shown in Fig. 1. It has two inputs (X, Y) and three outputs (W, Z+, Z-).

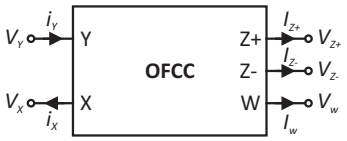

Fig. 1: OFCC block.

The port X is a low impedance current input while the port labeled Y is a high impedance voltage input. The ports Z+ and Z- are high impedance current outputs, where Z+ has positive polarity and Z- has negative polarity. The terminal marked W is the low impedance output voltage terminal. The terminal characteristics of the OFCC are characterized by the matrix given in Eq. (1):

$$\begin{bmatrix} I_Y \\ V_X \\ V_W \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & Z_t & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ I_W \\ V_{Z+} \\ V_{Z-} \end{bmatrix}, \quad (1)$$

where open loop transimpedance gain Z_t is impedance between the ports X and W and other symbols have their usual meanings.

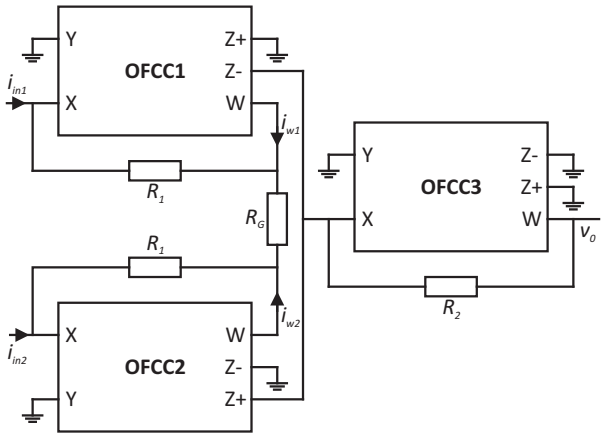

Fig. 2: Proposed OFCC based TIA.

Figure 2 shows the proposed TIA circuit. It consists of three OFCCs and four resistances. The third OFCC block in Fig. 2 is simply used as a current to voltage convertor which converts the amplified difference of currents that has been received as an input to OFCC1 and OFCC2, into voltage. The differential transimpedance gain of the instrumentation amplifier for an ideal case is computed as follows.

The currents (i_{w1}, i_{w2}) flowing out of W terminals of OFCC1 and OFCC2 respectively, are:

$$i_{w1} = -\left[i_{in1} + \frac{R_1}{R_G}(i_{in1} - i_{in2})\right], \quad (2)$$

$$i_{w2} = -\left[i_{in2} + \frac{R_1}{R_G}(i_{in2} - i_{in1})\right]. \quad (3)$$

The output voltage is computed as:

$$v_{out} = -R_2(-i_{w1} + i_{w2}) = R_2(i_{w1} - i_{w2}) = \\ = \left[(i_{in2} - i_{in1})\left(1 + \frac{2R_1}{R_G}\right)\right]. \quad (4)$$

Using Eq. (4), the differential gain (A_d) is obtained as:

$$A_d = \frac{v_{out}}{i_{in2} - i_{in1}} = \left(1 + \frac{2R_1}{R_G}\right) R_2. \quad (5)$$

3. Non Ideal Analysis

Practically, there are two kinds of OFCC non-idealities. The first type of nonidealities comes from tracking errors between port voltages and currents and their effect depend strongly on topology. As the Y terminal in proposed topology is grounded the performance is unaffected due to voltage tracking errors. Considering the current tracking error, the currents at Z+ and Z- terminals are represented as:

$$i_{Z+} = \alpha i_{w2}, \tag{6}$$

$$i_{Z-} = -\gamma i_{w1}, \tag{7}$$

where α and γ are non ideality constants.

Therefore, Eq. (4) modifies to:

$$v_{out} = \Big[(\alpha i_{in2} - \gamma i_{in1}) + \ldots \\ \ldots + \left((\alpha+\gamma)\frac{R_1}{R_G}(i_{in2} - i_{in1})\right)\Big] R_2. \tag{8}$$

Assuming $\alpha = \gamma = 1$ in Eq. (8) the differential gain (A_d) is written as:

$$A_d = \frac{v_{out}}{i_{in2} - i_{in1}} = \left(1 + \frac{2R_1}{R_G}\right) R_2. \tag{9}$$

Considering $i_{in1} = i_{in2} = i_{cm}$ in Eq. (8) for common mode operation, the common mode gain (A_{cm}) is obtained as:

$$A_{cm} = \frac{v_{out}}{i_{cm}} = (\alpha - \gamma) R_2. \tag{10}$$

Therefore the CMRR of the final circuit is:

$$\text{CMRR} = \frac{A_d}{A_{cm}} = \frac{1}{\alpha - \gamma}\left(1 + \frac{2R_1}{R_G}\right). \tag{11}$$

The second nonideality comes due to finite transimpedance gain Z_t and its frequency dependence which is approximated as $Z_t = 1/(sC_p)$ at high frequencies. The value of C_p is $(Z_{to}\ \omega_{tc})$, where Z_{to} and ω_{tc} represent open loop transimpedance gain and its cut off frequency respectively.

Considering finite Z_t, Eq. (4) is recalculated as

$$v_{out} = [\epsilon_1(s) i_{w1} - \epsilon_2(s) i_{w2}] \epsilon_3(s) R_2, \tag{12}$$

$$v_{out} = \Big[\left((i_{in2} - i_{in1})(\epsilon_2(s) - \epsilon_1(s))\frac{R_1}{R_G}\right) + \ldots \\ \ldots (\epsilon_2(s) i_{in2} - \epsilon_1(s) i_{in1})\Big] \epsilon_3(s) R_2, \tag{13}$$

where $\epsilon_i(s) = \dfrac{1}{1 + sC_{pi}R_1}$ for $i = 1, 2$ and $\epsilon_3(s) = \dfrac{1}{1 + sC_{p3}R_2}$.

Assuming $\epsilon_1(s) = \epsilon_2(s)$, differential gain is calculated as:

$$A_d = \left(1 + \frac{2R_1}{R_G}\right) R_2 \epsilon_{uc}, \tag{14}$$

where $\epsilon_{uc} = \dfrac{1}{1 + sC_{p3}R_2} \cdot \dfrac{1}{1 + sC_{p1}R_1}$ and is uncompensated error function.

Taking $i_{in1} = i_{in2} = i_{cm}$ the common mode gain is given by:

$$A_{cm} = \frac{sR_1R_2(C_{p1} - C_{p2})}{(1 + sC_{p1}R1)(1 + sC_{p2}R_1)(1 + sC_{p3}R_2)}. \tag{15}$$

Therefore the CMRR becomes:

$$\text{CMRR} = \frac{A_d}{A_{cm}} = \\ = \left(1 + \frac{R_G}{2R_1}\right)\left(\frac{2 + sR_1(C_{p1} + C_{p2})}{s(C_{p2} - C_{p1})R_G}\right). \tag{16}$$

4. Simulation Results

The CMOS based OFCC implementation [12] as shown in Fig. 3, is used for verifying functionality of proposed TIA. The transistor aspect ratios are given in Tab. 2. SPICE simulations are carried out using supply voltages of ±1.5 V and bias voltages of ±0.8 V. The simulated differential gain response of the proposed TIA is depicted in Fig. 4 for $R_G = 1$ kΩ, $R_1 = 5$ kΩ and R_2 is varied from 1 kΩ to 3 kΩ in step of 1 kΩ in order to obtain different gains. The CMRR frequency response is shown in Fig. 5. It may be noted that CMRR is independent of gain and has a bandwidth of 112 kHz. Figure 6 shows the noise spectral analysis of the proposed TIA using the same component values as those taken for obtaining differential gain response. It is observed that the output noise level has small magnitude. The power consumption of the proposed OFCC based TIA is found to be 1.5 mW.

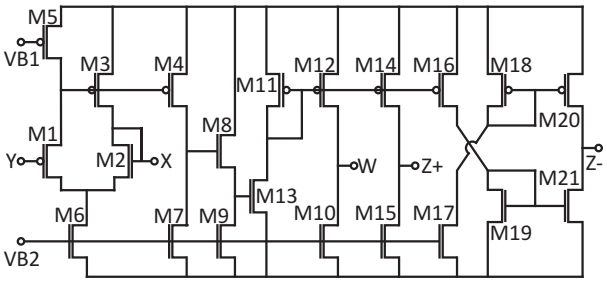

Fig. 3: CMOS schematic of OFCC [12].

5. Conclusion

In this paper, an OFCC based TIA is presented and simulated. The circuit requires only three OFCCs,

Tab. 2: Characteristics of available instrumentation amplifiers.

Transistor	W (μm)/L (μm)
M1, M2	50/1
M3, M4, M11, M12, M14, M16, M18, M20	50/2.5
M5, M7, M10, M15, M17, M19, M21	20/2.5
M6, M8	40/2.5
M9, M13	100/2.5

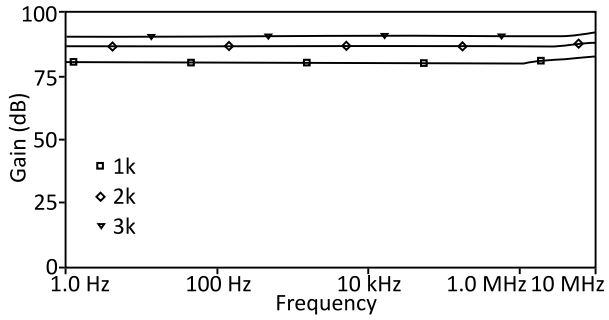

Fig. 4: Frequency response of the proposed TIA.

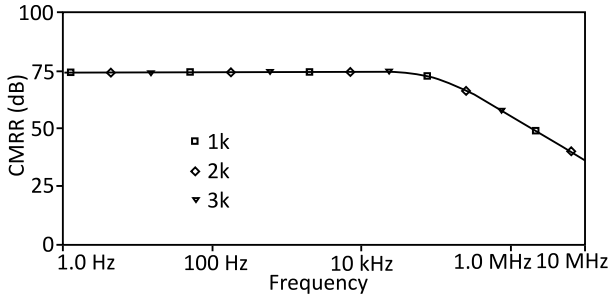

Fig. 5: CMRR of the proposed TIA for different gain values.

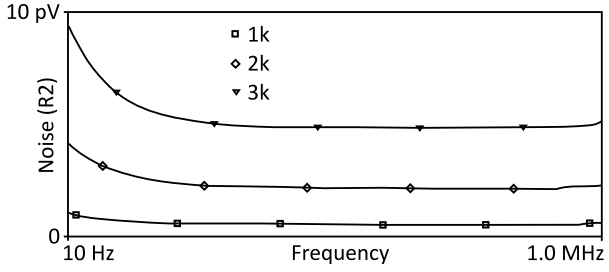

Fig. 6: Noise spectral density for different values of gain.

three feedback resistors and one grounded resistor. It works with current mode of input in order to produce an amplified output without using complex designs. The AC analysis proves the efficiency of this new circuit and the huge bandwidth it possesses. The proposed topology offers advantages over the existing operational amplifiers based TIAs, in terms of a wider bandwidth that stays independent of the finite open loop gain of the TIA. The proposed circuit also offers low component count as compared to the existing OTRA based design.

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