Ultra Low Power High Speed Domino Logic Circuit by Using FinFET Technology

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Abstract. *Scaling of the MOSFET faces greater challenge because of extreme power density due to leakage current in ultra-deep sub-micron (UDSM) technology. To overcome this situation double gate device such as FinFET is used which has excellent control over the thin silicon fins with two electrically coupled gates that mitigate shorter channel effect and exponentially reduce leakage current. The present work utilized the property of FinFET in domino logic, for high speed operation and reduction of power consumption in wide fan-in OR gate. The proposed circuit is simulated in FinFET technology by BISM4 model using HSPICE and 32nm process technology at 25 °C with C_L =1 pF and 100 MHz frequency. For 8 and 16 input OR gate in SG mode, we saved an average power of 11.5 % and 11.39 % in SFLD, 22.97 % and 18.12 % in HSD, 30.90 % and 34.57 % in CKD, respectively; while for that in LP mode, we saved an average power of 11.26 % and 15.78 % in SFLD, 19.74 % and 17.94 % in HSD, 45.23 % and 34.69 % in CKD respectively.*

Keywords

FinFET, high speed, multigate device, short channel effect.

1. Introduction

Scaling of CMOS technology is needed to improve device density and performance of the circuit. However difficulties in scaling of bulk CMOS are the prime thrust for developing a new architecture with a double gate which has higher scalability than single gate transistor, because both the gates control the fin potential over the body [1]. It is important to develop an efficient technique to overcome shorter channel effect and; power consumption as well as maintain the performance of the circuit. As shown in Fig. 1(a) and Fig. 1(b), double gate FinFET has an excellent control over thin silicon body which suppresses the shorter channel effect in sub 22 nm and beyond, and reduces the sub threshold and gate oxide leakage current [2]. FinFET technology has a wide range of characteristics. The gate terminal can be shortened to replace CMOS technology in SG mode. In Independent Gate (IG) mode, two gates work independently, for better control over the silicon fin. The fin body of a double-gate device is typically undoped or lightly doped; therefore, enhancement of carrier mobility and device variations due to doping fluctuations are reduced. To increase the ION current of the FinFET the number of fins in the FinFET can be increased, which in turn increases the current driving capability.

The paper is organized as follows: Section 2. describes the FinFET technology for DSM. Section 3. presents the literature review of high speed domino circuits. Section 4. depicts the proposed circuit for low-power and high- speed operation. Section 5. describes the simulation results and discussion using HSPICE EDA tool, and finally, the conclusion is presented in Section 6.

2. FinFET Technology

The main advantage of the FinFET structure is the fabrication of double gate using a single lithography and etch step. A gate is easily wrapped over the silicon fin. As the front and back gate have different doping profile, they operate independently according to the requirement [3]. One of the main challenges in developing FinFET over bulk-CMOS is the high current drive by reducing parasitic resistance, and the source drain region requires re-engineering.

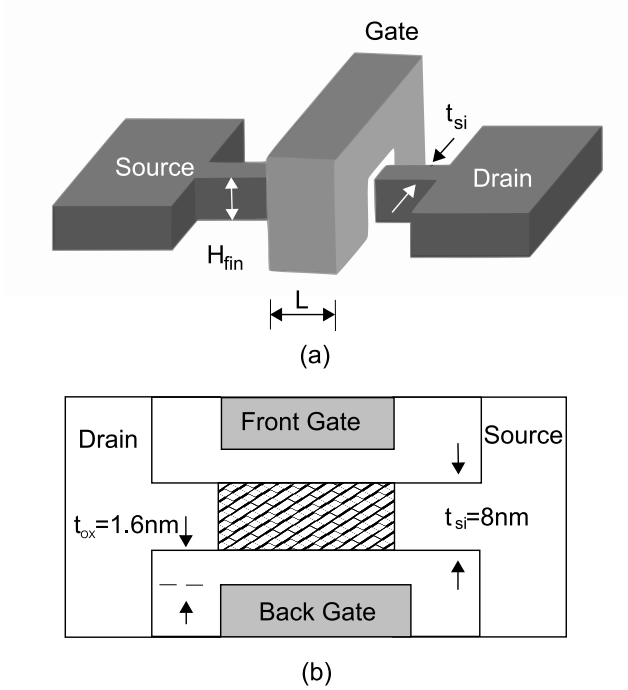

Fig. 1: (a) 3D view of a single fin of FinFET. (b) Top view of FinFET.

Owing to the vertical gate structure, the width of FinFET is quantized, and the fin height is determined by minimum transistor width (W_{min}). When two gates of a single-FinFET is tied together as shown in Fig. 1(a), W_{min} is effective channel width:

$$W_{min} = 2H_{fin} + T_{fin}, \tag{1}$$

effective channel length:

$$L_{eff} = L_{gate} + 2 \cdot L_{ext}, \tag{2}$$

where H_{fin} is the height of the fin, T_{fin} is the thickness of the silicon body, and L_{ext} is the extension of fin from gate to source or drain terminal [4]. To suppress shorter channel effect and enhance the area efficiency in FinFET, the fin thickness should be much lower than the fin height [5], [6], [7]. Table 1 shows the parameters that must be taken into consideration during the simulation of N-FinFET and P-FinFET.

Tab. 1: Device technology parameters.

Parameter	32nm N-FinFET	32 nm P-FinFET
Length of Channel (L)	32 nm	32 nm
Fin thickness(tsi)	8.6 nm	8.6 nm
Fin height($Hfin$)	40 nm	50 nm
Oxide thickness(tox)	1.4 nm	1.4 nm
Source/drain doping (N-type and P-type FinFETs)	$2 \cdot 10^{-20}$ cm^{-3}	$2 \cdot 10^{-20}$ cm^{-3}
Power Supply (Vdd)	0.8 V	0.8 V

FinFET works in three different modes according to the supply of front and back gates, namely Short Gate (SG) mode, Low Power (LP) mode and Independent gate (IG) mode as shown in Fig. 2 [8].

- SG mode - In this mode, the front and back gates are tied together with common supply voltage. The short gate is faster and has higher ION current.
- LP mode - In this mode, the front and back gates bias independently, and back gate is reverse biased for reduction of leakage current.
- IG mode - In this mode, both gates are connected to different inputs, similar to a two parallel transistors which reduces the area of the circuit.

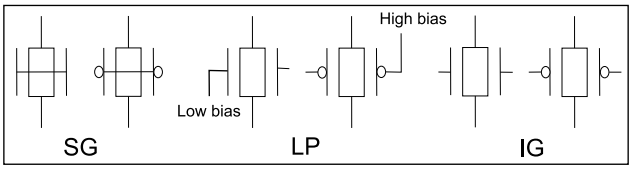

Fig. 2: Mode of operation of FinFET.

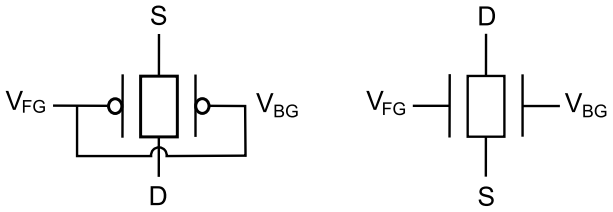

Fig. 3: SG mode (($V_{FG} = V_{BG}$)), IG mode ($V_{FG} \neq V_{BG}$) configuration of FinFET.

Biasing of the back gate of FinFET increases the ON state current (I_{ON}) and mitigates the OFF state current (I_{OFF}). I_{ON} can be defined when V_{ds}=0.8 V and V_{GS}=0.8 V, where I_{OFF} can be defined when V_{ds}=0.8 V and V_{GS}=0 V. A symbolic representation and biasing is shown in Fig. 3, FinFET has four terminals that's why we call it is 4T device. As shown in Tab. 2 and Tab. 3 following application of different biasing on the back gate of N and P FinFET, P-FinFET presented significantly lower leakage current than N-FinFET. Furthermore, it can be observed that with the increase in VBG of 4T P-FinFET from 0.6 to 1.6 V both the I_{ON} and I_{OFF} decreased, but the percentage of reduction of I_{OFF} was much higher than I_{ON} (reduction is 250x) from orignal [8].

Table 3 presents the value of I_{ON} and I_{OFF} calculated for V_{GB} from -0.6 V to 0.4 V both I_{OFF} and I_{ON} increases but increment of I_{OFF} is much higher than I_{ON} current. The simulation results indicate that the driving capability of N-FinFET was higher than that of P-FinFET when V_{BG} was reverse biased N-FinFET presented greater advantage than P-FinFET when the

back gate biased, which significantly reduced the leakage current in FinFET based digital circuit. Nevertheless P-FinFET exhibited higher driving capability and decreased the sub-threshold leakage current [9].

Tab. 2: Results of I_{OFF} and I_{ON} of 4T P-FinFET for single Fin.

V_{BG}	I_{OFF} (aA)	I_{ON} (μA)
0.6	487.5	8.27
0.8	256.2	6.67
1.0	25.15	4.35
1.2	5.57	3.02
1.4	2.11	1.45
1.6	1.06	0.94

Tab. 3: Results of I_{OFF} and I_{ON} of 4T N-FinFET for single Fin.

V_{BG}	I_{OFF} (pA)	I_{ON} (μA)
-0.6	0.067	0.81
-0.4	0.251	12.20
-0.2	2.75	14.63
0.0	37.24	16.25
0.2	867.36	19.37
0.4	22930	21.32

3. Literature Review

Domino logic circuit is used in high-speed microprocessors, where speed and high performance are the prime concern with respect to scaling of technology.

3.1. Footless Domino Logic Circuit

Footless domino logic circuit is an existing domino logic circuit. The major difference between footless and footed domino logic circuit is the footed NMOS transistor which is placed below the evaluation network in footed domino logic circuit, and which is absent in footless domino logic circuit. The circuit diagram for footless domino logic circuit is shown in Fig. 4.

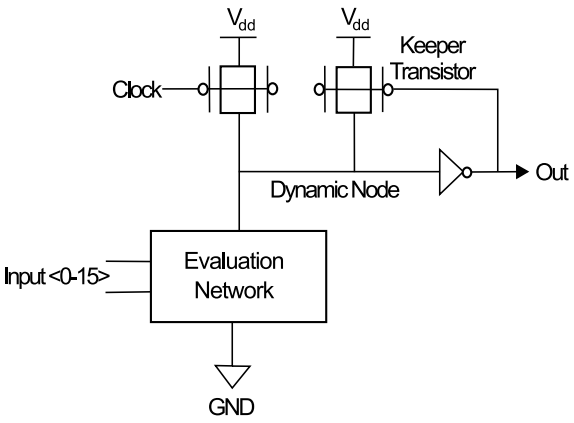

Fig. 4: Footless Domino logic circuit.

3.2. Footed Domino Logic Circuit

Footed domino logic is a general form of domino logic circuit. It is called so because of the presence of a footer transistor in the circuit. The footer transistor is generally an NMOS transistor and shows better noise and leakage tolerance because of leakage reduction due to stacking effect [6], [7]. The circuit diagram for footed domino logic circuit is shown in Fig. 5.

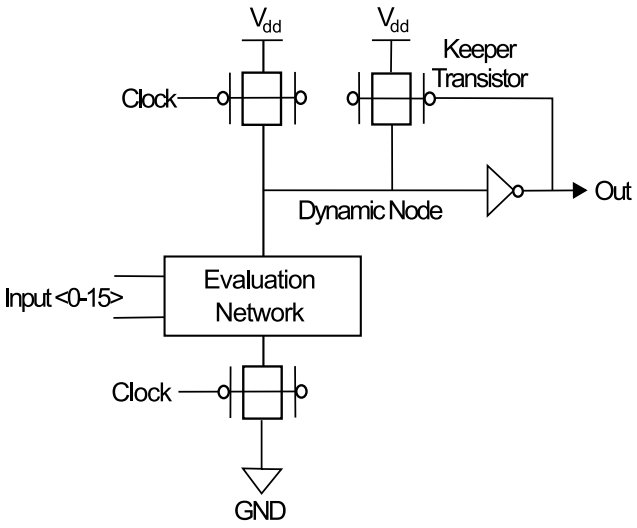

Fig. 5: Footed Domino logic circuit.

3.3. High-speed Domino Logic Circuit

In high speed domino logic circuit current is drawn through the keeper transistor and evaluation network at the beginning of the evaluation phase. Thus current can be reduced on applying a clock delay at keeper transistor [10], this leads to high speed domino logic circuit shown Fig. 6. This arrangement does not affect the leakage current in the circuit; however, the extra clock delay consumes extra area and power, which is a big drawback of the circuit [11].

In High-speed domino logic circuit when the clock becomes high, M_{n1} is still off and M_{p2} is still on. Therefore, M_{p2} turns off the keeper transistor. After some delay in inverter M_{p2} turns off. Now, if the dynamic node remains high during the evaluation phase, NMOS is turned on which turns on the keeper transistor. Hence, at the beginning of the evaluation phase the dynamic node is afloat, and hence in the absence of keeper transistor, the evaluation node may be discharged for any noise at the input section. Furthermore the voltage at the gate of the keeper transistor is V_{DD}-V_{tMn1}, which could provide a DC current flow through the PMOS keeper transistor and the NMOS network.

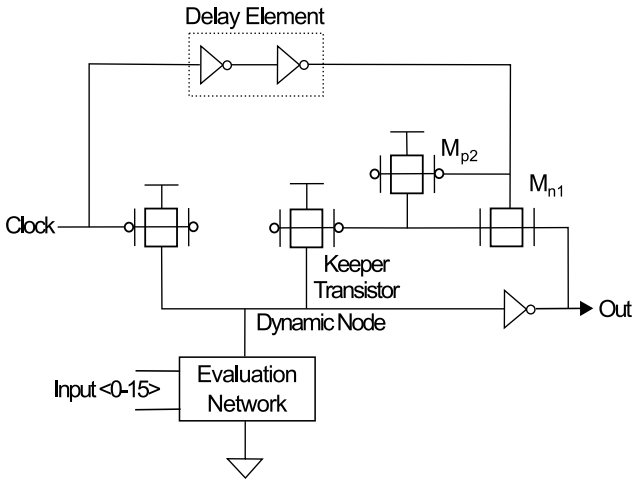

Fig. 6: High-speed Domino logic circuit.

3.4. Conditional Keeper Domino Logic Circuit

In most of the high-speed timing performance schemes, input signals of the dynamic logic gates are ready just before or close to the start of the evaluation phase. In such situations the maximum time slot for any output transition is only a fraction of the total evaluation time, which takes half time period of 50 % duty cycle clock. Therefore leakage and noise exist unnecessarily for a long time at the output of the gate [12]. In the conventional circuit a standard keeper transistor is used, which is turned on unconditionally at the start of the evaluation phase, and takes down the performance of the dynamic logic gate as shown in Fig. 7.

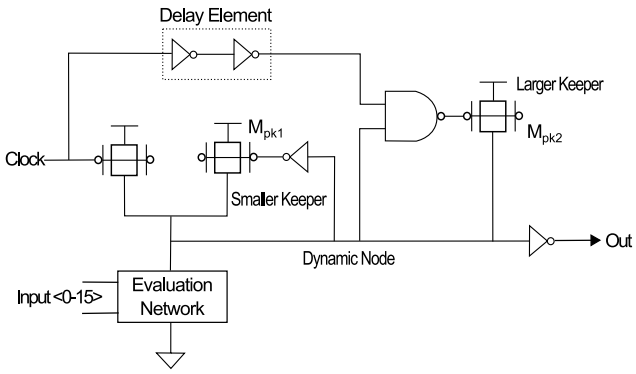

Fig. 7: Conditional keeper Domino logic circuit.

The conditional keeper domino logic contains two PMOS keeper transistor circuits with variable strength. One keeper transistor has lower strength, while the other has higher strength [13]. When the dynamic node is at high voltage M_{kp1} turns on to avoid the voltage drop at the dynamic node. If the dynamic node is still high, then after a certain amount of delay, during the evaluation phase, the output of NAND gate becomes low, thus turning on M_{kp2}. It must be noted that M_{kp1} is responsible for maintaining the state of the dynamic node, during the beginning of the evaluation phase, while M_{kp2} is responsible for it for the rest of the evaluation phase. Another type of domino circuit developed from CMOS technology is the diode footed domino logic (DFD), which reduces power consumption and delay of the circuit by inserting the mirror circuit below the evaluation network. By inserting the mirror, the path of discharge of the dynamic node increases as shown in Fig. 8. Thus, the dynamic node discharges slowly and removes the contention current between the dynamic node and evaluation network, improving the performance and robustness of the circuit [6], [14], [15].

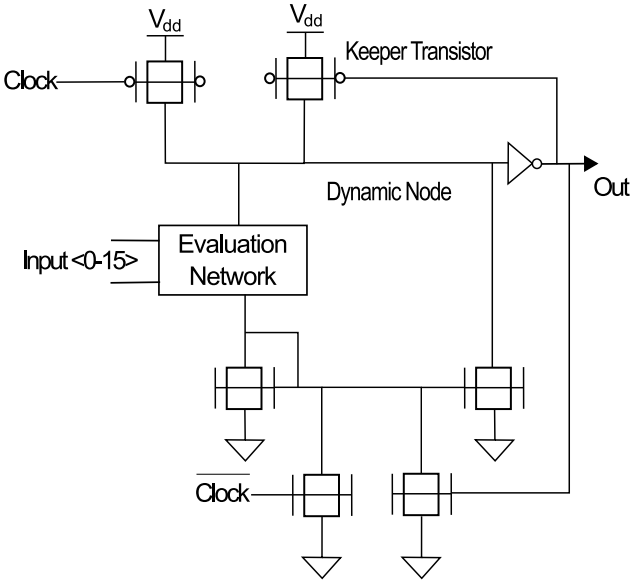

Fig. 8: Diode footed Domino logic.

In Leakage Controlled Replica (LCR) modification is achieved over the keeper transistor by inserting a mirror circuit in parallel to the keeper transistor, which mitigates power consumption and area of the circuit, as shown in Fig. 9 [15]. This circuit is helpful in improving the noise immunity of the circuit in evaluation phase [16], [17].

Several studies have been conducted on domino logic to achieve faster operation of the circuit and reduction of power consumption. In the present study, a new current comparison of domino (CCD) circuit has been proposed which enhances the performance of the circuit; and improves the UNG of the circuit by maintaining its robustness [18]. Thus, our proposed circuit is a new class of domino circuit with lower power and high speed with constant delay of the circuit.

A recent addition to the different type of domino circuit is voltage comparison circuit which has been developed, with domino circuit for wide fan in gate. In present study, the voltage swing of the dynamic node has been reduced by decreasing the power consumption

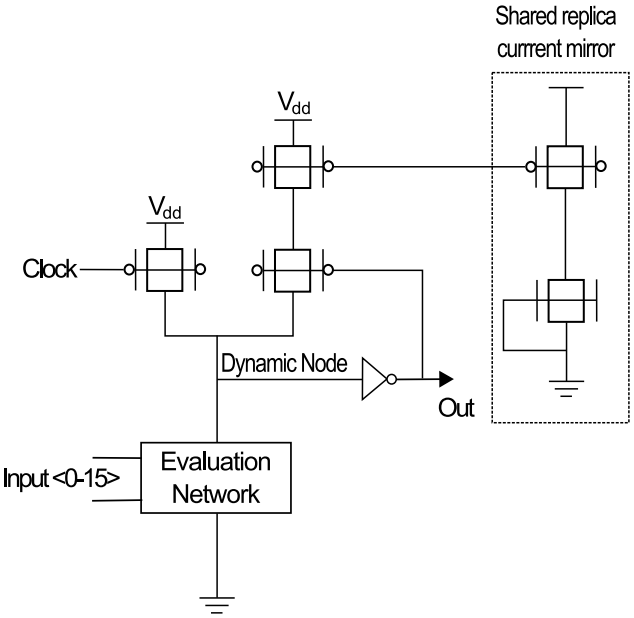

Fig. 9: Leakage controlled replica.

by heavy swing of the switching capacitance [14]. All simulations were performed with 90 nm technology for 64-bit OR gate, which saved 36 % power and provided 2.32x noise immunity.

4. Proposed Circuit

In proposed circuit we have modified the keeper transistor. For the reduction of contention between the keeper and evaluation network, we split the keeper transistor into two for proper strength. Furthermore, by sizing the keeper transistor we reduced the power and delay of the domino circuit.

As shown in Fig. 10 we use Ultra Low Power Stacked Design (ULSD) which is a combination of PMOS and NMOS. ULSD achieves higher reduction of leakage current, when compared with other standard logic.

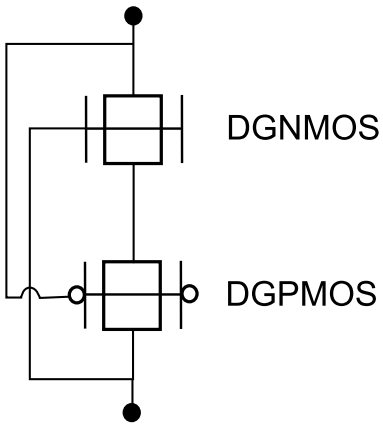

Fig. 10: Ultra low power stacked design.

Our proposed circuit works in two phases. In first phase when the clock pulse is 0, the circuit remains in pre-charge phase, which charges the dynamic node and the output of the logic is always 0. During second phase the circuit enters the evaluation phase, the clock pulse becomes 1, and if one of the inputs of the OR gate is active then the dynamic node is discharged. Subsequently transistor MN1is is turned ON, dynamic node easily discharges through MN1, and also MN2 transistor is turned ON as gate voltage is high on transistor MN2, dynamic node discharges through evaluation and MN1 transistor slowly due to gate delays, hence two invertors are connected in series at a gate of MN1 to provide delay in making MN1 ON. This will save power of the circuit. As shown in Fig. 11 transistors MN3 and MP4 try to discharge the dynamic node towards the ground. The main function of this transistor is to draw the contention current of the PMOS keeper, which also speeds up the discharging process of the capacitor at the dynamic node. At the beginning of the pre-charge phase the pre-charge transistor is in active mode and the voltage at the dynamic node will be at 0 V. This 0 V is fed to the inverter as an input which makes the output of the inverter as V_{DD}. The modification of the keeper transistor helps in discharging the dynamic node, and the charge stored over the dynamic node floats, when all the inputs of the OR gate are disconnected. By providing a proper stacking with the help of ULSD transistor, which helps in improving the UNG of the circuit, power consumption is reduced and speed is enhanced by using FinFET technology in different mode. The transistors MN3, MP4 and MN2 are arranged as stack transistors and provide a stacked effect in pull down network, and by reducing the leakage current simultaneously a proper logic level is achieved as shown in Fig. 12.

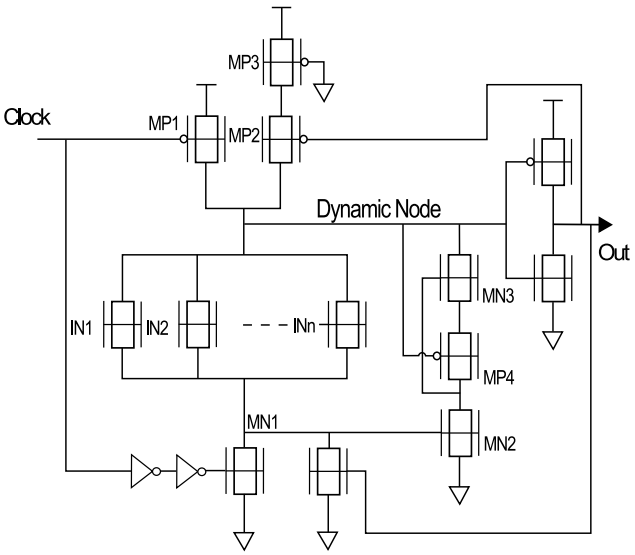

Fig. 11: Proposed circuit.

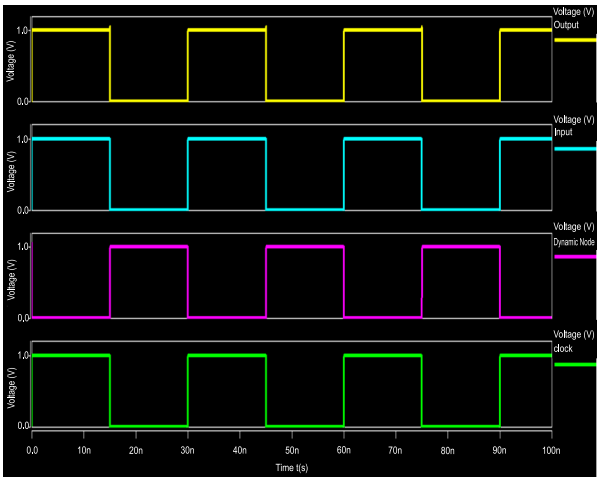

Fig. 12: Transient characteristics of the proposed two input Domino OR using HSPICE in FinFET technology.

5. Simulation Results and Discussion

The simulation results were obtained by using BISM4, HSPICE model at 32 nm technology, by using Predictive Technology Model (PTM). In FinFET technology, the circuit is simulated in SG and LP modes with 0.8 V supply at 100 MHz frequency. All simulations were performed at room temperature of 25 °C for all the existing and proposed circuits. The I_{SUB} and I_{GATE} leakage currents vary with VDD and temperature in a 32-nm CMOS and FinFET technology. At room temperature, I_{GATE} was noted to be 2.4 times higher than I_{SUB}, with output capacitance, $I_L = 1$ pF for 8 and 16 input OR gate as shown in Tab. 4 and Tab. 5. Figure 11 and Fig. 12 present the comparison of COMS and SP, LP mode of FinFET technology. The FinFET technology mitigates, the average power in SG and LP modes. The keeper ratio (K) is defined as the ratio of the current drivability of the keeper transistor to that of the evaluation transistor,

$$K = \frac{\mu_p \left(\frac{W}{L}\right) keeper\ \ transistor}{\mu_n \left(\frac{W}{L}\right) evaluation\ \ transistor}, \qquad (3)$$

where W and L denote the transistor size, and μ_n, μ_p are the mobility of electron and hole respectively [2]. The simulation was performed by setting Mkeeper (W/L) = 16/32 n, PMOS (W/L) =128/32 n, NMOS (W/L) = 64/32 n and C_L=1 pF for fair comparison of the results.

Table 4 and Tab. 5 show the comparison of the average power, delay and PDP using FinFET technology. It can be observed that the proposed FinFET based circuit shaved maximum power, with an average power 11.25 % and 11.39 % in FLD, 18.76 % and 18.12 % in HSD, 30.90 % and 34.57 % in CKD for 8 input OR gate in SG and LP modes of the FinFET technology. Furthermore, the saving of the delay was 24.31 % and 13.18 % in FLD, 53.19 % and 46.79 % in FDL, 20.60 % and 10.34 % in HSD, 29.34 % and 24.99 % in CKD for 8 input OR gate in SG and LP mode of FinFET technology respectively. The saving of the average power of the proposed circuit was 15.60 % and 14.86 % in DFD and 13.93 % and 17.64 % in LCR for 8 and 16 input OR gate respectively.

Subsequently, the Unit Noise Gain (UNG) of the circuit was calculated (Tab. 6) by applying narrow width of pulse having 50 ps and measuring the amplitude at the output of the circuit. If the amplitude obtained at the input and output was the same, we considered as the UNG of the circuit. UNG can be defined as the amplitude of the input noise that causes the same amplitude of noise at the output:

$$\text{UNG} = \{V_{noise}; V_{noise} = V_{out}\}. \qquad (4)$$

UNG is inversely proportional to the leakage current. As shown in Tab. 6 the proposed circuit presented higher UNG than the existing circuit, which was, 0.382 in SG mode and 0.532 in LP mode. However, the UNG was lower in LP mode due to reverse biase of the pull down network of the circuit which reduced the leakage power of the circuit.

In the standby power, the evaluation network of the circuit is turned off and the precharge transistor comes into the existence. Subsequently, the PMOS of the transistor turns on and charges the dynamic node. As dynamic node does not acquire any path to discharge the voltage, the volatge is floats over thedynamic node

Tab. 4: Calculation of average power, delay and PDP for 8 input OR gate in SG and LP mode using FinFET technology.

	Average Power (μW)		Delay (pS)		PDP (aJ)	
	SG Mode	**LP Mode**	**SG Mode**	**LP Mode**	**SG Mode**	**LP Mode**
FLD	0.1200	0.0316	9.635	8.243	1.156	0.2608
FDL	0.0776	0.0242	15.58	13.45	0.492	0.0119
HSD	0.1306	0.0342	9.185	7.982	1.199	0.3987
CKD	0.1537	0.0428	10.32	9.541	1.586	0.4083
DFD	0.1256	0.0345	9.723	8.934	1.215	0.2997
LCR	0.1234	0.0324	9.854	9.251	1.215	0.2997
Proposed Circuit	0.1062	0.0280	7.292	7.156	0.774	0.0216

Tab. 5: Calculation of average power, delay and PDP for 16 input OR gate in SG and LP mode using FinFET technology.

	Average Power (μW)		Delay (pS)		PDP (aJ)	
	SG Mode	LP Mode	SG Mode	LP Mode	SG Mode	LP Mode
FLD	0.142	0.038	10.235	9.317	1.461	0.364
FDL	0.096	0.027	19.94	15.34	1.914	0.426
HSD	0.157	0.039	10.02	9.254	1.460	0.362
CKD	0.183	0.049	11.01	10.25	1.883	0.506
DFD	0.148	0.041	10.94	9.89	1.619	0.066
LCR	0.153	0.045	11.03	10.32	1.728	0.464
Proposed Circuit	0.126	0.032	8.384	8.945	1.058	0.0273

Tab. 6: Calculation of UNG, standby power and evaluation delay for 8 input OR gate in SG and LP mode using FinFET technology.

	UNG		Standby Power (μW)		Evaluation Delay (ps)	
	SG Mode	LP Mode	SG Mode	LP Mode	SG Mode	LP Mode
FLD	0.293	0.282	0.091	0.014	6.333	5.124
FDL	0.352	0.337	0.046	0.010	12.05	11.324
HSD	0.314	0.289	0.105	0.018	6.461	5.0129
CKD	0.325	0.294	0.127	0.025	7.031	5.1455
DFD	0.316	0.310	0.103	0.024	6.217	5.935
LCR	0.338	0.298	0.093	0.021	6.753	6.255
Proposed Circuit	0.382	0.352	0.080	0.009	5.193	4.615

and this power is known as standby power. As shown in Tab. 6, the proposed circuit, achieved maximum saving of standby power with 37.0 % and 96.4 % CKD in SG and LP modes of FinFET technology, respectively. It can be noted that the saving of standby power was very high in LP mode when compared with that in SG mode due to reverse bias of the pull down network which increased the threshold voltage of the transistor and reduced the leakage power of the circuit.

Furthermore, calculation of the Evalation delay revealed that the proposed circuit saved maximum delay (Tab. 6), which increased the speed of the circuit. When CLK=1 the circuit entered the evaluation phase, the dynamic node tried to discharge through the evaluation network and the current flowed from minimum resistance path. The time taken by the dynamic node to discharge is known as evaluation delay. The proposed circuit presented improved evaluation delay when compared with other existing circuits in low-power circuit design.

5.1. Power Analysis

If there are many pulses, then buffer frequently turns on and off. The power consumption of the logic circuit in conventional circuit can be given as follows.

$$P_{avg} = K \cdot {V_{DD}}^2 \cdot C_{dyn} + r \cdot f \cdot V_{DD} \cdot V_{noise} \cdot C_{dyn}, \quad (5)$$

where

$$r = \frac{T_{on}}{(T_{on} + T_{off})}. \quad (6)$$

T_{on} is the time when the input logic is on, T_{off} is the time when he input logic is off, K is the probability of the state that the input logic changes in a unit time, C_{dyn} is the capacitor in dynamic node and V_{noise} is the pulse in dynamic node.

Figure 13 shows the comparison of CMOS and FinFET Technology, from the Fig. 12. We observe that power consumption of CMOS technology is huge in comparison with SG and LP mode of FinFET technology this is because, FinFET technology has three dimensional structure, where current flows vertically, where CMOS is a planar device, where current flows horizontally with respect to the channel. In Fig. 14 it is observe that FinFET technique have lower delay than CMOS and proposed circuit save power and delay with other existing circuit for 8 input domino OR gate.

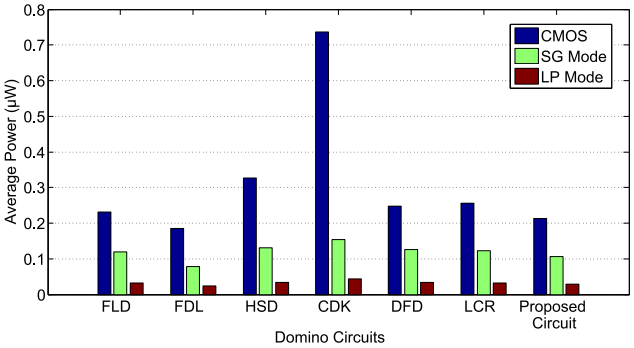

Fig. 13: Average power comparison CMOS and FinFET for 8 inputs OR Gate (SG, LP modes).

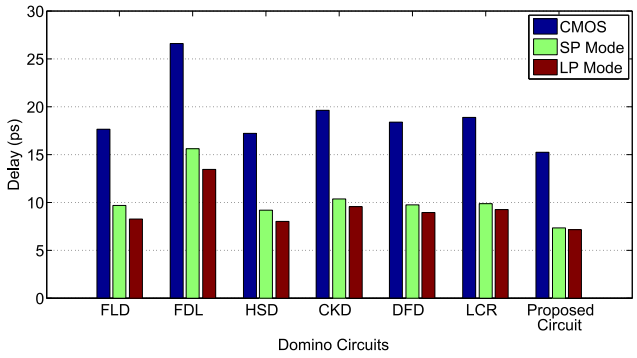

Fig. 14: Delay comparison CMOS and FinFET for 8 inputs OR Gate (SG, LP modes).

6. Conclusion

In this paper we discussed about FinFET and recent domino circuits design to enlighten our knowledge. Here in UDSM technology FinFET based domino logic circuit is proposed. Various existing domino logic circuits along with our proposed circuit were simulated we observed that FinFET based domino circuit is faster and consume less power than the bulk CMOS device. The new circuit technique was found to reduce the power consumption up to 32 % and 38 % without sacrificing the speed of the circuit. The proposed technique can be applied on high performance, low power applications, where leakage is a major concern such as microprocessors, memory units, and other portable devices. Thus, FinFET technology can completely replace CMOS by maintaining the law of technology scaling. Moreover, FinFET technology reduces the size of the transistor by up to 10 nm, the process parameters such as voltage and temperature can be varied with the scaling of technology. In future, we can implement next-generation domino circuit using carbon nanotubes, which has advantages such as low power, high speed and smaller area of 10 nm - 7 nm.

References

[1] WONG, P. H.-S., D. J. FRANK., P. M. SOLOMON, C. H. J. WANN and J. J. WELSER. Nanoscale CMOS. *Proceedings of the IEEE*. 1999, vol. 87, iss. 4, pp. 537–570. ISSN 0018-9219. DOI: 10.1109/5.752515.

[2] NOWAK, E. J., I. ALLER, T. LUDWIG, K. KIM, R. V. JOSHI, C.-T. CHUANG, K. BERNSTEIN and R. PURI. Turning silicon on its edge [double gate CMOS/FinFET technology]. *IEEE Circuits and Devices Magazine*. 2004, vol. 20, iss. 1, pp. 20–31. ISSN 8755-3996. DOI: 10.1109/MCD.2004.1263404.

[3] TAWFIK, S. A. and V. KURSUN. FinFET domino logic with independent gate keepers. *Microelectronics Journal*. 2009, vol. 40, iss. 11, pp. 1531–1540. ISSN 0026-2692. DOI: 10.1016/j.mejo.2009.01.011.

[4] HISAMOTO, D., W.-C. LEE, J. KEDZIERSKI, H. TAKEUCHI, K. ASANO, C. KUO, E. ANDERSON, T.-J. KING, J. BOKOR and C. HU. FinFET - A Self-Aligned Double-Gate MOSFET Scalable to 20 nm. *IEEE Transactions on Electron Devices*. 2000, vol. 47, iss. 12, pp. 2320–2325. ISSN 0018-9383. DOI: 10.1109/16.887014.

[5] RASOULI, S. H., H. F. DADGOUR, K. ENDO, H. KOIKE and K. BANERJEE. Design Optimization of FinFET Domino Logic Considering the Width Quantization Property. *IEEE Transactions on Electron Devices*. 2010, vol. 57, iss. 11, pp. 2934–2943. ISSN 0018-9383. DOI: 10.1109/TED.2010.2076374.

[6] MAHMOODI-MEIMAND, H. and K. ROY. Diode-footed domino: a leakage-tolerant high fan-in dynamic circuit design style. *IEEE Transactions on Circuits and Systems I: Regular Papers*. 2004, vol. 51, iss. 3, pp. 495–503. ISSN 1549-8328. DOI: 10.1109/TCSI.2004.823665.

[7] GONG, N., B. GUO, J. LOU and J. WANG. Analysis and optimization of leakage current characteristics in sub-65 nm dual V_t footed domino circuits. *Microelectronics Journal*. 2008, vol. 39, iss. 9, pp. 1149–1155. ISSN 0026-2692. DOI: 10.1016/j.mejo.2008.01.028.

[8] NAN, L., C. XIAOXIN, L. KAI, M. KAISHENG, W. DI, W. WEI, L. RUI and Y. DUNSHAN. Low power adiabatic logic based on FinFETs. *Science China Information Sciences*. 2014, vol. 57, iss. 2, pp. 1–13. ISSN 1869-1919. DOI: 10.1007/s11432-013-4902-x.

[9] MISHRA, P., A. MUTTREJA and N. K. JHA. FinFET Circuit Design. *Nanoelectronic Circuit Design*. New York: Springer, 2011, pp. 23–54. ISBN 978-1-4419-7444-0. DOI: 10.1007/978-1-4419-7609-3_2.

[10] RAKESH, G. D. J. and N. BHAT. A low power, process invariant keeper design for High speed dynamic logic circuits. In: *International Symposium on Circuits and Systems*. Seattle: IEEE, 2008, pp. 1668–1671. ISBN 978-1-4244-1684-4. DOI: 10.1109/ISCAS.2008.4541756.

[11] ALLAM, M. W., M. H. ANIS and M. I. ELMASRY. High-speed dynamic logic styles for scaled-down CMOS and MTCMOS technologies.

In: *Proceedings of the 2000 International Symposium on Low Power Electronics and Design*. Rapallo: IEEE, 2000, pp. 155–160. ISBN 1-58113-190-9. DOI: 10.1109/LPE.2000.155270.

[12] FRUSTACI, F., P. CORSONELLO, S. PERRI, and G. COCORULLO. High-performance noise-tolerant circuit techniques for CMOS dynamic logic. *IET - Circuits, Devices & Systems*. 2008, vol. 2, iss. 6, pp. 537–548. ISSN 1751-858X. DOI: 10.1049/iet-cds:20080070.

[13] PEIRAVI, A. and M. ASYAEI. Robust low leakage controlled keeper by current-comparison domino for wide fan-in gates. *Integration the VLSI Journal*. 2012, vol. 45, iss. 1, pp. 22–32. ISSN 0167-9260. DOI: 10.1016/j.vlsi.2011.07.002.

[14] ASYAEI, M. A new leakage-tolerant domino circuit using voltage-comparison for wide fan-in gates in deep sub-micron technology. *Integration the VLSI Journal*. 2015, vol. 51, iss. 1, pp. 61–71. ISSN 0167-9260. DOI: 10.1016/j.vlsi.2015.06.003.

[15] ROY, T., I. U. ZAMAN and M. S. ISLAM. Novel FinFET domino logic circuit using dual keepers. In: *International Conference on Electrical Engineering and Information & Communication technology*. Dhaka: IEEE, 2014, pp. 219–224. ISBN 978-1-4799-4820-8. DOI: 10.1109/ICEEICT.2014.6919057.

[16] AHN, S. Y. and K. CHO. Small-swing domino logic based on twist-connected transistors. *Electronics Letters*. 2014, vol. 50, iss. 15, pp. 1054–1056. ISSN 0013-5194. DOI: 10.1049/el.2014.0471.

[17] XIA, Z., M. HARIYAMA and M. KAMEYAMA. Asynchronous Domino Logic Pipeline Design Based on Constructed Critical Data Path. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*. 2014, vol. 23, iss. 4, pp. 619–630. ISSN 1063-8210. DOI: 10.1109/TVLSI.2014.2314685.

[18] PEIRAVI, A. and M. ASYAEI. Current-Comparison-Based Domino: New Low-Leakage High-Speed Domino Circuit for Wide Fan-In Gates. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*. 2013, vol. 21, iss. 5, pp. 934–943. ISSN 1063-8210. DOI: 10.1109/TVLSI.2012.2202408.

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