# Operational Transresistance Amplifier Based PID Controller

*Rajeshwari PANDEY*[1], *Neeta PANDEY*[1], *Saurabh CHITRANSHI*[1], *Sajal K. PAUL*[2]

[1]Department of Electronics and Communication Engineering, Shahbad Daulatpur, Delhi Technological University, Bawana Road, DL - 42, Delhi, India
[2]Department of Electronics Engineering, Indian School of Mines, Dhanbad – 826004, Jharkhand, India

rpandey@dce.ac.in, neetapandey@dce.ac.in, chitransi.dtu@gmail.com, sajalkpaul@rediffmail.com

DOI: 10.15598/aeee.v13i2.1164

***Abstract.*** *This paper presents Operational transresistance amplifier (OTRA) based proportional-integral-derivative (PID) controller with independent electronic tuning of proportional, integral, and derivative constants. The configuration can be made fully integrated by implementing the resistors using matched transistors operating in the linear region. Theoretical propositions are verified through SPICE simulations using 0.18 µm process parameters from MOSIS (AGILENT). In order to demonstrate the workability of the proposed controller, its effect on step response of an OTRA based second order system is analyzed and presented.*

## Keywords

***OTRA, PD, PI, PID, second order system.***

## 1. Introduction

A controller monitors and modifies the operational conditions of a given dynamical system. These operational conditions are referred to as measured output variables and can be modified by adjusting certain input variables. The controller calculates the difference between a measured output variable and a desired set point as an error value and attempts to minimize the error by adjusting the process control inputs. In general controllers can be classified as (i) conventional and (ii) non-conventional controllers. For conventional controllers, such as PID controller, a prior knowledge of the mathematical model of the process to be controlled is required in order to design a controller whereas for unconventional controllers this information is generally not needed. P, PI, PD, and PID are few typical examples of conventional controllers, and neuro-fuzzy controllers are representatives of the unconventional class. The controllers based on proportional-integral-derivative (PID) algorithm are most popularly used in the process industries. These are used to control various processes satisfactorily with proper tuning of controller parameters. Generally operational amplifiers (OPAMPs) are used to design classical analog controllers [1], [2]. However the OPAMPs, being voltage mode circuit, have their limitations of constant gain bandwidth product ($f_T$) and low slew rate. This inaccurately limits the speed of the OPAMP-based controllers and might influence the dynamics of the system [3]. It is well known that inherent wide bandwidth almost independent of closed loop gain; greater linearity and large dynamic range are the key performance features of current mode technique [4]. Therefore, the current mode building blocks would be a good alternative of OPAMP for designing the analog controllers. Literature survey reveals that number of current mode circuits have been reported relating to PID controllers [3], [5], [6], [7], [8]. Operational transconductance amplifier (OTA) based controllers are proposed in [5] and are electronically tunable. However, these provide voltage output at high impedance making a buffer necessary to drive the voltage input circuits. The current difference buffered amplifier (CDBA) based PID controller presented in [6] uses an excessively large number of active and passive components. References [3], [7], [8] present current conveyor II (CCII) based PID controllers. Two different structures are proposed for voltage and current outputs respectively in [7], [8] whereas [3] presents only voltage output configuration. All the CCII based voltage mode designs deliver output voltage at high impedance and are thus not suitable for driving voltage input circuits. The OTRA is yet another, relatively recently proposed current mode build-

**Tab. 1:** Comparison of proposed work with existing literature.

| Reference | Active block used | No. of Active block used | Passive elements | Outputs | Output Impedance | Electronic Tunability |
|---|---|---|---|---|---|---|
| [1] | Opamp | 4 | 8R, 2C | Voltage | Low | No |
| [3] | Opamp | 1 | 3R, 3C | Voltage | Low | No |
| [5] | OTA | 8 | 2C | Voltage | High | Yes |
| [6] | CDBA | 4 | 8R, 2C | Voltage | Low | No |
| [7] | CCII | 3 | 4R, 2C | Fig. 2: Current<br>Fig. 3: Voltage | High<br>High | No<br>No |
| [8] | CCII | 3 | 4R, 2C | Fig. 2: Current<br>Fig. 3: Voltage | High<br>High | No<br>No |
| Proposed work | OTRA | 2 | 4R, 3C | Voltage | Low | Yes |

ing block which is a high gain current input, voltage output amplifier [9].

Being a current processing analog building block, it inherits the advantages of the current mode technique. Additionally it is also free from the effects of parasitic capacitances at the input due to virtually internally grounded input terminals [10] and hence the non-ideality problem is less in circuits implemented using OTRA. Therefore, this paper aims at presenting OTRA based PID controller with orthogonally tunable proportional, integral and derivative constants. The proposed circuit can be made fully integrated by implementing the resistors using MOS transistors operating in the non-saturation region. This also facilitates electronic tuning of the controller parameters. A detailed comparison of the PID controllers available in the literature is given in Tab. 1 which suggests that OTRA based structure is the most suitable choice for voltage mode operation.

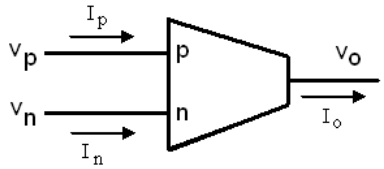



**Fig. 1:** The OTRA circuit symbol.

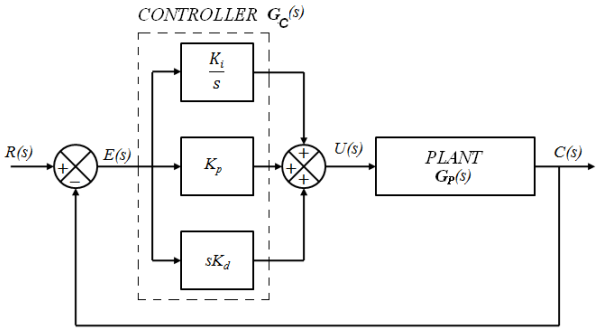



**Fig. 2:** Block diagram of a closed loop system with PID controller.

## 2. Proposed Circuits

The OTRA is a three terminal device shown symbolically in Fig. 1 and its port relations can be characterized by the matrix as follows:

$$\begin{bmatrix} V_p \\ V_n \\ V_0 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ I_0 \end{bmatrix}, \qquad (1)$$

where $R_m$ is the transresistance gain of the OTRA. For ideal operations, $R_m$ approaches infinity and forces the input currents to be equal. Thus, OTRA must be used in a negative feedback configuration [9], [10].

### 2.1. PID Controller

In a given system the proportional action improves the rise time of the system, the integral action improves the steady-state error whereas the derivative action improves the degree of stability. So, none alone is capable of achieving the complete improvement in system performance [11]. This leads to the motivation of using a PID controller so that the best features of each of the PI and PD controllers are utilized. In a PID controller as shown in Fig. 2 the proportional, integral and the derivative of the error signal $E(s)$ are summed up to calculate the output actuating signal $U(s)$ of the controller which controls the plant's $(G_P(s))$ function. Thus, the transfer function $G_C(s)$ of the PID controller can be written as:

$$G_C(s) = K_p + \frac{K_i}{s} + sK_d, \qquad (2)$$

where $K_p$, $K_i$, and $K_d$ are the proportional, integral and derivative constants respectively.

In the following subsection first an OTRA based PI controller is introduced followed by a PD controller. By combining these two controllers, the proposed PID controller is designed.

### 1) Proposed PI Controller

The PI controller comprises of proportional and integral actions and can be derived from the controller block of Fig. 2 if the derivative block is excluded. The transfer function $G_{PI}(s)$, of the PI controller so obtained is given by:

$$G_{PI}(s) = K_p + \frac{K_i}{s}. \tag{3}$$

The OTRA based proposed PI controller is shown in Fig. 3.

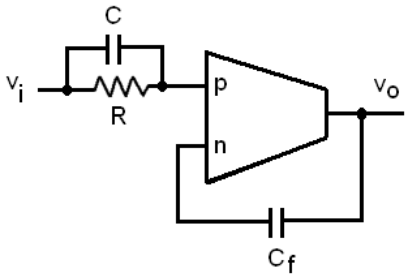



**Fig. 3:** Proposed PI controller.

Using routine analysis the voltage transfer function of the proposed controller can be as expressed as:

$$G_{PI}(s) = \frac{V_o}{V_i} = \frac{C}{C_f} + \frac{1}{s \cdot C_f \cdot R}. \tag{4}$$

From Eq. (4) the controller parameters can be computed as:

$$K_p = \frac{C}{C_f},\ K_i = \frac{1}{R \cdot C_f}. \tag{5}$$

It is clear from Eq. (5) that $K_p$ value can be adjusted independently of $K_i$ by varying $C$, and $K_i$ can be independently controlled by varying $R$.

### 2) Proposed PD Controller

A PD controller can be obtained if proportional and derivative actions only are taken into consideration in Fig. 2. Transfer function of a PD Controller $G_{PD}(s)$, can be represented as:

$$G_{PD}(s) = K_p + s \cdot K_d. \tag{6}$$

Figure 4 shows the proposed PD controller circuit and the transfer function of this controller is obtained as:

$$G_{PD}(s) = \frac{V_o}{V_i} = \frac{R_f}{R} + s \cdot C \cdot R. \tag{7}$$

The controller parameters can be expressed as:

$$K_p = \frac{R_f}{R},\ K_d = s \cdot C \cdot R. \tag{8}$$

From Eq. (8) it is clear that by varying $R$, $K_p$ value can be adjusted independently of $K_d$ and by simultaneous variation of $R_f$ and $R$ such that $R_f/R$ remains constant, $K_d$ can be independently controlled.

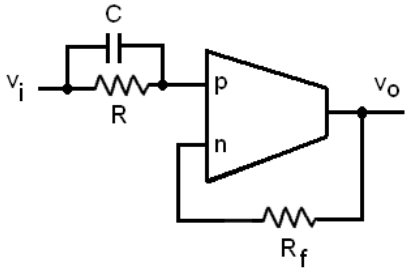



**Fig. 4:** Proposed PD controller.

### 3) Proposed PID Controller

The proposed OTRA based PID Controller can be derived by combining the proposed PI and PD controllers and is shown in Fig. 5. The routine analysis of this circuit gives the transfer function of the controller as:

$$G_{PID}(s) = \frac{V_o}{V_i} == \left(\frac{R_4}{R_2} + \frac{R_4 \cdot C_1}{R_3 \cdot C_1}\right) + \frac{R_4}{s \cdot C_3 \cdot R_1 \cdot R_3} + s \cdot C_2 \cdot R_4, \tag{9}$$

from Eq. (9) the controller parameters can be identified as:

$$K_p = \frac{R_4 \cdot C_1}{R_3 \cdot C_3} + \frac{R_4}{R_2},\quad K_i = \frac{R_4}{C_3 \cdot R_1 \cdot R_3},\quad K_d = C_2 \cdot R_4. \tag{10}$$

It is observed from Eq. (10) that the $K_p$ value can be adjusted independently by varying $R_2$, independent tuning of $K_i$ is possible through $R_1$ variation whereas $K_d$ can be controlled independently by simultaneous variation of $R_2$, $R_3$ and $R_4$, such that $R_4/R_2$ and $R_4/R_3$ remain constant.

## 2.2. MOS-C Implementation and Electronic Tuning of the Proposed Controllers

It is well known that the linear passive resistor consumes a large chip area as compared to the linear resistor implementation using transistors operating in the non-saturation region. The differential input of OTRA

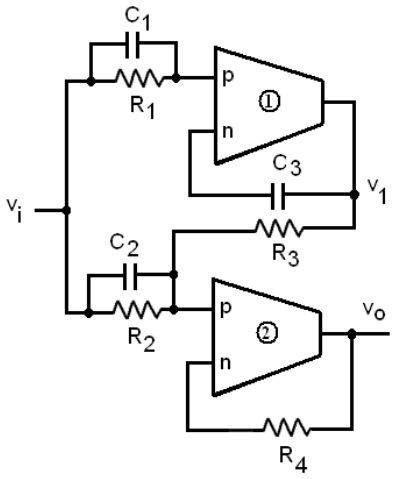



**Fig. 5:** Proposed PID controller.

allows the resistors connected to the input terminals of OTRA to be implemented using MOS transistors with complete non-linearity cancelation [10]. Figure 6(a) shows a typical MOS implementation of resistance connected between negative input and output terminals of OTRA. The resistance value may be adjusted by appropriate choice of gate voltages thereby making controller parameters electronically tunable. The value of resistance so obtained is given by:

$$R = \frac{1}{\mu_n \cdot C_{ox} \cdot \left(\frac{W}{L}\right) \cdot (V_a - V_b)}, \tag{11}$$

where $V_a$ and $V_b$ are control gate voltages; the parameters $\mu_n$, $C_{ox}$, $W$, and $L$ represent electron mobility, oxide capacitance per unit gate area, effective channel width, and effective channel length respectively and their value are expressed as:

$$\mu_n = \frac{\mu_0}{\theta\,(V_{GS} - V_T)}, \tag{12}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}, \tag{13}$$

$$W = W_{Drawn} - 2W_D, \tag{14}$$

$$L = L_{Drawn} - 2L_D, \tag{15}$$

where the symbols have their usual meaning.

The MOS transistors based implementation of linear resistors not only reduces the chip area but also makes controller parameters electronically tunable. The MOS-C implementation of the circuit of Fig. 5 is shown in Fig. 6(b).

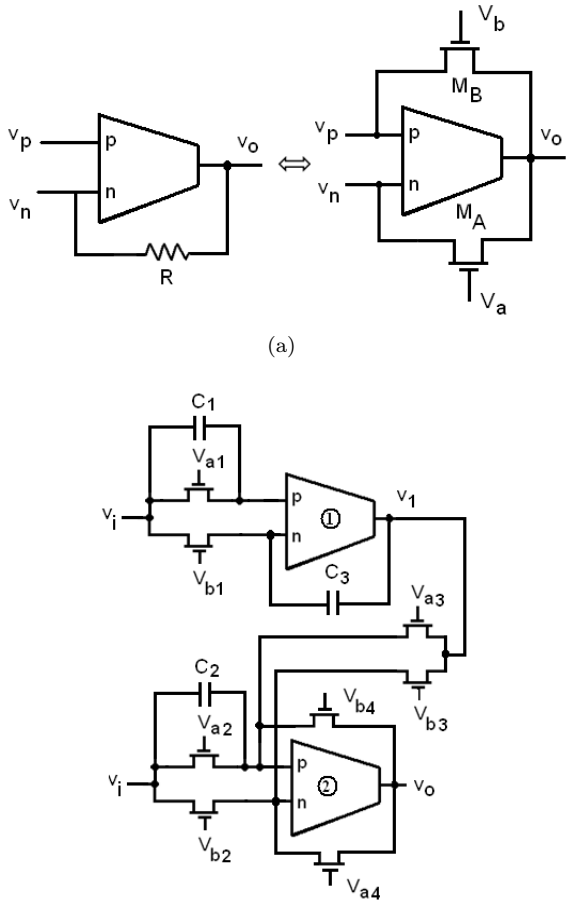



**Fig. 6:** MOS implementation of (a) linear resistance, (b) proposed PID controller.

## 3. Nonideality Analysis of PID Controller

The non-idealities associated with OTRA based circuits may be divided into two groups. The first group results due to finite trans-resistance gain whereas the second one concerns with the nonzero impedances of $p$ and $n$ terminals of OTRA.

### 3.1. Nonideality due to Finite Transresistance Gain

Here the effect of finite transresistance gain ($R_m$) on PID controller is considered, and passive compensation is employed for high-frequency applications. Ideally the $R_m$ is assumed to approach infinity. However, practically $R_m$ is a frequency dependent finite value. Considering a single pole model for the trans-resistance gain, it can be expressed in Eq. (16):

$$R_{\mathrm{m}} = \frac{R_0}{1 + \frac{s}{\omega_0}}, \tag{16}$$

$$R_m(s) \approx \frac{1}{s \cdot C_p}. \tag{17}$$

$$G_{PID}(s)_{NI} = \frac{V_o}{V_i} = \left( \frac{R_4}{R_2 \cdot (1 + s \cdot C_{p2} \cdot R_4)} + \frac{R_4 \cdot C_1}{R_3 \cdot (C_3 + C_{p1}) \cdot (1 + s \cdot C_{p2} \cdot R_4)} \right) + \frac{R_4}{s \cdot R_1 \cdot R_3 \cdot (C_3 + C_{p1}) \cdot (1 + s \cdot C_{p2} \cdot R_4)} + \frac{s \cdot C_2 \cdot R_4}{(1 + s \cdot C_{p2} \cdot R_4)}, \tag{18}$$

$$\frac{V_o}{V_i} = \frac{R_4}{R_2 \cdot (1 + s \cdot (C_{p2} - Y) \cdot R_4)} + \frac{R_4 \cdot C_1}{R_3 \cdot (C_3 + C_{p1}) \cdot (1 + s \cdot (C_{p2} - Y) \cdot R_4)} + \frac{R_4}{s \cdot R_1 \cdot R_3 \cdot (C_3 + C_{p1}) \cdot (1 + s \cdot (C_{p2} - Y) \cdot R_4)} + \frac{s \cdot C_2 \cdot R_4}{(1 + s \cdot (C_{p2} - Y) \cdot R_4)}. \tag{19}$$

where $R_0$ is dc transresistance gain. For high-frequency applications the transresistance gain reduces to Eq. (17).

The term $C_p$ represents parasitic capacitance associated with OTRA and is given by $C_p = R_0\omega_0$. Taking this effect into account Eq. (9) modifies to Eq. (18), where $C_{p1}$ and $C_{p2}$ are the parasitic capacitances of OTRA1 and OTRA2 respectively.

For high-frequency applications, compensation methods must be employed to account for the error introduced in Eq. (9). The effect of $C_{p1}$ can be eliminated by pre-adjusting the value of capacitors $C_3$ and thus achieving self-compensation. The $sC_{p2}$ term appearing in parallel to $R_4$ will result in the introduction of a parasitic pole having radian frequency as $\omega = 1/R_4C_{p2}$. The effect of $C_{p2}$ can be eliminated by connecting an admittance $Y$ between the non-inverting terminal and the output as shown in Fig. 7. Considering the circuit of Fig. 7, Eq. (18) modifies to Eq. (19).

By taking $Y = sC_{p2}$, Eq. (19) reduces to Eq. (9) thus eliminating the effect of $C_{p2}$ and hence achieving the passive compensation.

## 3.2. Effect of Nonzero Impedances of p and n Terminals

Ideally the input as well as output resistances of an OTRA are assumed to be zero. Considering the input ($R_n$ and $R_p$) and output ($R_o$) resistances of the OTRA to be finite, the equivalent model of proposed PID controller can be drawn as shown in Fig. 8.

Routine analysis of circuit of Fig. 8 results in terminal currentsIp1 and $I_{n1}$ as:

$$I_{p1} = \frac{V_i \cdot (1 + s \cdot C_1 \cdot R_1)}{R_1 + R_{p1} + s \cdot C_1 \cdot R_1 \cdot R_{p1}}, \tag{20}$$

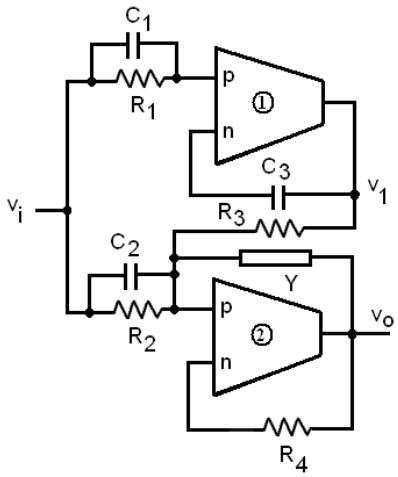



**Fig. 7:** Compensated PID controller.

$$I_{p1} = \frac{V_i \cdot s \cdot C_3}{1 + s \cdot C_3 \cdot R_{n1}}, \tag{21}$$

where $I_{p1}$ and $I_{n1}$ are the currents and $R_{p1}$ and $R_{n1}$ are the input resistances of $p$ and $n$ terminals respectively of OTRA 1. Considering $R_{m1}$ to be the transresistance gain and $R_{o1}$ is the output resistance of OTRA1, the output voltage of OTRA1, can be computed as:

$$V_1{}' = R_{m1}(I_{p1} - I_{n1}) - R_0 \cdot I_{n1}, \tag{22}$$

$$V_1{}' = R_{m1} \cdot I_{p1} - (R_{m1} + R_0) \cdot I_{n1}, \tag{23}$$

as $R_{m1} >> R_{o1}$, so $R_{m1} + R_{o1} \approx R_{m1}$ and hence:

$$V_1{}' = R_{m1} \cdot (I_{p1} - I_{n1}), \tag{24}$$

$$\frac{V_1'}{V_i} = \frac{R_{m1} \cdot (1 + s \cdot C_1 \cdot R_1)}{R_1 + R_{p1} + s \cdot C_1 \cdot R_1 \cdot R_{p1}} \cdot \frac{1 + s \cdot C_3 \cdot R_{m1}}{1 + s \cdot C_3(R_{m1} + R_{n1})}, \tag{25}$$

$$\frac{V_1'}{V_i} = \frac{(1 + s \cdot C_1 \cdot R_1) \cdot (1 + s \cdot C_3 \cdot R_{m1})}{R_1 \cdot (1 + s \cdot C_1 \cdot R_{p1}) \cdot \left(\frac{1}{R_{m1}} + s \cdot C_3\right)}, \tag{26}$$

$$V_i' = \frac{(1 + s \cdot C_1 \cdot R_1) \cdot (1 + s \cdot C_3 \cdot R_{m1}) \cdot V_i}{R_1 \cdot (1 + s \cdot C_1 \cdot R_{p1}) \cdot (s \cdot C_3)}, \tag{27}$$

$$I_{p2} = \frac{V_1'R_2 + V_iR_3\,(1 + sC_2R_2)}{R_2R_{p2} + R_2R_3 + R_{p2}R_3\,(1 + sC_2R_2)} = \frac{V_1'R_2 + V_iR_3\,(1 + sC_2R_2)}{R_2\,(R_{p2} + R_3) + R_{p2}R_3\,(1 + sC_2R_2)}$$

$$\approx \frac{V_1'R_2 + V_iR_3\,(1 + sC_2R_2)}{R_2R_3 + R_{p2}R_3\,(1 + sC_2R_2)} = \frac{V_1'R_2 + V_iR_3\,(1 + sC_2R_2)}{R_3\,(R_2 + R_{p2}) + sC_2R_2R_3R_{p2}} \tag{28}$$

$$\approx \frac{V_1'}{R_3\,(1 + sC_2R_{p2})} + \frac{V_i\,(1 + sC_2R_2)}{R_2\,(1 + sC_2R_{p2})},$$

$$I_{p2} = \frac{(1 + sC_1R_1)(1 + sC_3R_{m1})V_i}{R_1R_3(1 + sC_2R_{p2})(1 + sC_1R_{p1})(sC_3)} + \frac{V_i(1 + sC_2R_2)}{R_2(1 + sC_2R_{p2})}. \tag{29}$$

Substituting $I_{p1}$ and $I_{n1}$, Eq. (24) results in Eq. (25). As $R_1 >> R_{p1}$ and $R_{m1} >> R_{n1}$, Eq. (25) yields to Eq. (26). It can be further simplified to Eq. (27) since $1/R_{m1} << 1$.

From Fig. 8 $I_{p2}$, the $p$ terminal current of OTRA2, can be written as Eq. (28), where $R_{p2}$ is the $p$ terminal resistance of OTRA2. Substituting for from Eq. (27) $I_{p2}$ can be expressed as Eq. (29)

Similarly considering $R_{n2}$ to be the $n$ terminal resistance of OTRA2 the $I_{n2}$ can be represented as Eq. (30) shown bellow:

$$I_{n2} = \frac{V_o}{R_4 + R_{n2}}, \tag{30}$$

and the output voltage of OTRA2, can be computed as:

$$V_o = R_{m2}(I_{p2} - I_{n2}) - R_{o2}I_{n2}, \tag{31}$$

where $R_{m2}$ and $R_{o2}$ are transresistance gain and output resistance of OTRA2 respectively. Since $R_{m2} >> R_2$, so $R_{m2} + R_{o2} \approx R_{m2}$ and hence

$$V_o \approx R_{m2}\,(I_{p2} - I_{n2})\,, \tag{32}$$

$$V_o = \frac{R_4(1 + sC_1R_1)(1 + sC_3R_{n1})V_i}{R_1R_3sC_3(1 + sC_1R_{p1})(1 + sC_2R_{p2})} + \frac{R_4(1 + sC_2R_2)V_i}{R_2(1 + sC_2R_{p2})}, \tag{33}$$

and the transfer function $V_o/V_i$ modifies to:

$$\frac{V_o}{V_i} = \frac{1}{(1 + sC_2R_{p2})}\left(\frac{R_4C_1\,(1 + sC_3R_{n1})}{R_3C_3\,(1 + sC_1R_{p1})} + \frac{R_4}{R_2}\right) + \frac{R_4\,(1 + sC_3R_{n1})}{R_1R_3sC_3\,(1 + sC_1R_{p1})\,(1 + sC_2R_{p2})} + \frac{sC_2R_4}{(1 + C_2R_{p2})}. \tag{34}$$

It is observed from Eq. (34) that the nonzero values of input resistances at $n$ and $p$ terminal of OTRAs result in introduction of parasitic pole and zero in proportional and integral terms and the derivative term consists of a parasitic pole. The numerical values of poles and zeros are very high as parasitic resistances of OTRA are very small. Thus, the parasitic zero and pole frequencies would not practically influence the system performance.

## 4. Simulation Results

The theoretical propositions are verified through SPICE simulations using 0.18 µm CMOS process parameters provided by MOSIS. The CMOS implementation of the OTRA, proposed in [13] with supply voltages ± 1.5 V was used for simulation. For performance evaluation of the proposed controllers, their time domain responses are obtained. The ideal and simulated time domain responses of the proposed PI controller of Fig. 3, for a 50 mV step input voltage with 20 ns rise time, are shown in Fig. 9(a). The passive component values of the PI controller are chosen as $R = 50$ kΩ, $C = 4$ pF and $C_f = 2$ pF and the corresponding controller parameters are computed to be $K_p = 2$, $K_i = 10^7$ s$^{-1}$. For transient analysis of PD controller of Fig. 4, a 50 mV peak triangular input voltage is applied. The ideal and simulated transient responses are depicted in Fig. 9(b). The component values for the PD controller are chosen as R = 10 kΩ, $R_f = 20$ kΩ and $C = 20$ pF and the controller parameters are computed to be $K_p = 2$, $K_d = 0.4$ µs. For the PID controller of Fig. 5, values of the capacitors are taken as $C_1 = C_3 = 10$ pF and $C_2 = 0.05$ pF. The resistive component values are chosen as $R_1 = R_2 = R_3 = R_4 = 50$ kΩ. Using these passive component values various controller parame-

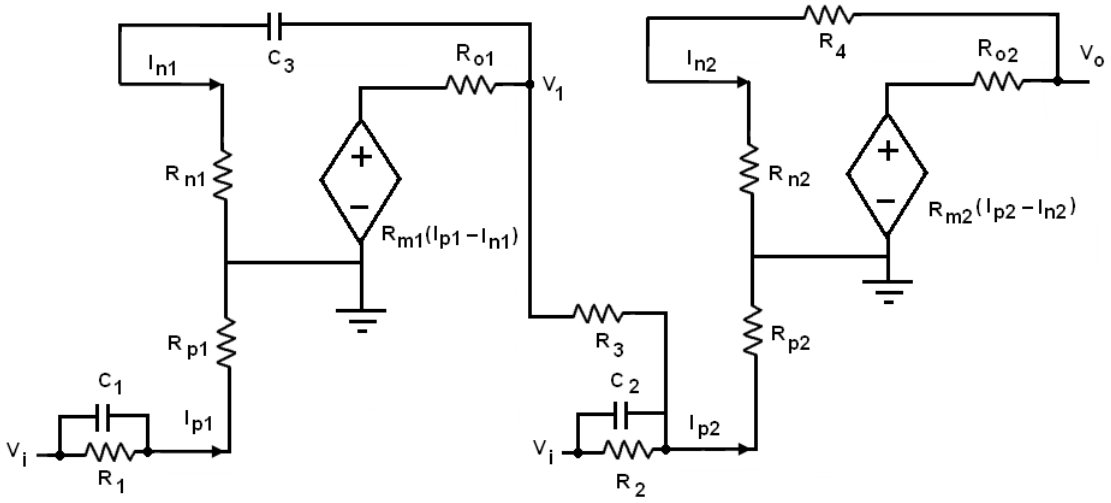
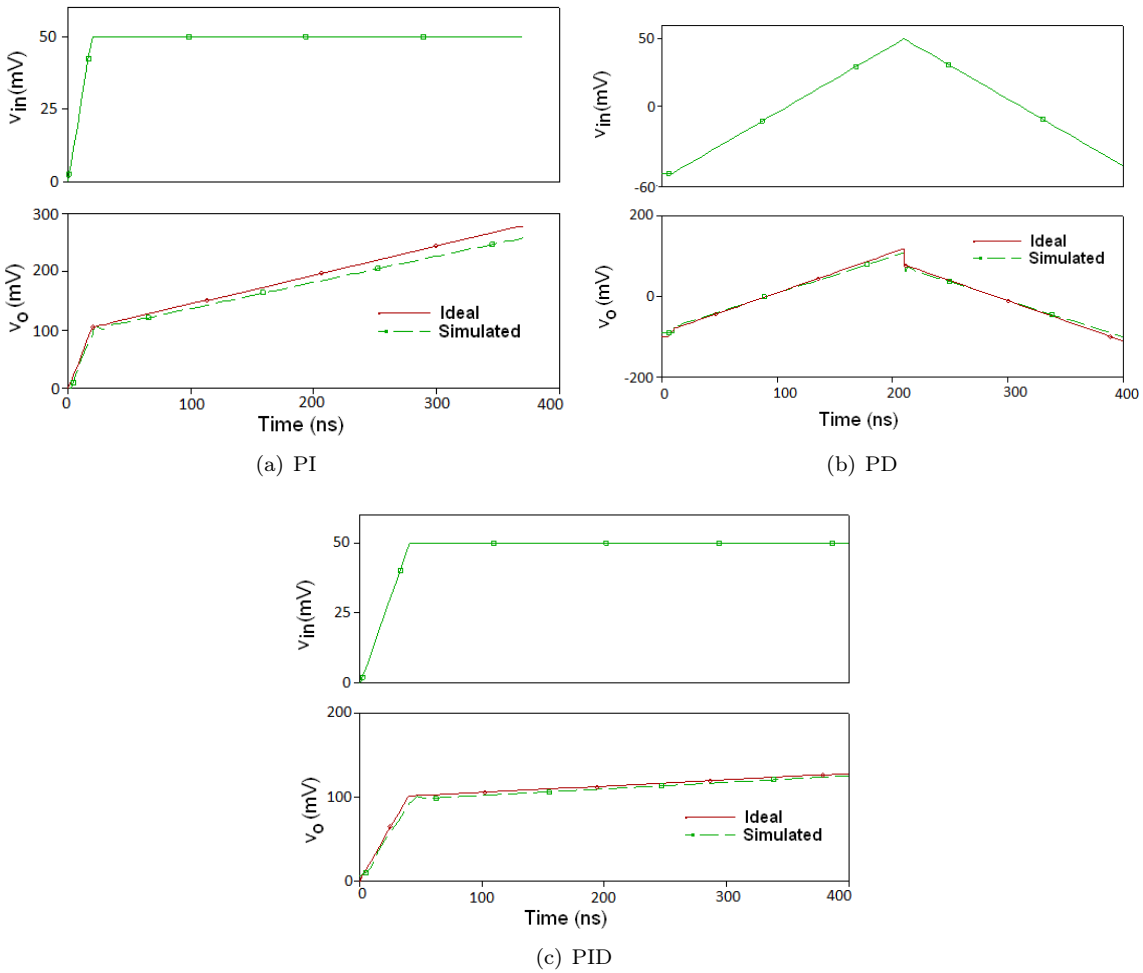



**Fig. 8:** Equivalent model of proposed PID controller.




(a) PI

(b) PD

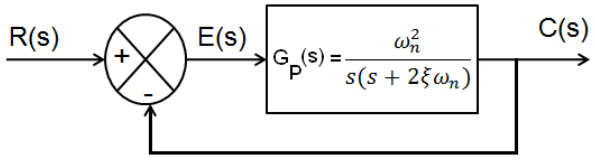
(c) PID

**Fig. 9:** Time domain response of the proposed controllers.

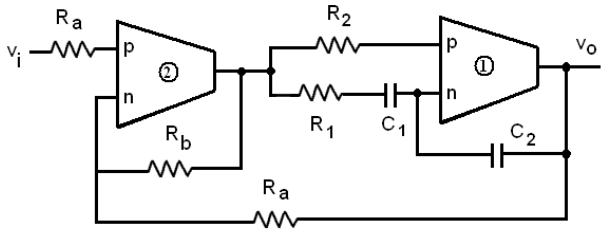
ters are computed as $K_p = 2$, $K_i = 2 \cdot 10^6$ s$^{-1}$ and $K_d = 2.5$ ns. For time domain analysis, a 50 mV step signal with 10 ns rise time is applied. The transient response of proposed PID controller is shown in Fig. 9(c). It is observed that for all the controllers the simulated and ideal responses are in close agreement.

## 5. Performance Evaluation of the Proposed Controllers

To evaluate the effect of various controllers, the performance of a second order plant is analyzed by forming a closed loop system as shown in Fig. 10(a) where $G_P(s)$ represents the open loop transfer function of a unity feedback system. For OTRA based realization of the closed loop system the low-pass filter (LPF) presented in [14] is used and is modified as shown in Fig. 10(b). The OTRA1, resistors $R_1$, $R_2$, along with capacitors $C_1$ and $C_2$ form the second order plant whereas OTRA2 along with resistors $R_a$ and $R_b$ is used as subtractor thereby forming the error signal. The circuit of Fig. 10 can also be made electronically tunable by implementing all the related resistors using MOS transistors operating in the linear region.




(a) Block diagram.




(b) OTRA based realization.

**Fig. 10:** Second order closed loop system.

The transfer function of the circuit of Fig. 10(b) using equal component design with $R_1 = R_2 = R$ and $C_1 = C_2 = C$ can be derived as:

$$\frac{V_o(s)}{V_i(s)} = \frac{\frac{K}{R^2C^2}}{\left(s^2 + \frac{s}{CR} + \frac{K}{R^2C^2}\right)}, \tag{35}$$

where

$$K = \frac{R_b}{R_a}. \tag{36}$$

The standard characteristic polynomial, $D(s)$, of second order system [12] is given by:

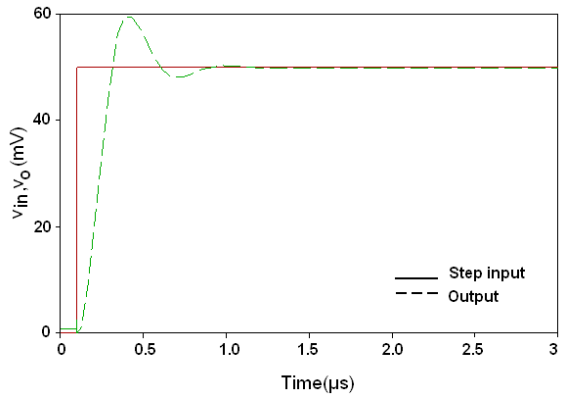
$$D(s) = s^2 + 2\xi\omega_n s + \omega^2{}_n, \tag{37}$$

where $\omega_n$ is the natural frequency of oscillations and $\xi$ represents the damping factor. Comparing the denominator of Eq. (35) with Eq. (37) the $\omega_n$ and $\xi$ for the LPF can be computed as:

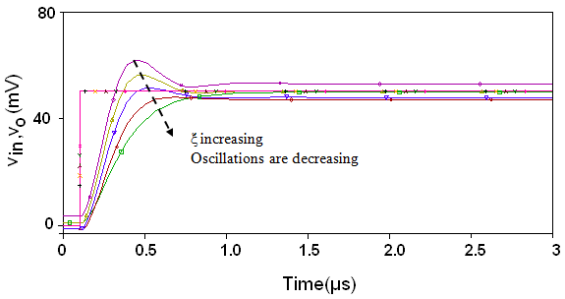
$$\omega_n = \frac{\sqrt{K}}{RC} \; and \; \xi = \frac{1}{2\sqrt{K}}. \tag{38}$$

In the study that follows, the step response of the open loop second order system (LPF) is analysed first and then the effect of various proposed controllers on this second order system is observed by forming closed loop with controllers.

For the second order system shown in Fig. 10(b), the passive component values are chosen as $R_a = R_b = 20$ kΩ, $R_1 = R_2 = R_3 = 2$ kΩ, and $C_1 = C_2 = 20$ pF. The $f_n$ and $\xi$ for the LPF can be computed as 3.98 MHz and 0.5 respectively.




(a) with fixed $\xi$



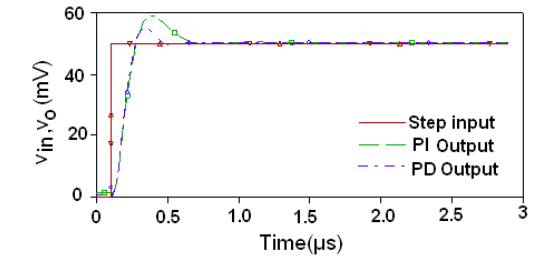

(b) with varying $\xi$

**Fig. 11:** Step Response of LPF.

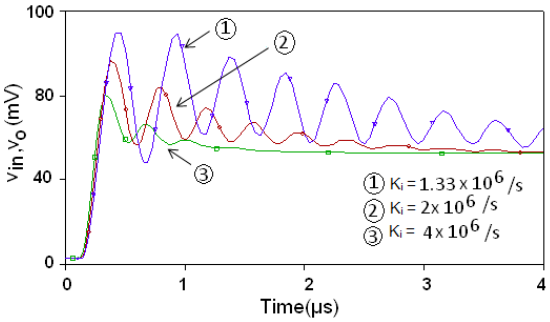
To observe the step response of the LPF a step input of 50 mV is applied, and the simulated response is shown in Fig. 11(a). The effect of damping ratio, $\xi$ on the step response of the second order LPF is shown in Fig. 11(b). To change $\xi$, $R_b$ is kept constant while $R_a$

**Tab. 2:** Performance Comparison of second order system.

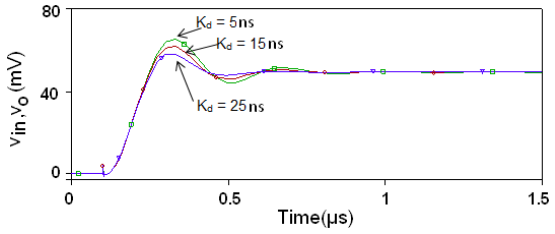
| Parameter | Unity feedback closed loop system | Closed loop with PD controller ($K_p = 2$, $K_i = 10^7$ s$^{-1}$) | Closed loop with PI controller ($K_p = 2$, $K_d = 0.4$ µs) | Closed loop with PID controller ($K_p = 2$, $K_i = 2 \cdot 10^6$s$^{-1}$, $K_d = 2.5$ ns) |
|---|---|---|---|---|
| **Overshoot** | 19.56 % | 12.47 % | 18.76 % | 8.16 % |
| **Peak output** | 58.26 mV | 56.52 mV | 57.83 mV | 52.59 mV |
| **Rise time** | 140.43 ns | 119.89 ns | 112.28 ns | 99.75 ns |
| **Settling time** | 303.12 ns | 274.35 ns | 266.11 ns | 252.27 ns |



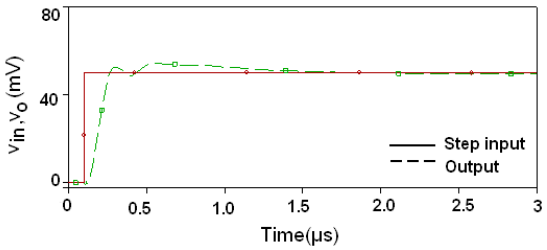

(a) with PI and PD controllers.




(b) with variable $K_i$ for PI controller.




(c) with variable $K_d$ for PD controller.




(d) PID controller.

**Fig. 12:** Response of a second order system.

is varied electronically by changing gate voltages of the transistors used for implementing it. It is observed that with the increase in $\xi$, oscillations are decreasing and is perfectly in tune with the theoretical concept. The performance of PI, PD, and PID controllers is evaluated by comparing step responses of closed loop systems based on these controllers. Figure 12(a) depicts the effects of proposed PI ($K_p = 2$, $K_i = 10^7$ s$^{-1}$) and PD ($K_p = 2$, $K_d = 0.4$ µs) controllers on step response of the closed loop system. Step response for varying values of $K_i$, while keeping $K_p = 2$ constant, is depicted in Fig. 12(b). The effect of variable $K_d$ on the step response of the system, keeping $K_p = 2$ constant, is shown in Fig. 12(c). System step response with PID controller is represented by Fig. 12(d). Performance parameters such as overshoot, peak output, rise time and settling time of the closed-loop system with different controllers are measured and tabulated in Tab. 2. The study of the table clearly suggests that with the help of controllers the system performance is improved in a desired manner. The PD controller prominently improves the overshoot whereas PI controller influences mainly the settling time as compared to all other parameters. The PID includes best features of all individual controllers and results in improvement of all the performance measure parameters.

## 6. Conclusion

Operational transresistance amplifier based PI, PD and PID controllers have been presented which possess the feature of independent tuning of proportional ($K_p$), derivative ($K_d$) and integral ($K_i$) constants. By implementing the resistors using MOS transistors operating in linear region MOS-C equivalent of the controllers can be obtained which are suitable for full integration. This also results in reduced chip area and power consumption as compared to passive resistors. To verify the functionality of the proposed controllers their effect on a second order closed loop system was analyzed through simulations. The simulated results are in line with the proposed theory. The performance analysis reveals that PD controller improves percentage overshoot, PI controller refines settling time while PID as a combination of the two, enhances transient as well as the steady-state response of the system.

## References


[1] FRANCO, S. *Design with operational amplifiers and analog integrated circuits.* 3rd ed. Boston: McGraw-Hill, 2002. ISBN 00-723-2084-2.

[2] KARA, M. T. and M. E. RIZKALLA. Single op-amp proportional-integral compensator with antiwindup. In: *1993 IEEE International Symposium on Circuits and Systems.* Chicago: IEEE, 1993, pp. 2260–2263. ISBN 0-7803-1281-3. DOI: 10.1109/ISCAS.1993.394212.

[3] MICHAL, V., C. PREMONT, G. PILLONET and N. ABOUCHI. Single active element PID controllers. In: *20th International Conference Radioelektronika 2010.* Brno: IEEE, 2010, pp. 1–4. ISBN 978-1-4244-6318-3. DOI: 10.1109/RADIOELEK.2010.5478563.

[4] TOUMAZOU, C., F. J. LIDGEY and D. G. HAIGH. *Analogue IC Design the Current Mode Approach.* 1st ed. London: Peter Peregrinus on behalf of the Institution of Electrical Engineers, 1990. ISBN 08-634-1297-1.

[5] EDRAL, C., A. TOKER and C. ACAR. OTA-C Based Proportional- Integral-Derivative (PID) Controller and Calculating Optimum Parameter Tolerances. *Turkish Journal of Electrical Engineering and Computer Sciences.* 2001, vol. 9, no. 2, pp. 189–198. ISSN 1303-6203.

[6] KESKIN, A. U. Design of a PID Controller Circuit Employing CDBAs. *International Journal of Electrical Engineering Education.* 2006, vol. 43, no. 1, pp. 48–56. ISSN 0020-7209. DOI: 10.7227/IJEEE.43.1.5

[7] MINAEI, S., E. YUCE, S. TOKAT and O. CICEKOGLU. Simple Realizations of Current-Mode and Voltage-Mode PID, PI and PD Controllers. In: *Proceedings of the IEEE International Symposium on Industrial Electronics.* Dubrovnik: IEEE, 2005, pp. 195–198. ISBN 0-7803-8738-4. DOI: 10.1109/ISIE.2005.1528911

[8] YUCE, E., S. TOKAT, S. MINAEI and O. CICEKOGLU. Low-Component-Count Insensitive Current-Mode and Voltage-Mode PID, PI and PD Controllers. *Frequenz.* 2006, vol. 60, no. 3–4, pp. 65–70. ISSN 2191-6349. DOI: 10.1515/FREQ.2006.60.3-4.65.

[9] CHEN, J. J., H. W. TSAO and C. C. CHEN. Operational transresistance amplifier using CMOS technology. *Electronics Letters.* 1992, vol. 28, no. 22, pp. 2087–2088. ISSN 0013-5194. DOI: 10.1049/el:19921338.

[10] SALAMA, K. N., A. M. SOLIMAN and C. C. CHEN. CMOS operational transresistance amplifier for analog signal processing. *Microelectronics Journal.* 1999, vol. 30, no. 3, pp. 235–245. ISSN 0026-2692. DOI: 10.1016/S0026-2692(98)00112-8.

[11] ASTROM, K. J., T. HAGGLUND and C. C. CHEN. The future of PID control. *Control Engineering Practice.* 2001, vol. 9, no. 11, pp. 1163–1175. ISSN 0967-0661. DOI: 10.1016/S0967-0661(01)00062-4.

[12] GOLNARAGHI, M. and B. C. KUO. *Automatic control systems.* 9th ed. Hoboken, NJ: Wiley, 2010. ISBN 978-047-0048-962.

[13] KAFRAWY, A. K. and A. M. SOLIMAN. A modified CMOS differential operational transresistance amplifier (OTRA). *AEU - International Journal of Electronics and Communications.* 2009, vol. 63, no. 12, pp. 1067–1071. ISSN 1434-8411. DOI: 10.1016/j.aeue.2008.08.003.

[14] GOKCEN, A., S. KILINC and U. CAM. Second Order Analog Filter Design Using a Single OTRA Suitable for Integration. In: *15th Signal Processing and Communications Applications.* Eskisehir: IEEE, 2007, pp. 1–4. ISBN 1-4244-0719-2. DOI: 10.1109/SIU.2007.4298816.


## About Authors

**Rajeshwari PANDEY** did B.Tech. (Electronics and Telecommunication) from University of Allahabad, India, M.E. (Electronics and Control) from Birla Institute of Technology and Sciences, Pilani, Rajasthan, and Ph.D. from Delhi University, India.Currently, she is Associate Professor in Department of Electronics and Communication Engineering, Delhi Technological University, Delhi. Her research interests include Analog Integrated Circuits, and Microelectronics.

**Neeta PANDEY** did M.E. in Microelectronics from Birla Institute of Technology and Sciences, Pilani, Rajasthan, India and Ph.D. from Guru Gobind Singh Indraprastha University Delhi, India. At present she is Associate Professor in Department of Electronics and Communication Engineering, Delhi Technological University, Delhi. A life member of ISTE, and member of IEEE, USA, she has published papers in International, National Journals of repute and conferences. Her research interests are in Analog and Digital VLSI Design.

**Saurabh CHITRANSI** did B.Tech. (Electronics and Communication) from Uttar Pradesh Technical

University of Lucknow, India and M.Tech. (VLSI Design and Embedded System) from Delhi Technological University, Delhi, India. Currently, he is Executive Engineer in Diffusion and CVD Department, SITAR, DRDO, Bangalore, India. His research interests include Analog Integrated Circuits, MEMS and Silicon process integration.

**Sajal K. PAUL** did B.Tech., M.Tech., and Ph.D. in Radio Physics and Electronics from the Institute of Radio Physics and Electronics, University of Calcutta. He has served Webel Telecommunication Industries, Kolkata; Indira Gandhi National Open University (IGNOU), Kolkata; Advanced Training Institute for Electronics and Process Instrumentation(ATI-EPI), Hyderabad; North Eastern Regional Institute of Science Technology(NERIST), Nirjuli and Delhi College of Engineering(DCE), Delhi in various capacities. He has served the Department of Electronics Engineering, Indian School of Mines, Dhanbad as Head of the Department and at present Professor of the same department. His research interest includes Microelectoncic Devices, Electronic Properties of Semiconductor and Bipolar and MOS Analog Integrated Circuits. He has more than 60 research publications in International and National journals of repute and conferences.