PQ Improvement by Moderation of Multi-Level Inverter Controlling Techniques and Intensifying the Performance of DVR

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DOI: 10.15598/aeee.v13i2.1244

Abstract. *A novel control scheme is proposed for the enhancement of Dynamic Voltage Restorer (DVR) performance. In this paper, the moderation of inverter controlling techniques has been adopted to intensify the DVR characteristics and thereby to improve the Power Quality. The proposed model verification has been obtained by simulation of the PWM patterns which provides the better utilization of the device (DVR) for the compensation of voltage deviations during voltage sag. Also, it has been shown that Dynamic Voltage Restorer can be worked as a harmonic compensator for the compensation of the current and voltage harmonics. Obtained simulation results verify that the control approach gives very effective regulation and performs excellent voltage compensation by adopting multilevel inverter.*

Keywords

DVR, harmonic sistortion, mitigation, multi level inverter, power quality (PQ), voltage sag.

1. Introduction

The development of industrial as well as commercial sectors depends on power electronic based process control and sensitive electronic appliances, which further rely on their amenability to power quality problems. The well discerned power quality problems includes voltage spikes and transients; shallow and deep momentary sags; momentary interruptions; temporary or sustained interruptions, etc.

The productivity loss due to these brief power interruptions and deep voltage sags has been called the vital concern affecting the most commercial and industrial customers thus costing billions of dollars per annum in the U.S.A. alone [1].

Though these PQ events typically last for less than 1 second, resulting voltage sag down to 50 % of nominal voltage and these may be accompanied by the occasional short-term interruptions, which may endure for nearly 6 to 10 cycles. During these PQ events, the cost has been computed in several studies in the aspects of long restart, scrapped products and cleanup times, totaling from several hundred dollars to $ 800 000 per event especially for semiconductor plants.

The use of power electronic devices using inverters, unbalanced loads like large furnaces or rectifiers can lead to the aggravation of power quality. The poor power quality causes troubles in power electronic equipment.

There are many power quality issues that may be categorized by different characteristics and are described in IEEE Standard 1159 [4]. From this, it is clear that every event of power quality phenomenon has its consequence with its duration and magnitude [18]. Though the duration of events is for few cycles, the effect of respective event may be severe for the sensitive instruments Because of many reasons these power quality issues may occur at the supplier's system or the user's system.

Voltage sag shown in Fig. 1 amid various PQ issues appeals an attention of researchers from industries and academia as well. The semiconductor and IT industries recognize willingness of instruments against these voltage sags and ensuring their concerned costs to the end

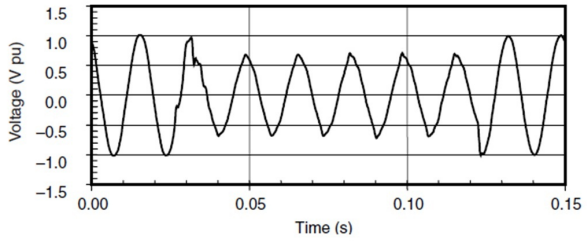

Fig. 1: Sample distribution system.

user. Also they recommend the allowable input voltage magnitude and duration of curves for their apparatus.

Since the electrical power system network consisting of parallel distribution and transmission feeders may have variable load conditions and may lead to the various faults. These faults may cause voltage sag and that should be mitigated before it reaches the sensitive load as shown in Fig. 2. This is possible by adopting a Dynamic Voltage Restorer, which is a custom power device.

Since the faults on parallel distribution and transmission feeders normally lead to the voltage dip, a distinct solution to this problem at large power levels has been called upon a Dynamic Voltage Restorer, which is a custom power device.

2. Working of DVR

DVR shown in Fig. 2 is a series of FACTS device used to mitigate PQ issues like voltage sag, voltage swell, harmonic distortion, and flicker. DVR is intended to compensate transient voltages by the series injection of voltage to the mains of distribution system. The phase and magnitude of the series injected voltage can compensate sag or swell occurred in the distribution network at the upstream level [11]. To operate DVR independently and to make it as a custom power device, a large storage device is required, which can be operated from an external power source during transients. A capacitor bank, a battery, and flywheel are broadly used for this purpose as described in Fig. 3.

The voltage improvement is obtained conventionally by injecting a voltage in phase with the mains supply voltage, as described in [20], [11], [21], [22], and [23]. Mostly used technique that makes the injected voltage and load current in phase quadrature with each other is based on operating the Dynamic Voltage Restorer as a series capacitor. This most commonly used method consists of 2-level or multi-level converter and it has a DC capacitor, which it shares among all the three phases [22]. The main function of the capacitor used in the converter is to absorb the harmonic ripple, which requires small energy storage during balanced condi-

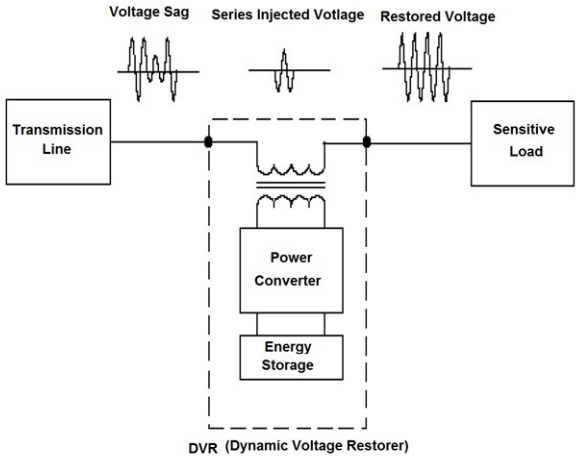

Fig. 2: Voltage sag waveform.

tions. During an un-balanced circumstance, the size of the capacitor needs to be increased since the capacitor is shared amongst all the three phases. If voltage dip occurs only in one phase, which may also lead to the deformation in the waveforms of the other two phase currents.

The Dynamic Voltage Restorer is cascaded with the power distribution line as shown in Fig. 3. With a series connected transformer and by injecting desirable voltage phasor through it, the DVR is capable to control the voltage across a sensitive load. With this effect, any voltage disruption in the upstream can be compensated through DVR and unseen to the sensitive load [24].

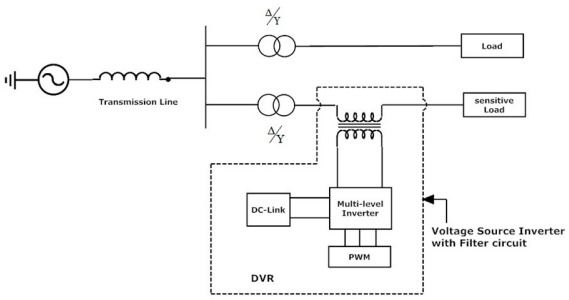

Fig. 3: Elaborated schematic diagram of a DVR.

2.1. Sag Compensation

The power distribution system during voltage sag can be represented by its phasor diagram as depicted in Fig. 4. Where, V_1 is the post voltage sag magnitude, V_2 is compensated load voltage magnitude, and V_{dvr} is the DVR injected voltage magnitude. Also IL represents the load current, φ represents the load power factor angle, δ represents supply voltage phase angle deviation, and α represents voltage advance angle.

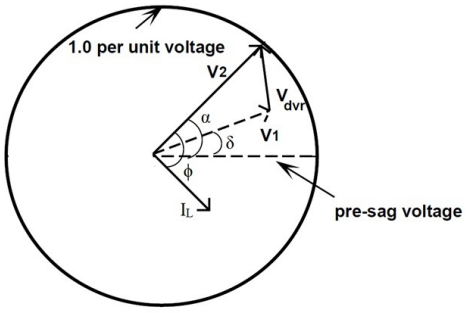

Fig. 4: Phasor diagram of a power system network during sag.

The energy required by DVR for the voltage refurbishment can be kept at minimal by elevating all the three phases with a certain amount of advance angle α.

The desired DVR injected voltage magnitude V_{dvr} and its phase angle can be obtained within component and modulation limits by designing an appropriate Pulse Width Modulation (PWM) technique. By assuming that V_{dvr} is in quadrature then the minimal value of supply voltage that can be injected to V_2 is:

$$\left|V_1^{\min}\right| = \cos(\varphi)\left|V_2\right|, \tag{1}$$

where cos (φ) is the load power factor in the respective phase. If is considered as the voltage of the quadrature DVR which has the magnitude of limited value, then the minimal supply voltage that can be injected to V_2 is given by:

$$\left|V_1^{\min}\right| = \\ = \sqrt{\left[\left|V_2\right|^2\right] - 2\left|V_2\right|\left|V_{dvr}^{\max}\right|\sin(\varphi) + \left|V_{dvr}^{\max}\right|^2}. \tag{2}$$

The cascaded injection transformer's turns ratio and the PWM inverter's limitations would decide the limiting value of the injected voltage. Since, the DVR is adequate to supply both real power and reactive power; only through an exchange of reactive power, a small disturbance can be furbished. However, for the large disturbances a capacitor bank is provided to supply real power to the sensitive load [24].

1) Voltage Sags with Phase Jumps

When a short circuit current flows through into a fault, which causes voltage sags as depicted in Fig. 5. From this circuit a simplified Eq. (3) can be obtained as:

$$V_{sag} = \frac{EZ_f}{(Z_f + Z_s)}. \tag{3}$$

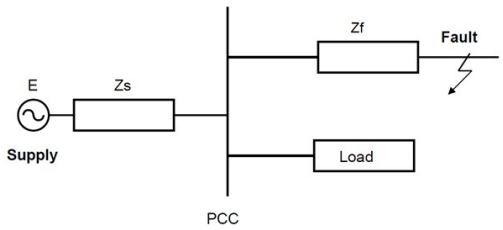

Fig. 5: Circuit for voltage reduction and phase jump calculation.

The Eq. (3) is used to determine magnitude and phase of the voltage, V_{sag} during voltage sag at the Point of Common Coupling (PCC).

2.2. Compensation with Phase Advancement

The PAC (Phase Advancement Compensation) technique is accomplished by the adjustment in angle α with an advantage of minimal real power requirement from the DVR energy storage device. This PAC technique accords DVR to help the load hinges through more severe voltage sags.

However, for an un-interrupting operation of the sensitive loads, it is desired to have the gradual advancement of α both at the beginning and at the end of the sag compensation.

A power system network connected with a DVR is described in Fig. 6, from which it is clear that the compensated load voltage magnitude V_2 is regulated by the DVR through injected voltage V_{dvr}.

Assuming L_1, R_2, L_f, and R_f are the inductance and resistance of the load and DVR harmonic filter respectively and C_f is the capacitance of the filter circuit. Also, R_t is the combined winding resistance and L_t is the leakage inductance of a series injection transformer.

Under the phase advancement scheme, the power flow contributions of the Dynamic Voltage Restorer for the j^{th} phase are given as:

$$P_{in} = \sum_{\forall j} V_{1j} I_j \cos(\varphi - \alpha + \delta_j), \tag{4}$$

$$P_{out} = \sum_{\forall j} V_{2j} I_j \cos(\varphi), \tag{5}$$

where P_{in} and P_{out} are power from the source and load respectively and j=1, 2, 3... If the load is balanced, i.e. I_j=I, and for balanced output voltage V_{2j}=V_2, the correction introduced by the DVR can be given as:

$$P_{out} = 3V_2 I\cos(\varphi). \tag{6}$$

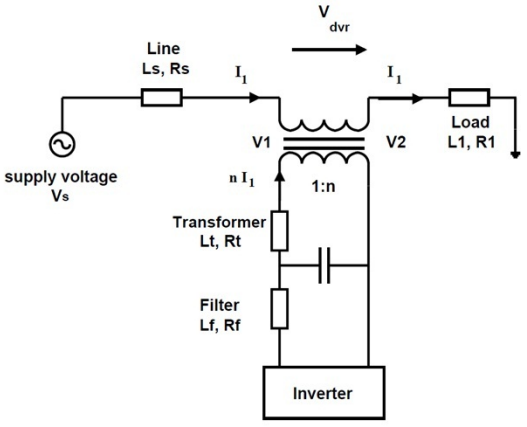

Fig. 6: DVR connected to power system network.

Power supplied by the DVR is assumed as P_{dvr}, and then the following equation can be obtained.

$$P_{dvr} = P_{out} - P_{in}. \tag{7}$$

From the Eq. (4) and Eq. (6), the required power that can be supplied by DVR can be given as:

$$P_{dvr} = 3V_2 I\cos(\varphi) - \sum_{\forall j} V_{1j} I_j \cos(\varphi - \alpha + \delta_j). \tag{8}$$

Similarly the reactive power equations can be written as follows:

$$Q_{in} = \sum_{\forall j} V_{1j} I_j \sin(\varphi - \alpha + \delta_j), \tag{9}$$

$$Q_{out} = \sum_{\forall j} V_{2j} I_j \sin(\varphi), \tag{10}$$

$$Q_{out} = 3V_2 I\sin(\varphi), \tag{11}$$

$$Q_{dvr} = Q_{out} - Q_{in}, \tag{12}$$

$$Q_{dvr} = 3V_2 I\sin(\varphi) - \sum_{\forall j} V_{1j} I_j \sin(\varphi - \alpha + \delta_j), \tag{13}$$

where, Q_{in} and Q_{out} are the input and load reactive power respectively.

From the Eq. (4) to Eq. (13), it is apparent that the exchange of real and reactive powers between DVR and a distribution system can be controlled possibly by proper adjustment of the phase angle α for a given values of φ, δ, $V1$, and $V2$. There are many controlling techniques for adjusting the angle α, for voltage compensation known as PWM techniques. The performance of DVR can be intensified by adopting multi-level inverter based DVR.

The proposed method is based on cascaded H-bridge based DVR, which is extremely useful in the higher power applications.

3. Multi-Level Inverter

A Two-Level DVR with different switching patterns can be designed for low power and low voltage applications. However, the switching patterns with the series and parallel connections realize the problem with the sharing of both the voltage and current. To avoid such problem, a new method is proposed here with a Cascaded H-Bridge Multi-Level Inverter (MLI) based DVR.

3.1. Cascaded H-Bridge Inverter

An MLI produces considerably fewer harmonics compared to Two-Level Inverter, and also it can synthesize the desired output voltage with smaller steps by potentially reducing dv/dt, thus lowering the Electro Magnetic Interference (EMI). In addition, the H-Bridge cascaded structure is able to solve the problems of inadequate device rating and disturbed DC link voltage.

The Fig. 7 describes a cascaded H-Bridge for n-level inverter, in which each H-Bridge cell consists of four switches. The different switch positions determine different voltages such that one switch for $V+$, one switch for $V-$ and other two switches for 0 volts. S_1, S_2 are connected to $+ve$ terminal and S_3, S_4 are connected to $-ve$ terminal of DC voltage.

The total output voltage of this configuration is obtained by summation of voltages that each cell generates. The total number of output voltage levels is given by $2n + 1$; where n gives the number of cells. One of

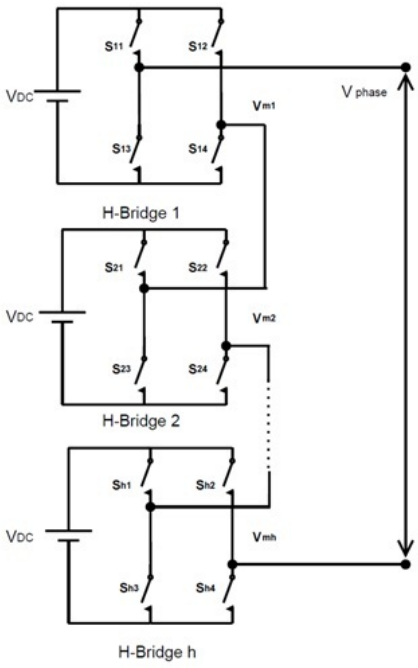

Fig. 7: Cascaded H-Bridge for n-level inverter.

the advantages of this type of configuration is that it needs less number of components compared to other two widely used configurations. One is diode clamped, and the other is a flying capacitor. For an n level H-bridge MLI, $2n-1$ switching devices are required.

3.2. Control Circuit for H-Bridge Inverter

The cascaded H-Bridge MLI control scheme is described in Fig. 8. In this control strategy, all the three phase voltages i.e. a, b and c are measured. Also, with the stationary reference frame they can metamorphose to an orthogonal equivalent two-phase system (α, β). Later these voltages are converted into synchronous frame (d, q). By an appropriate monitoring the change in the direct axis synchronously rotating frame voltage at the disturbance such as sag, the PWM signals are generated to inject correcting voltage.

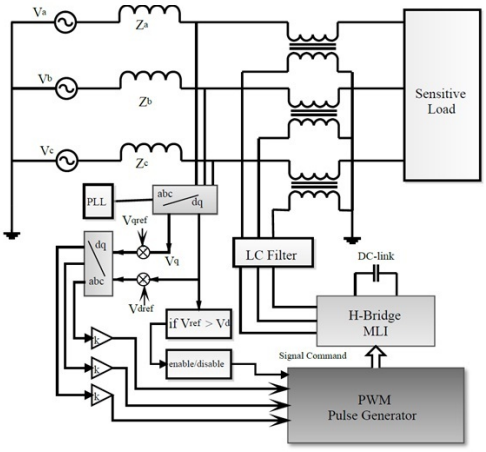

Fig. 8: Control circuit for H-Bridge MLI.

3.3. Simulation Results

The control scheme shown in Fig. 8 is simulated for both balanced and un-balanced conditions, where DVR is compensating the voltage sag and providing smooth voltage to the sensitive load.

The sag is created using three different faults namely, line to ground fault, three phase fault and line to line fault. Digital simulation is done using the blocks of MATLAB Simulink, and the results are presented here.

When Sag occurs in the three phase system, its magnitude reduces about 10 % to 90 % of the actual peak value. The effect of sag can be described with a simulated waveform of a three phase systems (shown in Fig. 9) and out of three phases one phase got affected.

Now, it is required to inject the reduced magnitude of the voltage into the system through DVR. The injected voltage should be for the only affected phase as described in Fig. 10, so that the complete system gets restored as shown in Fig. 11.

The system voltages, injected DVR voltages and voltage given to critical loads are described from Fig. 9 to Fig. 17 respectively.

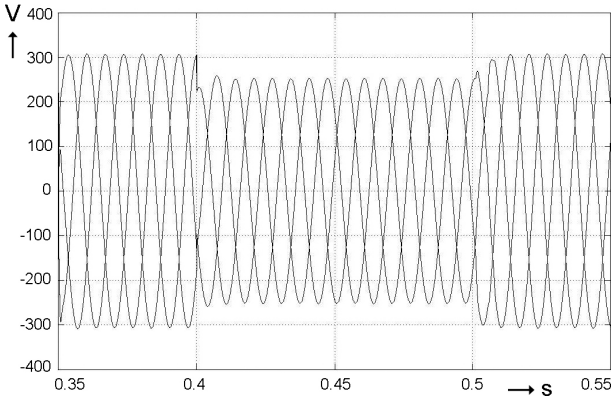

Fig. 9: Voltage sag occurred in three phases.

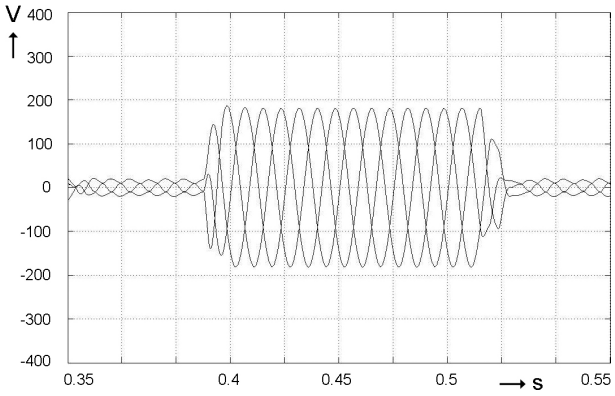

Fig. 10: Injected DVR voltages for sag compensation.

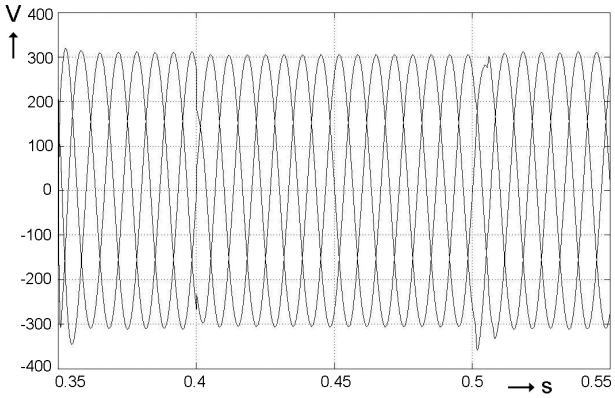

Fig. 11: Restored grid voltages.

The simulation results as shown in Fig. 9 describes the voltage waveforms of a 3-phase system during a sag in three phases. Similarly, Fig. 12 and Fig. 15 gives

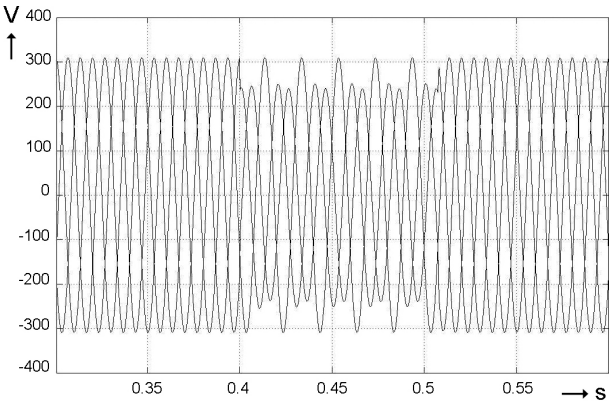

Fig. 12: A fault causing sag in two phases.

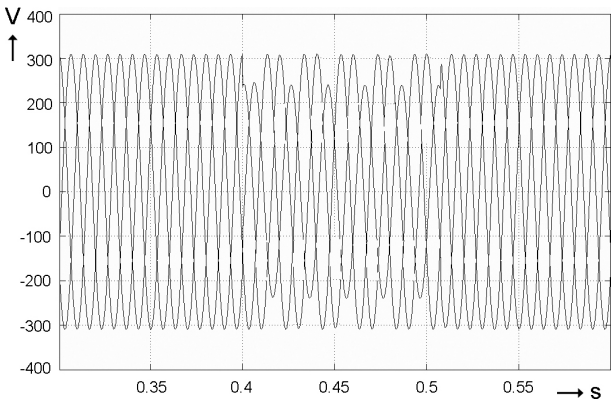

Fig. 15: Voltage sag in single phase.

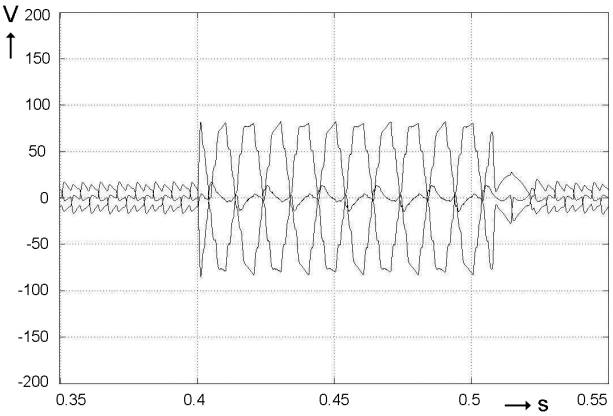

Fig. 13: Injected DVR voltages.

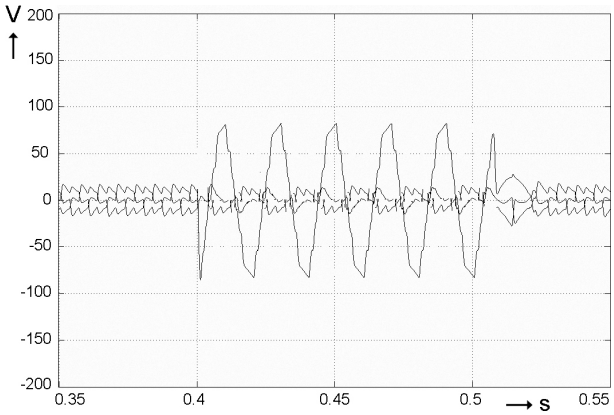

Fig. 16: DVR injected voltages.

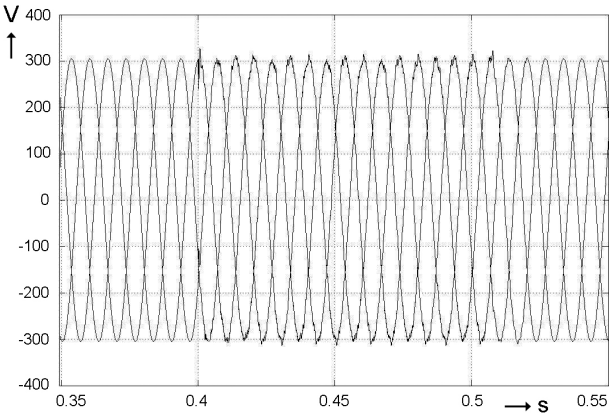

Fig. 14: Restored grid voltages.

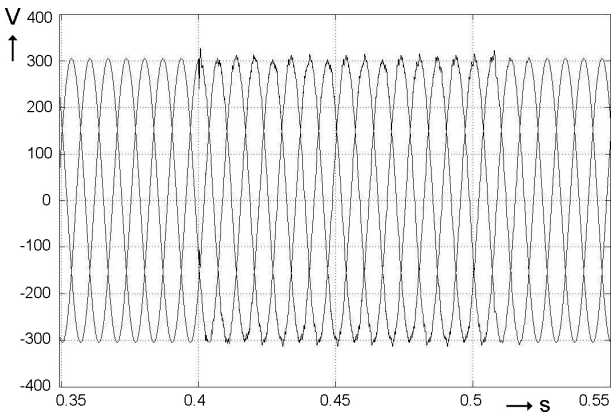

Fig. 17: Control circuit for H-Bridge MLI.

the voltage waveforms during a sag in two phases and a single phase respectively. During a sag in the system voltages, the required DVR injected voltages are developed with the simulation circuit, and the corresponding DVR injected voltages were obtained as shown in Fig. 10, Fig. 13 and Fig. 16.

All the three phase voltages were compensated, and the grid voltages were restored with the help of a DVR according to their corresponding voltage variations during a sag. The obtained restored grid voltages are represented in Fig. 11, Fig. 13 and Fig. 17.

4. Conclusion

The effect of sag in a 3-Phase system could be reduced, and the system was effectively restored by using DVR. From the simulation studies it was shown that the voltage source Multi-Level converter accompanying with the improved H-bridge control scheme can be applied for minimization of harmonics and also for the compensation of reactive power in custom power devices like DVR.

The control scheme used in this paper is a novel method that can restore the sag in a fraction of a cycle of the waveform through monitoring the direct axis voltage of the synchronously rotating frame. The digital simulation results are plotted against different fault conditions.

From the simulation results, it can be noted that the Multi-Level Inverter with H-Bridge based DVR is the most promising alternative for improving the power quality and resulting in the low harmonic output voltage. Hence, utilizing MLI gives better output voltage and lower harmonic level which intensifies the performance of DVR.

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