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Dielectrophoresis-assisted Integration of 1'024 Carbon Nanotube Sensors into a CMOS Microsystem

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Abstract

Carbon-nanotube (CNT)-based sensors offer the potential to detect single-molecule events and picomolar analyte concentrations. An important step towards applications of such nanosensors is their integration in large arrays. The availability of large arrays would enable multiplexed and parallel sensing, and the simultaneously obtained sensor signals would facilitate statistical analysis. We present a reliable method to fabricate an array of 1'024 CNT-based sensors on a fully processed complementary-metal-oxide-semiconductor (CMOS) microsystem. We developed a high-yield process for the deposition of CNTs from a suspension by means of liquid-coupled floating-electrode dielectrophoresis (DEP), which yielded 80% of the sensor devices featuring between one and five CNTs. We studied the mechanism of floating-electrode DEP on full arrays and individual devices to understand its self-limiting behavior. We characterized the resistance distributions across the array of CNT devices with respect to different DEP parameters. The CNT devices were then operated as liquid-gated CNT field-effect-transistors (LG-CNTFET) in liquid environment. Current dependency to the gate voltage of up to two orders of magnitude was recorded. Finally, we validated the sensors by studying the

pH dependency of the LG-CNTFET conductance and demonstrated that 73% of the CNT sensors of a given microsystem showed a resistance decrease upon increasing the pH-value.

The potential of carbon nanotubes (CNTs) as electronic sensors in liquid environments has been extensively demonstrated. The dependency of the conductance of CNTs on their electronic environment and the nanotube's high surface/volume ratio render them particularly suited for sensing applications in liquid phases. Furthermore, through functionalization of the CNTs, a specificity for numerous analytes can be achieved.[1–5]

Highly sensitive CNT nanosensors have been demonstrated in liquid-gate CNT field-effect-transistor (LG-CNTFET) configurations, where the carrier density of the CNT gate was controlled via a potential applied to the surrounding electrolyte.[6] By using LG-CNTFET sensors consisting of only a single or a small number of individual CNTs as sensing material, only few molecules are required to generate detectable signals. In the case of DNA hybridization, even the detection of a single molecule is possible.[7,8]

Despite their application potential in point-of-care diagnosis and label-free sensing, the widespread use of CNT nanosensor technologies is still hampered by technological hurdles. First of all, a route to fabricating large numbers of devices with reproducible characteristics has to be developed. Additionally, the high sensitivity of CNT sensors entails the presence of baseline fluctuations due to unspecific and random adsorption events, which are likely to create detection errors.[9] Finally, the limited adsorption area of single-CNT nanosensors leads to slow response times for low concentrations.[10]

A possibility to overcome some of these issues, without reducing the CNT sensitivity, includes the use of a large array of such nanosensors. The availability of multiple independent sensor units will increase the total adsorption area and reduce the response time without signal-averaging effects. Moreover, an array of independent devices with flexible selection capabilities will help to overcome the problem of non-uniform sensor responses and non-specific detection as statistical analysis methods can be applied. Additionally, the integration of an array of sensors

with differently functionalized devices or graded sensitivity will offer the possibility to multiplex sensor signals or to achieve a larger dynamic range. The use of an array will also offer the possibility to detect and select devices that have been functionalized through low-yield techniques, such as point functionalization.[11] Finally, a dense spatial integration of many sensors reduces the detection volume and external interference and even allows for spatially resolved detection of low-concentration analytes.[12] The most suitable way for monolithic integration of multiple nanoscale devices in arrays is the use of complementary-metal-oxide-semiconductor (CMOS) technology, as it enables the direct integration of the transducers with readout and amplification electronics in a dedicated microsystem.[13] However, a CMOS approach also introduces restrictions in the choice of materials and fabrication process steps (*e.g.*, temperature limitations), as CMOS compatibility has to be ensured.

Despite promising demonstrations of the integration of CNT devices into CMOS systems,[14–16] methods to reliably and reproducibly integrate CNTs into VLSI technologies are still lacking. Local catalytic growth of high structural quality CNTs requires high temperatures, and is, therefore, not compatible with CMOS-based substrates. A CMOS-compatible technique is the transfer of the CNTs from a growth substrate to the final devices. However, the use of this method can entail misalignment issues and a reduction in the yield of functional devices.[16] Another approach is the CNT assembly from a suspension (top-down). Its main advantage compared to local-catalytic-growth techniques is the possibility to functionalize or sort the CNTs before integration.[17,18] Among established top-down techniques, dielectrophoretic manipulation (DEP)[19] offers good directional and spatial control.[20] DEP is usually performed at room temperature, so that thermal compatibility with CMOS technology is ensured.[15,21] Through the use of specific electrode geometries and control of deposition parameters, DEP can be used to assemble devices ranging from single, individual CNTs to high-density carpets of CNTs with controlled orientation.[22] The position at which the CNTs are integrated can be precisely controlled in the micrometer range by the geometry of the DEP electrodes[23] and the inter-electrode spacing.[24] For integrating large numbers of single CNTs, self-limiting processes have been proposed, which includes the use of floating-potential electrodes by adding a series resistor[25] or capacitance[26] to the assembly circuit. A configuration that makes use of electrical coupling through the deposition medium has been proposed to obviate the necessity of a back gate electrode for assembly.[24]

In this study, we developed an individually addressable array of 1’024 CNT electronic nanosensors, each consisting of only one single or very few CNTs as sensing element. We focused on the development of a reliable fabrication process based on the floating-electrode DEP method to directly integrate the CNT devices into a CMOS system without the need to transfer them. We characterized large numbers of CNT devices to study the statistics and mechanisms of the self-limitation features of floating-electrode DEP. We finally integrated the system in a fluidic environment and characterized the sensor sensitivities to defined potentials applied through a liquid gate and to pH variations.

The custom-designed CMOS system used in this study has been described and characterized previously.[27] Applications of this microsystem for spatially (100 µm pitch) and temporally (up to 1 kHz) highly resolved electrochemical detection have been demonstrated.[12] The CMOS system is composed of an array of 1’024 electrodes, which can be connected to the readout electronics via an on-chip switch system by using two different routing modes. One routing mode connects electrodes in a row-wise fashion, whereas the other mode connects the electrodes to form 4x8 blocks. The routing provides additional selection flexibility as detailed in Rothe *et al*.[27] The integrated readout circuits facilitated current readout by means of on-chip amplifiers and analog-to-digital converters (ADCs) with a wide input range (100 pA – 10 µA). Each of the 1’024 electrodes was used as one terminal of the CNT sensor. The second terminal provided a connection to a common electrode, which was controlled by an on-chip voltage buffer or an external source. A block diagram of the system is presented in Figure 1a. The data stream was collected via a field-programmable gate array (FPGA) and transferred to a computer via USB. A dedicated interface has been programmed in LabView for operating the system and data acquisition. The CMOS system has been fabricated in a 2P4M-0.35-µm process. The full system chip size was 7.5x4.8 mm^2, while the electrode array located in the center occupied 3.2x3.2 mm^2 as shown in the micrograph in Figure 1b. The geometry of the DEP electrodes has been chosen so as to limit the number of parallel CNTs on each device and to make CNT integration on a wafer scale possible.[28] The principal layout is presented in Figure 1c. Two interdigitated platinum (Pt) leads (A and B in Figure 1c) have been designed to connect to a pattern of 32x32 electrode pairs at a pitch of 100 µm. One of the electrodes of each pair has been left floating and was capacitively coupled to the first Pt lead (A) through the suspension during DEP assembly. The second electrode has been directly wired to the second Pt lead (B). During DEP assembly,

the AC sinusoidal signal is applied between the two Pt leads (A and B). By using this geometry, the generated electric field gradient is maximized in the 5 µm gap between each of the 1'024 electrode pairs; the CNT assembly on each electrode pair is independent of the rest of the array.

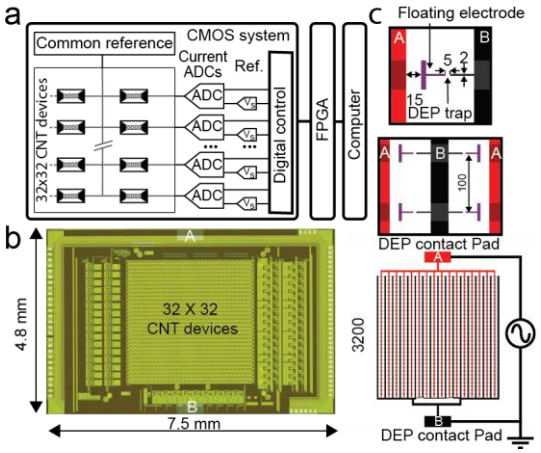

Figure 1: a. Block diagram of the CMOS system. All devices share a common reference electrode (V_d). Each CNT sensor can be selected individually and connected to the reference electrode and one of 32 on-chip current readout units. The user interface was implemented in LabView, the CMOS system was operated via an FPGA. b. Micrograph of the CMOS system. The 32x32 CNT array is located in the center of the chip, and the readout channels are located on either side. The contact for the DEP integration can be seen at the top and bottom of the system. c. Schematic view of the two interdigitated connector leads (A. red and B. black). The DEP AC signal is applied between A and B. These connector leads were used to create a local electric field gradient between each of the 1'024 electrode pairs (*i.e.*, a DEP trap). Each pair included a floating electrode (in purple) separated by 15 µm from the connector lead A and an electrode connected to connector lead B. The electrodes were 2 µm wide, and each pair was separated by a gap of 5 µm (all scales in µm).

CNTs have been synthetized by a catalytic chemical vapor deposition (CCVD) process. This synthesis route produced a majority of double-wall CNTs (DWNTs) of diameters ranging from 1 to 3 nm.[29] The extracted CNTs were then dispersed in de-ionized water using carboxymethyl cellulose as a surfactant. The concentration of the CNT suspension has been selected low enough to promote the integration of single CNTs. The solution was homogenized

before use. Typically, a CNT concentration of approximately 80 $\mu g.l^{-1}$ was used. The conductivity of the suspension was 2.5±0.7 $\mu S\ cm^{-1}$.

The fabrication steps to integrate CNTs have been realized by classic contact photolithography techniques and are schematically shown in Figure 2a-f. Briefly, two interdigitated Pt connector leads were patterned on the top passivation layer of the CMOS circuit (Figure 2a). A 1-µm thick passivation stack of SiO_2 and Si_3N_4 was deposited to protect the system from corrosion in liquid environments during sensing experiments. The passivation was etched away to open contact windows to the two interdigitated connector leads and the CMOS electrode for each pixel (Figure 2b). The 8'' wafers were then diced in individual CMOS microsystem chips. A second layer of Pt was patterned to fabricate the array of electrode pairs (Figure 2c). A layer of poly(methyl methacrylate) based photoresist (PR) was deposited to protect the microsystem regions outside of the electrode array from exposure to the CNT suspension during DEP deposition. A droplet of CNT suspension was added on top of the array, and a sinusoidal AC signal (5 to 20 V_{pp}, 300 kHz) was applied between the DEP contact pads (Figure 1c) to generate a positive DEP force on the CNTs. After assembly, the droplet was infinitely diluted with de-ionized water, and the array was dried with nitrogen (Figure 2d). A Pt layer was patterned to reduce the CNT/Pt contact resistance, to clamp the CNTs and connect the floating side of each electrode pair to the CMOS readout circuits (Figure 2e). As a top passivation a thick SU-8 layer was used. In order to promote the adhesion of SU-8 on the die and to allow for homogeneous coating, the gaps between the electrodes pairs, where CNTs were integrated, were first selectively protected with a patterned layer of PR. An oxygen plasma treatment was then performed before removing the remaining PR. The electrodes were afterwards protected with the 1-µm-thick SU-8 layer (Figure 2f).

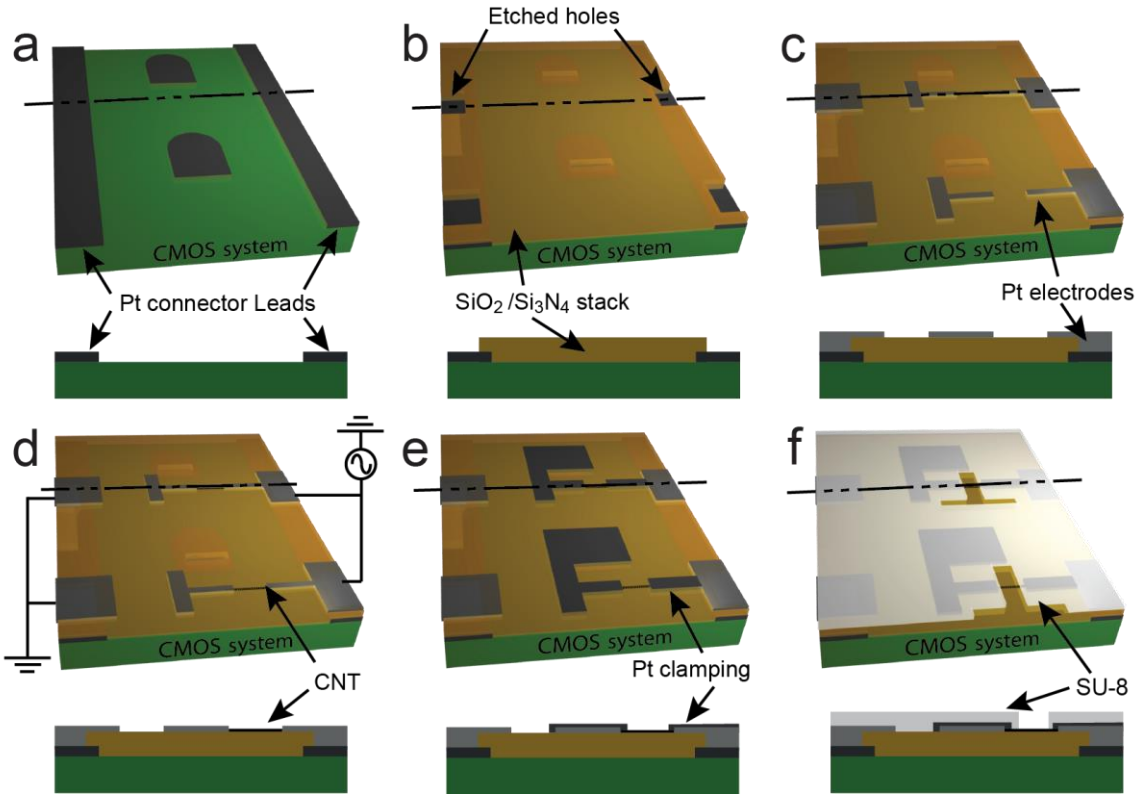

Figure 2: a. Pt interdigitated connector leads were patterned on the CMOS top passivation layer. b. The CMOS system is protected by a stack of SiO_2/Si_3N_4 and opening were etched. c. An array of Pt electrode pairs was patterned. d. CNTs were then integrated in between each electrode pair by using DEP. e. A Pt layer was added on the electrodes. f. The electrodes were passivated with a 1-µm-thick SU-8 layer.

Scanning electron microscope (SEM) images of the sensor array before SU-8 passivation are presented Figure 3a. The DEP process parameters have been selected to achieve the integration of a homogeneous number of CNTs across the electrode array. A single CNT can be observed in between two electrodes in the high-magnification SEM picture. The number of CNTs per device has been studied by using SEM. The distribution of the estimated number of CNTs is presented in Figure 3b. In this experiment, a DEP integration time of 60 min and a DEP signal of 20 V_{pp} at 300 kHz have been used. The result was that 80% of the electrode pairs have been connected through five or less CNTs. A subset of electrodes that had been connected with only few single CNTs was selected to compare the respective SEM pictures and atomic-force microscope (AFM) measurements. A comparison of a SEM picture and an AFM phase picture of

a selected CNT-connected electrode pair is shown in Figure 3c. The diameter distribution of the CNT bundles, measured by AFM, ranges from 3 to 20 nm (Figure 3d), which corresponds to an average of one to five CNTs per bundle.

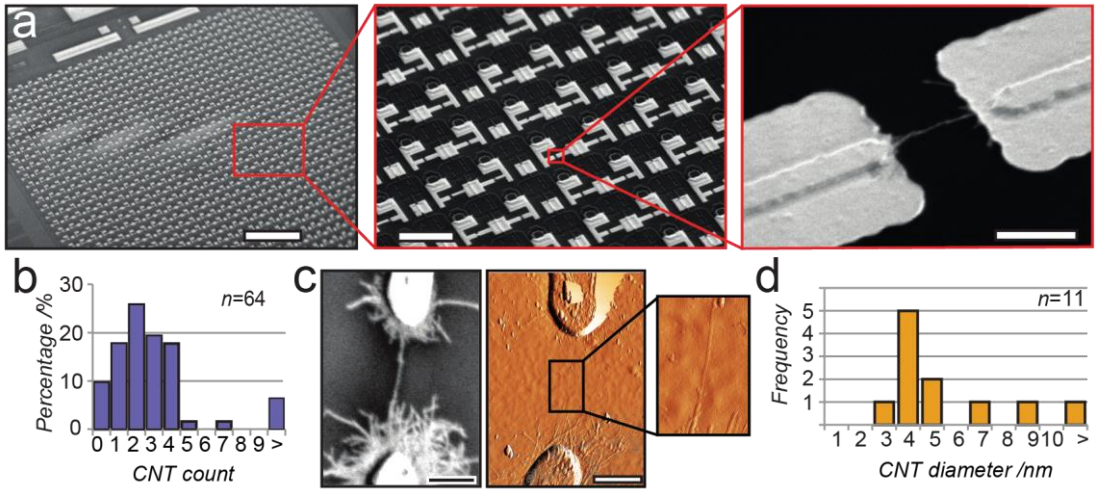

Figure 3: a. SEM picture of the CNT sensor array. An array overview can be obtained with lower magnification (scale bar 300 µm). The sensor pattern can be seen at medium magnification (scale bar 100 µm). At higher magnification, the two levels of Pt can be seen, and a CNT bundle between the electrodes becomes visible (scale bar 5 µm). b. Histogram of the number of CNTs deposited on 64 electrode pairs estimated by using SEM. c. Single CNT connection observed by SEM and compared to an AFM measurement (phase image, scale bar 3 µm). d. Diameter distribution of CNT connections as measured by using AFM.

The yield of electrodes interconnected by CNTs can be measured by using voltage-contrast SEM (VC-SEM).[30] The floating electrodes, which are connected to the common electrode through CNTs accumulate less charge during SEM imaging and appear darker than electrodes without CNT connection. VC-SEM has been previously used to study single connections or a few devices,[31,32] here we propose to use it for large CNT arrays. For this investigation, the DEP assembly has been stopped after every 5 min (10 V_{pp}, 300 kHz), the sample has been dried and VC-SEM has then been used to assess the CNT integration status over the full array. Figure 4a illustrates the VC-SEM technique by showing four SEM pictures of the same subset of CNT devices, taken after successive DEP deposition. The evolution of the number of connected devices can be directly observed. The four devices changed from "all

unconnected" at 15 min (floating electrodes appear white) to "all connected" at 45 min (floating electrodes appear black). The evolution of the total yield over time for 1'024 devices has been plotted in Figure 4b. For long enough deposition times, 100% of the DEP traps were filled with dense CNT assemblies (several tens of CNTs). To understand the CNT assembly dynamics on a single device scale, the evolution of connections over time has been followed via SEM. Results are presented in Figure 4c and d. A few oriented CNTs that connect the electrodes can be seen in the center of the DEP trap in Figure 4c. In Figure 4d, three successive SEM pictures have been colorized and superimposed so as to demonstrate the evolution of the DEP-induced CNT assembly over time. After the initial CNT assembly, CNTs are preferentially attracted to the edges of the grounded electrode. These observations are coherent with the previously reported hypothesis of a limitation mechanism for floating-electrode DEP, controlled by modification of the local electric field distribution during the assembly process.[28] This assembly characterization experiment has been repeated on different electrodes pairs and for different DEP parameters with similar results.

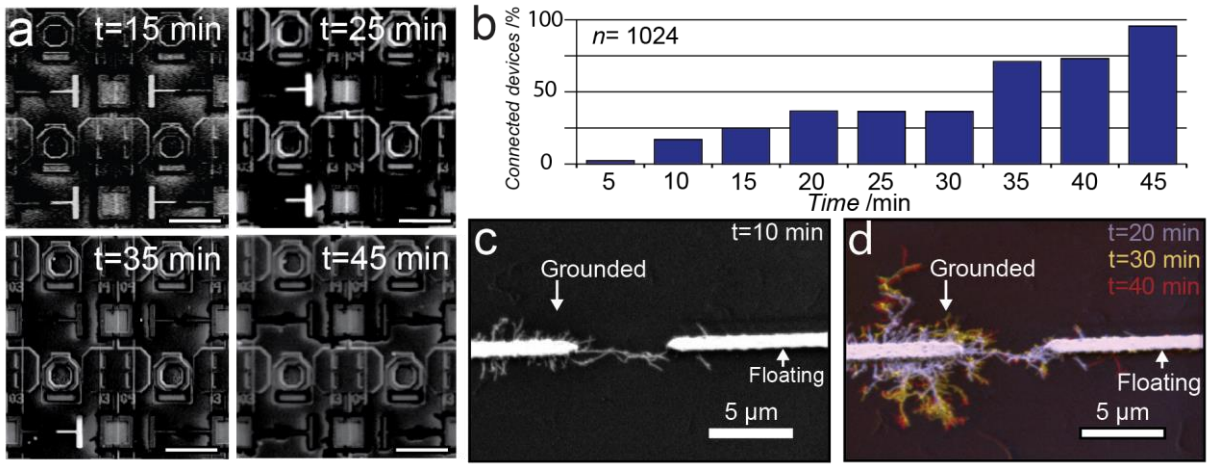

Figure 4: a. VC-SEM images of a subset of four devices at different times (15, 25 35 and 45 min) during the DEP assembly process (10 V_{pp}, 300 kHz) (Scale bar: 50 µm). b. Evolution of the yield of 1024 electrode pair versus DEP time as monitored by VC-SEM. c. SEM picture of a specific connection after 10 min DEP deposition (10 V_{pp}, 300 kHz). d. Superposition of colorized SEM pictures of the same connection after different DEP deposition times (20, 30 and 40 min).

After the clamping and packaging steps, the CMOS circuitry enables the sequential current readout of all 1'024 CNT devices via 32 simultaneously useable signal amplification channels. To characterize each device, the potential of the common drain electrode (V_d) was fixed to a certain value, and the source potential (V_s) was swept in reference to the drain electrode potential from -0.2 V to 0.2 V. The current between source and drain (I_{ds}) was measured for every pixel through the readout channels. The corresponding resistance was calculated by linear regression of the I_{ds}/V_{ds} characteristics of the devices between -20 mV and 20 mV. A typical subset of I_{ds}/V_{ds} characteristics of a row of CNT sensors has been plotted in Figure 5b. The corresponding representation of the spatial distribution of the device resistances of a CNT sensor array is shown Figure 5a. Each pixel in this image corresponds to a CNT device with the resistances represented in colors. Devices for which no current were measurable with our setup are referred as non-connected (NC). Resistance values were usually quite homogeneously distributed over the array. Local inhomogeneity has been occasionally observed and then could be associated with improper handling of the suspension droplet during the DEP deposition process. A histogram of the obtained resistance values for this specific array has been plotted in Figure 5c. The distribution ranges from a few tens of kΩ to a few MΩ. A subset of device resistance values has been compared to the respective number of CNTs as obtained through SEM measurements per device (Figure 5d). As expected, the resistance was lower when a larger number of CNTs was found. For devices featuring a single CNT, a resistance on the order of a few MΩ to a few tens of MΩ has been observed. The measurement results reflect the type of CNTs that has been used for this study. The CNTs have not been sorted and, thus, contain both, semi-conducting and metallic CNTs. The resistance distributions were comparable to that of previously investigated CCVD DWNT samples.[23,33] For arrays with denser arrangements of parallel CNTs, resistances in the range of a few kΩ to a few tens of kΩ have been measured.

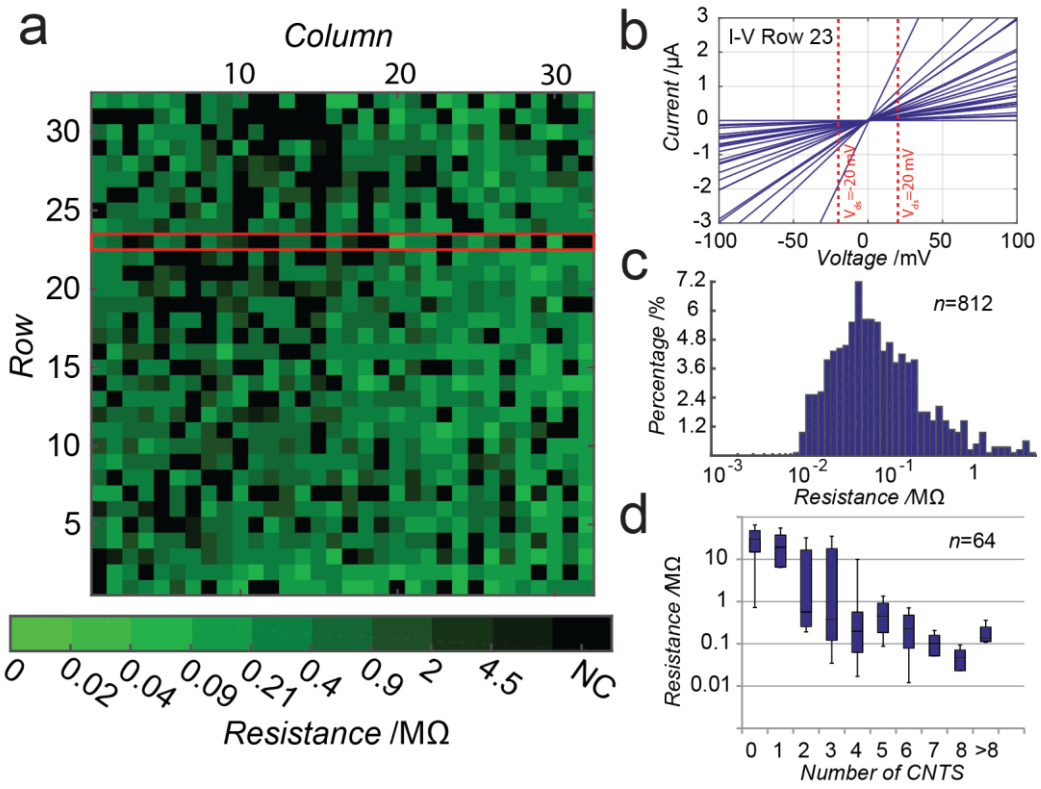

Figure 5: a. Map of device resistances of a fabricated CNT sensor array. (NC = Non-connected devices) b. I_{ds}-V_{ds} characteristics of all the CNT devices of one selected row of the array (row number 23). The resistance has been calculated between -20 mV and 20 mV. c. Histogram of the resistance values of the full array. d. Correlation between the numbers of CNTs connecting the electrodes as observed by SEM and the measured resistances of the CNT devices.

The advantage of the DEP-assisted integration approach is the ability to control the sensor property distribution through variation of CNT suspension and assembly parameters. The influence of the DEP assembly parameters (time and amplitude) on the sensor resistance distribution has been investigated (Figure 6). For a given deposition time (60 min), an increase in the DEP signal amplitude leads to a narrower distribution and lower values of resistances, as has been demonstrated for three deposition voltages in Figure 6a (10, 15 and 20 V_{pp}). Lower resistance values (<10 kΩ) are obtained upon deposition of large bundles of CNTs (>10), which explains the narrower distributions. In case of the largest applied voltage (20 V_{pp}), nearly 100%

of the devices were found to be connected through CNTs. In a similar way, the influence of the DEP assembly duration has been studied using a constant signal amplitude (20 V_{pp}) and three different deposition times (10, 30 and 60 min) (Figure 6b). As expected, using a longer deposition time leads to lower device resistances and a narrower resistance distribution. Finally, the DEP assembly has been conducted on two different arrays using the same parameters (15 V_{pp}, 60 min, Figure 6c). Upon repeating deposition experiments with the same parameters, the observed resistance distributions were fairly similar.

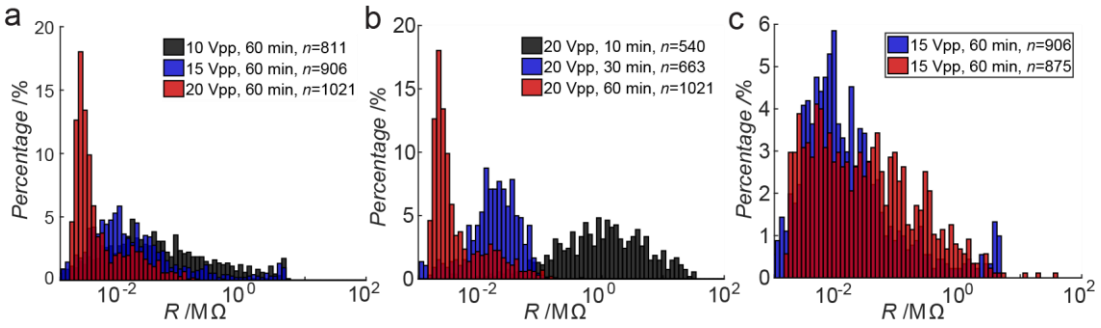

Figure 6: Histogram of the sensor resistance distribution in several different chips. a. Influence of the DEP assembly signal amplitude on sensor resistance distribution. b. Influence of the DEP assembly duration on sensor resistance distribution. c. CNT Assembly on two different chips with identical DEP parameters (15 V_{pp}, 60 min).

The sensitivity of the electronic CNT sensors was directly correlated to the influence of the liquid environment on their conductivity. The dependency of the I_{ds} current on the liquid-gate potential (V_{lg}) was measured in phosphate-buffered saline (PBS) for different values. The CNT devices were configured as LG-CNTFETs. A schematic view of the device configuration is shown in Figure 7a. A constant voltage was applied between the drain and source electrodes (V_{ds}) and the drain current (I_{ds}) was recorded while V_{lg} was swept. Characteristic values obtained from a CNT device and recorded via the CMOS interface are presented Figure 7b. In this case, I_{ds} values upon varying V_{lg} from -1 V to 0.7 V have been plotted for different V_{ds} ranging from 20 mV to 120 mV. When used as sensors, the sensitivity of an LG-CNTFET is highest when the transconductance ($gm=\Delta I_{ds}/\Delta V_{lg}$) is maximum.[34] The value of g_m has been measured for all the sensors on a chip. The variation of I_{ds} and g_m for a selected sensor has been plotted in Figure 7c. For this specific sensor, I_{ON}/I_{OFF} = 4.6 for V_{ds} = 0.1 V and g_m present a local maximum for V_{lg}

= -0.27 V (-0.6 V < Vlg < 0.2 V). A similar local maximum of g_m has been measured in 22% of the functional devices at an average gate voltage of V_{lg} = -0.42 V. To study the behavior of the sensors over the full array, we defined I_{ON} as the value of I_{ds} for V_{lg}= -0.6 V and I_{OFF} as the value of I_{ds} for V_{lg}= 0.2 V. The correlation between I_{ON} and I_{OFF} over the full array can be used to deduce the nature of the CNT devices (semi-conducting or metallic). The correlation between I_{ON} and I_{OFF} values of each array of sensor has been plotted in Figure 7d. Figure 7e shows the distribution of the I_{ON}/I_{OFF} ratio for all sensors. A large variety of characteristics have been observed: pure metallic behavior (I_{OFF} = I_{ON}), devices with a large I_{ON}/I_{OFF} ratio exceeding two orders of magnitude, and a large number of devices with a low ratio of I_{ON}/I_{OFF}. The larger I_{ON}/I_{OFF} ratios are comparable to those previously reported for single-semi-conducting-CNT LG-CNTFETs.[34] The obtained spread of the CNT characteristics and resistance values corresponds to what would be predicted for sensor assembly from a mixture of semi-conducting and metallic CNTs without prior sorting. The lower spread for devices with the highest I_{OFF} values can be explained by the fact that resistance characteristics average over a larger number of parallel CNTs.

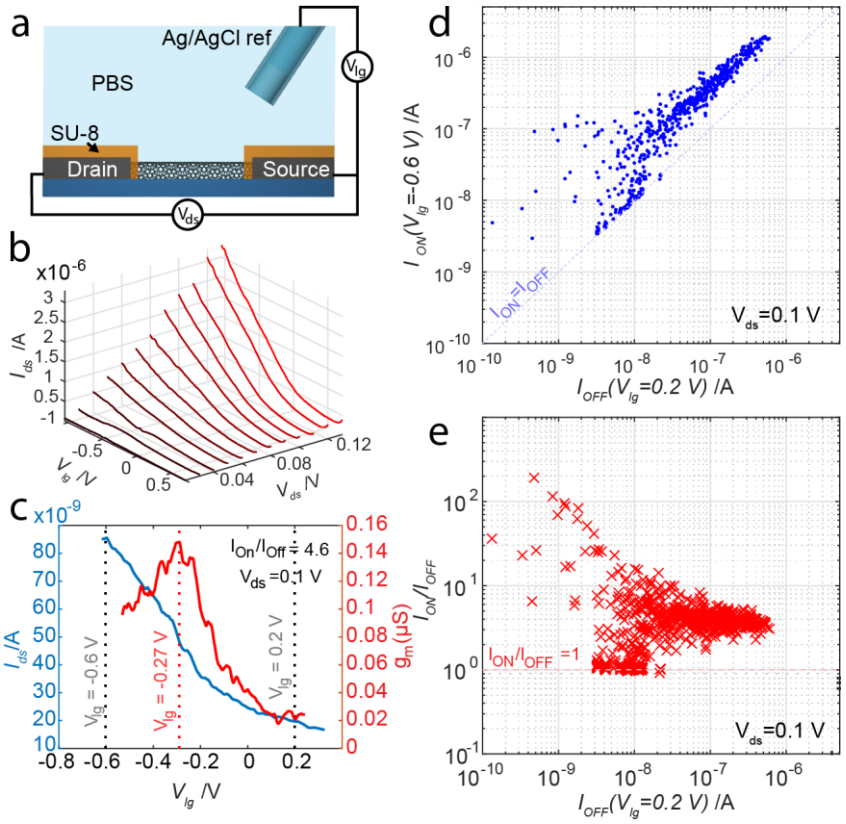

Figure 7: a. Schematic of the LG-CNTFET. An Ag/AgCl reference electrode is used to control the liquid potential above the CNT devices. The electrodes were protected with a SU-8 layer, and only the CNT channel was exposed to the liquid environment. b. I_{ds} versus V_{lg} plots of a LG-CNTFET for different V_{ds} ranging from 20 mV to 120 mV. c. I_{ds} versus V_{lg} plot of a sensor for V_{ds} = 0.1 V (blue) and plot of the corresponding transconductance g_m versus V_{lg} (red). A local maximum was observed at V_{lg} = -0.27 V for this device. d. Scatter plot of the current variation over all array sensors between V_{lg} = 0.2 V (I_{OFF}) and V_{lg} = -0.6 V (I_{ON}). e. Ratios of I_{ON}/I_{OFF} versus I_{OFF}.

To test sensor device sensitivity to changes in the liquid environment, the dependency of I_{ds} on the solution pH has been studied by using phosphate-citrate buffered solutions. The solutions were successively injected in the fluidic chamber atop the sensor array, and I_{ds} was continuously measured while V_{lg} was set to -0.4 V. The resistance of all sensors has been first measured in a pH 8 solution and, then, in a pH 5 solution. Figure 8a shows the histogram of the relative variation of I_{ds} across all sensors of the chip. 73% of the functional sensors showed an

increase in the resistance. As the CNTs used for this study have not been oxidized or chemically modified, the CNT conductance exhibited a relatively low sensitivity to pH, as has been previously reported.[16] The large variation in the response to the pH change can be, again, attributed to the spread in the CNT properties. The flexibility of the presented array system in sensor selection, along with the large number of available sensor devices can help to overcome the issue of a large spread in sensor properties. After the first pH experiment, we selected the most sensitive sensors per readout channel, which yielded a subset of 27 sensors. In Figure 8b, we present the average responses of those sensors to 8 successive medium changes with pH values ranging from 4 to 8. An average response of 2.4 nA/pH has been recorded in this case. The pH values have been stepped from 4 to 8 and back to 4 to show the reversibility of the sensing process. Finally we studied the stability of our sensors, using a second sensor array, during successive exposure to pH 8 and pH 5 solutions. In Figure 8c, we present the normalized response of a subset of 10 sensors selected using the same protocol as the previous experiment. The CNT sensors proved to be stable over time and during the experiment cycles.

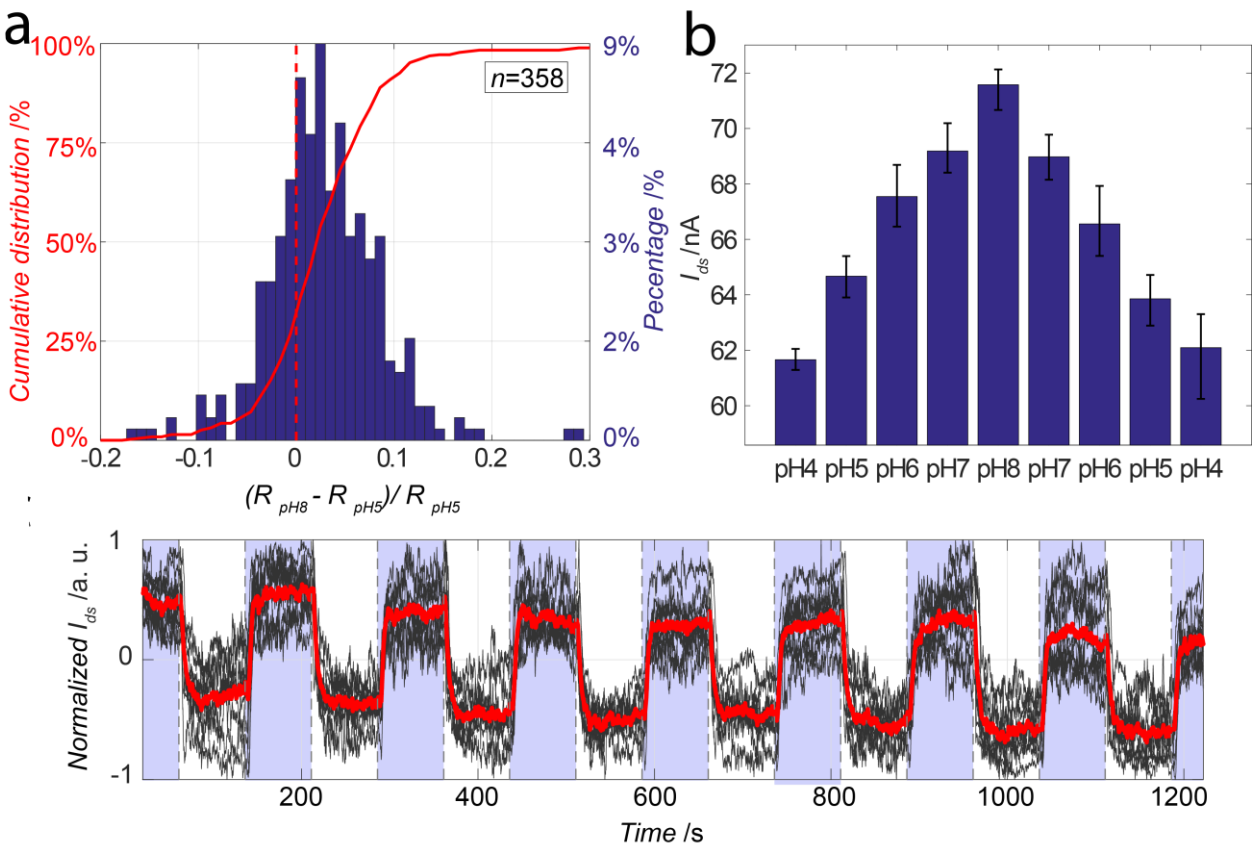

Figure 8: a. In red, left axis, cumulative distribution of the resistance variation of all sensors of an array upon exposure to pH 8 and pH 5 solutions. In blue, right axis, corresponding histogram. b. Averaged I_{ds} for a subset of 27 sensors upon exposure to solutions of different pH. I_{ds} was recorded during 100 s before changing the solution pH. c. Normalized I_{ds} values versus time for 10 sensors (black) and averaged response (red) during successive alternations between pH 8 (blue) and pH 5 (white) solutions using another sensors array.

Single CNT-based sensors, fabricated by DEP, have previously been reported on. A straightforward way to achieve more specific analyte sensing using the CNT sensor array would include to control the nature of the integrated CNTs by either sorting them based on their electronic properties or by performing a functionalization step prior to integration by means of DEP, as has been described in *Hennrich et al.*.[18] A second route is to functionalize the CNT surface after DEP integration on the CMOS system.[35,36]

CONCLUSION

We have demonstrated the potential of using a DEP-based protocol for the parallel deposition of CNTs on electrode pairs of a CMOS system. We developed an interdigitated floating-electrode configuration to fabricate 1'024 independent CNT devices on a CMOS array in parallel. We developed a monolithic system that features 1'024 independently selectable devices and a parallel readout of 32 devices through on-chip amplification and signal-conditioning circuitry channels. By using VC-SEM techniques, we have, for the first time, monitored the time course of CNT deposition on large scale by means of DEP. We studied the dependency of the sensor device properties on the applied parameters. The trade-off between achieving a high overall yield of functional devices and having only a small numbers of parallel CNTs per electrodes pair has been established by using arrays with several hundreds of devices. We finally demonstrated that the DEP-based integration technique is suitable for the fabrication of large arrays of CNT sensors: we characterized the fabricated CNT-FETs in measuring the pH of different analyte solutions. As our integration process depends on DEP, additional chemical processes to better control and select the CNTs according to their nature before assembly can be applied.[18] Further on-chip micro control of the DEP could render the integration process more flexible.[37] Moreover, CNT and sensor surface modification techniques to enhance sensor selectivity can be applied after integration, similar to those reported for single CNT devices or CNT carpet-based devices.[1]

Experimental Section

Suspension preparation

CNTs have been synthetized by a catalytic chemical vapor deposition (CCVD) process. $Mg_{0.9}Co_{0.1}O$ solid solution was used as starting material to catalyze the decomposition of CH_4 at 1000°C in a reducing atmosphere (CH_4:H_2). The catalyst was then dissolved in a non-oxidizing HCl treatment.[29] The extracted CNTs were dispersed in de-ionized water using carboxymethyl cellulose as a surfactant and CNTs at a ratio of 1:1 and an ultrasonic homogenizer (VCX-130, SONICS). The CNTs were stored in a suspension at a concentration of about 80 $mg.l^{-1}$. This

suspension has been diluted 100 times, sonicated (30 min, 90 Watt) and centrifuged at (150,000 rpm, 30 min). Afterwards 10% of the volume at the top were extracted. The last dilution was performed 24 h before each DEP deposition process.

Fabrication process

The connector leads have been patterned by deposition and subsequent ion-beam etching of tungsten-titanium (WTi) (50 nm) and Pt layer (270 nm). The SiO_2 and Si_3N_4 has been deposited by chemical vapor deposition process and etched by reactive-ion etching. The second and the last layer of Pt have been deposited by ion-beam assisted sputtering (Elionix E-220, 120 nm) and patterned respectively by ion etching (Elionix E-220) and lift-off (OFPR 800 PR). The devices protection has been done with a 1 µm SU-8 layer (SU8-2 Microchem, coating 1000 rpm).

Packaging

An encapsulation and packaging method has been developed to allow for controlled liquid flow over the sensor array. The microsystem was first glued and wire-bonded onto a printed circuit board (PCB) that, in turn, was plugged on a 40-contacts card connector The card connector was interfaced with the FPGA control board (Figure 9a). Two epoxy encapsulants of different viscosities (G8345-29 and G8345D-37 from NAMICS) were used to protect the bonding wires while exposing the sensor area to the liquid environment (Figure 9b). A robust fluidic chamber (about 12 µL) was fabricated by using a preformed polydimethylsiloxane (PDMS) sheet, clamped between two poly(ethyleneterephtalate) (PET) supports (Figure 9c). One or two liquid inlets, one outlet and an Ag/AgCl reference electrode were connected to the chamber through the PET upper plate.

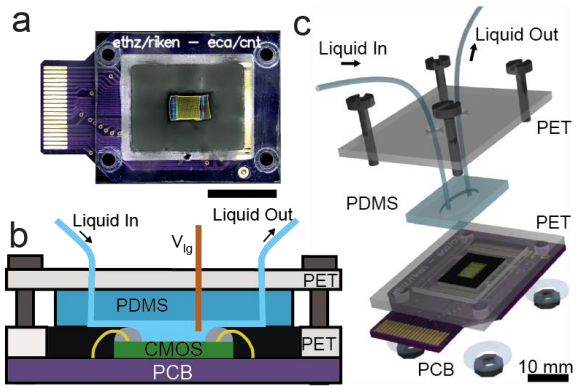

Figure 9: a. Picture of the CMOS system packaged on the PCB (scale: 10 mm). b. Cross-sectional view of the packaged system. The two components of the chip encapsulation, the grey dams, and the black fill material can be seen along with the green CMOS die and the yellow bond wires. c. Exploded 3D view of the fluidic system.

Characterization techniques

SEM imaging was performed with a Keyence microscope (VE-8800) using a low acceleration voltage (V_{acc}) (1-2 keV). A tilt angle (30-45°) was used for CNT observation in order to improve the contrast. VC-SEM was performed at a higher V_{acc} of 10 keV without a tilt angle. AFM measurements have been performed on a JPK Nanowizard using an intermittent contact mode. The software ImageJ was used to perform the SEM image colorization and superimposition showing the CNT integration in Figure 4c.

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