31st Annual AIAA/USU Conference on Small Satellites, 10AUG17

CHREC
NSF Center for High-Performance Reconfigurable Computing

SSIVP

Spacecraft Supercomputing Experiment

For STP-H6 on ISS

Investigators and Students

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Gary Crum, Tom Flatley – NASA Goddard Space Flight Center

Research Partners

DoD Space Test Program & CHREC Consortium Members

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Outline

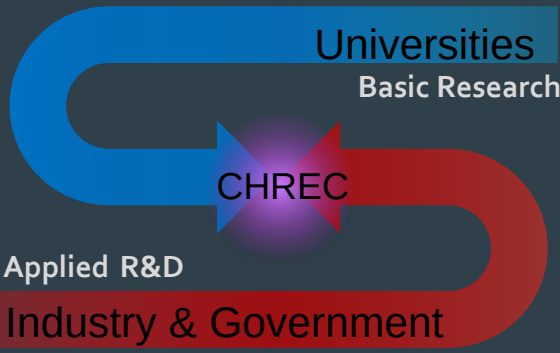
- Acknowledgements and Programs
- Technology and CSP Concept
- Mission Design & Architecture
  - Goals and Objectives
  - Hardware & Software
- Mission Computing & Sub-Experiment
  - Parallel & Reliable Computing
  - GaN Sub-Experiment
- Conclusions

Acknowledgements & Programs

Acknowledgements

- SSIVP is a research mission at Pittsburgh CHREC Site
  - NSF Center for High-Performance Reconfigurable Computing (**CHREC**)
    - Founded in 2007
    - Comprises 4 university sites and **over 30 industry and government** partners
- SSIVP is collaborative effort
  - Builds on success and experience of STP-H5/CSP experiment
  - Key development partners:
    - DoD Space Test Program
    - NASA Goddard Space Flight Center
    - University of Pittsburgh's – Mechanical Engineering and Materials Science Department & Electric Power Systems Laboratory

National Science Foundation
WHERE DISCOVERIES BEGIN



See **www.chrec.org** for more info

Space Test Program

Space Test Program – Houston

- Provides sole interface to NASA for all DoD payloads on International Space Station (ISS)
- Provides timely spaceflight, payload readiness, management, and technical support for safety and integration

History of Mission Success

- Build upon successes of HREP, MISSE 6/7/8, STP-H3, STP-H4, STP-H5 while incorporating valuable lessons learned
- STP in-house contractor (MEI Technologies) expertise allows for aggressive 2-year build/integration schedule
- Aerospace Corp provides assistance to Houston team with leadership and mission assurance roles

Image Courtesy DoD Space Test Program

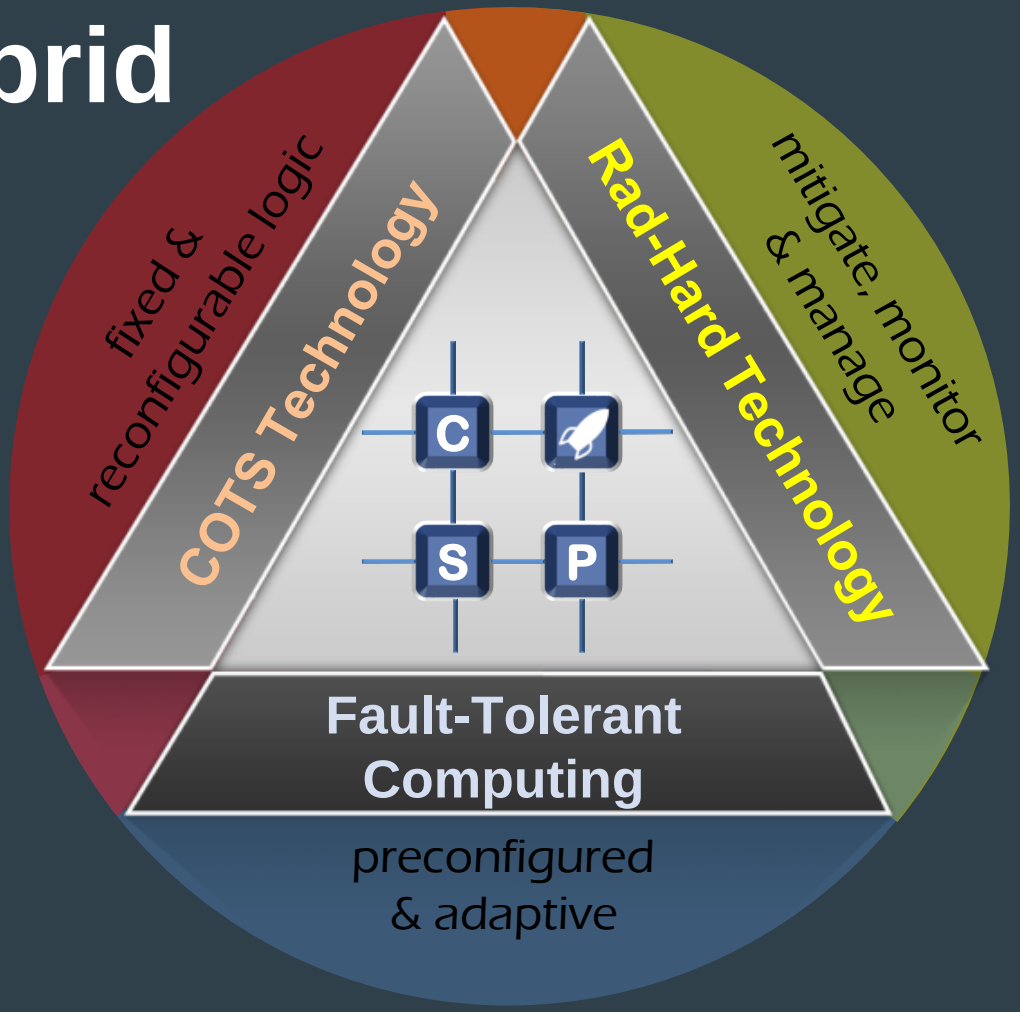

Technology and CSP Concept

CSP The Concept

Multifaceted Hybrid

Space Computing

- **Hybrid processor** (multicore CPU + FPGA subsystem)
- **Hybrid system** (commercial + rad-hard)
- **Robust Design** (Novel mix of COTS, rad-hard, & FTCA)



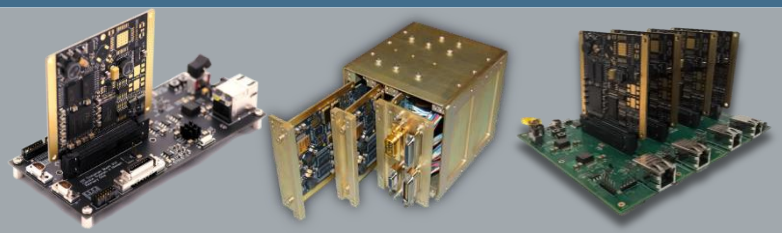
CHREC Space Processor (CSPv1)

Easy Development with CSP

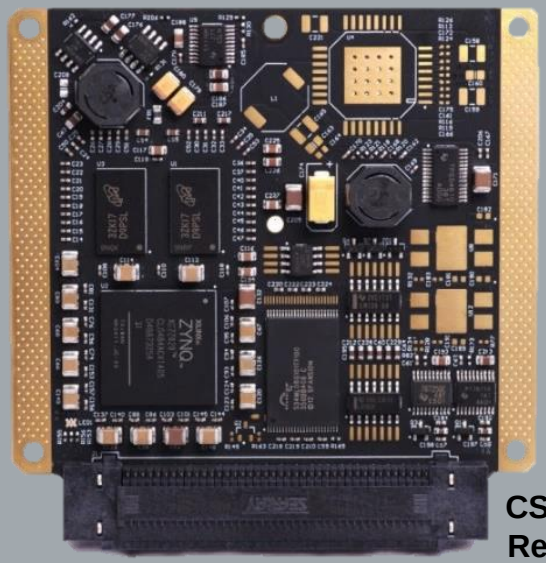
- Selective component population scheme supports Engineering Model (EM) and Flight Design
- Rapid and cost-effective design prototyping using evaluation kit or Zedboard / Zybo / Pynq board
- Downloadable example software designs and configurations (Linux/RTEMs cFE etc…)

Specifications:

- Xilinx Zynq 7020 (ARM dual-core Cortex-A9 + Artix-7 FPGA)
- (1-4) GB NAND Flash
- (256 MB–1 GB) DDR3
- Dedicated Watchdog Unit
- Internal Power Regulation
- 26 Configurable ARM GPIO Pins
- 12 Single-Ended FPGA I/O Pins
- 24 High-Speed Differential Pairs



Eval Kit | STP-H5 Flight Unit | SuperCSP



CSPv1 Rev. B

Flight Heritage on STP-H5, Radiation & Env. Tested

Order at spacemicro.com

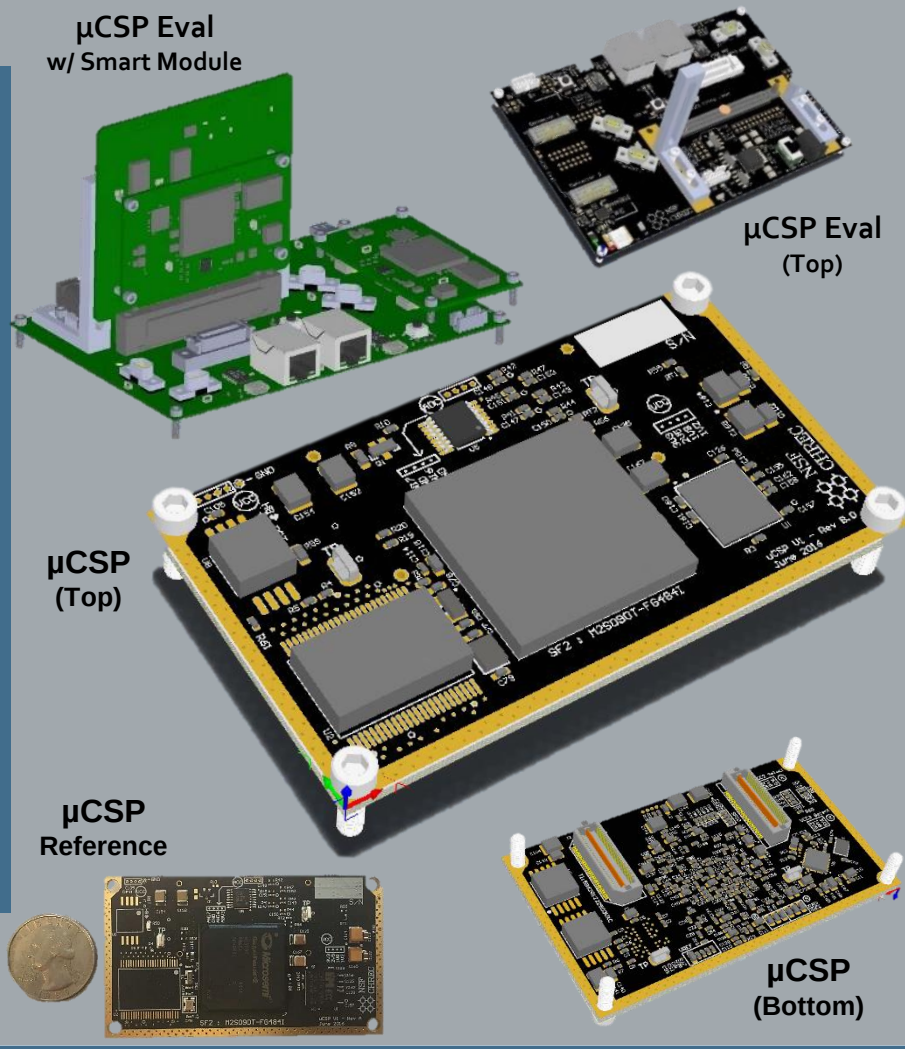
µCSP Rev. B Flight Computer

Even Smaller Solutions…

- Multifaceted hybrid processor at center of CSP Concept
- Even lower SWaP-C profile than CSPv1 for small spacecraft missions
- Provided template for “Smart Module” designs

Specifications:

- SmartFusion 2 (ARM Cortex-M3 + FPGA)
- 64 Mb NOR Flash
- 1 Gb LPDDR3
- Dedicated Watchdog Unit
- ADC for board temp and 2 ch. For flyleaded measurements



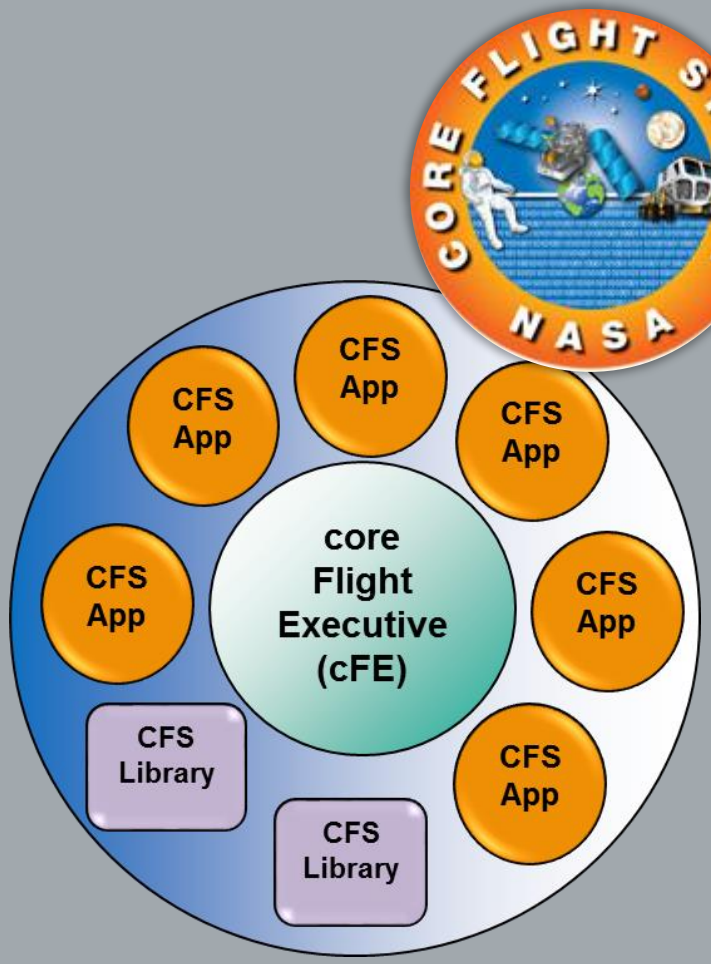
Core Flight Executive

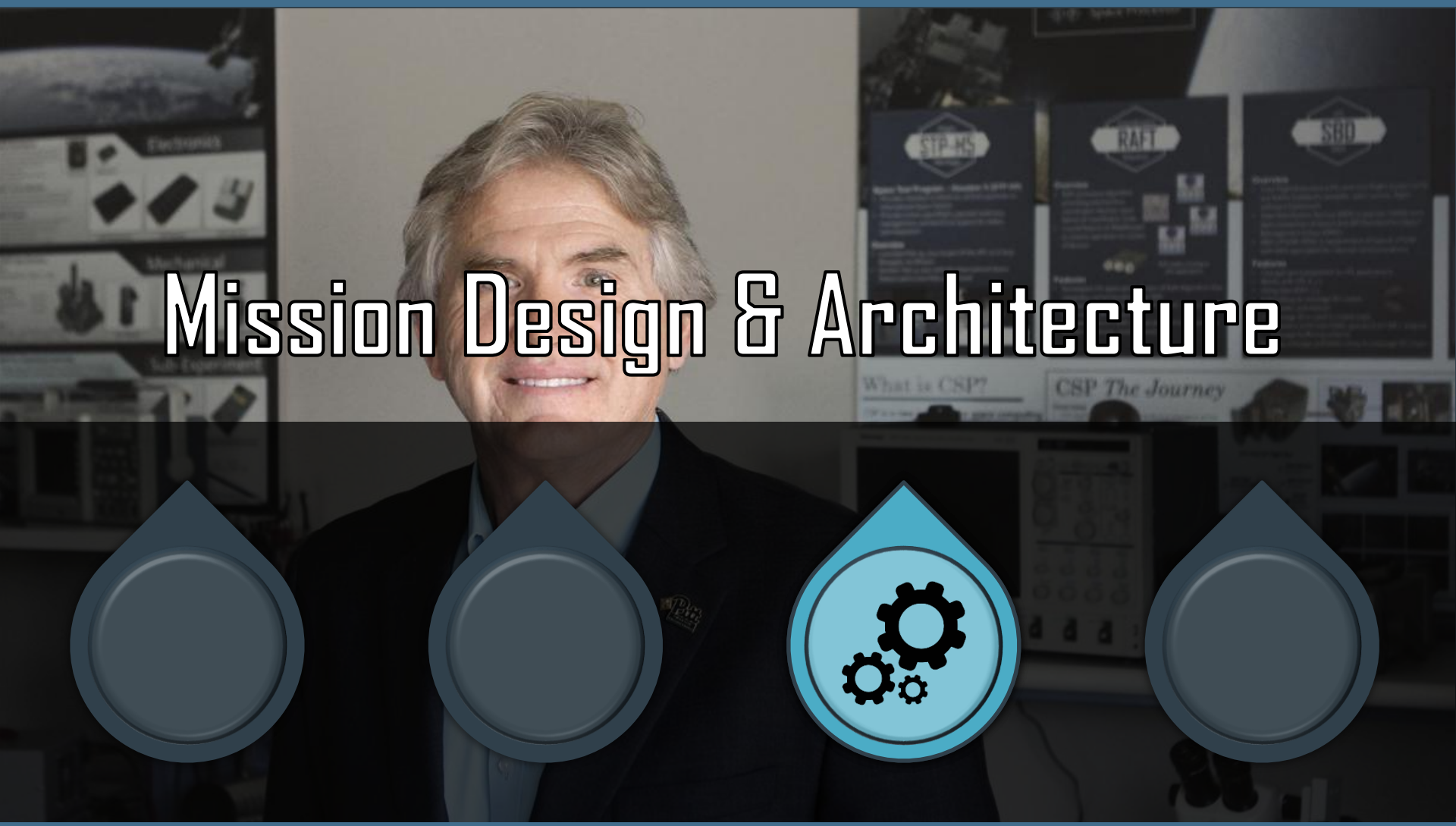
Description

- NASA Goddard's **reusable** flight-software framework
- Open source version of cFE and cFS **available at SourceForge**
- Additional information at **cfs.gsfc.nasa.gov** and **coreflightsoftware.org**
- Perform local device management, software messaging, & event generation
- **Flight heritage** on multiple missions, but specifically STP-H5/CSP

Core Components

- Core Flight Executive (cFE)
  - Mission-independent software services
- Core Flight System (cFS)
  - Applications and libraries running on cFE



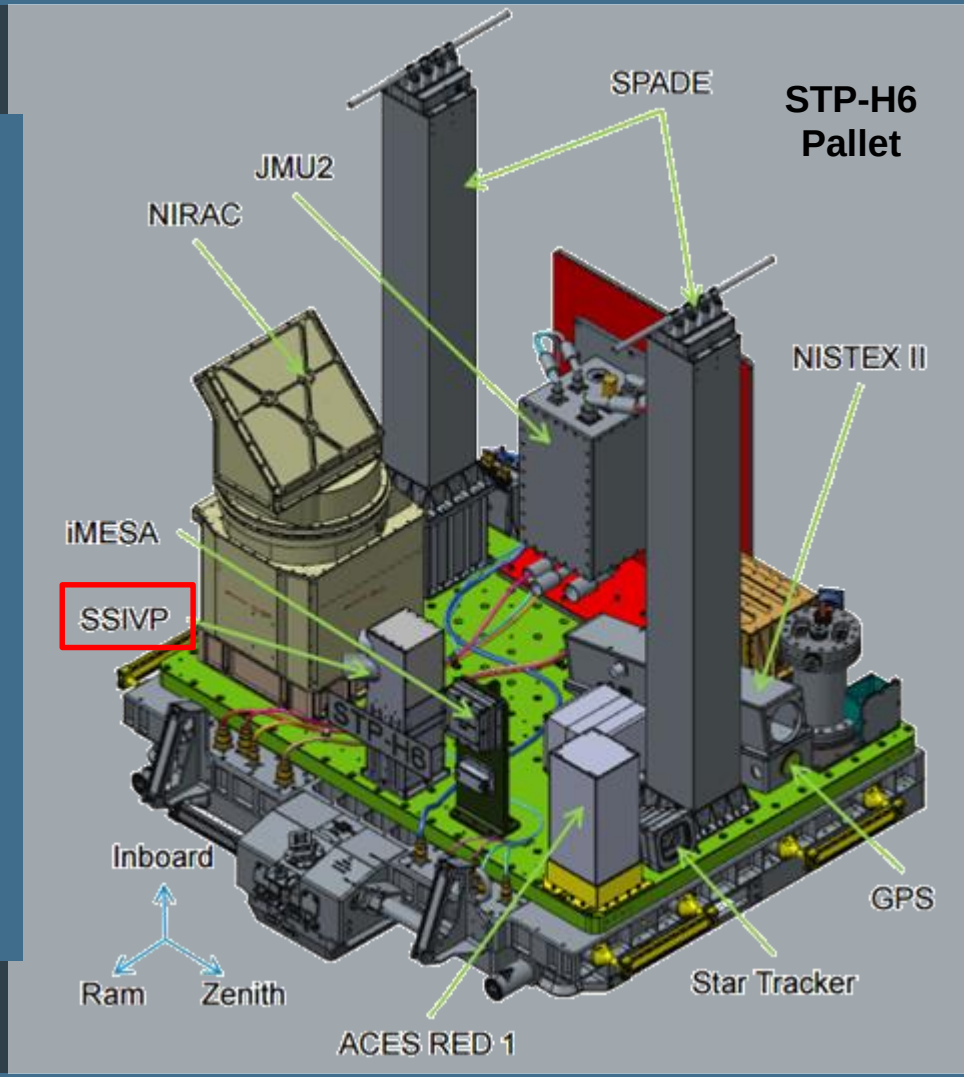

Mission Design & Architecture

SSIVP Introduction

Motivation

Develop, demonstrate, and evaluate next-gen technologies for space supercomputing, featuring image and video processing

- Run parallel jobs and apps from ground (just like those sent to HPC center), but to cluster in space instead
- 3U computing payload (5 CSPs, 1 µCSP, Power, Backplane) 2 image sensors
- SSIVP will evaluate several GaN HEMTs and controllers



STP-H6 will be integrated and flown under the management and direction of the Department of Defense Space Test Program Human Spaceflight Payloads Office. Image Courtesy DoD Space Test Program.

STP-H6 Location

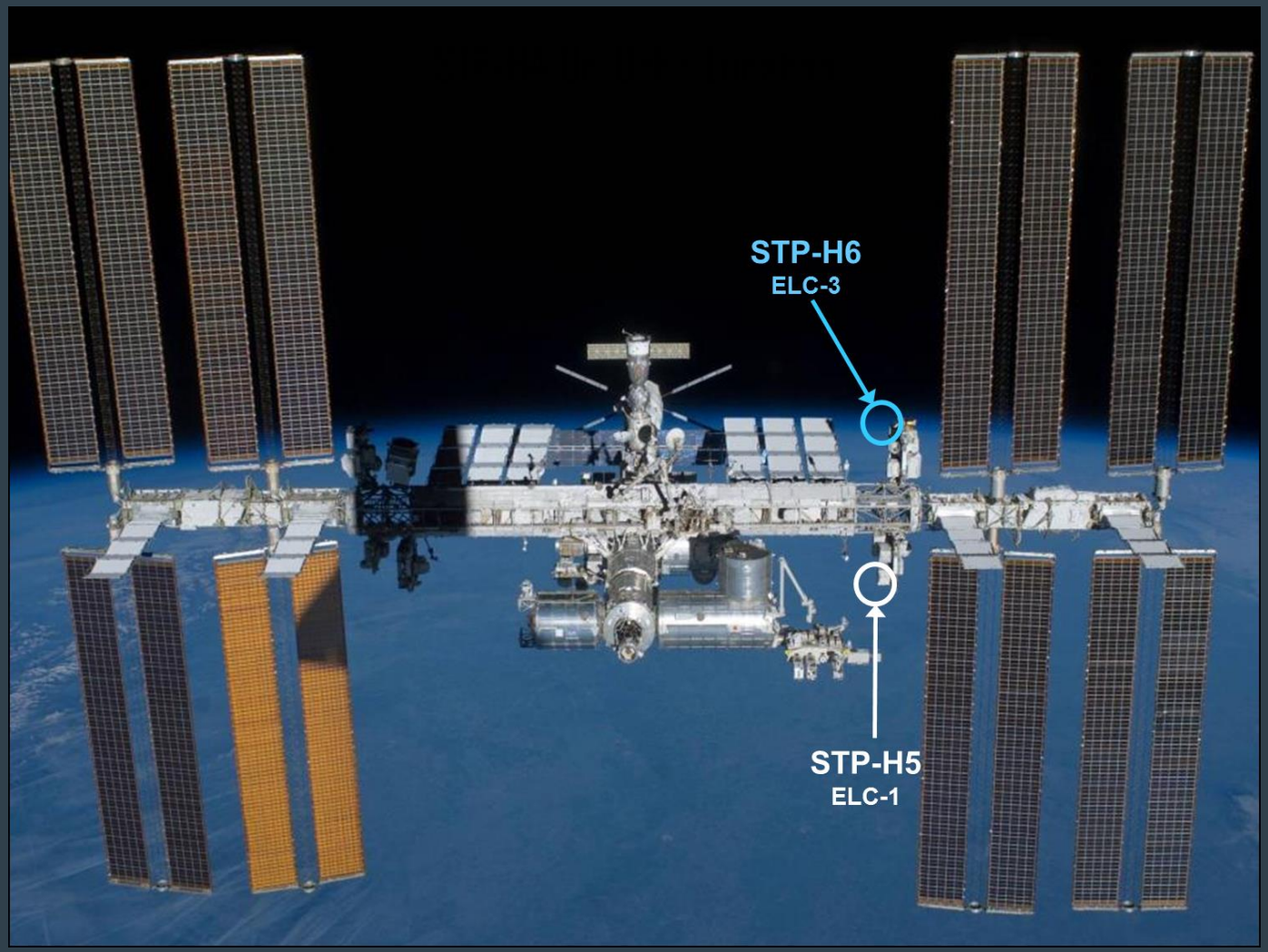


Image Courtesy DoD Space Test Program

SSIVP Specifications

Main Assembly

- Mass: ~9.5lbs

Power Interface

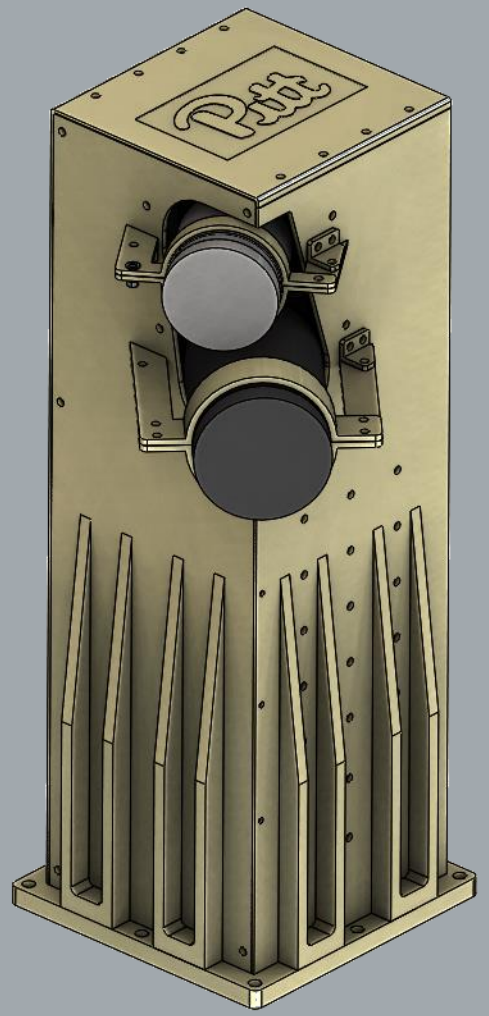
- Max SSIVP (All Cameras / Full Processing): 30.22 W
- Nominal Power: 26.10 W
- Min (Cameras Off): 17.02 W

Data Interface

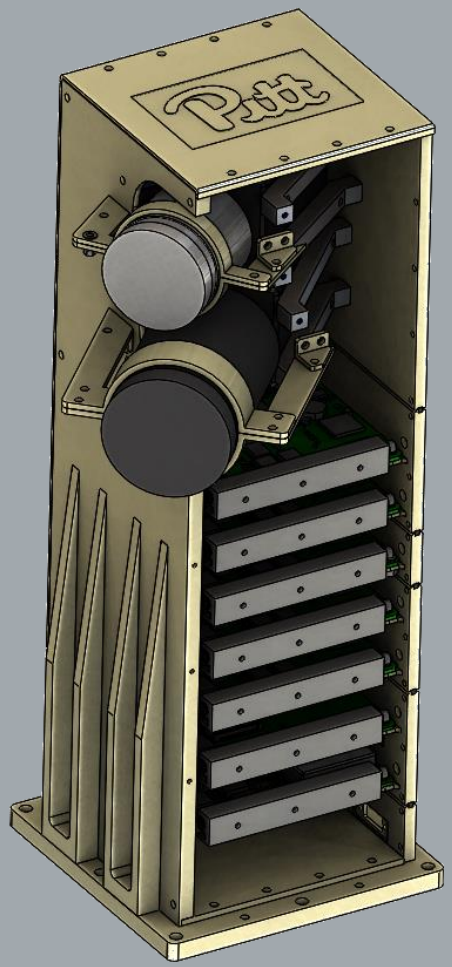
- Data rate: 931Kbaud / 737.28 kbps
- Average throughput: 737.28 kbps / 2 kbps

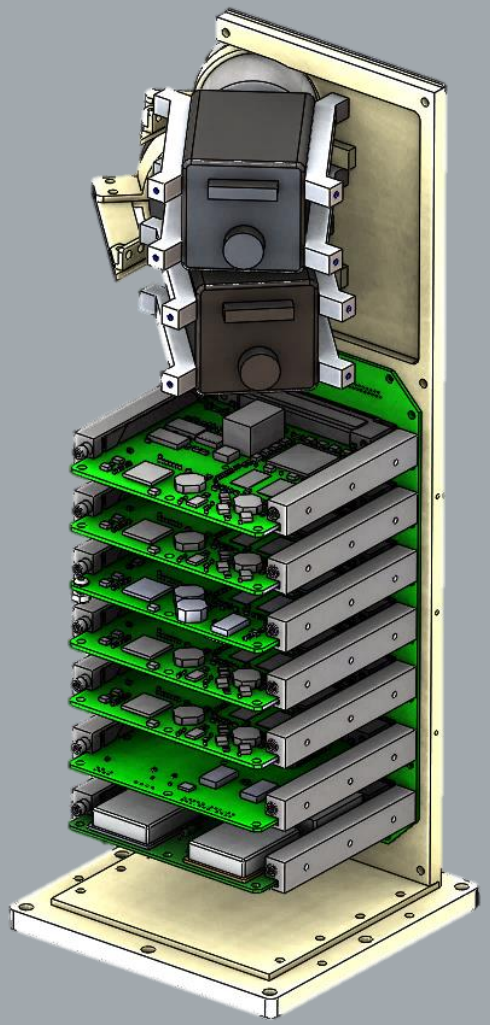
Debug Interface

- Capped for flight: Debug signals for 5 CSPv1s UART, 1 uCSP UART, Power Good, Heart beat and 2 JTAG Ports, 3 total connectors

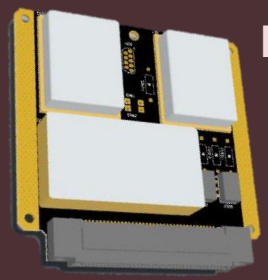


Additional Views



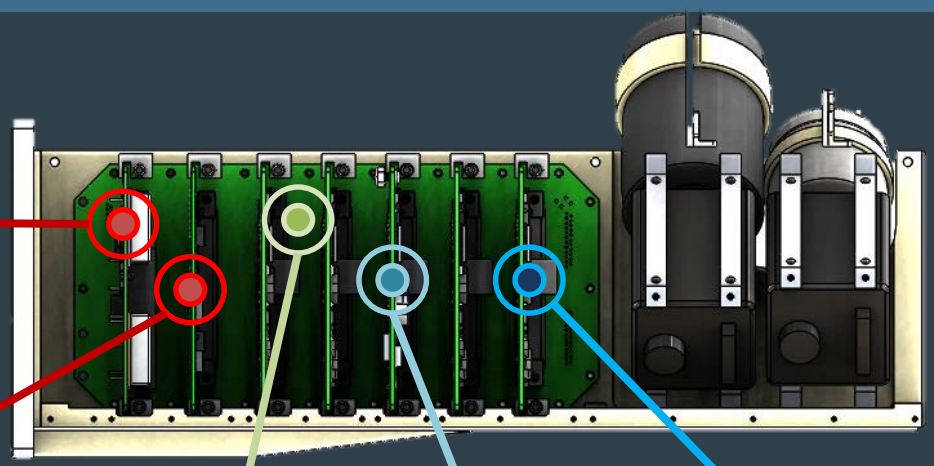


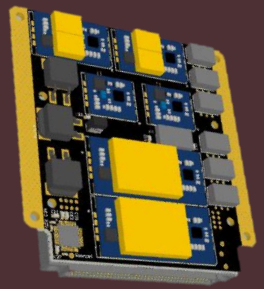
SSIVP Hardware



Power Card

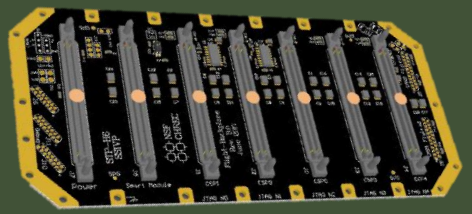
Design card to provide regulation to entire STP-H6/SSIVP flight unit





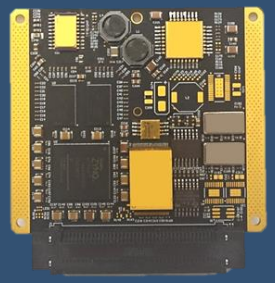
Smart Module

Prototype for Smart Module Designs, features GaN Sub-Experiment, accelerometer, RTDs and µCSP



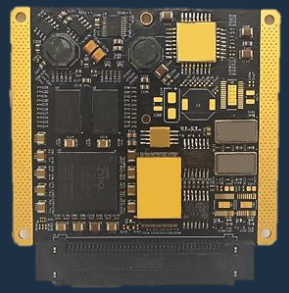
SSIVP Backplane

Design supports specific topology for 5 CSPv1 cards and smart module with µCSP



CSPv1 Rev. C

Even more rad-hard successor



CSPv1 Rev. B

Original CSPv1 flight card

SSIVP Software

Flight Software

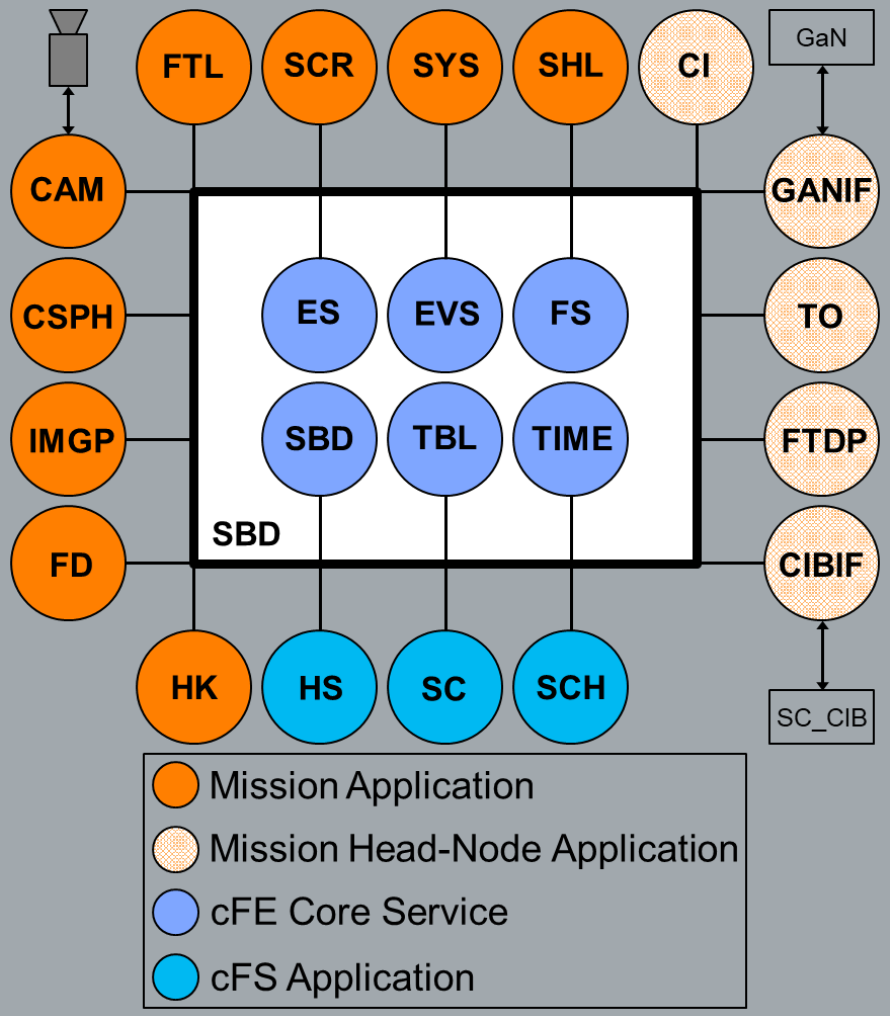
- CSPv1 flight software is Wumbo Linux, lightweight, custom operating system, based on Xilinx's Linux kernel fork and BusyBox
- Wumbo Linux is developed using Buildroot

CFS Applications

- Collection of adopted and custom cFS applications

SBD (Software Bus Distributed)

- Augmented version of cFE/SB
- Adds inter-node comm. support to cFE's messaging system
- Uses peer discovery and publish/subscribe msg features in OMG's RTPS protocol



OMG – Object Management Group **RTPS** - Real-time Publish/Subscribe


Mission Computing & Sub-Experiment

Network Topology

Two Network Architecture

- Primary network connects CSPv1 nodes with point-to-point differential signals
- Secondary network connects CSPv1 nodes with point-to-point, single-ended signals

Asymmetric Bandwidth

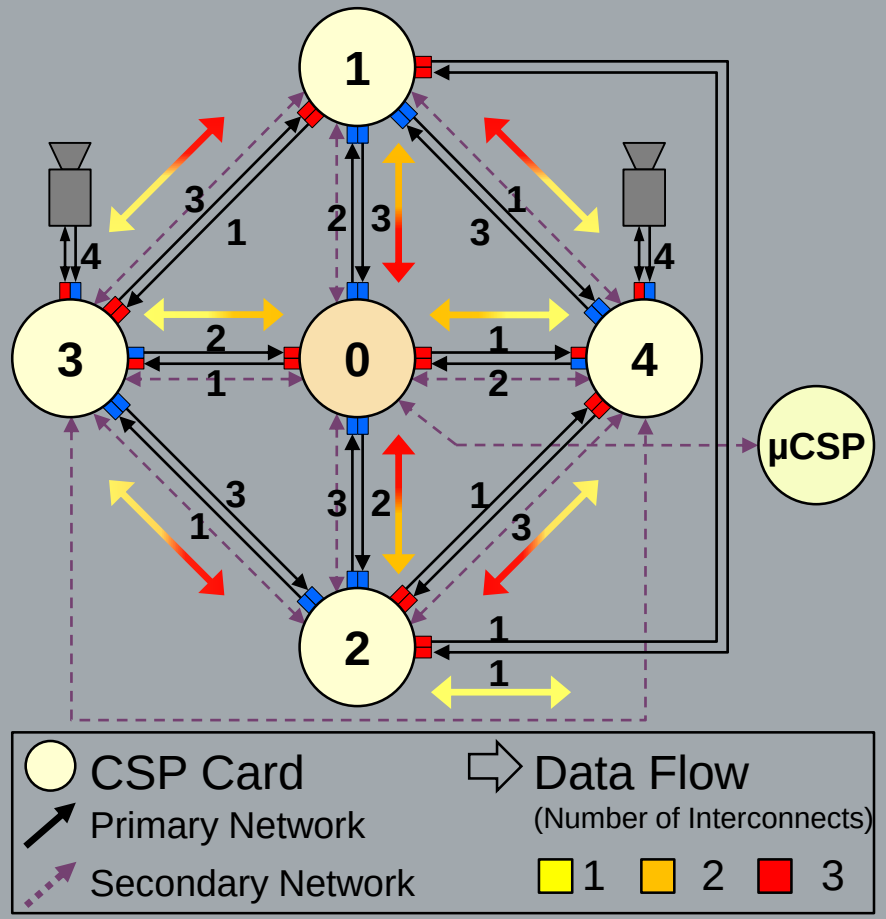
- Primary network is designed to optimize communication for **scatter-gather applications**
- Camera nodes have more transmission bandwidth
- Head node has more receiving bandwidth

Reconfigurable Network

Networking interface reside in Zynq FPGA and can be **reconfigured post-launch**

Custom Design

Custom networking interface, called Sabo-Link, leverages SerDes resources in Zynq FPGA for high-performance serial communication



Parallel Computing

Goal of SSIVP to enable Super Computing concepts with high-performance, parallel, and distributed computing

Enables High-Performance Computing

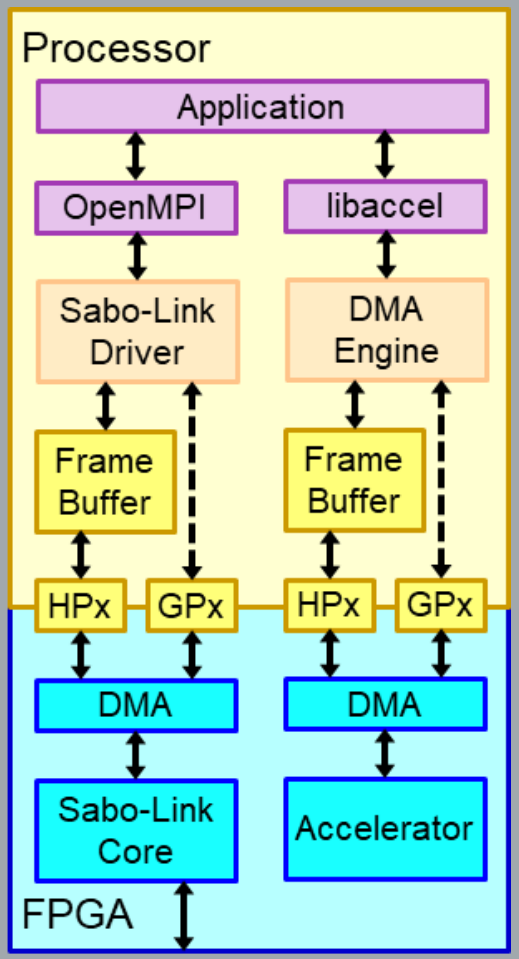
- Network driver support for native networking applications including **OpenMPI**
- Libraries and resources for **OpenMP** and **NEON**

Advanced Acceleration Framework

- Includes frameworks for inter-node communication and FPGA-based hardware acceleration
- Acceleration stack includes an FPGA-based image or video hardware accelerator, DMA-engine character device driver, and custom userspace library, called **libaccel**

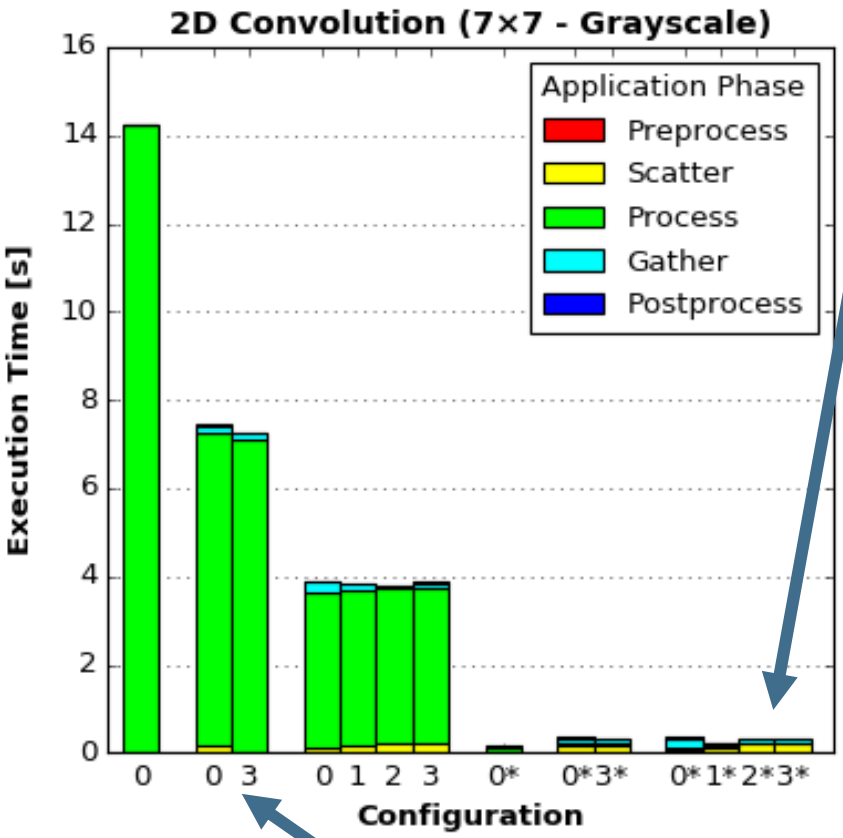
Partial Reconfiguration

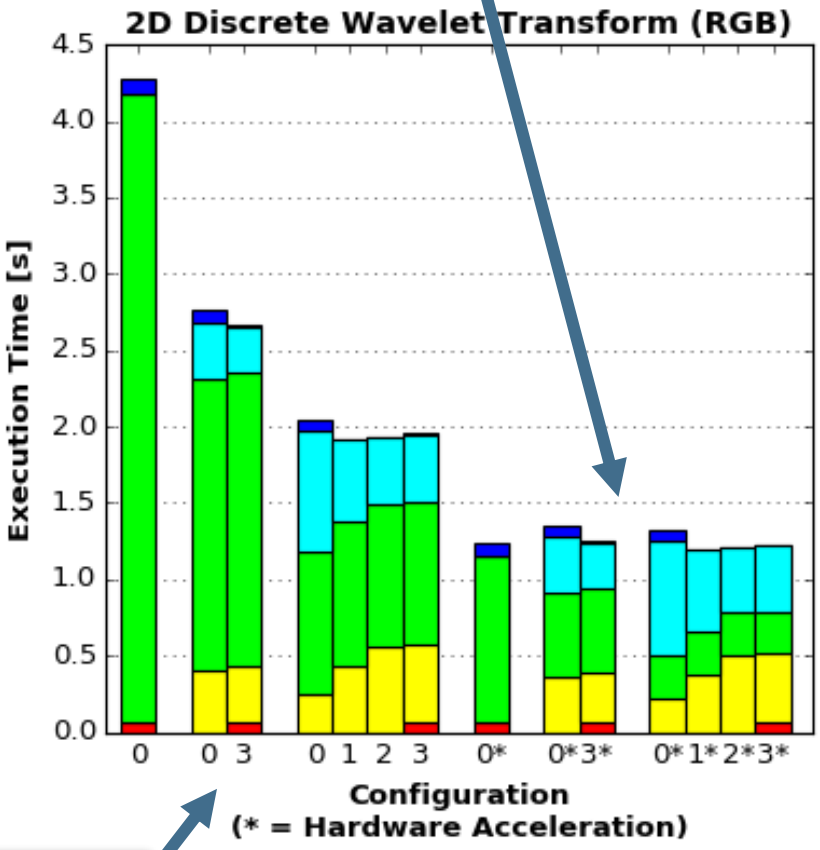
- **Partial Reconfiguration** is used to alternate between FPGA sub-designs at runtime



Results by Application Phase

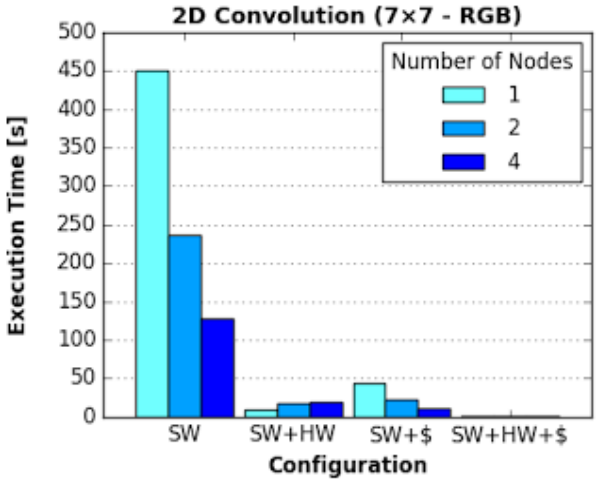
Speedup due to hardware acceleration

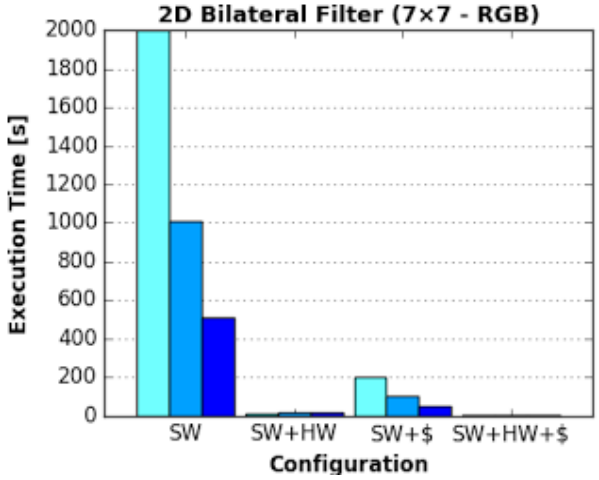


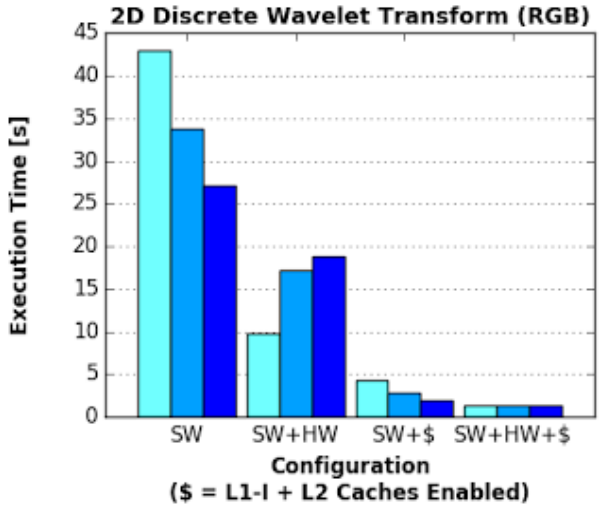


Speedup due to parallelization

Results by Node Number







Near-linear speedup with number of nodes

Significant gains with hardware acceleration

Performance benefits with caches enabled (reliability trade-off consideration)

Dependable Computing

Hybrid Adaptive Reconfigurable Fault Tolerance

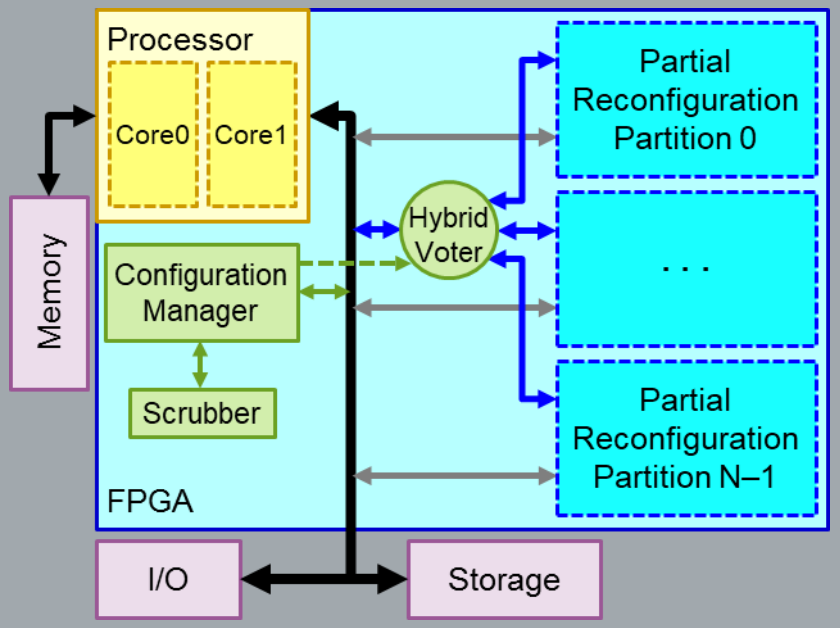
- Framework for Adaptive Fault-Tolerance on FPGA-based Hybrid SoCs
- Realize fault-tolerant strategy to apply over both fixed and reconfigurable architectures of SoC

Modes in CPU and FPGA Subsystems

- Adapt processor cores for symmetric multiprocessing (**SMP**) or asymmetric multiprocessing (**AMP**)
- Adapt FPGA partial reconfiguration partitions with HW accelerators or soft processors in simplex, duplex, or triplex **redundancy schemes**

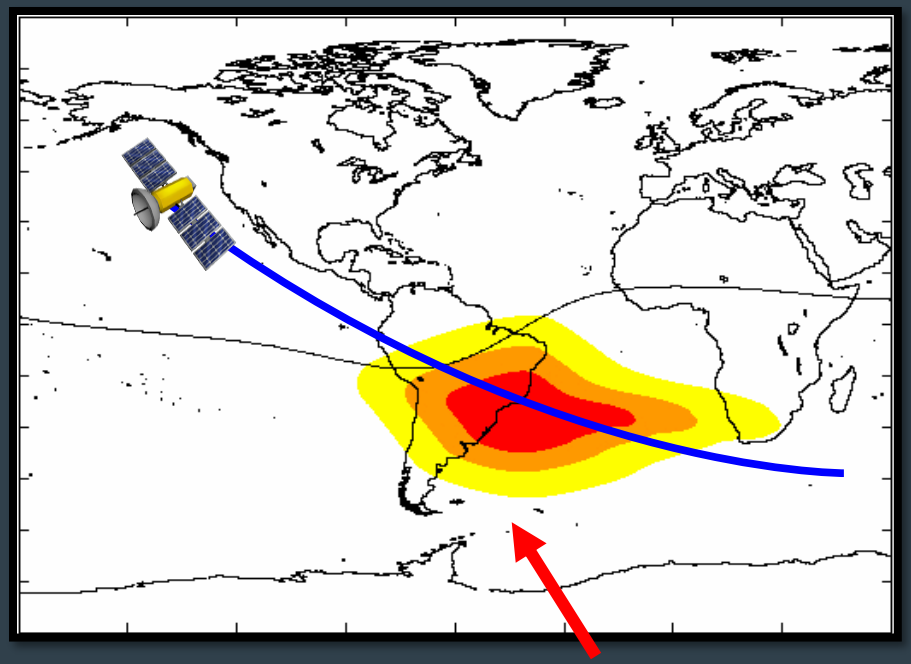
Environmentally Responsive

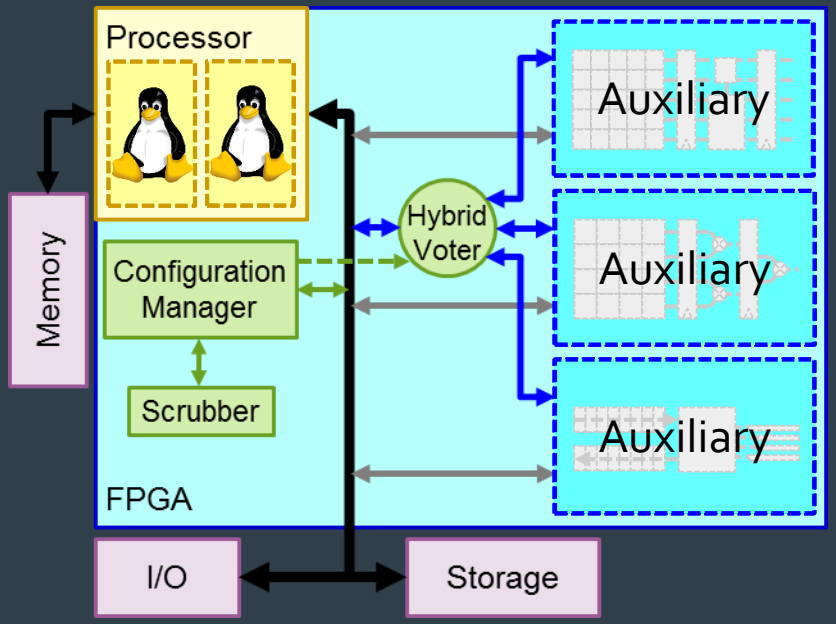
Adapt to dynamic upset rate by repurposing system resources for reliability or performance



Concept of Operation

Reliability Mode 2
HPS in **AMP** mode
SPS has 1 **triplex** soft-core





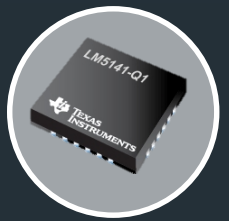
Performance
Power
Dependability

GaN PoL Sub-Experiment

Why GaN?

- Existing rad-hard PoL converters can be large, expensive, and inefficient
- GaN devices allow for efficient, high-frequency operation in small, radiation resistant packages
- SSIVP will evaluate several GaN HEMTs and controllers

2 Synchronous Buck Controllers



LTC3833


LM25141-Q1

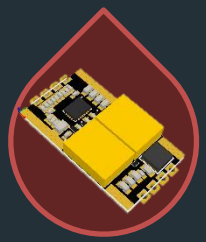
3 GaN HEMTs

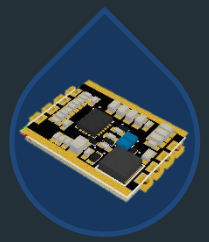

EVG100E15

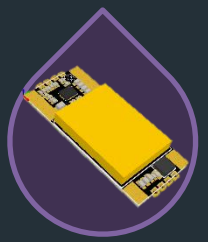

FBG04N08A

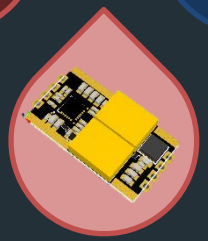

EPC2014C

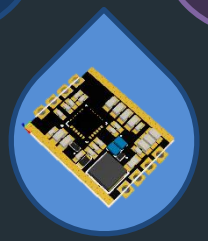
6 Board Combos

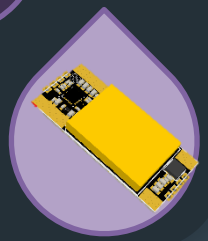












High Density

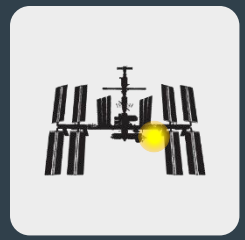
- Minimal Filtering Requirements
- Small Transistor Footprint
- Low Switching Losses
- Low Conduction Losses

High Reliability

- Operation to Full-Rated Voltage
- Low Voltage Gate Operation
- Wide Thermal Range
- Radiation Resistant

Conclusions

- **Major challenges lie ahead**
  - Escalating app demands in harsh environments
  - Tightening constraints of platform, budget, process
  - ***Necessitates adeptly doing more with less***
- **High-performance experiments on STP-H6**
  - Focus upon validating scalability of CSPv1 flight design
    - Submit compute intensive parallel jobs to onboard system
  - Download exciting science and technology results
    - Record vital heath & status, images, and upset rates
  - Push bounds of possibility in space
    - Demonstrate experimental technology and methods in space with secondary objectives



More information?

Dr. Alan D. George (PI), Department Chair, R&H Mickle Endowed Chair, Full Professor, and NSF CHREC Center Director

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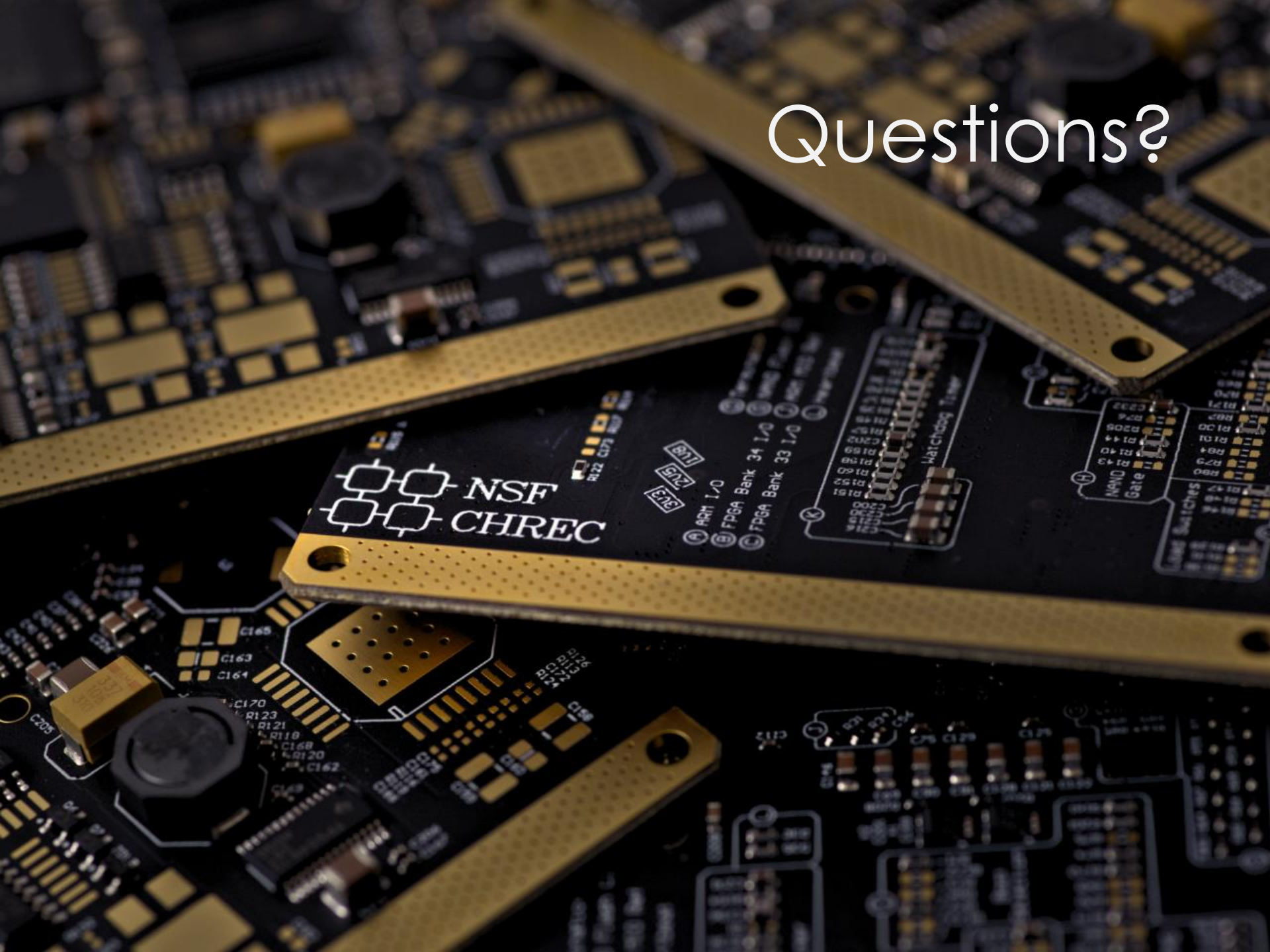
Questions?
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