EXTREME ENVIRONMENT OPERATION OF THICK-FILM SOI SIGE HBTS IN BOTH HIGH TEMPERATURE & RADIATION-RICH ENVIRONMENTS

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SUMMARY

The objective of this work is to characterize and investigate the effect of extreme environments, such as high temperature (up to 300°C) and radiation, on the response of thick-film SOI SiGe HBTs. Two different SiGe platforms are explored in this work with one aimed at RF applications (180 GHz f_{max}) and the other aimed at high performance and high voltage (up to 48V) analog applications (20 GHz f_{max}). To the best of the author's knowledge, this is the first look into the 300°C operation of thick-film SOI SiGe HBTs and the effect of TID on a high-voltage complementary SiGe platform.

Chapter 1 presents a brief overview and summary of the SiGe technology. The effect of incorporating Ge in a Si BJT is emphasized and is quantitatively described.

Chapter 2 presents the high temperature (to 300°C) DC and AC performance of a > 100 GHz f_T/f_{max} SiGe HBTs on thick-film SOI. Metrics such as current gain (β_F), BV_{CEO}, M-1, f_T, f_{max} are extracted from 24°C to 300°C and compared with a bulk SiGe HBT platform. The results demonstrate that while there are degradation to key device metrics at high temperatures, the devices are still usable over a wide temperature range. Additionally, while SOI is known for its high thermal resistance, it is demonstrated that the device is constrained by electrical effects rather than thermal effects at higher temperatures, which should therefore yield acceptable reliability. This work was presented at the IEEE Bipolar/BiCMOS Circuits and Technology Meeting 2015 [3].

Chapter 3 presents the impact of total ionizing dose (TID) on a high-voltage (36V) complementary SiGe on SOI technology, including the effects of irradiation and bias on the device oxides and the implications on forward and inverse-mode

device operation. The results indicate a multi-Mrad tolerance to TID similar to other SiGe HBTs, however, they illustrate a slightly anomalous behavior at high injection due to a decrease in collector resistance. A clear difference between forward mode and inverse mode response is also observed with bias. This work was submitted for the IEEE Nuclear and Space Radiation Effects Conference 2016.

Chapter 4 provides a summary of the contributions presented in this thesis. Additionally, it outlines the future work to be done based on the current research.

CHAPTER I

INTRODUCTION

Silicon-based electronics dominates today's world. There are several reasons for this but it's mainly due to the ubiquity and low cost associated with the production of Silicon-based electronics. As Silicon is abundant on Earth and the manufacturing methods are well-defined, the first choice for creating most electronics will be Silicon-based. Aside from the low cost and manufacturing ease, Silicon also has other advantages such as being able to create a high-quality oxide easily, can be grown as a large crystal with minimal defects (up to 300mm), and has excellent thermal properties [4]. However, the one downside to Silicon is it's not nearly as fast as some other more exotic III-V semiconductors due to its' lower mobility. In order to overcome this, increasingly complex scaling has to be undertaken for Silicon-based devices to be competitive in the RF realm.

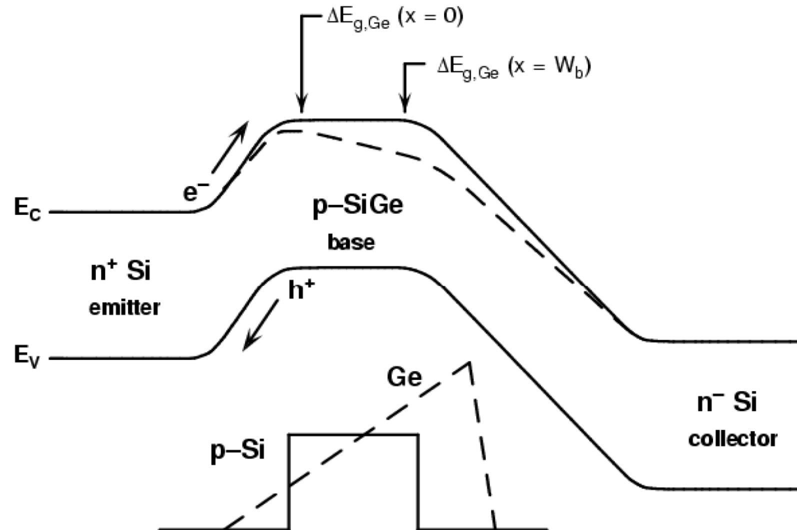

Figure 1: Change in the bandgap of a Si BJT with Ge incorporation in the base [1].

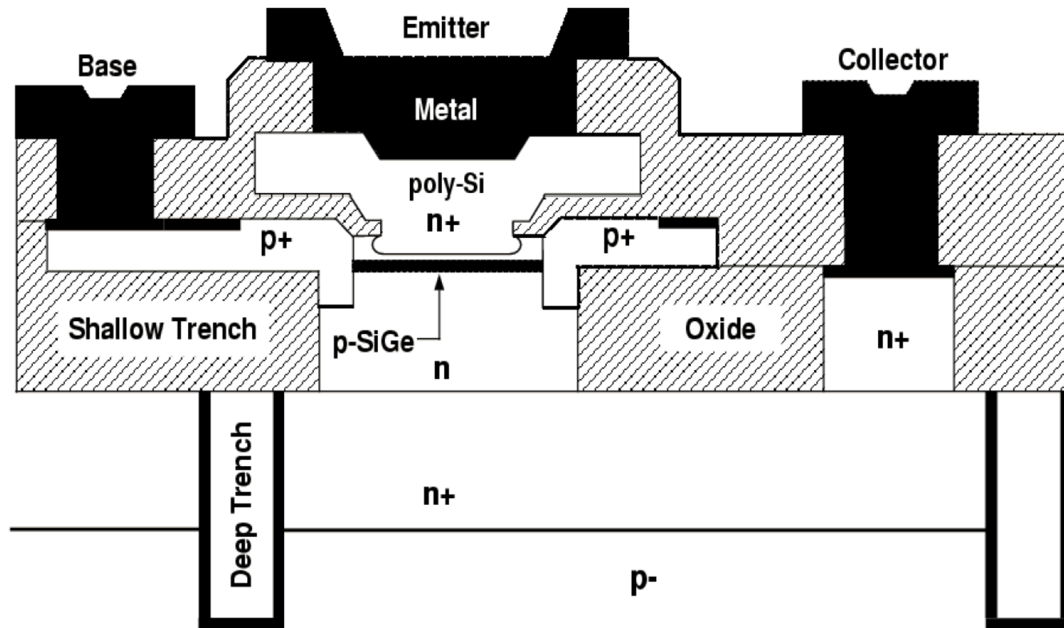

Figure 2: Cross-section of a typical SiGe HBT [1].

A Silicon-based platform that can achieve close to III-V performance while keeping the other advantages of Silicon is Silicon-Germanium Heterojunction Bipolar Transistors (SiGe HBTs). Incorporation of Germanium (Ge) in the base of a Si BJT leads to several advantages from a bandgap perspective as highlighted in Fig. 1. As Ge has a smaller bandgap than Si, a Ge grading in the base of an HBT results in a built-in electric-field that greatly enhances the AC performance of the device. Another key advantage to SiGe HBTs is the ease with which it can be incorporated with a CMOS process flow thus enabling a BiCMOS platform.

A cross-section of a typical SiGe HBT is illustrated in Fig. 2. The SiGe layer is only in the base as highlighted in the figure. The thickness of this SiGe layer has to be carefully controlled as too thick a layer with high Ge % can result in a SiGe film with heavy defects (making it unusable for device operation). The allowable thickness of the SiGe layer as a function of average Ge fraction is illustrated in Fig. 3. The different curves correspond to different cap layer thickness (H). The stability curve

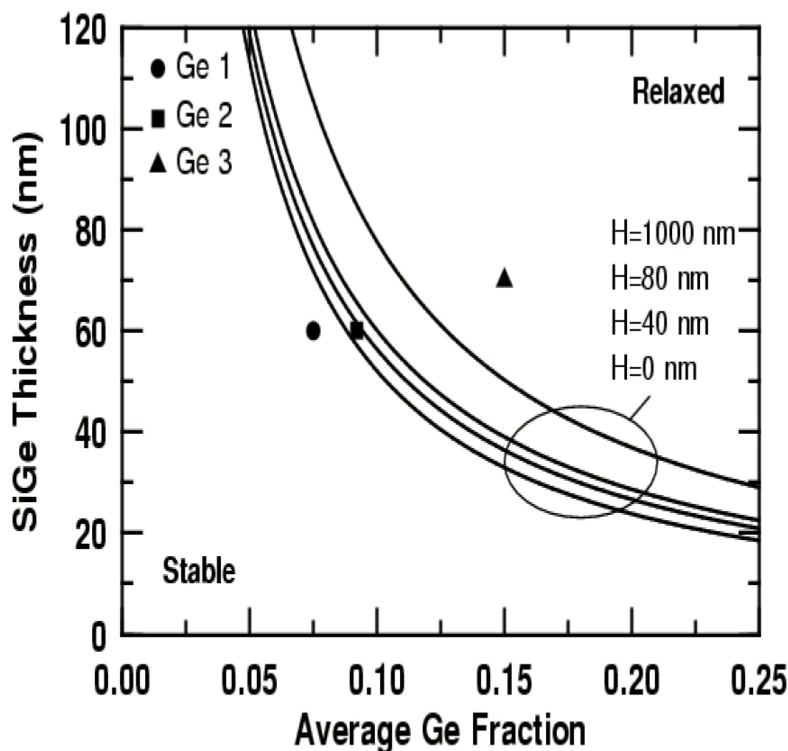

Figure 3: Stability diagram of different SiGe film thickness as a function of average Ge fraction [1].

was extracted using a force-balance approach that's discussed in detail in [1]. SiGe films that lay below the given curves are unconditionally stable while anything above the curves will lead to a thermodynamically unstable state. Essentially, Ge produces a bandgap reduction by causing a valence band offset that can be beneficial for *npn* devices. Ge also removes the conduction and valence band degeneracies in Silicon leading to higher mobility [4].

While it's easy to see some of the cursory effects the incorporation of Ge can have on the SiGe HBT performance due to the change in the bandgap, there are several other implications that can be derived mathematically. The first is the change in J_C (collector current density). To better illustrate this, a simple Ge profile in the base is shown along with the change it causes to the bandgap in Fig. 4. It should be noted that the two key parameters to SiGe HBT performance is $\Delta E_{g,Ge}(0)$, which is the

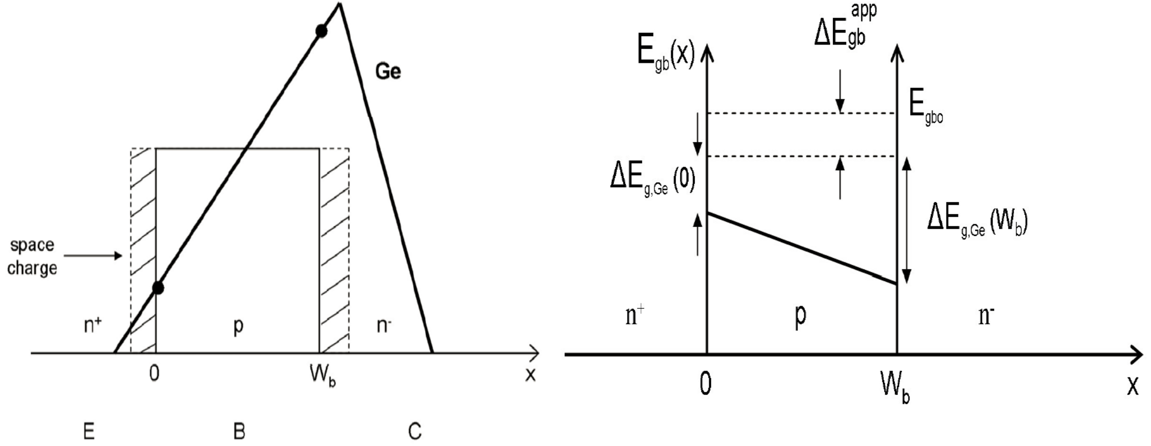

Figure 4: A Simple triangle Ge profile along with the changes it causes to the bandgap along the base [1].

change in bandgap due to Ge at the left edge of the base, and $\Delta E_{g,Ge}$(grade), which is the change in bandgap across the base. From first principles, it can be shown that J_C is equal to the following for SiGe HBTs (assuming constant base doping):

$$J_{C,SiGe} = \frac{qD_{nb}}{N_{ab}W_b}(e^{qV_{BE}/kT} - 1)n_{io}^2 e^{\Delta E_{gb}^{app}/kT} \cdot \left\{ \frac{\widetilde{\gamma}\widetilde{\eta}\Delta E_{g,Ge}(grade)/kT e^{\Delta E_{g,Ge}(0)/kT}}{1 - e^{-\Delta E_{g,Ge}(0)/kT}} \right\} \tag{1}$$

While there are several parameters in the equation, the dominant term is $e^{\Delta E_{g,Ge}(0)/kT}$ as J_C is directly proportional to an exponential. The $e^{\Delta E_{g,Ge}(0)/kT}$ illustrates that the Ge % at the edge of the base has profound impact on the total J_C for a given bias. To put it another way, compared to a normal Si BJT with the same doping/parameters, a SiGe HBT will get a marked increase in its J_C simply by having some Ge at the base edge. To better illustrate the impact this has on performance, the current gain (β) for a fixed V_{BE} can be compared between a normal Si BJT and SiGe HBT as the following:

$$\frac{\beta_{SiGe}}{\beta_{Si}} = \left\{ \frac{\widetilde{\gamma}\widetilde{\eta}\Delta E_{g,Ge}(grade)/kT e^{\Delta E_{g,Ge}(0)/kT}}{1 - e^{-\Delta E_{g,Ge}(0)/kT}} \right\} \tag{2}$$

Essentially, the base current doesn't change significantly with Ge incorporation while there's a large increase in collector current as illustrated in Fig. 5. This enables the decoupling of doping from current gain as the current gain of a SiGe HBT can be independently changed without changing the doping profile of the base or emitter. This has a profound impact on device optimization as doping can now be used to optimize other significant parameters (f_{max} by decreasing base resistance) while not affecting current gain much.

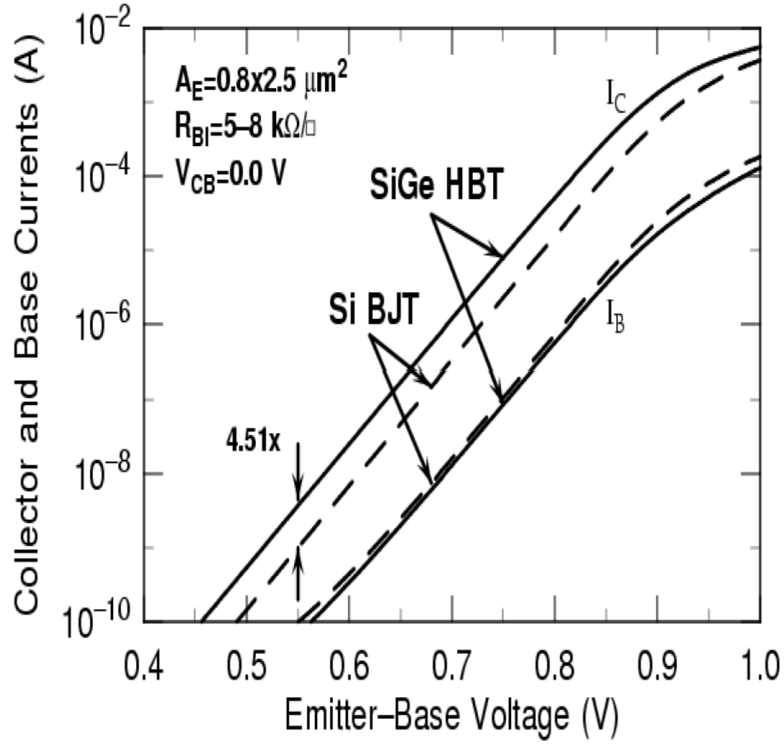

Figure 5: Comparison of Gummel between a "matched" Si BJT and a SiGe HBT [1].

Another important figure-of-merit (FoM) that is directly affected by the incorporation of Ge is Early voltage (V_A). The formula for V_A for SiGe HBTs relative to V_A for Si BJTs is as follows:

$$\frac{V_{A,SiGe}}{V_{A,Si}} = e^{\Delta E_{g,Ge}(grade)/kT} \cdot \left\{ \frac{1 - e^{-\Delta E_{g,Ge}(grade)/kT}}{\Delta E_{g,Ge}(grade)/kT} \right\} \tag{3}$$

Similar to the J_C case, the key parameter here is the $e^{\Delta E_{g,Ge}(grade)/kT}$ term as it's an exponential that's directly proportional to V_A. Therefore, by simply adding a Ge grading in the base, it can significantly increase the V_A which can greatly enhance circuit performance in both the analog and RF realm.

Aside from DC FoM, Ge incorporation has major implications on the AC response of SiGe HBTs. As it was already shown that Ge has a smaller bandgap than Si, a grading of Ge in the base will inevitably create band bending leading to a built-in electric field. This electric field aids carriers through drift and significantly increases the maximum achievable speed of the device. To quantitatively define this increase in speed, two AC FoM can be defined, f_T and f_{max}, where f_T is the unity gain frequency and f_{max} is the maximum oscillation frequency. They are quantitatively defined as follows:

$$f_T = \frac{1}{2\pi} \cdot \left[\frac{kT}{qI_C}(C_{te} + C_{tc}) + \tau_b + \tau_e + \frac{W_{CB}}{2v_{sat}} + r_c C_{tc} \right]^{-1} \tag{4}$$

$$f_{max} = \sqrt{\frac{f_T}{8\pi C_{bc} r_b}} \tag{5}$$

While f_T is dependent on several different capacitances, resistances, and intrinsic semiconductor parameters, the peak is mainly controlled by the base transit time given as τ_b [1]. As Ge grading in the base induces a built-in electric field, it has strong implications on τ_b. Not surprisingly, f_T experiences a sizable increase in overall speed due to τ_b reduction. As f_{max} is strongly dependent on f_T, a reduction in τ_b has a similar effect on its' performance as well. It should be noted that f_{max} can also be increased considerably by decreasing base resistance through higher base doping and lateral scaling.Thus, the decoupling of base doping from current gain greatly helps even from a AC perspective.

It's worth noting from all the listed equations above, SiGe HBTs have a different temperature dependence compared to typical Si BJTs. As all the parameters are

exponentially related to 1/kT, they will all appreciably increase with decreasing temperature. This is extremely desirable from a cryogenic perspective as demonstrated in [5].

CHAPTER II

HIGH TEMPERATURE CHARACTERIZATION OF THICK-FILM SIGE HBTS ON SOI

2.1 Motivation

Several studies have reported on the operation of high speed SiGe HBTs in extreme environments, particularly at cryogenic temperatures and in radiation-rich environments [6, 7, 8]. Due to the nature of the exponential dependence on temperature, SiGe HBTs enjoy an appreciable increase in most DC and AC key figures-of-merit (FoM) at reduced temperatures [7]. Record performance of 0.8 THz f_{max} was demonstrated at 4.3 K for a high speed SiGe HBT, thus lending credence to the capabilities of SiGe HBTs operating at extremely low temperatures [5].

However, the operation of SiGe HBTs on the higher end of the temperature spectrum has not been explored as much as cryogenic temperatures. Recent work for a bulk SiGe HBT with an f_T of 120 GHz were published in [9], while SiGe HBTs on thin-film SOI with a peak f_T of 35 GHz were reported in [10]. The work in [9] illustrated favorable DC, AC, and low noise performance, even at elevated temperatures, but the use of bulk devices resulted in high off-state leakage current. A CMOS compatible thin-film SOI was used in [10], which was more suitable for high temperature operation, but at the cost of significantly lower AC performance.

High temperature electronics has emerged as a field of recent interest, with applications in automotive electronics, aviation electronics, oil well digging, and even radar systems [9, 11]. In particular, telemetry applications (e.g., deep oil well digging and space electronics) require high speed devices. For bulk devices, wide-bandgap

semiconductors such as SiC or GaN have been looked at for high temperature operation due to lower intrinsic concentration even at elevated temperatures (leading to lower leakage current) [12]. As lower temperature favors the SiGe HBT performance, it also leads to degraded performance with increasing temperature. As such, high speed SiGe HBTs have not been considered applicable in the realm of high temperature electronics. However, with modern SiGe HBTs routinely reaching >120 GHz performance at room temperature, it is likely that device performance will remain high enough with temperature. The use of SOI can alleviate the leakage currents at high temperatures while offering other benefits such as isolation, reduced parasitics, and lower sensitivity to single event upsets (SEU) [10]. SiGe HBTs on thick-film SOI can provide several benefits at temperatures up to 300°C, especially from a speed perspective compared to bulk BJT silicon devices, and are becoming increasingly common.

Prior studies show that the use of SOI, however, tends to increase the thermal resistance (R_{th}) due to the poor thermal conductivity of SiO_2 that can lead to strong self-heating and electrothermal runaway at high DC power [13]. High performance SiGe HBTs are already aggressively scaled and this contributes to strong self-heating resulting from the larger current densities and electric fields [14]. The aim of this research was to look at, for the first time, the high temperature operation of 120/180 GHz f_T/f_{max} SiGe HBTs on SOI technology, and show whether the devices can be reliably operated up to 300°C without severe electrical or thermal degradation.

2.2 High Temperature Characterization

2.2.1 Technology & Measurement Details

The devices used in this study are a 0.2 x 10.25 μm^2 SiGe *npn* on SOI (and bulk), with a peak f_T/f_{max} of 120/180 GHz. The cross-section for the bulk device can be found in [15]. An approximate cross-section illustrating the major differences between

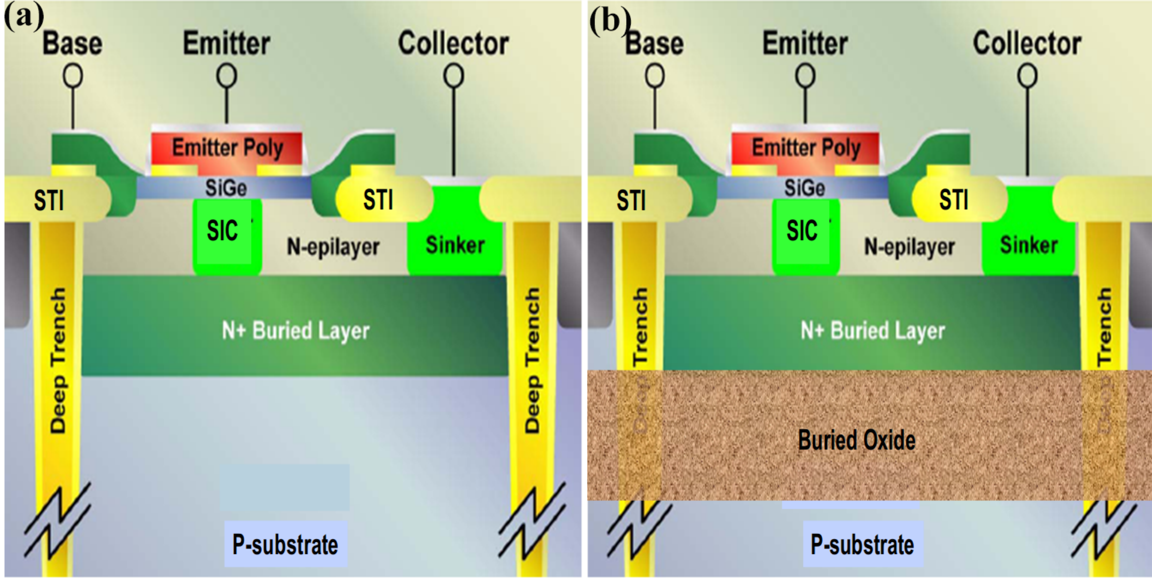

Figure 6: 2-D cross-section of (a) bulk device and (b) SOI device.

the bulk and SOI devices is illustrated in Fig. 6. The devices contain both STI and DT isolation and were not optimized for high temperature operation. Aside from the substrate differences, the SOI and bulk devices are completely identical.

Both DC and AC measurements were made on-wafer on a hot chuck capable of operating from 24°C (room temperature) to 300°C. An Agilent 4155C parameter analyzer was used to make all DC measurements, while an Agilent E8316C network analyzer was used to make S-parameter AC measurements.

2.2.2 DC Characteristics

The DC characteristics at high temperature were measured using the forward-mode Gummel with $V_{CB} = 0$ V, from 24°C to 300°C, as illustrated in Fig. 7. The Gummel characteristics remain nearly ideal over a wide temperature range, indicating normal operation. No deleterious series resistance effects were seen at high injection, as shown by the steady increase in collector current up to 300°C. Due to the SOI substrate, off-state leakage current is suppressed at high temperatures relative to the bulk device.

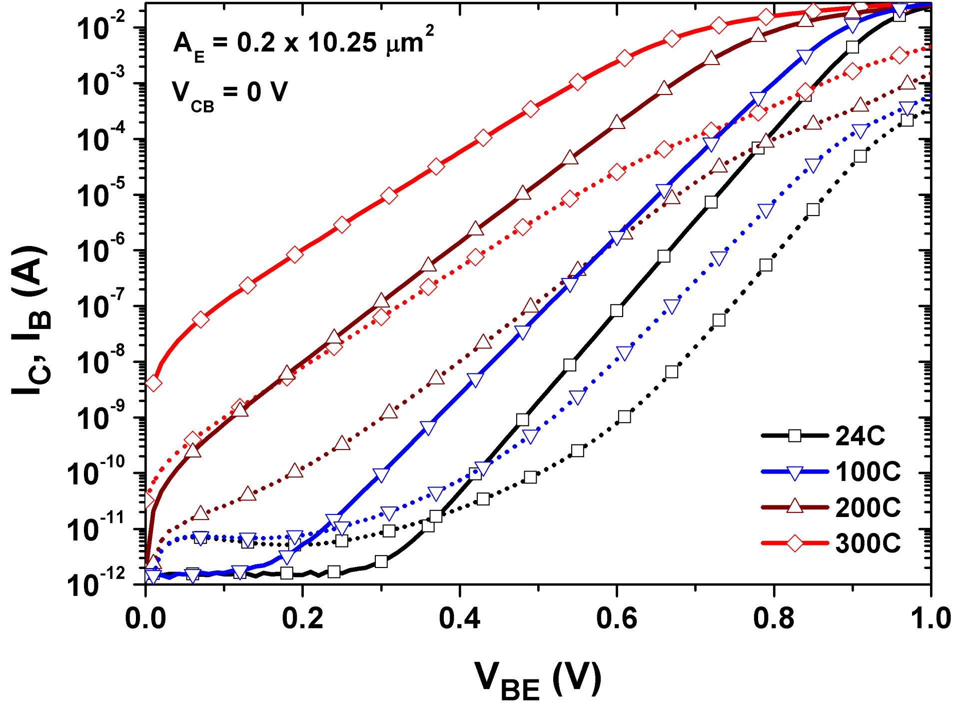

Figure 7: Forward-mode Gummel as a function of temperature. Solid lines are I_C while dotted lines are I_B.

This is illustrated in Fig. 8, and three orders of magnitude difference between the off-state leakage current at 250°C results from the use of SOI. This low off-state current is advantageous for many analog applications.

Forward-mode current gain (β_F) data from 24°C to 300°C are shown in Fig. 9. The peak β_F decreases with temperature, which is consistent with theory [1]. Although the data show approximately a 40% decrease in peak β_F at 300°C relative to 24°C, the device still yields a gain of over 100, demonstrating that these devices have adequate 300°C gain for most analog applications. An unexpected trend is observed at low injection, where the β_F increases with temperature up to 250°C. This disparity is attributed to the excess base current leakage found at 24°C in Fig. 7. Until 250°C, the collector current increases faster than the base current leading to an increasing

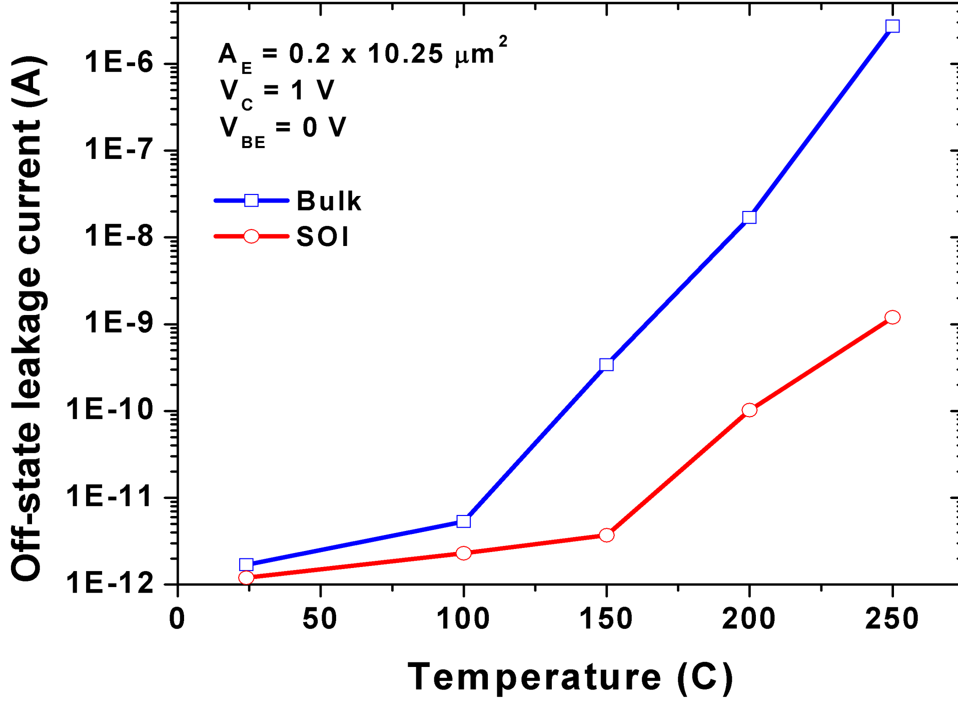

Figure 8: Off-state leakage current as a function of temperature for both bulk and SOI devices.

β_F at low injection.

One area where SiGe HBTs have an advantage with increasing temperature is in collector-emitter breakdown voltage (BV_{CEO}). BV_{CEO} values were extracted using the technique in [1]. Fig. 10(a) shows that there is close to 25% increase in BV_{CEO} from 24°C to 300°C. This is another positive factor for circuits operating at high temperature. Since BV_{CEO} is directly related to both β_F and the impact ionization rate (M-1), the behavior of M-1 over temperature was also measured and analyzed. M-1 as a function of V_{CB} over temperature is plotted in Fig. 10(b). With increasing temperature, the impact ionization rate decreases, as previously reported in [9, 10]. This is attributed to higher phonon scattering at elevated temperatures that decreases the probability of an electron causing impact ionization which is highly advantageous

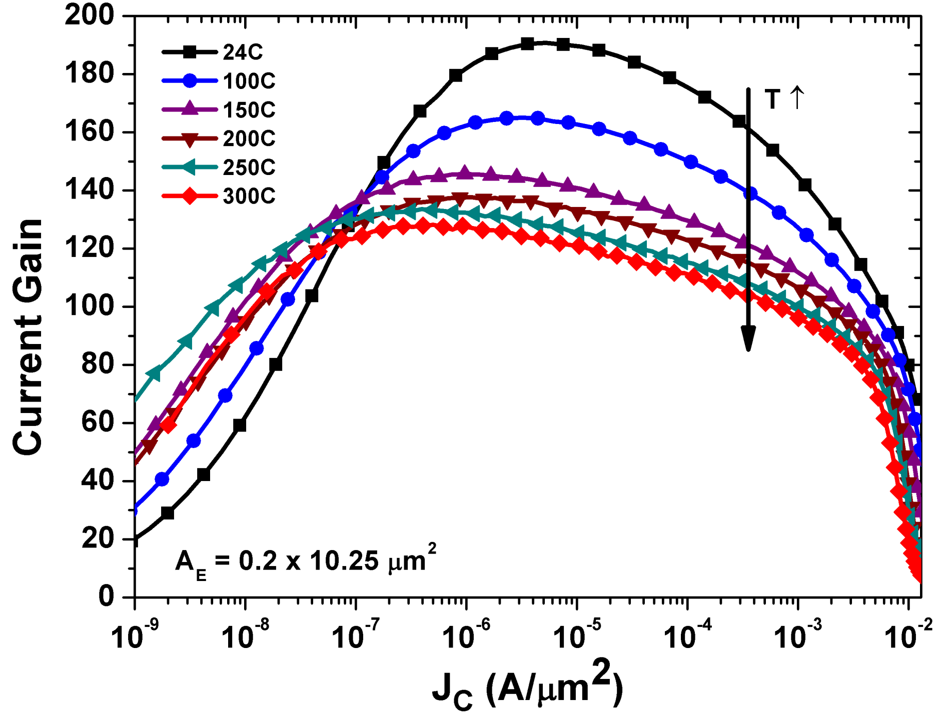

Figure 9: Forward-mode current gain (β_F) as a function of temperature.

from a reliability perspective. Since both M-1 and β_F are decreasing with temperature, it supports the observed BV_{CEO} trend over temperature.

2.3 Mixed-Mode Reliability

In order to access the implication of high temperature on the reliability of SiGe HBTs, mixed-mode (high-V, low-I) stress was used. As there were not enough devices for extensive reliability measurements, a third-generation (160nm W_E) bulk SiGe HBT (IBM 8HP) was used instead. The stress response for these devices will be more severe than the SOI devices used in this work due to a more scaled emitter window therefore, it can be considered a worst case stress response. The bulk device will also have less self-heating thus a higher M-1 which would lead to higher mixed-mode damage.

The devices were stressed at a mixed-mode stress of $6V_{CB}$ and 1 mA/μm^2 J_E

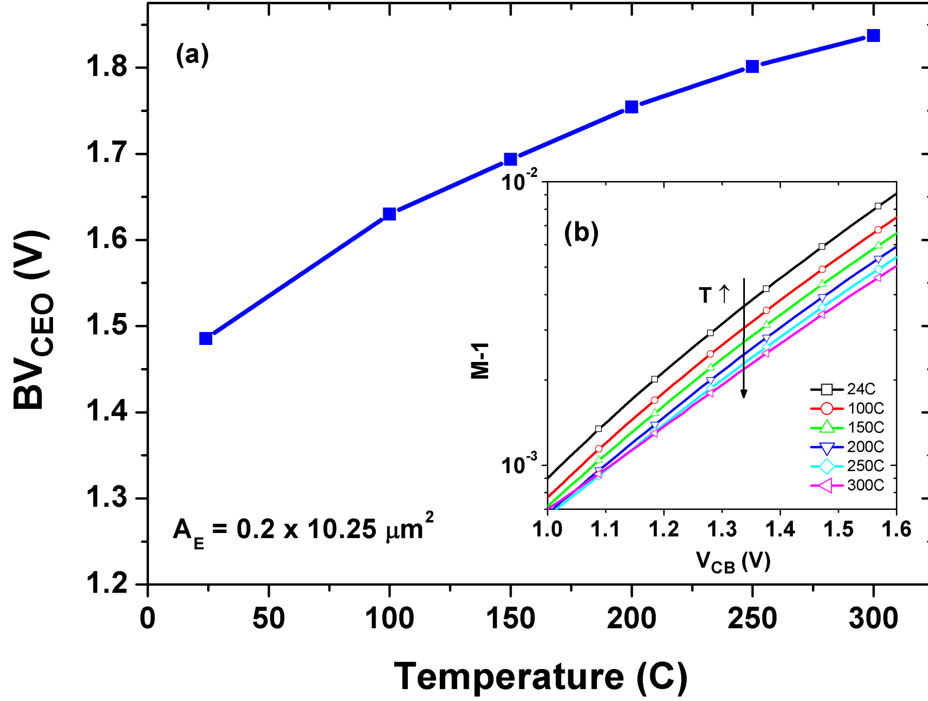

Figure 10: (a) BV_{CEO} as a function of temperature (b) M-1 as a function of temperature.

at four different temperatures: 24°C, 100°C, 200°C, and 300°C. The V_{CB} chosen is approximately 4V above BV_{CEO}. The J_E chosen is much lower than $J_{C,Kirk}$ which is optimal for stressing since at the onset of Kirk Effect, the peak electric field reduces significantly near the CB junction. The total stress time was 1000s and between evenly logarithmically spaced time points, the forward and inverse mode Gummel were measured to look at the I_B degradation (and subsequently β). The ΔI_B was measured at a J_C of 10 nA/μm^2.

The results are illustrated in Fig. 11 where Fig. 11(a) shows the ΔI_B for forward-mode Gummel and Fig. 11(b) shows the ΔI_B for inverse-mode Gummel. It be clearly seen that with increasing temperature, there is a strong reduction in mixed-mode damage in both forward and inverse mode which is consistent with the M-1 results from measurements. Inverse mode damage is much higher at low temperatures (24C

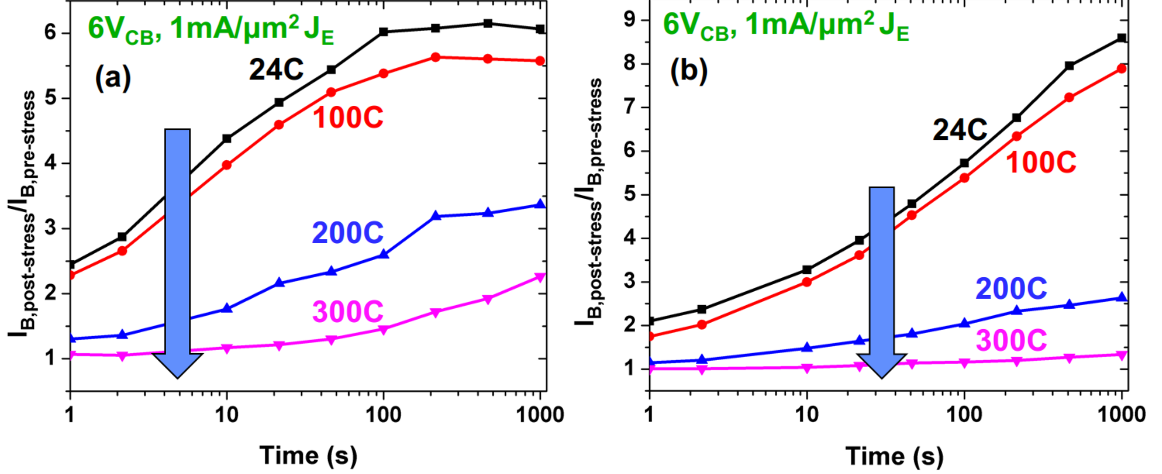

Figure 11: (a) Change in forward-mode I_B with mixed-mode stress of $6V_{CB}$, $1mA/\mu m^2$ J_E (b) Change in inverse-mode I_B with mixed-mode stress of $6V_{CB}$, $1mA/\mu m^2$ J_E

and 100C) but with increasing temperature, inverse mode damage becomes much more suppressed relative to forward mode damage. The implication here is that with increasing temperature, the probability of a hot carrier reaching the EB spacer or STI oxide interfaces becomes significantly smaller leading to the reduced damage manifestation in both forward and inverse mode. It should be noted that aside from M-1 reduction, annealing will also play a large role at these high temperatures as Hydrogen atoms will diffuse more and thus reduce the dangling Si bonds that produce the trap states at Si/SiO_2 interfaces.

2.4 Thermal Effects

Prior work have been reported on the positive temperature coefficient of R_{th} in SiGe HBTs [9, 10]. Thus, self-heating effects are expected to worsen with increasing temperature. R_{th} was extracted using similar technique as described in [16] and is plotted across temperature in Fig. 12 for both bulk and SOI devices. R_{th} increases for both devices, however, the bulk device shows a higher rate of increase relative to SOI. We

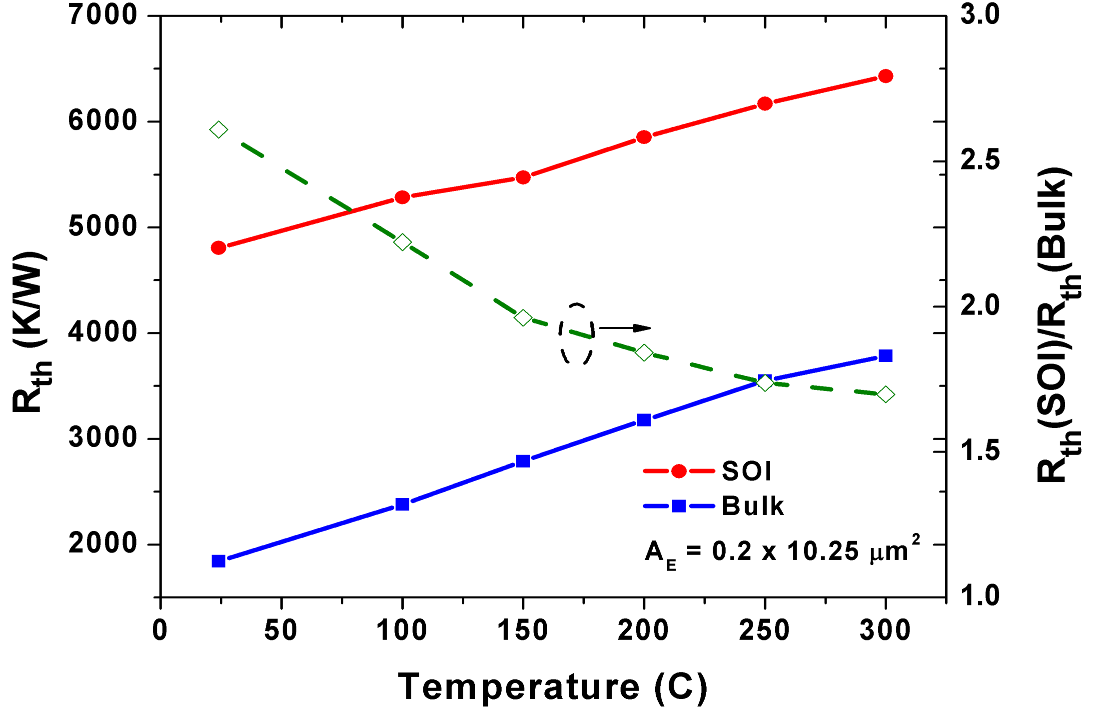

Figure 12: Thermal Resistance (R_{th}) as a function of temperature for both bulk and SOI devices with the ratio between SOI and bulk R_{th} overlaid.

note that the device measured is a single emitter geometry and the thermal resistance can be significantly reduced by using multi-fingered devices instead [9]. The self-heating effects leading to thermal runaway at room temperature for these devices were previously reported in [14].

Using [14] as the reference, the boundary for safe operation without strong electrothermal instability is defined as the point where $\partial V_{BE}/\partial I_C < 0$. This electrothermal instability point was extracted under a forced-I_B Gummel instead of forced-V_{BE} Gummel to be able to accurately get at the negative differential resistance (NDR) region. This is more clearly illustrated in Fig. 13 where the forced-I_B Gummel is plotted for various V_{CE} values from 1V to 2.3V. $V_{BE,crit}$ and $V_{CB,crit}$ are defined as the voltages where the onset of thermal runaway is observed. Forced-I_B Gummel with various V_{CE} over the temperature range of interest were measured to capture these

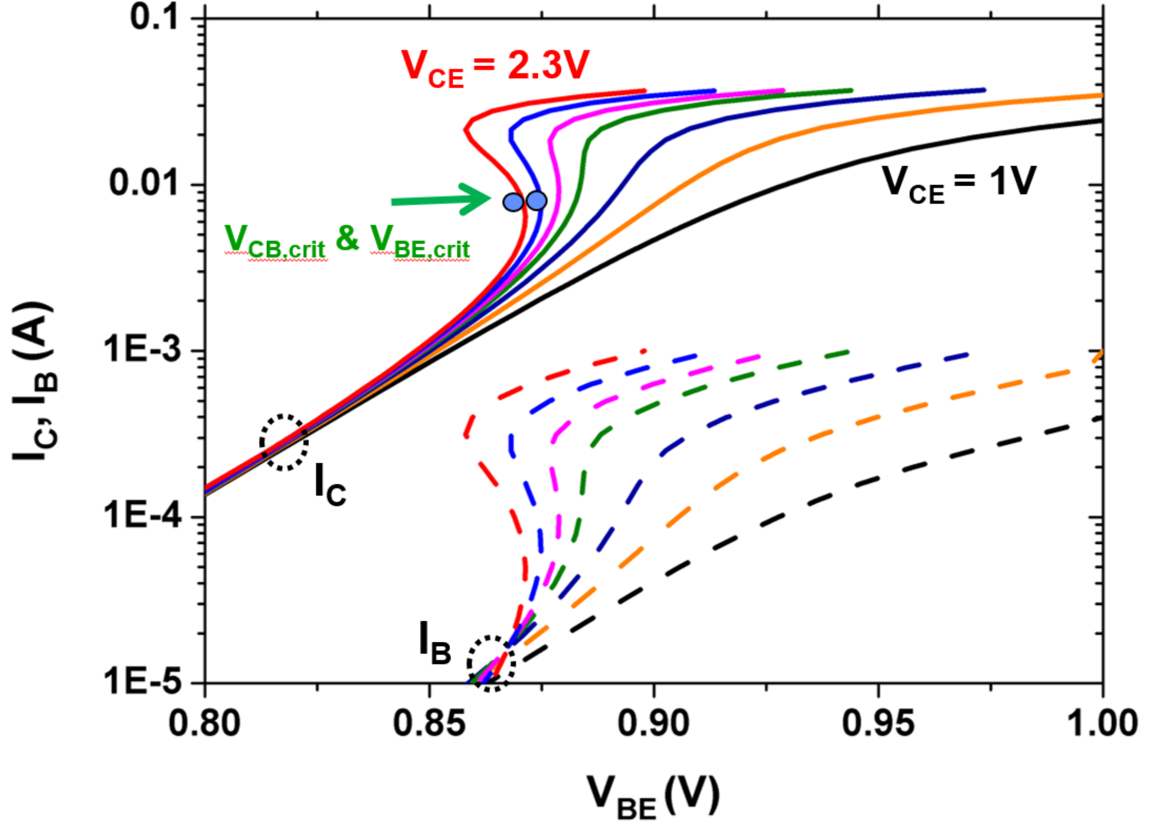

Figure 13: Illustration of the Negative Differential Region (NDR) due to strong self-heating at high DC power.

critical voltage points.

With increasing temperature, it is expected that $V_{CB,crit}$ should decrease, since higher thermal resistance can potentially cause more self-heating at same DC power, leading to electrothermal instabilities. $V_{BE,crit}$ is expected to naturally decrease since a lower V_{BE} is needed for a fixed I_C with increasing temperature. The measured results plotted in Fig. 14, however, indicate a different trend across temperature, especially for $V_{CB,crit}$. The results indicate that for a similar I_C, a higher V_{CB} is needed to initiate the onset of thermal runaway. Up to 150°C, $BV_{CEO} > V_{CB,crit}$, but past 150°C, the relationship becomes opposite. One of the major implications of this result is that at extremely high temperatures (>150°C), the device is more constrained by BV_{CEO} rather than electrothermal instabilities, which is clearly good news for using SOI in high temperature applications.

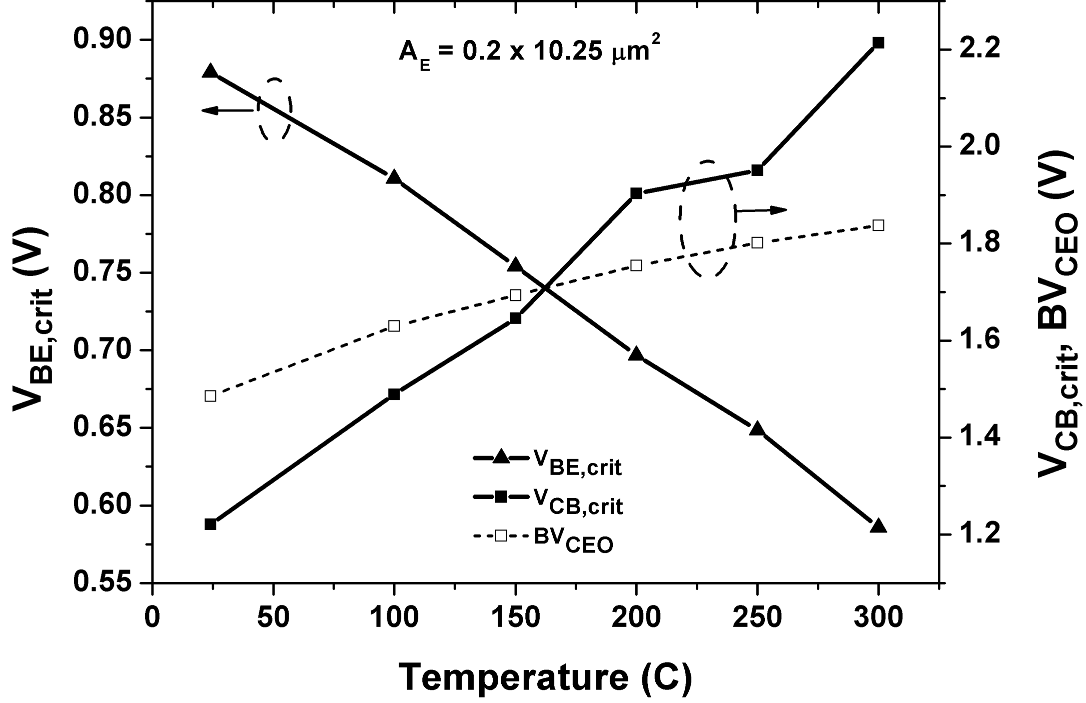

Figure 14: $V_{CB,crit}$ and $V_{BE,crit}$ as a function of temperature with the BV_{CEO} overlaid.

The reason for increasing $V_{CB,crit}$ can be explained by looking at the relationship between $V_{CB,crit}$ and T_{crit} as defined in [17]:

$$V_{CB,crit}(J_C) = \frac{\varphi(J_C)\Delta T_{crit}}{\gamma} - \frac{1}{\gamma+1}V_{BE}|_{V_{CB}=0} + \frac{1}{\gamma+1}AJ_CR_{EC} \tag{6}$$

where $\varphi(J_C) = \partial V_{BE}/\partial T$, $\gamma = \partial V_{BE}/\partial V_{CB}$ for a fixed I_C, A is the emitter area, J_C is the collector current density, R_{EC} is the series combination of the external emitter and collector resistors, and ΔT_{crit} is defined as:

$$\Delta T_{crit} = \Delta T_{min} + \Delta T_{R,EB} + \Delta T_{R,EC} \tag{7}$$

where ΔT_{min} is the change in temperature needed for thermal runaway to occur, $\Delta T_{R,EB}$ is the change in temperature needed to compensate for the decrease in voltage due to base and emitter series resistances, and $\Delta T_{R,EC}$ is the change in temperature

needed to compensate for influence of external emitter and collector resistances. The last term in both (1) and (2) can be neglected here, since the measurement setup used does not include any ballast resistors. Therefore, (1) can be rewritten as:

$$V_{CB,crit}(J_C) = \frac{\varphi(J_C)\Delta T_{crit}}{\gamma} - \frac{1}{\gamma+1} V_{BE}|_{V_{CB}=0} \tag{8}$$

While (1)-(3) were derived for a SOI Silicon BJT, the underlying concept should still be applicable to these SiGe HBTs. From measured results, γ was found to be negative (ranging from -0.044 to -0.056 over temperature) and $\partial\gamma/\partial T$ was measured as -4.3×10^{-5}. V_{BE} for a fixed I_C at $V_{CB} = 0$ is a decreasing function of temperature, as shown in Fig. 7 and the $\partial V_{BE}/\partial T$ and φ at the current density where thermal runaway occurs was measured as -7.9×10^{-4}. The temperature dependent variables in the first term in (3) are ΔT_{crit} and γ, while φ is temperature independent [17]. Without any external resistances, ΔT_{crit} is dominated by ΔT_{min}, which is a linear increasing function of temperature. However, as temperature increases, series base and emitter resistances can become significant which causes an additional increase in ΔT_{crit}, according to (2). Overall, this results in the first term of (3) increasing with temperature. Both an increasing $|\gamma|$ and $V_{BE}|_{V_{CB}=0}$ should result in the second term of (3) to increase. However, it is mostly dominated by $V_{BE}|_{V_{CB}=0}$, since $\partial V_{BE}/\partial T$ is one order of magnitude larger than $\partial\gamma/\partial T$. Therefore, the first term of (3) increases with temperature while the second term decreases with temperature, resulting in an overall increasing function of temperature. This temperature dependence for $V_{CB,crit}$ is consistent with the measured results in Fig. 14.

2.5 AC Characteristics

To accurately measure the peak f_T and f_{max} of the device at high V_{CE} and not run into thermal runaway issues, the forced-I_B method in [14] was used. Both measured h_{21} and MUG showed a nearly ideal 20 dB/dec slope and were reliably used to extract up to

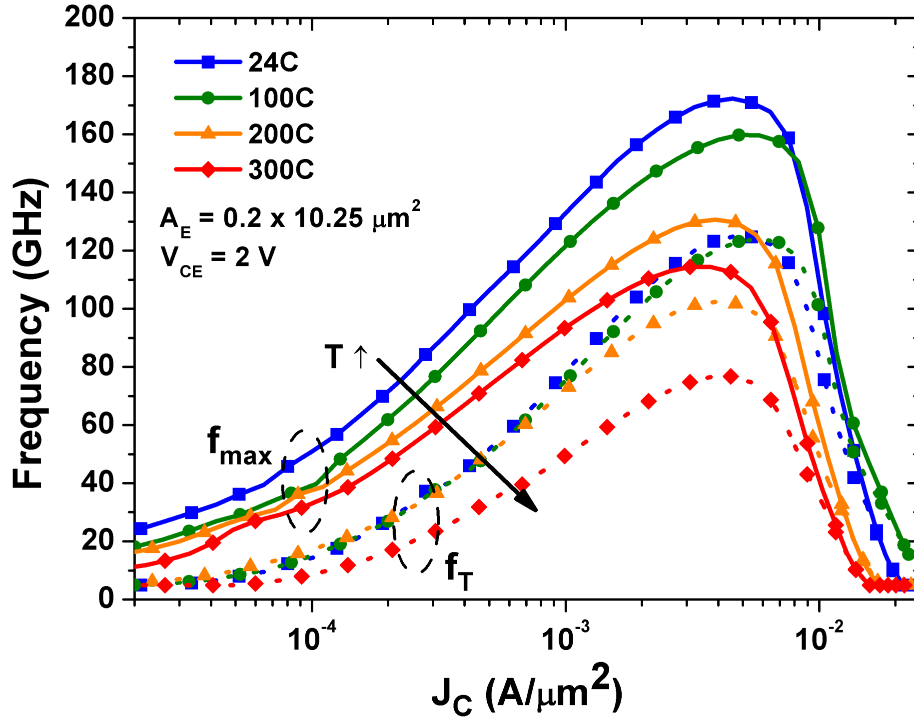

Figure 15: f_T and f_{max} as a function of collector current density from 24°C to 300°C for SOI.

f_T and f_{max}. Proper deembedding and calibration were obtained at each temperature through the use of calibration substrate standards. V_{CE} of 1.0 V, 1.5 V, 2.0 V were used for f_T and f_{max} extraction. Fig. 15 shows the extracted f_T and f_{max} at 24°C, 100°C, 200°C, and 300°C for a V_{CE} of 2 V as a function of J_C. The V_{CE} of 2 V demonstrated the highest peak f_T and f_{max}. To the best of the author's knowledge, this is the first reported data of measured f_T and f_{max} at 300°C for SiGe HBTs.

A clear decrease in both peak f_T and f_{max} for bulk and SOI devices are observed in Fig. 16 with increasing temperature, as expected. For the SOI device, f_T decreases from 125 GHz to 77 GHz (a 38.4% change) while f_{max} decreases from 172 GHz to 114 GHz (a 33.7% change). A similar trend is seen for the bulk devices; however, f_{max} shows a 44% change from 24°C to 300°C. An important observation is that even at 300°C, the device still achieves an $f_{max} > 100$ GHz, more than adequate to support

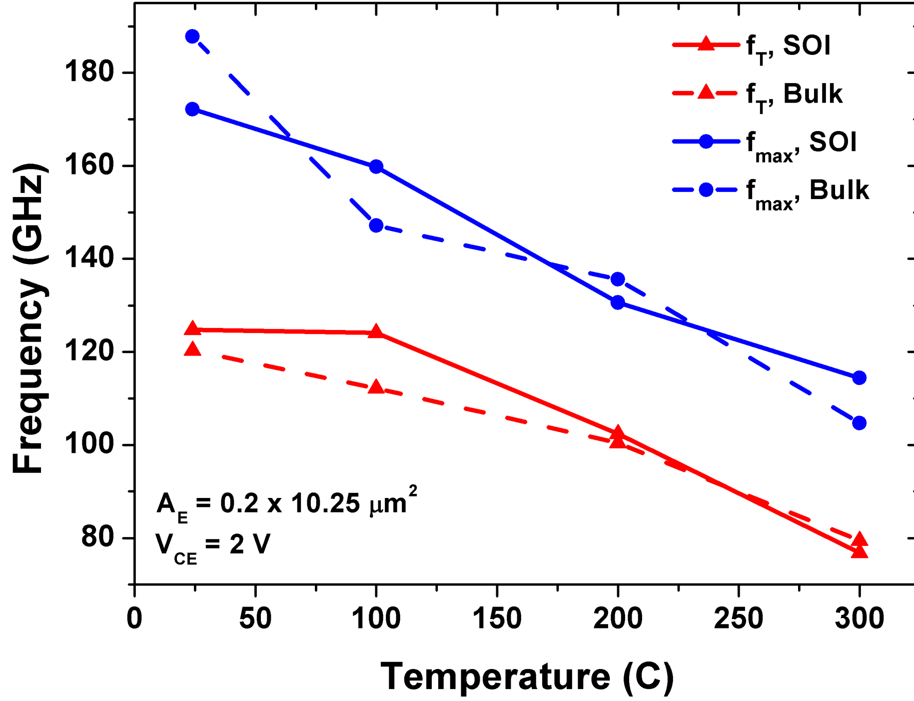

Figure 16: Peak f_T and f_{max} as a function of temperature for both bulk and SOI devices.

several high temperature applications. The f_T reduction with temperature can be attributed to the increase in total transit time, which was extracted using [1], and an increasing trend was observed due to enhanced minority carrier scattering in the base, and hence a reduction in mobility. Since f_{max} is directly related to f_T, it also shows a decreasing relationship with temperature. A slight decrease in the $J_{C,Kirk}$ with increasing temperature is also observed in Fig. 15 (past 100°C). As $J_{C,Kirk}$ is related to the saturation drift velocity (which decreases with increasing temperature due to higher carrier scattering), $J_{C,Kirk}$ also decreases with increasing temperature, thus reducing the peak f_T and f_{max} at high temperatures [14].

2.6 Summary

DC and AC characteristics, along with thermal effects, were examined from 24°C to 300°C for SiGe HBTs on SOI, and it is demonstrated that high speed SiGe HBTs on SOI can be operated for most applications even at elevated temperatures as high as 300°C. Mixed-mode reliability measurements also indicate that there is severe suppression of avalanche induced damage with increasing temperature due to the significant reduction in M-1.

CHAPTER III

TOTAL IONIZING DOSE EFFECTS ON A HIGH-VOLTAGE (36V) COMPLEMENTARY SIGE ON SOI TECHNOLOGY

3.1 Introduction

The investigation of total ionizing dose (TID) effects on a high-voltage (36V) complementary thick-film SOI SiGe technology is investigated for the first time. Typical SiGe platforms involve high-speed devices that find use in performance-constrained RF applications such as LNAs, PAs, mixers, oscillators, etc. However, there is also a large (and growing) interest in using SiGe HBTs in the analog domain. While Ge incorporation and grading in the base of a SiGe HBT significantly reduces the carrier transit time, it also enhances the current gain (β) and the Early Voltage (V_A), which are both extremely important metrics for analog applications.

One realm of analog electronics that less frequently utilizes SiGe HBTs is the domain of high-voltage circuits. As the unity-gain frequency (f_T) is a vital parameter in SiGe HBT optimization, BV_{CEO} typically has to be compromised. This is usually done by increasing collector doping, which pushes out the onset of Kirk and barrier effects. However, from a high-voltage analog perspective, it would be beneficial to sacrifice f_T for the sake of BV_{CEO} by using a lower collector doping and thicker collector epi. This enables a SiGe HBT to receive the benefits of higher β and V_A relative to a Si BJT, while offering comparable BV_{CEO} (along with a host of advantages from a high-temperature operational perspective). These high-power devices can find use in both power management systems (i.e., DC-DC converters) and in motor drivers typically used in conjunction with telemetry equipment [18].

Many investigations have been performed on the TID tolerance of SiGe HBTs from 1st generation to 4th generation devices [6, 19]. These studies have shown that modern SiGe technologies are multi-Mrad tolerant due to their structure. Recent work has also been done on a thick-film complementary SOI 5V SiGe process that illustrated favorable TID response from both a forward and inverse-mode perspective [20]. However, the TID response of a high-voltage ($>$ 30V) complementary SOI SiGe HBT has never been explored. As high voltage capable devices utilize lower doping to reduce peak electric fields at larger voltages, they also tend to have larger depletion regions near oxide interfaces that could potentially adversely affect their TID response. Charge accumulation and interface traps is significant in the emitter-base (EB) spacer oxide and shallow trench isolation (STI) oxide due to the presence of the surrounding depletion region.

3.2 Experimental Setup

A device cross-section of the 3HV *npn* & *pnp* used in this work is illustrated in Fig. 17 & Fig. 18, respectively. It should be noted that both the *npn* & *pnp* are SOI devices, built on top of a 0.4 μm thick BOX [2]. The devices were optimized for a high β-V_A product while maintaining a BV_{CEO} up to 48V. The TID experiments were performed at Vanderbilt University using a 10-keV X-ray ARACOR test system. The devices were bonded out in a 28-pin DIP and were irradiated from 50 krad (SiO_2) to a cumulative dose up to 5 Mrad (SiO_2) at a dose rate of 32.5 krad(SiO_2)/min.

Pre-irradiation DC characteristics were measured and after each subsequent dose, DC characteristics were once again measured to track the change in behavior with exposure. Two different bias conditions were investigated. The first condition was with all the terminals grounded, which is typically the worst case condition for SiGe HBTs [21]. The second condition is with a V_{BE} of 0.6V and a V_{CB} of 40V (referred to

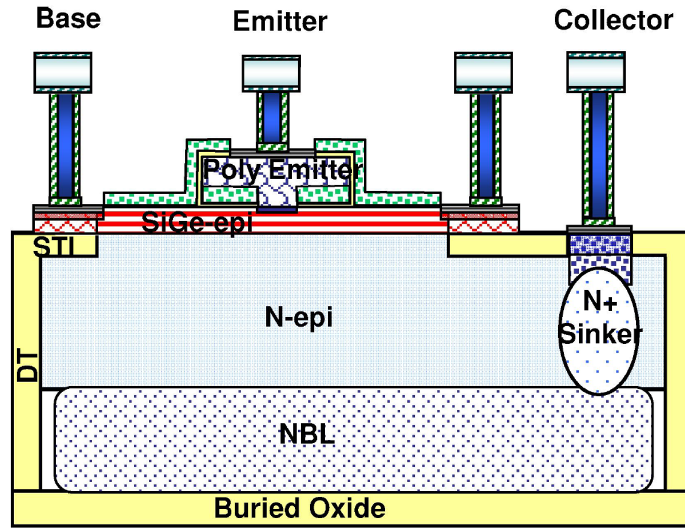

Figure 17: A cross-section of the 3HV *npn* [2].

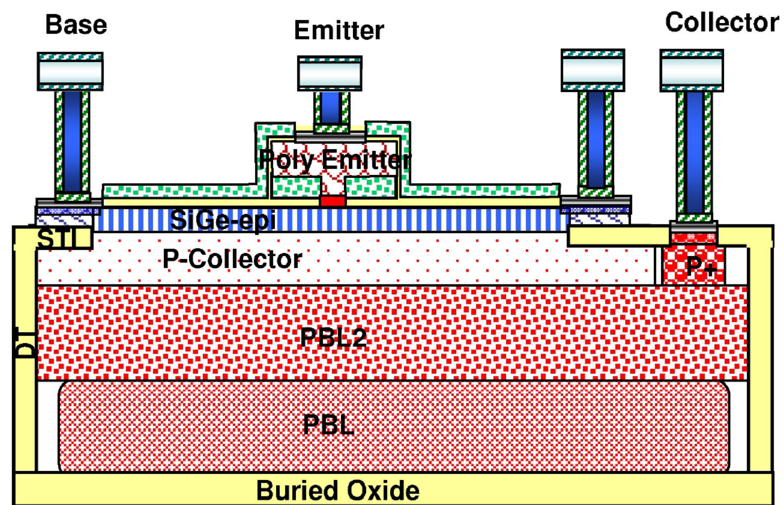

Figure 18: A cross-section of the 3HV *pnp* [2].

as “HV bias” in this work). The second condition was chosen to test whether high-voltage operation can potentially influence the TID response. It should be noted that the V_{CB} used in this work is not high enough to cause mixed-mode damage. BV_{CEO} was measured at 0.6 V_{BE} and it was approximately 48V therefore, avalanche induced damage can be ruled out. The devices were measured in both forward active and inverse-mode to better understand their disparities in damage mechanisms at the EB spacer oxide, the STI, and the underlying buried oxide (BOX).

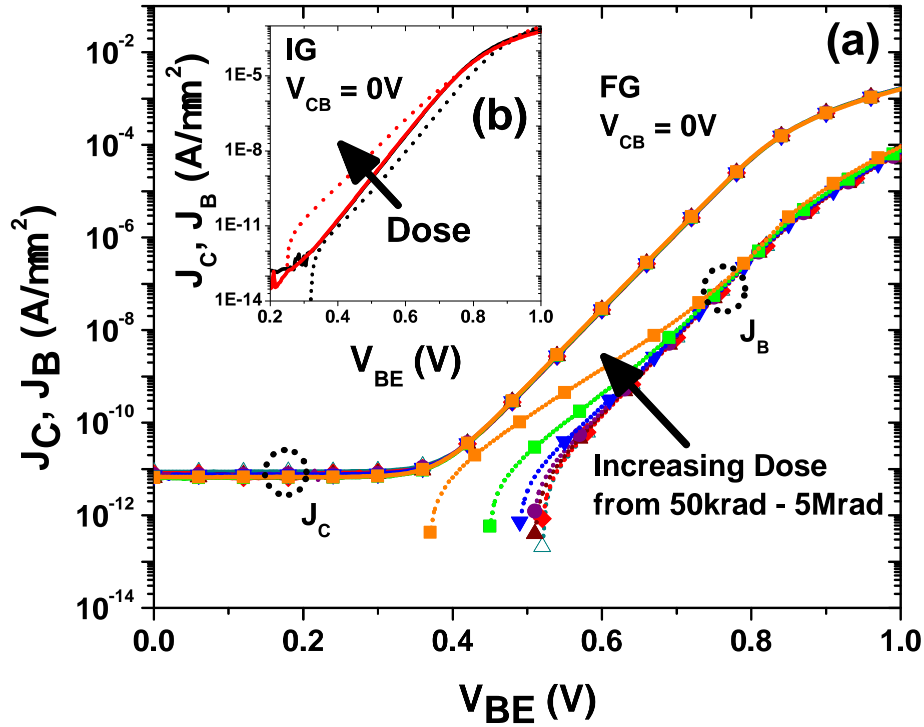

Figure 19: (a) Forward Gummel of the *npn* (grounded condition) for the following cumulative doses: pre-rad, 50 krad (SiO_2), 100 krad (SiO_2), 300 krad (SiO_2), 500 krad (SiO_2), 1 Mrad (SiO_2), 2 Mrad (SiO_2), and 5 Mrad (SiO_2). (b) Inverse Gummel of the *npn* for pre-rad and 5 Mrad (SiO_2). Solid lines are J_C and dotted lines are J_B.

3.3 Results

The grounded condition for the *npn* was initially measured and the Gummel response is illustrated in Fig. 19. Fig. 19(a) shows the forward Gummel (FG) response, and it

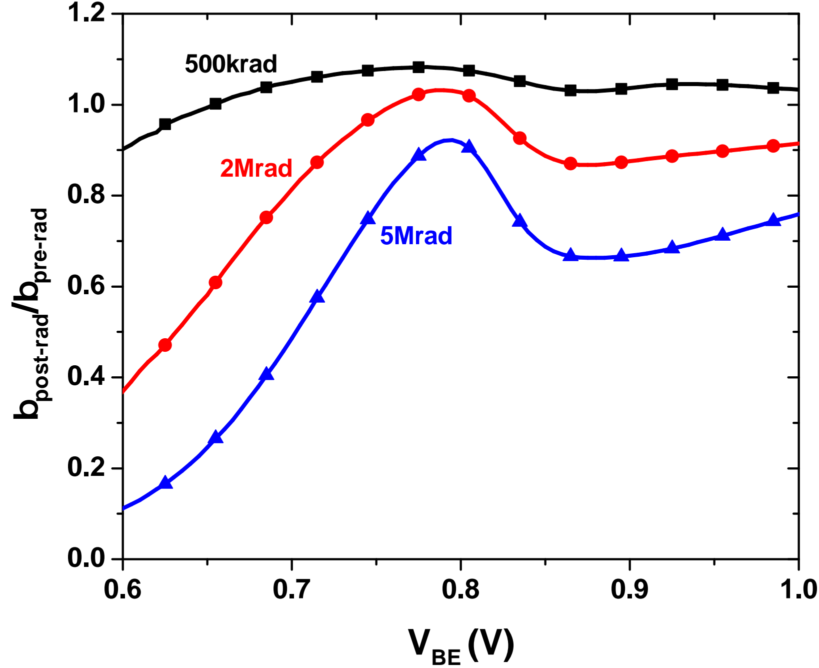

Figure 20: Normalized current gain (grounded condition) post- and pre-radiation for the *npn* as a function of V_{BE} for the following cumulative doses: 500 krad (SiO_2), 2 Mrad (SiO_2), and 5 Mrad (SiO_2).

can be seen that there is an increase in base current density (J_B) at low and medium injection with increasing dose, as expected. Fig. 19(b) illustrates the inverse Gummel (IG) response at pre-rad and 5 Mrad (SiO_2), which shows a similar response. No major shift ($< 5\%$) in the collector current in both forward-mode and inverse-mode is observed, indicating that there is not enough lateral charge accumulation under the EB spacer oxide to significantly affect the total emitter area [22]. The normalized change in β as a function of V_{BE} for three different doses is illustrated in Fig. 20. The low to mid V_{BE} shift in β is expected, while surprisingly, there is a significant shift at high injection (> 0.8V). To better understand this phenomenon, the excess J_C and J_B were examined at different doses. As J_C showed minimal change, J_B was the primary cause in the β reduction, even at high injection, as illustrated in Fig. 21. As J_C, and consequently J_E, show minimal change, it is clear that there is not a significant change in emitter resistance, thus implying that a different mechanism is causing a

shift at high injection. J_B shift at high injection has been observed before in [23] with high current electrical stress, which can lead to trap states at the interfacial oxide between poly/monosilicon regions.

The excess normalized difference in I_B at a V_{BE} of 0.6V for the forward and inverse-mode is illustrated in Fig. 22, along with some other SiGe technologies for comparison. It can be clearly seen that the inverse-mode shows greater than 2x increase in I_B relative to the forward-mode at high doses (> 1 Mrad (SiO_2)). This is attributed to the larger surface area of the STI oxide relative to the EB spacer oxide, which leads to more interface traps and oxide charge concentration [20]. It is also worth noting that for the more scaled (130nm) technology, forward-mode damage is much higher than inverse-mode damage.

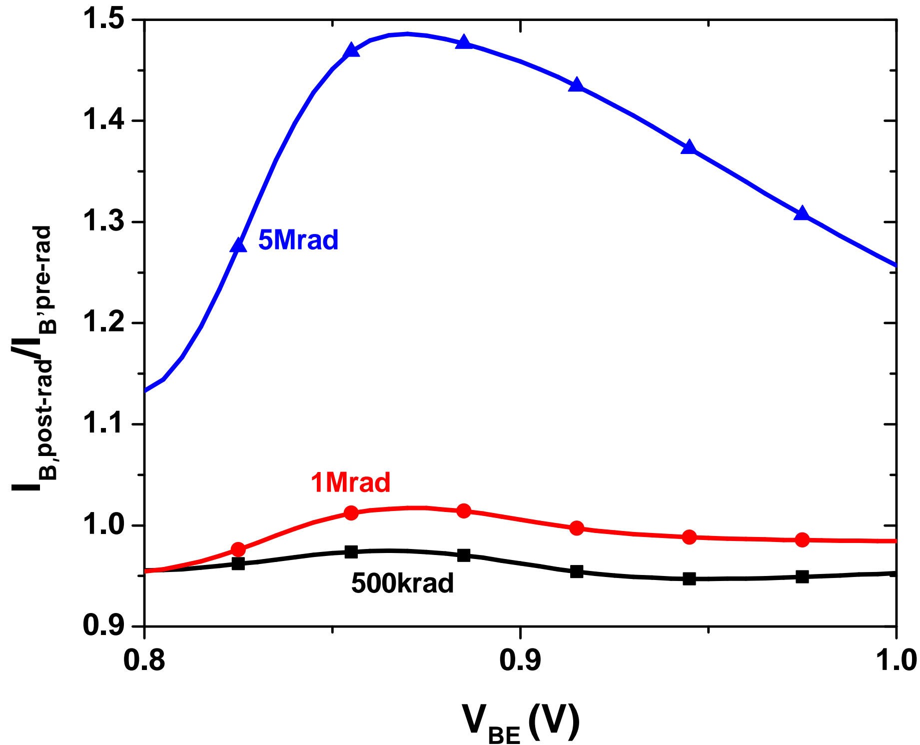

Figure 21: Normalized I_B (grounded condition) post- and pre-radiation for the *npn* as a function of V_{BE} for the following doses: 500 krad (SiO_2), 1 Mrad (SiO_2), and 5 Mrad (SiO_2). Only the high injection bias is shown.

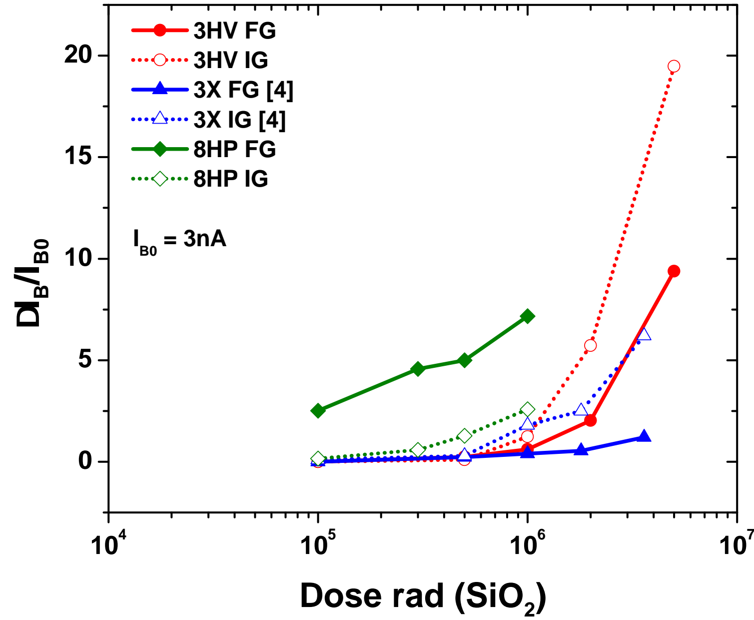

Figure 22: Excess normalized I_B for the *npn* as a function of dose. The 3X and 8HP SiGe technology are compared with the results for the 3HV platform for both forward and inverse-mode.

The HV bias was tested next, and the response was compared with the grounded condition in Fig. 23. Forward-mode operation shows minimal bias dependence, which is consistent with previous TID studies; however, in the inverse-mode operation, there is a significant difference under HV bias. Specifically, there is up to a 30x difference between the grounded and HV bias conditions, an effect which has not been previously reported. This difference can be explained by looking at the electric field differences in the device between the two bias conditions. Calibrated TCAD simulations were performed at the two bias conditions, and it was seen that the electric field near the STI had far higher peaks (2-3 orders of magnitude) under HV bias. The larger electric field near and within the STI region under the HV bias condition results in more of the electrons being swept away from the STI during irradiation, leaving more holes in the oxide and resulting in the higher leakage current [20]. The behavior of β for

the HV bias case did not change significantly compared to the grounded condition.

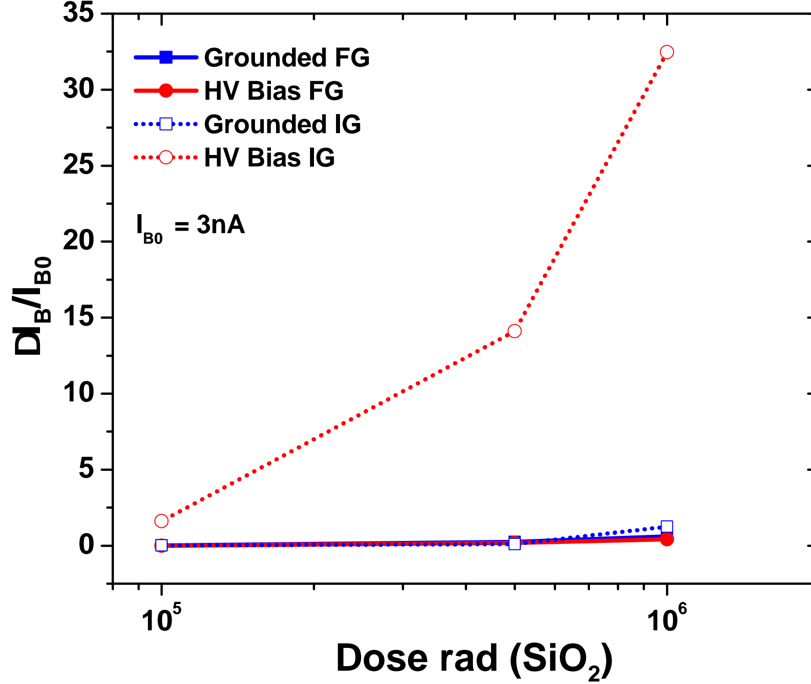

Figure 23: Excess normalized I_B for the *npn* as a function of dose for forward and inverse-mode grounded and HV bias condition.

Similar to the *npn*, the *pnp* SiGe HBT was also first irradiated under grounded conditions. The results are shown in Fig. 24. Fig. 24(a) shows the forward Gummel response from 50 krad (SiO_2) to 5 Mrad (SiO_2) while Fig. 24(b) shows the inverse-mode Gummel response. Both responses are qualitatively similar to the *npn* data. However, the *pnp* shows significantly lower J_B leakage current in both forward and inverse-mode with large doses. This difference is more clearly illustrated in Fig. 25. Only 1-2x increase in forward-mode I_B and 1.2-4x increase in inverse-mode I_B is observed in the *pnp*. This leakage is 5-7x lower than the leakage current observed in the *npn* under the same conditions. We believe that this is due to the accumulation of positive charge in the *pnp* oxides near the n-type base, which helps to increase the electron concentration and reduce the excess I_B due to surface recombination [24]. In Fig. 25, the forward and inverse-mode response is also compared with the

complementary 5V technology presented in [20], and it shows that the forward-mode response is comparable, while the inverse-mode change is much higher. This discrepancy is likely due to a larger depletion region at the collector-base junction resulting from the lower doping, which in turn leads to a larger surface area available on the STI-silicon interface.

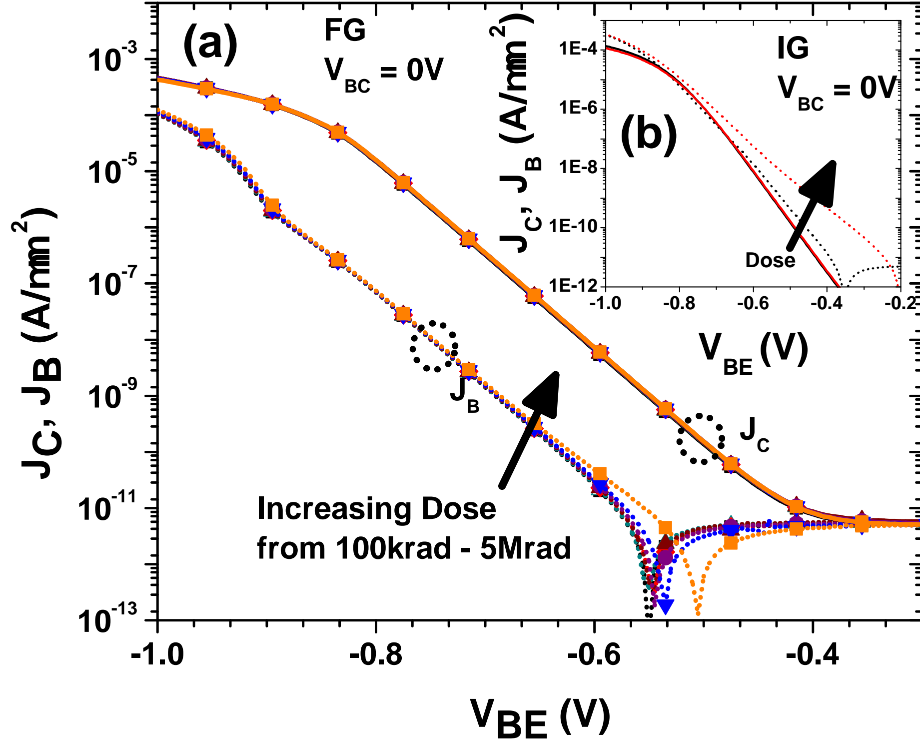

Figure 24: (a) Forward Gummel of the *pnp* (grounded condition) for the following cumulative doses: pre-rad, 100 krad (SiO_2), 300 krad (SiO_2), 500 krad (SiO_2), 1 Mrad (SiO_2), 2 Mrad (SiO_2), and 5 Mrad (SiO_2). (b) Inverse Gummel of the *pnp* for pre-rad and 5 Mrad (SiO_2). Solid lines are J_C and dotted lines are J_B.

To see the impact of TID on β, the normalized β as a function of V_{BE} for 3 different doses is plotted on Fig. 26. A similar behavior as the *npn* is observed, with the expected large change at low and medium injection and an additional decrease at high injection. Once again, J_C showed minimal change ($< 5\%$) with accumulated dose, and therefore J_B was the limiting factor and the normalized I_B is plotted on Fig. 27. The same trend as the *npn* is observed, with a 10-50% change in I_B at large

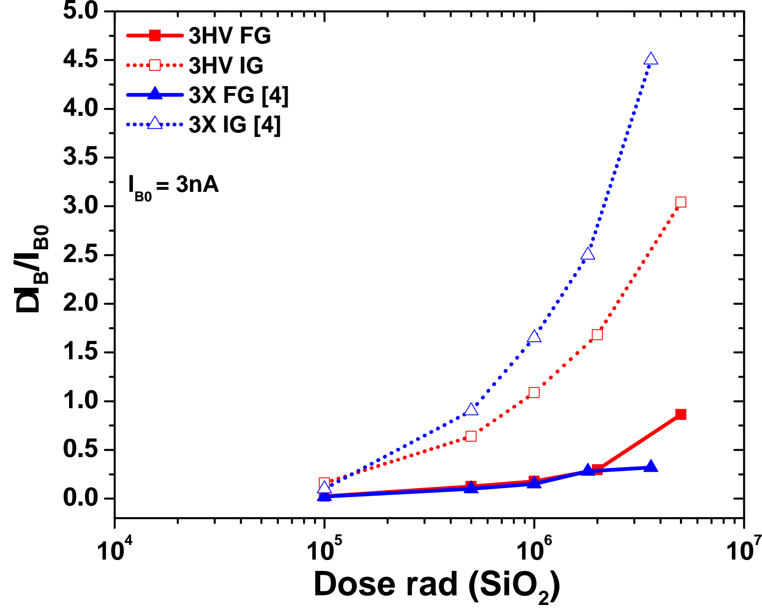

Figure 25: Excess normalized I_B for the *pnp* as a function of dose. The 3X technology is compared with the results for the 3HV platform for both forward and inverse-mode.

V_{BE} with increasing dose.

The HV bias condition was tested next and compared with the grounded condition in Fig. 28. Similar to the *npn*, minimal differences are observed between the grounded and HV bias condition for forward-mode operation. A more significant difference is observed, however, in the inverse-mode operation. This implies that with higher bias, there is lower residual charge at the oxide, which results in smaller accumulation of electrons in the base. One possible explanation is that the electric-field aligns to prevent electrons and holes from being efficiently separated at the oxide due to the incident radiation. We are presently attempting to confirm this via simulations.

In order to demonstrate that the measured J_B leakage in both forward-mode and inverse-mode were due to EB spacer oxide and STI charge/interface traps, a calibrated TCAD model was built for the *npn*. Charge/interface traps that would manifest

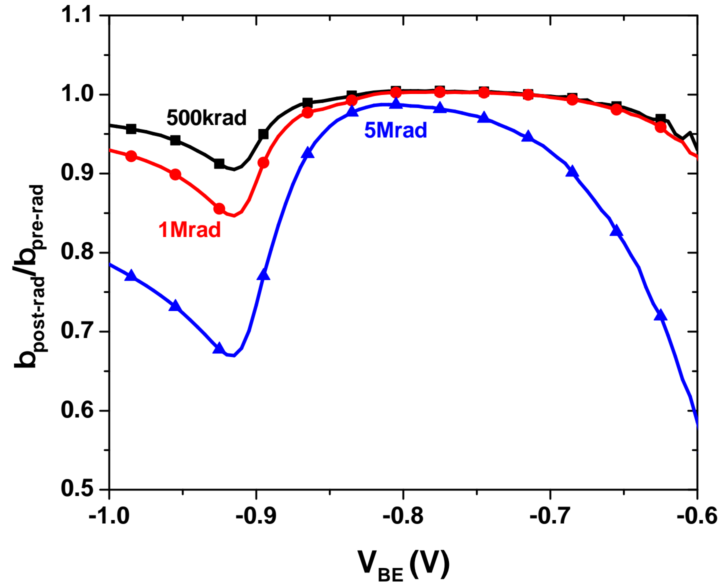

Figure 26: Normalized current gain (grounded condition) post- and pre-radiation for the *pnp* as a function of V_{BE} for the following cumulative doses: 500 krad (SiO_2), 1 Mrad (SiO_2), and 5 Mrad (SiO_2).

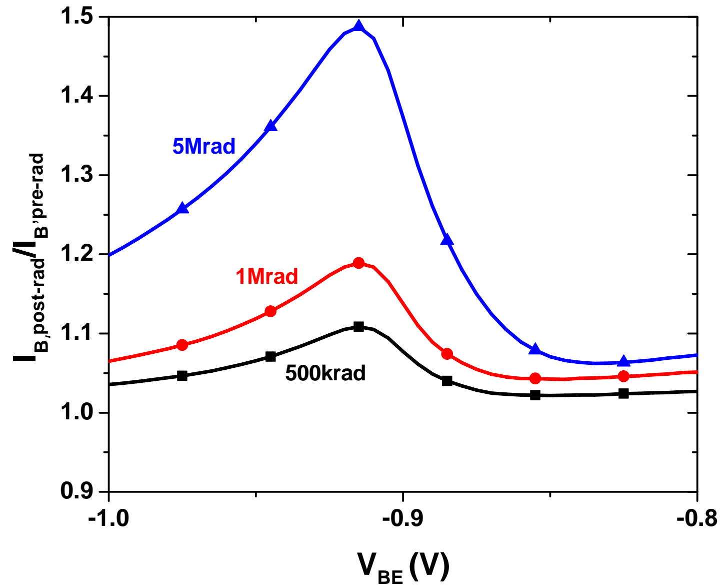

Figure 27: Normalized I_B (grounded condition) post- and pre-radiation for the *pnp* as a function of V_{BE} for the following doses: 500 krad (SiO_2), 1 Mrad (SiO_2), and 5 Mrad (SiO_2). Only the high-injection bias is shown.

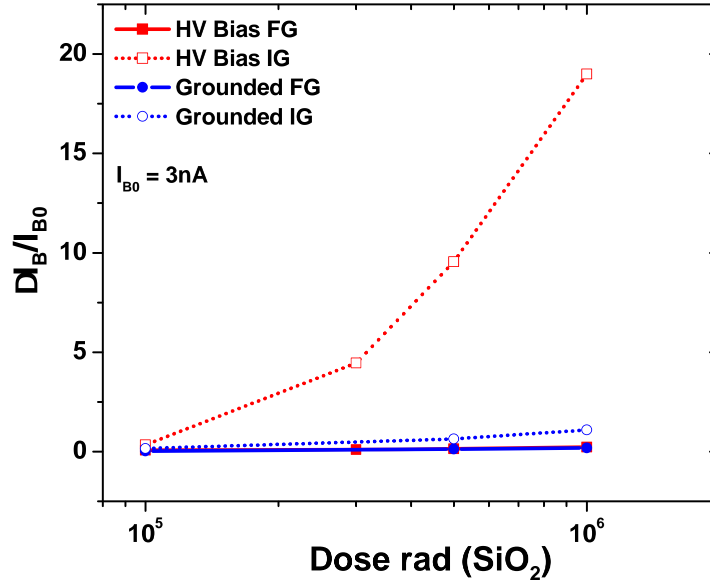

Figure 28: Excess normalized I_B for the *pnp* as a function of dose for forward and inverse-mode grounded and HV bias condition.

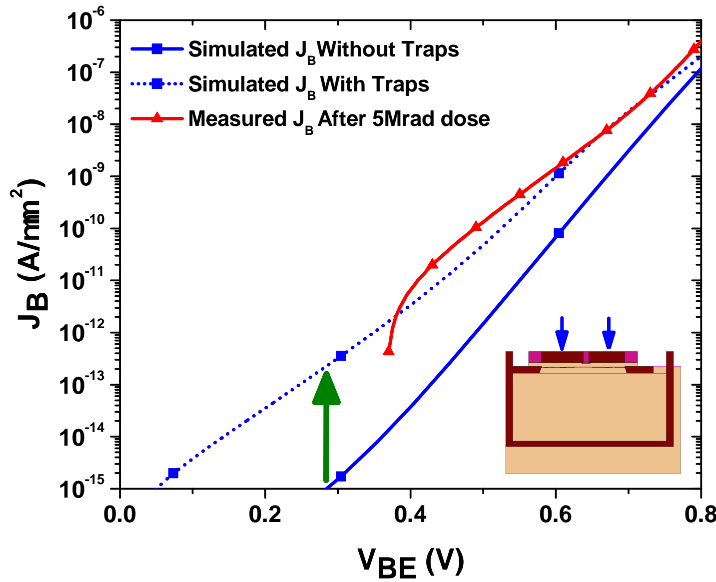

Figure 29: TCAD simulated J_B (forward-mode) for the *npn* with and without EB spacer interface traps and charges compared with measured J_B after 5 Mrad (SiO_2) cumulative dose (grounded condition).

themselves from TID exposure were placed at the various oxides within the TCAD device model, and the responses in both forward and inverse-mode were simulated.

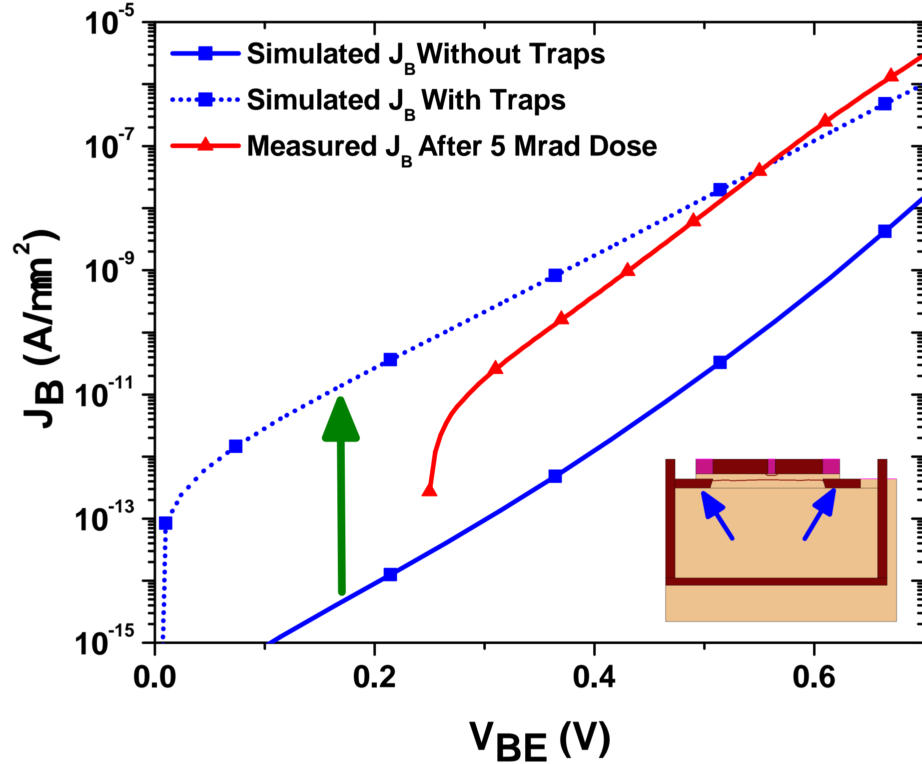

Figure 30: TCAD simulated J_B (inverse-mode) for the *npn* with and without STI interface traps and charges compared with measured J_B after 5 Mrad (SiO_2) cumulative dose (grounded condition).

The results are shown in Fig. 29 and Fig. 30. Fig. 29 illustrates the J_B shift with interface traps and charge at the EB spacer oxide in the forward Gummel. An ideality factor of approximately 1.6 was measured in both measured and simulated results. Fig. 30 demonstrates the J_B shift with traps and charge at the STI oxide in the inverse Gummel. A similar shift is observed; however, the ideality factor is not a complete match. This deviation is likely a result of the inverse-mode calibration, which is not as closely matched as the forward-mode. Nevertheless, the trend is consistent with measured results. Traps and charges were also placed at the other oxides such as deep trench isolation (DT) and BOX. There was no observable difference in DC behavior with traps or charge at these oxides. This is an expected result as these oxides are too far from the base to have a profound effect on the base current.

3.4 Summary

The total dose effects of a complementary thick-film SOI SiGe HBTs were explored and it was shown that the devices show multi-Mrad tolerance consistent with other SiGe platforms. A bias dependence in damage was observed, especially in inverse mode operation, which has not been reported or explored in detail before. Significant changes in the high injection base current was also observed with high doses which is likely due to change in the nonlinear collector resistance. TCAD simulations addressing the high injection J_B change with dose along with the effect of other types of TID (proton etc.) on 3HV will need to be looked at for future work. The implications of this work bode well for the utilization of emerging high-voltage SiGe technologies in space systems.

CHAPTER IV

CONCLUSION & FUTURE WORK

4.1 Summary

This thesis has presented the operation of thick-film SOI SiGe HBTs in two extreme environments: high temperature (up to 300°C) and radiation. For the first time, the DC, AC, and thermal performance of thick-film SiGe HBTs at temperatures up to 300°C were characterized and analyzed. While the HBT shows degradation in some key parameters such as current gain and f_T and f_{max}, it is still high enough to use in a plethora of RF applications. Additionally, for the first time, we looked at the effect of strong self-heating and thermal runaway with increasing temperature. We illustrate that while the thermal resistance increases with increasing temperature, the devices are electrically constrained by BV_{CEO} at extremely high temperatures (>150°C) than thermally constrained. Thus, the safe-operating-area (SOA) is not thermally dominated with increasing temperature.

The impact of radiation on a high-voltage thick-film SOI SiGe HBT was also explored. Both a grounded condition and high-V bias condition were tested to see the effect of bias on the TID response. The devices showed strong TID tolerance up to 1 Mrad, however, with increasing dose, an interesting phenomena was observed where there was a significant increase in the base current at high injection which led to a 40% decrease in the current gain. From TCAD simulations, it was seen that this was due to an increase in collector resistance. As for the effect of bias, the devices showed no bias dependence in the TID response in forward mode but inverse mode showed a significant bias dependence as the high-V bias condition showed much higher base current degradation. This was shown to be a mainly an effect of the large electric field

that efficiently separated the electron-hole pairs at the STI oxide leading to larger charge and interface traps.

4.2 Future Work

While we illustrated the DC & AC performance of a thick-film SOI SiGe HBT at high temperatures, more reliability data needs to be obtained to truly access the viability of these devices at high temperatures. Mixed-mode damage has been already shown to decrease with increasing temperature, however, high-current (Auger) induced damage has a positive temperature coefficient. Therefore, it needs to be verified as to how the SOA shrinks at high temperatures at high current densities. Linearity measurements at high temperatures will also be vital in understanding the implications of operating an RF circuit at these extreme conditions.

As for the radiation effects, a more detailed TCAD model needs to be built to better understand how TID causes a change in the collector resistance. The use of other types of radiation sources will also be more useful in gauging the TID tolerance of these high-voltage HBTs.

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