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Control Strategy for a Modified Cascade Multilevel Inverter with Dual DC Source for Enhanced Drivetrain Operation

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***Abstract*— This paper presents a new control strategy for a modified cascade multilevel inverter used in drivetrain operations. The proposed inverter is a three-phase bridge with its dc link fed by a dc source (battery), and each phase series-connected respectively to an H-bridge fed with a floating dc source (ultracapacitor). To exploit the potentials of the inverter for enhanced drivetrain performance, a sophisticated yet efficient modulation method is proposed to optimise energy transfer between the dc sources and with the load (induction motor) during typical operations, and to minimise switching losses and harmonics distortion. Detailed analysis of the proposed control method is presented, which is supported by experimental verifications.**

Keywords — Multilevel inverter, dual energy source, switching strategy, drivetrain.

I. INTRODUCTION

The performance of conventional drivetrains is usually limited by the capability of the energy sources such as batteries when the electric motor can easily be overloaded for short durations. In addition, high dc voltage is required to overcome the back EMF generated by the motor during high speed [17-19]. A common approach is to incorporate high power density sources such as ultracapacitors (UC). The most established solution that allows power flow between batteries and UC is realized by parallel connection of bidirectional DC/DC converters [1-11]. More recently, hybrid configurations with multi-level inverters are proposed to provide better utilization of battery and UC as well as increased available voltage output [16-22]. Moreover, incorporation of multilevel inverters has shown the potential benefits of reducing torque ripple, harmonic distortion and switching losses [18]. This paper presents a detailed analysis on a modified cascade multilevel inverter supplied by a dual-DC source against realistic constraints. Based on the analysis, a new control strategy that optimizes the inverter performance in the whole operating range is proposed and implemented.

II. TOPOLOGY OF INVERTER MOTOR DRIVE

The multilevel inverter under study is shown in Fig.1. It consists a three-phase bridge with the main DC link fed by a single dc source (battery), and each phase series-connected respectively to an H-bridge fed with a floating DC source (ultracapacitor) where the voltage is allowed to vary depending on energy stored. This type of modified cascade multilevel inverter is selected since the structure is known to deliver a high number of output voltage levels for relatively low number of switches, and that the dc sources are isolated [18-21]. The output phase voltage (V_{an}, V_{bn}, V_{cn}) of the inverter in reference to the centre point "n" of the main voltage source can be described as a function of battery voltage (V_{bat}), ultracapacitor

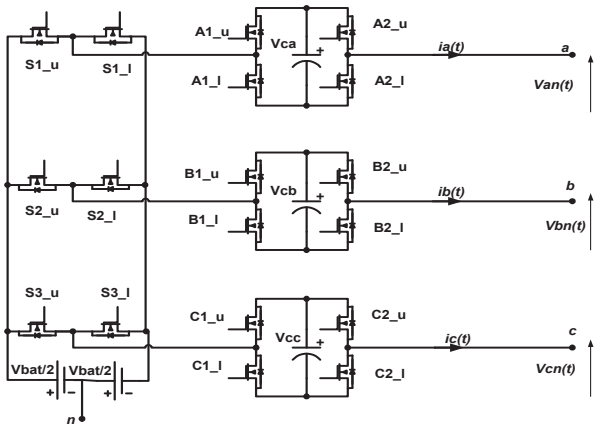

Fig 1. Modified cascade inverter with 3-phase inverter and three H-bridges.

voltage ($V_{uc\_a}, V_{uc\_b}, V_{uc\_c}$) and switch combinations (S1,S2,S3,A1,A2,B1,B2,C1,C2) as summarised by the following equations:

$$V_{an} = \frac{V_{bat}}{2} * (2 * S1 - 1) + V_{uc\_a}(A2 - A1) \quad (1)$$

$$V_{bn} = \frac{V_{bat}}{2} * (2 * S2 - 1) + V_{uc\_b}(B2 - B1) \quad (2)$$

$$V_{cn} = \frac{V_{bat}}{2} * (2 * S3 - 1) + V_{uc\_c}(C2 - C1) \quad (3)$$

Converting those three-phase voltages in time domain by Clark *alpha-beta* transformation into stationary space vectors two phase plane (V_{alpha}, V_{beta}), it becomes possible to generate 512 voltage vectors. It is because for nine top and bottom switches there are 2^9 combinations.

$$V_{alpha} = \frac{2}{3}(V_{an} - \frac{1}{2}V_{bn} - -\frac{1}{2}V_{cn}) \quad (4)$$

$$V_{beta} = \frac{\sqrt{3}}{3}(V_{bn} - V_{cn}) \quad (5)$$

Since the aim of ultracapacitors is to provide additional power during acceleration or to recuperate energy from braking, their voltage will vary depending on state of charge. This results in available voltage vectors being not constant and the traditional Space Vector Modulation (SVM) for multilevel inverters cannot be implemented without modification, as illustrated in Fig.2 [13-14]. To simplify analysis it is assumed that the voltages on all three sources that supply the H-bridges are equal since the regulator controls them to the same capacitor reference voltage. Simultaneously switching different combinations of the three-phase inverter and the H-bridges provides the enhanced capability to control power flow between batteries, UC's and the motor and at the same time to generate precise voltage vectors with reference amplitude.

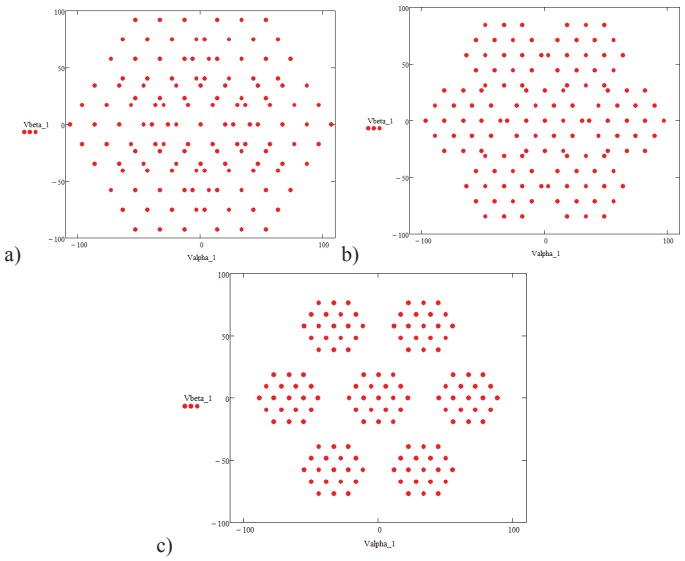

Fig. 2: Variations of voltage vectors for different DC voltage ratios on stationary alpha beta plane: a) V_{bat}=3.4V_{cap}, b) V_{bat}=4.2V_{cap}, c) V_{bat}=6V_{cap}.

III. SWITCHING STRATEGIES

For voltage ratios between the main voltage source and ultracapacitor $\left({V_{bat}}/{V_{cap}}\right)$ that are integer and if that ratio is lower or equal to four it is possible to achieve redundant vectors. For non-integer supply voltage ratios each vector is unique since it can be generated only by one switching combination (without considering individual redundant switching states for H-bridges and three-phasebridge). It is easy to observe in Fig.2 that with the increase of the voltage ratio between inverter sources the gaps between vectors start to appear. This means that modulated vectors with circular trajectory that have transitions through those areas, the closest vectors will require change in high number of switching states both in three-phase bridge and H-bridges. This might cause high switching losses and large ripples in the output voltage since transition through the 'undesirable' vectors is needed. Additionally modulation solution between the closest vector could have different power share between sources from the required. To overcome the problem the strategy where the H-Bridges are switched at fundamental frequency and three-phase bridge is responsible for SVM has been implemented as shown in Fig.3 (a). In opposite situation when the ratio between the sources gets smaller the H-bridges hexagon envelope for the closest vectors in three-phase bridge starts to overlap as shown in Fig.3 (b). In this case depending when vector transition in three-phase bridge occurs the proportion of power delivered between sources might be adjusted.

To create switching strategy for the hybrid cascade multilevel inverter where amplitude of auxiliary voltage source is at last 50% lower than the main source voltage and can go down to less than 5%, six main operating modes are identified. By finding the output voltage limitation for each mode and expected output power, optimum configuration can be selected during the whole operating range for various UC's voltage. Calculation for the power distribution is simplified by the assumption that the motor current vector (I) seen by inverter is ideally sinusoidal.

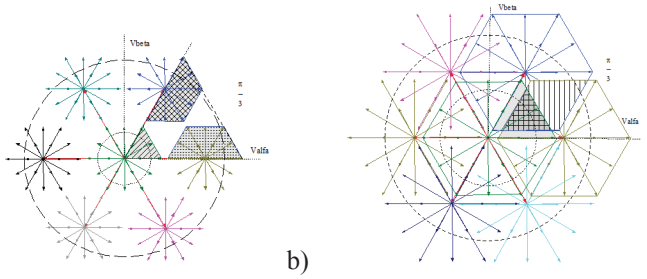

Fig 3. Overlapping of voltage vectors when the voltage ratio between the sources vary.

MODE I: Only three-phase bridge operates in SVM like a standard three-phase voltage source inverter. All H-bridges will stay in "00" position (A1,A2,B1,B2,C1,C2 are 0), meaning that only lower switches are on. For this switching strategy inverter has only six active and two zero voltage vectors. The amplitude of the active vectors is 2/3 of supply voltage. For standard SVM in this mode without over modulation the maximum amplitude of rotary voltage vector equals radius of the circle that can be inscribed inside hexagon ($V_{I\_max} = \frac{V_{bat}}{\sqrt{3}}$) as presented on Fig. 4.

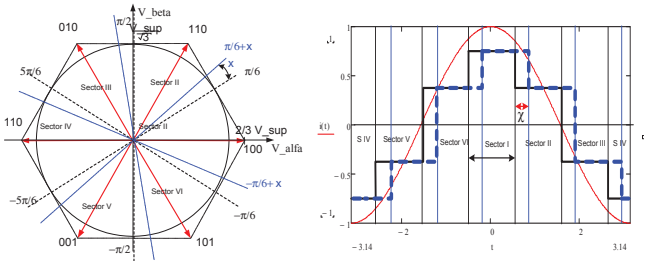

Fig 4. Available voltage vectors for three-phase bridge (red vectors) with corresponding sectors(left).Current and six step voltage in time domain with and without phase shift(right) .

For inverter operations when only three-phase bridge is active it is obvious that power delivered from dc source (P_{bat}) has to be equal to power dissipated at load (P_{out}) if inverter losses are omitted. This can be presented as simple product of battery current (I_{bat}) and its voltage (V_{bat}) or product of reference voltage (V_{ref}) vector, motor current in stationary *alpha-beta* plane (I) and power factor ($\cos(\emptyset)$).

$$P_{out} = P_{bat} = V_{bat} * I_{bat} = \frac{3}{2} V_{ref} * I * \cos(\emptyset)\,, P_{uc} = 0 \qquad (6)$$

MODE II: In this mode three-phase bridge is switched at fundamental frequency and remaining H-Bridges operate in SVM mode. Each active vector of three-phase bridge is switched on for one sixths of fundamental frequency forming six step waveform. The H-bridges are mainly used to minimise voltage error and harmonic, and depends on amplitude of reference voltage to sink or source energy. In Fig.4 six sectors and corresponding voltage vectors for three-phase bridge are illustrated. Additionally the phase shift angle (χ) has been marked to present how the sectors in which voltage vectors are activated can be adjusted according to the output power requirement. The power delivered by the main source can be calculated as integral of current seen by the source and product of its voltage as presented in equation (7).

$$P_{bat} = \frac{3}{\pi}\int_{-\frac{\pi}{6}}^{\frac{\pi}{6}} V_{bat} * I * \cos(\omega t + \emptyset + \chi)dt = \quad (7)$$
$$= \frac{3}{\pi} V_{bat} * I * \cos(\emptyset + \chi),$$

In Fig.5 the current that is sourced by battery has been presented to illustrate the influence of power factor on output power. Introduced phase shift (χ) angle will have similar effect on main source power.

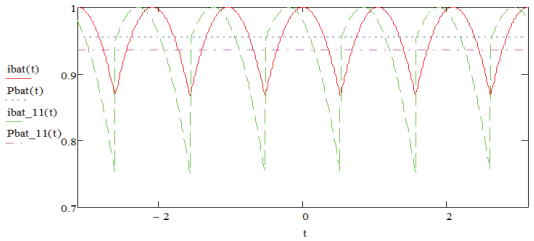

Fig 5. Current seen by main source for resistive load ibat(t)(red) and for RL load ibat_11(t)(green) and corresponding output power.

In Fig.6 the graph with possible switching combinations for active "100" (S=1,S2=0,S3=0) voltage vector in three-phase bridge and its limiting hexagon is presented. It is noted that for this mode the key to operate inverter is to find its limitations. The maximum amplitude of output voltage vector is $2\frac{(V_{bat}+2V_{uc})}{3}$ so the maximum output voltage has to be smaller than $V_{II\_max} = \frac{(V_{bat}+2V_{uc})}{\sqrt{3}}$. Additionally the smallest voltage vector in this configuration has to be higher than $V_{II\_min} = 2\frac{(V_{bat}-2V_{uc})}{3}$. In Fig.6 the grey ring marks the amplitude of voltage vector that can be generated through whole sector $(-\frac{\pi}{6}, +\frac{\pi}{6})$ for vector vector "100". For a set reference within the grey area it is possible to add or subtract phase shift angle "χ" to either increase (only if $\cos(\emptyset) < 1$) or to reduce power delivered by the main source. The maximum phase shift angle can be calculated from following equations where the smallest value should be used.

$$\chi_1 = arcsin\left(\frac{2V_{uc}}{\sqrt{3}\,V_{ref}}\right) - \frac{\pi}{6} \text{ and } \chi_2 = \frac{\pi}{3} - arcsin\left(\frac{V_{bat}-2V_{uc}}{\sqrt{3}\,V_{ref}}\right) \quad (8)$$

MODE III: Modulation strategy where H–bridges are only active in SVM and three-phase bridge is in "000" zero vector state (or "111"). The amplitude of the rotary output voltage vector is limited to ($V_{III\_max} = \frac{2V_{uc}}{\sqrt{3}}$) and the whole power required by output is delivered by ultracapacitors (P_{uc}).

$$P_{uc} = \frac{3}{2} V_{ref} * I * \cos(\emptyset) = P_{out} \quad , P_{bat} = 0 \quad (9)$$

The SVM modulation for H-bridges needs additional control to keep all three ultracapacitors voltage at same level. For normal operations the symmetrical switching of voltage vectors provides good results but drift might appear for variable load. In Fig.7 two switching combinations (" a" and "b") that can be used to generate redundant reference voltage vector for two level and three level operations are presented. In case voltage of a capacitor exceeds the average value over the set threshold then for 1/6th of period the switching configuration where capacitor is sourcing less current is chosen ("b" combination).

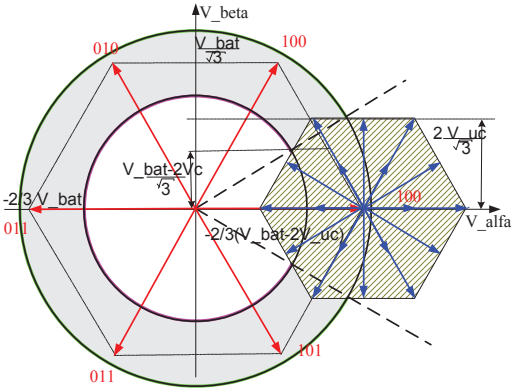

Fig.6 Modulations limits for strategy with three-phase bridge in six step mode and H-bridges in SVM, (grey ring) Red vectors represents switching states for three-phase bridge, blue vectors are switching states of three H-Bridges .

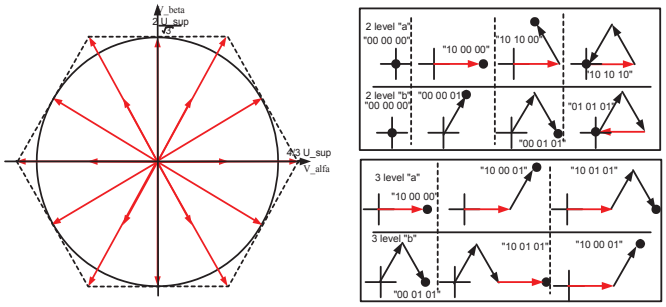

Fig 7. Available voltage vectors for three H-bridge only and redundant voltage vectors combinations to control capacitors voltage

MODE IV: The H–bridge's operates in six-step mode at fundamental frequency where only one H-bridge is active at the same time (each H-bridge active through 1/3 of period) and a three-phase bridge is compensating harmonics by SVM. Similarly to MODE II the active power delivered by ultracapacitors can be calculated as an integral of active power seen by three H-bridges what is simplified to equation (10).

$$P_{ucap} = \frac{1}{\pi}(V_{uc\_A} + V_{uc\_B} + V_{uc\_C}) * I * \cos(\emptyset + \chi) \quad (10)$$

The profile of instantaneous power seen by each source and its average value is presented in Fig.8. The maximum output voltage in this configuration equals to $V_{IV\_max} = \frac{V_{bat}+V_{uc}}{\sqrt{3}}$. Additionally it is possible to change sign of active power flowing from ultracapacitors by setting phase shift angle "χ" opposite to motor current vector ($\chi = \phi \pm \pi$) that allows to generate the maximum output voltage limited to $V_{N\_IV\_max} = \frac{V_{bat}-V_{uc}}{\sqrt{3}}$ as shown in Fig. 9. For the ratio between main source and ultracapacitor higher than two, the modulation can be performed through the whole sector. Power sharing control by phase shifting "χ" for amplitude of reference voltage $V_{ref} < V_{N\_IV\_max}$ can be performed for any angle. If the reference voltage is higher than $V_{N\_IV\_max}$ the maximum phase shift is limited by ratio between amplitude of main dc source and reference vector according to equation 11. Additionally for $V_{ref} > V_{N\_IV\_max}$ maximum phase shift angle has been defined as χ_{max} to simplify control.

$$\chi = arcsin\left(\frac{V_{bat}}{\sqrt{3}\,V_{ref}}\right) - \frac{\pi}{6}, \quad \chi_{max} = arctg\left(\frac{\sqrt{3}V_{bat}}{2V_{uc}-V_{bat}}\right) - \frac{\pi}{6} \quad (11)$$

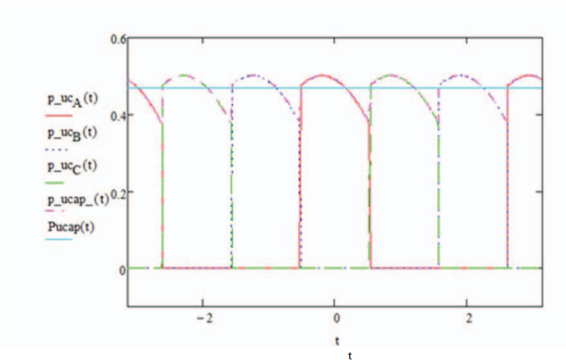

Fig.8 Current sourced by ultracapacitors in mode IV, red- UC in phase A, blue doted –UC in phase B, green - UC in phase C, purple- instantaneous power from three UC's, blue- average power from H-Bridges

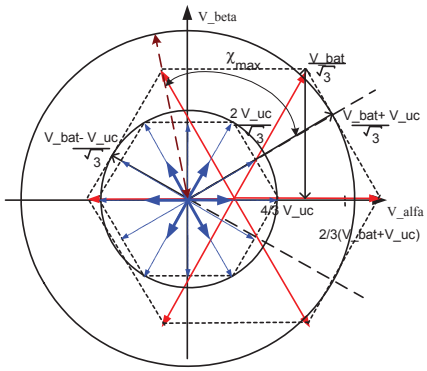

Fig.9 Limitation of modulation scheme with H-Bridges switched at fundamental frequency (mode IV). Blue vectors are switching combinations of three H-Bridges, red vectors are switching combinations of three-phase bridge.

MODE V: To increase power flow from H-bridges, it is possible to extend mode IV by modifying six step switching sequence with two H-bridges active at the same time. Since two adjacent vectors are switched on together, the operating sector shifts by $\pi/6$. Solving integral of the instantaneous power seen by all three H-bridges gives equation (12) that calculates power sourced by UC's. The profile of instantaneous power, its sum and average value is shown in Fig.10.

$$P_{ucap} = \frac{\sqrt{3}}{\pi}\left(V_{uc_A} + V_{uc_B} + V_{uc_C}\right) * I * \cos(\emptyset + x) \qquad (12)$$

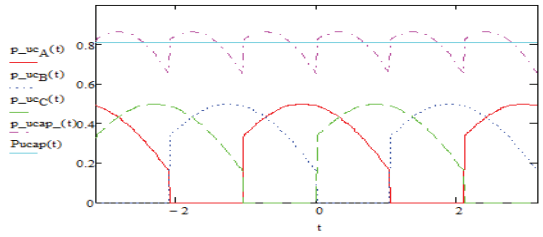

Fig.10 Current sourced by ultracapacitors in mode V, red- UC in phase A, blue doted –UC in phase B, green - UC in phase C, purple- instantaneous power from three UC's, blue- average power from H-Bridges

In Fig. 11 we can find that the maximum modulated voltage is $V_{V\_max} = \frac{2(V_{bat}+V_{uc})}{3}$ and for six-step waveform phase shifted by $\pm\pi$ the output has to be smaller than $V_{N\_V\_max} = \frac{V_{bat}-2V_{uc}}{\sqrt{3}}$. The phase shift power control is limited by equation (13) where maximum angle to simplify control is limited to χ_{max}.

$$\chi = arcsin\left(\frac{V_{bat}+V_{uc}}{\sqrt{3}\,V_{ref}}\right) - \frac{\pi}{3},\ \chi_{max} = arctg\left(\frac{V_{bat}+V_{uc}}{\sqrt{3}\left(V_{uc}-\frac{1}{3}V_{bat}\right)}\right) - \frac{\pi}{3} \qquad (13)$$

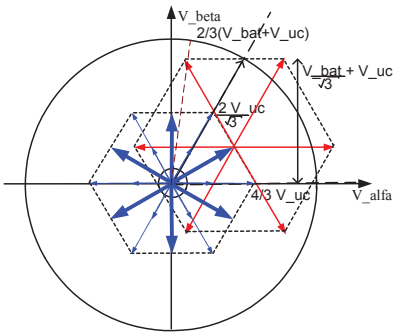

Fig.11 Limitation of modulation scheme with H-Bridges switched at fundamental frequency (mode V). Blue vectors are switching combinations of three H-Bridges, red vectors are switching combinations of three-phase bridge.

MODE VI: To achieve maximum output power from H–bridges it is proposed to keep all three ultracapacitors active in six step mode at fundamental frequency. The power by H-Bridges doubles in comparison with mode IV as predicted by equation (14), and is shown in Fig 12.

$$P_{ucap} = \frac{2}{\pi}\left(V_{uc\_A} + V_{uc\_B} + V_{uc\_C}\right) * I * \cos(\emptyset + x) \qquad (14)$$

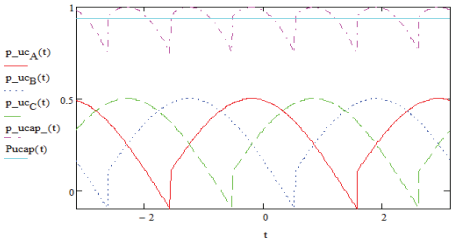

Fig.12 Current sourced by ultracapacitors in mode VI, red- UC in phase A, blue doted –UC in phase B, green - UC in phase C, purple- instantaneous power from three UC's, blue- average power from H-Bridges

Fig.13 shows that the maximum modulated voltage $V_{VI\_max} = \frac{V_{bat}+2V_{uc}}{\sqrt{3}}$ and for six-step waveform phase shifted by $+\pi$ or $-\pi$ the output has to be smaller than $V_{N\_VI\_max} = \frac{V_{bat}-2V_{uc}}{\sqrt{3}}$. The available phase shift power control for given reference vector becomes limited by equation (15):

$$\chi = arcsin\left(\frac{V_{bat}}{\sqrt{3}\,V_{ref}}\right) - \frac{\pi}{6}, \chi_{max} = arctg\left(\frac{\sqrt{3}\,V_{bat}}{4V_{uc}-V_{bat}}\right) - \frac{\pi}{6} \qquad (15)$$

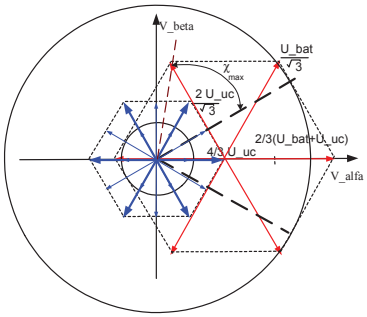

Fig.13 Limitation of modulation scheme with H-Bridges switched at fundamental frequency (mode VI). Blue vectors are switching combinations of three H-Bridges, red vectors are switching combinations of three-phase bridge.

The above analysis provides the voltage limits, which depend on UC's state of charge, for all switching strategies as shown in Fig.14. By selecting suitable strategy it is possible to modulate voltage vector from 0V up to ($\frac{V_{bat}+2V_{uc}}{\sqrt{3}}$). The negative voltage symbolizes modulation with 180° phase shift ($\chi = \pm\pi$).

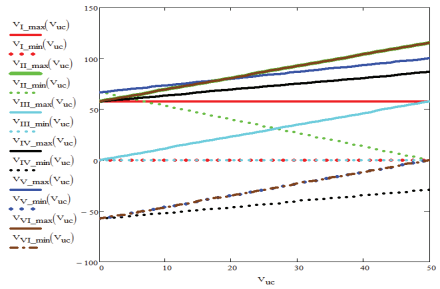

Fig.14 Voltage limits for all switching configuration in relation to auxiliary source voltage , solid line – maximum voltage, dotted line – minimum voltage .

To understand power sharing for above switching modes, typical calculations of power delivered by sources for variable phase shift angle between ($\chi < -\frac{\pi}{6}, +\frac{\pi}{6} >$) at with p.f. $\cos(\emptyset) = 0.966$ are shown in Fig.15 ($V_{bat} = 100V, V_{uc} = 50V$). It is clear that it is not always possible with phase shift control to produce required power from sources. Strategies where H-bridges operate in SVM mode are marked with bold lines in Fig.15.

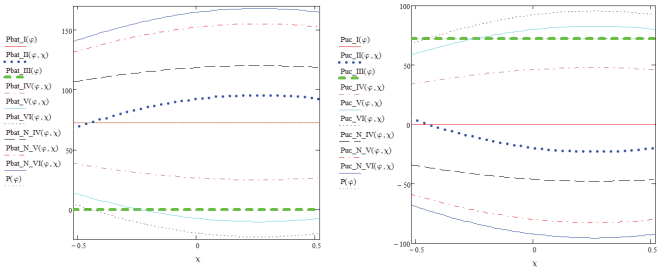

Fig.15 Power sharing regulation with phase shift angle "χ" for all switching modes at p.f =0.966: Battery (left); UC (right)

As mentioned previously the phase shift control is limited by hexagon boundaries of voltage vectors specific to each mode. Since inverter has six symmetrical sectors it is proposed to alternate between two switching modes twice per every one sixth of the period. To control power the switch angle $\propto$ has been defined that can be set from 0 up to $\frac{\pi}{6}$ as shown in Fig.16. In this modulation scheme output voltage is limited by the smallest maximum output voltage from two selected switching strategies.

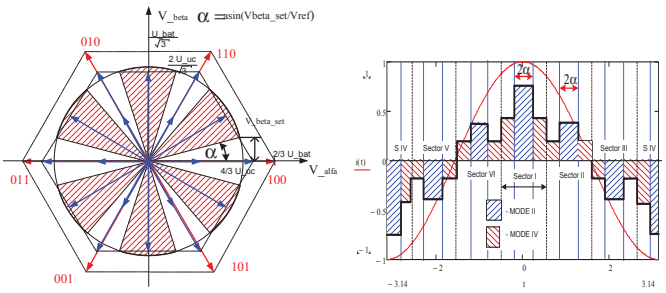

Fig.16 Principles of mixed switching strategy presented in alpha beta coordinates (left), Current and mixed six step voltage for alpha axis in time domain (right)

By solving integrals of instantaneous power for two combined modulation strategies alternating at defined angle (α) the following example power control equations are formulated:

Mode I and III:

$$P_{bat} = \frac{6}{\pi} * P_{out} * \alpha \ , \ P_{ucap} = \left(1 - \frac{6}{\pi}\alpha\right) * P_{out} \quad (16)$$

Mode I and II:

$$P_{bat} = \frac{3}{\pi} V_{bat} I \cos(\emptyset + x)\, 2\sin(\alpha) + \frac{3}{2} V_{ref} I \cos(\emptyset)\left(1 - \frac{6}{\pi}\alpha\right) \quad (17)$$

Mode II and III:

$$P_{bat} = \frac{3}{\pi} V_{bat} * I * \cos(\emptyset + x) * 2\sin(\alpha) \quad (18)$$

Mode II and IV:

$$P_{bat} = \frac{3}{\pi} V_{bat} * I * \cos(\emptyset + x) * 2\sin(\alpha) + P_{out} - \frac{1}{\pi}\left(V_{uc_A} + V_{uc_B} + V_{uc_C}\right) * I * \cos(\emptyset + x) * (1 - 2\sin(\alpha)) \quad (19)$$

Mode V and VI:

$$P_{ucap} = \frac{1}{\pi}(V_{uc_A} + V_{uc_B} + V_{uc_C}) * I * \cos(\emptyset + x) * (\sin(\alpha) + \sqrt{3}\cos(\alpha)) \quad (20)$$

Fig.17 shows possible power control for various switching combinations with parameters $\chi = 0$, $\cos(\emptyset) = 0.966$, $V_{bat} = 100V, V_{uc} = 50V$, and that the strategy allows complete power sharing.

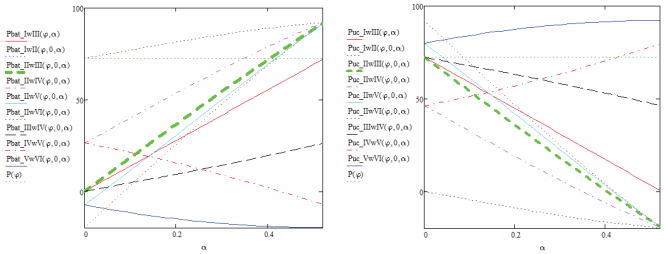

Fig.17 Power sharing regulation in mixed mode switching for various switching combinations, left graph power delivered by battery, right – power delivered by UC. (power factor $\cos(\emptyset) = 0.966$*)*

IV. Implementation of Modulation Strategy

Based on earlier analysis the control switching algorithm has been developed. In Fig.18, the block diagram of the proposed modulator is presented with following blocks:

1. Cartesian to polar transformation to calculate angular position of reference vector.
2. Comparator module generating switch signal to change modulation mode in each sector when voltage vector is crossing switch angle "α".
3. Lookup table with six-step switch combination for Mode I to Mode VI. The function includes voltage vector angle comparator to find switch combination adequate to sector. The voltage angle signal includes added phase shift (ϲ).
4. Estimator of six step voltage in alpha beta plane base on equations 1-5 and switch combination from block3.
5. Space Vector Modulation block to modulate remaining voltage error. The block include lookup table to find adequate voltage vectors and perform dwell times calculations for SVM.
6. 10 bit counter configure for discontinuous SVM to generate switching pulses for corresponding vectors and dwell times [23].

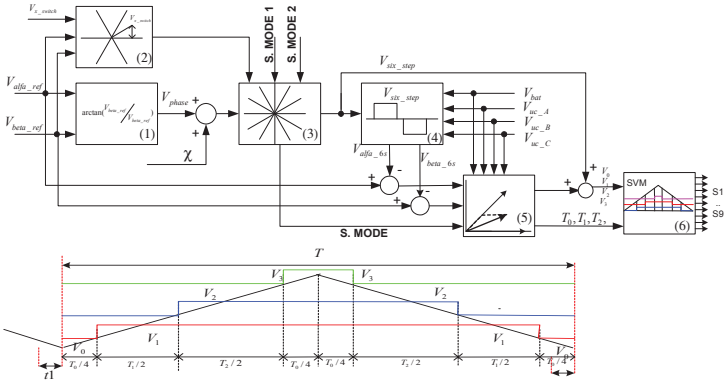

Fig.18 Block diagram of modulation algorithm for cascade multilevel inverter with variable sources voltage and power flow control.

The whole algorithm is synchronized with counter (block 6) and takes one count before counter overflow (t1) to calculate new switching pattern. The period T was set to 1024us with 1us resolution (t1) (Digital output card limitation). The whole modulator algorithm together with motor encoder, analogue signal conditioning, P and Q power estimator, flux and torque estimator has been implemented on cRIO-9112 FPGA (Virtex-5 LX30) with 19200 LUTs operating at 40MHz.

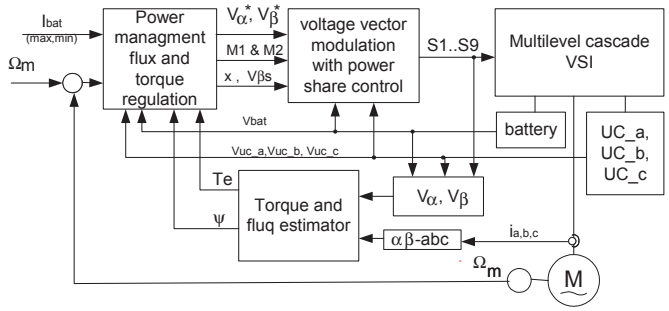

Fig.19 Block diagram of cascade multilevel inverter motor drive with power flow management.

The above modulator has been incorporated into motor drive system with Direct Torque Control and Power Management supervisory algorithm as shown in Fig.19. The Power Management is implemented in real-time system synchronized with SVM counter and base on selected operating modes. The power sharing control algorithm operates in three main steps:

1. The output reference vector is compared with maximum voltage that can be generated by each modulation scheme. Switching modes that are not able to provide sufficient output voltage become inhibited for further calculations.
2. The limiting phase shift angles for remaining modulation schemes are calculated, and the limits for phase shift control of power share are found.
3. Based on reference torque, motor speed, dc sources voltage and motor current, the reference power for main and auxiliary inverter is calculated. For each mode the expected power share by each source is estimated in order to find the operating mode that can provide the requested power distribution between sources.

The output from Power management module to the vector modulator includes voltage reference in alpha beta plane($V_{alfa\_ref}, V_{beta\_ref}$), two selected switching modes (S.

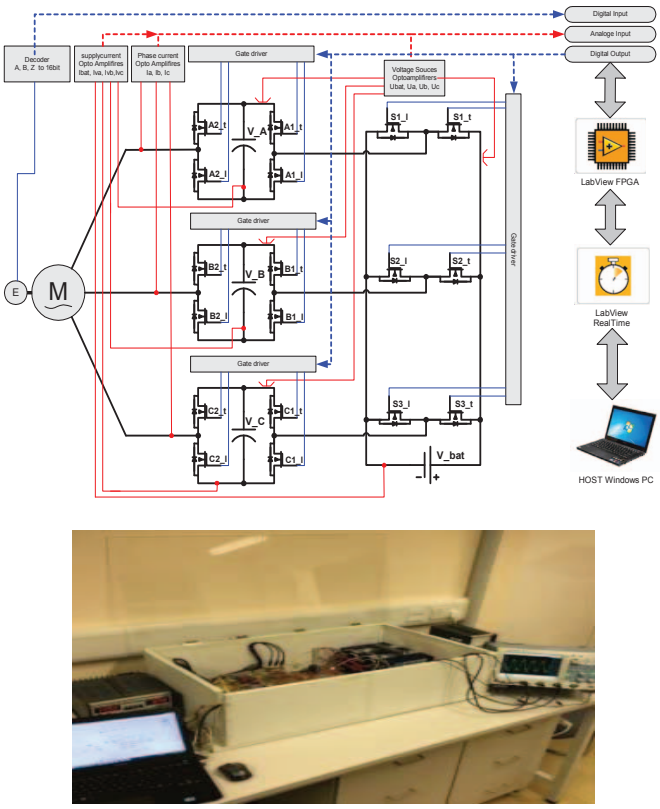

Fig.20 Prototype Validation: Block diagram (top) and realization (bottom)

MODE1 and S. MODE2), phase shift angle (χ) and angle (α) where modulation mode is changed from MODE1 to MODE2. Since it is desirable to use small vectors to minimise switching losses and distortions in output voltage, the modulation that use H-bridges is always prioritized (mode II and mode III).

V. EXPERIMENTAL VALIDATION

A prototype of the system is built for experimental validation. Fig. 20 shows the setup which includes: three-phase induction motor (delta configuration 230V, 370W, 2840rpm); modified cascade multilevel inverter; dc source (60V/120V); three sets of 45V ultracapacitors (Maxwell 19F UC's or 2mF electrolytic capacitors); voltage and current sensing circuit; NI Compact RIO Real Time platform NI cRIO-9012.

The operation where three-phase bridge is switched at fundamental frequency is to be used during most of the inverter operations. Fig.21 presents the typical waveforms captured in mode II for two different phase shifts *"χ"*. For the first maximum phase shift the current seen by the main source is minimized, while in second case the phase shift is optimized for battery maximum current (six step switching synchronized with phase of motor current). The change in phase shift allows the main source current to change by almost 25% without major impact on phase current. In case when UC's voltage is not sufficient for continuous six step switching or required power split in mode II cannot be met, then the mix switching operation has to be used. Typical waveforms for mixed operation including mode II and IV with α=π/12 are presented in Fig.22. The mode change will not introduce switching ripples other that ripples specific to the modulation mode. In the presented example the amplitude of the main source is

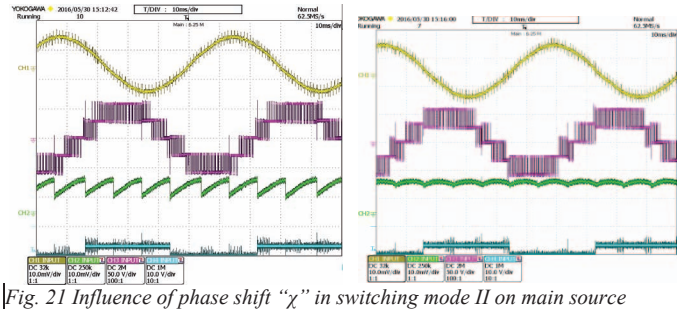

Fig. 21 Influence of phase shift "χ" in switching mode II on main source current . Channel 1(yellow)motor phase A current, Channel 2(green)battery current, Channel3 (purple) voltage between phase A and B, Channel4(blue)3phase bridge phase A gate signal.

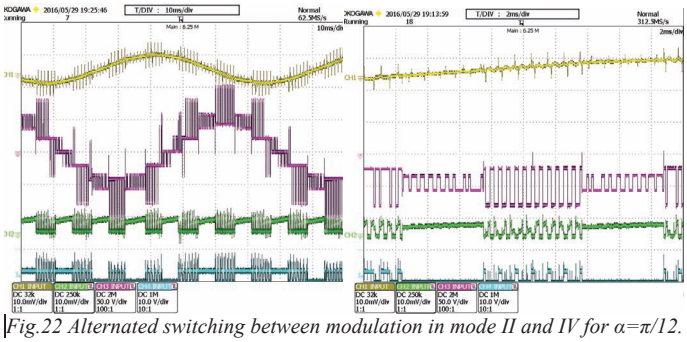

Fig.22 Alternated switching between modulation in mode II and IV for α=π/12. Channel 1(yellow)motor phase A current, Channel 2(green)battery current, Channel3 (purple) voltage between phase A and B, Channel4(blue)3phase bridge phase A gate signal.

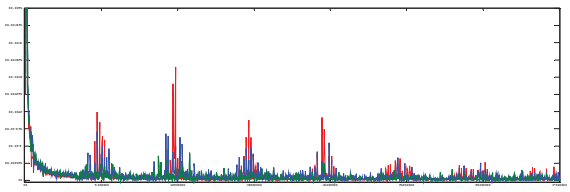

Fig. 23 Comparison of harmonic content in phase current for modulation in mode II (green), mode IV (red) and mixed mode including switching II and IV for α=π/12(blue).

around three times bigger than amplitude of ultracapacitors what is related with around three times higher current ripples when main source is used in SVM.

In Fig.23, the harmonic analysis proves that mixed modulation scheme has harmonic content that is proportional to average level o two modulation schemes. Fig.24 shows another example where maximum output from inverter is generated and the ratio between sources voltage is close to four. This produces maximum number of levels (six voltage levels in phase to phase voltage) which helps to minimise ripples in motor current. Since between vectors in mode II empty spaces might start to appear as UC's discharge and power sharing is limited, the modulation in mode VI is activated. Because the percentage of mode VI in modulation is small, the increase in motor current ripples is insignificant.

Mixed modulation strategy is found to be also efficient for capacitors voltage control. In experiment with 2mF capacitance as a source for H-Bridge, it was proven that for whole range of output voltage it was possible to keep capacitors voltage with constant amplitude. Fig.25 captures the waveforms showing variation of capacitors voltage where the average value remains stable (around 35V where main source voltage is 62V) and only small variations related with its switching appears. For

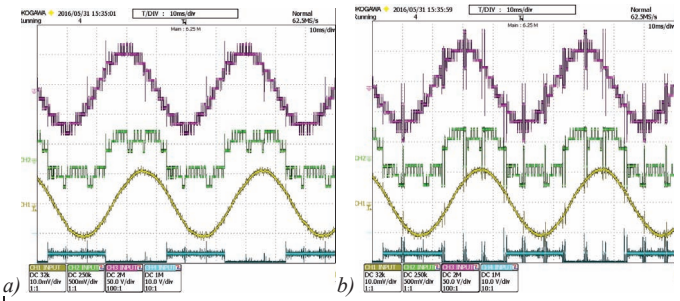

Fig. 24 Modulation of output voltage with six step switching of 3phase bridge a) mode II only, b)mode II with added mode VI. Channel 1(yellow)motor phase A current, Channel 2(green) phase A line voltage, Channel3 (purple) voltage between phase A and B, Channel4(blue)3phase bridge phase A gate signal.

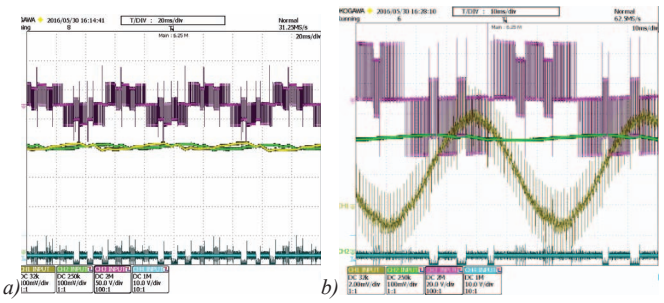

Fig. 25 Capacitors voltage level control for mixed mode II and III for low output voltage. a) Channel 1(yellow) capacitor voltage in phase B b) Channel 1(yellow)motor phase A current, Channel 2(green) capacitor voltage in phase B, Channel3 (purple) voltage between phase A and B, Channel4(blue)3phase bridge phase A gate signal

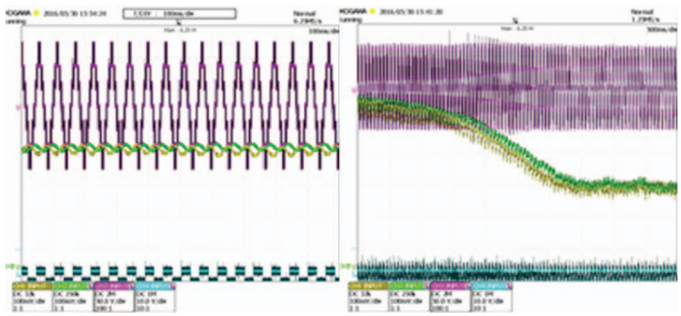

Fig. 26 Capacitors voltage level control for mode II modulation with phase shift and its respond to capacitors reference voltage change. Channel 1(yellow) capacitor voltage in phase B, Channel 2(green) capacitor voltage in phase B, Channel3 (purple) voltage between phase A and B, Channel4(blue)3phase bridge phase A gate signal.

higher amplitude of output voltage the phase shift regulation of capacitors voltage become more adequate. The amplitude of modulated output voltage is 20V so mode II altered with mode III is used. The variation in capacitors voltage does not disturb SVM so the quality of phase current is not affected. In Fig. 26 the output voltage from inverter in six step operation is presented. It is noted that capacitors voltage is kept at constant value and capacitors in phase A and B have same amplitude. The second picture shows the case where capacitors are charged to 50V and the new reference voltage of 25V has been set. The energy transfer has been accomplished by phase shift in mode II with all capacitors reaching same set point.

Power management algorithm has also been validated during motor acceleration with aims to provide smooth battery current

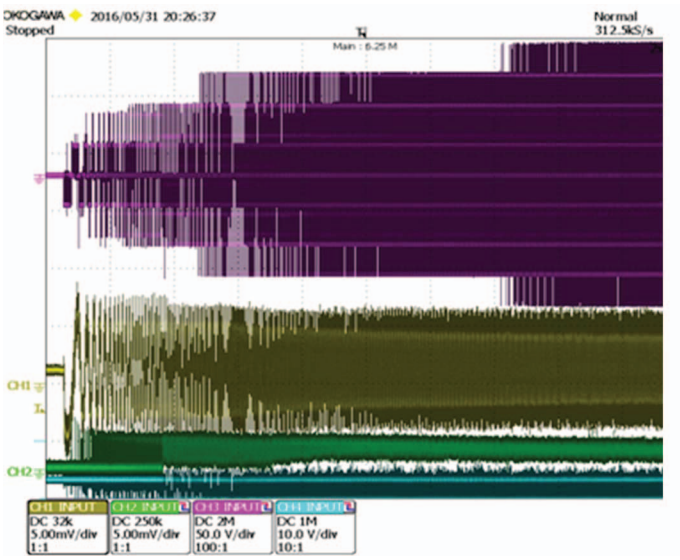

Fig. 27 Motor acceleration from 0 rpm to 200rpm with battery current limitation. Channel 1(yellow)motor phase A current; Channel 2(green) battery current; Channel3 (purple) voltage between phase A and B; Channel4(blue) 3phase bridge phase A gate signal.

rise and to avoid its average value to increase over set threshold. Fig.27 shows the profile where the motor is accelerating from zero up to 2000rpm with fully charged ultracapacitors ($V_{bat} = 2V_{uc}$). During acceleration first mode III is used to cope with initial inrush current and then gradually the three-phase bridge starts to operate (mode II with mode III). After the point where reference voltage is high enough the inverter changes the operation with three-phase bridge in six-step switching (mode II). To limit current seen by the main source, the inverter initially operates with maximum phase shift "χ" angle, and as motor current decreases the phase shift is reduced, which can be observed as reduced ripples in the main source current (green).

IV. CONCLUSION

A novel control method has been presented for the topology of a multi-level multisource inverter together with detailed analysis of its limitation. The method has been validated by experimental tests with control algorithm implemented on the C-Rio platform with FPGA. The same proved to be feasible solution for hardware implementation what provides opportunities for practical designs. From the experimental results, it is evident that the proposed system can fully utilize ultracapacitors and can increase output voltage in comparison to conventional three-phase bridges. The results also show that proposed multilevel configuration provides an effective method of power flow management between battery and UC, and is able to provide stable output during transient operation and at the same time to enhance the steady state performance of the drivetrain.

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