Optimized Active Disturbance Rejection Control for DC-DC Buck Converters With Uncertainties Using A Reduced-Order GPI Observer

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***Abstract*—The output voltage regulation problem of a PWM-based DC-DC buck converter under various sources of uncertainties and disturbances is investigated in this paper via an optimized active disturbance rejection control (ADRC) approach. Aiming to practical implementation, a new reduced-order generalized proportional integral (GPI) observer is first designed to estimate the lumped (possibly time-varying) disturbances within the DC-DC circuit. By integrating the disturbance estimation information raised by the reduced-order GPI observer (GPIO) into the output prediction, an optimized ADRC method is developed to achieve optimized tracking performance even in the presence of disturbances and uncertainties. It is shown that the proposed controller will guarantee the rigorous stability of closed-loop system, for any bounded uncertainties of the circuit, by appropriately choosing the observer gains and the bandwidth factor. Experimental results illustrate that the proposed control solution is characterised by improved robustness performance against various disturbances and uncertainties compared to traditional ADRC and integral MPC approaches.**

***Index Terms*—DC-DC buck converter, active disturbance rejection control, optimized disturbance rejection, reduced-order GPIO, circuit uncertainties and disturbances.**

I. Introduction

Rapid developments in smart grid and renewable energy favoured extensive utilisation of DC-DC buck converters in various types of dc voltage regulation, e.g. in high voltage dc (HVDC) transmission, in adapters of electric devices, in dc motor drives, in the automotive industry etc. [11]–[13]. Being one of the most crucial components in power conversion, the precision of output voltage regulation in DC-DC buck converters is of particular importance to enable satisfactory performance of connected loads or devices [1]–[3]. However, accurate control of a DC-DC buck power converter is a rather challenging design exercise due to the following two major reasons: (i) it is intrinsically a hybrid system given the frequently switching mode of the circuit, (ii) the voltage regulation is subject to undesirable effects of the various disturbances and other system uncertainties, e.g. load resistance change, input voltage variation, circuit parameter perturbation etc. [1], [14]. For example, the line voltage of HVDC transmission system is dependent of collected distributed generators and loads, which causes input voltage variation of grid connected DC-DC buck converters. Another example is the connected loads to adapters of electric devices that sometimes have different resistances [15], which is an important uncertainty factor for output voltage regulation. In addition, the magnetic characteristics of an inductor are usually nonlinear and uncertain especially under cases of large magnetic flux density in the ferromagnetic core of the converter circuit. The electro-magnetic interference produced by the switching actions of semiconductor such as switch transistors, diode, variable frequency transformer also causes external disturbances for the converter control. The various uncertainty factors inevitably degrade the quality and efficiency of power conversion, and consequently impose great challenges on higher-performance output voltage regulation of DC-DC buck converters.

Controlling such devices, Proportional-plus-Integral (PI) controllers have been traditionally utilized due to their simplicity in implementation but with limited control precision especially in the presence of large disturbances/uncertainties [15]. Advances in computational power availability of new generation of hardware devices enable practical implementation of modern advanced control approaches, i.e. sliding-mode control [5], [7], [9], [10], [14], geometric approach [8], robust control [4], [16], adaptive control [6], disturbance rejection control [15], [17], and receding optimization control [3], [18]–[20], to enhance the control performance of DC-DC buck converters. Among them, receding optimization control (ROC) has attracted considerable attention in the field of power converter control, attributed to the many advantages of its control algorithmic capacity guaranteeing optimized fast dynamic tracking responses to reference mutation, uncertain nonlinearities and undesirable disturbances [19]. Still within ROC, steady-state errors (SSE) raised by disturbances/uncertainties are addressed by employing integral action in the controller design [18]. Hence, SSE removal is realized at the price of sacrificing other control performance of the closed-loop system, due to the integral term interacting with other performance aspects such as transient behaviour, tracking, robust stability and performance [30], [31].

Therefore, it is of great importance to develop a controller that achieves optimized control performance of DC-DC power converters even in the presence of disturbances and uncertain-

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ties. A promising way to address this is by introducing an observation of disturbance into the controller design [32]. Disturbance rejection control (DRC) offers a potentially advantageous technique to obtain outstanding disturbance rejection and robustness performances in DC-DC power converters. Active DRC (ADRC) is one of the most popular DRC approaches due to its intuitive concepts and simplicity for implementation, while requiring the least amount of plant information (i.e. only the system order should be known [21]–[23]). To date, ADRC has been extensively applied to practical systems such as AC servo motors [24], MEMS gyroscopes [25], fast tool servosystems [26], robotics [27], antenna systems [28] and gasoline engines [29].

In this paper, an optimized ADRC approach is proposed for the output voltage regulation of DC-DC buck converters without adopting integral control action. Rather than utilizing traditional GPIO [24], [33], a new reduced-order GPIO is firstly constructed to estimate the state and also the time varying uncertainties and disturbances simultaneously. Both the state and disturbance estimations are then introduced for output voltage prediction via Taylor series expansion. An optimized ADRC law is finally derived by solving a receding optimization problem. The utilization of a reduced-order GPIO in the optimized ADRC design provides a current sensorless mode to address the disturbance/uncertainty attenuation problem of the DC-DC buck converter, while exhibits the following noteworthy characteristics:

1) In the best knowledge of the authors, this is the first time a rigorous stability analysis of the interconnected closed-loop of the DC-DC buck converter is presented, which ensures asymptotic stability and robust performance even in the case of both system state-dependent and control input-dependent uncertainties.
2) A novel reduced-order GPIO that is one order lower than existing GPIOs is proposed. This admits the ability to higher-order disturbance estimation, while -similar to traditional ADRC - requires limited information of model and parameters (namely only the nominal values of input voltage, filter inductance and filter capacitor utilized).
3) An optimized ADRC approach is proposed by integrating the estimates by reduced-order GPIO into output voltage prediction. The optimized tracking performance and robustness against disturbance and uncertainties performed separately by assigning optimized feedback control parameters and observer gains, respectively, which addresses the coupling between system performance and controller parameters.

The newly proposed optimized ADRC is implemented on an NI LabVIEW-based real-time control test setup for validation purposes. The experimental results illustrate that the proposed control approach exhibits superior robustness performance against various disturbances and uncertainties compared to traditional ADRC and integral MPC approaches.

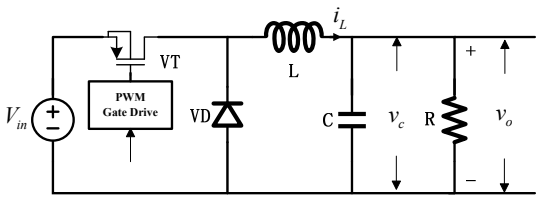

Fig. 1. The circuit diagram of a DC-DC buck converter.

II. Preliminaries

A. Dynamic Models of DC-DC Converters

A generic PWM-based DC-DC buck converter comprising a dc input voltage source V_{in}, a PWM gate drive controlled switch VT, a diode VD, a filter inductor, a filter capacitor and a load resistor is shown in Fig. 1. The dynamic model is given as

$$\begin{cases} \dfrac{dv_o(t)}{dt} = \dfrac{1}{C} i_L(t) - \dfrac{1}{CR} v_o(t), \\ \dfrac{di_L(t)}{dt} = \dfrac{1}{L}\mu(t) V_{\text{in}} - \dfrac{1}{L} v_o(t), \end{cases} \tag{1}$$

where i_L is the average input current, v_o is the average output capacitor voltage, R is the load resistance of the circuit, V_{in} is an input voltage, L is a filter inductance, C is a filter capacitor, and the duty ratio $\mu(t) \in [0, 1]$ represents the control signal. The model in (1) can be also re-arranged as follows

$$\frac{d^2 v_o(t)}{dt^2} = -\frac{1}{CR}\frac{dv_o(t)}{dt} - \frac{1}{CL} v_o(t) + \frac{V_{\text{in}}}{CL}\mu(t). \tag{2}$$

Moreover, the reference output voltage is defined as $v_r(t) = V_r$, and the output voltage tracking error is defined as $e(t) = v_o(t) - v_r(t)$.

The objective of work presented in this paper is to design an optimized ADRC algorithm such that $e(t) \to 0$ as $t \to \infty$ in the presence of various uncertainties such as load resistance changes, input voltage variations, circuits parametric uncertainties and other external disturbances.

B. Benchmark ADRCs

The nominal values of V_{in}, L and C are denoted as V_{in0}, L_0 and C_0, respectively. The DC-DC buck converter dynamics (2) are hence re-arranged as follows

$$\ddot{v}_o(t) = f(v_o(t), \dot{v}_o(t), \mu(t)) + b_0\mu(t), \tag{3}$$

where $f(v_o, \dot{v}_o, \mu) = a_1 v_o + a_2 \dot{v}_o + (b - b_0)\mu$ denotes the lumped uncertainties including variations of load resistance and input voltage, inductance and capacitance uncertainties, and other unmodeled disturbances such as EMI of the converter, with

$$b = \frac{V_{\text{in}}}{CL},\ b_0 = \frac{V_{\text{in0}}}{C_0 L_0},\ a_1 = -\frac{1}{CL},\ a_2 = -\frac{1}{CR}.$$

In the context of traditional ADRCs, an Extended State Observer (ESO) for the above converter system is designed

as [21]

$$\begin{cases} \dot{\zeta}_1 = -\iota_1(\zeta_1 - v_o) + \zeta_2, \\ \dot{\zeta}_2 = -\iota_2(\zeta_1 - v_o) + \zeta_3 + b_0\mu, \\ \dot{\zeta}_3 = -\iota_3(\zeta_1 - v_o), \\ \hat{v}_o = \zeta_1,\ \hat{\dot{v}}_o = \zeta_2,\ \hat{f} = \zeta_3, \end{cases} \tag{4}$$

where ι_i $(i = 1, 2, 3)$ are observer gains, $\hat{v}_o$, $\hat{\dot{v}}_o$ and $\hat{f}$ are estimations of v_o, $\dot{v}_o$ and f, respectively. Similarly, a traditional full-order GPIO for the converter system is designed as [24]

$$\begin{cases} \dot{\zeta}_1 = -\iota_1(\zeta_1 - v_o) + \zeta_2, \\ \dot{\zeta}_2 = -\iota_2(\zeta_1 - v_o) + \zeta_3 + b_0\mu, \\ \dot{\zeta}_3 = -\iota_3(\zeta_1 - v_o) + \zeta_4, \\ \dot{\zeta}_4 = -\iota_4(\zeta_1 - v_o), \\ \hat{v}_o = \zeta_1,\ \hat{\dot{v}}_o = \zeta_2,\ \hat{f} = \zeta_3,\ \hat{\dot{f}} = \zeta_4, \end{cases} \tag{5}$$

where ι_i $(i = 1, 2, 3, 4)$ are observer gains, $\hat{v}_o$, $\hat{\dot{v}}_o$, $\hat{f}$ and $\hat{\dot{f}}$ are estimations of v_o, $\dot{v}_o$, f and $\dot{f}$, respectively. The traditional ADRC laws based on the above two observers are generally designed as follows [21], [24]

$$\mu(t) = -\frac{1}{b_0}\left[k_1\left(v_o(t) - v_r(t)\right) + k_2\hat{\dot{v}}_o(t) + \hat{f}(t)\right], \tag{6}$$

where k_1 and k_2 are feedback control gains to be designed.

III. Optimized ADRC

A. Controller Design

1) Construction of the Reduced-Order GPIO: To enhance estimation precision and also enable easier practical implementation, a new reduced-order GPIO rather than ESO in traditional ADRC is constructed for the DC-DC buck converter as follows

$$\begin{cases} \dot{z}_2 = -\beta_1(z_2 + \beta_1 v_o) + z_3 + \beta_2 v_o + b_0\mu, \\ \dot{z}_3 = -\beta_2(z_2 + \beta_1 v_o) + z_4 + \beta_3 v_o, \\ \dot{z}_4 = -\beta_3(z_2 + \beta_1 v_o), \\ \hat{\dot{v}}_o = z_2 + \beta_1 v_o,\ \hat{f} = z_3 + \beta_2 v_o,\ \hat{\dot{f}} = z_4 + \beta_3 v_o, \end{cases} \tag{7}$$

where β_i $(i = 1, 2, 3)$ are observer gains, z_i $(i = 2, 3, 4)$ are state variables of observer, $\hat{\dot{v}}_o$, $\hat{f}$ and $\hat{\dot{f}}$ are estimations of $\dot{v}_o$, f and $\dot{f}$, respectively.

Remark 1. *It can be seen from (5) and (7) that the signals $\dot{v}_o$, f and $\dot{f}$ can be estimated by both traditional GPIO and the presented reduced-order GPIO. However, the signal $\dot{f}$ can not be estimated by the ESO in (4). Clearly, GPIOs (5) and (7) do estimate the derivative of lumped disturbances, while the ESO (4) does not. On the other hand, the order of reduced-order GPIO (7) is three, which is one order lower than the traditional GPIO (5). Such a reduced-order feature shall facilitate the practical implementation to some extent.*

Remark 2. *It is noted that there are many other types of disturbance estimators [46], such as high-gain ESO [39], [40], sliding mode disturbance observer [41], [42], disturbance observer [38], unknown input observer [43], uncertainty and disturbance estimator [44], and equivalent input disturbance-based estimator [45]. A major difference between GPIO and other types of disturbance estimators is that GPIO can estimate both the perturbations and the derivatives of the perturbations. The reason for utilizing GPIO here is that the estimate of the derivative of perturbations can be used to improve the prediction accuracy within the predictive control algorithm.*

The observer estimation errors are defined as $\varepsilon_2 = \hat{\dot{v}}_o - \dot{v}_o$, $\varepsilon_3 = \hat{f} - f$ and $\varepsilon_4 = \hat{\dot{f}} - \dot{f}$. Combining the DC-DC converter dynamics (3) with the observer dynamics (7) we have

$$\begin{cases} \dot{\varepsilon}_2 = -\beta_1\varepsilon_2 + \varepsilon_3, \\ \dot{\varepsilon}_3 = -\beta_2\varepsilon_2 + \varepsilon_4, \\ \dot{\varepsilon}_4 = -\beta_3\varepsilon_2 - \ddot{f}. \end{cases} \tag{8}$$

2) Design of Optimized ADRC: Since most optimal control approaches do not directly impose disturbance/uncertain information into the optimization problem, we utilize an output predictive approach for the development of the optimized ADRC approach. The design of the proposed approach is performed by the following three steps:

Step 1–Define of Cost Function: The cost function to be optimized for the DC-DC buck converter is defined as follows

$$\begin{aligned} J = &\frac{1}{2}\int_0^{T_P} \left[(\hat{v}_o(t+\tau) - \hat{v}_r(t+\tau))^2\right. \\ &\left. +\rho(\hat{\mu}(t+\tau) - \hat{\mu}_r(t+\tau))^2\right] d\tau, \end{aligned} \tag{9}$$

where T_P is the predictive period, $\hat{v}_o(t+\tau)$ is the predicted output voltage, $\hat{v}_r(t+\tau)$ is the desired future reference output voltage, $\hat{\mu}(t+\tau)$ is the future duty ratio to be determined, $\hat{\mu}_r(t+\tau)$ is the corresponding future duty ratio to achieve desired $\hat{v}_r(t+\tau)$, and ρ is a positive real number weighting on the control input, respectively.

Step 2–Output Voltage Prediction: Noting that the input relative degree of the DC-DC buck converter is two, the future output voltage $v_o(t+\tau)$ is predicted by Taylor series expansion

$$v_o(t+\tau) \approx v_o(t) + \tau\dot{v}_o(t) + \cdots + \frac{\tau^{2+r}}{(2+r)!}v_o^{[2+r]}(t), \tag{10}$$

where r is the control order (see [34] for detailed definition). It should be noticed that the output prediction approach in (10) is different from many existing continuous prediction approaches such as [35]–[37] in the sense that the control order r is restricted to be one therein, while could be larger than 1 for the predictive approach in this paper. This additional design of freedom increases the accuracy of prediction and the stability for higher-order nonlinear systems [34]. Define the control sequence (also known as decision variables) by

$$\hat{\bar{\mu}}(t) = \left[\hat{\mu}(t),\ \hat{\dot{\mu}}(t)\right]^\top.$$

To facilitate the implementation, we set $r = 1$ for the DC-DC buck converter here.Therefore, the estimations of higher-order derivatives of the output voltage under consideration of the disturbances are calculated by

$$\widehat{\dot{v}}_o(t) = b_0\hat{\mu}(t) + \hat{f}(t), \tag{11}$$

$$\widehat{\ddot{v}}_o(t) = b_0\hat{\dot{\mu}}(t) + \widehat{\dot{f}}(t). \tag{12}$$

Based on the estimations of $\hat{v}_o$ in (7), $\hat{\dot{v}}_o$ in (11) and $\hat{\ddot{v}}_o$ in (12), the output voltage prediction $\hat{v}_o(t+\tau)$ under the control sequence $\hat{\tilde{\mu}}(t)$ is approximated by

$$\begin{aligned}\hat{v}_o(t+\tau) =& v_o(t) + \tau\hat{\dot{v}}_o(t) + \frac{\tau^2}{2!}\hat{\ddot{v}}_o(t) + \frac{\tau^3}{3!}\hat{\dddot{v}}_o(t)\\ =& \mathcal{T}(\tau)(\hat{U}(t) + \hat{X}(t)),\end{aligned} \tag{13}$$

where

$$\mathcal{T}(\tau) = \left[1,\ \tau,\ \ \frac{\tau^2}{2!},\ \frac{\tau^3}{3!}\right],$$

$$\hat{X}(t) = \left[v_o(t), \hat{\dot{v}}(t), \hat{f}(t), \hat{\dot{f}}(t)\right]^\top,\ \hat{U}(t) = \left[0, 0, b_0\hat{\tilde{u}}^\top(t)\right]^\top.$$

Step 3–Receding Optimization: The reference signal and the control input can be written as

$$\hat{v}_r(t+\tau) = \mathcal{T}(\tau)Y_r(t), \tag{14}$$

$$\hat{\mu}(t+\tau) = \mathcal{F}(\tau)\hat{\tilde{\mu}}(t), \tag{15}$$

and

$$\hat{\mu}_r(t+\tau) = \mathcal{F}(\tau)\hat{\tilde{\mu}}_r(t), \tag{16}$$

where $Y_r(t) = [v_r(t), \dot{v}_r(t), \ddot{v}_r(t), \dddot{v}_r(t)]^\top$, $\mathcal{F}(\tau) = [1, \tau]$ and $\hat{\tilde{\mu}}_r(t) = \left[\hat{\mu}_r(t), \hat{\dot{\mu}}_r(t)\right]^\top$. According to (3), the variables $\hat{\mu}_r(t)$ and $\hat{\dot{\mu}}_r(t)$ are defined as

$$\hat{\mu}_r(t) = \frac{\ddot{v}_r(t) - \hat{f}(t)}{b_0}, \hat{\dot{\mu}}_r(t) = \frac{\dddot{v}_r(t) - \hat{\dot{f}}(t)}{b_0}. \tag{17}$$

By virtue of (13)-(16), the performance index (9) is expressed as follows

$$\begin{aligned}J =& \frac{1}{2}\int_0^{T_P}\Big[(\mathcal{T}(\tau)(\hat{X} + \hat{U} - Y_r))^2\\ &+\rho\left(\hat{\tilde{\mu}}^\top - \hat{\tilde{\mu}}_r^\top\right)\mathcal{F}^\top(\tau)\mathcal{F}(\tau)\left(\hat{\tilde{\mu}} - \hat{\tilde{\mu}}_r\right)\Big]d\tau\\ =& \frac{1}{2}(\hat{X}^\top + \hat{U}^\top - Y_r^\top)\bar{\mathcal{T}}(\hat{X} + \hat{U} - Y_r)\\ &+ \frac{1}{2}\rho\left(\hat{\tilde{\mu}}^\top - \hat{\tilde{\mu}}_r^\top\right)\bar{\mathcal{F}}\left(\hat{\tilde{\mu}} - \hat{\tilde{\mu}}_r\right),\end{aligned} \tag{18}$$

where

$$\bar{\mathcal{T}} = \int_0^{T_P}\mathcal{T}^\top(\tau)\mathcal{T}(\tau)d\tau,\ \bar{\mathcal{F}} = \int_0^{T_P}\mathcal{F}^\top(\tau)\mathcal{F}(\tau)d\tau.$$

Matrix $\bar{\mathcal{T}}$ is partitioned in the following sub-matrices

$$\bar{\mathcal{T}} = \begin{bmatrix}\bar{\mathcal{T}}_{22} & \bar{\mathcal{T}}_{21}\\ \bar{\mathcal{T}}_{21}^\top & \bar{\mathcal{T}}_{11}\end{bmatrix} \tag{19}$$

where the sub-matrices are all with dimension of 2×2. Taking partial derivative of J with respect to $\hat{\tilde{\mu}}$ gives

$$\begin{aligned}\frac{\partial J}{\partial\hat{\tilde{\mu}}} =& b_0\left[\bar{\mathcal{T}}_{21}^\top,\ \bar{\mathcal{T}}_{11}\right](\hat{X} - Y_r) + (b_0^2\bar{\mathcal{T}}_{11} + \rho\bar{\mathcal{F}})\hat{\tilde{\mu}} - \rho\bar{\mathcal{F}}\hat{\tilde{\mu}}_r\\ =& b_0\left[\bar{\mathcal{T}}_{21}^\top,\ \bar{\mathcal{T}}_{11} + \rho\bar{\mathcal{F}}/b_0^2\right](\hat{X} - Y_r) + (b_0^2\bar{\mathcal{T}}_{11} + \rho\bar{\mathcal{F}})\hat{\tilde{\mu}}\end{aligned} \tag{20}$$

Letting $\partial J/\partial\hat{\tilde{\mu}} = 0$, the optimized control law $\hat{\tilde{\mu}}^*$ is obtained from (20) given below

$$\hat{\tilde{\mu}}^* = -\frac{1}{b_0}\left[\left(\bar{\mathcal{T}}_{11} + \frac{\rho}{b_0^2}\bar{\mathcal{F}}\right)^{-1}\bar{\mathcal{T}}_{21}^\top, I_{2\times 2}\right](\hat{X} - Y_r). \tag{21}$$

Taking the first row of the optimized control law (21), the control law to be applied to the plant is given by

$$\hat{\mu}^*(t) = C_\mu\hat{\tilde{\mu}}^*, \tag{22}$$

where $C_\mu = [1, 0]$.

Since the reference voltage V_r is a constant, the resultant optimized ADRC law is given by

$$\mu^*(t) = -\frac{1}{b_0}\left[k_1\left(v_o(t) - v_r(t)\right) + k_2\hat{v}_o(t) + \hat{f}(t)\right], \tag{23}$$

where $\hat{v}_o$ and $\hat{f}$ are generated by the reduced-order G-PIO (7), and $K = [k_1,\ k_2]$ is the first row of matrix $\left(\bar{\mathcal{T}}_{11} + \frac{\rho}{b_0}\bar{\mathcal{F}}\right)^{-1}\bar{\mathcal{T}}_{21}^\top$. The following lemma plays a key role in stability analysis of the presented control approach.

Lemma 1. *The presented control law (23) with assigned control order $r = 1$ ensures that the characteristic function $P(s) = s^2 + k_2 s + k_1$ is Hurwitz stable.*

Proof: With the definition given in (23), the control gains k_1 and k_2 are calculated as

$$\begin{aligned}k_1 =& \frac{15T_p^2b_0^2(T_p^4b_0^2 + 420\rho)}{T_p^8b_0^4 + 1224\rho T_p^4b_0^2 + 15120\rho^2},\\ k_2 =& \frac{6T_p^3b_0^2(T_p^4b_0^2 + 7560\rho)}{T_p^8b_0^4 + 1224\rho T_p^4b_0^2 + 15120\rho^2}.\end{aligned} \tag{24}$$

Since both the weighting factor ρ and the prediction period T_p are positive constants, the characteristic function $P(s) = s^2 + k_2 s + k_1$ is always Hurwitz stable. This completes the proof. ■

Note that the proposed control approach needs few numerous computations for practical implementation. Indeed, the presented controller consisting of (23) and (7) is rather concise and straightforward for implementation in the sense that the control law (23) acting as a common linear feedback control law, while (7) serving as a third order linear observer. The control structure and the implementation block diagram of the proposed optimized ADRC method for DC-DC buck converter are shown in Figs. 2 and 3, respectively.

B. Stability Analysis

Combining the DC-DC buck converter dynamics (3), the observer dynamics (7), and the control law (23), the closed-loop system dynamics are governed by the following expression

$$\ddot{e} + k_2\dot{e} + k_1 e = -\varepsilon_3 - k_2\varepsilon_2, \tag{25}$$

where ε_2 and ε_3 given by (8) are state and disturbance estimation errors of the reduced-order GPIO (7), respectively.

Remark 3. *Similar to most of the existing disturbance estimator-based control approaches, see [23], [30], stability of the closed-loop system (8) and (25) could be easily established if the lumped disturbances f satisfy the condition of $\ddot{f} = 0$. However, the lumped disturbance is an uncertain function in terms of the states of the system, and rigorous stability of the closed-loop system is a rather complicated task.*

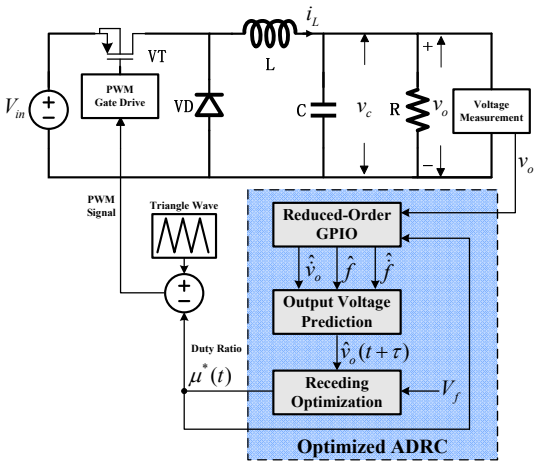

Fig. 2. The control structure of the DC-DC buck converter under the proposed optimized ADRC control approach.

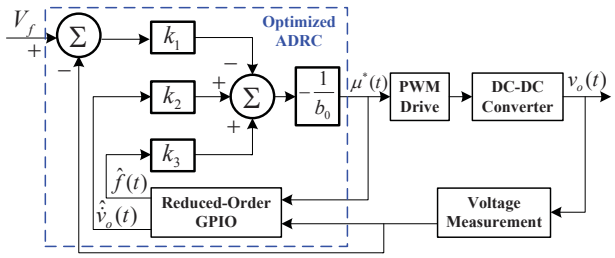

Fig. 3. The implementation block diagram of the DC-DC buck converter under the proposed optimized ADRC control approach.

In this section, we attempt to establish rigorous stability of the closed-loop system with general lumped disturbance f. The result is summarized in the following theorem.

Theorem 1. *Consider the closed-loop system consisting of the DC-DC buck converter system (1), and the proposed optimized ADRC law (23) with the reduced-order GPIO (7). The observer gains are designed as $\beta_i = \omega^i \bar{\beta}_i$ for $i = 1, 2, 3$ where $\omega > 0$ is an observer bandwidth factor to be assigned, and $\bar{\beta}_i$ is selected such that the following inequalities hold for any $\gamma_b = b/b_0 > 0$, i.e.*

$$\begin{aligned} &\bar{\beta}_1 > 0,\ \bar{\beta}_2 > 0, \\ &(2-2\gamma_b)\bar{\beta}_1\bar{\beta}_2/\gamma_b < \bar{\beta}_3 < (2-\gamma_b)\bar{\beta}_1\bar{\beta}_2/\gamma_b, \end{aligned} \tag{26}$$

The rigorous stability of the closed-loop system can be guaranteed by choosing sufficiently large observer bandwidth factor ω.

Proof: First, combining the plant dynamics (3), the observer estimation error (8) and the control law (23) with f, the dynamics of $\ddot{f}$ is governed by

$$\begin{aligned} \ddot{f} =& \delta_{e_1} e + \delta_{e_2}\dot{e} + \delta_{\varepsilon_2}(\beta_1,\beta_2)\varepsilon_2 \\ &+ \delta_{\varepsilon_3}(\beta_1,\beta_2)\varepsilon_3 + \delta_{\varepsilon_4}\varepsilon_4 + \mu_b\beta_3\varepsilon_2, \end{aligned} \tag{27}$$

where

$$\begin{aligned} \mu_b &= (b-b_0)/b_0, \\ \delta_{e_1} &= -k_1\varpi_1 + k_1k_2\varpi_2, \\ \delta_{e_2} &= -k_2\varpi_1 + (k_2^2 - k_1)\varpi_2, \\ \delta_{\varepsilon_2} &= -k_2\varpi_1 + (k_2^2 + k_2\beta_1 + \beta_2)\varpi_2 \\ &\quad -\mu_b\left(k_2(\beta_1^2 - \beta_2) - \beta_1\beta_2\right), \\ \delta_{\varepsilon_3} &= -\varpi_1 + \mu_b\left(k_2\beta_1 + \beta_2\right), \\ \delta_{\varepsilon_4} &= -\varpi_2 - \mu_b k_2, \end{aligned}$$

with $\varpi_1 = a_1 - \mu_b k_1,\ \varpi_2 = a_2 - \mu_b k_2$.

Define $\eta_2 = \omega^2\varepsilon_2$, $\eta_3 = \omega\varepsilon_3$ and $\eta_4 = \varepsilon_4$. Collecting the tracking error dynamics (25) and the observer error dynamics (8), the closed-loop system is given below

$$\begin{aligned} \dot{\xi} =& \underbrace{\begin{bmatrix} 0 & 1 \\ -k_1 & -k_2 \end{bmatrix}}_{A_\xi}\xi + \underbrace{\begin{bmatrix} 0 & 0 & 0 \\ -k_2\omega^2 & -1/\omega & 0 \end{bmatrix}}_{B_\xi}\eta, \\ \dot{\eta} =& \omega\underbrace{\begin{bmatrix} -\bar{\beta}_1 & 1 & 0 \\ -\bar{\beta}_2 & 0 & 1 \\ -\gamma_b\bar{\beta}_3 - \mu_b\bar{\beta}_1\bar{\beta}_2 & -\mu_b\bar{\beta}_2 & 0 \end{bmatrix}}_{A_\eta}\eta \\ &+ \underbrace{\begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ \tau_2(\omega) & \tau_3(\omega) & -\delta_{\varepsilon_4} \end{bmatrix}}_{E_\eta}\eta \\ &+ \underbrace{\begin{bmatrix} 0 & 0 \\ 0 & 0 \\ -\delta_{e_1} & -\delta_{e_2} \end{bmatrix}}_{B_\eta}\xi, \end{aligned} \tag{28}$$

where $\xi = [e_1, e_2]^\top = [e, \dot{e}]^\top$, $\eta = [\eta_2, \eta_3, \eta_4]^\top$, and

$$\begin{aligned} \tau_2(\omega) =& (k_2\varpi_1 - k_2^2\varpi_2 - k_2\varpi_2\omega)/\omega^2 \\ &+(\mu_b k_2\bar{\beta}_1^2 - \mu_b k_2\bar{\beta}_2 - \varpi_2\bar{\beta}_2), \\ \tau_3(\omega) =& (\varpi_1 - \mu_b k_2\bar{\beta}_1\omega)/\omega. \end{aligned}$$

With a choice of observer parameters $\bar{\beta}_i$ satisfying the inequalities (26), it can be shown that matrix A_η is Hurwitz stable, indicating that there exists a symmetric positive definite matrix P_η such that

$$A_\eta^\top P_\eta + P_\eta A = -2I_{3\times 3}. \tag{29}$$

It follows from Lemma 1 that the predictive control law (23) ensures that A_ξ is Hurwitz stable. Consequently, we also have that

$$A_\xi^\top P_\xi + P_\xi A_\xi = -2I_{2\times 2}, \tag{30}$$

where P_ξ is also a symmetric positive definite matrix.

Define a composite candidate Lyapunov function as follows

$$V(\xi,\eta) = \frac{1}{2}\xi^\top P_\xi\xi + \frac{1}{2}\eta^\top P_\eta\eta. \tag{31}$$

Taking derivative of $V(\xi,\eta)$ in (31) along the closed-loop

system dynamics (28) gives

$$\begin{aligned}\dot{V}(\xi,\eta) =& -\|\xi\|^2-\omega\|\eta\|^2+\xi^\top P_\xi B_\xi\eta\\ &+\xi^\top B_\eta^\top P_\eta\eta+\frac{1}{2}\eta^\top(E_\eta^\top P_\eta+P_\eta E_\eta)\eta\\ \le& -\|\xi\|^2-\omega\|\eta\|^2+\|\xi\|^2/4+\|P_\xi B_\xi\|^2\|\eta\|^2\\ &+\|\xi\|^2/4+\|B_\eta^\top P_\eta\|^2\|\eta\|^2\\ &+\frac{1}{2}\|E_\eta^\top P_\eta+P_\eta E_\eta\|\cdot\|\eta\|^2\\ \le& -\|\xi\|^2/2-(\omega-\omega^*)\|\eta\|^2,\end{aligned} \tag{32}$$

where ω^* is a sufficiently large positive constant regardless of ω, determined by

$$\omega^* > \|P_\xi B_\xi\|^2+\|B_\eta^\top P_\eta\|^2+\frac{1}{2}\|E_\eta^\top P_\eta+P_\eta E_\eta\|.$$

Hence, for any $\omega>\omega^*$, the following holds

$$\begin{aligned}\dot{V}(\xi,\eta) \le& -\min\left\{\frac{1}{2},\omega-\omega^*\right\}\left(\|\xi\|^2+\|\eta\|^2\right),\\ \le& -\gamma_v V(\xi,\eta),\end{aligned} \tag{33}$$

where $\gamma_v>0$ is determined by

$$\gamma_v=\frac{\min\{1,2(\omega-\omega^*)\}}{\max\{\lambda_{\max}(P_\xi),\lambda_{\max}(P_\eta)\}},$$

with $\lambda_{\min}(\bullet)$ and $\lambda_{\max}(\bullet)$ representing the minimum and maximum eigenvalues of matrix $\bullet$. This completes the proof. ■

Remark 4. *In most of existing ADRCs, the extended state observer is used to estimate the lumped disturbances including uncertainties. However, it is not clear how large amount of uncertainties can be handled by a designed ADRC law. In this paper, we propose a new approach ensuring qualitative robustness performance of the presented reduced-order GPIO-based control approach. As indicated in Theorem 1 in the paper, the qualitative relationship between controller parameters and circuit parameters ensuring stability is established.*

Remark 5. *The structure of the optimized ADRC law (23) is quite similar with the traditional ADRC law (6) with the gains k_1 and k_2 determined by the optimized design, which also indicates that the presented control law has a similar efficiency on controller operation in comparison with the traditional ADRC method. As clearly shown by (24) the optimized control gains k_1 and k_2 are functions of the predictive period T_P and control input weighting factor ρ. The purpose of the optimized design is that the parameters T_P and ρ in the performance index (9) is directly related to the tracking performance of closed-loop system. For example, the parameter T_P determines the transient performance (fast or slow), and the parameter ρ can be tuned to penalize the excessive control energy.*

Remark 6. *Theorem 1 reveals that it is necessary to assign a larger bandwidth factor ω to gain more emphasized robustness/disturbance rejection performances. However, the measurement noises will be amplified by the observer if ω is too large. Consequently, from a practical application perspective, the bandwidth factor ω of the observer should be appropriately selected to trade off between robustness/disturbance rejection performance and measurement noise attenuation. In addition, the existing noise attenuation approaches such as Kalman Filter could be combined with the presented approach to simultaneously enhance disturbance rejection and noise attenuation performances.*

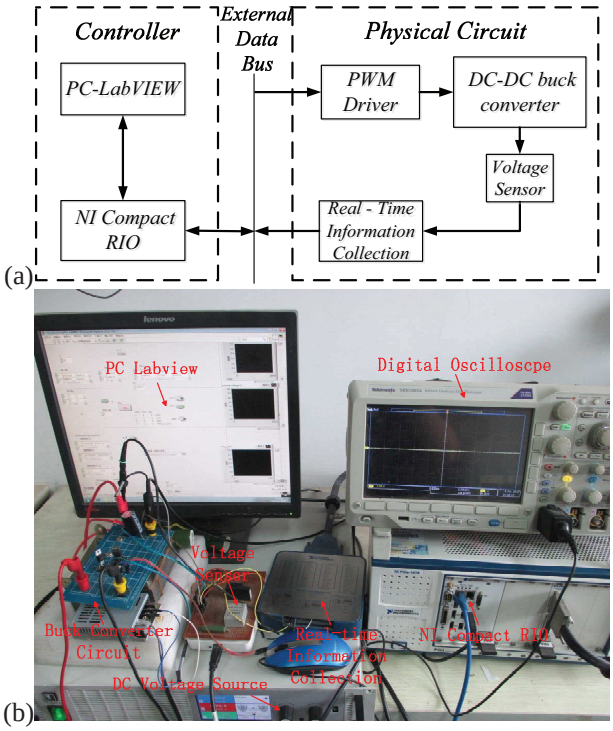

Fig. 4. (a) Configuration of experimental setup, (b) Photograph of the experimental prototype.

IV. Experimental Implementation and Performance Validation

The experimental test setup configuration and prototype are depicted in Fig. 4, comprising a DC-DC buck converter,a NI Compact RIO (embedded monitoring and control platform: NI PXIe-1078, NI R Series Multifunction RIO: NI PXI-7853R, NI LabVIEW Real-Time Module 12.0), a PC-LabVIEW2012, a programmable desktop laboratory DC power supplies (EA-PSI 9500-20 2U), a voltage sensor (VSM025A), etc. The nominal values of the parameters of the DC-DC buck converter are listed in Table I. The wordlength of the voltage AD converter is 16 Bits in the experimental test setup. The control algorithm is discretized using the basic forward difference approach. The controller updating period is 0.1 ms, and the sampling frequency for the experiment is $f_s=10$ kHz. The converter is controlled by a basic PWM gate drive; that is, the PWM driven signal is generated by comparing the duty ratio signal with a triangle wave signal. The fixed PWM switching frequency is $f_{pwm}=10$ kHz.

To evaluate the performance improvement of the proposed optimized ADRC method and enable fair comparison with conventional approaches, instead of assessing the power circuit specifications that extensively used for circuit topology and parameters design and analysis, two benchmark control

TABLE I
PARAMETERS OF THE DC-DC BUCK CONVERTER

Parameter	Symbol	Value
Input Voltage	V_{in0}	100 V
Reference Output Voltage	V_f	50 V
Inductance	L	10 mH
Capacitance	C	1000 μF
Nominal Resistance	R_0	50 Ω

approaches including traditional ADRC [21] and integral MPC [47] approaches are implemented accordingly. A tradeoff among various performances including satisfactory tracking (offset free, small overshoot, fast transient behaviour, etc.), disturbance rejection and robustness against parametric uncertainties must be taken into account when tuning the controller parameters in the paper. Consequently, fast transient performance is one of the most important control specifications but not the unique one for controller design and tuning. The fast transient behaviour can be easily achieved by assigning larger control gains for all the three controllers, however, this will inevitably degrade other control specifications such as larger overshoot, undesirable disturbance rejection and robustness performances. Since this paper is mainly concerned with disturbance rejection and robustness performance against uncertainties, our parameter tuning criterion is to assign adequate controller parameters ensuring similar satisfactory tracking performance for all the three control approaches. We then discuss and compare the disturbance rejection and robustness performance of the three control approaches. It is shown in later Figs. 5 and 6 that all the three controllers have quite similar tracking control performance. The control inputs (duty ratios) during the tracking task are quite similar as well. To this end, the controller parameters of the optimized ADRC law (23) are

$$k_1 = 4.15 \times 10^3,\ k_2 = 570,$$
$$\beta_1 = 1.2 \times 10^4,\ \beta_2 = 4.8 \times 10^7,\ \beta_3 = 6.4 \times 10^{10}.$$

The control parameters of the traditional ADRC law (with a reduced-order ESO) are

$$k_1 = 7000,\ k_2 = 300,\ \iota_1 = 8,000,\ \iota_2 = 1.6 \times 10^7.$$

The integral MPC controller parameters are

$$N_p = 75,\ N_c = 2,\ T_s = 3.53 \times 10^{-5}.$$

Then, the robustness performance of the proposed optimized ADRC method is tested for the DC-DC buck converters in the cases of various sources of disturbances and uncertainties.

A. Robustness Performance Test

1) Case I-Robustness Against Sudden Load Resistance Changes: Here the load resistance is assumed to have sudden decrease and increase during the operating process. The load resistance settings are the following

$$R = \begin{cases} 50\ \Omega\ (= R_0), & \text{for } t \in [0,\ 0.4) \text{ sec}, \\ 25\ \Omega\ (= 0.5R_0), & \text{for } t \in [0.4\ 0.8) \text{ sec}, \\ 100\ \Omega\ (= 2R_0), & \text{for } t \in [0.8,\ 1.2] \text{ sec}. \end{cases}$$

The experimental response curves of the output voltage and the duty ratio under the proposed optimized ADRC, traditional ADRC and integral MPC approaches are shown in Fig. 5.

2) Case II-Robustness Against Input Voltage Variations: Here the robustness against input voltage variations of the proposed method is tested. The input voltage is take to vary as follows

$$V_{\text{in}} = \begin{cases} 100\ V\ (= V_{\text{in0}}), & \text{for } t \in [0,\ 0.4) \text{ sec}, \\ 125\ V\ (= 1.25V_{\text{in0}}), & \text{for } t \in [0.4\ 0.8) \text{ sec}, \\ 75\ V\ (= 0.75V_{\text{in0}}), & \text{for } t \in [0.8,\ 1.2] \text{ sec}. \end{cases}$$

The experimental response curves of the output voltage and the duty ratio under the proposed controller, traditional ADRC and integral MPC control approaches are hence shown in Fig. 6.

3) Case III-Robustness Against Time-Varying Disturbances: Here we further investigate robustness against time-varying disturbances of the proposed optimized ADRC approach. A generic sawtooth waveform of time-varying disturbance is taken to acting on the input voltage of the converter system. The frequency and amplitude of the disturbances are 10 Hz and 10V, respectively. Response curves of the output voltage and duty ratio in the presence of such a time-varying disturbance via the three control approaches are shown in Fig. 7.

It can be observed from the above three cases of experimental validation that although both the traditional ADRC and integral MPC approaches could remove the offset caused by load resistance change and input voltage variations, fail to remove the offset caused by time-varying disturbances (it should be noted that integral MPC is superior than TADRC). As shown by Figs. 5-7, the proposed optimized ADRC (based on the usefulness of the ADRC method) further improves transient and static performance in the presence of various disturbances and uncertainties including load resistance changes, output voltage variations and time-varying disturbances compared to the other approaches. It is also observed from Figs. 5 and 6 that the maximum output voltage drop/raise (MOVD/MOVR) of the proposed optimized ADRC approach is lesser than those provided by the traditional ADRC and integral MPC methods. Similarly, the recovery time after sudden load changes and input voltage variations of the optimized ADRC method is much shorter than those of the other two approaches. For completeness the performance indices (MOVD, MOVR, maximum recovery time (MRT) and integral of absolute error (IAE)), comparison among the three control approaches is shown in Table II.

B. Adaptive Capacity Verification

Here the adaptive capacity of the proposed optimized ADRC with respect to various load resistance change and input voltage variations is investigated. The response curves of the output voltage under the three controllers in the presence of different load resistance changes and input voltage variations are shown by Fig. 8 and Fig. 9, respectively.

The results shown in the aforementioned figures illustrate that the output voltage responses of the proposed optimized ADRC approach (which inherits good properties of traditional

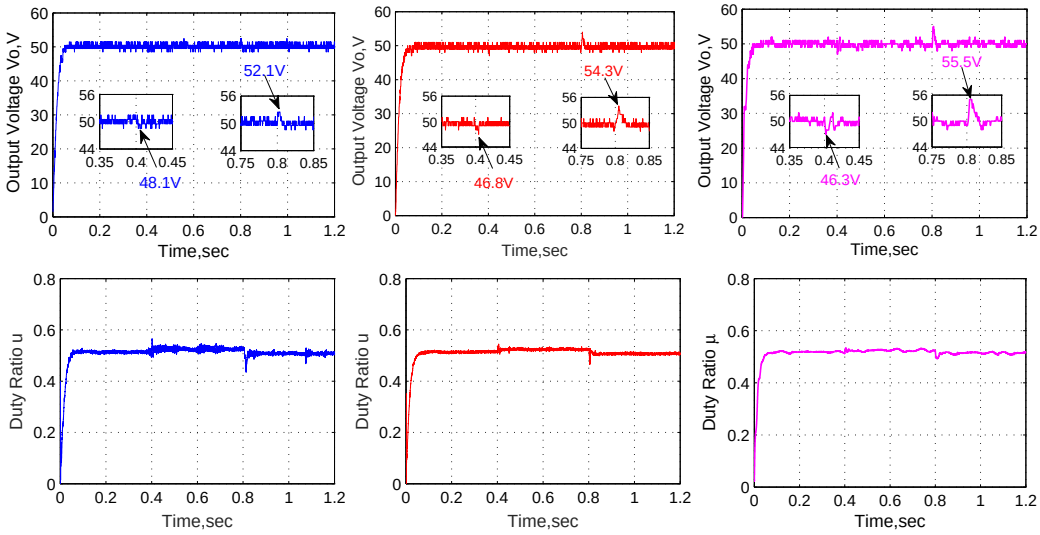

Fig. 5. Variable response curves of DC-DC buck converter via optimized ADRC (left), traditional ADRC (middle) and integral MPC (right) control, in the presence of sudden load resistance changes (top: o/p voltage; bottom: duty ratio).

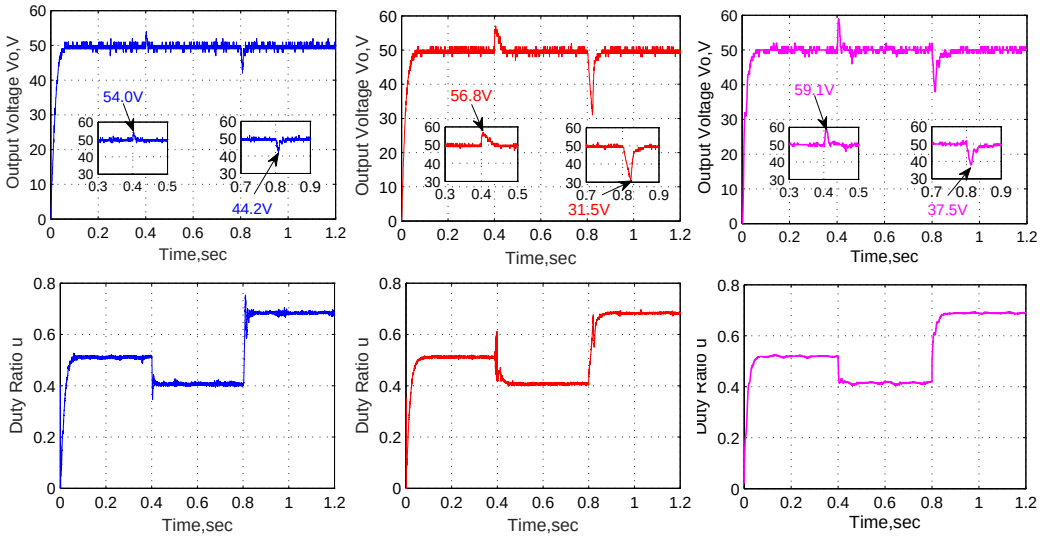

Fig. 6. Variable response curves of DC-DC buck converter under the optimized ADRC (left), traditional ADRC (middle) and integral MPC (right) control, in the presence of sudden input voltage variations (top: o/p voltage; bottom: duty ratio).

TABLE II
EXPERIMENTAL PERFORMANCE INDICES OF OPTIMIZED ADRC (OADRC), TRADITIONAL ADRC (TADRC) AND INTEGRAL MPC CONTROLLER

Test Type	Performance	Controllers		
		OADRC	TADRC	Integral MPC
Case I	MOVR (V)	2.1	4.3	5.5
	MOVD (V)	1.9	3.2	3.7
	MRT (sec)	0.0064	0.0188	0.0350
	IAE (V)	0.5988	0.6564	0.6030
Case II	MOVR (V)	4.0	6.8	9.1
	MOVD (V)	5.8	18.5	12.5
	MRT (sec)	0.0292	0.0716	0.0862
	IAE (V)	0.234	0.4412	0.6200
Case III	IAE (V)	1.3844	4.396	2.8850

ADRC) under the given variations offers an almost flat response in all cases. This illustrates the efficacy of the adaptive capacity of the proposed control solution.

V. CONCLUSION

The work in this paper has addressed the current sensorless optimized ADRC design problem for a generic DC-DC buck converter subject to multiple sources of disturbances including load resistance mutation, input voltage variation, etc. To facilitate practical implementation, a novel reduced-order GPIO has been proposed for the involved lumped time-varying disturbance estimation. Moreover, disturbance estimations have been incorporated into the output voltage prediction process largely improving the output prediction accuracy. Different from most of existing disturbance estimator-based control approaches,

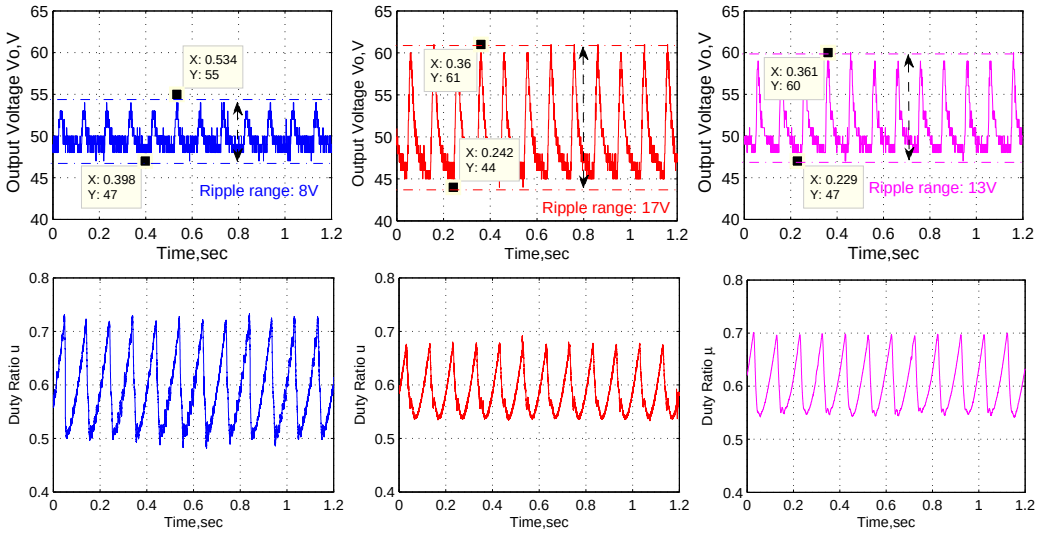

Fig. 7. Variable response curves of DC-DC buck converter under the optimized ADRC (left), traditional ADRC (middle) and integral MPC (right) control, in the presence of time-varying disturbances (top: o/p voltage; bottom: duty ratio).

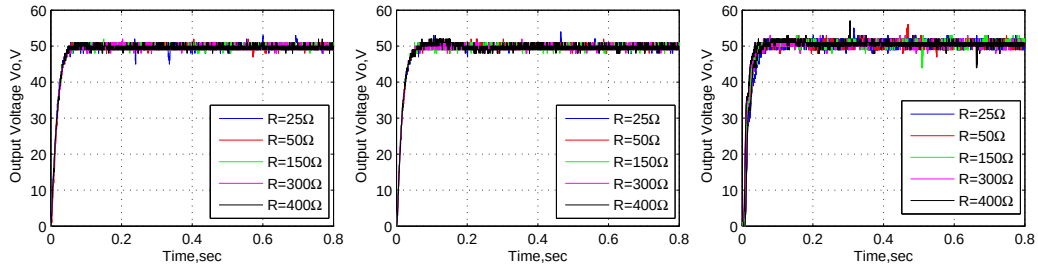

Fig. 8. Output voltage response curves of DC-DC buck converter in the presence of various load resistance changes under the optimized ADRC (left), traditional ADRC (middle) and integral MPC control (right) approaches.

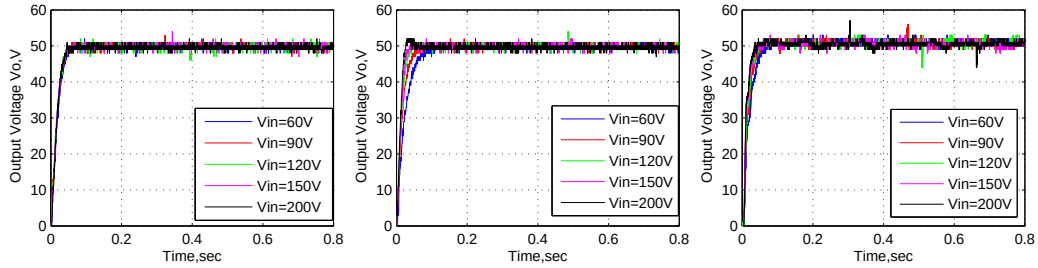

Fig. 9. Output voltage response curves of DC-DC buck converter in the presence of various input voltage variations under the optimized ADRC (left), traditional ADRC (middle) and integral MPC (right) control approaches.

including traditional ADRC, a rigorous analysis on robustness stability has been provided for the proposed optimized ADRC method. The experimental results on the power converter have shown that overall the proposed optimized method outperforms both traditional ADRC and integral MPC approaches in the presence of various disturbances and uncertainties.

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