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Fault detection for Modular Multilevel Converters Based on Sliding Mode Observer

Shuai Shao, Patrick W. Wheeler, *Member, IEEE*, Jon C. Clare, *Senior Member, IEEE*, and Alan J. Watson, *Member, IEEE*

Abstract—This letter presents a fault detection method for modular multilevel converters (MMC) which is capable of locating a faulty semiconductor switching device in the circuit. The proposed fault detection method is based on a sliding mode observer (SMO) and a switching model of a half-bridge, the approach taken is to conjecture the location of fault, modify the SMO accordingly and then compare the observed and measured states to verify, or otherwise, the assumption. This technique requires no additional measurement elements and can easily be implemented in a DSP or micro-controller. The operation and robustness of the fault detection technique are confirmed by simulation results for the fault condition of a semiconductor switching device appearing as an open-circuit.

Index Terms—Fault detection, modular multilevel converter, sliding mode observer, switching model.

I. INTRODUCTION

THE modular multilevel converter (MMC) has drawn considerable interest, as it offers very attractive features [1]–[4].

- Modular construction with scalable, manufacturable, standardised cells (half-bridge).
- Submodules are fed by floating DC capacitors, no multi-pulse transformer is required.
- High power and high voltage capability, extendable by adding additional cells.
- Flexible control of the voltage level and simple realization of redundancy if required.

Fault detection is an important issue for a MMC. When an open-circuit fault occurs, the output voltage and current are distorted, moreover, the voltages of the DC floating capacitors will keep increasing, leading to further, vast destruction. Therefore, it is vital to locate the fault after its occurrence and take measures such as bypassing the faulty cell to reconfigure the MMC.

Given the large numbers of identical cells (half-bridge) and the symmetrical structure of the converter, the process of fault location in a MMC is challenging if significant extra cost is to be avoided. An effective but inefficient way to detect faults is to add additional sensors to each semiconductor switching device [5], to each cell [6], or to use a gate drive module capable of detecting faults and providing feedback [7]. These

additional sensors and signals increase not only the cost but also the implementation complexity. Some conventional fault detection methods for voltage source converters (VSCs), such as the calculation of the output current trajectory using Park's Vector [8] [9] or comparison of the actual AC voltage and the reference quantity [10] are however not suitable for a MMC, as there is not enough information present to locate the fault.

Fault diagnosis methods for a cascaded H-bridge (CHB) are applicable to a MMC because of the similar structure. Reference [11] presented a detection approach for a CHB multilevel converter, which analyses magnitude of the switching frequency component (v_s) of the output phase voltage: v_s becomes significantly larger after the occurrence of a fault due to the imbalanced cancellation of the switching frequency harmonics. The faulty cell can be located according to the angle of v_s [11]. However, the faulty switching device cannot be located, and it is complex to implement and easy to get the wrong diagnosis in transient operation. In [12] the authors proposed an artificial intelligence (AI) based algorithm to detect the fault of a CHB, the major drawbacks are the accuracy (only 76% in some cases) and the long training time required for the circuit and all the fault scenarios.

This paper proposes a sliding mode observer (SMO) based fault detection method for a MMC. The method uses the converter arm currents and the cell capacitor voltages as the inputs, which are already available as measurement inputs to the control system, no additional sensors are required. Using this method not only the faulty cell, but also the faulty switching device can be located. Moreover, inherited from the easy implementation and robustness of the SMO [13]–[15], this method has good immunity to conditions such as transient operation, degradation of capacitance over time and measurement inaccuracies.

II. SWITCHING MODEL OF A HALF-BRIDGE

A half-bridge (Fig. 1) is the basic cell of a MMC. In order to diagnose an open-circuit fault, it is essential to identify the characteristics of a half-bridge as observed from its DC-side and AC-side both in normal and fault conditions.

g_1 and g_2 in Fig. 1 are the gate signals for the switches, and are complementary. When the gate signal is 1, the corresponding switch turns on; when it is 0, the corresponding switch turns off.

The analysis assumes ideal devices and instantaneous commutation. The fault detection method is however robust against non-ideal device characteristics. This is verified in the all of

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The authors are with the Power Electronics, Machines and Control Group, School of Electrical and Electronic Engineering, University of Nottingham, Nottingham, NG7 2RD, U.K. (e-mail: eexs21@nottingham.ac.uk; Pat.Wheeler@nottingham.ac.uk; Jon.Clare@nottingham.ac.uk; Alan.watson@nottingham.ac.uk).

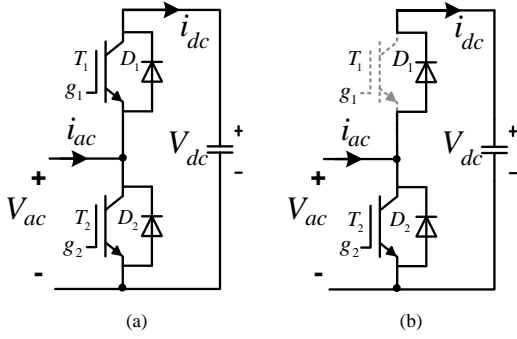


Fig. 1: Switching model of half-bridge. (a)Normal condition. (b)Fault condition (an open-circuit fault at T_1).

the simulation results where generous values of $5V$ and $1\mu s$ are included for the device voltage drop and dead-time delay respectively.

1) *Normal (fault-free) condition:* As shown in Fig. 1(a), when $g_1 = 1, g_2 = 0$, T_1 is on and T_2 is off, thus $V_{ac} = V_{dc}, i_{dc} = i_{ac}$; alternatively, when $g_1 = 0, g_2 = 1$, $V_{ac} = 0, i_{dc} = 0$. Therefore, the relationship between the AC-side and DC-side voltages and currents can be calculated as

$$\begin{cases} V_{ac} = S \cdot V_{dc} \\ i_{dc} = S \cdot i_{ac} \end{cases}, \quad (1)$$

where S is the switching state given by Table I.

TABLE I: Switching state S in normal condition

S	Driving signals
1	$g_1 = 1, g_2 = 0$
0	$g_1 = 0, g_2 = 1$

2) *Fault condition:* In the fault condition (one open-circuit fault of the switch), the switching models can still be described as (1), but the switching states S have to be modified.

Consider the half-bridge with an open circuit fault at T_1 , as shown in Fig. 1(b). When $g_1 = 1, i_{ac} < 0$, i_{ac} is forced to go through D_2 instead of T_1 as the result of the open-circuit fault. Thus, the switching state S should be changed from 1 to 0. For all other conditions, the half-bridge operates just as normal.

When the open-circuit fault occurs on T_2 , the switching state can be modified in a similar way. Table II demonstrates the modifications of switching states of a faulty half-bridge.

TABLE II: Switching state S in fault condition

Location of the fault	Condition	Switching State	
		Normal	Fault
T_1	$g_1 = 1, i_{ac} < 0$	1	$S_F = 0$
	Other conditions	S	$S_F = S$
T_2	$g_2 = 1, i_{ac} > 0$	0	$S_F = 1$
	Other conditions	S	$S_F = S$

III. SLIDING MODE OBSERVER

An observer is a contrivance designed from a real system, generally in the same mathematical form as the original system, so as to estimate its internal state [13] [16]. The SMO uses high-gain feedback in the observer vector (normally in the form of a high frequency switching function, for example the saturation function of an observed-measured error, as (3) and (4) present) to force the observed output to converge to the actual output [13] [15]. The SMO offers desirable features such as robustness to parameter uncertainty and insensitivity to measurement noise [13]–[15], [17]. With simple realization, the SMO can be implemented in the FPGA [16] [17].

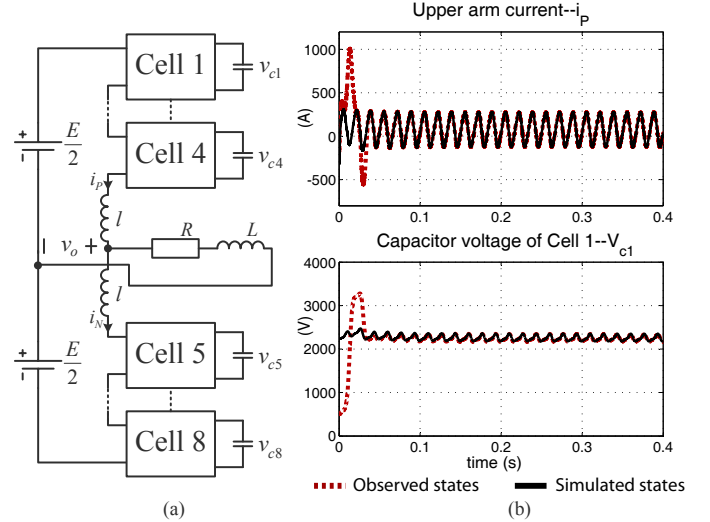


Fig. 2: (a) An eight cell MMC circuit (each cell represents a half-bridge). (b) SMO simulated results in normal conditions.

Based on [16] [18], the SMO can be developed for a single phase eight cell MMC as shown in Fig. 2(a). The equations which characterize the upper arm can be expressed as

$$\frac{di_p}{dt} = -\frac{1}{l} (S_1 v_{c1} + S_2 v_{c2} + S_3 v_{c3} + S_4 v_{c4} + v_o - \frac{E}{2}) \quad (2)$$

$$\frac{dv_{ci}}{dt} = \frac{1}{C} S_i i_p \quad (i = 1, 2, 3, 4),$$

where l is the arm inductance, as shown in Fig. 2(a), C is the DC-capacitance, v_{c1}, \dots, v_{c4} are the capacitor voltages of cell 1 to cell 4 respectively, S_1, \dots, S_4 are the corresponding switching states of the half-bridges given by Table I.

If i_p and one of the capacitor voltages (v_{c1}, \dots, v_{c4} , we consider v_{c1} in this case) are selected to be observed, then the SMO equation is

$$\frac{d\hat{i}_p}{dt} = -\frac{1}{l} (S_1 \hat{v}_{c1} + S_2 v_{c2} + S_3 v_{c3} + S_4 v_{c4} + v_o - \frac{E}{2}) - L_1 \text{sat}(\hat{i}_p - i_p) \quad (3)$$

$$\frac{d\hat{v}_{c1}}{dt} = \frac{1}{C} S_1 \hat{i}_p - L_2 \text{sat}(-L_1 L_1 \text{sat}(\hat{i}_p - i_p)),$$

where \hat{i}_p and \hat{v}_{c1} denote the observed states associated with the actual states i_p and v_{c1} ; $L_1 \text{sat}(\hat{i}_p - i_p)$ and

$L_2 \text{sat}(-lS_1 L_1 \text{sat}(\hat{i}_P - i_P))$ comprise the observer vector, whose derivations are detailed in [16] [18]; L_1 and L_2 are the observer gains (large constant, for example 20000) to guarantee the sliding mode; $\text{sat}(x)$ is the saturation function, which is defined as

$$\text{sat}(x) = \begin{cases} 1 & x \geq 1 \\ x & -1 < x < 1 \\ -1 & x \leq -1 \end{cases} \quad (4)$$

According to the analysis of [16], the system described in (3) is fully observable.

The MMC circuit is simulated using SIMULINK/PLECS. The observed and actual simulated states are shown in Fig. 2(b), from which one can see that \hat{i}_P and \hat{v}_{c1} accurately match i_P and v_{c1} respectively. The lower arm current and capacitor voltage can be observed in the same way.

IV. FAULT DETECTION ON A MMC USING SLIDING MODE OBSERVER

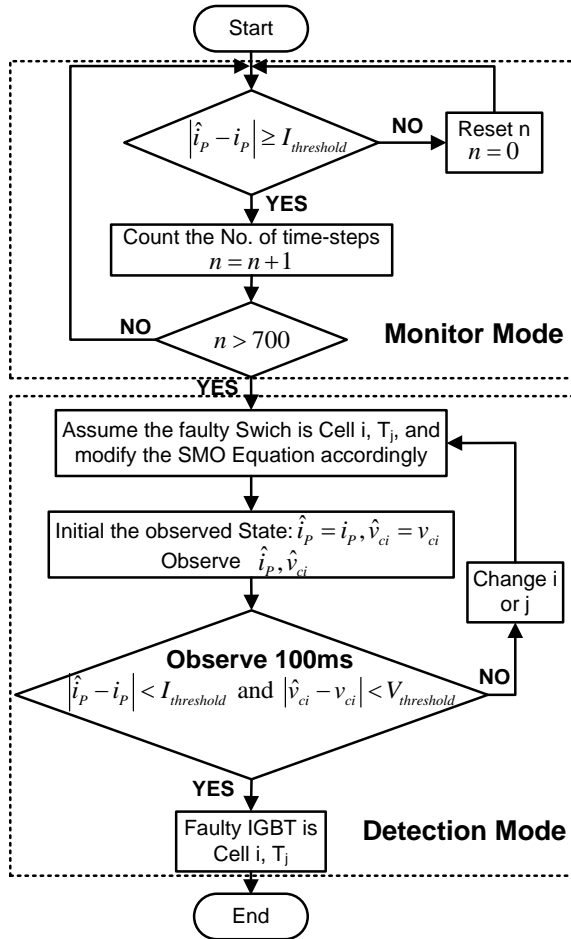


Fig. 3: Flow chart of the fault detection.

The basic idea of this detection method is to compare the observed state and the actual simulated state of the MMC, and if they are different for a predefined period of time, then a fault has occurred, and a procedure including assumption, modification and judgement to locate the open-circuit fault begins.

The fault detection systems consists of two modes, as specified in Fig. 3. The process of each mode is detailed as follows. Consider the upper arm of the MMC circuit in Fig. 2(a), and suppose that it initially operates in normal, steady conditions.

Monitor mode: The aim of this mode is to determine whether the MMC is operating normally. i_P and one of the any capacitor voltages (for example v_{c1}) are observed.

If $|\hat{i}_P - i_P| \geq I_{Threshold}$, where $I_{Threshold}$ is the threshold value of current error, and it lasts for 700 time steps ($2\mu s$ per step), then an open-circuit fault has occurred. We denote this moment as t_0 and go to the *Detection mode*; else, repeat the *Monitor mode*. Note that the decision of fault occurrence is made only if the observed-simulated error ($|\hat{i}_P - i_P|$) lasts for a period of time (700 time-steps in this letter, empirical value), this is useful to prevent "false positives", as the measurement noise may also lead to $|\hat{i}_P - i_P| \geq I_{Threshold}$.

Detection mode: The aim of this mode is to locate the open-circuit after its occurrence.

D1. [Assumption and Modification] Set the assumed faulty switch as *Cell* i ($i = 1, 2, 3, 4$), T_j ($j = 1, 2$), modify S_i (replace S with S_F) of SMO in (3) based on the Table II, set $\hat{i}_P(t_0) = i_P(t_0)$, $\hat{v}_{ci}(t_0) = v_{ci}(t_0)$, and observe i_P and v_{ci} . For example, if the assumed faulty switch is *Cell* 4, T_1 , then i_P and v_{c4} are observed, and the observer equations are

$$\begin{aligned} \frac{d\hat{i}_P}{dt} &= -\frac{1}{l} (S_{4(F)}\hat{v}_{c4} + S_1v_{c1} + S_2v_{c2} + S_3v_{c3} + \\ &\quad v_o - \frac{E}{2}) - L_1\text{sat}(\hat{i}_P - i_P) \\ \frac{d\hat{v}_{c4}}{dt} &= \frac{1}{C} S_{4(F)}\hat{i}_P - L_2\text{sat}(-lS_{4(F)}L_1\text{sat}(\hat{i}_P - i_P)). \end{aligned} \quad (5)$$

D2. [Judgement] If $|\hat{i}_P - i_P| < I_{Threshold}$ and $|\hat{v}_{ci} - v_{ci}| < V_{Threshold}$, where $V_{Threshold}$ is the threshold value of voltage error, and it lasts for 100ms (empirical value), then the assumption is correct—the faulty switch is *Cell* i ($i = 1, 2, 3, 4$), T_j ($j = 1, 2$); else alter i or j , go to *D1* to try another switch.

Note that the threshold value ($I_{Threshold}$ and $V_{Threshold}$) are chosen in such a way that the observed-simulated error ($|\hat{i}_P - i_P|$ and $|\hat{v}_{ci} - v_{ci}|$) are significant enough to allow a decision to be made with low risk of "false positive". In this letter, $I_{Threshold}$ is the peak value of the arm current, and $V_{Threshold}$ is 1/10 of the DC capacitor voltage.

The Detection mode can be executed in parallel for each cell, such that the open-circuit fault can be located within a very short time.

V. SIMULATED RESULTS

Consider an open-circuit fault occurring at *Cell* 4, T_1 at $t = 0.1s$, as illustrated in Fig. 4 (a).

Firstly, Fig. 4 (b) shows that if no fault detection algorithm is applied, the observed states cannot follow the actual simulated states after the occurrence of the open-circuit fault. One can see that \hat{i}_P and \hat{v}_{c1} cannot track i_P and v_{c1} after $t = 0.1s$.

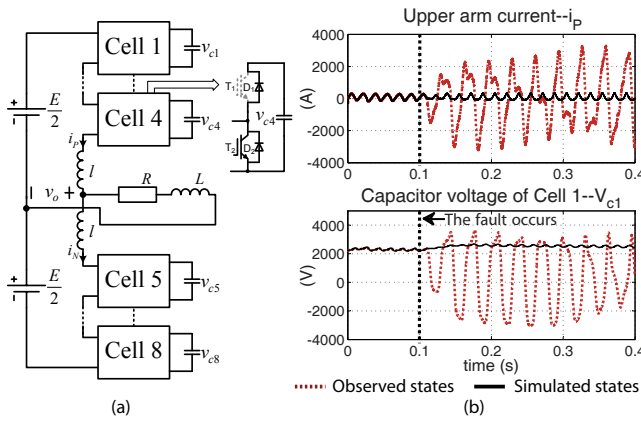


Fig. 4: (a)An open-circuit fault occurs at *Cell 4, T₁*. (b) Observed and actual simulated states without using the fault detection algorithm.

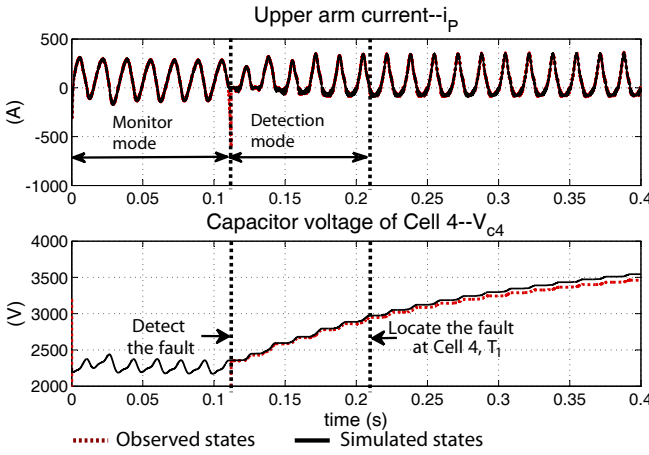


Fig. 5: Fault detection process: assume the faulty switch is *Cell 4, T₁*.

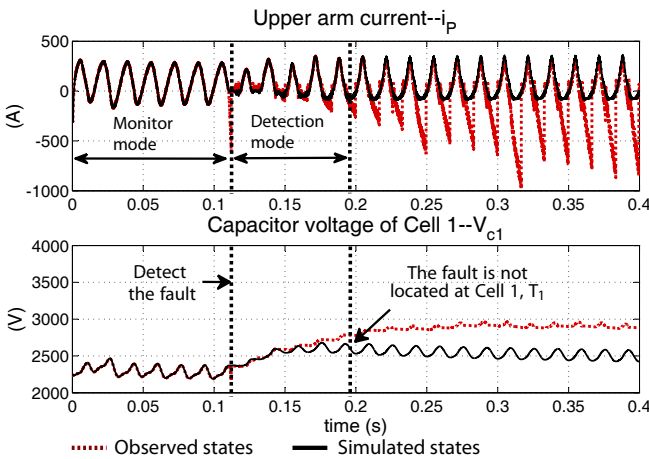


Fig. 6: Fault detection process: assume the faulty switch is *Cell 1, T₁*.

Secondly, Fig. 5 and Fig. 6 illustrate the process of the fault detection. In the monitor mode (0 to 0.1s), the observed current \hat{i}_P can follow the simulated current i_P , as shown in both

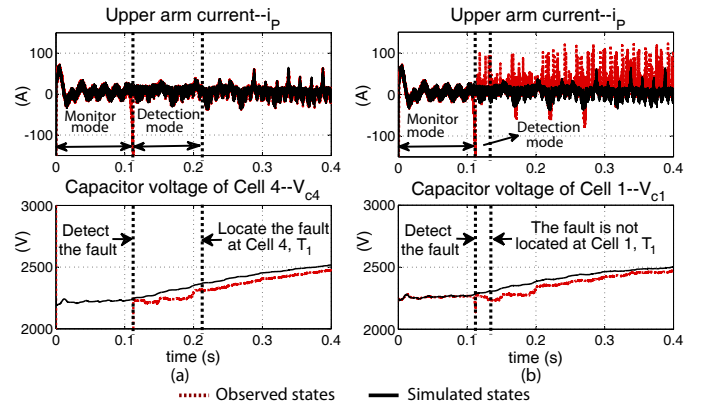


Fig. 7: Fault detection at the 5% load condition.

Fig. 5 and Fig. 6. After 0.1s, the occurrence of the open-circuit fault is detected with the condition $|\hat{i}_P - i_P| \geq I_{Threshold}$, and the algorithm enters into the detection mode. In Fig. 5, the assumed the faulty switch is the actual one—*Cell 4, T₁*. It can be seen that the observed states \hat{i}_P and \hat{v}_{c4} can track i_P and v_{c4} again. In Fig. 6, the assumed faulty switch is *Cell 1, T₁*. The observed states \hat{i}_P and \hat{v}_{c1} cannot track the simulated states i_P and v_{c1} after the modification, and it can be judged that the faulty switch is not *Cell 1, T₁* as $|\hat{v}_{c1} - v_{c1}| > V_{Threshold}$ within 100ms.

Finally, the light load condition is considered. At the 5% load, when the assumed faulty switch is the actual one—*Cell 4, T₁*, the observed states can follow the actual states, as shown in Fig. 7 (a); when the assumed faulty switch is not the actual one, a significant difference between observed and simulated current ($|\hat{i}_P - i_P| > I_{Threshold}$) is appeared soon after the algorithm enters into the Monitor Mode, as shown in Fig. 7 (b). The open-circuit fault can still be located at the light load condition.

VI. ROBUSTNESS

The proposed SMO-based fault detection method has immunity to the parameter uncertainty, measurement inaccuracy and imbalanced voltage. A simulation has been undertaken to demonstrate these properties, and part of the simulation parameters have been amended as follows to imitate the parameters and measurement errors and the imbalanced capacitor voltage. Other conditions are the same as the ones in Section V.

- *Parameter uncertainty.* Let the arm inductance used in the calculation be 110% of the actual value, and the DC-capacitance 120% of the actual value, namely, $l_{cal} = 1.1l$, $C_{cal} = 1.2C$.
- *Measurement inaccuracy.* Add 2% of the systematic error (Δ_S) and 10% of the random error (Δ_R) to the measured capacitor voltage, namely, $v_{ci_cal} = (1 + \Delta_S + \Delta_R) \cdot v_{ci}$.
- *Imbalanced capacitor voltage.* Let $V_{c1} = 1.25V_{c4}$ before the occurrence of the open-circuit fault.

The results are illustrated in Fig. 8 and Fig. 9. In the monitor mode (0 to 0.1s), the observed current can still track the simulated current. One can also notice that the capacitor

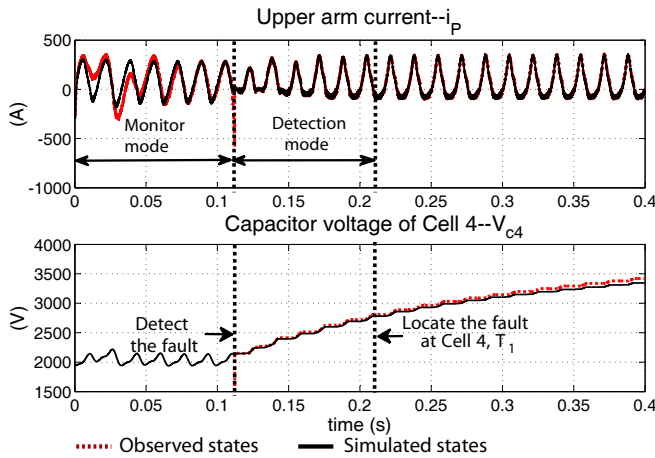


Fig. 8: Robustness test: assume the faulty switch is *Cell 4, T₁*.

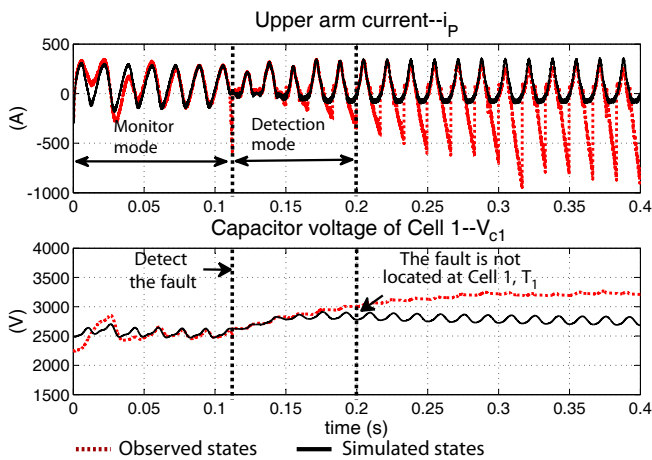


Fig. 9: Robustness test: assume the faulty switch is *Cell 1, T₁*.

voltage is imbalanced during this period: v_{c1} in Fig. 9 is 1.25 times the value of v_{c4} in Fig. 8. In regard to locating the fault (after 0.1s), when the assumed switch is the actual faulty one, the observed states \hat{i}_p and \hat{v}_{c4} can track i_p and v_{c4} , as Fig. 8 presents; whereas the assumed switch is not the actual one, the observed \hat{i}_p and \hat{v}_{c1} cannot match i_p and v_{c1} , as Fig. 9 illustrates. In the presence of parameter uncertainty and measurement noise and imbalanced capacitor voltage, the faulty switch can still be located.

VII. CONCLUSION

This paper proposes a SMO-based fault detection method for a MMC. Simulations, which include device voltage drops and commutation delays, have shown that it is effective in locating the faulty switch and very robust against both parameter uncertainty and measurement error. This method is also independent of operation frequency of a MMC. With parallel execution, the open-circuit fault can be located within a very short time. The accuracy of the measurement may limit the application of this method—it is not able to locate the fault when the systematic measurement error is larger than 7%.

Construction of experiments is currently underway, the SMO is going to be implemented in the ACTEL A3P400

FPGA, while the control system and the fault detection algorithm will be carried out in the TMS320C6713 DSP, this is similar to the approaches taken in [17] and [18].

This method can also be used on any other multilevel half or full bridge converters.

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